INTERSIL

DATA BOOK 1981

ABOUT OUR COVER

We, at Intersil, believe in using the wisdom of the past to help turn today's ideals into tomorrow's realities. This policy is reflected in our advertising posters, each of which shows one of history's great thinkers.

A copy of one or all of the posters is yours for the asking. See the back of this Product Guide for offer details.

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INTERSIL — A VIEWPOINT

Intersil is ranked among the ten largest independent manufacturers of semiconductors in the United States. The present Intersil is the result of a 1976 merger between Intersil, Inc., a major supplier of semiconductor devices, and Advanced Memory Systems (AMS), a leading source of add-on and add-in memories for computers and computer-related equipment. This strength was further augmented in 1979 by the acquisition of Datel Systems, Inc., a company widely known for superior data acquisition products and systems.

Intersil employs over 4000 people in its three operating divisions (Semiconductor, Memory Systems and Datel-Intersil) and carries out product development and manufacturing activities at plants in Cupertino, Santa Clara and Sunnyvale, California; Mansfield, Massachusetts; Bombay, India; and Singapore. The company produces analog and digital integrated circuits, using CMOS/LSI, MOS/LSI, low-power CMOS, and bipolar LSI technologies. Applications and markets include data acquisition and processing, industrial process control, portable and fixed instrumentation, RF and telecommunications, data conversion, and horological equipment.

Intersil's Systems Division is a major manufacturer of add-on memories for upgrading IBMs 370, 360 and 303XX series of computer mainframes, and to date has shipped and installed more than five billion bytes of semiconductor memory. The group also manufactures a line of standard and custom microsystems and memory expansion boards for numerous micro and minicomputer applications.

Significant new semiconductor products introduced in 1980 include:

☐ IVN6000K Series Vertical Power FETs—A proprietary double-diffusion planar process yields vertical power MOS FETs with breakdown voltage ratings as high as 450V. Unique geometry of the IVN6000 series provides for low ON resistance and high current density. Devices can switch in 10 ns, ten times faster than other DMOS power transistors on the market.

☐ ICL7660 Voltage Converter—A unique CMOS chip which converts positive voltage to negative voltage with 99.9% accuracy ($R_L = 55\Omega$). Power conversion efficiency is 98% and I_{OUT} is greater than 40 mA. Solves the problem of providing a second power supply, and can be cascaded or paralleled for greater negative voltages or more current.

☐ ICL7650 Ultra-Stable Op Amp—Very nearly the "universal" op amp, in terms of error-free operation, low power consumption, DC stability and input offset voltage. Long-term drift with temperature is only 0.01 μV/°C over the full temperature range. DC input bias current is only 10 pA, and gain, CMRR and PSRR are extremely high—in excess of 130 dB. High slew rate is 2.5V/μs. Gain-bandwidth product is 2 MHz. Needs no trimming potentiometer to maintain stability. Phase error is less than 10°.

☐ 82HM Series High-Speed ROMs—An attractive alternative to the hard-to-get bipolar 82S series PROMs; pin-for-pin replacements, but with better delivery time and better prices. HMOS process provides high reliability and cost effectiveness.

Available ROMs include:

82HM137 (1K x 4)
82HM141 (512 x 8)
82HM181 (1K x 8)
82HM185 (2K x 4)
82HM191 (2K x 8)

Access times are 60 ns for the 137 and 141, 70 ns for the 181 and 185, and 80 ns for the 191.

☐ ICM7240/50/60 CMOS Programmable Timer/Counters—A family of RC oscillators/timers/counters with selectable output counts from RC to 255 RC. High frequency operation to 13 MHz. Timing may be programmed from microseconds to days, and counting modes can be straight binary or decimal.

☐ ICL7126 Micropower 3½-Digit A/D Converter—A CMOS chip which includes all active devices needed for direct LCD interface, including seven segment decoders, direct display drivers, reference and clock. Capable of operation for as long as 9000 hours—nearly a year—on a single 9V battery. High-accuracy features include auto-zero to less than 10 μV, zero drift of less than 1 μV/°C, input bias current of 10 pA max, and rollover error of less than one count.

☐ ICM7236 4½-Digit VF Counter-Driver—New low-power CMOS up-counter with static drivers for vacuum fluorescent displays. High-performance device includes decoders, output latches, count inhibit, reset and leading-zero blanking on a single chip. For fast counting, 15 MHz is guaranteed and 25 MHz is typical. Maximum count to 19999. Typical power consumption is 10 μA.

☐ IM80C48/IM80C35 CMOS Microprocessor—An 8-bit single-chip microprocessor which is pin and function compatible with the NMOS 8048/8035 while offering the inherent low power dissipation and excellent noise immunity typical of CMOS. Power dissipation with a 6 MHz crystal (3 MHz internal clock) is less than 55 mW. The devices also feature a power-down mode which retains RAM data integrity.

☐ ICM7235 4½-Digit VF Display Decoder/Driver—A single-chip interface between microprocessors and non-multiplexed 7-segment vacuum fluorescent displays. Available with multiplexed BCD input for digital logic interface, or with high-speed μP interface, and in hexadecimal (0-9, A-F) or Code B (0-9, dash, E, H, L, P, blank) outputs. The CMOS device features display blanking, static discharge protection, brightness control and low power consumption.

Intersil's full range of quality integrated circuits and discrete devices is available through a world-wide network of stocking distributors. Field sales offices are located in all major market areas of the United States and Canada to provide a high level of product support. A complete listing of these distributors, Sales Representatives and Company Sales Offices is included at the end of this publication.

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HOW TO USE THIS PUBLICATION

BASE NUMBER INDEX

If only the basic part number is known, use the Base Number Index as a locator aid. The Base Number Index is organized in alpha-numeric sequence, with prefix letters appearing in bold type. Devices are arranged in this index according to the numeric value of the first digit on the left, then the value of the second digit, then the third, and so on. For example, device number ICM7218 precedes ICL741. No package/temperature/pin number suffixes are included, but may be obtained from the specific product data sheet.

FUNCTIONAL INDEX

This is an index of Intersil device types categorized by product grouping and function. The first major subsection, DISCRETES, is further subdivided into categories for JFETs, MOSFETs, and special function devices. VMOS, the next major subsection, is arranged according to device characteristics for $r_{DS(ON)}$. All remaining major subsections (ANALOG SWITCHES/MULTIPLEXERS, DATA ACQUISITION, LINEAR, TIMERS/COUNTERS, CONSUMER CIRCUITS, MEMORIES, MICROPROCESSORS/PERIPHERALS and DEVELOPMENT SYSTEMS) are organized alphabetically by function within easy grouping. The Functional Index appears in its entirety in the front matter section of this publication, and an appropriate sub-index appears at the beginning of each major product subsection.

CROSS-REFERENCE GUIDES

Two cross-reference guides are provided, including one for discrete devices and one for integrated circuits.

The discrete device cross reference indicates whether Intersil can provide the industry-standard type, or an Intersil-preferred part instead.

The IC alternate source cross-reference lists competitive manufacturer device types for which Intersil makes pin-for-pin replacements. In the left-hand column, the competitive device part number is organized alphabetically by manufacturer. The Intersil pin-for-pin replacement appears in the right-hand column.

SELECTOR GUIDES

Selector guide tables appear at the front of each major product category subsection, and provide a quick reference of key parameters for the devices contained in that section.

DEVICE FUNCTION/PACKAGE CODES

Diagrams which provide decoding information for device prefix and suffix codes are provided as rear matter material, as are package dimensions.

DIE SELECTION CRITERIA

Many of Intersil's semiconductor products are available in die form. This section contains general information on criteria for transistor and integrated circuit die selection, including physical parameters, packaging for shipment, assembly, testing, and purchase options.

HIGH-RELIABILITY PROCESSING

Defines Intersil's commitment to 100 percent compliance with MIL-STD-883, MIL-STD-750, MIL-M-38510 and MIL-S-19500 specifications. Also outlines Intersil's programs for quality conformance, quality testing and limited use qualification, and includes a glossary of military/aerospace Hi-Rel terms.

NOTE:
In this publication, PRELIMINARY is used to indicate that at the time of printing the device was not fully characterized. ADVANCE INFORMATION means that the device is in the pre-production stages.

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LF156	LF156
LF157	LF157
LF255	LF255
LF256	LF256
LF257	LF257
LF355	LF355
LF356	LF356
LF357	LF357
LH2301	LH2301
LH2311	LH2311
LM101	AD101
LM102	LM102
LM105	LM105
LM107	LM107
LM108	LM108
LM110	LM110
LM111	LM111
LM124	LM124
LM201	AD201
LM202	LM202
LM205	LM205
LM207	LM207
LM208	LM208
LM210	LM210
LM211	LM211
LM224	LM224
LM301	AD301
LM302	LM302
LM305	LM305
LM307	LM307
LM308	LM308
LM310	LM310
LM311	LM311
LM324	LM324
NE555	NE555
NE556	NE556
723	LM723
741	μA733
741	ICL741
748	LM748

AMI	**Intersil**
S6508	IM65X08
S6518	IM65X18

Analog Devices	**Intersil**
AD101	AD101
AD108	LM108
AD201	AD201
AD208	LM208
AD301	AD301
AD308	LM308
AD503	AD503
AD590	AD590
AD741	AD741
AD7506/COM/CHIPS	IH6116C/D
AD7506/MIL/CHIPS	IH6116M/D
AD7506JD	IH6116CJI
AD7506JD/883B	IH6116CJI/883B
AD7506JN	IH6116CPI
AD7506KD	IH6116CJI
AD7506KD/883B	IH6116CJI/883B
AD7506KN	IH6116CPI
AD7506SD	IH6116MJI
AD7506SD/883B	IH6116MJI/883B
AD7506TD	IH6116MJI
AD7506TD/883B	IH6116MJI/883B
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AD7507/MIL/CHIPS	IH6216M/D
AD7507JD	IH6216CJI
AD7507JD/883B	IH6216CJI/883B
AD7507JN	IH6216CPI
AD7507KD	IH6216CJI
AD7507KD/883B	IH6216CJI/883B
AD7507KN	IH6216CPI
AD7507SD	IH6216MJI
AD7507SD/883B	IH6216MJI/883B
AD7507TD	IH6216MJI
AD7507TD/883B	IH6216MJI/883B
AD7520JD	AD7520JD
AD7520JN	AD7520JN
AD7520KD	AD7520KD
AD7520KN	AD7520KN
AD7520LD	AD7520LD
AD7520LN	AD7520LN
AD7520SD	AD7520SD
AD7520TD	AD7520TD
AD7520UD	AD7520UD
AD7521JD	AD7521JD
AD7521JN	AD7521JN
AD7521KD	AD7521KD
AD7521KN	AD7521KN
AD7521LD	AD7521LD
AD7521LN	AD7521LN
AD7521SD	AD7521SD
AD7521TD	AD7521TD
AD7521UD	AD7521UD
AD7523AD	AD7523AD
AD7523BD	AD7523BD
AD7523CD	AD7523CD
AD7523JN	AD7523JN
AD7523KN	AD7523KN
AD7523LN	AD7523LN
AD7523SD	AD7523SD
AD7523TD	AD7523TD
AD7523UD	AD7523UD
AD7530JD	AD7530JD
AD7530JN	AD7530JN
AD7530KD	AD7530KD
AD7530KN	AD7530KN
AD7530LD	AD7530LD
AD7530LN	AD7530LN
AD7531JD	AD7531JD
AD7531JN	AD7531JN
AD7531KD	AD7531KD
AD7531KN	AD7531KN
AD7531LD	AD7531LD
AD7531LN	AD7531LN
AD7533AD	AD7533AD
AD7533BD	AD7533BD
AD7533CD	AD7533CD
AD7533JN	AD7533JN
AD7533KN	AD7533KN
AD7533LN	AD7533LN
AD7533SD	AD7533SD
AD7533TD	AD7533TD
AD7533UD	AD7533UD
AD7541AD	AD7541AD
AD7541BD	AD7541BD
AD7541JN	AD7541JN
AD7541KN	AD7541KN
AD7541SD	AD7541SD
AD7541TD	AD7541TD

Datel	**Intersil**
AM5402	HA2505 HA2525

EMM/SEMI	**Intersil**
2114	2114

Exar	**Intersil**
XR2240	ICL7240
XR4741	LM148
XR555	NE555
XR556	NE556
XR8038	ICL8038
XRL555	ICL7555
XRL556	ICL7556

Fairchild	**Intersil**
μAF155	LF155
μAF156	LF156
μAF157	LF157
μAF255	LF255
μAF256	LF256
μA257	LF257
μAF355	LF355
μAF356	LF356
μAF357	LF357
μA101	AD101
μA102	LM102
μA105	LM105
μA107	LM107
μA108	LM108
μA110	LM110
μA111	LM111
μA124	LM124
μA201	AD201
μA202	LM202
μA205	LM205
μA207	LM207
μA208	LM208
μA210	LM210
μA211	LM211
μA224	LM224
μA301	AD301
μA302	LM302
μA305	LM305
μA307	LM307
μA308	LM308
μA310	LM310
μA311	LM311
μA324	LM324
μA3302	MC3302
μA555	NE555
μA556	NE556
μA723	LM723
μA733	μA733
μA740	LM740
μA741	μA741
μA748	LM748
μA777	μA777
F4721	IM65X51
F4736	IM65X08
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93417	IM5603
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Fujitsu	**Intersil**
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MB7051	IM5610
MB7052	IM5623
MB7053	IM5624
MB7056	IM5600
MB7057	IM5603
MB7058	IM5604
MB8114	IM2114
MB8227	MK4027
MB8401	IM65X08
MB8411	IM65X16

Harris	**Intersil**
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HA2502	HA2502
HA2505	HA2505
HA2507	HA2507
HA2510	HA2510
HA2512	HA2512
HA2515	HA2515
HA2517	HA2517
HA2520	HA2520
HA2522	HA2522
HA2525	HA2525
HA2527	HA2527
HA2600	HA2600
HA2602	HA2602
HA2605	HA2605
HA2607	HA2607
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HA2622	HA2622
HA2625	HA2625
HA2627	HA2627
HA2720	ICL8021
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HI1-0506-2	IH6116MJI
HI1-0506-5	IH6116CJI
HI1-0506-8	IH6116MJI/883B
HI3-0506-5	IH6116CPI
HI0-0507-6	IH6216C/D
HI1-0507-2	IH6216MJI
HI1-0507-5	IH6216CJI
HI1-0507-8	IH6216MJI/883B
HI3-0507-5	IH6216CPI
HI0-0200-6	IH200B/D DG200B/D
HI1-0200-2	IH200AK DG200AK
HI1-0200-4	IH200BK DG200BK
HI1-0200-5	IH200BK DG200BK
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HI1-0201-8	IH201MJE/883B DG201AK/883B
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HI0-5043-6	IH5043C/D
HI1-5043-2	IH5043MJE
HI1-5043-5	IH5043CPE
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HI0-5044-6	IH044C/D
HI1-5044-2	IH5044MJE
HI1-5044-5	IH5044CPE
HI1-5044-8	IH5044MJE/883B
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HI1-5045-5	IH5045CPE
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HI1-5050-2	IH5050MJE
HI1-5050-5	IH5050CJE,CPE
HI1-5050-8	IH5050MJE/883B
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HI1-5051-2	IH5051MJE
HI1-5051-5	IH5051CJE,CPE
HI1-5051-8	IH5051MJE/883B
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HM6101	IM6101
HM6102	IM6102
HM6103	IM6103
HM6312	IM6312
HM6508	IM65X08
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HM6551	IM65X51
HM6561	IM65X61
HM7603	IM5610
HM7610	IM5603
HM7611	IM5623
HM7620	IM5604
HM7621	IM5624

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2114	2114
2141	IM7141
3602	IM5604
3604	IM5605
3622	IM5624
8049	IM80C49
8741	IM87C41

Maruman	**Intersil**
MIC2114	2114

MicroPower Systems	**Intersil**
MP7520JD	AD7520JD
MP7520JN	AD7520JN
MP7520KD	AD7520KD
MP7520KN	AD7520KN
MP7520LD	AD7520LD
MP7520LN	AD7520LN
MP7520SD	AD7520SD
MP7520TD	AD7520TD
MP7520UD	AD7520UD
MP7521JD	AD7521JD
MP7521JN	AD7521JN
MP7521KD	AD7521KD
MP7521KN	AD7521KN
MP7521LD	AD7521LD
MP7521LN	AD7521LN
MP7521SD	AD7521SD
MP7521TD	AD7521TD
MP7521UD	AD7521UD
MP7523JN	AD7523JN
MP7523KN	AD7523KN
MP7523LN	AD7523LN
MP7530JD	AD7530JD
MP7530JN	AD7530JN
MP7530KD	AD7530KD
MP7530KN	AD7530KN
MP7530LD	AD7530LD
MP7530LN	AD7530LN
MP7531JD	AD7531JD
MP7531JN	AD7531JN
MP7531KD	AD7531KD
MP7531KN	AD7531KN
MP7531LD	AD7531LD
MP7531LN	AD7531LN
MP7533AD	AD7533AD
MP7533BD	AD7533BD
MP7533CD	AD7533CD
MP7533JN	AD7533JN
MP7533KN	AD7533KN
MP7533LN	AD7533LN
MP7533SD	AD7533SD
MP7533TD	AD7533TD
MP7533UD	AD7533UD
MP7621AD	AD7541AD
MP7621BD	AD7541BD
MP7621JN	AD7541JN
MP7621KN	AD7541LN
MP7621SD	AD7541SD
MP7621TD	AD7541TD

MMI	**Intersil**
5300-1	IM5603
5301-1	IM5623
5305-1	IM5604
5306-1	IM5624
5330-1	IM5600
5331-1	IM5610
6300-1	IM5603
6301-1	IM5623
6305-1	IM5604
6306-1	IM5624
6330-1	IM5600
6331-1	IM5610

Mostek	**Intersil**
MK4027	IM7027 MK4027

Motorola	**Intersil**
LF155	LF155
LF156	LF156
LF157	LF157
LF255	LF255
LF256	LF256
LF257	LF257
LF355	LF355
LF356	LF356
LF357	LF357
LM101	AD101
LM105	LM105
LM107	LM107
LM110	LM110
LM111	LM111
LM124	LM124
LM201	AD201
LM205	LM205
LM207	LM207
LM208	LM208
LM210	LM210
LM211	LM211
LM224	LM224
LM301	AD301
LM305	LM305
LM307	LM307
LM308	LM308
LM310	LM310
LM311	LM311
LM324	LM324
MCM2114	2114
MC1723	LM723
MC1741	ICL741
MC1748	LM748
MC3302	MC3302

National Semiconductor	**Intersil**
AD7520JD (DAC1022LCD)	AD7520JD
AD7520JN (DAC1022LCN)	AD7520KD
AD7520KN (DAC1021LCD)	AD7520KD
AD7520KN (DAC1021LCN)	AD7520KN
AD7520LD (DAC1020LCD)	AD7520LD
AD7520LN (DAC1020LCN)	AD7520LN
AD7520SK (DAC1022LD)	AD7520SD
AD7520TD (DAC1021LD)	AD7520TD
AD7520UD (DAC1020LD)	AD7520UD
AD7521JD (DAC1222LCD)	AD7521JD
AD7521JN (DAC1222LCN)	AD7521JN
AD7521KD (DAC1221LCD)	AD7521KD
AD7521KN (DAC1221LCN)	AD7521KN
AD7521LD (DAC1220LCD)	AD7521LD
AD7521LN (DAC1220LCN)	AD7521LN
AD7521SD (DAC1222LD)	AD7521SD
AD7521TD (DAC1221LD)	AD7521TD
AD7521UD (DAC1220LD)	AD7521UD
AD7530JD (DAC1022LCD)	AD7530JD
AD7530JN (DAC1022LCN)	AD7530JN
AD7530KD (DAC1021LCD)	AD7530KD
AD7530KN (DAC1021LCN)	AD7530KN
AD7530LD (DAC1020LCD)	AD7530LD
AD7530LN (DAC1020LCN)	AD7530LN
AD7531JD (DAC1222LCD)	AD7531JD
AD7531JN (DAC1222LCN)	AD7531JN
AD7531KD (DAC1221LCD)	AD7531KD
AD7531KN (DAC1221LCN)	AD7531KN
AD7531LD (DAC1220LCD)	AD7531LD
AD7531LN (DAC1220LCN)	AD7531LN
AD7533AD (DAC1022LCD)	AD7533AD
AD7533BD (DAC1021LCD)	AD7533BD
AD7533CD (DAC1020LCD)	AD7533CD
AD7533JN (DAC1022LCN)	AD7533JN
AD7533KN (DAC1021LCN)	AD7533KN
AD7533LN (DAC102OLCN)	AD7533LN
AD7533SD (DAC1022LD)	AD7533SD
AD7533TD (DAC1021LD)	AD7533TD
AD7533UD (DAC1020LD)	AD7533UD
AH0126CD	DG126BK
AH0126D	DG126AK
AH0126D/883	DG126AK/883B
AH0129CD	DG129BK
AH0129D	DG129AK
AH0129D/883	DG129AK/883B
AH0133CD	DG133BK
AH0133D	DG133AK
AH0133D/883	DG133AK/883B
AH0134CD	DG134BK
AH0134D	DG134AK
AH0134D/883	DG134AK/883B
AH0139CD	DG139BK
AH0139D	DG139AK
AH0139D/883	DG139AK/883B
AH0140CD	DG140BK
AH0140D	DG140AK
AH0140D/883	DG140AK/883B
AH0141CD	DG141BK
AH0141D	DG141AK
AH0141D/883	DG141AK/883B
AH0142CD	DG142BK
AH0142D	DG142AK
AH0142D/883	DG142AK/883B
AH0143CD	DG143BK
AH0143D	DG143AK
AH0143D/883	DG143AK/883B
AH0144CD	DG144BK
AH0144D	DG144AK
AH0144D/883	DG144AK/883B
AD0145CD	DG145BK
AH0145D	DG145AK
AH0145D/883	DG145AK/883B
AH0146CD	DG146BK
AH0146D	DG146AK
AH0146D/883	DG146AK/883B
AH0151CD	DG151BK

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AH0151D	DG151AK
AH0151D/883	DG151AK/883B
AH0152CD	DG152BK
AH0152D	DG152AK
AH0152D/883	DG152AK/883B
AH0153CD	DG153BK
AH0153D	DG153AK
AH0153D/883	DG153AK/883B
AH0154CD	DG154BK
AH0154D	DG154AK
AH0154D/883	DG154AK/883B
AH0161CD	DG161BK
AH0161D	DG161AK
AH0161D/883	DG161AK/883B
AH0162CD	DG162BK
AH0162D	DG162AK
AH0162D/883B	DG162AK/883B
AH0163CD	DG163BK
AH0163D	DG163AK
AH0163D/883	DG163AK/883B
AH0164CD	DG164BK
AH0164D	DG164AK
AH0164D/883	DG164AK/883B
AH5009CN	IH5009CPD
AH5010CN	IH5010CPD
AH5011CN	IH5011CPE
AH5012CN	IB5012CPE
AN5013CN	IH5013CPD
AH5014CN	IH5014CPD
AH5015CN	IH5015CPE
AH5016CN	IH5016CPE
AM9709CN	IH5009CPD
AM97C09CN	IH5009CPD
AM9710CN	IH5010CPD
AM97C10CN	IH5010CPD
AM9711CN	IH5011CPE
AM97C11CN	IH5011CPE
AM9712CN	IH5012CPE
AM97C12CN	IH5012CPE
DM54S188	IM5600
DM54S287	IM5623
DM54S288	IM5610
DM54S387	IM5603
DM74S188	IM5600
DM74S287	IM5623
DM74S288	IM5610
DM74S387	IM5603
LF155	LF155
LF156	LF156
LF157	LF157
LF255	LF255
LF256	LF256
LF257	LF257
LF355	LF355
LF356	LF356
LF357	LF357
LF11201D	IH201MJE DG201AK
LF11201D/883	IH201MJE/883B DG201AK/883B
LF11202D	IH202MJE DG202AK
LF11202D/883	IH202MJE/883B DG202A/883B
LF11508D	IH6108MJE
LF11508D/883	IH6108MJE/883B
LF11509D	IH6208MJE
LF11509D/883	IH6208MJE/883B
LH0042	LH0042
LH2101	LH2101
LH2108	LH2108
LH2110	LH2110
LH2111	LH2111
LH2301	LH2301
LH2308	LH2308
LH2310	LH2310
LH2311	LH2311
LM100	LM100
LM101	AD101
LM102	LM102
LM105	LM105
LM107	LM107
LM108	LM108
LM110	LM110
LM111	LM111
LM124	LM124
LM200	LM200
LM201	AD201
LM202	LM202
LM205	LM205
LM207	LM207
LM208	LM208
LM210	LM210
LM211	LM211
LM224	LM224
LM2902	LM2902
LM300	LM300
LM301	AD301
LM302	LM302
LM305	LM305
LM307	LM307
LM308	LM308
LM310	LM310
LM311	LM311
LM4250	LM4250
LM555	NE555
LM556	NE556
LM723	LM723
LM733	µA733
LM740	LM740
LM741	LM741
LM742	LM748
MC3302	MC3302
MM2114	2114
MM450	MM450
MM451	MM451
MM452	MM452
MM455	MM455
MM5257	IM7141
MM550	MM550
MM551	MM551
MM552	MM552
MM555	MM555
MM74C920	IM65X51
MM74C929	IM65X08
MM74C930	IM65X18

NEC	**Intersil**
µPB403	IM5603
µPD2114	2114
µPD6508	IM65X08

Plessey	**Intersil**
SC748	LM748

PMI	**Intersil**
PM155	LF155
PM156	LF156
PM157	LF157
PM255	LF255
PM256	LF256
PM257	LF257
PM308	LM308
PM355	LF355
PM356	LF356
PM357	LF357
SSS741	ICL741

Raytheon	**Intersil**
LF155	LF155
LF156	LF156
LF157	LF157
LF255	LF255
LF256	LF256
LF257	LF257
LF355	LF355
LF356	LF356
LF357	LF357
LH2101	LH2101
LH2301	LH2301
LH2311	LH2311
LM101	AD101
LM105	LM105
LM107	LM107
LM108	LM108
LM124	LM124
LM201	AD201
LM205	LM205
LM207	LM207
LM208	LM208
LM211	LM211
LM224	LM224
LM2902	LM2902
LM301	AD301
LM305	LM305
LM307	LM307
LM308	LM308
LM311	LM311
LM324	LM324
RC555	NE555
RC556	NE556
RC723	LM723
RC733	µA733
RC741	ICL741
RC748	LM748
RM723	LM723
RM741	ICL741
RM748	LM748
RV3302	MC3302

RCA	**Intersil**
CA101	AD101
CA107	LM107
CA111	LM111
CA124	LM124
CA201	AD201
CA207	LM207
CA208	LM208
CA211	LM211
CA224	LM224
CA301	AD301
CA307	LM307
CA308	LM308
CA311	LM311
CA324	LM324
CA555	NE555
CA723	LM723
CA741	ICL741
CA748	LM748
CDP1854	IM6402

Signetics	**Intersil**
µA723	LM723
µA733	µA733
µ740	LM740
µA741	µA741
µA748	LM748
LF155	LF155
LF156	LF156
LF157	LF157
LF255	LF255
LF256	LF256
LF257	LF257
LF355	LF355
LF356	LF356
LF357	LF357
LH2101	LH2101
LH2108	LH2108
LH2301	LH2301
LH2308	LH2308
LH2311	LH2311
LM101	AD101
LM107	LM107
LM111	LM111
LM124	LM124
LM201	AD201
LM207	LM207
LM224	LM224
LM2902	LM2902
LM301	AD301
LM307	LM307
LM308	LM308
LM324	LM324
MC3302	MC3302
NE555	NE555
NE556	NE556
8049	IM80C49
82S123	IM5610
82S126	IM5603
82S129	IM5623
82S130	IM5604
82S131	IM5624
82S23	IM5600

Silicon General	**Intersil**
µA777	µA777
SG101	AD101
SG105	LM105
SG107	LM107
SG108	LM108
SG110	LM110
SG111	LM111
SG124	LM124
SG201	AD201
SG205	LM205
SG207	LM207
SG208	LM208
SG210	LM210
SG211	LM211
SG224	LM224
SG301	AD301
SG305	LM305
SG307	LM307
SG308	LM308
SG311	LM311
SG324	LM324
SG3302	MC3302
SG4250	LM4250
SG555	NE555

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SG556	NE556
SG723	LM723
SG733	μA733
SG741	ICL741
SG748	LM748

Siliconix	**Intersil**
DGM111AL	DG111AL
DGM111AP	DG111AK
DGM111BP	DG111BK
DG123AL	DG123AL
DG123AP	DG123AK
DG123BP	DG123BK
DG125AL	DG125AL
DG125AP	DG125AK
DG125BP	DG125BK
DG126AL	DG126AL
DG126AP	DG126AK
DG126BP	DG126BK
DG129AL	DG129AL
DG129AP	DG129AK
DG129BP	DG129BK
DG133AL	DG133AL
DG133AP	DG133AK
DG133BP	DG133BK
DG134AL	DG134AL
DG134AP	DG134AK
DG134BP	DG134BK
DG139AL	DG139AL
DG139AP	DG139AK
DG139BP	DG139BK
DG140AL	DG140AL
DG140AP	DG140AK
DG140BP	DG140BK
DG141AL	DG141AL
DG141AP	DG141AK
DG141BP	DG141BK
DG142AL	DG142AL
DG142AP	DG142AK
DG142BP	DG142BK
DG143AL	DG143AL
DG143AP	DG143AK
DG143BP	DG143BK
DG144AL	DG144AL
DG144AP	DG144AK
DG144BP	DG144BK
DG145AL	DG145AL
DG145AP	DG145AK
DG145BP	DG145BK
DG146AL	DG146AL
DG146AP	DG146AK
DG146BP	DG146BK
DG151AL	DG151AL
DG151AP	DG151AK
DG151BP	DG151BK
DG152AL	DG152AL
DG152AP	DG152AK
DG152BP	DG152BK
DG153AL	DG153AL
DG153AP	DG153AK
DG153BP	DG153BK
DG154AL	DG154AL
DG154AP	DG154AK
DG154BP	DG154BK
DG161AL	DG161AL
DG161AP	DG161AK
DG161BP	DG161BK
DG162AL	DG162AL
DG162AP	DG162AK
DG162BP	DG162BK
DG163AL	DG163AL
DG163AP	DG163AK
DG163BP	DG163BK
DG164AL	DG164AL
DG164AP	DG164AK
DG164BP	DG164BK
DG180AA	DG180AA
DG180AL	DG780AL
DG180AP	DG180AK
DG180BA	DG180BA
DG180BP	DG180BK
DG181AA	DG181AA
DG181AL	DG181AL
DG181AP	DG181AK
DG181BA	DG181BA
DG181BP	DG181BK
DG182AA	DG182AA
	DGM182AA
DG182AL	DG182AL
	DGM182AL
DG182AP	DG182AK
	DGM182AK
DG182BA	DG182BA
	DGM182BA
DG182BP	DG182BK
	DGM182BK
DG183AL	DG183AL
DG183AP	DG183AK
DG183BP	DG183BK
DG184AL	DG184AL
DG184AP	DG184AK
DG184BP	DG184BK
DG185AL	DG185AL
	DGM185AL
DG185AP	DG185AK
	DGM185AK
DG185BP	DG185BK
	DGM185BK
DG186AA	DG186AA
DG186AL	DG186AL
DG186AP	DG186AK
DG186BA	DG186BA
DG186BP	DG186BK
DG187AA	DG187AA
DG187AL	DG187AL
DG187AP	DG187AK
DG187BA	DG187BA
DG187BP	DG187BK
DG188AA	DG188AA
	DGM188AA
DG188AL	DG188AL
DG188AP	DG188AK
DG188BA	DG188BA
	DGM188BA
DG188BP	DG188BK
DG189AL	DG189AL
DG189AP	DG189AK
DG189BP	DG189BK
DG190AL	DG190AL
DG190AP	DG190AK
DG190BP	DG190BK
DG191AL	DG191AL
	DGM191AL
DG191AP	DG191AK
	DGM191AK
DG191BP	DG191BK
	DGM191BK
DG200AA	IH200AA
	DG200AA
DG200AL	IH200AL
	DG200AL
DG200AP	IH200AK
	DG200AK
DG200BA	IH200BA
	DG200BA
DG200BP	IH200BK
	DG200BK
DG200CJ	DG200CJ
DG201AP	IH201MJE
	DG201AK
DG201BP	IH201CJE
	DG201BK
DG201CJ	DG201CJ
DG506AR	IH6116MJI
DG506BR	IH6116CJI
DG506CJ	IH6116CPI
DG507AR	IH6216MJI
DG507BR	IH6216CJI
DG507CJ	IH6216CPI
DG508AP	IH6108MJE
DG508BP	IH6108CJE
DG508CJ	IH6108CPE
DG509AP	IH6208MJE
DG509BP	IH6208CJE
DG509CJ	IH6208CPE
D123AL	D123AL
D123AP	D123AK
D123BP	D123BK
D125AL	D123BJ
D125AP	D125AL
	D125AK
D125BP	D125BK
	D125BJ
D129AL	D129AL
D129AP	D129AK
D129BP	D129BK
G115AP	G115AK
G115BP	G115BJ
	G115BK
G116AL	G116AL
G116AP	G116AK
G116BP	G116BK
	G116BJ
G117AL	G117AL
G118AL	G118AL
G118AP	G118AK
G119AL	G119AL
G123AL	G123AL
G123AP	G123AK
LD110	LD110
LD111	LD111
LD114	LD114
SI452	MM452
SI455	MM455
SI552	MM552
SI555	MM555

Synertek	**Intersil**
SY2114	2114

TI	**Intersil**
μA723	LM723
μA733	μA733
μ741	μA741
μA748	LM748
μA777	μA777
LF155	LF155
LF156	LF156
LF157	LF157
LF255	LF255
LF256	LF256
LF257	LF257
LF355	LF355
LF356	LF356
LF357	LF357
LM101	AD101
LM105	LM105
LM107	LM107
LM111	LM111
LM124	LM124
LM201	AD201
LM224	LM224
LM2902	LM2902
LM301	AD301
LM305	LM305
LM307	LM307
LM311	LM311
LM324	LM324
NE555	NE555
NE556	NE556
SN54S188	IM5600
SN54S288	IM5610
SN54S387	IM5603
SN74S188	DGM182BA
SN74S288	IM5610
SN74S387	IM5603
TL182CL	DGM182BA
TL182CN	DGM182CJ
TL182IL	DGM182BA
TL182IN	DGM182CJ
TL182ML	DGM182AA
TL185CJ	IH5045CJE
TL185CN	IH5045CPE
TL185IJ	IH5045CJE
TL185IN	IH5045CPE
TL185MJ	IH5045MJE
TL188CL	IH5042CTW
TL188CN	IH5042CPE
TL188IL	IH5042CTW
TL188IN	IH5042CPE
TL188ML	IH5042MTW
TL191CJ	IH5043CJE
TL191CN	IH5043CPE
TL1911J	IH5043CJE
TL191IN	IH5043CPE
TL191MJ	IH5043MJE
TMS4027	IM7027
	MK4027
TMS4044	IM7141
TMS4045	2114

DISCRETE & POWER MOS ALTERNATE SOURCE INDEX

INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
100S	2N5458	2N2606	2N2607	2N3331	2N5270	2N3814	IT132
100U	2N3684	2N2607	2N2607	2N3332	2N5268	2N3815	IT132
102M	2N5686	2N2608	2N2608	2N3333	IT132	2N3816	IT130
102S	2N5457	2N2609	2N2609	2N3334	IT132	2N3816A	IT130A
103M	2N5457	2N2609JAN	2N2609JAN	2N3335	IT132	2N3817	IT130
103S	2N5459	2N2639	IT120	2N3336	IT132	2N3817A	IT130A
104M	2N5458	2N2640	IT122	2N3347	IT137	2N3819	2N5484
105M	2N5459	2N2641	IT122	2N3348	IT138	2N3820	2N2608
105U	2N4340	2N2642	IT120	2N3349	IT139	2N3821	2N3821
106M	2N5485	2N2643	IT122	2N3350	IT137	2N3821JAN	2N3821JAN
107M	2N5485	2N2644	IT122	2N3351	IT138	2N3821JANTX	2N3821JANTX
110U	2N3685	2N2652	IT120	2N3352	IT139	2N3821JTXV	2N3821JTXV
120U	2N3686	2N2652A	IT120	2N3365	2N4340	2N3822	2N3822
125U	2N4339	2N2720	IT120	2N3366	2N4338	2N3823	2N3823
1277A	2N3822	2N2721	IT122	2N3367	2N4338	2N3823JAN	2N3823JAN
1278A	2N3821	2N2722	IT120	2N3368	2N4341	2N3823JANTX	2N3823JANTX
1279A	2N3821	2N2802	IT139	2N3369	2N4339	2N3823JANTXV	2N3823JANTXV
1280A	2N4224	2N2803	IT139	2N3370	2N4338	2N3824	2N3824
1281A	2N3822	2N2804	IT139	2N3376	2N2608	2N3907	IT120
1282A	2N4341	2N2805	IT139	2N3378	2N2608	2N3908	IT120
1283A	2N4340	2N2806	IT139	2N3380	2N2609	2N3909	2N2609
1284A	2N4222	2N2807	IT139	2N3382	2N3994	2N3909A	2N2609
1285A	2N3821	2N2841	2N2607	2N3384	2N3993	2N3921	2N3921
1286A	2N4220	2N2842	2N2607	2N3386	2N5114	2N3922	2N3922
130U	2N3687	2N2843	2N2607	2N3409	IT122	2N3949	IT132
1325A	2N4222	2N2844	2N2607	2N3410	IT122	2N3950	IT132
135U	2N4339	2N2903	IT122	2N3411	IT122	2N3954	2N3954
14T	2N4224	2N2903A	IT120	2N3423	IT122	2N3954A	2N3954A
155U	2N4416	2N2910	IT122	2N3424	IT122	2N3955	2N3955
1714A	2N4340	2N2913	IT122	2N3425	IT122	2N3955A	2N3955A
182S	2N4391	2N2914	IT120	2N3436	2N4341	2N3956	2N3956
183S	2N3823	2N2915	IT120	2N3437	2N4340	2N3957	2N3957
197S	2N4338	2N2915A	IT120	2N3438	2N4338	2N3966	2N4416
198S	2N4340	2N2916	IT120	2N3452	2N4220	2N3967	2N4221
199S	2N4341	2N2916A	IT120	2N3453	2N4338	2N3967A	2N4221
2000M	2N3823	2N2917	IT122	2N3454	2N4338	2N3968	2N3685
2001M	2N3823	2N2918	IT122	2N3455	2N4340	2N3968A	2N3685
200S	2N4392	2N2919	IT120	2N3456	2N4338	2N3969	2N3686
200U	2N3824	2N2919A	IT120	2N3457	2N4338	2N3969A	2N3686
201S	2N4391	2N2920	2N2920	2N3458	2N4341	2N3970	2N3970
202S	2N4392	2N2920A	2N2920	2N3459	2N4339	2N3971	2N3971
203S	2N3821	2N2936	IT120	2N3460	2N4338	2N3972	2N3972
204S	2N3821	2N2937	IT120	2N3513	IT122	2N3993	2N3993
2078A	2N3955	2N2972	IT122	2N3514	IT122	2N3993A	2N3993
2079A	2N3955	2N2973	IT122	2N3515	IT122	2N3994	2N3994
2080A	2N3955A	2N2974	IT120	2N3516	IT122	2N3994A	2N3994
2081A	2N3955A	2N2975	IT120	2N3517	IT122	2N4009	IT132
2093M	2N3687	2N2976	IT120	2N3521	IT122	2N4010	IT132
2094M	2N3686	2N2977	IT120	2N3522	IT122	2N4011	IT132
2095M	2N3686	2N2978	IT120	2N3574	2N2607	2N4015	IT139
2098A	2N3954	2N2979	IT120	2N3575	2N2607	2N4016	IT137
2099A	2N3955A	2N2980	IT121	2N3578	2N2608	2N4017	IT139
210U	2N4416	2N2981	IT122	2N3587	IT122	2N4018	IT139
2130U	2N5452	2N2982	IT122	2N3608	3N172	2N4019	IT139
2132U	2N3955	2N3043	IT121	2N3680	IT120	2N4020	IT139
2134U	2N3956	2N3044	IT122	2N3684	2N3684	2N4021	IT139
2136U	2N3957	2N3045	IT122	2N3684A	2N3684	2N4022	IT139
2138U	2N3958	2N3046	IT121	2N3685	2N3685	2N4023	IT137
2139U	2N3958	2N3047	IT122	2N3685A	2N3685	2N4024	IT137
2147U	2N3958	2N3048	IT122	2N3686	2N3686	2N4025	IT137
2148U	2N3958	2N3049	IT139	2N3686A	2N3686	2N4026	3N163
2149U	2N3958	2N3050	IT139	2N3687	2N3687	2N4038	2N4351
231S	2N3954	2N3051	IT139	2N3687A	2N3687	2N4039	2N4351
232S	2N3955	2N3052	IT129	2N3726	IT131	2N4065	3N163
233S	2N3956	2N3059	IT139	2N3727	IT130	2N4066	3N166
234S	2N3957	2N3066	2N4340	2N3728	IT122	2N4067	3N166
235S	2N3958	2N3067	2N4338	2N3729	IT121	2N4082	2N3954
241U	2N4869	2N3068	2N4338	2N3800	IT132	2N4083	2N3955
250U	2N4091	2N3069	2N4341	2N3801	IT132	2N4084	2N3954
251U	2N4392	2N3070	2N4339	2N3802	IT132	2N4085	2N3955
2N2060	IT120	2N3071	2N4338	2N3803	IT132	2N4091	2N4091
2N2060A	IT121	2N3084	2N4339	2N3804	IT130	2N4091A	2N4091
2N2060B	IT121	2N3085	2N4339	2N3804A	IT130A	2N4091JAN	2N4091JAN
2N2223	IT122	2N3086	2N4339	2N3805	IT130	2N4091JANTX	2N4091JANTX
2N2223A	IT121	2N3087	2N4339	2N3805A	IT130A	2N4091JANTXV	2N4091JANTXV
2N2386	2N2608	2N3088	2N4339	2N3806	IT122	2N4092	2N4092
2N2386A	2N2608	2N3088A	2N4339	2N3807	IT122	2N4092A	2N4092
2N2453	IT122	2N3089	2N4339	2N3808	IT122	2N4092JAN	2N4092JAN
2N2453A	IT121	2N3089A	2N4339	2N3809	IT122	2N4092JANTX	2N4092JANTX
2N2480	IT122	2N3113	2N2607	2N3810	2N3810	2N4092JANTXV	2N4092JANTXV
2N2480A	IT121	2N3277	2N2606	2N3810A	2N3810A	2N4093	2N4093
2N2497	2N2608	2N3278	2N2607	2N3811	2N3811	2N4093A	2N4093
2N2498	2N2608	2N3328	2N5265	2N3811A	2N3811A	2N4093JAN	2N4093JAN
2N2499	2N2609	2N3329	2N5267	2N3812	IT132	2N4093JANTX	2N4093JANTX
2N2500	2N2608	2N3330	2N5268	2N3813	IT132	2N4093JANTXV	2N4093JANTXV

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
2N4100	2N4100	2N4979	2N4859	2N5471	2N5265	2N6448	IT121
2N4117	2N4117	2N5018	2N5018	2N5472	2N5265	2N6451	U310
2N4117A	2N4117A	2N5019	2N5019	2N5473	2N5265	2N6452	U310
2N4118	2N4118	2N5020	2N2843	2N5474	2N5265	2N6453	U310
2N4118A	2N4118A	2N5021	2N2607	2N5475	2N5265	2N6454	U310
2N4119	2N4119	2N5033	2N5460	2N5476	2N5266	2N6483	2N6483
2N4119A	2N4119A	2N5045	2N5453	2N5484	2N5484	2N6484	2N6484
2N4120	3N163	2N5046	2N5454	2N5485	2N5485	2N6485	2N6485
2N4139	2N3822	2N5047	2N5454	2N5486	2N5486	2N6502	IT122
2N4220	2N4220	2N5078	2N5397	2N5515	2N5515	2N6503	IT122
2N4220A	2N4220	2N5090	IT122	2N5516	2N5516	2N6550	2N4868A
2N4221	2N4221	2N5103	2N4416	2N5517	2N5517	2N6568	2N5432
2N4221A	2N4221	2N5104	2N4416	2N5518	2N5518	2N6656	IVN6657
2N4222	2N4222	2N5105	2N4416	2N5519	2N5519	2N6657	2N6657
2N4222A	2N4222	2N5114	2N5114	2N5520	2N5520	2N6658	2N6658
2N4223	2N4223	2N5114JAN	2N5114JAN	2N5521	2N5521	2N6659	IVN6658
2N4224	2N4224	2N5114JANTX	2N5114JANTX	2N5522	2N5522	2N6660	2N6660
2N4267	3N163	2N5114JANTXV	2N5114JANTXV	2N5523	2N5523	2N6661	2N6661
2N4268	3N161	2N5115	2N5115	2N5524	2N5524	2SC294	IT122
2N4302	2N4302	2N5115JAN	2N5115JAN	2N5545	2N3954	2SJ11	2N2607
2N4303	2N5459	2N5115JANTX	2N5115JANTX	2N5546	2N3955A	2SJ12	2N2607
2N4304	2N5458	2N5115JANTXV	2N5115JANTXV	2N5547	2N3955	2SJ13	2N5270
2N4338	2N4338	2N5116	2N5116	2N5549	2N4093	2SJ15	2N2607
2N4339	2N4339	2N5116JAN	2N5116JAN	2N5555	J310	2SJ16	2N2607
2N4340	2N4340	2N5116JANTX	2N5116JANTX	2N5556	2N3685	2SJ47	**
2N4341	2N4341	2N5116JANTXV	2N5116JANTXV	2N5557	2N3684	2SJ48	**
2N4342	2N5461	2N5117	2N5117	2N5558	2N3684	2SJ49	**
2N4343	2N5462	2N5118	2N5118	2N5561	U401	2SJ50	**
2N4351	2N4351	2N5119	2N5119	2N5562	U402	2SJ78	**
2N4352	3N163	2N5120	IT131	2N5563	U404	2SJ79	**
2N4353	3N172	2N5121	IT132	2N5564	2N5564	2SJ80	**
2N4360	2N5460	2N5122	IT132	2N5565	2N5565	2SK11	2N5457
2N4381	2N2609	2N5123	IT131	2N5566	2N5566	2SK12	2N5457
2N4382	2N5115	2N5124	IT132	2N5592	2N3822	2SK13	2N5457
2N4391	2N4391	2N5125	IT132	2N5593	2N3822	2SK132	**
2N4392	2N4392	2N5158	2N5434	2N5594	2N3822	2SK133	**
2N4393	2N4393	2N5159	2N5433	2N5638	2N5638	2SK134	**
2N4416	2N4416	2N5163	2N3822	2N5639	2N5639	2SK135	**
2N4416A	2N4416A	2N5196	2N5196	2N5640	2N5640	2SK15	2N4868
2N4417	2N4416	2N5197	2N5197	2N5647	2N4117A	2SK17	2N5484
2N4445	2N5432	2N5198	2N5198	2N5648	2N4117A	2SK178	**
2N4446	2N5434	2N5199	2N5199	2N5649	2N4117A	2SK179	**
2N4447	2N5432	2N5245	ITE4416	2N5653	2N5638	2SK18	2N3821
2N4448	2N5434	2N5246	2N5484	2N5654	2N5639	2SK180	**
2N4856	2N4856	2N5247	2N5486	2N5668	2N5484	2SK19	ITE4416
2N4856A	2N4856	2N5248	2N5486	2N5669	2N5485	2SK23	2N5459
2N4856JAN	2N4856JAN	2N5254	IT132	2N5670	2N5486	2SK30	2N5458
2N4856JANTX	2N4856JANTX	2N5255	IT132	2N5793	IT129	2SK32	2N3822
2N4856JANTXV	2N4856JANTXV	2N5256	IT130	2N5794	IT129	2SK33	2N5397
2N4857	2N4857	2N5257	2N5457	2N5795	IT139	2SK34	2N3822
2N4857A	2N4857	2N5258	2N5458	2N5796	IT139	2SK37	2N5484
2N4857JAN	2N4857JAN	2N5259	2N5459	2N5797	2N2608	2SK41	2N5459
2N4857JANTX	2N4857JANTX	2N5265	2N2607	2N5798	2N2608	2SK42	2N3822
2N4857JANTXV	2N4857JANTXV	2N5266	2N2607	2N5799	2N2608	2SK43	ITE4092
2N4858	2N4858	2N5267	2N2608	2N5800	2N2608	2SK44	ITE4416
2N4858A	2N4858	2N5268	2N2608	2N5801	2N4393	2SK46	2N5459
2N4858JAN	2N4858JAN	2N5269	2N2609	2N5802	2N4393	2SK48	2N3821
2N4858JANTX	2N4858JANTX	2N5270	2N2609	2N5803	2N4392	2SK49	2N5484
2N4858JANTXV	2N4858JANTXV	2N5277	2N4341	2N5843	IT130	2SK50	ITE4416
2N4859	2N4859	2N5278	2N4341	2N5844	IT130	2SK54	2N3822
2N4859A	2N4859	2N5358	2N4220	2N5902	2N5902	2SK55	2N3822
2N4859JAN	2N4856JAN	2N5359	2N4220	2N5903	2N5903	2SK56	2N5459
2N4859JANTX	2N4856JANTX	2N5360	2N4221	2N5904	2N5904	2SK61	2N5397
2N4860	2N4860	2N5361	2N4221	2N5905	2N5905	2SK65	J201
2N4860A	2N4860	2N5362	2N4222	2N5906	2N5906	2SK66	2N3821
2N4860JAN	2N4857JAN	2N5363	2N4222	2N5907	2N5907	2SK68	2N3822
2N4860JANTX	2N4857JANTX	2N5364	2N4222	2N5908	2N5908	2SK72	2N5196
2N4861	2N4861	2N5391	2N4867A	2N5909	2N5909	3GS	2N3821
2N4861A	2N4861	2N5392	2N4868A	2N5911	2N5911	3N145	3N163
2N4861JAN	2N4858JAN	2N5393	2N4869A	2N5912	2N5912	3N146	3N163
2N4861JANTX	2N4858JANTX	2N5394	2N4869A	2N5949	2N5486	3N147	3N189
2N4867	2N4867	2N5395	2N4869A	2N5950	2N5486	3N148	3N189
2N4867A	2N4867A	2N5396	2N4869A	2N5951	2N5486	3N149	3N161
2N4868	2N4868	2N5397	2N5397	2N5952	2N5484	3N150	3N163
2N4868A	2N4868A	2N5398	2N5398	2N5953	2N5484	3N151	3N190
2N4869	2N4869	2N5432	2N5432	2N6085	IT122	3N155	3N163
2N4869A	2N4869A	2N5433	2N5433	2N6086	IT122	3N155A	3N163
2N4878	2N4878	2N5434	2N5434	2N6087	IT121	3N156	3N163
2N4879	2N4879	2N5452	2N5452	2N6088	IT121	3N156A	3N163
2N4880	2N4880	2N5453	2N5453	2N6089	IT122	3N157	3N163
2N4937	IT131	2N5454	2N5454	2N6090	IT121	3N157A	3N163
2N4938	IT132	2N5457	2N5457	2N6091	IT121	3N158	3N163
2N4939	IT132	2N5458	2N5458	2N6092	IT121	3N158A	3N163
2N4940	IT132	2N5459	2N5459	2N6441	IT122	3N160	3N161
2N4941	IT131	2N5460	2N5460	2N6442	IT122	3N161	3N161
2N4942	IT132	2N5461	2N5461	2N6443	IT122	3N163	3N163
2N4955	IT122	2N5462	2N5462	2N6444	IT122	3N164	3N164
2N4956	IT122	2N5463	2N5463	2N6445	IT121	3N165	3N165
2N4977	2N5433	2N5464	2N5464	2N6446	IT121	3N166	3N166
2N4978	2N5433	2N5465	2N5465	2N6447	IT121	3N167	3N161

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
3N168	3N161	AD838	2N3956	BFX36	IT131	CM646	2N4092
3N169	3N170	AD839	2N3957	BFX70	IT122	CM647	2N4091
3N170	3N170	AD840	2N5520	BFX71	IT122	CM650	2N5432
3N171	3N171	AD841	2N5521	BFX72	IT122	CM651	2N5433
3N172	3N172	AD842	2N5523	BFX78	2N5397	CM652	2N5432
3N173	3N173	BC264	2N5458	BFX82	2N5019	CM653	2N5433
3N174	3N163	BC264A	2N5457	BFX83	2N5019	CM697	2N5433
3N175	3N170	BC264B	2N5458	BFX99	IT120A	CM800	2N5433
3N176	3N170	BC264C	2N5458	BFY20	IT122	CM856	2N5433
3N177	3N171	BC264D	2N4416	BFY81	IT122	CM860	2N4868A
3N178	3N172	BCY87	IT121	BFY82	IT122	CMX740	2N5432
3N179	3N172	BCY88	IT122	BFY83	IT122	CP640	2N4091
3N180	3N172	BCY89	IT122	BFY84	IT122	CP643	2N5434
3N181	3N161	BD512	**	BFY85	IT122	CP650	2N5432
3N182	3N161	BD522	IVN5001BNE	BFY86	IT122	CP651	2N5433
3N183	3N161	BF244	2N5486	BFY91	IT122	CP652	2N5433
3N188	3N188	BF244A	2N5484	BFY92	IT122	CP653	2N5433
3N189	3N189	BF244B	2N5485	BN209	IT122	D1101	2N3821
3N190	3N190	BF244C	2N5486	BSV22	2N4416	D1102	2N3821
3N191	3N191	BF245	2N5486	BSV78	2N4856A	D1103	2N4338
3N207	3N190	BF245A	2N4416	BSV79	2N4857A	D1177	2N3821
3N208	3N188	BF245B	2N4416	BSV80	2N4858A	D1178	2N3821
3SK22	2N5486	BF245C	2N4416	BSX82	2N3822	D1179	2N4338
3SK23	2N5397	BF246	2N5485	C21	2N3821	D1180	2N3822
3SK28	2N5397	BF246A	2N5639	C2306	2N5196	D1181	2N4338
42T	2N4392	BF246B	2N5638	C38	2N4338	D1182	2N4338
4360TP	2N5462	BF246C	2N5638	C413N	2N5434	D1183	2N4341
5033TP	2N5460	BF247	2N4091	C610	2N4392	D1184	2N4340
588U	2N4416	BF247A	2N4091	C611	2N4221	D1185	2N4339
58T	2N5457	BF247B	2N4091	C612	2N4221	D1201	2N4224
59T	2N4416	BF247C	2N4091	C613	2N4221	D1202	2N3821
703U	2N4220	BF256	2N5484	C614	2N4220	D1203	2N4220
704U	2N4220	BF256A	2N5484	C615	2N4221	D1301	2N4222
705U	2N4224	BF256B	2N4416	C620	2N4220	D1302	2N4220
707U	2N4860	BF256C	2N4416	C621	2N4220	D1303	2N4220
714U	2N3822	BF320	2N5461	C622	2N4220	D1420	2N4868
734EU	2N4416	BF346	ITE4392	C623	2N4220	D1421	2N3822
734U	2N5516	BF347	J201	C624	2N4220	D1422	2N4869
751U	2N4340	BF348	J310	C625	2N4220	D2T2218	IT129
752U	2N4340	BF800	2N4867	C650	2N4220	D2T2218A	IT129
753U	2N4341	BF801	2N4867	C651	2N4220	D2T2219	IT129
754U	2N4340	BF802	2N4338	C652	2N4220	D2T2219A	IT129
755U	2N4341	BF804	2N4338	C653	2N4220	D2T2904	IT139
756U	2N4340	BF805	2N4869	C6690	2N4341	D2T2904A	IT139
A190	ITE4416	BF806	2N4869	C6691	2N4341	D2T2905	IT139
A191	ITE4416	BF808	2N4868	C6692	2N4339	D2T2905A	IT139
A192	2N4416	BF810	2N4858	C673	2N4341	D2T918	IT129
A193	2N5484	BF811	2N4858	C674	2N4341	DA102	2N5196
A194	2N5484	BF815	2N4858	C680	2N4338	DA402	2N5196
A195	2N5484	BF816	2N4858	C680A	2N4338	DN3066A	2N3821
A196	ITE4416	BF817	2N4858	C681	2N4338	DN3067A	2N4338
A197	ITE4391	BF818	2N4858	C681A	2N4338	DN3068A	2N4338
A198	ITE4392	BFQ10	U401	C682	2N4339	DN3069A	2N3822
A199	ITE4393	BFQ11	U401	C682A	2N4339	DN3070A	2N3821
A5T3821	2N5484	BFQ12	U402	C683	2N4339	DN3071A	2N4338
A5T3822	2N5484	BFQ13	U403	C683A	2N4339	DN3365A	2N4220
A5T3823	2N4416	BFQ14	U404	C684	2N4220	DN3365B	2N4091
A5T3824	2N4341	BFQ15	U405	C684A	2N4220	DN3366A	2N3686
A5T5460	2N5460	BFQ16	U406	C685	2N4220	DN3366B	2N4091
A5T5461	2N5461	BFS21	2N5199	C685A	2N4220	DN3367A	2N3687
A5T5462	2N5462	BFS21A	2N5199	C80	2N4338	DN3367B	2N4091
AD3954	2N3954	BFS67	2N3821	C81	2N4338	DN3368A	2N4341
AD3954A	2N3954A	BFS67P	2N5459	C84	2N4338	DN3368B	2N4221
AD3955	2N3955	BFS68	2N3823	C85	2N4338	DN3369A	2N4339
AD3956	2N3956	BFS68P	2N4416	C91	2N4858	DN3369B	2N4220
AD3958	2N3958	BFS70	2N3821	C92	2N4091	DN3370A	2N4338
AD5905	2N5905	BFS71	2N3822	C93	2N4393	DN3370B	2N4338
AD5906	2N5906	BFS72	2N3823	C94	2N468	DN3436A	2N4341
AD5907	2N5907	BFS73	2N3821	C94E	2N5457	DN3436B	2N4222
AD5908	2N5908	BFS74	2N4856	C95	2N5457	DN3437A	2N4340
AD5909	2N5909	BFS75	2N4857	C95E	2N5459	DN3437B	2N4220
AD810	2N4878	BFS76	2N4858	C96E	2N5484	DN3438A	2N4338
AD811	2N4878	BFS77	2N4859	C97E	2N3822	DN3438B	2N4339
AD812	2N4878	BFS78	2N4860	C98E	2N3822	DN3458A	2N4341
AD813	2N4878	BFS79	2N4861	CC4445	2N5432	DN3458B	2N4222
AD814	IT124	BFS80	2N4416A	CC4446	2N5434	DN3459A	2N4339
AD815	IT124	BFT10	2N5397	CC697	2N4856	DN3459B	2N4220
AD816	IT120A	BFT11	2N5019	CF2386	2N5458	DN3460A	2N4338
AD818	IT140	BFW10	2N3823	CF24	2N3824	DN3460B	2N4220
AD820	IT132	BFW11	2N3822	CFM13026	2N4858	DNX1	2N4338
AD821	IT130A	BFW12	2N4416	CM600	2N4092	DNX2	2N4338
AD822	IT130A	BFW13	2N4867	CM601	2N4091	DNX3	2N4338
AD830	2N5520	BFW39	IT129	CM602	2N4091	DNX4	2N4869
AD831	2N5521	BFW39A	IT120	CM603	2N4091	DNX5	2N4868
AD832	2N5522	BFW54	2N3822	CM640	2N4093	DNX6	2N4338
AD833	2N5523	BFW55	2N3822	CM641	2N4093	DNX7	2N4416
AD833A	2N5524	BFW56	2N4860	CM642	2N4093	DNX8	2N4416
AD835	2N3954	BFW61	2N4224	CM643	2N4092	DNX9	2N4339
AD836	2N3955	BFX11	IT132	CM644	2N4092	DU4339	2N5397
AD837	2N3955	BFX15	IT122	CM645	2N4092	DU4340	2N5398

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
E100	2N5458	FE5459	2N5459	IRF132	**	ITC3806	IT132
E101	J204	FE5484	2N5484	IRF133	**	ITC3807	IT132
E102	2N5457	FE5485	2N5485	IRF150	**	ITC3808	IT132
E103	2N5459	FE5486	2N5486	IRF151	**	ITC3809	IT132
E105	J105	FF400	2N5457	IRF152	**	ITC3810	IT130
E106	J106	FM1100	2N3954A	IRF153	**	ITC3811	IT130
E107	J107	FM1100A	2N5906	IRF300	**	ITC4017	IT139
E108	J105	FM1101A	2N5906	IRF301	**	ITC4018	IT139
E109	J106	FM1102	2N3954	IRF305	**	ITC4019	IT139
E110	J107	FM1102A	2N5906	IRF306	**	ITC4020	IT139
E111	J111	FM1103	2N3955	IRF330	**	ITC4021	IT139
E111A	J111	FM1103A	2N5908	IRF331	**	ITC4022	IT139
E112	J112	FM1104	2N3957	IRF332	**	ITC4023	IT137
E112A	J112	FM1104A	2N5909	IRF333	**	ITC4024	IT137
E113	J113	FM1105	2N3954A	IRF350	**	ITC4025	IT137
E113A	J113	FM1105A	IT500	IRF351	**	ITE2453	IT120
E114	J204	FM1106	2N3954A	IRF352	**	ITE2639	IT120
E174	J174	FM1106A	IT500	IRF353	**	ITE2640	IT122
E175	J175	FM1107	2N3954	IRF530	**	ITE2641	IT122
E176	J176	FM1107A	IT500	IRF531	**	ITE2642	IT120
E177	J177	FM1108	2N3955	IRF532	**	ITE2643	IT122
E201	J201	FM1108A	IT502	IRF533	**	ITE2644	IT122
E202	J202	FM1109	2N3957	IRF730	**	ITE2720	IT120
E203	J203	FM1109A	IT503	IRF731	**	ITE2721	IT122
E204	J204	FM1110	2N3955	IRF732	**	ITE2722	IT120
E210	2N5397	FM1110A	2N5908	IRF733	**	ITE2903	IT122
E211	2N5397	FM1111	2N3957	IT100	IT100	ITE2913	IT122
E212	2N5397	FM1111A	2N5909	IT101	IT101	ITE2914	IT122
E230	2N4867	FM1112	2N5196	IT108	IT108	ITE2915	IT120
E231	2N4868	FM1200	2N3954	IT109	IT109	ITE2916	IT120
E232	2N4869	FM1201	2N3954	IT110	IT110	ITE2917	IT122
E270	J270	FM1202	2N3954	IT111	IT111	ITE2918	IT122
E271	J271	FM1203	2N3955A	IT120	IT120	ITE2919	IT120
E300	2N5397	FM1204	2N3955	IT120A	IT120A	ITE2920	IT120
E304	2N5486	FM1205	2N3954	IT121	IT121	ITE2936	IT120
E305	2N5484	FM1206	2N3954	IT122	IT122	ITE2937	IT120
E308	J308	FM1207	2N3954	IT124	IT124	ITE2972	IT122
E309	J309	FM1208	2N3955A	IT124A	IT124A	ITE2973	IT122
E310	J310	FM1209	2N3955	IT124B	IT124B	ITE2974	IT120
E311	J310	FM1210	2N3955A	IT125	IT125	ITE2975	IT120
E312	2N5397	FM1211	IT5911	IT126	IT126	ITE2976	IT120
E400	2N3955	FM3954	2N3954	IT127	IT127	ITE2977	IT120
E401	2N3955	FM3954A	2N3954A	IT128	IT128	ITE2978	IT120
E402	2N3957	FM3955	2N3955	IT129	IT129	ITE2979	IT120
E410	2N3955	FM3955A	2N3955A	IT130	IT130	ITE3066	2N3685
E411	IT5911	FM3956	2N3956	IT130A	IT130A	ITE3067	2N3686
E412	IT5911	FM3957	2N3957	IT131	IT131	ITE3068	2N3687
E413	2N5454	FM3958	IT5911	IT132	IT132	ITE3347	IT137
E414	2N3956	FP4339	2N4339	IT136	IT136	ITE3348	IT138
E415	2N3957	FP4340	2N4340	IT137	IT137	ITE3349	IT139
E420	IT5911	FT0654A	2N5486	IT138	IT138	ITE3350	IT137
E421	IT5912	FT0654B	2N5486	IT139	IT139	ITE3351	IT138
E430	J309(X2)	FT0654C	2N4221	IT140	IT140	ITE3680	IT120
E431	J310(X2)	FT0654D	2N4221	IT1700	IT1700	ITE3800	IT132
ESM25	U401	FT3820	2N5460	IT1701	3N172	ITE3802	IT132
ESM25A	U401	FT3820	2N5019	IT1702	3N163	ITE3804	IT130
ESM4091	2N4091	FT3909	2N5019	IT1750	IT1750	ITE3806	IT132
ESM4092	2N4092	FT703	3N161	IT2700	3N165	ITE3807	IT132
ESM4093	2N4093	FT704	3N163	IT2701	3N165	ITE3808	IT132
ESM4302	2N5457	FVN2	VN67AK	IT400	2N4392	ITE3809	IT132
ESM4303	2N5459	FVP2	**	IT404	IT404	ITE3810	IT130
ESM4304	2N5458	GET5457	2N5457	IT500	IT500	ITE3811	IT130
ESM4445	2N5432	GET5458	2N5458	IT500P	IT500	ITE3907	IT120
ESM4446	2N5434	GET5459	2N5459	IT501	IT501	ITE3908	IT120
ESM4447	2N5432	HA7807	IT132	IT501P	IT501	ITE4017	IT139
ESM4448	2N5434	HA7809	IT132	IT502	IT502	ITE4018	IT139
FE0654A	2N4386	HDIG1030	3N163	IT502P	IT502	ITE4019	IT139
FE0654B	2N5485	HEP801	2N3822	IT503	IT503	ITE4020	IT139
FE100	2N3821	HEP802	2N5484	IT503P	IT503	ITE4021	IT139
FE100A	2N3821	HEP803	2N5019	IT504	IT504	ITE4022	IT139
FE102	2N4119	HEPF0021	2N5484	IT5911	IT5911	ITE4023	IT137
FE102A	2N4119	HEPF1035	J176	IT5911	IT5911	ITE4024	IT137
FE104	2N4118	HEPF2004	2N5484	IT5912	IT5912	ITE4025	IT137
FE104A	2N4118	HEPF2005	2N5459	ITC2972	IT122	ITE4091	ITE4091
FE1600	2N4092	ID100	ID100	ITC2973	IT122	ITE4092	ITE4092
FE200	2N3821	ID101	ID101	ITC2974	IT120	ITE4093	ITE4093
FE202	2N3821	IMF3954	2N3954	ITC2975	IT120	ITE4117	2N4117
FE204	2N3821	IMF3954A	2N3954A	ITC2976	IT120	ITE4118	2N4118
FE300	2N3822	IMF3955	2N3955	ITC2977	IT120	ITE4119	2N4119
FE302	2N3821	IMF3955A	2N3955A	ITC2978	IT120	ITE4338	2N4338
FE304	2N3821	IMF3956	2N3956	ITC2979	IT120	ITE4339	2N4339
FE3819	2N5484	IMF3957	2N3957	ITC3347	IT137	ITE4340	2N4340
FE4302	2N5457	IMF3958	2N3958	ITC3348	IT138	ITE4341	2N4341
FE4303	2N5459	IMF5911	IMF5911	ITC3349	IT139	ITE4391	ITE4391
FE4304	2N5458	IMF5912	IMF5912	ITC3350	IT137	ITE4392	ITE4392
FE5245	2N4416	IMF6485	IMF6485	ITC3351	IT138	ITE4393	ITE4393
FE5246	2N5484	IRF100	**	ITC3352	IT139	ITE4416	ITE4416
FE5247	2N5486	IRF101	**	ITC3800	IT132	ITE4867	2N4867
FE5457	2N5457	IRF130	**	ITC3802	IT132	ITE4868	2N4868
FE5458	2N5458	IRF131	**	ITC3804	IT130	ITE4869	2N4869

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
IVN5000AND	IVN5000AND	J203	J203	KE3823	2N3823	LS5359	J204
IVN5000ANE	IVN5000ANE	J203-18	J203	KE3970	ITE4391	LS5360	J202
IVN5000ANF	IVN5000ANF	J204	J204	KE3971	ITE4392	LS5361	J202
IVN5000BND	IVN5000BND	J204-18	J204	KE3972	ITE4393	LS5362	J203
IVN5000BNE	IVN5000BND	J210	2N5397	KE4091	ITE4091	LS5363	J203
IVN5000BNF	IVN5000BNF	J211	2N5397	KE4092	ITE4092	LS5364	J203
IVN5000SND	IVN5000SND	J212	2N5397	KE4093	ITE4093	LS5391	2N4867A
IVN5000SNE	IVN5000SNE	J230	2N4867	KE4220	2N5457	LS5392	2N4868A
IVN5000SNF	IVN5000SNF	J231	2N4868	KE4221	2N5459	LS5393	2N4869A
IVN5001AND	IVN5001AND	J232	2N4869	KE4222	2N5459	LS5394	2N4869A
IVN5001ANE	IVN5001ANE	J270	J270	KE4223	J204	LS5395	2N4869A
IVN5001ANF	IVN5001ANF	J270-18	J270	KE4391	ITE4391	LS5396	2N4869A
IVN5001BND	IVN5001BND	J271	J271	KE4392	ITE4392	LS5457	2N5457
IVN5001BNE	IVN5001BNE	J271-18	J271	KE4393	ITE4393	LS5458	2N5458
IVN5001BNF	IVN5001BNF	J300	2N5397	KE4416	ITE4416	LS5459	2N5459
IVN5001SND	IVN5001SND	J304	2N5486	KE4856	ITE4391	LS5484	2N5484
IVN5001SNE	IVN5001SNE	J305	2N5484	KE4857	ITE4392	LS5485	2N5485
IVN5001SNF	IVN5001SNF	J308	J308	KE4858	ITE4393	LS5486	2N5486
IVN5200HND	IVN5200HND	J309	J309	KE4859	ITE4391	LS5556	2N3685
IVN5200HNE	IVN5200HNE	J310	J310	KE4860	ITE4392	LS5557	2N3684
IVN5200HNF	IVN5200HNF	J315	2N5397	KE4861	ITE4393	LS5558	2N3684
IVN5200KND	IVN5200KND	J316	U309	KE510	ITE4393	LS5638	2N5638
IVN5200KNE	IVN5200KNE	J317	U310	KE5103	J204	LS5639	2N5639
IVN5200KNF	IVN5200KNF	J3970	ITE4391	KE5104	ITE4416	LS5640	2N5640
IVN5200TND	IVN5200TND	J3971	ITE4392	KE5105	ITE4416	M103	3N161
IVN5200TNE	IVN5200TNE	J3972	ITE4393	KE511	ITE4392	M104	3N161
IVN5200TNF	IVN5200TNF	J401	IT501	KH5196	2N5196	M106	3N166
IVN5201CND	IVN5201CND	J402	IT502	KH5197	2N5197	M107	3N189
IVN5201CNE	IVN5201CNE	J403	IT503	KH5198	2N5198	M108	3N191
IVN5201CNF	IVN5201CNF	J404	IT503	KH5199	2N5199	M113	3N161
IVN5201HND	IVN5201HND	J405	IT504	LDF603	2N4221	M114	3N161
IVN5201HNE	IVN5201HNE	J406	IT505	LDF604	2N4221	M116	M116
IVN5201HNF	IVN5201HNF	J4091	ITE4091	LDF605	2N4221	M117	2N4351
IVN5201KND	IVN5201KND	J4092	ITE4092	LM114	IT120	M119	3N161
IVN5201KNE	IVN5201KNE	J4093	ITE4093	LM114A	IT120A	M163	3N163
IVN5201KNF	IVN5201KNF	J410	IT502	LM114AH	IT120A	M164	3N164
IVN5201TND	IVN5201TND	J411	IT503	LM114H	IT120	M511	3N172
IVN5201TNE	IVN5201TNE	J412	IT503	LM115	IT120	M511A	3N172
IVN5201TNF	IVN5201TNF	J420	IT5911	LM115A	IT120A	M517	3N163
IVN6657	IVN6657	J421	IT5912	LM115AH	IT120A	MA7807	IT132
IVN6658	IVN6658	J4220	J204	LM115H	IT120	MA7809	IT132
IVN6660	IVN6660	J4221	J202	LM194	IT120A	MAT-01AH	IT140
IVN6661	IVN6661	J4222	J203	LM394	IT120A	MAT-01FH	IT140
J100	2N5458	J4223	J202	LS3069	2N5458	MAT-01GH	IT140
J101	2N4338	J4224	J202	LS3070	2N5458	MAT-01H	IT140
J102	2N5457	J430	J309(X2)	LS3071	2N5458	MD1120	IT122
J103	2N5459	J4302	2N4302	LS3458	J204	MD1120F	**
J105	J105	J4303	2N5459	LS3459	J204	MD1121	IT122
J105-18	J105	J4304	2N5458	LS3460	J204	MD1122	IT122
J106	J106	J431	J310(X2)	LS3684	2N3684	MD1123	IT139
J106-18	J106	J433	2N5457	LS3685	2N3685	MD1129	IT129
J107	J107	J4338	2N5457	LS3686	2N3686	MD1129F	**
J107-18	J107	J4339	2N5457	LS3687	2N3687	MD1130	IT139
J108	J105	J4391	ITE4391	LS3819	2N5484	MD1130F	**
J108-18	J105	J4392	ITE4392	LS3821	2N5457	MD2218	IT129
J109	J106	J4393	ITE4393	LS3822	2N5458	MD2218A	IT129
J109-18	J106	J4416	ITE4416	LS3823	2N5458	MD2218AF	**
J110	J107	J4856	ITE4856	LS3921	2N3921	MD2218F	**
J110-18	J107	J4857	ITE4857	LS3922	2N3922	MD2219	IT129
J111	J111	J4858	ITE4858	LS3966	ITE4416	MD2219A	IT129
J111-18	J111	J4859	ITE4859	LS3967	ITE4416	MD2219AF	**
J111A	J111	J4860	ITE4860	LS3968	ITE4416	MD2219F	**
J111A-18	J111	J4861	ITE4861	LS3969	ITE4416	MD2369	IT129
J112	J112	J4867	2N4867	LS4220	J204	MD2369A	IT129
J112-18	J112	J4867A	2N4867A	LS4221	J202	MD2369AF	**
J112A	J112	J4867RR	2N4867	LS4222	J203	MD2369B	IT122
J112A-18	J112	J4868	2N4868	LS4223	J202	MD2369BF	**
J113	J113	J4868A	2N4868A	LS4224	J202	MD2369F	**
J113-18	J113	J4868RR	2N4868	LS4338	2N5457	MD2904	IT139
J113A	J113	J4869	2N4869	LS4339	2N5457	MD2904A	IT139
J113A-18	J113	J4869A	2N4869A	LS4340	2N5457	MD2904AF	**
J114	2N5555	J4869RR	2N4869	LS4341	2N5458	MD2904F	**
J1401	IT501	J5103	2N5484	LS4391	ITE4391	MD2905	IT139
J1402	IT502	J5104	2N5485	LS4392	ITE4392	MD2905A	IT139
J1403	IT503	J5105	2N5486	LS4393	ITE4393	MD2905AF	**
J1404	IT503	J5163	2N5486	LS4416	ITE4416	MD2905F	**
J1405	IT504	K114-18	2N5555	LS4856	ITE4091	MD2974	IT120
J1406	IT505	K210-18	2N5397	LS4857	ITE4092	MD2975	IT120
J174	J174	K211-18	2N5397	LS4858	ITE4093	MD2978	IT120
J174-18	J174	K212-18	2N5397	LS4859	ITE4091	MD2979	IT120
J175	J175	K300-18	2N5397	LS4860	ITE4092	MD3008	IT120
J175-18	J175	K304-18	2N5486	LS4861	ITE4093	MD3250	IT132
J176	J176	K305-18	2N5484	LS5103	2N5484	MD3250A	IT131
J176-18	J176	K308-18	J308	LS5104	2N5485	MD3250AF	**
J177	J177	K309-18	J309	LS5105	2N5486	MD3250F	**
J177-18	J177	K310-18	J310	LS5245	ITE4416	MD3251	IT132
J201	J201	KE3684	2N3684	LS5246	2N5484	MD3251A	IT131
J201-18	J201	KE3685	2N3685	LS5247	2N5486	MD3251AF	**
J202	J202	KE3686	2N3686	LS5248	2N5486	MD3251F	**
J202-18	J202	KE3687	2N3687	LS5358	J204	MD3409	IT129

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
MD3410	IT129	MEF5563	U403	MHQ6100	**	MPQ6100A	**
MD3467	IT139	MEM511	3N172	MHQ6100A	**	MPQ6501	**
MD3467F	**	MEM511A	3N172	MK10	2N4416	MPQ6502	**
MD3725	IT129	MEM511C	3N172	MMF1	2N5197	MPQ6600	**
MD3725F	**	MEM517	3N172	MMF2	2N3921	MPQ6600A	**
MD3762	IT139	MEM517A	3N172	MMF3	2N5198	MPQ6700	**
MD3762F	**	MEM517B	3N172	MMF4	2N3922	MPQ918	**
MD4957	IT132	MEM517C	3N172	MMF5	2N5199	MQ1120	**
MD5000	IT132	MEM550	3N189	MMF6	2N3955A	MQ1129	**
MD5000A	IT132	MEM550C	3N189	MMT3823	2N3823	MQ2218	**
MD5000B	IT132	MEM550F	3N189	MP301	IT124B	MQ2218A	**
MD7000	IT129	MEM551	3N190	MP302	IT125	MQ2219	**
MD7001	IT139	MEM551C	3N189	MP303	IT124B	MQ2219A	**
MD7001F	**	MEM556	3N172	MP310	2N4045	MQ2369	**
MD7002	IT122	MEM556C	3N172	MP311	2N4045	MQ2484	**
MD7002A	IT122	MEM560	3N161	MP312	2N4044	MQ2904	**
MD7002B	IT122	MEM560C	3N161	MP318	IT120A	MQ2905	**
MD7003	IT132	MEM561	3N163	MP350	IT132	MQ3251	**
MD7003A	IT132	MEM561C	3N163	MP351	IT130	MQ3467	**
MD7003AF	**	MEM562	2N4351	MP352	IT130	MQ3725	**
MD7003B	IT132	MEM562C	2N4351	MP358	IT130A	MQ3762	**
MD7003F	**	MEM563	2N4351	MP3954	2N3954	MQ3798	**
MD7004	IT129	MEM563C	2N4351	MP3954A	2N3954A	MQ3799	**
MD7004F	**	MEM711	M116	MP3955	2N3955	MQ3799A	**
MD7007	IT129	MEM712	M116	MP3956	2N3956	MQ7001	**
MD7007A	IT129	MEM712A	M116	MP3957	2N3957	MQ7003	**
MD7007B	IT129	MEM713	3N170	MP3958	2N3958	MQ7004	**
MD7007BF	**	MEM806	3N163	MP5905	2N5905	MQ7007	**
MD7007F	**	MEM806A	3N163	MP5906	2N5906	MQ930	**
MD708	IT129	MEM807	3N172	MP5907	2N5907	MQ982	**
MD708A	IT129	MEM807A	3N172	MP5908	2N5908	MTF101	2N5484
MD708AF	**	MEM814	3N161	MP5909	2N5909	MTF102	2N5484
MD708B	IT129	MEM816	3N172	MP5911	2N5911	MTF103	2N5457
MD708BF	**	MEM817	3N172	MP5912	2N5912	MTF104	2N5459
MD708F	**	MEM823	MFE823	MP804	2N5520	ND5700	IT120A
MD8001	IT120	MEM954	3N188	MP830	2N5520	ND5701	IT120A
MD8002	IT120	MEM954A	3N188	MP831	2N5521	ND5702	IT120
MD8003	IT122	MEM954B	3N188	MP832	2N5522	NDF9401	IT500
MD918	**	MEM955	3N190	MP833	2N5523	NDF9402	IT501
MD918A	**	MEM955A	3N190	MP835	2N3954	NDF9403	IT502
MD918AF	**	MEM955B	3N190	MP836	2N3955	NDF9404	IT503
MD918B	**	MF510	2N4092	MP837	2N3955	NDF9405	IT504
MD918F	**	MF803	2N4338	MP838	2N3956	NDF9406	IT500
MD918F	**	MF818	2N4858	MP839	2N3957	NDF9407	IT501
MD982	IT139	MFE2000	2N4416	MP841	2N5521	NDF9408	IT502
MD982F	**	MFE2001	2N4416	MP842	2N5523	NDF9409	IT503
MD984	IT139	MFE2004	2N4093	MPF102	2N5486	NDF9410	IT504
MEF103	2N5457	MFE2005	2N4092	MPF103	2N5457	NF3819	2N5484
MEF104	2N5459	MFE2006	2N4091	MPF104	2N5458	NF4302	2N5457
MEF3069	2N4341	MFE2007	2N4860	MPF105	2N5459	NF4303	2N5459
MEF3070	2N4339	MFE2008	2N4859	MPF106	2N5485	NF4304	2N5458
MEF3458	2N4341	MFE2009	2N4859	MPF107	2N5486	NF4445	2N5432
MEF3459	2N4339	MFE2010	2N4859	MPF108	2N5486	NF4446	2N5433
MEF3460	2N4338	MFE2011	2N5433	MPF109	2N5484	NF4447	2N5433
MEF3684	2N3684	MFE2012	2N5434	MPF111	2N5458	NF4448	2N5433
MEF3685	2N3685	MFE2012	2N5433	MPF112	2N5458	NF500	2N4224
MEF3686	2N3686	MFE2093	2N4338	MPF161	2N5398	NF501	2N4224
MEF3687	2N3687	MFE2094	2N4339	MPF208	2N3821	NF506	2N4416
MEF3821	2N3821	MFE2095	2N4340	MPF209	2N3821	NF5101	2N4867
MEF3822	2N3822	MFE2133	2N4860	MPF256	ITE4416	NF5102	2N4867
MEF3823	2N3823	MFE2912	2N5433	MPF4391	ITE4391	NF5103	2N4867
MEF3954	2N3954	MFE3002	3N170	MPF4392	ITE4392	NF511	2N4860
MEF3955	2N3955	MFE3003	3N164	MPF4393	ITE4393	NF5163	2N4341
MEF3956	2N3956	MFE3020	3N166	MPF820	J310	NF520	2N3684
MEF3957	2N3957	MFE3021	3N166	MPF970	J175	NF521	2N3685
MEF3958	2N3958	MFE4007	2N3686	MPF971	J175	NF522	2N3686
MEF4223	2N4223	MFE4008	2N3686	MPQ1000	**	NF523	2N3865
MEF4224	2N4224	MFE4009	2N3685	MPQ1050	**	NF530	2N4341
MEF4391	ITE4391	MFE4010	2N2608	MPQ2221	**	NF531	2N4339
MEF4392	ITE4392	MFE4011	2N2608	MPQ2222	**	NF532	2N4341
MEF4393	ITE4393	MFE4012	2N2609	MPQ2369	**	NF533	2N4339
MEF4416	ITE4416	MFE5000	**	MPQ2483	**	NF5457	2N5457
MEF4856	2N4856	MFE823	MFE823	MPQ2484	**	NF5458	2N5458
MEF4857	2N4857	MHQ2221	**	MPQ2606	**	NF5459	2N5459
MEF4858	2N4858	MHQ2222	**	MPQ2607	**	NF5484	2N5484
MEF4859	2N4859	MHQ2369	**	MPQ3303	**	NF5485	2N5485
MEF4860	2N4860	MHQ2483	**	MPQ3467	**	NF5486	2N5486
MEF4861	2N4861	MHQ2484	**	MPQ3546	**	NF5555	2N5484
MEF5103	ITE4416	MHQ2906	**	MPQ3725	**	NF5638	2N5638
MEF5104	ITE4416	MHQ2907	**	MPQ3725A	**	NF5639	2N5639
MEF5105	ITE4416	MHQ3467	**	MPQ3762	**	NF5640	2N5640
MEF5245	ITE4416	MHQ3546	**	MPQ3798	**	NF5653	2N4860
MEF5246	2N5484	MHQ3798	**	MPQ3799	**	NF5654	2N4861
MEF5247	2N5486	MHQ3799	**	MPQ3904	**	NF580	2N5432
MEF5248	2N5486	MHQ4001A	**	MPQ3906	**	NF581	2N5432
MEF5284	2N5484	MHQ4002A	**	MPQ4003	**	NF582	2N5433
MEF5285	2N5485	MHQ4013	**	MPQ4004	**	NF583	2N5434
MEF5286	2N5486	MHQ4014	**	MPQ6001	**	NF584	2N5433
MEF5561	U401	MHQ6001	**	MPQ6002	**	NF585	2N4859
MEF5562	U402	MHQ6002	**	MPQ6100	**	NF6451	U310

**CONSULT FACTORY

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NKT80421	2N4220
NKT80422	2N4220
NKT80423	2N4220
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P1005	2N5115
P1027	2N5267
P1028	2N5270
P1029	2N5270
P1069E	2N2609
P1086E	2N5115
P1087E	2N5516
P1117E	2N5640
P1118E	2N5641
P1119E	2N5640
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PF5101	2N4867
PF5102	2N4867
PF5103	2N4867
PF511	2N5114
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PL1094	2N3823
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PN4092	ITE4092
PN4093	ITE4093
PN4220	J204
PN4221	J202
PN4222	J203
PN4223	J204
PN4224	J202
PN4342	2N5461
PN4360	2N5460
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PN4392	ITE4392
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PTC152	2N5485
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SL301CT	IT129
SL301ET	IT129
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SL362C	IT129
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TD202	IT129
TD2219	IT129
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TD5433	2N5433
TD5434	2N5434
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TD709	IT122
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TD711	IT122
TD713	IT122
TIS14	2N4340
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TIS88	2N4416
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TIXS41	2N4859
TIXS42	2N5639
TIXS59	2N5459
TIXS78	2N4341
TIXS79	2N4341
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TP5116	2N5116
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U111	2N2608
U112	2N2608
U113	2N2608
U114	2N2608
U1177	2N4220
U1178	2N3821
U1179	2N3821
U1180	2N4221
U1181	2N4220
U1182	2N3821

**CONSULT FACTORY

INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
U1277	2N3684	U301	2N5115	UC714E	2N4341	VN1308N2	* *
U1278	2N3685	U3010	2N4341	UC734	2N4416	VN1308N3	* *
U1279	2N3686	U3011	2N4340	UC734E	2N4416	VN1308N6	* *
U1280	2N3684	U3012	2N4338	UC751	2N4340	VN1308ND	* *
U1281	2N3822	U304	U304	UC752	2N4340	VN1309N2	* *
U1282	2N4341	U305	U305	UC753	2N4341	VN1309N3	* *
U1283	2N4340	U306	U306	UC754	2N4340	VN1309N6	* *
U1284	2N4341	U308	U308	UC755	2N4341	VN1309ND	* *
U1285	2N4220	U309	U309	UC756	2N4340	VN1A	VN89AA
U1286	2N4341	U310	U310	UC805	2N5270	VN1B	VN67AJ
U1287	2N4092	U311	U310	UC807	2N5115	VN2	VN67AK
U1321	2N4860	U312	2N5397	UC814	2N5270	VN2A	VN89AB
U1322	2N3822	U314	2N5555	UC851	2N2608	VN2B	VN67AK
U1323	2N3822	U315	2N5397	UC853	2N2608	VN3	IVN5000ANE
U1324	2N3687	U316	U309	UC854	2N2608	VN30AA	VN30AA
U1325	2N3686	U317	U310	UC855	2N2609	VN30AB	VN30AB
U133	2N2608	U320	2N5433	UT100	2N5397	VN33AJ	VN35AJ
U1420	2N3821	U321	2N5434	UT101	2N5397	VN33AK	VN35AK
U1421	2N3822	U322	2N5433	UXC2910	IT126	VN35AA	VN35AA
U1422	2N3822	U328	* *	VCR10N	2N4869	VN35AB	VN35AB
U146	2N2608	U329	* *	VCR11N	VNR11N	VN35AJ	VN35AJ
U147	2N2608	U330	* *	VCR12N	2N3958	VN35AK	VN35AK
U148	2N2608	U331	* *	VCR13N	2N3958	VN35JA	* *
U149	2N2609	U350	* *	VCR20N	2N4341	VN3A	IVN5000ANF
U168	2N2609	U401	U401	VCR2N	VCR2N	VN3B	IVN5000AND
U1714	2N4340	U402	U402	VCR3P	VCR2P	VN4	IVN5000BNE
U1715	2N4340	U403	U403	VCR4N	VCR4N	VN40AF	VN40AF
U182	2N4857	U404	U404	VCR5P	VCR5P	VN45JA	* *
U183	2N3824	U405	U405	VCR6P	VCR6P	VN46AF	VN46AF
U1837E	2N5486	U406	U406	VCR7N	VCR7N	VN4A	IVN5000BNF
U184	2N5397	U410	2N3955	VF28	2N4392	VN4B	IVN5000BND
U1897E	U1897	U411	2N3956	VF811	2N4858	VN5	* *
U1898E	U1898	U412	2N3958	VF815	2N4858	VN5A	* *
U1899E	U1899	U421	U421	VFW40	IT122	VN5B	* *
U197	2N4338	U422	U422	VFW40A	IT120	VN64GA	* *
U198	2N4340	U423	U423	VMP1	IVN6657	VN66AF	VN66AF
U199	2N4341	U424	U424	VMP11	IVN6657	VN66AJ	VN66AJ
U1994E	2N4416	U425	U425	VMP12	IVN6658	VN66AK	VN66AK
U200	2N4861	U426	U426	VMP2	IVN6660	VN67AA	VN67AA
U201	2N4860	U430	J309(X2)	VMP21	IVN6660	VN67AB	VN67AB
U202	2N4859	U431	J310(X2)	VMP22	IVN6661	VN67AF	VN67AF
U2047E	2N4416	U440	U440	VMP4	* *	VN67AJ	VN67AJ
U221	2N4391	U441	U441	VN0104N1	VN67AJ	VN67AK	VN67AK
U222	2N4391	UC100	2N3684	VN0104N2	VN67AK	VN84GA	* *
U231	U231	UC110	2N3685	VN0104N3	IVN5000AND	VN86HF	IVN5000VNF
U232	U232	UC115	2N4340	VN0104N5	* *	VN88AF	VN88AF
U233	U233	UC120	2N3686	VN0104ND	* *	VN89AA	VN89AA
U234	U234	UC130	2N3687	VN0106N1	VN67AJ	VN89AB	VN89AB
U235	U235	UC155	2N4416	VN0106N2	VN67AK	VN89AF	VN89AF
U240	2N5432	UC1700	3N163	VN0106N3	IVN5000ANE	VN90AA	VN90AA
U241	2N5433	UC1764	3N163	VN0106N5	* *	VN90AB	VN90AB
U242	2N5432	UC20	2N3686	VN0106N6	* *	VN98AJ	VN98AJ
U243	2N5433	UC200	2N3824	VN0106ND	* *	VN98AK	VN98AK
U244	2N5433	UC201	2N3824	VN0108N1	VN99AJ	VN99AJ	VN99AJ
U248	2N5902	UC21	2N3687	VN0108N2	VN99AK	VN99AK	VN99AK
U248A	2N5906	UC210	2N4416	VN0108N3	IVN5000ANF	VND	* *
U249	2N5903	UC2130	2N5452	VN0108N5	* *	VNDA	* *
U249A	2N5907	UC2132	2N5453	VN0108N6	* *	VNDB	* *
U250	2N5904	UC2134	2N5454	VN0108ND	* *	VP0104N1	* *
U250A	2N5908	UC2136	2N5454	VN0109N2	VN99AK	VP0104N2	* *
U251	2N5905	UC2138	2N5454	VN0109N3	* *	VP0104N3	* *
U251A	2N5909	UC2139	2N3958	VN0109N5	* *	VP0104N5	* *
U252	IT5911	UC2147	2N3958	VN0109ND	* *	VP0104N6	* *
U253	IT5912	UC2148	2N3958	VN1	VN67AJ	VP0104ND	* *
U254	2N4859	UC2149	2N3958	VN1014N6	* *	VP0106N1	* *
U255	2N4860	UC220	2N3822	VN10KM	IVN5000ANE	VP0106N2	* *
U256	2N4861	UC240	2N4869	VN1204N1	IVN5200KND	VP0106N3	* *
U257	U257	UC241	2N4869	VN1204N2	IVN5200TND	VP0106N5	* *
U257/TO-71	U257/TO-71	UC250	2N4091	VN1204N5	IVN5201CND	VP0106N6	* *
U266	2N4856	UC251	2N4392	VN1204ND	* *	VP0106ND	* *
U273	2N4118A	UC2766	3N166	VN1206N1	IVN5200KNE	VP0108N1	* *
U273A	2N4118A	UC300	2N2608	VN1206N2	IVN5200TNE	VP0108N2	* *
U274	2N4119A	UC310	2N2607	VN1206N5	IVN5201CNE	VP0108N3	* *
U274A	2N4119A	UC320	2N2607	VN1206ND	* *	VP0108N5	* *
U275	2N4119A	UC330	2N2607	VN1208N1	IVN5200KNF	VP0108N6	* *
U275A	2N4119A	UC340	2N2607	VN1208N2	IVN5200TNF	VP0108ND	* *
U280	2N5452	UC40	2N2608	VN1208N5	IVN5201CNF	VP0109N1	* *
U281	2N5453	UC400	2N5270	VN1208ND	* *	VP0109N2	* *
U282	2N5453	UC401	2N5116	VN1209N1	IVN5200KNF	VP0109N3	* *
U283	2N5453	UC41	2N2608	VN1209N2	IVN5200TNF	VP0109N5	* *
U284	2N5454	UC410	2N5268	VN1209N5	IVN5201CNF	VP0109N6	* *
U285	2N5454	UC420	2N5267	VN1209ND	* *	VP0109ND	* *
U290	2N5432	UC450	2N5114	VN1304N2	* *	VP1	* *
U291	2N5434	UC451	2N5116	VN1304N3	* *	VP1A	* *
U295	2N5432	UC588	2N4416	VN1304N6	* *	VP1B	* *
U296	2N5434	UC703	2N4220	VN1304ND	* *	VP2	* *
U300	2N5114	UC704	2N4220	VN1306N2	* *	VP2A	* *
U3000	2N4341	UC705	2N4224	VN1306N3	* *	VP2B	* *
U3001	2N4339	UC707	2N4860	VN1306N6	* *	VP3	* *
U3002	2N4338	UC714	2N3822	VN1306ND	* *	VP3A	* *

**CONSULT FACTORY

INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
VP3B	**						
VP4	**						
VP4A	**						
VP4B	**						
VP5	**						
VP5A	**						
VP5B	**						
VPD	**						
VPDA	**						
VPDB	**						
W245A	ITE4416						
W245B	ITE4416						
W245C	ITE4416						
W300	2N5398						
W300A	2N5397						
W300B	2N5397						
W300C	2N5397						
W300D	2N5398						
WK5457	2N5457						
WK5458	2N5458						
WK5459	2N5459						
ZDT40	IT129						
ZDT41	IT129						
ZDT42	IT129						
ZDT44	IT129						
ZDT45	IT129						

**CONSULT FACTORY

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Switches — Junction FET

Ordering Information												
Preferred Part Number	Package	$r_{DS\ (on)}$ max Ω	V_p min/max V		I_{GSS} max pA	BV_{GSS} min V	$I_{D\ (off)}$ max pA	I_{DSS} min/max mA		t_{ap} max ns	C_{RSS} max pF	C_{iss} max pF
N-channel: Generally requires driver circuit to translate the popular logic levels to voltages required to divide the JFET.												
2N3970	TO-18	30	-4.0	-10.0	—	-40	250	50	150	50	25	6.0
2N3971	TO-18	60	-2.0	-5.0	—	-40	250	25	75	90	25	6.0
2N3972	TO-18	100	-0.5	-3.0	—	-40	250	5	30	180	25	6.0
2N4091	TO-18	30	-5.0	-10.0	-200	-40	200	30		65	16	5.0
2N4092	TO-18	50	-2.0	-7.0	-200	-40	200	15		95	16	5.0
2N4093	TO-18	80	-1.0	-5.0	-200	-40	200	8		140	16	5.0
2N4391	TO-18	30	-4.0	-10.0	-100	-40	100	50	150	55	14	3.5
2N4392	TO-18	60	-2.0	-5.0	-100	-40	100	25	75	75	14	3.5
2N4393	TO-18	100	-0.5	-3.0	-100	-40	100	5	30	100	14	3.5
2N4856	TO-18	25	-4.0	-10.0	-250	-40	250	50		34	18	6.0
2N4857	TO-18	40	-2.0	-6.0	-250	-40	250	20	100	60	18	6.0
2N4858	TO-18	60	-0.8	-4.0	-250	-40	250	8	80	120	18	6.0
2N4859	TO-18	25	-4.0	-10.0	-250	-30	250	50		34	18	8.0
2N4860	TO-18	40	-2.0	-6.0	-250	-30	250	20	100	60	18	8.0
2N4861	TO-18	60	-0.8	-4.0	-250	-30	250	8	80	120	18	8.0
2N5432	TO-52	5	-4.0	-10.0	-200	-25	200	150		41	30	15.0
2N5433	TO-52	7	-3.0	-9.0	-200	-25	200	100		41	30	15.0
2N5434	TO-52	10	-1.0	-4.0	-200	-25	200	30		41	30	15.0
2N5638	TO-92	30		-12.0	-1 nA	-30	1 nA	50		24	10	4.0
2N5639	TO-92	60		-8.0	-1 nA	-30	1 nA	25		54	10	4.0
2N5640	TO-92	100		-6.0	-1 nA	-30	1 nA	5		63	10	4.0
ITE4091	TO-92	30	-5.0	-10.0	-200	-40	200	30		65	16	5.0
ITE4092	TO-92	50	-2.0	-10.0	-200	-40	200	15		95	16	5.0
ITE4093	TO-92	80	-1.0	-10.0	-200	-40	200	8		140	16	5.0
ITE4391	TO-92	60	-4.0	-10.0	-100	-40	100	50	150	55	14	3.5
ITE4392	TO-92	100	-2.0	-10.0	-100	-40	100	25	75	75	14	3.5
ITE4393	TO-92	30	-0.5	-10.0	-100	-40	100	5	30	100	14	3.5
J105	TO-92	3	-4.5	-10.0	-3 nA	-25	3 nA	500	—	20	—	—
J106	TO-92	6	-2.0	-6.0	-3 nA	-25	3 nA	200	—	20	—	—
J107	TO-92	8	-0.5	-4.5	-3 nA	-25	3 nA	100	—	20	—	—
J111	TO-92	30	-3.0	-10.0	1 nA	35	1 nA	20		—	—	—
J112	TO-92	50	-1.0	-5.0	1 nA	35	1 nA	5		—	—	—
J113	TO-92	100	-0.5	-3.0	1 nA	35	1 nA	2		—	—	—
P-channel:												
2N3993	TO-72	150	4.0	9.5	1.2 nA	25	1.2 nA	-10			16	4.5
2N3994	TO-72	300	1.0	5.5	1.2 nA	25	1.2 nA	- 2			16	4.5
2N5114	TO-18	75	5.0	10.0	500	30	500	-30	-90	37	25	7.0
2N5115	TO-18	100	3.0	6.0	500	30	500	-15	-60	68	25	7.0
2N5116	TO-18	150	1.0	4.0	500	30	500	- 5	-25	102	25	7.0
IT100	TO-18	75	2.0	4.5	200	35	100	-10			35	12.0
IT101	TO-18	60	4.0	10.0	200	35	100	-20			35	12.0
J174	TO-92	85	5.0	10.0	1 nA	30	-1 nA	-20	-100	—	—	—
J175	TO-92	125	3.0	6.0	1 nA	30	-1 nA	- 7	-60	—	—	—
J176	TO-92	250	1.0	4.0	1 nA	30	-1 nA	- 2	-25	—	—	—
J177	TO-92	300	0.8	2.25	1 nA	30	-1 nA	-1.5	-20	—	—	—
J270	TO-92	—	0.5	2.0	200	30	—	- 2	-15	—	20	5.0
J271	TO-92	—	1.5	4.5	200	30	—	- 6	-50	—	20	5.0
P1086	TO-92	75	—	10.0	2 nA	30	-10 nA	-10.0	—	15	45	10
P1087	TO-92	150	—	5.0	2 nA	30	-10 nA	- 5.0	—	25	45	10

Switches and Amplifiers — MOSFET

Ordering Information Preferred Part Number	Package	$V_{GS\ (TH)}$ $V_{GS(off)}$ min/max V		BV_{GSS} min V	I_{DSS} max pA	I_{GSS} max pA	G_{fs} min µmho	$r_{DS\ (on)}$ max Ω		$I_{Q\ (on)}$ min mA	
P-Channel Enhancement: Gen. used where max isolation between signal source and logic drive required: sw. "On" resistance varies with signal amplitude.											
3N161	TO-72	-1.5	-5.0	-25	-10 nA	-100.0	3500.0	—	-40	-120	Diode Protected
3N163	TO-72	-2.0	-5.0	-40	-200	-10.0	2000.0	250	- 5	- 30	
3N164	TO-72	-2.0	-5.0	-30	400	10.0	1.0	300	- 3	- 30	
3N172	TO-72	-2.0	-5.0	-40	-400	-10.0	1500.0	250	- 5	- 30	Diode Protected
3N173	TO-72	-2.0	-5.0	-30	-10 nA	-500.0	—	350	- 5	- 30	
IT1700	TO-72	0.2	-5.0	-40	200	10.0	2.0	400	2	—	
N-Channel Enhancement: Can switch positive signals directly from TTL logic; gen. requires driver or translator circuit to switch bipolar signals.											
2N4351	TO-72	1.0	5.0	25	10 nA	10.0	1000.0	300	3		
2N170	TO-72	1.0	2.0	25	10 nA	10.0	1000.0	200	10		
2N171	TO-72	1.5	3.0	25	10 nA	10.0	1000.0	200	10		
IT1750	TO-72	0.5	3.0	25	10 nA	10.0	30.0	50	10	100	
M116	TO-72	1.0	5.0	30	—	100.0	—	100	—		Diode Protected

Amplifiers—N-Channel Junction FET

Ordering Information Preferred Part Number	Package	g_{fs} min µ mho	I_{DSS} min/max mA		V_p min/max V		I_{GSS} max pA	BV_{GSS} min V	C_{iss} max pF	C_{rss} max pF	e_n max nv/√Hz
2N3684	TO-72	2000	2.5	7.5	-2.0	-5.0	-100	-50	4	1.2	140 @ 100 Hz
2N3685	TO-72	1500	1.0	3.0	-1.0	-3.5	-100	-50	4	1.2	140 @ 100 Hz
2N3686	TO-72	1000	0.4	1.2	-0.6	-2.0	-100	-50	4	1.2	140 @ 100 Hz
2N3687	TO-72	500	0.1	0.5	-0.3	-1.2	-100	-50	4	1.2	140 @ 100 Hz
2N3821	TO-72	1500	0.5	2.5	-4.0		-100	-50	6	3.0	200 @ 10 Hz
2N3822	TO-72	3000	2.0	10.0		-6.0	-100	-50	6	3.0	200 @ 10 Hz
2N3823	TO-72	3500	4.0	20.0	-8.0		-500	-30	6	2.0	—
2N3824	TO-72	—	—	—			-100	-50	6	2.0	—
2N4117	TO-72	70	0.03	0.09	-0.6	-1.8	-10	-40	3	1.5	
2N4117A	TO-72	70	0.03	0.09	-0.6	-1.8	-1	-40	3	1.5	
2N4118	TO-72	80	0.08	0.24	-1.0	-3.0	-10	-40	3	1.5	
2N4118A	TO-72	80	0.08	0.24	-1.0	-3.0	-1	-40	3	1.5	
2N4119	TO-72	100	0.2	0.6	-2.0	-6.0	-10	-40	3	1.5	
2N4119A	TO-72	100	0.2	0.6	-2.0	-6.0	-1	-40	3	1.5	
2N4220	TO-72	1000	0.5	3.0		-4.0	-100	-30	6	2.0	
2N4221	TO-72	2000	2.0	6.0		-6.0	-100	-30	6	2.0	
2N4222	TO-72	2500	5.0	15.0		-8.0	-100	-30	6	2.0	
2N4223	TO-72	3000	3.0	18.0	-0.1	-8.0	-250	-30	6	2.0	
2N4224	TO-72	2000	2.0	20.0	-0.1	-0.8	-150	-30	6	2.0	
2N4338	TO-18	600	0.2	0.6	-0.3	-1.0	-100	-50	7	3.0	65 @ 1 kHz
2N4339	TO-18	800	0.5	1.5	-0.6	-1.8	-100	-50	7	3.0	65 @ 1 kHz
2N4340	TO-18	1300	1.2	3.6	-1.0	-3.0	-100	-50	7	3.0	65 @ 1 kHz
2N4341	TO-18	2000	3.0	9.0	-2.0	-6.0	-100	-50	7	3.0	65 @ 1 kHz
2N4416	TO-72	4500	5.0	15.0		-6.0	-100	-30	4	2.0	
2N4867	TO-72	700	0.4	1.2	-0.7	-2.0	-250	-40	25	5.0	10 @ 1 kHz
2N4867A	TO-72	700	0.1	1.2	-0.7	-2.0	-250	-40	25	5.0	5 @ 1 kHz
2N4868	TO-72	1000	1.0	3.0	-1.0	-3.0	-250	-40	25	5.0	10 @ 1 kHz
2N4868A	TO-72	1000	1.0	3.0	-1.0	-3.0	-250	-40	25	5.0	5 @ 1 kHz
2N4869	TO-72	1300	2.5	7.5	-1.8	-5.0	-250	-40	25	5.0	10 @ 1 kHz
2N4869A	TO-72	1300	2.5	7.5	-1.8	-5.0	-250	-40	25	5.0	5 @ 1 kHz
2N5397	TO-72	6000	10.0	30.0	-1.0	-6.0	-100	-25	5	1.2	3 dB @ 450 MHz
2N5398	TO-72	5000	5.0	40.0	-1.6	-0.1	-100	-25	5.5	1.3	
2N5457	TO-92	1000	1.0	5.0	-0.5	-6.0	1 nA	25	7	3.0	3 dB @ 450 MHz
2N5458	TO-92	1500	2.0	9.0	-1.0	-7.0	1 nA	25	7	3.0	3 dB @ 450 MHz
2N5459	TO-92	2000	4.0	16.0	-2.0	-8.0	-1 nA	-25	7	3.0	3 dB @ 450 MHz

Amplifiers — N-Channel Junction FET continued

2N5484	TO-92	3000	1.0	5.0	-0.3	-0.3	-1 nA	-25	5	1.0	120 @ 1 kHz
2N5485	TO-92	3500	4.0	10.0	-0.5	-4.0	-1 nA	-25	5	1.0	120 @ 1kHz
2N5486	TO-92	4000	8.0	20.0	-2.0	-6.0	-1 nA	-30	5	1.0	120 @ 1 kHz
ITE4416	TO-92	4500	5.0	15.0		-6.0	-100	-30	4	2.0	
J201	TO-92	500	0.2	1.0	-0.3	-1.5	-100	-40	4	1.0	5 @ 1 kHz
J202	TO-92	1000	0.9	4.5	-0.8	-4.0	-100	-40	4	1.0	5 @ 1 kHz
J203	TO-92	1500	4.0	20	-2.0	-10.0	-100	-40	4	1.0	5 @ 1 kHz
J204	TO-92	1500	1.2	typ	-0.5	-2.0	-100	-25	4	1.0	10 @ 1 kHz
J308	TO-92	8000	12.0	60.0	-1.0		-1 nA	-25	—	—	10 @ 100 Hz
J309	TO-92	10,000	12.0	30.0	-1.0		-1 nA	-25	—	—	10 @ 100 Hz
J310	TO-92	8000	24.0	60.0	-2.0		-1 nA	-25	—	—	10 @ 100 Hz
U308	TO-52	10,000	12.0	60.0	-1.0	-6.0	-150	-25	7 typ.	4.0 typ.	10 @ 10 Hz typ.
U309	TO-52	10,000	12.0	30.0	-1.0	-4.0	-150	-25	7 typ.	4.0 typ.	10 @ 10 Hz typ.
U310	TO-52	10,000	24.0	60.0	-2.5	-6.0	-150	-25	7 typ.	4.0 typ.	10 @ 10 Hz typ.

Amplifiers — P-Channel Junction FET

Ordering Information Preferred Part Number	Package	g_{fs} min μ mho	I_{DSS} min/max mA		V_P min/max V		I_{GSS} max nA	BV_{GSS} min V	C_{iss} max pF	C_{rss} max pF	e_n max nv/√ Hz
2N2607	TO-18	330	-0.3	-1.5	1.0	4.0	3	30	7	2	400 @ 1 kHz
2N2608	TO-18	1000	-0.9	-4.5	1.0	4.0	10	30	7	2	180 @ 1 kHz
2N2609	TO-18	2500	-2.0	-10.0	1.0	4.0	30	30	7	2	180 @ 1 kHz
2N5460	TO-92	1000	-1.0	-5.0	0.75	6.0	5	40	7	2	115 @ 100 Hz
2N5461	TO-92	1500	-2.0	-9.0	1.0	7.5	5	40	7	2	115 @ 100 Hz
2N5462	TO-92	2500	-4.0	-16.0	1.5	9.0	5	40	7	2	115 @ 100 Hz
2N5463	TO-92	1000	-1.0	-5.0	0.75	6.0	5	60	7	2	115 @ 100 Hz
2N5464	TO-92	1500	-2.0	-9.0	1.0	7.5	5	60	7	2	115 @ 100 Hz
2N5465	TO-92	2500	-4.0	-16.0	1.8	9.0	5	60	7	2	115 @ 100 Hz
U304	TO-18		-30	-90		5	.5	30	27	7	—
U305	TO-18		-15	-60		3	.5	30	27	7	—
U306	TO-18		-5	-25		1	.5	30	27	7	—

Differential Amplifiers — Dual Monolithic N-Channel Junction FETs

Ordering Information Preferred Part Number	Package	V_{GSI-2} max mV	ΔV_{GS} max μV/°C	I_G max pA	BV_{GSS} min V	V_P min/max V		g_{fs} min/max μ mho		I_{DSS} min/max mA		e_n max nV/ √ Hz
2N3921	T0-71	5	10	-250	-50	-	-3.0	1500	7500	1.0	10.0	—
2N3922	T0-71	5	25	-250	-50	-	-3.0	1500	7500	1.0	10.0	—
2N3954	T0-71	5	10	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3954A	T0-71	5	5	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3955	T0-71	10	25	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3955A	T0-71	10	10	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3956	T0-71	15	50	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3957	T0-71	20	75	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3958	T0-71	25	100	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100 Hz
2N5196	T0-71	5	5	-15	-50	-0.7	-4.0	700 @ 200 μA		0.7	7.0	20 @ 1 kHz
2N5197	T0-71	5	10	-15	-50	-0.7	-4.0	700 @ 200 μA		0.7	7.0	20 @ 1 kHz
2N5198	T0-71	10	20	-15	-50	-0.7	-4.0	700 @ 200 μA		0.7	7.0	20 @ 1 kHz
2N5199	T0-71	15	40	-15	-50	-0.7	-4.0	700 @ 200 μA		0.7	7.0	20 @ 1 kHz
2N5452	T0-71	5	5	IGSS-100	-50	-1.0	-4.5	1	4	0.5	5.0	20 @ 1 kHz
2N5453	T0-71	10	10	IGSS-100	-50	-1.0	-4.5	1	4	0.5	5.0	20 @ 1 kHz
2N5454	T0-71	15	25	IGSS-100	-50	-1.0	-4.5	1	4	0.5	5.0	20 @ 1 kHz
2N5515	T0-71	5	5	-100	-40	-0.7	-4.0	1	4	0.5	7.5	30 @ 10 Hz
2N5516	T0-71	5	10	-100	-40	-0.7	-4.0	1	4	0.5	7.5	30 @ 10 Hz
2N5517	T0-71	10	20	-100	-40	-0.7	-4.0	1	4	0.5	7.5	30 @ 10 Hz
2N5518	T0-71	15	40	-100	-40	-0.7	-4.0	1	4	0.5	7.5	30 @ 10 Hz
2N5519	T0-71	15	80	-100	-40	-0.7	-4.0	1	4	0.5	7.5	30 @ 10 Hz
2N5520	T0-71	5	5	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10 Hz
2N5521	T0-71	5	10	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10 Hz
2N5522	T0-71	10	20	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10 Hz
2N5523	T0-71	15	40	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10 Hz
2N5524	T0-71	15	80	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10 Hz
2N5564	T0-71	5	10	—	-40	-0.5	-3.0	7.5	12.5	5.0	30.0	10 @ 10 Hz
2N5565	T0-71	10	25	—	-40	-0.5	-3.0	7.5	12.5	5.0	30.0	10 @ 10 Hz
2N5566	T0-71	20	50	—	-40	-0.5	-3.0	7.5	12.5	5.0	30.0	10 @ 10 Hz
2N5902	T0-99	5	5	-3	-40	-0.6	-4.5	70	250	0.3	0.5	100 @ 1 kHz
2N5903	T0-99	5	10	-3	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1 kHz
2N5904	T0-99	10	20	-3	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1 kHz
2N5905	T0-99	15	40	-3	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1 kHz
2N5906	T0-99	5	5	-1	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1 kHz
2N5907	T0-99	5	10	-1	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1 kHz
2N5908	T0-99	10	20	-1	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1 kHz
2N5909	T0-99	15	40	-1	-40	-0.6	-4.5	70	250	0.03	.05	100 @ 1 kHz
2N5911	T0-99	10	20	-100	-25	-1.0	-5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10 kHz
2N5912	T0-99	15	40	-100	-25	-1.0	-5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10 kHz
2N6483	T0-71	5	5	-100	-50	-0.7	-4.0	1000	4000	0.5	7.5	10 @ 10 Hz
2N6484	T0-71	15	10	-100	-50	-0.7	-4.0	1000	4000	0.5	7.5	10 @ 10 Hz
2N6485	T0-71	15	25	-100	-50	-0.7	-4.0	1000	4000	0.5	7.5	10 @ 10 Hz
IMF5911	T0-99	10	20	-100	-25	-1.0	-5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10 kHz
IMF5912	T0-99	15	40	-100	-25	-1.0	-5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10 kHz
IMF6485	T0-71	25	40	-100	-50	-0.7	-4.0	1000	4000	0.5	7.5	15 @ 10 Hz
IT500	T0-52	5	5	-5	-50	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10 Hz
IT501	T0-52	5	10	-5	-50	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10 Hz
IT502	T0-52	10	20	-5	-50	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10 Hz
IT503	T0-52	15	40	-5	-50	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10 Hz
IT504	T0-52	25	100	-5	-25	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10 Hz
IT505	T0-52	50	200	-5	-25	-0.7	-4.0	700	1600	0.7	7.0	35 @ 10 Hz
IT5911	T0-52	10	20	-100	-25	-1.0	-5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10 kHz
IT5912	T0-52	15	40	-100	-25	-1.0	-5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10 kHz
U257	T0-99	100	—	-100	-25	-1.0	-5.0	5000	10000	5.0	40.0	30 @ 10 kHz
U401	T0-71	5	10	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U402	T0-71	10	10	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U403	T0-71	10	25	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U404	T0-71	15	25	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U405	T0-71	20	40	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U406	T0-71	40	80	-15	-50	-0.5	-2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U421	T0-99	10	10	0.1	-60	-0.4	-2.0	300	800	60-1000μA		20 @ 10 Hz
U422	T0-99	15	25	0.1	-60	-0.4	-2.0	300	800	60-1000μA		20 @ 10 Hz
U423	T0-99	25	40	0.1	-60	-0.4	-2.0	300	800	60-1000μA		20 @ 10 Hz
U424	T0-99	10	10	0.5	-60	-0.4	-3.0	300	1000	60-1800μA		20 @ 10 Hz
U425	T0-99	15	25	0.5	-60	-0.4	-3.0	300	1000	60-1800μA		20 @ 10 Hz
U426	T0-99	25	40	0.5	-60	-0.4	-3.0	300	1000	60-1800μA		20 @ 10 Hz

Differential Amplifiers — Dual Monolithic P-Channel MOSFETS (Enhancement)

Ordering Information Preferred Part Number	Package	$V_{GS(TH)}$ min/max V		BV_{OSS} min/max V	I_{DSS} max pA	I_{GSS} max pA	g_{fs} min µmho	$I_{D(on)}$ min/max mA		$r_{DS(on)}$ max Ω	$V_{GS\ 1-2}$ max mV
3N165	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300	100
3N166	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300	
3N188	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300	100 Zener Protected
3N189	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300	Zener Protected
3N190	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300	
3N191	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300	

Differential Amplifiers — Dual NPN Bipolar Transistors

Ordering Information Preferred Part Number	Package	$V_{BE\ 1-2}$ mV max	ΔV_{BE} µV/°C max	h_{FE} @ I_C = 10 µA V_{CE} = 5V min	$I_{B\ 1-2}$ @ I_C = 10 µA V_{CE} = 5V nA max	BV_{CEO} V min	I_{CBO} nA max	Noise dB max	f_t MHz @ I_C min	C_{obo} pF max	Structure
2N4044	TO-78	3	3	200	5	60	.1	2	200 @ 1 mA	0.8	Dielec. Isol.
2N4045	TO-78	5	10	80	25	45	.1	3	150 @ 1 mA	0.8	Dielec. Isol.
2N4100	TO-78	5	5	150	10	55	.1	3	150 @ 1 mA	0.8	Dielec. Isol.
2N4878	TO-71	3	3	200	5	60	.1	2	200 @ 1 mA	0.8	Dielec. Isol.
2N4879	TO-71	5	5	150	10	55	.1	3	150 @ 1 mA	0.8	Dielec. Isol.
2N4880	TO-71	5	10	80	25	45	.1	3	150 @ 1 mA	0.8	Dielec. Isol.
IT120	TO-78 TO-71	2	5	200	5	45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT120A	TO-78 TO-71	1	3	200	2.5	45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT121	TO-78 TO-71	3	10	80	25	45	1	2 typ.	180 @ 1 mA	2	Junc. Isol.
IT122	TO-78 TO-71	5	20	80	25	45	1	2 typ.	180 @ 1 mA	2	Junc. Isol.
IT124	TO-78	5	10	1500	0.6A V_{CE} = 1 V	2	.1	3	100 @ 200 µA	0.8	Dielec. Isol.
IT126	TO-78 TO-71	1	3	200	2.5	60	.1	1 typ.	250 @ 10 mA	4	Dielec. Isol.
IT127	TO-78 TO-71	2	5	200	5	45	.1	1 typ.	250 @ 10 mA	4	Dielec. Isol.
IT128	TO-78 TO-71	5	10	100	10	45	.5	1 typ.	250 @ 10 mA	4	Dielec. Isol.
IT129	TO-78 TO-71	10	20	100	25	45	.5	1 typ.	250 @ 10 mA	4	Dielec. Isol.
IT140	TO-71	1	3	300	2.5	22	1	2 typ.	250 @ 10 mA	2	Junc. Isol.

Differential Amplifiers — Dual PNP Bipolar Transistors

Ordering Information											
Preferred Part Number	**Package**	$V_{BE\ 1-2}$ mV max	ΔV_{BE} µV/°C max	h_{FE} @ $I_C = 10\ \mu A$ $V_{CE} = 5V$ min	$I_{b\ 1-2}$ @ $I_C = 10\ \mu A$ $V_{CE} = 5V$ nA max	BV_{CEO} V min	I_{CBO} nA max	Noise dB max	f_t MHz @ I_C min	C_{obo} pF max	**Structure**
2N5117	TO-78	3	3	100	10	45	.1	4	100 @ 0.5 mA	.8	Junc. Isol.
2N5118	TO-78	5	5	100	15	45	.1	4	100 @ 0.5 mA	.8	Junc. Isol.
2N5119	TO-78	5	15	50	40	45	.1	4	100 @ 0.5 mA	.8	Junc. Isol.
IT130	TO-78 TO-71	2	5	200	5	−45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT130A	TO-78 TO-71	1	3	200	2.5	−60	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT131	TO-78 TO-71	5	10	80	10	−45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT132	TO-78 TO-71	10	20	80	25	−45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT136	TO-78 TO-71	1	3	200	2.5	−60	.1	2 typ.	250 @ 10 mA	4	Dielec. Isol.
IT137	TO-78 TO-71	2	5	200	5	−45	.1	2 typ.	250 @ 10 mA	4	Dielec. Isol.
IT138	TO-78 TO-71	5	10	100	10	−45	.5	2 typ.	250 @ 10 mA	4	Dielec. Isol.
IT139	TO-78 TO-71	10	20	100	25	−45	.5	2 typ.	250 @ 10 mA	4	Dielec. Isol.

Specialty Items

IC-100 ID-101	This product is a back to back diode combination used to protect those P-channel MOSFET duals which are not diode protected. Their chief characteristic is <1 pA leakage when voltage across them is less than 5 mV. If voltage across diodes is adjusted to 0V ±0.1 mV, leakage is less than 0.01 pA.
VCR2N VCR3P VCR4N VCR5P VCR7N VCR11N (Dual)	The VCR family consists of three terminal variable resistors where the resistance value between two of the terminals is controlled by the voltage potential applied to the third.

Note: Intersil offers the following military qualified devices:*

N-channel switches	N-channel amplifiers	P-channel switches	P-channel amplifiers
2N4091 JAN, JANTX, JANTXV	2N3821 JAN, JANTX, JANTXV	2N5114 JAN, JANTX, JANTXV	2N2609 JAN
2N4092 JAN, JANTX, JANTXV	2N3823 JAN, JANTX, JANTXV	2N5115 JAN, JANTX, JANTXV	
2N4093 JAN, JANTX, JANTXV		2N5116 JAN, JANTX, JANTXV	
2N4856 JAN, JANTX, JANTXV			
2N4857 JAN, JANTX, JANTXV			
2N4858 JAN, JANTX, JANTXV			

*JAN processing consists of a sample Group B pulled from the production run.
JANTX processing consists of JAN processing plus 100% electrical read and record, and 100% burn-in.
JANTVX processing consists of JANTX processing plus 100% pre-cap visual and on-shore assembly.

DISCRETE SELECTOR GUIDE

	Detailed Application	Important Parameters	Recommended Part Numbers							
			Single N-Channel JFET	Single P-Channel JFET	Dual N-Channel JFET	Single N-Channel MOSFET	Single P-Channel MOSFET	Dual P-Channel MOSFET	Dual NPN Bipolar	Dual PNP Bipolar
Amplifiers	Audio	low noise	2N4220, 2N3821	2N2607 2N5460	2N3958 IT500-5	2N4351 3N170-1	3N163 3N164		2N4044	IT130
	Buffer	low leakage, high gain	2N4221	2N2609 2N5462	2N5905 U426	M116 IT1750	3N172 IT1700		IT120	IT136
	Differential	good matching & drift	—	—	2N3954 U401	—	—	3N165	IT126 IT140	2N3810
	Fet Input Op Amp		—	—	2N5515	—	—		—	—
	High Impedance	low leakage	2N4117A	IT100 J176 2N5116	2N5905 IT503 U426	IT1750	IT1700		—	—
	High Frequency	high gain, low capacitance	U308 2N5397	2N5114 J176	2N5912 IT5912	2N4351	3N163 3N164	3N188	2N4044 IT120	IT130 IT136
	Low Supply Voltage	low pinch-off voltage	2N4338 2N3687	2N5265 J177	U406 2N3958	3N170-1			IT126 IT140	2N3810
	Low Noise	low noise	2N4867A	2N5116 J176	2N5519 2N5199	M116	3N172		—	—
	Preamplifier	high gain	2N5397 U310	2N5116 J176	2N5566 U406				2N4044 IT120	IT130 IT136
	Video	high gain, low capacitance	2N4393 ITE4393	IT100	IT5912 2N5912				IT126 IT140	2N3810
Mixers	VHF	RF parameters,	U310 2N5397	IT100 J174	2N6485 IT5912	—	—	—	—	—
	UHF	high g_{fs}/C_{iss}	J310 2N5484	2N5114	2N5912					
Switches	Commutators	low C_{rss}	2N4392 ITE4391	2N3993-4		IT1750	IT1700			
	Sample and Hold			2N5114-6	2N5564-6		3N163	3N165		
	Analog Gates	fast switching,	2N4091-3 2N4391-3	2N5114-6	2N5912				—	—
	Digital	low $r_{DS(on)}$	ITE4391-3	J174-7		3N170-1	3N164	3N188		
	Chopper		2N5432-4	IT100-1			3N172			
	Integrator Reset	low $r_{DS(on)}$, high I_{DSS}	J111-3 J105-7							
Voltage Control Resistors	Gain Control Amplitude Stability Attenuators	high $V_{GS(off)}$	VCR2N VCR4N VCR7N	VCR3P VCR5P	VCR11N	—	—	—	—	—
Protection Diodes	Signal Clipping and Clamping	low leakage current	—	—	—	—	—	—	ID100-1	—

VCR2N/3P/4N/5P/7N Voltage-Controlled Resistors

APPLICATIONS

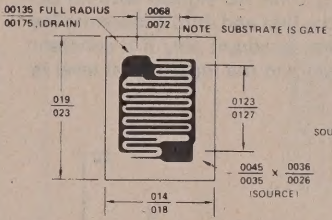
- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage 15V
Gate Current .... 10 mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0 mW/°C to 175°C) ...... 300 mW
Storage Temperature Range ......−55 to +175°C

CHIP TOPOGRAPHY

VCR2N
5001B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0045
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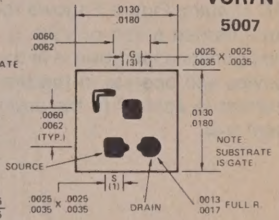
x
0036
0026
(SOURCE)
014
018

VCR7N
5007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x
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SOURCE
0130
0180
NOTE
SUBSTRATE
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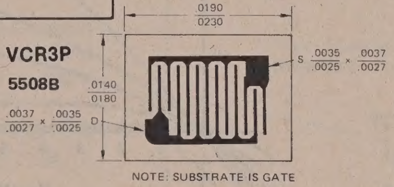
DRAIN
0013
0017
FULL R

VCR3P
5508B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S
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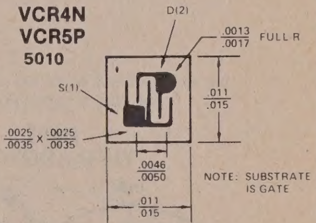
NOTE: SUBSTRATE IS GATE

VCR4N
VCR5P
5010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FULL R
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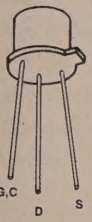
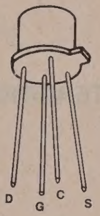
NOTE: SUBSTRATE
IS GATE
.011
.015

PIN CONFIGURATIONS

TO-18



TO-72



ORDERING INFORMATION

TO-18	TO-72	WAFER	DICE
VCR2N		VCR2N/W	VCR2N/D
VCR4N		VCR4N/W	VCR4N/D
	VCR3P	VCR3P/W	VCR3P/D
	VCR5P	VCR5P/W	VCR5P/D
	VCR7N	VCR7N/W	VCR7N/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

N-Channel VCR FETs

		Characteristic		VCR2N		VCR4N		VCR7N		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		−5		−0.2		−0.1	nA	V_{GS} = −15V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	−15		−15		−15		V	I_G = −1 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−3.5	−7	−3.5	−7	−2.5	−5		I_D = 1 μA, V_{DS} = 10V	
4		$r_{ds(on)}$	Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		7.5		3		1.5	pF	V_{GD} = −10V, I_S = 0	f = 1 MHz
6		C_{sgo}	Source-Gate Capacitance		7.5		3		1.5		V_{GS} = −10V, I_D = 0	

P-Channel VCR FETs

		Characteristic		VCR3P		VCR5P		Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		20		10	nA	V_{GS} = 15V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	15		15		V	I_G = 1μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	3.5	7	3.5	7		I_D = −1μA, V_{DS} = −10V	
4		$r_{ds(on)}$	Drain-Source ON Resistance	70	200	300	900	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		6		3	pF	V_{GD} = 10V, I_S = 0	f = 1 MHz
6		C_{sgo}	Source-Gate Capacitance		6		3		V_{GS} = 10V, I_D = 0	

Intersil cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in an Intersil product. No other circuit patent licenses are implied. Intersil reserves the right to change the circuitry and specifications without notice at any time.

JFETS AS VOLTAGE CONTROLLED RESISTORS

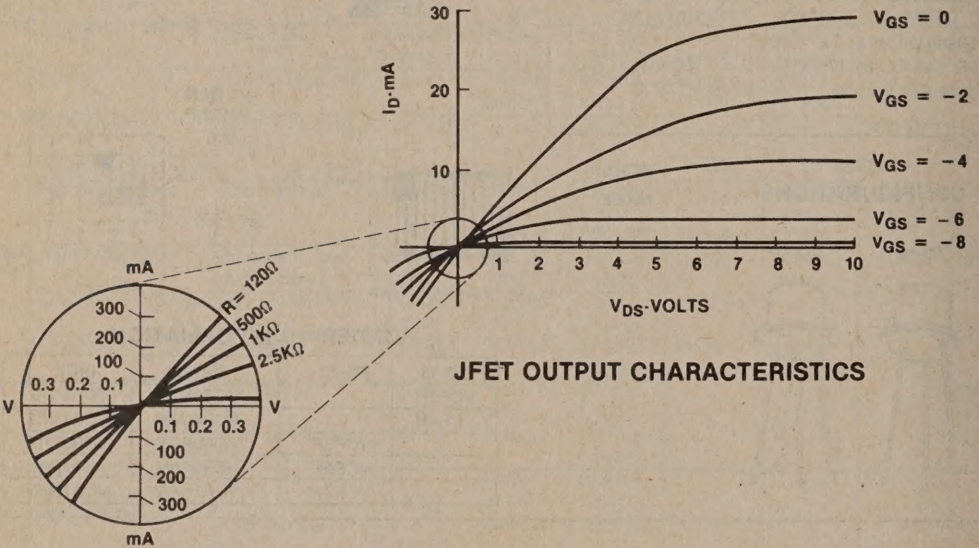
The voltage controlled resistor is a junction field effect transistor whose drain to source ON resistance is controlled by gate to source voltage.

The gate control terminal is high impedance thereby allowing negligible control current. The gate voltage is zero for minimum resistance, and increases as the gate voltage approaches the pinch-off voltage.

This VCR is intended for use on applications using low level AC signals. Figure 1 shows the output characteristics, with an enlarged graph of VDS = 0 for AC signals with no DC component. Operation is in the first and third quadrants; the device will operate in the first quadrant only if a constant current is applied to the drain and the input signal level is kept low.

Figure 1 also shows that certain combinations of gate control voltage and signal levels will cause resistance modulation. This distortion may be improved by introducing local feedback as shown in figure 2 for best frequency response and impedance levels; eliminating the feedback capacitor will require the gate control voltage to be double for the same ON resistance. The resistor values should be equal, and about 100kΩ.

Best gate control voltage for best linearity is up to about $0.8V_{PK}$; ON resistance increases rapidly beyond this point.



JFET OUTPUT CHARACTERISTICS

JFET OUTPUT CHARACTERISTICS
ENLARGED AROUND V_{DS} = 0

FIGURE 1

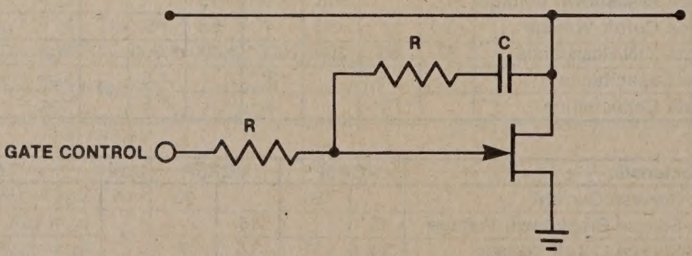


FIGURE 2

ID100, ID101
Low Leakage Monolithic Dual Diode

FEATURES

- **I_R = 0.1 pA (typical)**
- **BV_R > 30 V**
- **C_r = 0.75 pF (typical)**

GENERAL DESCRIPTION

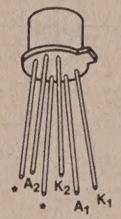
The ID100 and ID101 are monolithic dual diodes intended for use in applications requiring extremely low leakage currents. Applications include interstage coupling with reverse isolation, signal clipping and clamping and protection of ultra low leakage FET differential dual and operational amplifiers.

ABSOLUTE MAXIMUM RATINGS
(@ 25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Currents	
V_R Reverse Voltage	30 V
$V_{D_1D_2}$ Diode to Diode Voltage	±50 V
I_F Forward Current	20 mA
I_R Reverse Current	100 µA

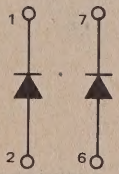
PIN CONFIGURATIONS

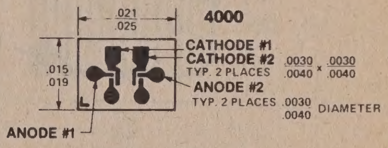
TO-71
TO-78



* These leads are not to be tied together nor connected to the circuit in any way.

CHIP TOPOGRAPHY





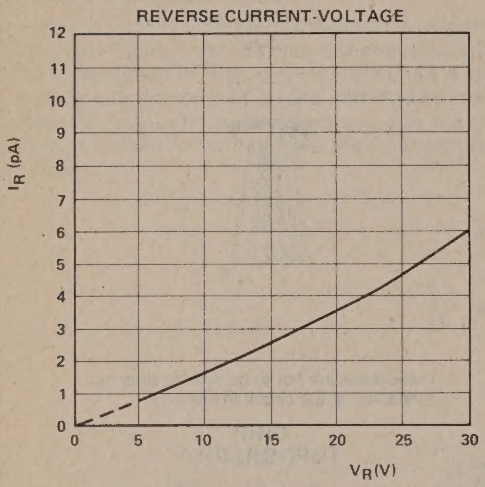
ORDERING INFORMATION

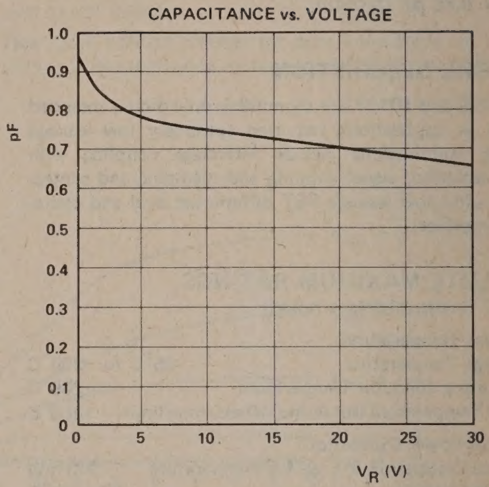
TO78	TO71	WAFER	CHIP
ID100	ID101	ID100/W	ID101/D

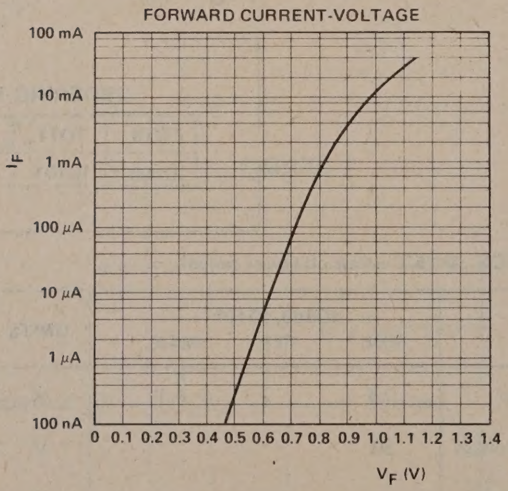
ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		ID100, ID101			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
V_F	Forward Voltage Drop	0.8		1.1	V	I_F = 10 mA
BV_R	Reverse Breakdown Voltage	30			V	I_R = 1 µA
I_R	Reverse Leakage Current		0.1		pA	V_R = 1 V, T_A = 25°C
			2.0	10	pA	V_R = 10 V, T_A = 25°C
				10	nA	V_R = 10 V, T_A = 125°C
$\lvert I_{R_1} - I_{R_2} \rvert$	Differential Leakage Current			3	pA	V_R = 10 V
C_r	Total Reverse Capacitance		0.75	1	pF	V_R = 10 V, f = 1 MHz

TYPICAL CHARACTERISTICS OF ID100/ID101







INTERSIL

IT100, IT101
P-Channel JFET

FEATURES

- **Interfaces Directly with T²L Logic Elements so that No Extra Driver Stage is Required.**
- **$r_{DS(on)} < 75\Omega$ for 5V Logic Drive**
- **$I_{D(off)} < 100$ pA**

GENERAL DESCRIPTION

This P-channel JFET has been designed to directly interface with T²L logic, thus eliminating the need for costly drivers, in analog gate circuitry. Bipolar inputs of ±15 V can be switched. The FET is OFF for hi level inputs (+5 V or +15 V) and ON for low level inputs (< 0.5 V for IT100 < 1.5 V for IT101.

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation

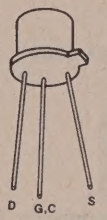
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	35V
V_{GD}	Gate to Drain Voltage	35V
I_G	Gate Current	50 mA

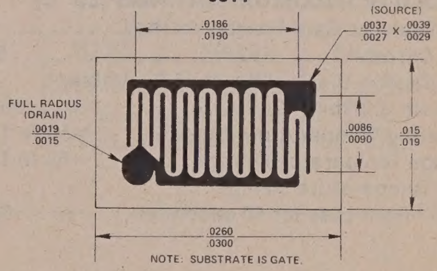
PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

5514



NOTE: SUBSTRATE IS GATE.

ORDERING INFORMATION

TO-18	WAFER	DICE
IT100	IT100/W	IT100/D
IT101	IT101/W	IT101/D

ELECTRIC CHARACTERISTICS @ 25°C (unless otherwise noted)

	CHARACTERISTIC	IT100		IT101		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{DSS}	Max Drain Current	-10	–	-20	–	mA	$V_{GS} = 0, V_{DS} = -15$ V
V_P	Pinch Off Voltage	2	4.5	4	10	V	$I_D = 1$ nA, $V_{DS} = -15$ V
BV_{GSS}	Gate-Source Breakdown Voltage	35		35		V	$I_G = 1\ \mu$A, $V_{DS} = 0$
I_{GSS}	Gate Leakage Current		200		200	pA	$V_{GS} = 20$ V, $V_{DS} = 0$
g_{fs}	Transconductance	-8		-8		mmho	$V_{GS} = 0, V_{DS} = -15$ V
g_{os}	Output Conductance		−1		−1	mmho	$V_{GS} = 0, V_{DS} = -15$ V
$I_{D(off)}$	Drain (OFF) Leakage		-100		-100	pA	$V_{DS} = 10$ V, $V_{GS} = -15$ V
$r_{DS(on)}$	Drain-Source "ON" Resistance		75		60	Ω	$V_{GS} = 0, V_{DS} = -0.1$ V
C_{iss}	Input Capacity		35		35	pF	$V_{DG} = -20$ V, $V_{GS} = 0$
C_{rss}	Reverse Transfer Capacity		12		12	pF	$V_{DG} = -10$ V, $I_S = 0$

INTERSIL

J105-J107
N-Channel JFET

FEATURES

- Low $r_{DS(on)}$ (3Ω MAX J105)

APPLICATIONS

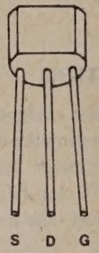
Analog Switches, Choppers, Commutators

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . −25V
Gate Current 50mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27mW/°C) 360mW
Operating Temperature Range . . . . . . −55 to 135°C
Storage Temperature Range . . . . −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

PIN CONFIGURATION

TO-92



ORDERING INFORMATION

J105	TO-92 only
J106	TO-92 only
J107	TO-92 only

ELECTRICAL CHARACTERISTICS
TEST CONDITIONS: 25°C unless otherwise noted

	PARAMETER		J105			J106			J107			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
STATIC	I_{GSS}	Gate-Reverse Current (Note 1)			−3			−3			−3	nA	$V_{DS}=0V$, $V_{GS}=-15V$	
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4.5		−10	−2		−6	−0.5		−4.5	V	$V_{DS}=5V$, $I_D=1\ \mu A$	
	BV_{GSS}	Gate-Source Breakdown Voltage	−25			−25			−25				$V_{DS}=0V$, $I_G=-1\ \mu A$	
	I_{DSS}	Drain Saturation Current (Note 2)	500			200			100			mA	$V_{DS}=15V$, $V_{GS}=0V$	
	$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	$V_{DS}=5V$, $V_{GS}=-10V$	
	$r_{DS(on)}$	Drain source ON Resistance			3			6			8	Ω	$V_{DS}\leq 0.1V$, $V_{GS}=0V$	
DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			35			35			35	pF	$V_{DS}=0V$, $V_{GS}=-10V$	f = 1 MHz
	$C_{sg(off)}$	Source Gate OFF Capacitance			35			35			35			
	$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance			160			160			160		$V_{DS}=V_{GS}=0V$	
	$t_{d(on)}$	Turn On Delay Time		15			15			15		ns	Switching Time Test Conditions J105 J106 J107 V_{DD} 1.5V 1.5V 1.5V $V_{GS(off)}$ −12V −7V −5V R_L 50Ω 50Ω 50Ω	
	t_r	Rise Time		20			20			20				
	$t_{d(off)}$	Turn Off Delay Time		15			15			15				
	t_f	Fall Time		20			20			20				

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

INTERSIL

J111-J113
N-Channel JFET

APPLICATIONS

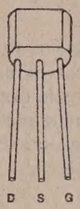
- **Analog Switches**
- **Choppers**
- **Commutators**

FEATURES

- **Low Cost**
- **Automated Insertion Package**
- **Low Insertion Loss**
  - **$r_{DS(on)} < 30\Omega$ (J111)**
- **No Offset or Error Voltage Generated by Closed Switch**
  - **Purely Resistive**
  - **High Isolation Resistance from Driver**
- **Fast Switching**
  - **$t_{D(on)} + t_r = 13$ ns Typical**
- **Short Sample and Hold Aperture Time**
  - **$C_{gd(off)} < 5$ pF**
  - **$C_{gs(off)} < 5$ pF**

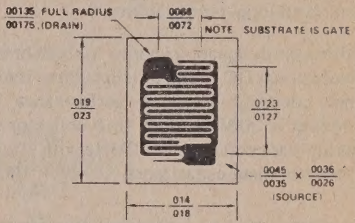
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5001B



ORDERING INFORMATION

TO-92	WAFER	DICE
J111	J111/W	J111/D
J112	J112/W	J112/D
J113	J113/W	J113/D

ABSOLUTE MAXIMUM RATINGS (@ 25° C)

Gate-Drain or Gate-Source Voltage	−35V
Gate Current	50 mA
Total Device Dissipation ($T_{LEAD} = 25°C$)	625 mW
Power Derating (to +135° C)	5.68 mW/° C
Storage Temperature Range	−55° C to +135° C
Operating Temperature Range	−55° C to +135° C
Lead Temperature (1/16'' from case for 10 seconds)	+300° C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25° C unless otherwise noted

		PARAMETERS		J111 MIN	J111 TYP	J111 MAX	J112 MIN	J112 TYP	J112 MAX	J113 MIN	J113 TYP	J113 MAX	UNIT	TEST CONDITIONS
1	S	I_{GSS}	Gate Reverse Current (Note 1)			1			1			1	nA	$V_{DS} = 0V$, $V_{GS} = -15V$
2	T	$V_{GS(off)}$	Gate Source Cutoff Voltage	3		10	1		5	0.5		3	V	$V_{DS} = 5V$, $I_D = 1\mu A$
3	A	BV_{GSS}	Gate Source Breakdown Voltage	35			35			35				$V_{DS} = 0V$, $I_G = -1\mu A$
4	T	I_{DSS}	Drain Saturation Current (Note 2)	20			5			2			mA	$V_{DS} = 15V$, $V_{GS} = 0V$
5	I	$I_{D(off)}$	Drain Cutoff Current (Note 1)			1			1			1	nA	$V_{DS} = 5V$, $V_{GS} = -10V$
6	C	$r_{DS(on)}$	Drain Source ON Resistance			30			50			100	Ω	$V_{DS} = 0.1V$, $V_{GS} = 0V$
7	D	$C_{dg(off)}$	Drain Gate OFF Capacitance			5			5			5	pF	$V_{DS} = 0V$, $V_{GS} = -10V$, f = 1 MHz
8	Y	$C_{sg(off)}$	Source Gate OFF Capacitance			5			5			5		
9	N	$C_{dg(on)}$	Drain Gate Plus Source Gate			28			28			28		$V_{DS} = V_{GS} = 0$, f = 1 MHz
	A	$+C_{sg(on)}$	ON Capacitance											
10	M	$t_{d(on)}$	Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions
11	I	t_r	Rise Time		6			6			6			J111 J112 J113
12	C	$t_{d(off)}$	Turn Off Delay Time		20			20			20			V_{DD} 10V 10V 10V
13		t_f	Fall Time		15			15			15			$V_{GS(off)}$ −12V −7V −5V R_L 800Ω 1,600Ω 3,200Ω

NOTES:

1. Approximately doubles for every 10° C increase in T_A.
2. Pulse Test duration 300μs; duty cycle ≤ 3%.

LM114/H, LM114A/AH
Dual NPN Monolithic Transistor

GENERAL DESCRIPTION

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of "popcorn noise," low leakages and improved long-term stability.

Although designed primarily for high breakdown voltage and exceptional DC characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 300MHz with 1mA collector current and 5V collector-base voltage and 22MHz with 10μA collector current. Collector-base capacitance is only ≈ 100pF at 5V.

ABSOLUTE MAXIMUM RATINGS

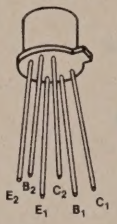
Collector-Base Voltage (BV_{CBO})	45V
Collector-Emitter Voltage (BV_{CER})	45V
Collector-Collector Voltage	45V
Emitter-Base Voltage (BV_{EBO})	6V
Collector Current	20mA
Total Power Dissipation (Note 1)	0.8W
Operating Junction Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	+300°C

FEATURES

- Low offset voltage — 0.5mV maximum
- Low drift — 2μV/°C maximum from −55°C to +125°C
- High current gain — 500 minimum at 10μA
- Tight beta match — 10% maximum
- High breakdown voltage — to 60V
- Matching guaranteed over a 0V to 45V collector-base voltage range
- CMRR > 100dB

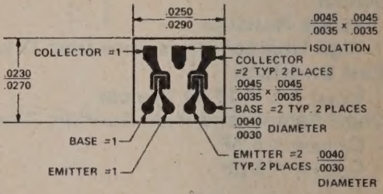
PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

4003


.0250/.0290
.0230/.0270
.0045/.0035 x .0045/.0035
ISOLATION
COLLECTOR #1
COLLECTOR #2 TYP. 2 PLACES
.0045/.0035 x .0045/.0035
BASE #2 TYP. 2 PLACES
.0040/.0030 DIAMETER
BASE #1
EMITTER #1
EMITTER #2 TYP. 2 PLACES .0040/.0030 DIAMETER

ORDERING INFORMATION

TO-71	TO-78	WAFER	DICE
LM114	LM114H	LM114/W	LM114/D
LM114A	LM114AH		

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	MAXIMUM LIMITS		UNITS
		LM114A, AH	LM114, H	
Offset Voltage	$1\mu A \le I_C \le 100\mu A$	0.5	2.0	mV
Offset Current	$I_C = 10\mu A$	2.0	10	nA
	$I_C = 1\mu A$	0.5		nA
Bias Current	$I_C = 10\mu A$	20	40	nA
	$I_C = 1\mu A$	3.0		nA
Offset Voltage Change	$0V \le V_{CB} \le V_{MAX}, I_C = 10\mu A$	0.2	1.5	mV
Offset Current Change	$0V \le V_{CB} \le V_{MAX}, I_C = 10\mu A$	1.0	4.0	nA
Offset Voltage Drift	$-55°C \le T_A \le +125°C$, $I_C = 10\mu A$	2.0	10	μV/°C
Offset Current	$-55°C \le T_A \le +125°$, $I_C = 10\mu A$	12	50	nA
Bias Current	$-55°C \le T_A \le +125°C$, $I_C = 10\mu A$	60	150	nA
Collector-Base Leakage Current	$V_{CB} = V_{MAX}$			
	$T_A = +25°C$	10	50	pA
	$T_A = +125°C$	10	50	nA
Collector-Emitter Leakage Current	$V_{CE} = V_{MAX}, V_{EB} = 0V$			
	$T_A = +25°C$	50	200	pA
	$T_A = +125°C$	50	200	nA
Collector-Collector Leakage Current	$V_{CC} = V_{MAX}$			
	$T_A = +25°C$	100	300	pA
	$T_A = +125°C$	100	300	nA

Note 1: The maximum dissipation given is for a +25°C case temperature. For operation under other conditions, the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +70°C/W junction to case of +230°C/W junction to ambient.

Note 2: These specifications apply for $T_A = +25°C$ and $0V \le V_{CB} \le V_{MAX}$, unless otherwise specified. For the LM114 and LM114A, V_{MAX} = 30V.

INTERSIL

M116
Diode Protected N-Channel Enhancement Mode MOS FET

GENERAL DESCRIPTION

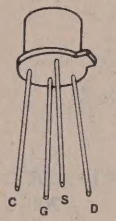
- Low I_{GSS}
- Integrated Zener Clamp Protects the Gate

ABSOLUTE MAXIMUM RATINGS (25°C)

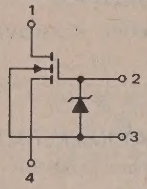
Drain-to-Source Voltage	30 V
Gate-to-Drain Voltage.	30V
Drain Current	50 mA
Gate Zener Current	±0.1 mA
Storage Temperature	−65 to 150°C
Operating Junction Temperature	−55 to 125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW

PIN CONFIGURATION

TO-72

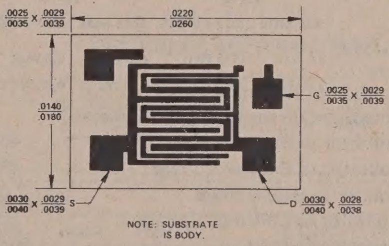


DEVICE SCHEMATIC



CHIP TOPOGRAPHY

1003-Z


.0025/.0035 x .0029/.0039
.0220/.0260
.0140/.0180
G .0025/.0035 x .0029/.0039
.0030/.0040 x .0029/.0039 S
D .0030/.0040 x .0028/.0038
NOTE: SUBSTRATE IS BODY.

ORDERING INFORMATION

TO-72	WAFER	DICE
M116	M116/W	M116/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	M116 MIN	M116 MAX	UNITS	TEST CONDITIONS
$r_{DS(on)}$	Drain Source ON Resistance		100 200	Ω	$V_{GS} = 20$ V, $I_D = 100\ \mu A$, $V_{BS} = 0$ $V_{GS} = 10$ V, $I_D = 100\ \mu A$, $V_{BS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	1	5	V	$V_{GS} = V_{DS}$, $I_D = 10\ \mu A$, $V_{BS} = 0$
BV_{DSS}	Drain-Source Breakdown Voltage	30		V	$I_D = 1\ \mu A$, $V_{GS} = V_{BS} = 0$
BV_{SDS}	Source-Drain Breakdown Voltage	30		V	$I_S = 1\ \mu A$, $V_{GD} = V_{BD} = 0$
BV_{GBS}	Gate-Body Breakdown Voltage	30	60	V	$I_G = 10\ \mu A$, $V_{SB} = V_{DB} = 0$
$I_{D(OFF)}$	Drain Cutoff Current		10	nA	$V_{DS} = 20$ V, $V_{GS} = V_{BS} = 0$
$I_{S(OFF)}$	Source Cutoff Current		10	nA	$V_{SD} = 20$ V, $V_{GD} = V_{BD} = 0$
I_{GSS}	Gate-Body Leakage		100	pA	$V_{GS} = 20$ V, $V_{DS} = V_{BS} = 0$
C_{gs} or C_{gd}	Gate-Source or Gate-Drain Capacitance		2.5	pF	$V_{GB} = V_{DB} = V_{SB} = 0$, f = 1 MHz Body Guarded
C_{db}	Drain-Body Capacitance		7	pF	$V_{GB} = 0$, $V_{DB} = 10$ V, f = 1 MHz
C_{iss}	Input Capacitance		10	pF	$V_{GB} = 0$, $V_{DB} = 10$ V, $V_{BS} = 0$ f = 1 MHz

INTERSIL

IT120-IT122
Dual Monolithic NPN Transistor

FEATURES

- High h_{FE} at Low Current > 200 @ 10 μA
- Low Output Capacitance < 2.0 pf
- $I_{B_1} - I_{B_2}$ < 2.5 nA
- Tight V_{BE} Tracking $< 3.0\ \mu V/°C$

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

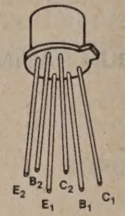
	TO-78		TO-71	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.4 Watt	0.75 Watt	0.3 Watt	0.5 Watt
Derating Factor	2.3mW/°C	4.3mW/°C	1.7mW/°C	4.3mW/°C

Maximum Voltage & Current for Each Transistor

V_{CBO}	Collector to Base Voltage	45 V
V_{CEO}	Collector to Emitter Voltage	45 V
V_{EBO}	Emitter to Base Voltage	7.0 V
V_{CCO}	Collector to Collector Voltage	60 V
I_C	Collector Current	50mA

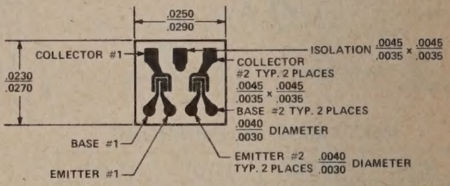
PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

4003


.0250
.0290
COLLECTOR #1
.0230
.0270
ISOLATION .0045/.0035 x .0045/.0035
COLLECTOR #2 TYP. 2 PLACES
.0045/.0035 x .0045/.0035
BASE #2 TYP. 2 PLACES
.0040/.0030 DIAMETER
BASE #1
EMITTER #1
EMITTER #2 TYP. 2 PLACES .0040/.0030 DIAMETER

ORDERING INFORMATION

TO-78	TO-71	WAFER	DICE
IT120	IT120-TO71	IT120/W	IT120/D
IT121	IT121-TO71	IT121/W	IT121/D
IT122	IT122-TO71	IT122/W	IT122/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		IT120A		IT120		IT121		IT122		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200		200		80		80			$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
h_{FE}	DC Current Gain	225		225		100		100			$I_C = 1.0$ mA, $V_{CE} = 5.0$ V
h_{FE}(−55°C)	DC Current Gain	75		75		30		30			$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
V_{BE}(ON)	Emitter-Base On Voltage		0.7		0.7		0.7		0.7	V	$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
V_{CE}(SAT)	Collector Saturation Voltage		0.5		0.5		0.5		0.5	V	$I_C = 0.5$ mA, $I_B = 0.05$ mA
I_{CBO}	Collector Cutoff Current		1.0		1.0		1.0		1.0	nA	$I_E = 0$, $V_{CB} = 45$ V
I_{CBO}(+150°C)	Collector Cutoff Current		10		10		10		10	μA	$I_E = 0$, $V_{CB} = 45$ V
I_{EBO}	Emitter Cutoff Current		1.0		1.0		1.0		1.0	nA	$I_C = 0$, $V_{EB} = 5.0$ V
C_{OB}	Output Capacitance		2.0		2.0		2.0		2.0	pF	$I_E = 0$, $V_{CB} = 5.0$ V
C_{TE}	Emitter Transition Capacitance		2.5		2.5		2.5		2.5	pF	$I_C = 0$, $V_{EB} = 0.5$ V
C_{C_1, C_2}	Collector to Collector Capacitance		4.0		4.0		4.0		4.0	pF	$V_{CC} = 0$
I_{C_1, C_2}	Collector to Collector Leakage Current		10		10		10		10	nA	$V_{CC} = \pm 60$ V
V_{CEO}(SUST)	Collector to Emitter Sustaining Voltage	45		45		45		45		V	$I_C = 1.0$ mA, $I_B = 0$
GBW	Current Gain Bandwidth Product	10 220		10 220		7 180		7 180		MHz MHz	$I_C = 10\ \mu A$, $V_{CE} = 5$ V $I_C = 1$ mA, $V_{CE} = 5$ V
$\lvert V_{BE_1} - V_{BE_2}\rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
$\lvert I_{B_1} - I_{B_2}\rvert$	Base Current Differential		2.5		5		25		25	nA	$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
$\lvert\Delta(V_{BE_1} - V_{BE_2})\rvert$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	μV/°C	$T_A = -55°C$ to $+125°C$ $I_C = 10\ \mu A$, $V_{CE} = 5.0$ V

NOTES: (1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
(2) The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

IT124
Super-Beta Dual Monolithic NPN Transistor

FEATURES

- **Very High Gain — $h_{FE} \geq 1500$ @ 1 and 10μA**
- **Low Output Capacitance — $C_{obo} \leq 0.8$ pF**
- **Tight V_{BE} Matching — $|V_{BE1} - V_{BE2}|$ — 2 mV TYP.**
- **High f_T — 100 MHz**

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

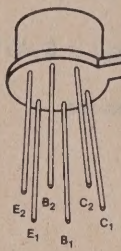
Maximum Temperatures
Storage Temperature .... −65°C to +200°C
Operating Junction Temperature .... +200°C
Lead Temperature (soldering, 10 second time limit) .... +260°C

Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation @ Free Air	400 mW	750 mW
Linear Derating Factor	2.3 mW/°C	4.3 mW/°C

Maximum Voltage and Current for Each Transistor
V_{CBO} Collector to Base Voltage 2V
V_{CEO} Collector to Emitter Voltage 2V
V_{EBO} Emitter to Base Voltage (Note 2) 7V
V_{CCO} Collector to Collector Voltage 100V
I_C Collector Current 10mA

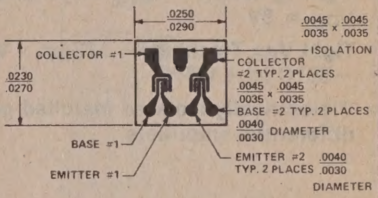
PIN CONFIGURATION

TO-78



CHIP TOPOGRAPHY

4003



ORDERING INFORMATION

TO-78	WAFER	DICE
IT124	IT124/W	IT124/D

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
h_{FE}	DC Current Gain	1500			$I_C = 1\mu A$, $V_{CE} = 1V$
h_{FE}	DC Current Gain	1500			$I_C = 10\mu A$, $V_{CE} = 1V$
$h_{FE}(-55°C)$	DC Current Gain	600			$I_C = 10\mu A$, $V_{CE} = 1V$
$V_{BE}(ON)$	Emitter-Base "ON" Voltage		0.7	V	$I_C = 10\mu A$, $V_{CE} = 1V$
$V_{CE}(SAT)$	Collector Saturation Voltage		0.5	V	$I_C = 1mA$, $I_B = 0.1mA$
I_{CBO}	Collector Cutoff Current		100	pA	$I_E = 0$, $V_{CB} = 1V$
$I_{CBO}(+150°C)$	Collector Cutoff Current		100	nA	$I_E = 0$, $V_{CB} = 1V$
I_{EBO}	Emitter Cutoff Current		100	pA	$I_C = 0$, $V_{EB} = 5V$
C_{OBO}	Output Capacitance		0.8	pF	$I_E = 0$, $V_{CB} = 1V$
C_{TE}	Emitter Transition Capacitance		1.0	pF	$I_C = 0$, $V_{EB} = 0.5V$
C_{C1C2}	Collector to Collector Capacitance		0.8	pF	$V_{CC} = 0$
I_{C1C2}	Collector to Collector Leakage Current		250	pA	$V_{CC} = \pm 50V$
f_T	Current Gain Bandwidth Product	10		MHz	$I_C = 10\mu A$, $V_{CE} = 1V$
f_T	Current Gain Bandwidth Product	100		MHz	$I_C = 100\mu A$, $V_{CE} = 1V$
NF	Narrow Band Noise Figure		3	dB	$I_C = 10\mu A$, $V_{CE} = 3V$, f = 1 KHz, R_G = 10 Kohms, BW = 200 Hz
BV_{CBO}	Collector-Base Breakdown Voltage	2		V	$I_C = 10\mu A$, $I_E = 0$
BV_{EBO}	Emitter-Base Breakdown Voltage	7		V	$I_E = 10\mu A$, $I_C = 0$
$V_{CEO}(SUST)$	Collector-Emitter Sustaining Voltage	2		V	$I_C = 1mA$, $I_B = 0$

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	2	5	mV	$I_C = 10\mu A$, $V_{CE} = 1V$
$\lvert(V_{BE1}-V_{BE2})\rvert/°C$	Base Emitter Voltage Differential Change with Temperature	5	15	μV/°C	$I_C = 10\mu A$, $V_{CE} = 1V$ T = −55°C to +125°C
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential		.6	nA	$T_C = 10\mu A$, $V_{CE} = 1V$

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μAmps.

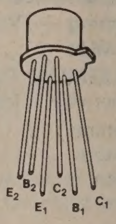
IT126-IT129
Dual Monolithic NPN Transistor

FEATURES

- **High Gain at Low Current — $h_{FE} \geq 230$ at 10 mA, $V_{CE} = 5V$**
- **Low Output Capacitance — $C_{obo} \leq 3$ pF**
- **Tight I_B Match — $I_{B1\text{-}2} < .25\ \mu A$ at 1 mA, $V_{CE} = 5V$**
- **Tight V_{BE} Tracking — $\Delta(V_{BE_1} - V_{BE_2}) \leq 3\ \mu V/°C$ $-55°C$ to $+125°C$**
- **Dielectrically isolated matched pairs for differential amplifiers**

PIN CONFIGURATION

TO-71
TO-78



ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

	TO71		TO78	
Maximum Power Dissipation	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7 mW/°C	2.9 mW/°C	2.3 mW/°C	4.3 mW/°C

Maximum Voltage and Current for Each Transistor		IT126,7	IT128	IT129
V_{CBO}	Collector to Base Voltage	60V	55V	45V
V_{CEO}	Collector to Emitter Voltage	60V	55V	45V
V_{EBO}	Emitter to Base Voltage (Note 2)	7V	7V	7V
V_{CCO}	Collector to Collector Voltage	70V	70V	70V
I_C	Collector Current	100 mA	100 mA	100 mA

CHIP TOPOGRAPHY

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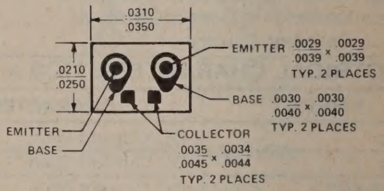


ORDERING INFORMATION

TO78	TO-71	WAFER	DICE
IT126	IT126-TO71	IT126/W	IT126/D
IT127	IT127-TO71	IT127/W	IT127/D
IT128	IT128-TO71	IT128/W	IT128/D
IT129	IT129-TO71	IT128/W	IT128/D

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		IT126		IT127		IT128		IT129		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	150		150		100		70			$I_C = 10\ \mu A$, $V_{CE} = 5V$
h_{FE}	DC Current Gain	200	800	200	800	150	800	100			$I_C = 1.0$ mA, $V_{CE} = 5V$
h_{FE}	DC Current Gain	230		230		170		115			$I_C = 10$ mA, $V_{CE} = 5V$
h_{FE}	DC Current Gain	100		100		75		50			$I_C = 50$ mA, $V_{CE} = 5V$
$h_{FE}(-55°C)$	DC Current Gain	75		75		60		40			$I_C = 1$ mA, $V_{CE} = 5V$
$V_{BE(on)}$	Emitter-Base On Voltage		.9		.9		.9		.9	V	$I_C = 10$ mA, $V_{CE} = 5V$
			1.0		1.0		1.0		1.0	V	$I_C = 50$ mA, $V_{CE} = 5V$
$V_{CE(sat)}$	Collector Saturation Voltage		.3		.3		.3		.3	V	$I_C = 10$ mA, $I_B = 1$ mA
			1.0		1.0		1.0		1.0	V	$I_C = 50$ mA, $I_B = 5$ mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1		0.1	nA	$I_E = 0$, $V_{CB} = 45V, 30V$
$I_{CBO}(+150°C)$	Collector Cutoff Current		0.1		0.1		0.1		0.1	µA	$I_E = 0$, $V_{CB} = 45V, 30V$
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1		0.1	nA	$I_C = 0$, $V_{EB} = 5V$
C_{obo}	Output Capacitance		3		3		3		3	pF	$I_E = 0$, $V_{CB} = 20V$

INTERSIL

IT130-IT132
Dual Monolithic PNP Transistor

FEATURES

- **High h_{FE} at Low Current > 200 @ 10 μA**
- **Low Output Capacitance < 2.0 pF**
- **I_{B1}-I_{B2} < 2.5 nA**
- **Tight V_{BE} Tracking < 3.0 μV/°C**

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

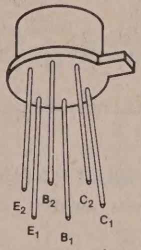
	TO-78		TO-71	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.4 Watt	0.75 Watt	0.3 Watt	0.5 Watt
Derating Factor	2.3mW/°C	4.3mW/°C	1.7mW/°C	2.9mW/°C

Maximum Voltage & Current for Each Transistor

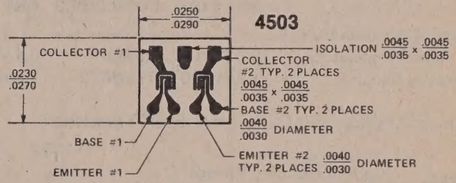
V_{CBO}	Collector to Base Voltage	45 V
V_{CEO}	Collector to Emitter Voltage	45 V
V_{EBO}	Emitter to Base Voltage	7.0 V
V_{CCO}	Collector to Collector Voltage	60 V
I_C	Collector Current	50 mA

PIN CONFIGURATIONS

TO-71
TO-78



CHIP TOPOGRAPHY


.0250
.0290
4503
COLLECTOR #1
ISOLATION .0045/.0035 x .0045/.0035
.0230
.0270
COLLECTOR #2 TYP. 2 PLACES
.0045/.0035 x .0045/.0035
BASE #2 TYP. 2 PLACES
.0040/.0030 DIAMETER
BASE #1
EMITTER #1
EMITTER #2 TYP. 2 PLACES .0040/.0030 DIAMETER

ORDERING INFORMATION

TO-79	TO-71	WAFER	DICE
IT130A	IT130A-TO71	IT130A/W	IT130A/D
IT130	IT130-TO71	IT130/W	IT130/D
IT131	IT131-TO71	IT131/W	IT131/D
IT132	IT132-TO71	IT132/W	IT132/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		IT130A		IT130		IT131		IT132		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200		200		80		80			$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$
h_{FE}	DC Current Gain	225		225		100		100			$I_C = 1.0\ mA$, $V_{CE} = 5.0\ V$
$h_{FE}(-55°C)$	DC Current Gain	75		75		30		30			$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$
$V_{BE}(ON)$	Emitter-Base On Voltage		0.7		0.7		0.7		0.7	V	$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$
$V_{CE}(SAT)$	Collector Saturation Voltage		0.5		0.5		0.5		0.5	V	$I_C = 0.5\ mA$, $I_B = 0.05\ mA$
I_{CBO}	Collector Cutoff Current		−1.0		−1.0		−1.0		−1.0	nA	$I_E = 0$, $V_{CB} = 45\ V$
$I_{CBO}(+150°C)$	Collector Cutoff Current		−10		−10		−10		−10	μA	$I_E = 0$, $V_{CB} = 45\ V$
I_{EBO}	Emitter Cutoff Current		−1.0		−1.0		−1.0		−1.0	nA	$I_C = 0$, $V_{EB} = 5.0\ V$
C_{ob}	Output Capacitance		2.0		2.0		2.0		2.0	pF	$I_E = 0$, $V_{CB} = 5.0\ V$
C_{te}	Emitter Transition Capacitance		2.5		2.5		2.5		2.5	pF	$I_C = 0$, $V_{EB} = 0.5\ V$
$C_{C_1-C_2}$	Collector to Collector Capacitance		4.0		4.0		4.0		4.0	pF	$V_{CC} = 0$
$I_{C_1-C_2}$	Collector to Collector Leakage Current		10		10		10		10	nA	$V_{CC} = \pm 60\ V$
$V_{CEO}(SUST)$	Collector to Emitter Sustaining Voltage	−45		−45		−45		−45		V	$I_C = 1.0\ mA$, $I_B = 0$
GBW	Current Gain Bandwidth Product	5		5		4		4		MHz	$I_C = 10\ \mu A$, $V_{CE} = 5\ V$
		110		110		90		90		MHz	$I_C = 1\ mA$, $V_{CE} = 5\ V$
$\|V_{BE_1}-V_{BE_2}\|$	Base Emitter Voltage Differential		1		2		3		5	mV	$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$
$\|I_{B_1}-I_{B_2}\|$	Base Current Differential		2.5		5		25		25	nA	$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$
$\|\Delta(V_{BE_1}-V_{BE_2})\|$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	μV/°C	$T_A = -55°C$ to $+125°C$ $I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$

NOTES: (1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
(2) The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

INTERSIL

IT136-IT139
Dual Monolithic PNP Transistor

FEATURES

- High Gain at Low Current — $h_{FE} \geq 200$ @ 1mA
- Low Output Capacitance — $C_{obo} < 3$ pF
- Tight I_B Match — $I_{B_{1-2}} < .25\ \mu A$ @ 1 mA – 5V
- Tight V_{BE} Tracking — $\Delta(V_{BE_1} - V_{BE_2}) \leq 3\ \mu V/^\circ C$ $-55^\circ C$ to $+125^\circ C$
- Dielectrically isolated matched pairs for differential amplifiers.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

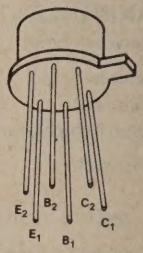
	TO71		TO78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation @ 25°C Case Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7mW/°C	2.9mW/°C	2.3mW/°C	4.3mW/°C

Maximum Voltage and Current for Each Transistor

		IT136,7	IT138	IT139
V_{CBO}	Collector to Base Voltage	60V	55V	45V
V_{CEO}	Collector to Emitter Voltage	60V	55V	45V
V_{EBO}	Emitter to Base Voltage	7V	7V	7V
V_{CCO}	Collector to Collector Voltage	70V	70V	70V
I_C	Collector Current	100mA	100mA	100mA

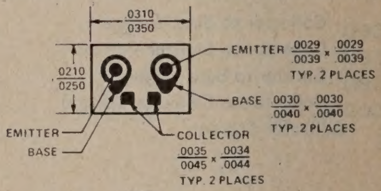
PIN CONFIGURATION

TO-71
TO-78



E2
B2
C2
C1
E1
B1

CHIP TOPOGRAPHY



.0310 / .0350
.0210 / .0250
EMITTER .0029/.0039 × .0029/.0039 TYP. 2 PLACES
BASE .0030/.0040 × .0030/.0040 TYP. 2 PLACES
EMITTER
BASE
COLLECTOR .0035/.0045 × .0034/.0044 TYP. 2 PLACES

4501

ORDERING INFORMATION

TO-78	TO-71	WAFER	DICE
IT136	IT136-TO71	IT136/W	IT136/D
IT137	IT137-TO71	IT137/W	IT137/D
IT138	IT138-TO71	IT138/W	IT138/D
IT139	IT139-TO71	IT139/W	IT139/D

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	150		150		100		70			I_C = 10 µA, V_{CE} = 5V
h_{FE}	DC Current Gain	150	800	150	800	100	800	70	800		I_C = 1.0 mA, V_{CE} = 5V
h_{FE}	DC Current Gain	125	230	125		80		50			I_C = 10 mA, V_{CE} = 5V
h_{FE}	DC Current Gain	65		60		40		25			I_C = 50 mA, V_{CE} = 5V
h_{FE}(-55°C)	DC Current Gain	75		75		60		40			I_C = 1 mA, V_{CE} = 5V
$V_{BE(on)}$	Emitter - Base On Voltage		.9		.9		.9		.9	V	I_C = 10 mA, V_{CE} = 5V
			1.0		1.0		1.0		1.0	V	I_C = 50 mA, V_{CE} = 5V
$V_{CE(sat)}$	Collector Saturation Voltage		.3		.3		.3		.3	V	I_C = 1 mA, I_B = .1 mA
			.6		.6		.6		.6	V	I_C = 10 mA, I_B = 1 mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1		0.1	nA	I_E = 0, V_{CB} = 45V, 30V
I_{CBO}(+150°C)	Collector Cutoff Current		0.1		0.1		0.1		0.1	µA	I_E = 0, V_{CB} = 45V, 30V
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1		0.1	nA	I_C = 0, V_{EB} = 5V
C_{obo}	Output Capacitance		3		3		3		3	pF	I_E = 0, V_{CB} = 20V

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$BV_{C_1C_2}$	Collector to Collector Breakdown Voltage	100		100		100		100		V	I_C = ±1 µA
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		60		55		45		V	I_C = 1 mA, I_B = 0
BV_{CBO}	Collector Base Breakdown Voltage	60		60		55		45		V	I_C = 10 µA, I_E = 0
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		7		V	I_E = 10 µA, I_C = 0

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	I_C = 1 ma , V_{CE} = 5V
$\lvert \Delta(V_{BE_1} - V_{BE_2}) \rvert$/°C	Base Emitter Voltage Differential Change with Temperature		3		5		10		20	µV/°C	I_C = 1 mA, V_{CE} = 5V T_A = -55°C to +125°C
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential		2.5		5		10		20	nA	I_C = 10 µA, V_{CE} = 5V
			.25		.5		1.0		2.0	µA	I_C = 1 mA, V_{CE} = 5V

INTERSIL

IT140
Dual Matched NPN Transistor

FEATURES

- **Excellent Conformance**
- **Tight V_{BE} Match $<$ 1.0mV**
- **Tight V_{BE} Tracking $<$ 3.0 μV/°C**

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Maximum Power Dissipation	

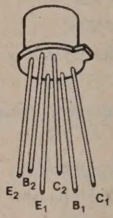
	TO-71 ONE SIDE	TO-71 BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.3 Watt	0.5 Watt
Derating Factor	1.7mW/°C	4.3mW/°C

Maximum Voltage & Current for Each Transistor

V_{CBO}	Collector to Base Voltage	20 V
V_{CEO}	Collector to Emitter Voltage	20 V
V_{EBO}	Emitter to Base Voltage	7.0 V
V_{CCO}	Collector to Collector Voltage	45 V
I_C	Collector Current	50mA

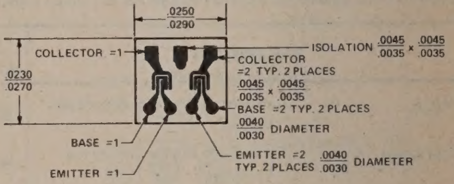
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

4003S



ORDERING INFORMATION

TO-71	WAFER	DICE
IT140	IT140/W	IT140/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	200			$I_C = 10mA, V_{CE} = 5V$
h_{FE}	DC Current Gain	100			$I_C = 10\mu A, V_{CE} = 5.0V$
h_{FE}	DC Current Gain	250			$I_C = 1.0mA, V_{CE} = 5.0V$
$h_{FE}(-55°C)$	DC Current Gain	30			$I_C = 10\mu A, V_{CE} = 5.0V$
$V_{BE}(ON)$	Emitter-Base On Voltage		0.7	V	$I_C = 10\mu A, V_{CE} = 5.0V$
$V_{CE}(SAT)$	Collector Saturation Voltage		0.3	V	$I_C = 0.5mA, I_B = 0.05mA$
I_{CBO}	Collector Cutoff Current		200	nA	$I_E = 0, V_{CB} = 45V$
$I_{CBO}(+150°C)$	Collector Cutoff Current		1.0	μA	$I_E = 0, V_{CB} = 45V$
I_{EBO}	Emitter Cutoff Current		400	nA	$I_C = 0, V_{EB} = 5.0V$
C_{OB}	Output Capacitance		2.0	pF	$I_E = 0, V_{CB} = 5.0V$
C_{TE}	Emitter Transition Capacitance		2.5	pF	$I_C = 0, V_{EB} = 0.5V$
C_{C_1, C_2}	Collector to Collector Capacitance		4.0	pF	$V_{CC} = 0$
I_{C_1, C_2}	Collector to Collector Leakage Current		10	nA	$V_{CC} = \pm 60V$
$V_{CEO}(SUST)$	Collector to Emitter Sustaining Voltage	20		V	$I_C = 1.0mA, I_B = 0$
	Current Gain			MHz	$I_C = 10\mu A, V_{CE} = 5V$
f_T	Bandwidth Product	400		MHz	$I_C = 1mA, V_{CE} = 5V$
V_{BE_1}-V_{BE_2}	Base Emitter Voltage Differential		1	mV	$I_C = 10\mu A, V_{CE} = 5.0V$
I_{B_1}-I_{B_2}	Base Current Differential		2.5	nA	$I_C = 10\mu A, V_{CE} = 5.0V$
$\Delta(V_{BE_1}$-$V_{B_2})$	Base-Emitter Voltage Differential Change with Temperature		3	μV/°C	$T_A = -55°C$ to $+125°C$ $I_C = 10\mu A, V_{CE} = 5.0V$
$\frac{h_{FE_1}-h_{FE_2}}{h_{FE_2}}$	Current Gain Match		5%		$I_C = 10\mu A, V_{CE} = 5V$
r_e	Emitter Resistance		1.5	Ω	$I_C = 100\mu A$ to $1mA, V_{CE} = 5V$

NOTES: (1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
(2) The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

INTERSIL

3N161
Diode Protected P-Channel Enhancement Mode MOS FET

GENERAL DESCRIPTION

DIODE-PROTECTED ENHANCEMENT-TYPE METAL-OXIDE-SEMICONDUCTOR TRANSISTOR

For applications requiring very high input impedance, such as series and shunt choppers, multiplexers, and commutators.

FEATURES

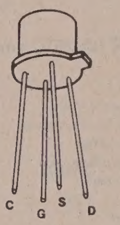
- Channel Cut Off with Zero Gate Voltage
- Square-Law Transfer Characteristic Reduces Distortion
- Independent Substrate Connection Provides Flexibility in Biasing
- Internally Connected Diode Protects Gate from Damage due to Overvoltage

DESCRIPTION

These devices are designed for applications requiring very high input impedance, such as choppers, commutators, and logic switches. Each device is protected from excessive input voltage by a shunting diode connected from the gate to the substrate. This eliminates the need for most precautionary handling procedures associated with unprotected MOS devices.

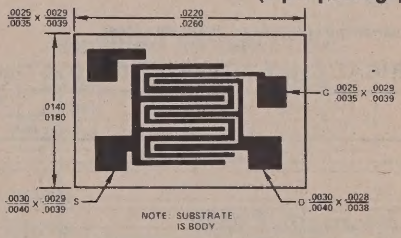
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

1503-Z
(2 per package)


.0025/.0035 x .0029/.0039
.0220/.0260
.0140/.0180
G .0025/.0035 x .0029/.0039
.0030/.0040 x .0029/.0039 S
D .0030/.0040 x .0028/.0038
NOTE: SUBSTRATE IS BODY

ORDERING INFORMATION

TO-72	WAFER	DICE
3N161	3N161/W	3N161/D

ELECTRICAL CHARACTERISTICS (25°C free-air temperature unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS	
I_{GSSF}	Forward Gate-Terminal Current			–0.1	nA	$V_{GS} = -25$ V, $V_{DS} = 0$	
				–1	nA	$V_{GS} = -25$ V, $V_{DS} = 0$,	$T_A = 100°C$
BV_{GSS}	Forward Gate-Source Breakdown Voltage	–25			V	I_G –0.1 mA, $V_{DS} = 0$,	
I_{DSS}	Zero-Gate-Voltage Drain Current			–10	nA	$V_{DS} = -15$ V, $V_{GS} = 0$	
				–10	µA	$V_{DS} = -25$ V, $V_{GS} = 0$	
$V_{GS(th)}$	Gate-Source Threshold Voltage	–1.5		–5	V	$V_{DS} = -15$ V, $I_D = 10\ \mu A$	
V_{GS}	Gate-Source Voltage	–4.5		–8	V	$V_{DS} = -15$ V, $I_D = -8$ mA	
$I_{D(on)}$	On-State Drain Current	–40		–120	mA	$V_{DS} = -15$ V, $V_{GS} = -15$ V	
$\lvert y_{fs} \rvert$	Small-Signal Common-Source Forward Transfer Admittance	3500		6500	µmho	$V_{DS} = -15$ V, $I_D = -8$ mA	f = 1 kHz
$\lvert y_{os} \rvert$	Small-Signal Common-Source Output Admittance			250	µmho		
C_{iss}	Common-Source Short-Circuit Input Capacitance			10	pF		f = 1 MHz
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance			4	pF		

3N163, 3N164
P-Channel Enhancement Mode MOS FET

FEATURES

- Very High Input Impedance
- High Gate Breakdown
- Fast Switching
- Low Capacitance

MAXIMUM RATINGS (@ 25°C ambient unless noted)

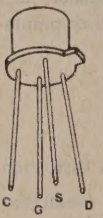
		3N163	3N164
V_{GSS}	Static Gate to Source Voltage	±40V	±30V
$V_{GSS}^{(1)}$	Transmit Gate to Source Voltage	±125V	±125V
V_{DSS}	Drain to Source Voltage	−40V	−30V
V_{SDS}	Source to Drain Voltage	−40V	−30V
V_{DGO}	Drain to Gate Voltage	−40V	−30V
I_D	Drain Current	−50 mA	−50 mA
P_D	Power Dissipation	375 mW	
	Derating Factor	3.0 mW/°C	
T_J	Operating Junction Temperature	−55 to +150°C	
T_{stg}	Storage Temperature	−65 to +200°C	
T_L	Lead Temperature 1/16" from Case for 10 sec max	+265°C	

(1) Devices must not be tested at ±125V more than once or for longer than 300 ms.

NOTE: See handling precautions on 3N170 data sheet.

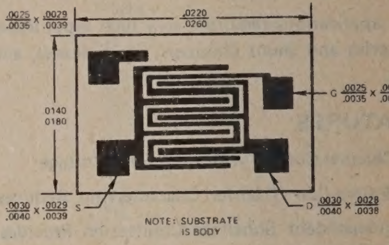
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

1503-Z


.0025/.0035 x .0029/.0039
.0220/.0260
0140/0180
G .0025/.0035 x .0029/.0039
.0030/.0040 x .0029/.0039 S
D .0030/.0040 x .0028/.0038
NOTE: SUBSTRATE IS BODY

ORDERING INFORMATION

TO-72	WAFER	DICE
3N163	3N163/W	3N163/D
3N164	3N164/W	3N164/D

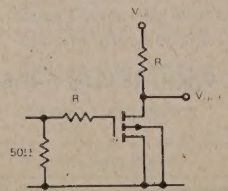
ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		3N163		3N164		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSS}	Gate Reverse Leakage Current		10①		10②	pA	① V_{GS} = 40V, ② V_{GS} = 30V
$I_{G(f)}$	Gate Forward Current		−10①		−10②	pA	① V_{GS} = −40V, ② V_{GS} = −30V
$I_{G(f)}$	Gate Forward Current @ 125°C		−25①		−25②	pA	① V_{GS} = −40V, ② V_{GS} = −30V
BV_{DSS}	Drain-Source Breakdown Voltage	−40		−30		V	$I_D = -10\,\mu A$, $V_{GS} = 0$
BV_{SDS}	Source Drain Breakdown Voltage	−40		−30		V	$I_S = -10\,\mu A$, $V_{GD} = 0$, $V_{DB} = 0$
$V_{GS(th)}$	Threshold Voltage	−2.0	−5.0	−2.0	−5.0	V	$V_{DS} = V_{GS}$, $I_D = -10\,\mu A$
$V_{GS(th)}$	Threshold Voltage	−2.0	−5.0	−2.0	−5.0	V	$V_{DS} = -15V$, $I_D = -10\,\mu A$
V_{GS}	Gate Source Voltage	−3.0	−6.5	−3.0	−6.5	V	$V_{DS} = -15V$, $I_D = 0.5$ mA
I_{DSS}	Zero Gate Voltage Drain Current		200		400	pA	$V_{DS} = -15V$, $V_{GS} = 0$
I_{SDS}	Source Drain Current		400		800	pA	$V_{SD} = 15V$, $V_{GS} = V_{DB} = 0$
$r_{ds(on)}$	Drain-Source on Resistance		250		300	ohms	$V_{GS} = -20V$, $I_D = -100\,\mu A$
$I_{D(on)}$	On Drain Current	−5.0	−30.0	−3.0	−30.0	mA	$V_{DS} = -15V$, $V_{GS} = -10V$
Y_{fs}	Forward Transconductance @ 1 kHz	2000	4000	1000	4000	μmhos	$V_{DS} = -15V$, $I_D = -10$ mA
Y_{OS}	Output Admittance @ 1 kHz		250		250	μmhos	$V_{DS} = -15V$, $I_D = -10$ mA
C_{iss}	Input Capacitance − Output Shorted		2.5		2.5	pF	$V_{DS} = -15V$, $I_D = -10$ mA, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		0.7		0.7	pF	$V_{DS} = -15V$, $I_D = -10$ mA, f = 1 MHz
C_{oss}	Output Capacitance Input Shorted		3.0		3.0	pF	$V_{DS} = -15V$, $I_D = -10$ mA, f = 1 MHz

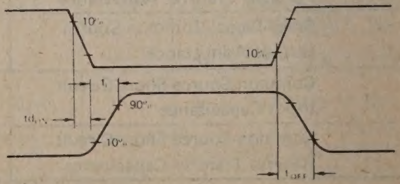
SWITCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0)

		3N163	3N164		
t_{on}	Turn-On Delay Time	12	12	ns	$V_{DD} = -15V$
t_r	Rise Time	24	24	ns	$I_{D(on)} = 10$ mA
t_{off}	Turn-Off Time	50	50	ns	$R_G = R_L = 1.4\ k\Omega$

SWITCHING TIME CIRCUIT



SWITCHING WAVEFORM



INTERSIL

3N165, 3N166
Dual P-Channel Enhancement Mode MOS FET

FEATURES

- Very High Input Impedance
- High Gate Breakdown
- Low Capacitance

MAXIMUM RATINGS (@ 25°C ambient unless noted)

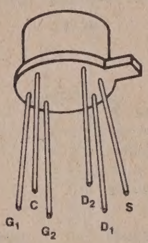
V_{GSS}	Static Gate to Source Voltage	±40V
V_{GSS}(1)	Transient Gate to Source Voltage	±125V
V_{DSS}	Drain to Source Voltage	−40V
V_{GDS}	Source to Drain Voltage	−40V
V_{GG}	Gate to Gate	±80V
V_G	Any Lead to Case	±40V
I_D	Drain Current	50 mA
P_D	Power Dissipation (each side)	300 mW
	(both sides)	525 mW
	Total Derating Factor	4.2 mW/°C
T_J	Operating Junction Temperature	−55 to +150°C
T_{stg}	Storage Temperature	−65 to +200°C
T_L	Lead Temperature 1/16″ from Case for 10 sec max	+300°C

(1) Devices must not be tested at ±125V more than once or for longer than 300 ms.

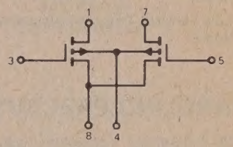
NOTE: See handling precautions on 3N170 data sheet.

PIN CONFIGURATION

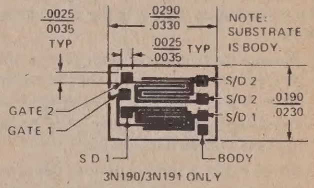
TO-99



DEVICE SCHEMATIC



2506C CHIP TOPOGRAPHY



ORDERING INFORMATION

TO-99	WAFER	DICE
3N165	3N165/W	3N165/D
3N166	3N166/W	3N166/D

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		MIN	MAX	UNITS	TEST CONDITIONS
I_{GSS}	Gate Reverse Leakage Current		10	pA	$V_{GS} = 40V$
$I_{G(f)}$	Gate Forward Leakage Current		−10	pA	$V_{GS} = -40V$
$I_{G(f)}$	Gate Forward Leakage Current (+125°C)		−25	pA	$V_{GS} = -40V$
I_{DSS}	Drain to Source Leakage Current		−200	pA	$V_{DS} = -20V$
I_{SDS}	Source to Drain Leakage Current		−400	pA	$V_{SD} = -20, V_{DB} = 0$
$I_{D(on)}$	On Drain Current	−5	−30	mA	$V_{DS} = -15V, V_{GS} = -10V$
$V_{GS(th)}$	Gate Source Threshold Voltage	−2	−5	V	$V_{DS} = -15V, I_D = -10\mu A$
$V_{GS(th)}$	Gate Source Threshold Voltage	−2	−5	V	$V_{DS} = V_{GS}, I_D = -10\mu A$
$r_{fs(on)}$	Drain Source On Resistance		300	ohms	$V_{GS} = -20V, I_D = -100\mu A$
g_{fs}	Forward Transconductance	1500	3000	µmhos	$V_{DS} = -15V, I_D = -10mA, f = 1kHz$
g_{os}	Output Admittance		300	µmhos	$V_{DS} = -15V, I_D = -10mA, f = 1kHz$
C_{iss}	Input Capacitance		3.0	pF	$V_{DS} = -15V, I_D = -10mA, f = 1MHz$
C_{rss}	Reverse Transfer Capacitance		0.7	pF	$V_{DS} = -15V, I_D = -10mA, f = 1MHz$
C_{oss}	Output Capacitance Input Shorted		3.0	pF	$V_{DS} = -15V, I_D = -10mA, f = 1MHz$
$R_E(Y_{fs})$	Real Part Forward Transconductance		1200	µmhos	$V_{DS} = -15V, I_D = -10mA, f = 100MHz$

MATCHING CHARACTERISTICS 3N165

		MIN	MAX	UNITS	TEST CONDITIONS
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.90	1.0		$V_{DS} = -15V, I_D = -1500\mu A, f = 1KHz$
V_{GS1-2}	Gate-Source Threshold Voltage Differential		100	mV	$V_{DS} = -15V, I_D = -500\mu A$
$\triangle V_{GS1-2}$	Gate Source Threshold Voltage Differential Change with Temperature		8	mV	$V_{DS} = -15V, I_D = -500\mu A$ $T = -55°C$ to $+25°C$
$\triangle V_{GS1-2}$	Gate-Source Threshold Voltage Differential Change with Temperature		10	mV	$V_{DS} = -15V, I_D = -500\mu A$ $T = +25°C$ to $+125°C$

3N170, 3N171
N-Channel Enhancement Mode MOS FET

FEATURES

- Low Switching Voltages—$V_{GS(th)} \leq 3.0$ V
- Fast Switching Times—$t_r \leq 10$ ns
- Low Drain-Source Resistance $r_{ds(on)} = 200\Omega$ (Max)
- Low Reverse Transfer Capacitance C_{rss} = 1.3pF (Max)

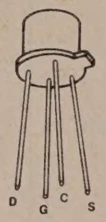
HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the device while wiring, testing, or in actual operation, by following the procedures outlined below:

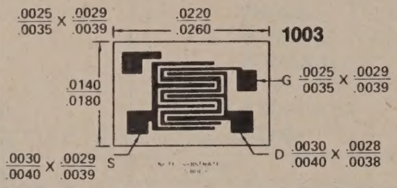
1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on as transient voltages may cause permanant damage to the devices.

PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY


.0025/.0035 X .0029/.0039
.0220/.0260
1003
.0140/.0180
G .0025/.0035 X .0029/.0039
.0030/.0040 X .0029/.0039 S
D .0030/.0040 X .0028/.0038

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	25	V
Drain-Gate Voltage	V_{DG}	±35	V
Gate-Source Voltage	V_{GS}	±35	V
Drain Current	I_D	30	mA
Power Dissipation @ T_A = 25°C	P_D	300	mW
Derate above 25°C		1.7	mW/°C
Power Dissipation @ T_C = 25°C	P_D	800	mW
Derate above 25°C		4.56	mW/°C
Operating Junction Temperature	T_J	175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

ORDERING INFORMATION

TO-72	WAFER	DICE
3N170	3N170/W	3N170/D
3N171	3N170/W	3N170/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connected to source.

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
OFF CHARACTERISTICS					
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	25		V	I_D = 10 μA, V_{GS} = 0
I_{GSS}	Gate Leakage Current		10	pA	V_{GS} = −35 V, V_{DS} = 0
			100		V_{GS} = −35 V, V_{DS} = 0, T_A = 125°C
I_{DSS}	Zero-Gate-Voltage Drain Current		10	nA	V_{DS} = 10 V, V_{GS} = 0
			1.0	μA	V_{DS} = 10 V, V_{GS} = 0, T_A = 125°C
ON CHARACTERISTICS					
$V_{GS(th)}$	Gate-Source Threshold Voltage	1.0	2.0	V	V_{DS} = 10 V, I_D = 10 μA 3N170
		1.5	3.0		3N171
$I_{D(on)}$	"ON" Drain Current	10		mA	V_{GS} = 10 V, V_{DS} = 10 V
$V_{DS(on)}$	Drain-Source "ON" Voltage		2.0	V	I_D = 10 mA, V_{GS} = 10 V
SMALL SIGNAL CHARACTERISTICS					
$r_{ds(on)}$	Drain-Source Resistance		200	Ω	V_{GS} = 10 V, I_D = 0, f = 1.0 kHz
$\|Y_{fs}\|$	Forward Transfer Admittance	1000		μmhos	V_{DS} = 10 V, I_D = 2.0 mA, f = 1.0 kHz
C_{rss}	Reverse Transfer Capacitance		1.3	pF	V_{DS} = 0, V_{GS} = 0, f = 1.0 MHz
C_{iss}	Input Capacitance		5.0	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz
$C_{d(sub)}$	Drain-Substrate Capacitance		5.0	pF	$V_{D(SUB)}$ = 10 V, f = 1.0 MHz
SWITCHING CHARACTERISTICS					
$t_{d(on)}$	Turn-On Delay Time		3.0	ns	V_{DD} = 10 V, $I_{D(on)}$ = 10 mA, $V_{GS(on)}$ = 10 V, $V_{GS(off)}$ = 0, R_G = 50 Ω
t_r	Rise Time		10	ns	
$t_{d(off)}$	Turn-Off Delay Time		3.0	ns	
t_f	Fall Time		15	ns	

INTERSIL

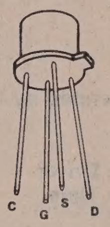
3N172, 3N173
Diode Protected P-Channel Enhancement Mode MOS FET

FEATURES

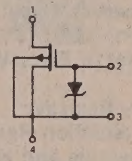
- High Input Impedance
- Diode Protected Gate

PIN CONFIGURATION

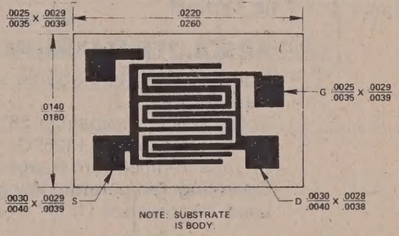
TO-72



DEVICE SCHEMATIC



CHIP TOPOGRAPHY 1503 Z


.0025/.0035 x .0029/.0039
.0220/.0260
.0140/.0180
G .0025/.0035 x .0029/.0039
.0030/.0040 x .0029/.0039 S
D .0030/.0040 x .0028/.0038
NOTE: SUBSTRATE IS BODY

ORDERING INFORMATION

TO-72	WAFER	DICE
3N172	3N172/W	3N172/D
3N173	3N173/W	3N173/D

MAXIMUM RATINGS (@ 25°C ambient unless noted)

		3N172	3N173
V_{GSS}	Gate to Source Voltage	–40V	–30V
V_{DSS}	Drain to Source Voltage	–40V	–30V
V_{SDS}	Source to Drain Voltage	–40V	–30V
V_{DGO}	Drain to Gate Voltage	–40V	–30V
I_D	Drain Current	–50 mA	–50 mA
$I_{G(f)}$	Gate Forward Current	10 μA	10 μA
$I_{G(r)}$	Gate Reverse Current	1.0 mA	1.0 mA
P_D	Power Dissipation	375 mW	
	Derating Factor	3.0 mW/°C	
T_J	Operating Junction Temperature	–55 to +150°C	
T_{stg}	Storage Temperature	–65 to +200°C	
T_L	Lead Temperature 1/16″ from Case for 10 sec max	+256°C	

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

PARAMETER		3N172		3N173		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSS}	Gate Reverse Current		–200		–500	pA	$V_{GS} = -20V$
I_{GSS}	Gate Reverse Current (+125°C)		–0.5		–1.0	μA	$V_{GS} = -20V$
BV_{GSS}	Gate Breakdown Voltage	–40	–125	–30	–125	V	$I_D = -10\,\mu A$
BV_{DSS}	Drain-Source Breakdown Voltage	–40		–30		V	$I_D = -10\,\mu A$
BV_{SDS}	Source-Drain Breakdown Voltage	–40		–30		V	$I_S = -10\,\mu A$, $V_{DB} = 0$
$V_{GS(th)}$	Threshold Voltage	–2.0	–5.0	–2.0	–5.0	V	$V_{DS} = V_{GS}$, $I_D = -10\,\mu A$
$V_{GS(th)}$	Threshold Voltage	–2.0	–5.0	–2.0	–5.0	V	$V_{DS} = -15V$, $I_D = -10\,\mu A$
V_{GS}	Gate Source Voltage	–3.0	–6.5	–2.5	–6.5	V	$V_{DS} = -15V$, $I_D = -500\,\mu A$
I_{DSS}	Zero Gate Voltage Drain Current		–0.4		–10	nA	$V_{DS} = -15V$
I_{SDS}	Zero Gate Voltage Source Current		–0.4		–10	nA	$V_{SD} = -15V$, $V_{DB} = 0$
$r_{ds(on)}$	Drain Source On Resistance		250		350	ohms	$V_{GS} = -20V$, $I_D = -100\,\mu A$
$I_{D(th)}$	On Drain Current	–5.0	–30	–5.0	–30	mA	$V_{DS} = -15V$, $V_{GS} = -10V$

INTERSIL

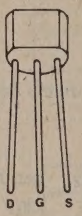
J174-J177
P-Channel JFET

APPLICATIONS
- Analog Switches
- Choppers
- Commutators

FEATURES
- Low Insertion Loss
  $r_{ds\ (on)} < 85\Omega$ (J174)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  $C_{sg(off)} < 5.5$ pF
  $C_{dg(off)} < 5.5$ pF
- Fast Switching
  $t_{d(on)} + t_r = 7$ ns Typical

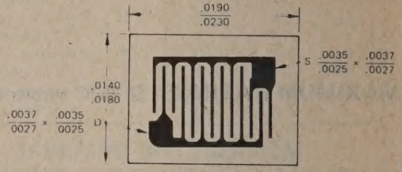
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5508B



NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION

TO-92	WAFER	DICE
J17X	J17X/W	J17X/D

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current .... 50 mA
Total Device Dissipation (25°C Free-Air Temperature) .... 350 mW
Power Derating (to +125°C) .... 3.5 mW/°C
Storage Temperature Range .... −55 to +125°C
Operating Temperature Range .... −55 to +125°C
Lead Temperature (1/16" from case for 10 seconds) .... 300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETERS				J174			J175			J176			J177			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			1			1			1			1	nA	$V_{DS} = 0$, $V_{GS} = 20V$
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	$V_{DS} = -15V$, $I_D = -10nA$
3		BV_{GSS}	Gate-Source Breakdown Voltage	30			30			30			30				$V_{DS} = 0$, $I_G = 1\mu A$
4		I_{DSS}	Saturation Drain Current (Note 3)	−20		−100	−7		−60	−2		−25	−1.5		−20	mA	$V_{DS} = -15V$, $V_{GS} = 0$
5		$I_{D(off)}$	Drain Cutoff Current (Note 2)			−1			−1			−1			−1	nA	$V_{DS} = -15V$, $V_{GS} = 10V$
6		$r_{DS(on)}$	Drain-Source ON Resistance			85			125			250			300	Ω	$V_{GS} = 0$, $V_{DS} = -0.1V$
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	$V_{DS} = 0$, $V_{GS} = 10V$ f = 1 MHz
8		$C_{sg(off)}$	Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5			
9		$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source Gate ON Capacitance		40			40			40			40			$V_{DS} = V_{GS} = 0$
10		$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions J174 J175 J176 J177 V_{DD} −10V −6V −6V −6V $V_{GS(off)}$ 12V 8V 6V 3V R_L 560Ω 12KΩ 5.6KΩ 10KΩ $V_{GS(on)}$ 0V 0V 0V 0V
11		t_r	Rise Time		5			10			20			25			
12		$t_{d(off)}$	Turn Off Delay Time		5			10			15			20			
13		t_f	Fall Time		10			20			20			25			

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration −300μs; duty cycle ≤ 3%.

3N188-3N191
Dual P-Channel Enhancement Mode MOS FET

FEATURES

- Very High Input Impedance
- Low Capacitance
- High Gate Breakdown 3N190-3N191
- V_g & (TH) Matched
- Zener Protected gate 3N188-3N189
- V_g & (TH) Tracking

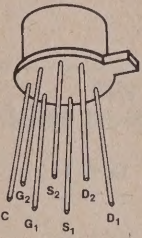
MAXIMUM RATINGS (@25°C ambient unless noted)

		3N188 3N189	3N190 3N191
V_{GSS}	Static Gate to Source Voltage	±40V	−40V
$V_{GSS}^{(1)}$	Transient Gate to Source Voltage	±40V	±125V
V_{DSS}	Drain to Source Voltage	−40V	−40V
V_{SDS}	Source to Drain Voltage	−40V	−40V
I_D	Drain Current	50 mA	50 mA
P_D	Power Dissipation		
	(each side)	300 mW	
	(both sides)	525 mW	
	Total Derating Factor	4.2 mW/°C	
T_j	Operating Junction Temperature	−55 to +150°C	
T_{stg}	Storage Temperature	−65 to +200°C	
T_l	Lead Temperature 1/16" from Case for 10 sec max	+300°C	

(1) Device must not be tested at ±125V more than once or for longer than 300 ms.

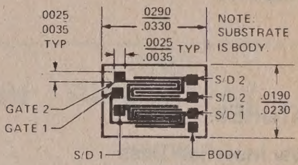
PIN CONFIGURATION

TO-99



CHIP TOPOGRAPHY

2506C



3N190/3N191 ONLY

ORDERING INFORMATION

TO-99	WAFER	DICE
3N188		
3N189		
3N190	3N190/W	3N190/D
3N191	3N191/W	3N191/D

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		3N188 3N189		3N190 3N191			
		MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
I_{GSS}	Gate Reverse Current				10	pA	V_{GS} = 40V
$I_{G(f)}$	Gate Forward Current		−200		−10	pA	V_{GS} = −40V
$I_{G(f)}$	Gate Forward Current @ 125°C		−200		−25	pA	V_{GS} = −40V
BV_{DSS}	Drain-Source Breakdown Voltage	−40		−40		V	I_D = −10µA
BV_{SDS}	Source-Drain Breakdown Voltage	−40		−40		V	I_S = −10µA, V_{BD} = 0
$V_{GS(th)}$	Threshold Voltage	−2.0	−5.0	−2.0	−5.0	V	V_{DS} = −15V, I_D = −10 µA
$V_{GS(th)}$	Threshold Voltage	−2.0	−5.0	−2.0	−5.0	V	V_{DS} = V_{GS}, I_D = −10 µA
V_{GS}	Gate Source Voltage	−3.0	−6.5	−3.0	−6.5	V	V_{DS} = −15V I_D = −500 µA
I_{DSS}	Zero Gate Voltage Drain Current		−200		−200	pA	V_{DS} = −15V
I_{SDS}	Source Drain Current		−400		−400	pA	V_{SD} = −15V, V_{DB} = 0
$r_{ds(on)}$	Drain-Source on Resistance		300		300	ohms	V_{DS} = −20V, I_D = −100 µA
$I_{D(on)}$	On Drain Current	−5.0	−30.0	−5.0	−30.0	mA	V_{DS} = −15V, V_{GS} = −10V
g_{fs}	Forward Transconductance	1500	4000	1500	4000	µmhos	V_{DS} = −15V, I_D = −5 mA, f = 1 kHz
Y_{OS}	Output Admittance		300		300	µmhos	V_{DS} = −15V, I_D = −5 mA, f = 1 kHz
C_{iss}	Input Capacitance Output Shorted		4.5		4.5	pF	V_{DS} = −15V, I_D = −5 mA, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		1.5		1.0	pF	V_{DS} = −15V, I_D = −5 mA, f = 1 MHz
C_{oss}	Output Capacitance Input Shorted		3.0		3.0	pF	V_{DS} = −15V, I_D = −5 mA, f = 1 MHz

SWITCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		MIN	MAX	UNITS	TEST CONDITIONS
$t_{D(on)}$	Turn On Delay Time		15	ns	V_{DD} = −15V, I_D = −5 mA
t_r	Rise Time		30	ns	R_G = R_L = 1.4 kΩ
t_{off}	Turn Off Time		50	ns	

MATCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted) 3N188 and 3N190

		MIN	MAX	UNITS	
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.85	1.0		V_{DS} = −15V, I_D = −500 µA, f = 1 kHz
V_{GS1-2}	Gate Source Threshold Voltage Differential		100	mV	V_{DS} = −15V, I_D = −500 µA
ΔV_{GS1-2}	Gate Source Threshold Voltage Differential Change with Temperature		8	mV	V_{DS} = −15V, I_D = −500 µA, T = −55°C to + 25°C
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature		10	mV	V_{DS} = −15V, I_B = −500 µA, T = +25°C to +125°C

INTERSIL

U200-U202
N-Channel JFET

Applications

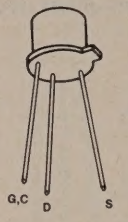
- Analog Switches
- Commutators
- Choppers

FEATURES

- Low Insertion Loss
- $r_{ds\ (on)} < 50\Omega$ (U202)
- Good Off-Isolation $I_{D(off)} < 1$ nA

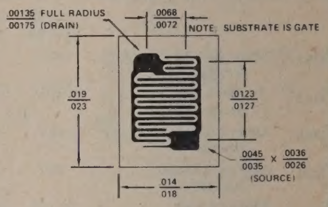
PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

5001B


.00135 / .00175 FULL RADIUS (DRAIN)
.0068 / .0072
NOTE: SUBSTRATE IS GATE
.019 / .023
.0123 / .0127
.0045 / .0035 × .0036 / .0026 (SOURCE)
.014 / .018

ORDERING INFORMATION

TO-18	WAFER	DICE
U200	U200/W	U200/D
U201	U201/W	U201/D
U202	U202/W	U202/D

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . −30 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . 1.8 W
Storage Temperature Range . . . . −65 to +200°C
Lead Temperature
Temperature . . . . −55 to +150°C
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic		U200		U201		U202		Unit	Test Conditions	
			Min	Max	Min	Max	Min	Max			
STATIC	I_{GSS}	Gate Reverse Current		−1		−1		−1	nA	$V_{GSS} = 20$ V, $V_{DS} = 0$	
				−1		−1		−1	μA		150°C
	BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		−30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−3	−1.5	−5	−3.5	−10		$V_{DS} = 20$ V, $I_D = 10$ nA	
	$I_{D(off)}$	Drain Cutoff Current		1		1		1	nA	$V_{DS} = 10$ V, $V_{GS} = -12$ V	
				1		1		1	μA		− 150°C
	I_{DSS}	Saturation Drain Current (Note 1)	3	25	15	75	30	150	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
	$r_{ds(on)}$	Drain-Source ON Resistance		150		75		50	ohm	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
DYN	C_{iss}	Common-Source Input Capacitance (Note 1)		30		30		30	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
	C_{rs}	Common Source Reverse Transfer Capacitance		3		8		8		$V_{DS} = 0$, $V_{GS} = -12$ V	

NOTE 1: Pulse test required, pulsewidth = 300 μsec, duty cycle ≤3%.

INTERSIL

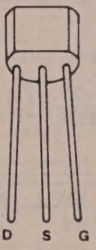
J201-J204
N-Channel JFET

FEATURES

- High Input Impedance (IG = 35pA Typ.)
- Low IGSS (IGSS = 100pA max)

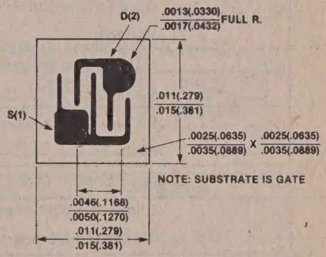
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5010


D(2)
.0013(.0330)/.0017(.0432) FULL R.
S(1)
.011(.279)/.015(.381)
.0025(.0635)/.0035(.0889) X .0025(.0635)/.0035(.0889)
.0046(.1168)/.0050(.1270)
.011(.279)/.015(.381)

NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION

TO-92	WAFER	DICE
J201	J201/W	J201/D
J202	J202/W	J202/D
J203	J203/W	J203/D
J204	J204/W	J204/D

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage.......... −40V
Gate Current............................50mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C).....................360mW
Operating Temperature Range....... −55 to 135°C
Storage Temperature Range......... −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds)...........300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETERS			J201			J202			J203			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
STATIC	I_{GSS}	Gate Reverse Current (Note 2)			−100			−100			−100	pA	$V_{DS}=0$, $V_{GS}=-20V$	
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.3		−1.5	−0.8		−4.0	−2.0		−10.0	V	$V_{DS}=20V$, $I_D=10$ nA	
	BV_{GSS}	Gate-Source Breakdown Voltage	−40			−40			−40				$V_{DS}=0$, $I_G=-1\mu A$	
	I_{DSS}	Saturation Drain Current (Note 3)	0.2		1.0	0.9		4.5	4.0		20	mA	$V_{DS}=20V$, $V_{GS}=0$	
	I_G	Gate Current (Note 1)		−3.5			−3.5			−3.5		pA	$V_{DG}=20V$, $I_D=200\mu A$	
DYNAMIC	g_{fs}	Common-Source Forward Transconductance(Note 2)	500			1,000			1,500			µmho	$V_{DS}=20V$, $V_{GS}=0$	f = 1 kHz
	g_{os}	Common Source Output Conductance		1			3.5			10				
	C_{iss}	Common-Source Input Capacitance		4			4			4		pF		f = 1 MHz
	C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1				
	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		5			5			5		$\frac{nV}{\sqrt{Hz}}$	$V_{DS}=10V$, $V_{GS}=0$	f = 1 kHz

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2ms.

	PARAMETERS		J204			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX			
STATIC	I_{GSS}	Gate Reverse Current (Note 2)			– 100	pA	$V_{DS} = 0$, $V_{GS} = -20V$	
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	– 0.5		– 2.0	V	$V_{DS} = 20V$, $ID = 10$ nA	
	BV_{GSS}	Gate-Source Breakdown Voltage	– 25				$V_{DS} = 0$, $I_G = -\mu A$	
	I_{DSS}	Saturation Drain Current (Note 3)		1.2		mA	$V_{DS} = 20V$, $V_{GS} = 0$	
	I_G	Gate Current (Note 1)		– 3.5		pA	$V_{DG} = 20V$, $I_D = 200\mu A$	
DYNAMIC	g_{fs}	Common-Source Forward Transconductance(Note 2)		1500		μmho	$V_{DS} = 20V$, $V_{GS} = 0$	f = 1 kHz
	g_{os}	Common Source Output Conductance		2.5				
	C_{iss}	Common-Source Input Capacitance		4		pF		f = 1 MHz
	C_{rss}	Common-Source Reverse Transfer Capacitance		1				
	e_n	Equivalent Short-Circuit Input Noise Voltage		10		$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10V$, $V_{GS} = 0$	f = 1 kHz

INTERSIL

U231-U235
Monolithic Dual N-Channel JFET

APPLICATIONS
- Differential Amplifiers
- Low and Maximum Frequency Amplifiers

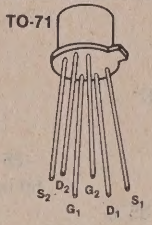
FEATURES
- Good Matching Characteristics

ABSOLUTE MAXIMUM RATINGS (25° C)

Gate-Drain or Gate-Source Voltage .... −50V
Gate Current .... 50 mA
Total Device Dissipation at 25° C
(Derate 1.7 mW/° C to 200° C) .... 300 mW
Storage Temperature Range .... −65 to +200° C
Lead Temperature
(1/16″ from case for 10 seconds) .... 300° C

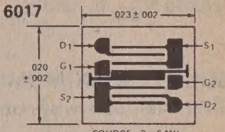
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6017



SOURCE 3 x 6 MIL
DRAIN 3 x 3 MIL
GATE 3 x 3 MIL

ORDERING INFORMATION

TO-71	WAER	DICE
U23X	U23X/W	U23X/D

ELECTRICAL CHARACTERISTICS
TEST CONDITIONS: 25° C unless otherwise noted.

		Characteristic		Min	Max	Unit	Test Conditions	
1		I_{GSS}	Gate Reverse Current		−100	pA	$V_{GS} = -30V$, $V_{DS} = 0$	
2					−500	nA		150° C
3	S	BV_{GSS}	Gate-Source Breakdown Voltage	−50		V	$I_G = 1\mu A$, $V_{DS} = 0$	
4	T	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−4.5		$V_{DS} = 20V$, $I_D = 1$ nA	
5	A	V_{GS}	Gate-Source Voltage	−0.3	−4.0		$V_{DG} = 20V$, $I_D = 200\mu A$	
6	T I	I_G	Gate Operating Current		−50	pA		
	C				−250	nA		125° C
7		I_{DSS}	Saturation Drain Current (Note 1)	0.5	5.0	mA	$V_{DS} = 20V$, $V_{GS} = 0$	
8		g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	3000	µmho	$V_{DS} = 20V$, $V_{GS} = 0$	f = 1 kHz
	D			1000				f = 100 MHz
9	Y	g_{fs}	Common-Source Forward Transconductance (Note 1)	600	1600		$V_{DG} = 20V$, $I_D = 200\mu A$	f = 1 kHz
10	N	g_{os}	Common-Source Output Capacitance		35		$V_{DS} = 20V$, $V_{GS} = 0$	
11	A	g_{os}	Common-Source Output Conductance		10		$V_{DG} = 20V$, $I_D = 200\mu A$	
12	M	C_{iss}	Common-Source Input Capacitance		6	pF	$V_{DS} = 20V$, $V_{GS} = 0$	f = 1 MHz
13	I C	C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		80	$\frac{nV}{\sqrt{Hz}}$		f = 100 Hz

		Characteristic		U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Unit	Test Conditions	
15		$\lvert I_{G1}-I_{G2} \rvert$	Differential Gate Current	10	10	10	10	10	nA	$V_{DG} = 20V$, $I_D = 200\mu A$	125° C
16		$\frac{(I_{DSS1}-I_{DSS2})}{I_{DSS1}}$	Saturation Drain Current Match (Note 1)	5	5	5	10	15	%	$V_{DS} = 20V$, $V_{GS} = 0$	
17	M A	$\lvert V_{GS1}-V_{GS2} \rvert$	Differential Gate-Source Voltage	5	10	15	20	25	mV	$V_{DG} = 20V$, $I_D = 200\mu A$	
18	T C H	$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)	10	25	50	75	100	µV/° C		$T_A = 25°C$ $T_B = 125°C$
19	I			10	25	50	75	100			$T_A = -55°C$ $T_B = 25°C$
20	N G	$\frac{(g_{fs1}-g_{fs2})}{g_{fs1}}$	Transconductance Match (Note 1)	3	5	5	10	15	%		f = 1 kHz
21		$\lvert g_{os1}-g_{os2} \rvert$	Differential Output Conductance	5	5	5	5	5	µmho		

NOTES:
1. Pulse test required, pulsewidth = 300 µs, duty cycle ≤ 3%.
2. Measured at end points, T_A and T_B.

INTERSIL

U257
Dual Monolithic N-Channel JFET

FEATURES

- $g_{fs} > 5000$ µmho from dc to 100 MHz
- Matched V_{GS}, g_{fs} and g_{os}

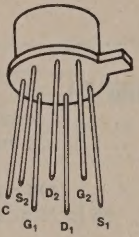
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	−25 V
Gate Current	50 mA
Device Dissipation (Each Side), $T_A = 85°C$ (Derate 3.85 mW/°C)	250 mW
Total Device Dissipation, $T_A = 85°C$ (Derate 7.7 mW/°C)	500 mW
Storage Temperature Range	−65°C to +150°C

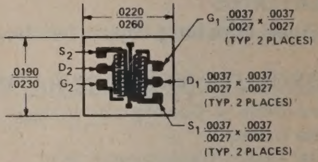
PIN CONFIGURATION

TO-99



CHIP TOPOGRAPHY

6022


.0220
.0260
.0190
.0230
S2
D2
G2
G1 .0037/.0027 × .0037/.0027 (TYP. 2 PLACES)
D1 .0037/.0027 × .0037/.0027 (TYP. 2 PLACES)
S1 .0037/.0027 × .0037/.0027 (TYP. 2 PLACES)

ORDERING INFORMATION

TO-99	WAFER	DICE
U257	U257/W	U257/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−100	pA	$V_{GS} = 15$ V, $V_{DS} = 0$	
			−250	nA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	$I_G = -1$ µA, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1	−5		$V_{DS} = 10$ V, $I_D = 1$ nA	
I_{DSS}	Saturation Drain Current (Note 1)	5	40	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	µmho	$V_{DS} = 10$ V, $I_D = 5$ mA	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000		$V_{DG} = 10$ V, $I_D = 5$ mA	f = 100 MHz
g_{os}	Common-Source Output Conductance		150		$V_{DS} = 10$ V, $I_D = 5$ mA	f = 1 kHz
g_{oss}	Common-Source Output Conductance		150		$V_{DG} = 10$ V, $I_D = 5$ mA	f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
$\overline{e_n}$	Equivalent Input Noise Voltage		30	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage (Note 1)	0.85	1		$V_{DS} = 10$ V, $V_{GS} = 0$	
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		100	mV	$V_{DG} = 10$ V, $I_D = 5$ mA	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.85	1			f = 1 kHz
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		20	µmho		

NOTE:
1. Pulse test required, pulse width = 300 µs, duty cycle ≤ 30%.

INTERSIL

U304-U306
P-Channel JFET

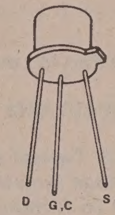
APPLICATIONS
- Analog Switches
- Commutators
- Choppers

FEATURES
- ON Resistance <85 ohms (U304)
- $I_{D(off)}$ <500 pA
- Switches directly from T²L Logic (U306)

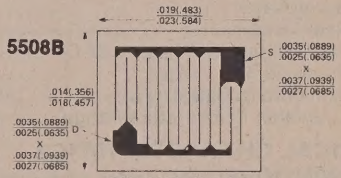
ABSOLUTE MAXIMUM RATINGS (25°C)
Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . . 30V
Gate Current . . . . 50 mA
Total Device Dissipation, Free-Air
(Derate 2.8 mW/°C) . . . . 350 mW
Storage Temperature Range . . . . −65 to +150°C
Lead Temperature
(1/16″ from case for 60 seconds) . . . . 300°C

PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY



NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION

TO-18	WAFER	DICE
U304	U304/W	U304/D
U305	U305/W	U305/D
U306	U306/W	U306/D

ELECTRICAL CHARACTERISTICS
TEST CONDITIONS: 25°C unless otherwise noted.

		Characteristic		U304 Min	U304 Max	U305 Min	U305 Max	U306 Min	U306 Max	Unit	Test Conditions	
1		I_{GSS}	Gate Reverse Current		500		500		500	pA	V_{GS} = 20V, V_{DS} = 0	
2					1.0		1.0		1.0	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4		V_{DS} = −15V, I_D = −1µA	
5	STATIC	$V_{DS(on)}$	Drain-Source ON Voltage		−1.3		−0.8		−0.6		V_{GS} = 0, I_D = −15mA(U304), I_D = −7mA (U305), I_D = −3mA (U306)	
6		I_{DSS}	Saturation Drain Current (Note 2)	−30	−90	−15	−60	−5	−25	mA	V_{DS} = −15V, V_{GS} = 0	
7		$I_{D(off)}$	Drain Cutoff Current		−500		−500		−500	pA	V_{DS} = −15V, V_{GS} = 12V (U304), V_{GS} = 7V (U305), V_{GS} = 5V (U306)	
8					−1.0		−1.0		−1.0	µA		150°C
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0V, I_D = −1mA	
10		$r_{ds(on)}$	Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0V, I_D = 0	f = 1 kHz
11	DYN	C_{iss}	Common-Source Input Capacitance		27		27		27	pF	V_{DS} = −15V, V_{GS} = 0	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		V_{DS} = 0, V_{GS} = 12V (U304) V_{GS} = 7V (U305), V_{GS} = 5V (U306)	
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		20		25		25			
14		t_r	Rise Time		15		25		35			
15		$t_{d(off)}$	Turn-OFF Delay Time		10		15		20			
16		t_f	Fall Time		25		40		60			

	U304	U305	U306
V_{DD}	−10V	−6V	−6V
$V_{GS(off)}$	12V	7V	5V
R_L	580Ω	743Ω	1800Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	−15mA	−7mA	−3mA

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsewidth = 300µs, duty cycle ≤3%.

INTERSIL

J308-J310
N-Channel Silicon JFET

APPLICATIONS

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

FEATURES

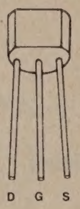
- **Industry Standard Part In Low Cost Plastic Package**
- **High Power Gain**
  11 dB Typical at 450 MHz
  Common-Gate
- **Low Noise - 2.7 dB Typical at 450 MHz**
- **Wide Dynamic Range Greater than 100 dB**
- **Easily Matches to 75 Ω Input**

ABSOLUTE MAXIMUM RATINGS (25°C)

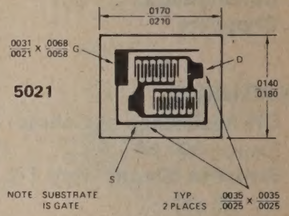
Drain-Gate Voltage	25V
Source-Gate Voltage	25V
Forward Gate Current	10 mA
Total Device Dissipation (T_{LEAD} = 25°C)	625 mW
Derate above 25°C	5.68 mW/°C
Storage Temperature Range	–55 to +150°C
Operating Junction Temperature Range	–55 to +135°C

PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY



ORDERING INFORMATION

TO-92	WAFER	DICE
J30X	J30X/W	J30X/D

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

PARAMETERS				J308			J309			J310					
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25			V	I_G = –1µA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current			–1.0			–1.0			–1.0	nA	V_{GS} = –15V, V_{DS} = 0	
3						–1.0			–1.0			–1.0	µA		T = +125°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1.0		–6.5	–1.0		–4.0	–2.0		–6.5	V	V_{DS} = 10V, I_D = 1nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	V_{DS} = 0, I_G = 1 mA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	8,000		20,000	10,000		20,000	8,000		18,000	µmhos	V_{DS} = 10V, I_D = 10mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			200			200			200			
9		g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000				
10		g_{og}	Common Gate Output Conductance		150			150			150				
11		C_{gd}	Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5	pF	V_{DS} = 0, V_{GS} = –10V	f = 1 MHz
12		C_{gs}	Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0			
13		e_n	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10V, I_D = 10 mA	f = 100 Hz
14	HIGH FREQ	$Re_{(Vfs)}$	Common-Source Forward Transconductance		12			12			12		mmho	V_{DS} = 10V, I_D = 10mA	f = 105 MHz
15		$Re_{(Vfg)}$	Common-Gate Input Conductance		14			14			14				
16		$Re_{(Vis)}$	Common-Source Input Conductance		0.4			0.4			0.4				
17		$Re_{(Vos)}$	Common-Source Output Conductance		0.15			0.15			0.15				
18		G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16		dB		
19		NF	Noise Figure		1.5			1.5			1.5				
20		G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11				f = 450 MHz
21		NF	Noise Figure		2.7			2.7			2.7				

NOTE: 1. Pulse test PW 300 µs, duty cycle ≤ 3%.

INTERSIL

U308-U310
N-Channel JFET

FEATURES

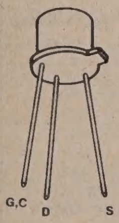
- High Power Gain
  - 15dB Typical at 100MHz, Common Gate
  - 10dB Typical at 450MHz, Common Gate
- Low Single Sideband Noise Figure
  - 1.5dB Typical at 100MHz, Common Gate
  - 3.2dB Typical at 450MHz, Common Gate
- Wide Dynamic Range — Greater than 100dB
- Offered in Wide Variety of Packages for Most Any Circuit Configuration.

GENERAL DESCRIPTION

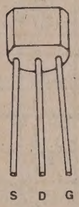
This family of N-channel Junction FETs are designed and characterized for VHF and UHF applications requiring high gain and low noise figure. The forward transconductance is relatively flat out to 1000MHz. Applications for these devices in military, commercial and consumer communications equipment include low noise, high gain RF amplifiers, low noise mixers with conversion gain, and low noise, ultra stable RF oscillators.

PIN CONFIGURATIONS

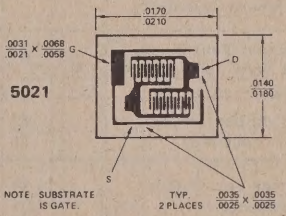
TO 52



TO-92



CHIP TOPOGRAPHY



ORDERING INFORMATION

TO-52	TO-92*	WAFER	DICE
U308		U308/W	U308/D
U309		U309/W	U309/D
U310		U310/W	U310/D

*See J308-310 data sheet for TO-92 package.

ABSOLUTE MAXIMUM RATINGS (25°C)

	TO-52	TO-92
Gate-Drain or Gate-Source Voltage	−25V	−25V
Gate Current	20mA	10mA
Total Power Dissipation	500mW	300mW
Power Derating (to maximum operating temperature)	4.0mW/°C	3.0mW/°C
Operating Temperature Range	−65 to 150°C	−55 to +125°C
Storage Temperature Range	−65 to 200°C	−55 to +125°C
Lead Temperature (1/16″ from case for 10 sec)	300°C	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC		U308			U309			U310			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSS}	Gate Reverse Current			-150			-150			-150	pA	$V_{GS} = -15$ V	
				-150			-150			-150	nA	$V_{GS} = 0$	T = 125°C
BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	$I_G = -1$ µA, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-6.0	-1.0		-4.0	-2.5		-6.0		$V_{DS} = 10$ V, $I_D = 1$ nA	
I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	$I_G = 10$ mA, $V_{DS} = 0$	
g_{fg}	Common-Gate Forward Transconductance (Note 1)	10		20	10		20	10		18	mmho	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 1 kHz
g_{ogs}	Common-Gate Output Conductance			150			150			150	µmho		
C_{gd}	Drain-Gate Capacitance			2.5			2.5			2.5	pF	$V_{GS} = -10$ V, $V_{DS} = 10$ V	f = 1 MHz
C_{gs}	Gate-Source Capacitance			5.0			5.0			5.0			
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 100 Hz
g_{fg}	Common-Gate Forward Transconductance		12			12			12		mmho	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 100 MHz
			11			11			11				f = 450 MHz
g_{ogs}	Common-Gate Output Conductance		0.18			0.18			0.18				f = 100 MHz
			0.7			0.7			0.7				f = 450 MHz
G_{pg}	Common-Gate Power Gain		15			15			15		dB		f = 100 MHz
			10			10			10				f = 450 MHz
NF	Noise Figure		1.5			1.5			1.5				f = 100 MHz
			3.2			3.2			3.2				f = 450 MHz

NOTE: Pulse test duration = 2 ms.

INTERSIL

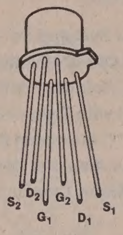
U401-U406
Monolithic Dual N-Channel JFET

FEATURES

- **Minimum System Error and Calibration — 5mV Offset Maximum (U401), 95dB Minimum CMRR (U401-04)**
- **Low Drift with Temperature — 10µV/°C Maximum (401, 02)**
- **Operates from Low Power Supply Voltages — $V_{GS(off)} < 2.5V$**
- **Simplifies Amplifier Design — Output Impedance >500KΩ**

PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

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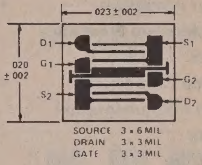


ORDERING INFORMATION

TO-71	WAFER	DICE
U40X	U40X/W	U40X/D

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage 50V
Forward Gate Current .... 10 mA
Device Dissipation (each side)
@ $T_A = 85°C$ derate 2.6 mW/°C .... 300 mW
Total Device Dissipation
@ $T_A = 85°C$ (derate 5 mW/°C) .... 500 mW
Storage Temperature Range ....–65 to 200°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25° unless otherwise noted.

		Characteristic		U401		U402		U403		U404		U405		U406		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–50		–50		–50		–50		–50		–50		V	$V_{DS} = 0$, $I_G = -1\mu A$	
2		I_{GSS}	Gate Reverse Current (Note 1)		–25		–25		–25		–25		–25		–25	pA	$V_{DS} = 0$, $V_{GS} = -30V$	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–5	–2.5	–.5	–2.5	–.5	–2.5	–.5	–2.5	–.5	–2.5	–.5	–2.5	V	$V_{DS} = 15V$, $I_D = 1\ nA$	
4		$V_{GS(on)}$	Gate-Source Voltage (on)		–2.3		–2.3		–2.3		–2.3		–2.3		–2.3		$V_{DG} = 15V$, $I_D = 200\mu A$	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	$V_{DS} = 10V$, $V_{GS} = 0$	
6					–15		–15		–15		–15		–15		–15	pA	$V_{DG} = 15V$, $I_D = 200\mu A$	
7		I_G	Gate Current (Note 1)		–10		–10		–10		–10		–10		–10	nA		$T_A = 125°C$
8		BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	$V_{DS} = 0$, $V_{GS} = 0$, $I_G = \pm1\mu A$	
9		g_{fs}	Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	µmho	$V_{DS} = 10V$, $V_{GS} = 0$	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		20		20		20		20		20		20			
11	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600		$V_{DG} = 15V$, $I_D = 200\mu A$	f = 1 kHz
12		g_{os}	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0			
13		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF		f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0			
15		e_N	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 15V$, $V_{GS} = 0$	f = 10 Hz
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20V, $I_D = 200\mu A$	
17		$\vert V_{GS1}-V_{GS2}\vert$	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	$V_{DG} = 10V$, $I_D = 200\mu A$	
18		$\frac{\Delta\vert V_{GS1}-V_{GS2}\vert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4)		10		10		25		25		40		80	µV/°C	$V_{DG} = 10V$, $I_D = 200\mu A$	$T_A = -55°C$, $T_B = +25°C$, $I_D = 200\mu A$ $T_C = +125°C$

NOTES:
1. Approximately doubles for every 10°C increase in T_A. 2. Pulse test duration = 300µs, duty cycle ≤ 3%. 3. $CMRR = 20 \log_{10}\left[\frac{\Delta V_{DD}}{\Delta|V_{GS1}-V_{GS2}|}\right]$ $\Delta V_{DD} = 10V$. 4. Measured at end points, T_A, T_B and T_C.

INTERSIL

U410 - U412
Monolithic Dual N-Channel JFET

APPLICATIONS

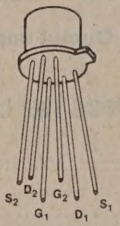
- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

FEATURES

- Minimum System Error and Calibration
  - 10 mV Offset Maximum (U410)
  - 70 dB Minimum CMRR (U410)
- Low Drift with Temperature
  - 10 μV/°C Maximum (U410)
- Simplifies Amplifier Design
  - Low Output Conductance

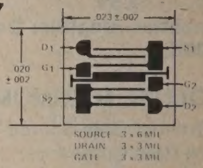
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6017



ORDERING INFORMATION

TO-71	WAFER	DICE
U410	U410/W	U410/D
U411	U411/W	U411/D
U412	U412/W	U412/D

ABSOLUTE MAXIMUM RATINGS (25°)

Gate-To-Gate Voltage .... ± 40 V
Gate-Drain or Gate-Source Voltage ....50 − 40 V
Gate Current ....50 mA
Total Package Dissipation (25°C Free-Air)...............375 mW
Power Derating.......................................3.0 mW/°C
Storage Temperature Range.................. − 65 to + 150°C
Lead Temperature
(1/16″ from case for 10 seconds)..........................300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic		U410			U411			U412			Unit	Test Conditions	
			Min	TYP	Max	Min	TYP	Max	Min	TYP	Max			
STATIC	I_{GSS}	Gate Reverse (Note 1)			− 200			− 200			− 200	pA	$V_{DS} = 0$, $V_{GS} = -30$ V	
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	− 1.0		− 3.5	− 1.0		− 3.5	− 1.0		− 3.5	V	$V_{DS} = 20$ V, $I_D = 1$ nA	
	BV_{GSS}	Gate-Source Breakdown Voltage	− 40			− 40			− 40				$V_{DS} = 0$ V, $I_G = -1$ μA	
	I_{DSS}	Saturation Drain Current (Note 2)	0.5		5.0	0.5		5.0	0.5		5.0	mA	$V_{DS} = 20$ V, $V_{GS} = 0$V	
	I_G	Gate Current (Note 1)			− 200			− 200			− 200	pA	$V_{DG} = 20$ V, $I_D = 200$ μA	
	V_{GS}	Gate-Source Voltage	− 0.2		− 3.0	− 0.2		− 3.0	− 0.2		− 3.0	V		
DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	μmho	$V_{DS} = 20$ V, $V_{GS} = 0$ V	f = 1 KHz
			600		1,200	600		1,200	600		1,200		$V_{DG} = 20$ V, $I_D = 200$ μA	
	g_{os}	Common-Source Output Conductance			20			20			20		$V_{DS} = 20$ V, $V_{GS} = 0$V	
					5			5			5		$V_{DG} = 20$ V, $I_D = 200$ μA	
	C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	$V_{DS} = 20$ V, $V_{GS} = 0$ V	f = 1 MHz
	C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2				
MATCHING	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage			50			50			50		$V_{DS} = 20$ V, $I_D = 200$ μA	f = 100 Hz
	$\lvert V_{GS_1} - V_{GS_2}\rvert$	Differential Gate-Source Voltage			10			20			40	mV	$V_{DG} = 20$ V, $I_D = 200$ μA	
	$\frac{\Delta\lvert V_{GS_1} - V_{GS_2}\rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			25			80	μV/°C	$V_{DG} = 20$ V, $I_D = 200$ μA $T_A = 25$°C to $T_B = 85$°C	
	CMRR	Common-Mode Rejection Ratio (Note 4)		80			80			70		dB	$V_{DD} = 10$ V to $V_{DD} = 20$ V $I_D = 200$ μA	

Note 1: Approximately doubles for every 10°C increase in T_A.
Note 2: Pulse test duration = 300 μsec; duty cycle ≤3%.
Note 3: Measured at end points, T_A and T_B.

Note 4: $\text{CMRR} = 20 \log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1} - V_{GS2}\rvert}\right]$ $\Delta V_{DD} = 10$ V.

U421-U426
Monolitic Dual N-Channel JFET

APPLICATIONS

- Very High Input Impedance Differential Amplifiers
- Electrometers
- Impedance Converters

FEATURES

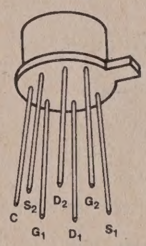
- High Input Impedance
  I_G = 0.1 pA Maximum (U421-3)
- High Gain g_{fs} = 140 μmho
  I_D = 30 μA (U421-3)
- Low Power Supply Operation
  $V_{GS(off)}$ = 2V Maximum (U421-3)
- Minimum System Error and Calibration
  10 mV Maximum Offset
  90 dB Minimum CMRR (U421, U424)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±40V
Gate-Drain or Gate-Source Voltage	−40V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3.2 mW/°C to 150°C)	400 mW
Total Device Dissipation, T_A = 25°C (Derate 6.0 mW/°C to 150°C)	750 mW
Storage Temperature Range	−65 to +150°C

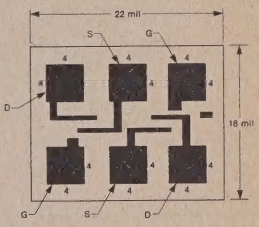
PIN CONFIGURATION

TO-99



CHIP TOPOGRAPHY

6034



ORDERING INFORMATION

TO-99	WAFER	DICE
U421	U421/W	U421/D
U422	U422/W	U422/D
U423	U423/W	U423/D
U424	U424/W	U424/D
U425	U425/W	U425/D
U426	U426/W	U426/D

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

		Characteristic		U421-3			U424-6			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1		BV_{GSS}	Gate-Source Breakdown Voltage	−40	−60		−40	−60		V	$I_G = -1\mu A$, $V_{DS} = 0$	
2		BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40				$I_G = -1\mu A$, $I_D = 0$, $I_S = 0$	
3	S	I_{GSS}	Gate Reverse Current (Note 1)			0.2			1.0	pA	T = +25°C	$V_{GS} = -20V$, $V_{DS} = 0$
	T					0.5			1.0	nA	T = +125°C	
4	A	I_G	Gate Operating Current (Note 1)			0.1			0.5	pA	T = +25°C	$V_{DG} = 10V$, $I_D = 30\mu A$
	T					−100			−500		T = +125°C	
5	I	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.4		−2.0	−0.4		−3.0	V	$V_{DS} = 10V$, $I_D = 1$ nA	
6	C	V_{GS}	Gate-Source Voltage			−1.8			−2.9		$V_{DG} = 10V$, $I_D = 30\mu A$	
7		I_{DSS}	Saturation Drain Current	60		1000	60		1800	μA	$V_{DS} = 10V$, $V_{GS} = 0$	
8		g_{fs}	Common-Source Forward Transconductance	300		800	300		1000	μ℧	$V_{DS} = 10V$, $V_{GS} = 0$	f = 1 kHz
9		g_{os}	Common-Source Output Conductance			3.0			5.0			
10	D	C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11	Y	C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5			
12	N	g_{fs}	Common-Source Forward Transconductance	140		250	135		300	μmho	$V_{DG} = 10V$, $I_D = 30\mu A$	f = 1 kHz
13	A	g_{os}	Common-Source Output Conductance			0.5			1.0			
14	M	e_n	Equivalent Short Circuit Input		20	50		20	70	nV/√Hz		f = 10 Hz
	I		Noise Voltage		10			10	50			f = 1 kHz
15	C	NF	Noise Figure			1.0			1.0	dB	f = 10 Hz	R_G = 10M Ω

		Characteristic		U421,4			U422,5			U423,6			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
16	M	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			15			25	mV	$V_{DG} = 10V$, $I_D = 30\mu A$
17	A T	$\frac{\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			10			25			40	μV/°C	$V_{DG} = 10V$, $I_D = 30\mu A$, $T_A = -55°C$, $T_B = 25°C$, $T_C = 125°C$
18	C H	CMRR	Common Mode Rejection Ratio (Note 3)	90	95		80	90		80	90		dB	$I_D = 30\mu A$, V_{DG} = 10 to 20V

NOTES: 1. Approximately doubles for every 10°C increase in T_A.

2. Measured at end points T_A, T_B and T_C.

3. $\text{CMRR} = \log_{10}\left[\frac{\Delta V_{DD}}{\Delta|V_{GS1}-V_{GS2}|}\right]$, $\Delta V_{DD} = 10V$

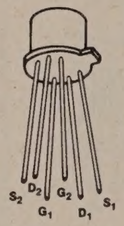
U440, U441
Matched Dual N-Channel JFET

Features

- **High Gain**
  g_{fs} = 4500 µmho Minimum

PIN CONFIGURATION

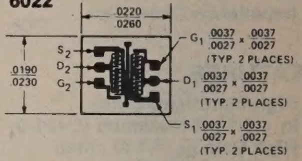
TO-71



S_2
D_2
G_2
G_1
D_1
S_1

CHIP TOPOGRAPHY

6022



.0220
.0260
.0190
.0230
S_2
D_2
G_2
G_1 $\frac{.0037}{.0027} \times \frac{.0037}{.0027}$
(TYP. 2 PLACES)
D_1 $\frac{.0037}{.0027} \times \frac{.0037}{.0027}$
(TYP. 2 PLACES)
S_1 $\frac{.0037}{.0027} \times \frac{.0037}{.0027}$
(TYP. 2 PLACES)

ORDERING INFORMATION

TO-71	WAFER	DICE
U440	U440/W	U440/D
U441	U441/W	U441/D

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage . . . . ± 50 V
Gate-Drain or Gate-Source Voltage . . . . – 25 V
Gate Current . . . . 50 mA
Total Package Dissipation
(25°C Free-Air Temperature) . . . . 350 mW
Power Derating . . . . 2.8 mW/°C
Storage Temperature Range . . . . – 65 to + 150°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic		U440			U441			Unit	Test Conditions	
			Min	Typ	Max	Min	Typ	Max			
STATIC	I_{GSS}	Gate Reverse Current (Note 1)			– 500			– 500	pA	V_{DS} = 0, V_{GS} = – 15 V	
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	– 1		– 6	– 1		– 6	V	V_{DS} = 10 V, I_D = 1 nA	
	BV_{GSS}	Gate-Source Breakdown Voltage	– 25			– 25				V_{DS} = 0, I_G = – 1µA	
	I_{DSS}	Saturation Drain Current (Note 2)	6		30	6		30	mA	V_{DS} = 10 V, V_{GS} = 0	
	I_G	Gate Current (Note 1)			– 500			– 500	pA	V_{DG} = 10 V, I_D = 5 mA	
DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500		9,000	4,500		9,000	µmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
	g_{os}	Common-Source Output Conductance			200			200			
	C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF		f = 1 MHz
	C_{rss}	Common-Source Reverse Transfer Capacitance		0.8			0.8				
MAT	V_{GS1}-V_{GS2}	Differential Gate-Source Voltage			10			20	mV	V_{DG} = 10 V, I_D = 5 mA	

NOTE 1: Approximately doubles for every 10°C increase in T_A.
NOTE 2: Pulse test duration = 300 µsec; duty cycle < 3%.

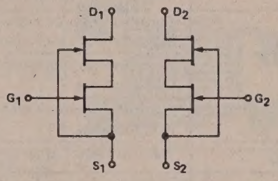
IT500-IT505
Dual Monolithic Cascode N-Channel JFET

FEATURES

- **$C_{MRR} > 120$ dB**
- **$I_G > 5$ pA @ $50V_{DG}$**
- **Low Miller Capacitance (C_{rss})**
- **Low $g_{os} > .025$ μmhos**

GENERAL DESCRIPTION

A low noise, low leakage FET that employs a cascode structure to accomplish very low I_G at high voltage levels, while giving high transconductance and very high common mode rejection ratio.


D1
D2
G1
G2
S1
S2

ABSOLUTE MAXIMUM RATINGS

(@ 25°C unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +150°C
Operating Temperature	+150°C
Lead Temperature (soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ 85°C Free Air Temperature

One Side	250 mW
Both Sides	500 mW

Linear Derating

One Side	3.85 mW/°C
Both Sides	7.7 mW/°C

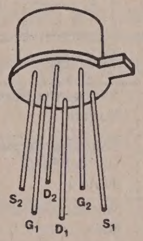
Maximum Voltages & Currents

V_{DS} Drain to Source Voltage	60V
V_{GS} Gate to Source Voltage	60V
V_{GD} Gate to Drain Voltage	60V
$V_{G1\,G2}$ Gate to Gate Voltage	60V
I_G Gate Current	50 mA

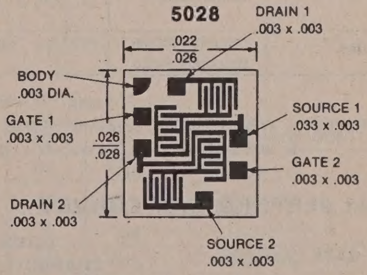
NOTE: Due to the non-symmetrical structure of these devices, the drain and source ARE NOT interchangeable.

PIN CONFIGURATION

TO-71 low profile


S2
D2
G2
G1
D1
S1

CHIP TOPOGRAPHY


5028
DRAIN 1
.003 x .003
.022
.026
BODY
.003 DIA.
GATE 1
.003 x .003
.026
.028
SOURCE 1
.033 x .003
GATE 2
.003 x .003
DRAIN 2
.003 x .003
SOURCE 2
.003 x .003

ORDERING INFORMATION

TO-78	WAFER	DICE
IT500	IT500/W	IT500/D
IT501	IT501/W	IT501/D
IT502	IT502/W	IT502/D
IT503	IT503/W	IT503/D
IT504	IT504/W	IT504/D
IT505	IT505/W	IT505/D

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

	Symbol	Characteristics	Min	Max	Unit	Test Conditions	
STATIC	I_{GSS}	Gate Reverse Current		-100	pA	$V_{GS} = -20V, V_{DS} = 0$	
				−5	nA		+125°C
	BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	$I_G = -1\ \mu A, V_{DS} = 0$	
	$V_{GS\ (off)}$	Gate-Source Cutoff Voltage	−0.7	−4		$V_{DS} = 20V, I_D = 1\ nA$	
	V_{GS}	Gate-Source Voltage	−0.2	−3.8			
	I_G	Gate Operating Current		−5	pA	$V_{DG} = 50V, I_D = 200\ \mu A$	
				−5	nA		125°C
	I_{DSS}	Saturation Drain Current (Note 1)	0.7	7	mA	$V_{DS} = 20V, V_{GS} = 0$	
DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	µmho	$V_{DS} = 20V, V_{GS} = 0$	f = 1 kHz
	g_{fs}	Common-Source Forward Transconductance (Note 1)	700	1600		$V_{DG} = 20V, I_D = 200\ \mu A$	
	g_{os}	Common-Source Output Conductance		1		$V_{DS} = 20V^*, V_{GS} = 0$	
	g_{os}	Common-Source Output Conductance		0.025		$V_{DS} = 20V, I_D = 200\ \mu A$	
	C_{g1g2}	Gate to Gate Capacitance		3.5	pF	$V_{G1} = V_{G2} = 10V$	f = 1 MHz
	C_{iss}	Common-Source Input Capacitance		7	pF	$V_{DS} = 20V, V_{GS} = 0$	
	C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3)		0.5			
	NF	Spot Noise Figure		0.5	dB		f = 100 Hz, $R_G = 10\ M\Omega$
	$\bar{e}_n$	Equivalent Input Noise Voltage		0.035 0.010	$\frac{\mu V}{\sqrt{Hz}}$		f = 10 Hz f = 1 kHz

	Symbol	Characteristics	IT500		IT501		IT502		IT503		IT504		IT505		Unit	Test Conditions	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
MATCHING	$I_{G1}-I_{G2}$	Differential Gate Current		5		5		5		5		10		15	nA	$V_{DG} = 20V,$ $I_D = 200\ \mu A$	+125°C
	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	0.90	1	0.85	1		—	$V_{DS} = 20V, V_{GS} = 0V$	
	$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	0.85	1	—		f = 1 kHz
	$V_{GS1}-V_{GS2}$	Differential Gate-Source Voltage		5		5		10		15		25		50	mV	$V_{DG} = 20V$ $I_D = 200\ \mu A$	
	$\frac{\Delta V_{GS1}-V_{GS2}}{\Delta T}$	Gate-Source Differential Voltage		5		10		20		40		100		200			$T_A = 25°C$ $T_B = 125°C$
		Change with Temp. (Note 2)		5		10		20		40					µV/°C		$T_A = -55°C$ $T_B = 25°C$
	C_{MRR}**	Common Mode Rejection Ratio	120		120		120		120						dB	$\Delta V_{DD} = 10V, I_D = 200\ \mu A$	

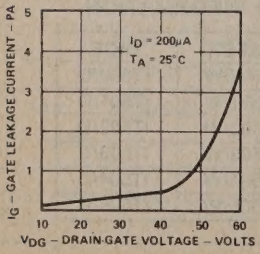
** $C_{MRR} = 20 \log_{10} \Delta V_{DD} / \Delta [V_{gs1} - V_{gs2}], \Delta V_{DD} = 10/ - 20V$

NOTES: 1. Pulse test required, pulsewidth = 300 µs, duty cycle ≤3%. 2. Measured at end points, T_A and T_B.

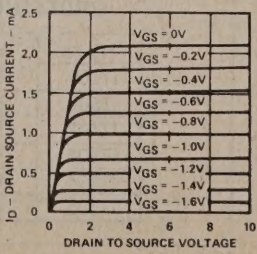
3. With case guarded C_{RSS} is typically < .15 pF

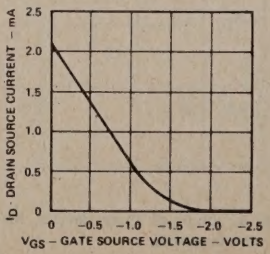
TYPICAL PERFORMANCE CURVES

GATE LEAKAGE

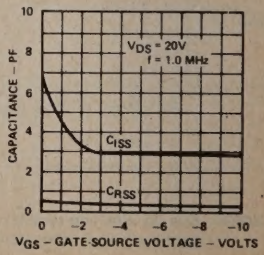


OUTPUT CHARACTERISTICS





TYPICAL CAPACITANCE VS. GATE-SOURCE VOLTAGE



MFE823
Enhancement Mode P-Channel MOSFET

APPLICATIONS

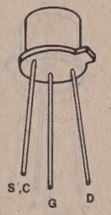
- High-Input Impedance Amplifiers
- Smoke Detectors
- Electrometers
- pH Meters

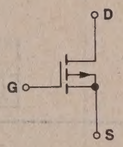
FEATURES

- High Input Impedance
  I_{GSS} = 30 Femto Amp Typical
- High Gain
  g_{fs} = 1000 μmho Minimum

PIN CONFIGURATION

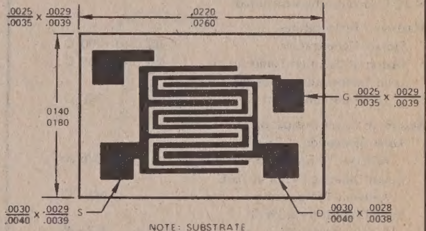
TO-18





CHIP TOPOGRAPHY

1503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D .0030/.0040 x .0028/.0038

NOTE: SUBSTRATE IS BODY

ORDERING INFORMATION

TO-18	WAFER	DICE
MFE823	MFE823/W	MFE823/D

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage . . . . 25 V
Gate-Source Voltage . . . . ± 10 V
Drain Current . . . . 30 mA
Total Device Dissipation at (Or Below) $T_A = 25°C$
(Derate 3 mW/°C to + 150°C) . . . . 375 mW
Operating Junction Temperature . . . . − 55 to + 150°C
Storage Temperature . . . . − 65 to + 200°C
Lead Temperature
(1/16″ from case for 10 seconds) . . . . 265°C

ELECTRICAL CHARACTERISTICS (25°C)

	Characteristic		Min	Max	Unit	Test Conditions
STATIC	I_{GSS}	Gate-Source Leakage Current		− 1.0	pA	$V_{GS} = -10$ V, $V_{DS} = 0$
	BV_{DSS}	Drain-Source Breakdown Voltage	− 25		V	$I_D = -10$ μA, $V_{GS} = 0$
	V_{GS}	Gate-Source Voltage	− 2.0	− 6.0	V	$V_{DS} = -10$ V, $I_D = -10$ μA
	I_{DSS}	Drain Cutoff Current		− 20	nA	$V_{DS} = -10$ V, $V_{GS} = 0$
	$I_{D(on)}$	ON Drain Current	− 3.0		mA	$V_{DS} = -10$ V, $V_{GS} = -10$ V
DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000		μmhos	$V_{DS} = -10$ V, $I_D = -2$ mA, f = 1 kHz
	C_{iss}	Common-Source Input Capacitance		6.0	pF	$V_{DS} = -10$ V, $V_{GS} = -10$ V, f = 1 MHz
	C_{rss}	Common-Source Reverse Transfer Capacitance		1.5 1.5		

INTERSIL

IT1700
P-Channel Enhancement Mode MOS FET

FEATURES

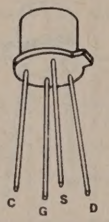
- Low On-Resistance – $r_{DS(on)} \leqslant 400$ ohms
- High Input Impedance – 10^{15} ohms
- High Gate Breakdown Voltage – V_{GSS} ±125 V
- Low Leakage – $I_{DSS} \leqslant 200$ ρA
- High Gain – $g_{fs} \geqslant 2000$ μmhos
- Low Noise Voltage – e_n 150 nV/√Hz typical @ 100 Hz

ABSOLUTE MAXIMUM RATINGS (Note 1)

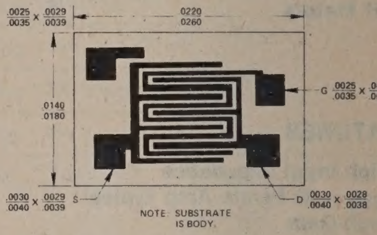
@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	−55°C to +150°C
Lead Temperature (soldering, 10 second time limit)	+300°C
Maximum Power Dissipation	
Total Dissipation at 25°C Ambient Temperature	0.375 W
Linear Derating Factor at 25°C Ambient Temperature	3 mW/°C
Total Dissipation at 25°C Case Temperature	1.25 W
Linear Derating Factor at 25°C Case Temperature	10 mW/°C
Maximum Voltages and Current	
V_{DSS} Drain to Source and Body Voltage	−40 V
V_{SDS} Source to Drain and Body Voltage	−40 V
V_{GSS} Transient Gate to Source Voltage (Note 2)	±125 V
V_{GSS} Gate to Source Voltage	−40 V
$I_{D(on)}$ Drain Current	50 mA

PIN CONFIGURATION
TO-72



CHIP TOPOGRAPHY
1503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G .0025/.0035 x .0029/.0039
.0030/.0040 x .0029/.0039 S
D .0030/.0040 x .0028/.0038
NOTE: SUBSTRATE IS BODY.

ORDERING INFORMATION

TO-72	WAFER	DICE
IT1700	IT1700/W	IT1700/D

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	−40		V	$V_{GS} = 0, I_D = -10\ \mu A$
BV_{SDS}	Source to Drain Breakdown Voltage	−40		V	$V_{GS} = 0, I_D = -10\ \mu A$
I_{GSS}	Gate Leakage Current				(See Note 2)
I_{DSS}	Drain to Source Leakage Current		200	pA	$V_{GS} = 0, V_{DS} = -20$ V
I_{DSS} (150°C)	Drain to Source Leakage Current		0.4	μA	$V_{GS} = 0, V_{DS} = -20$ V
I_{SDS}	Source to Drain Leakage Current		400	pA	$V_{GS} = 0, V_{DS} = -20$ V
I_{SDS} (150°C)	Source to Drain Leakage Current		0.8	μA	$V_{GS} = 0, V_{DS} = -20$ V
$V_{GS(th)}$	Gate Threshold Voltage	−2	−5	V	$V_{GS} = V_{DS}, I_D = -10\ \mu A$

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
$r_{DS\ (on)}$	Static Drain to Source "on" Resistance			400	ohms	$V_{GS} = -10$ V, $V_{DS} = 0$
$I_{DS\ (on)}$	Drain to Source "on" Current	2			mA	$V_{GS} = -10$ V, $V_{DS} = -15$ V
g_{fs}	Forward Transconductance Common Source	2000		4000	μmhos	$V_{DS} = -15$ V, $I_D = -10$ mA f = 1 kHz
C_{iss}	Small Signal, Short Circuit, Common Source, Input Capacitance			5	pF	$V_{DS} = -15$ V, $I_D = -10$ mA f = 1 MHz
C_{rss}	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance			1.2	pF	$V_{DG} = -15$ V, $I_D = 0$ f = 1 MHz
C_{oss}	Small Signal, Short Circuit, Common Source, Output Capacitance			3.5	pF	$V_{DS} = -15$ V, $I_D = -10$ mA f = 1 MHz
$\overline{e_n}$	Equivalent Input Noise Voltage		150		nV/√Hz	$V_{DS} = -15$ V, $I_D = -1$ mA f = 100 Hz; BW = 1 Hz

NOTE: 1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10 pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.

INTERSIL

IT1750
N-Channel Enhancement Mode MOS FET

FEATURES

- Low On-Resistance — 50Ω
- Low Capacitance — 1.7 pF
- High Gain — 3,000 μmhos
- High Gate Breakdown Voltage — ±125V
- Low Threshold Voltage — 3 V

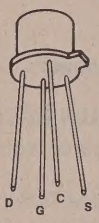
ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Operating Junction Temperature	-55°C to +150°C
Maximum Power Dissipation	
Total Dissipation at 25°C Ambient Temp.	375mW
Linear Derating Factor at 25°C Ambient Temp.	3 mW/°C
Maximum Voltages and Current	
V_{DSS} Drain to Source and Body Voltage	25 V
V_{GSS} Transient Gate to Source Voltage	±125 V
$I_{D(on)}$ Drain Current	100 mA

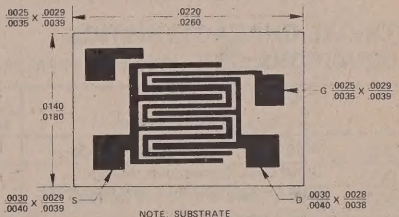
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

1003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.0220/.0260
.0140/.0180
G .0025/.0035 X .0029/.0039
.0030/.0040 X .0029/.0039 S
D .0030/.0040 X .0028/.0038

NOTE: SUBSTRATE IS BODY

ORDERING INFORMATION

TO-72	WAFER	DICE
IT1750	IT1750/W	IT1750/D

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Body connected to Source unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
$V_{GS(TH)}$	Gate to Source Threshold Voltage	0.50	1.5	3.0	V	$V_{DS} = V_{GS}$, $I_D = 10\ \mu A$; $V_{BS} = 0$
I_{DSS}	Drain Leakage Current		0.1	10	nA	$V_{DS} = 10$ V, $V_{GS} = V_{BS} = 0$
I_{GSS}	Gate Leakage Current (Note 2)					(See Note 2)
BV_{DSS}	Drain Breakdown Voltage	25			V	$I_D = 10\ \mu A$, $V_{GS} = V_{BS} = 0$
$r_{DS(on)}$	Drain To Source on Resistance		25	50	ohms	$V_{GS} = 20$ V, $V_{BS} = 0$
$I_{D(on)}$	Drain Current	10	50		mA	$V_{DS} = V_{GS} = 10$ V, $V_{BS} = 0$
Y_{fs}	Forward Transadmittance	3,000			μmhos	$V_{DS} = 10$ V, $I_D = 10$ mA, f = 1 KHz, $V_{BS} = 0$
C_{iss}	Total Gate Input Capacitance		5.0	6.0	pF	$I_D = 10$ mA, $V_{DS} = 10$ V, f = 1 MHz, $V_{BS} = 0$
C_{dg}	Gate to Drain Capacitance		1.3	1.6	pF	$V_{DG} = 10$ V, $V_{BS} = 0$

Note: 1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of <10pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.

INTERSIL

U1897-U1899
N-Channel JFET

FEATURES

- **Low insertion Loss**
  $r_{DS(on)} < 30\Omega$ (U1897)
- **No Error or Offset Voltage Generated by Closed Switch**

APPLICATIONS

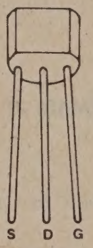
Analog, Switches, Choppers, Communicators

ABSOLUTE MAXIMUM RATINGS (25°)

Gate-Drain or Gate-Source Voltage.......... −40V
Forward Gate Current......................10mA
Total Continuous Device Dissipation
at (or Below) $T_A = 25°C$
(Derate 3.5mW/°C to 125°C)..............350mW
Storage Temperature Range....... −55 to +125°C
Operating Temperature Range..... −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds...........300°C

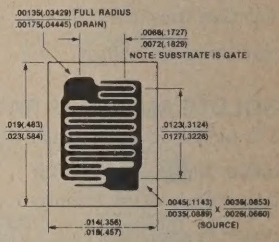
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5001B



ORDERING INFORMATION

TO-92	WAFER	DICE
U1897	U1897/W	U1897/D
U1898	U1898/W	U1898/D
U1899	U1899/W	U1899/D

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

		PARAMETERS	U1897		U1898		U1899		UNIT	TEST CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	$I_G = -1\mu A$, $V_{DS} = 0$
	BV_{DGO}	Drain-Gate Breakdown Voltage	40		40		40			$I_G = -1\mu A$, $I_S = 0$
	BV_{SGO}	Source-Gate Breakdown Voltage	40		40		40			$I_G = -1\mu A$, $I_D = 0$
	I_{GSS}	Gate Reverse Current		−400		−400		−400	pA	$V_{GS} = -20V$, $V_{DS} = 0$
	I_{DGO}	Drain-Gate Leakage Current		200		200		200		$V_{DG} = 20V$, $I_S = 0$
	I_{SGO}	Source-Gate Leakage Current		200		200		200		$V_{SG} = 20V$, $I_D = 0$
	$I_{D(off)}$	Drain Cutoff Current		200		200		200		$V_{DS} = 20V$, $V_{GS} = -12V$ (U1897)
				10		10		10	nA	$V_{GS} = -8V$ (U1898) $V_{GS} = -6V$ (U1899) $T_A = 85°C$
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−5.0	−10	−2.0	−7.0	−1.0	−5.0	V	$V_{DS} = 20V$, $I_D = 1$ na
	I_{DSS}	Saturation Drain Current (Note 1)	30		15		8.0		mA	$V_{DS} = 20V$, $V_{GS} = 0$
	$V_{DS(on)}$	Drain-Source ON Voltage		0.2		0.2		0.2	V	$V_{GS} = 0$, $I_D = 6.6mA$ (U1897) $I_D = 4.0mA$ (U1898) $I_D = 2.5mA$ (U1899)
	$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$I_D = 1mA$, $V_{GS} = 0$
DYNAMIC	C_{DG}	Drain-Gate Capacitance		5		5		5	pF	$V_{DG} = 20V$, $I_S = 0$ f = 1 MHz
	C_{SG}	Source-Gate Capacitance		5		5		5		$V_{SG} = 20V$, $I_D = 0$
	C_{iss}	Common-Source Input Capacitance		16		16		16		$V_{DS} = 20V$, $V_{GS} = 0$
	C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5		3.5		
	$t_{d(on)}$	Turn ON Delay Time		15		15		20	ns	Switching Time Test Conditions U1897 U1898 U1899 V_{DD} 3V 3V 3V $V_{GS(on)}$ 0 0 0 $V_{GS(off)}$ −12V −8V −6V R_L 430Ω 700Ω 1100Ω $I_{D(on)}$ 6.6mA 4mA 2.5mA
	t_r	Rise Time		10		20		40		
	t_{off}	Turn OFF Time		40		60		80		

NOTE: 1. Pulse test pulsewidth = 300 μs; duty cycle < 3%

2N2607-2N2609
2N2609 JAN
P-Channel JFET

APPLICATIONS

- Low-level Choppers
- Data Switches
- Commutators

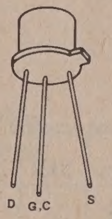
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+175°C
Lead Temperature (Soldering, 10 sec.)	+260°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	2.0 mW/°C
Maximum Voltages & Current	
V_{DG} Drain to Gate Voltage	30 V
V_{SG} Source to Gate Voltage	30 V
I_G Gate Current	50 mA

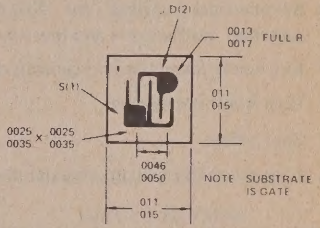
PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

5010 (for 2N2607, 8)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NOTE SUBSTRATE IS GATE
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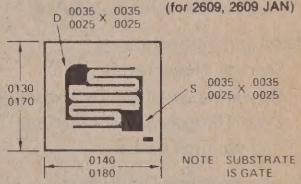
5503B (for 2609, 2609 JAN)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NOTE SUBSTRATE IS GATE

ORDERING INFORMATION

TO-18	WAFER	DICE
2N2607	2N2607/W	2N2607/D
2N2608	2N2608/W	2N2608/D
2N2609	2N2609/W	2N2609/D
2N2609 JAN	2N2609 JAN/W	2N2609 JAN/D

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

Characteristic		Test Conditions		2N2607		2N2608		2N2609		Unit
				Min	Max	Min	Max	Min	Max	
I_{GSS}	Gate-Source Cutoff Current	V_{GS} = 30 V, V_{DS} = 0			3		10		30	nA
		V_{GS} = 5 V, V_{DS} = 0, T_A = 150° C			3		10		30	µA
BV_{GDS}	Gate-Drain Breakdown Voltage	I_G = 1 µA, V_{DS} = 0		30		30		30		V
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = −5 V, I_D = −1 µA		1	4	1	4	1	4	V
I_{DSS}	Drain Current at Zero Gate Voltage	V_{DS} = −5 V, V_{GS} = 0		−0.30	−1.50	−0.90	−4.50	−2	−10	mA
g_{fs}	Small-Signal Common-Source Forward Transconductance	V_{DS} = −5 V, V_{GS} = 0, f = 1 kHz		330		1000		2500		µmho
C_{iss}	Gate-Source Input Capacitance	V_{DS} = −5 V, V_{GS} = 1 V, f = 140 kHz			10		17		30	pF
NF	Noise Figure	V_{DS} = −5 V, V_{GS} = 0, f = 1 kHz	R_G = 10 MΩ		3					dB
			R_G = 1 MΩ				3		3	

2N3684-2N3687
N-Channel JFET

FEATURES

- $C_{GSS} < 1.2$ pF
- Exceptionally high figure of merit
- Radiation Immunity
- Symmetrical devices for low-level choppers, data switches, multiplexers and low noise amplifiers
- Extremely low noise and capacitance
- High input impedance
- Zero offset
- High reliability silicon epitaxial planar construction

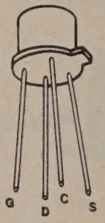
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−50 V
V_{GD} Gate to Drain Voltage	−50 V
I_G Gate Current	50 mA

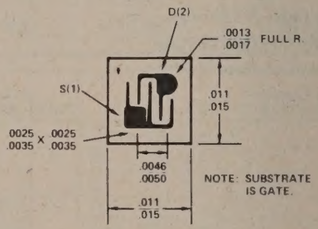
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5010



ORDERING INFORMATION

TO-72	WAFER	DICE
2N3684	2N3684/W	2N3684/D
2N3685	2N3685/W	2N3685/D
2N3686	2N3686/W	2N3686/D
2N3687	2N3687/W	2N3687/D

ELECTRICAL CHARACTERISTICS (25 °C unless otherwise specified)

PARAMETER		2N3684		2N3685		2N3686		2N3687		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage	−50		−50		−50		−50		V	$V_{DS} = 0$ V, $I_G = 1.0\ \mu A$
V_P	Pinch-Off Voltage	2.0	5.0	1.0	3.5	0.6	2.0	0.3	1.2	V	$V_{DS} = 20$ V, $I_D = 0.001\ \mu A$
I_{GSS}	Total Gate Leakage Current		−0.1		−0.1		−0.1		−0.1	nA	$V_{GS} = -30$ V, $V_{DS} = 0$
I_{GSS}	Total Gate Leakage Current (150°C)		−0.5		−0.5		−0.5		−0.5	μA	$V_{GS} = -30$ V, $V_{DS} = 0$ @150°C
I_{DSS}	Saturation Current, Drain-to-Source	2.5	7.5	1.0	3.0	0.4	1.2	0.1	0.5	mA	$V_{GS} = 0$ V, $V_{DS} = 20$ V
$\lvert Y_{fs} \rvert$	Forward Transadmittance	2000	3000	1500	2500	1000	2000	500	1500	μmhos	$V_{DS} = 20$ V, $V_{GS} = 0$ V f = 1 kHz
C_{iss}	Common Source Input Capacitance (Output Shorted)		4.0		4.0		4.0		4.0	pF	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 kHz
G_{os}	Small Signal, Common Source Output Conductance (input shorted)		50		25		10		5	μmhos	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 kHz
C_{rss}	Small Signal, Common Source Short Circuit Reverse Transfer Capacitance		1.2		1.2		1.2		1.2	pF	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 kHz
$r_{DS(on)}$	On Resistance		600		800		1200		2400	Ohms	$V_{DS} = 0$, $V_{GS} = 0$
NF	Noise Figure (Spot)		0.5		0.5		0.5		0.5	dB	f = 100 Hz, $R_G = 10\ M\Omega$ NBW = 6 Hz, $V_{DS} = 10$ V

2N3810/A, 2N3811/A
Monolithic Dual Matched PNP Transistor

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Temperature	200°C
Lead Temperature (10 seconds)	230°C

Maximum Power Dissipation

	One Side	Both Sides
Total Dissipation at 25°C Ambient Temperature	500 mW	600 mW
Linear Derating Factor	2.9 mW/°C	3.4 mW/°C

Maximum Voltage and Current (One side)

V_{EBO}	Emitter to Base Voltage	−5.0V
V_{CBO}	Collector to Base Voltage	−60V
V_{CEO}	Collector to Emitter Voltage	−60V
I_C	DC Collector Current	50 mA

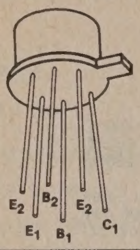
ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

SYMBOL	CHARACTERISTIC	2N3810 MIN.	2N3810 MAX.	2N3811 MIN.	2N3811 MAX.	UNITS	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current		10		10	nA	$V_{CB} = -50V$, $I_C = 0$
			10		10	μA	$V_{CB} = -50V$, $I_E = 0$, $T_A = 150°C$
I_{EBO}	Emitter Cutoff Current		20		20	nA	$V_{EB} = -4.0V$
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0		−5.0		V	$I_C = 0$, $I_E = 10\mu A$
BV_{CBO}	Collector to Base Breakdown Voltage	−60		−60		V	$I_E = 0$, $I_C = 10\mu A$
BV_{CEO}	Collector to Emitter Breakdown Voltage	−60		−60		V	$I_C = 10$ mA
h_{FE}	DC Current Gain	100		225			$I_C = 10\ \mu A$, $V_{CE} = -5.0V$
		150	450	300	900		$I_C = 100\mu A$, $V_{CE} = -5.0V$
		150	450	300	900		$I_C = 500\mu A$, $V_{CE} = -5.0V$
		150	450	300	900		$I_C = 1.0$ mA, $V_{CE} = -5.0V$
		125		250			$I_C = 10$ mA, $V_{CE} = -5.0V$
		75		150			$I_C = 100\mu A$, $V_{CE} = -5.0V$, $T_A = -55°C$
$V_{BE(ON)}$	Base to Emitter "On" Voltage		−0.7		−0.7	V	$I_C = 100\mu A$, $V_{CE} = -5.0V$
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage		−0.2		−0.2	V	$I_C = 100\mu A$, $I_B = 10\mu A$
			−0.25		−0.25	V	$I_C = 1.0$ mA, $I_B = 100\mu A$
$V_{BE(sat)}$	Base to Emitter Saturation Voltage		−0.7		−0.7	V	$I_C = 100\mu A$, $I_B = 10\mu A$
			−0.8		−0.8	V	$I_C = 1.0$ mA, $I_B = 100\mu A$
$\frac{h_{FE1}}{h_{FE2}}$	DC Current Gain Ratio	0.9	1.0	0.9	1.0		$V_{CE} = -5.0V$, $I_C = 0.1$ mA
$\lvert V_{BE1}-V_{BE2}\rvert$	Base to Emitter Voltage Differential		−5.0		−5.0	mV	$V_{CE} = -5.0V$, $I_C = 10\mu A$ to 10 mA
			−3.0		−3.0	mV	$V_{CE} = -5.0V$, $I_C = 100\mu A$
$\lvert \Delta(V_{BE1}-V_{BE2})\rvert$	Base to Emitter Voltage Differential Gradient		−1.0		−1.0	mV	$V_{CE} = -5.0V$, $I_C = 0.1$ mA
							$T_A = 25°C$ to $125°C$
			−0.8		−0.8	mV	$V_{CE} = -5.0V$, $I_C = 0.1$ mA
							$T_A = -55°C$ to $+25°C$
C_{ob}	Output Capacitance		4.0		4.0	pF	$V_{CB} = -5.0V$, $I_E = 0$, f = 100 kHz
C_{ib}	Input Capacitance		8.0		8.0	pF	$V_{EB} = 0.5V$, $I_C = 0$, f = 100 kHz
$\lvert h_{fe}\rvert$	Magnitude of Common Emitter Small Signal Current Gain	1.0		1.0			$I_C = 500\mu A$, $V_{CE} = -5.0V$, f = 30 MHz
		1.0	5.0	1.0	5.0		$I_C = 1.0$ mA, $V_{CE} = -5.0V$, f = 100 MHz
h_{ie}	Input Impedance	3.0	30	10	40	kΩ	$V_{CE} = -10V$, $I_C = 1.0$ mA, f = 1.0 kHz
h_{re}	Reverse Voltage Feedback Ratio		25		25	$\times 10^{-4}$	$V_{CE} = -10V$, $I_C = 1.0$ mA, f = 1.0 kHz
h_{oe}	Output Conductance	5.0	60	5.0	60	μmho	$V_{CE} = -10V$, $I_C = 1.0$ mA, f = 1.0 kHz
h_{fe}	Small Signal Current Gain	150	600	300	900		$V_{CE} = -10V$, $I_C = 1.0$ mA, f = 1.0 kHz
$RE(h_{ie})$	Real Part of Common Emitter Small Signal Input Impedance	3.0	30	10	40	kΩ	$V_{CE} = -10V$, $I_C = 1.0$ mA, f = 1.0 kHz
NF	Noise Figure		3.0		1.5	dB	$I_C = 100\mu A$, $V_{CE} = -10V$, f = 1.0 kHz, PBW = 200 Hz, $R_G = 3.0$ kΩ
			2.5		1.5	dB	$I_C = 100\mu A$, $V_{CE} = -10V$, f = 10 kHz, PBW = 2.0 kHz, $R_G = 3.0$ kΩ
			7.0		4.0	dB	$I_C = 100\mu A$, $V_{CE} = -10V$, f = 100 Hz, PBW = 20 Hz, $R_G = 3.0$ kΩ
			3.5		2.5	dB	$I_C = 100\mu A$, $V_{CE} = -10V$, $R_G = 3.0$ kΩ 3.0 dB down at 10 Hz and 10 kHz PBW = 15.7 kHz

PIN CONFIGURATION

TO-78



CHIP TOPOGRAPHY

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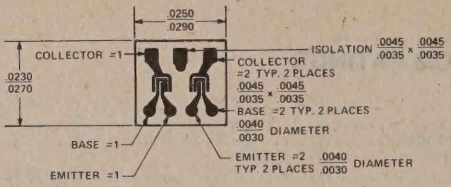


ORDERING INFORMATION

TO-78	WAFER	DICE
2N3810	2N3810/W	2N3810/D
2N3810A	2N3810A/W	2N3810A/D
2N3811	2N3811/W	2N3811/D
2N3811A	2N3811A/W	2N3811A/D

ELECTRICAL CONDITIONS

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

SYMBOL	CHARACTERISTIC	2N3810A		2N3811A		UNITS	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
I_{CBO}	Collector Cutoff Current		10		10	nA	V_{CB} = −50V, I_C = 0
			10		10	μA	V_{CB} = −50V, I_E = 0, T_A = 150°C
I_{EBO}	Emitter Cutoff Current		20		20	nA	V_{EB} = −4.0V
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0		−5.0		V	I_C = 0, I_E = 10μA
BV_{CBO}	Collector to Base Breakdown Voltage	−60		−60		V	I_E = 0, I_C = 10μA
BV_{CEO}	Collector to Emitter Breakdown Voltage	−60		−60		V	I_C = 10 mA
h_{FE}	DC Current Gain	100		225			I_C = 10μA, V_{CE} = −5.0V
		150	450	300	900		I_C = 100μA, V_{CE} = −5.0V
		150	450	300	900		I_C = 500μA, V_{CE} = −5.0V
		150	450	300	900		I_C = 1.0 mA, V_{CE} = −5.0V
		125		250			I_C = 10 mA, V_{CE} = −5.0V
		75		150			I_C = 100μA, V_{CE} = −5.0V, T_A = −55°C
$V_{BE(ON)}$	Base to Emitter "On" Voltage		−0.7		−0.7	V	I_C = 100μA, V_{CE} = −5.0V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage		−0.2		−0.2	V	I_C = 100μA, I_B = 10μA
			−0.25		−0.25	V	I_C = 1.0 mA, I_B = 100μA
$V_{BE(sat)}$	Base to Emitter Saturation Voltage		−0.7		−0.7	V	I_C = 100μA, I_B = 10 μA
			−0.8		−0.8	V	I_C = 1.0 mA, I_B = 100μA
$\frac{h_{FE1}}{h_{FE2}}$	DC Current Gain Ratio	0.95	1.0	0.95	1.0		V_{CE} = −5.0V, I_C = 0.1 mA
		0.85	1.0	0.85	1.0		V_{CE} = −5.0V, I_C = 0.1 mA,
							T_A = −55°C to +125°C
$\lvert V_{BE1}-V_{BE2}\rvert$	Base to Emitter Voltage Differential		−5.0		−5.0	mV	V_{CE} = −5.0V, I_C = 10μA to 10 mA
			−1.5		−1.5	mV	V_{CE} = −5.0V, I_C = 100μA
$\lvert\Delta(V_{BE1}-V_{BE2})\rvert$	Base to Emitter Voltage Differential Gradient		−0.5		−0.5	mV	V_{CE} = −5.0V, I_C = 0.1 mA
							T_A = 25°C to 125°C
			−0.4		−0.4	mV	V_{CE} = −5.0V, I_C = 0.1 mA
							T_A = −55°C to +25°C
C_{ob}	Output Capacitance		4.0		4.0	pF	V_{CB} = −5.0V, I_E = 0, f = 100 kHz
C_{ib}	Input Capacitance		8.0		8.0	pF	V_{EB} = 0.5V, I_C = 0, f = 100 kHz
$\lvert h_{fe}\rvert$	Magnitude of Common Emitter Small Signal Current Gain	1.0		1.0			I_C = 500μA, V_{CE} = −5.0V, f = 30 mHz
		1.0	5.0	1.0	5.0		I_C = 1.0 mA, V_{CE} = 5.0V, f = 100 MHz
h_{ie}	Input Impedance	3.0	30	10	40	kΩ	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
h_{re}	Reverse Voltage Feedback Ratio		25		25	x 10^{-4}	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
h_{oe}	Output Conductance	5.0	60	5.0	60	μmho	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
h_{fe}	Small Signal Current Gain	150	600	300	900		V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
$RE(h_{ie})$	Real Part of Common Emitter Small Signal Input Impedance	3.0	30	10	40	kΩ	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
NF	Noise Figure		3.0		1.5	dB	I_C = 100μA, V_{CE} = −10V, f = 1.0 kHz, PBW = 200 Hz, R_G = 3.0 kΩ
			2.5		1.5	dB	I_C = 10μA, V_{CE} = −10V, f = 10 kHz, PBW = 2.0 kHz, R_G = 3.0 kΩ
			7.0		4.0	dB	I_C = 100μA, V_{CE} = −10V, f = 100 Hz, PBW = 20 Hz, R_G = 3.0 kΩ
			3.5		2.5	dB	I_C = 100μA, V_{CE} = −10V, R_G = 3.0 kΩ, 3 dB down at 10 Hz and 10 kHz PBW = 15.7 kHz

INTERSIL

2N3821, 2N3822
N-Channel JFET

FEATURES

- **Low Capacitance**
- **Up to 6500 μmho Transconductance**

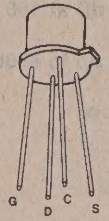
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−50 V
V_{GD} Gate to Drain Voltage	−50 V
I_G Gate Current	10 mA

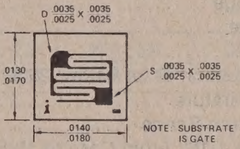
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5003B



ORDERING INFORMATION

TO-72	WAFER	DICE
2N3821	2N3821/W	2N3821/D
2N3822	2N3822/W	2N3822/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3821		2N3822		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		−0.1		−0.1	nA	$V_{GS} = -30$ V; $V_{DS} = 0$	
			−0.1		−0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		V	$I_G = -1$ μA, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4		−6		$V_{DS} = 15$ V, $I_D = 0.5$ nA	
V_{GS}	Gate-Source Voltage	−0.5	−2				$V_{DS} = 15$ V, $I_D = 50$ μA	
				−1	−4		$V_{DS} = 15$ V, $I_D = 200$ μA	
I_{DSS}	Saturation Drain Current	0.5	2.5	2	10	mA	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 3)	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	4500	3000	6500	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	1500		3000				f = 100 MHz
g_{os}	Common-Source Output Conductance (Note 1)		10		20			f = 1 kHz
C_{iss}	Common-Source Input Capacitance		6		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3		3			
NF	Noise Figure		5		5	dB	$V_{DS} = 15$ V, $V_{GS} = 0$, $R_{gen} = 1$ meg, BW = 5 Hz	f = 10 Hz
$\overline{e_n}$	Equivalent Input Noise Voltage		200		200	$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 15$ V, $V_{GS} = 0$, BW = 5 Hz	

NOTE: 1. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

INTERSIL

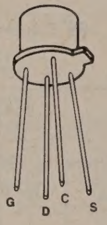
2N3823
N-Channel JFET

FOR VHF AMPLIFIER OSCILLATOR MIXER APPLICATIONS

- **Noise Figure < 2.5 dB at 100 MHz**
- **Low Capacitance**
- **Transconductance up to 6500 μmho**

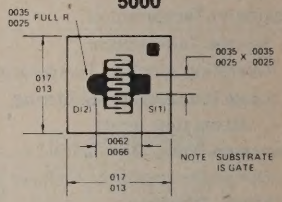
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5000



ORDERING INFORMATION

TO-72	WAFER	DICE
2N3823	2N3823/W	2N3823/D

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Source Voltage	−30V
Gate-Drain Voltage	−30V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature	300 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature 1/16″ From Case to 10 Sec	300°C

ELECTRICAL CHARACTERISTICS (25°C)

CHARACTERISTIC		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.5	nA	$V_{GS} = -20V$, $V_{DS} = 0$	
			−0.5	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−8		$V_{DS} = 15V$, $I_D = 0.5$ nA	
V_{GS}	Gate-Source Voltage	−1.0	−7.5		$V_{DS} = 15V$, $I_D = 400\ \mu A$	
I_{DSS}	Saturation Drain Current	4	20	mA	$V_{DS} = 15V$, $V_{GS} = 0$ (Note 3)	
g_{fs}	Common-Source Forward Transconductance	3,500	6,500	μmho	$V_{DS} = 15V$, $V_{GS} = 0$	f = 1 kHz (Note 1)
$\lvert Y_{fs}\rvert$	Common-Source Forward Transadmittance	3,200				f = 100 MHz
g_{os}	Common-Source Output Transconductance		35			f = 1 kHz (Note 1)
g_{iss}	Common-Source Input Conductance		800			f = 200 MHz
g_{oss}	Common-Source Output Conductance		200			
C_{iss}	Common-Source Input Capacitance		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2			
NF	Noise Figure		2.5	dB	$V_{DS} = 15V$, $V_{GS} = 0$ $R_G = 1\ k\Omega$	f = 100 MHz

NOTE 1: These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

INTERSIL

2N3824
N-Channel
JFET

FOR HIGH SPEED COMMUTATORS AND CHOPPERS

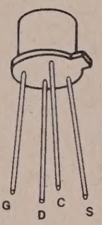
- r_{ds} < 250 ohms
- $I_{D(off)}$ < 0.1 nA

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Source Voltage .... −50V
Gate-Drain Voltage .... −50V
Gate Current .... 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature .... 300 mW
Storage Temperature Range .... −65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds) ... 300°C

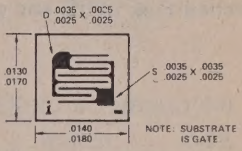
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5003B



ORDERING INFORMATION

TO-72	WAFER	DICE
2N3824	2N3824/W	2N3824/D

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

CHARACTERISTIC		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.1	nA	V_{GS} = −30V, V_{DS} = 0	
			−0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−50		V	I_G = 1 μA, V_{DS} = 0	
$I_{D(off)}$	Drain Cutoff Current		0.1	nA	V_{DS} = 15V, V_{GS} = −8V	
			0.1	μA		150°C
$r_{ds(on)}$	Drain-Source ON Resistance		250	Ω	V_{GS} = 0V, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 15V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF	V_{GS} = −8V, V_{DS} = 0	

INTERSIL

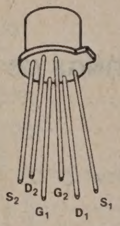
2N3921, 2N3922
Dual Monolithic N-Channel JFET

MATCHED FET PAIRS FOR DIFFERENTIAL AMPLIFIERS

- **I_G < 250 pA (25 nA at 100°C)**
- **g_{oss} < 20 μmhos (I_D = 700 μA)**
- **Matched V_{GS}, ΔV_{GS}, and g_{fs}**

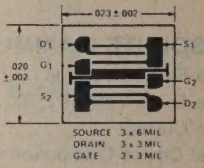
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6017



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage .... −50V
Gate Current .... 50 mA
Total Device Dissipation (Derate 1.7 mW/°C to 200°C) ... 300 mW
Storage Temperature Range .... −65 to +200°C

ORDERING INFORMATION

TO-71	WAFER	DICE
2N3921	2N3921/W	2N3921/D
2N3922	2N3922/W	2N3922/D

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

CHARACTERISTIC		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−1	nA	V_{GS} = −30V, V_{DS} = 0	
			−1	μA		100°C
BV_{DGO}	Drain-Gate Breakdown Voltage	50		V	I_D = 1 μA, I_S = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−3		V_{DS} = 10V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	−0.2	−2.7		V_{DS} = 10V, I_D = 100μA	
I_G	Gate Operating Current		−250	pA	V_{DG} = 10V, I_D = 700μA	
			−25	nA		100°C
I_{DSS}	Saturation Drain Current (Note 1)	1	10	mA	V_{DS} = 10V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	7500	μmho	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		35			
C_{iss}	Common-Source Input Capacitance		18	pF		
C_{rss}	Common-Source Reverse Transfer Capacitance		6			
g_{fs}	Common-Source Forward Transconductance	1500		μmho	V_{DG} = 10V, I_D = 700 μA	f = 1 kHz
g_{oss}	Common-Source Output Conductance		20			
NF	Spot Noise Figure		2	dB	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz, R_G = 1 meg

CHARACTERISTIC		2N3921		2N3922		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5	mV	V_{DG} = 10V, I_D = 700 μA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature		10		25	μV/°C		T_A = 0°C t_B = 100°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.95	1.0	0.95	1.0	—		f = 1 kHz

NOTE: 1. Pulse test duration = 2 ms.

INTERSIL

2N3954-2N3958
Monolithic Dual N-Channel JFET

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifiers requiring low offset voltage, drift, noise, and capacitance.

FEATURES

- Offset Voltage < 5 mV • Drift < 5 µV/°C
- Low Capacitance — C_{iss} = 4 pF Max
- Spot Noise Figure = 0.5 dB Max
- Superior Tracking Ability
- Low Output Conductance — g_{os} = 35 µmho Max

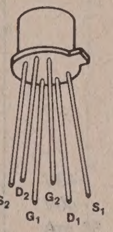
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Any Case-To-Lead Voltage		±100 V
Gate-Drain or Gate-Source Voltage		−50 V
Gate-To-Gate Voltage		±100 V
Gate Current		50 mA
Total Device Dissipation 85°C	(Each Side)	250 mW
Case Temperature	(Both Sides)	500 mW
Power Derating	(Each Side)	2.86 mW/°C
	(Both Sides)	4.3 mW/°C
Storage Temperature Range		−65°C to +125°C
Lead Temperature (1/16″ from case for 10 seconds)		300°C

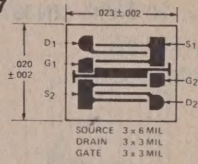
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6017



ORDERING INFORMATION

TO-71	WAFER	DICE
2N3954	2N3954/W	2N3954/D
2N3954A	2N3954A/W	2N3954A/D
2N3955	2N3955/W	2N3955/D
2N3955A	2N3955A/W	2N3955A/D
2N3956	2N3956/W	2N3956/D
2N3957	2N3957/W	2N3957/D
2N3958	2N3958/W	2N3958/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		−100		−100		−100		−100		−100		−100		−100	pA	V_{GS} = −30 V,	
			−500		−500		−500		−500		−500		−500		−500	nA	V_{DS} = 0	T_A = 125°C
BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		−50		−50		−50		V	V_{DS} = 0 I_G = 1 µA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5	−1.0	−4.5		V_{DS} = 20 V, I_D = 1 nA	
$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		2.0		2.0		2.0		V_{DS} = 0 I_G = 1 mA	
V_{GS}	Gate-Source Voltage		−4.2		−4.2		−4.2		−4.2		−4.2		−4.2		−4.2		V_{DS} = 20 V	I_D = 50 µA
		−0.5	−4.0	−0.5	−4.0	−0.5	−4.0	−0.4	−4.0	−0.5	−4.0	−0.5	−4.0	−0.5	−4.0			I_D = 200 µA
I_G	Gate Operating Current		−50		−50		−50		−50		−50		−50		−50	pA	V_{DS} = 20 V,	
			−250		−250		−250		−250		−250		−250		−250	nA	I_D = 200 µA	T_A = 125°C
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
		1000		1000		1000		1000		1000		1000		1000				f = 200 MHz
g_{os}	Common-Source Output Conductance		35		35		35		35		35		35		35			f = 1 kHz
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0		4.0		4.0		4.0		4.0	pF		f = 1 MHz
C_{rss}	Common Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2		1.2		1.2		1.2			
C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5		0.5		0.5		0.5		0.5	dB	V_{DS} = 20 V V_{GS} = 0 R_G = 10 MΩ	f = 100 Hz
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10		10		10		10	nA	V_{DS} = 20 V, I_D = 200 µA	T = 125°C
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0		V_{DS} = 20 V V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		5.0		10.0		5.0		15		20		25	mV	V_{DS} = 20 V, I_D = 200 µA	
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2		4.0		6.0		8.0			T = 25°C to −55°C
			1.0		0.5		2.5		1.5		5.0		7.5		10.0			T = 25°C to 125°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0			f = 1 kHz

2N3970-2N3972
N-Channel
JFET

FEATURES

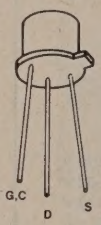
- $r_{DS(on)} < 30$ ohms (2N3970)
- $I_{D(off)} < 250$ pA
- Fast Switching

ABSOLUTE MAXIMUM RATINGS (25° C)

Reverse Gate-Drain Voltage	−40V
Gate-Source Voltage	−40V
Gate Current	50 mA
Total Device Dissipation at 25°C Case Temperature	1.8 W
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16" from case for 60 seconds)	300°C

PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

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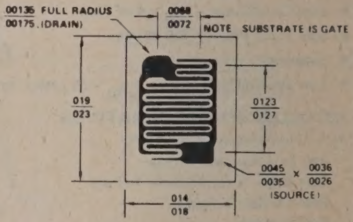

00135 / 00175 FULL RADIUS (DRAIN)
0068 / 0072
NOTE SUBSTRATE IS GATE
019 / 023
0123 / 0127
0045 / 0035 x 0036 / 0026 (SOURCE)
014 / 018

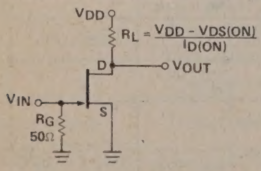
ORDERING INFORMATION

TO-18	WAFER	DICE
2N3970	2N3970/W	2N3970/D
2N3971	2N3971/W	2N3971/D
2N3972	2N3972/W	2N3972/D

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

CHARACTERISTIC		2N3970		2N3971		2N3972		UNIT	TEST CONDITIONS		
		MIN	MAX	MIN	MAX	MIN	MAX				
BV_{GSS}	Gate Reverse Breakdown Voltage	−40		−40		−40		V	$I_G = -1\mu A$, $V_{DS} = 0$		
I_{DGO}	Drain Reverse Current		250		250		250	pA	$V_{DG} = 20V$, $I_S = 0$		
			500		500		500	nA			150° C
$I_{D(off)}$	Drain Cutoff Current		250		250		250	pA	$V_{DG} = 20V$, $V_{GS} = -12V$		
			500		500		500	nA			150° C
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−2	−5	−0.5	−3	V	$V_{DS} = 20V$, $I_D = 1$ nA		
I_{DSS}	Saturation Drain Current (Pulse width 300μs, duty cycle ≤ 3%)	50	150	25	75	5	30	mA	$V_{DS} = 20V$, $V_{GS} = 0$		
$V_{DS(on)}$	Drain-Source ON Voltage						2		$V_{GS} = 0$	$I_D = 5$ mA	
					1.5			V		$I_D = 10$ mA	
			1							$I_D = 20$ mA	
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 1$ mA		
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz
C_{iss}	Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = 20V$, $V_{GS} = 0$		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		6		6		6		$V_{DS} = 0$, $V_{GS} = -12V$		
									$V_{DD} = 10V$, $V_{GS(on)} = 0$		
t_d	Turn-On Delay Time		10		15		40			$I_{D(on)}$	$V_{GS(off)}$
t_r	Rise Time		10		15		40	ns	2N3970	20 mA	−10V
t_{off}	Turn-Off Time		30		60		100		2N3971	10 mA	− 5V
									2N3972	5 mA	− 3V



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

INTERSIL

2N3993, 2N3994
P-Channel JFET

FEATURES

- Low $r_{DS(on)}$ – 150Ω Max (2N3993)
- High Y_{fs}/C_{iss} Ratio (High-Frequency Figure-of-Merit)

APPLICATIONS

Used in high-speed commutator and chopper applications. Also ideal for "Virtual Gnd" switching; needs no ext. translator circuit to switch ±10 VAC. Can be driven direct from T^2L or CMOS logic.

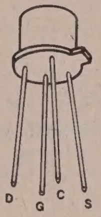
MAXIMUM RATINGS

@25°C free-air temperature (unless otherwise noted)

Drain-Gate Voltage	–25 V
Drain-Source Voltage	–25 V
Reverse Gate-Source Voltage	+25 V
Continuous Forward Gate Current	–10 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 1)	300 mW
Storage Temperature Range	–65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300°C

PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

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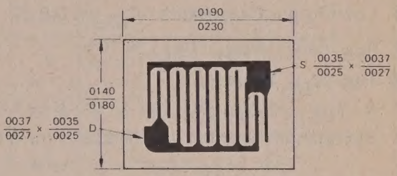

NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION

TO-72	WAFER	DICE
2N3993	2N3993/W	2N3993/D
2N3994	2N3994/W	2N3994/D

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	2N3993		2N3994		UNIT
			MIN	MAX	MIN	MAX	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = 1\ \mu A$, $V_{DS} = 0$	25		25		V
I_{DGO}	Drain Reverse Current	$V_{DG} = -15\ V$, $I_s = 0$		–1.2		–1.2	nA
		$V_{DG} = -15\ V$, $I_s = 0$, $T_A = 150°C$		–1.2		–1.2	μA
I_{DSS}	Zero-Gate-Voltage Drain Current	$V_{DS} = -10\ V$, $V_{GS} = 0$, See Note 2	–10		–2		mA
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = -10\ V$, $V_{GS} = 6\ V$				–1.2	nA
		$V_{DS} = -10\ V$, $V_{GS} = 6\ V$, $T_A = 150°C$				–1	μA
		$V_{DS} = -10\ V$, $V_{GS} = 10\ V$		–1.2			nA
		$V_{DS} = -10\ V$, $V_{GS} = 10\ V$, $T_A = 150°C$		–1			μA
$V_{GS(off)}$	Gate-Source Voltage	$V_{DS} = -10\ V$, $I_D = -1\ \mu A$	4	9.5	1	5.5	V
$r_{ds(on)}$	Small-Signal Drain-Source On-State Resistance	$V_{GS} = 0$, $I_D = 0$, f = 1 kHz		150		300	Ω
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	$V_{DS} = -10\ V$, $V_{GS} = 0$, f = 1 kHz, See Note 2	6	12	4	10	mmho
C_{iss}	Common-Source Short-Circuit Input Capacitance	$V_{DS} = -10\ V$, $V_{GS} = 0$, f = 1 MHz, See Note 3		16		16	pF
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance	$V_{DS} = 0$, $V_{GS} = 6\ V$, f = 1 MHz				5	pF
		$V_{DS} = 0$, $V_{GS} = 10\ V$, f = 1 MHz		4.5		4.5	pF

NOTES: 2. These parameters must be measured using pulse techniques. $t_p = 100$ ms, duty cycle ≤ 10%.

3. This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating.

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† The fourth lead (case) is connected to the source for all measurements.

2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880
Dual Monolithic Matched NPN Silicon Planar Transistors

FEATURES

- High Gain At Low Current $h_{FE} \geq 200$ @ 10 μA
- Low Output Capacitance $C_{obo} \leq 0.8$ pF
- h_{FE} Match $h_{FE_1} / h_{FE_2} \leq 10\%$
- Tight V_{BE} Tracking
  $\Delta (V_{BE_1} - V_{BE_2}) \leq 3\ \mu V/^\circ C$ −55°C to +125°C
- Dielectrically isolated matched pairs for differential amplifiers.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

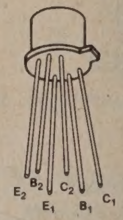
Maximum Power Dissipation

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7mW/°	2.9mW/°C	2.3mW/°C	4.3mW/°C

		2N4044 2N4878	2N4100 2N4879	2N4045 2N4880
V_{CBO}	Collector to Base Voltage	60 V	55 V	45 V
V_{CEO}	Collector to Emitter Voltage	60 V	55 V	45 V
V_{EBO}	Emitter to Base Voltage (Note 2)	7 V	7 V	7 V
V_{CCO}	Collector to Collector Voltage	100 V	100 V	100 V
I_C	Collector Current	10mA	10mA	10mA

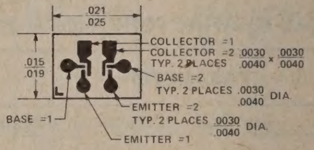
PIN CONFIGURATION

TO-71
TO-78



CHIP TOPOGRAPHY

4000


.021
.025
.015
.019
COLLECTOR =1
COLLECTOR =2 .0030/.0040 x .0030/.0040
TYP. 2 PLACES
BASE =2
TYP. 2 PLACES .0030/.0040 DIA.
EMITTER =2
TYP. 2 PLACES .0030/.0040 DIA.
EMITTER =1
BASE =1
L

ORDERING INFORMATION

TO-78	TO-71	WAFER	DICE
2N4044		2N4044/W	2N4044/D
2N4045		2N4045/W	2N4045/D
2N4100		2N4100/W	2N4100/D
	2N4878		
	2N4879		
	2N4880		

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200	600	150	600	80	800		$I_C = 10\ \mu A$, $V_{CE} = 5V$
h_{FE}	DC Current Gain	225		175		100			$I_C = 1.0$ mA, $V_{CE} = 5$ V
$h_{FE}(-55^\circ C)$	DC Current Gain	75		50		30			$I_C = 10\ \mu A$, $V_{CE} = 5$ V
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7	V	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
$V_{CE(sat)}$	Collector Saturation Voltage		0.35		0.35		0.35	V	$I_C = 1.0$ mA, $I_B = 0.1$ mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1	nA	$I_E = 0$, $V_{CB} = 45$ V, 30 V*
$I_{CBO}(+150^\circ C)$	Collector Cutoff Current		0.1		0.1		0.1	μA	$I_E = 0$, $V_{CB} = 45$ V, 30 V*
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1	nA	$I_C = 0$, $V_{EB} = 5$ V
C_{obo}	Output Capacitance		0.8		0.8		0.8	pF	$I_E = 0$, $V_{CB} = 5$ V

2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
C_{TE}	Emitter Transition Capacitance		1		1		1	pF	$I_C = 0, V_{EB} = 0.5V$
C_{C_1, C_2}	Collector to Collector Capacitance		0.8		0.8		0.8	pF	$V_{CC} = 0$
I_{C_1, C_2}	Collector to Collector Leakage Current		5		5		5	pA	$V_{CC} = \pm 100V$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		55		45		V	$I_C = 1mA, I_B = 0$
f_T	Current Gain Bandwidth Product	200		150		150		MHz	$I_C = 1mA, V_{CE} = 10V$
f_T	Current Gain Bandwidth Product	20		15		15		MHz	$I_C = 10\mu A, V_{CE} = 10V$
NF	Narrow Band Noise Figure		2		3		3	dB	$I_C = 10\mu A, V_{CE} = 5V$ f = 1kHz R_G = 10 kohms BW = 200 Hz
BV_{CBO}	Collector Base Breakdown Voltage	60		55		45		V	$I_C = 10\mu A, I_E = 0$
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		V	$I_E = 10\mu A, I_C = 0$

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	0.9	1	0.85		0.8	1		$I_C = 10\mu A$ to 1mA, $V_{CE} = 5V$
$\|V_{BE_1}-V_{BE_2}\|$	Base Emitter Voltage Differential		3		5		5	mV	$I_C = 10\mu A, V_{CE} = 5V$
$\|I_{B_1}-I_{B_2}\|$	Base Current Differential		5		10		25	nA	$I_C = 10\mu A, V_{CE} = 5V$
$\|\triangle(V_{BE_1}-V_{BE_2})\|/°C$	Base Current Differential Voltage Differential Change with Temperature		3		5		10	µV/°C	$I_C = 10\mu A$, $V_{CE} = 5V$ $T_A = -55°C$ to $+125°C$
$\|\triangle(I_{B_1}-I_{B_2})\|/°C$	Base Current Differential Change with Temperature		0.3		0.5		1	nA/°C	$I_C = 10\mu A$, $V_{CE} = 5V$ $T_A = -55°C$ to $+125°C$

SMALL SIGNAL CHARACTERISTICS

PARAMETER		TYPICAL VALUE	UNIT	TEST CONDITIONS
h_{ib}	Input Resistance	28	ohms	$I_C = 1mA, V_{CB} = 5V$
h_{rb}	Voltage Feedback Ratio	4.3	$\times 10^{-4}$	$I_C = 1mA, V_{CB} = 5V$
h_{fe}	Small Signal Current Gain	250		$I_C = 1mA, V_{CB} = 5V$
h_{ob}	Output Conductance	0.6	$\times 10^{-7}$mhos	$I_C = 1mA, V_{CB} = 5V$
h_{ie}	Input Resistance	9.6	k ohms	$I_C = 1mA, V_{CB} = 5V$
h_{re}	Voltage Feedback Ratio	4.2	$\times 10^{-4}$	$I_C = 1mA, V_{CB} = 5V$
h_{oe}	Output Conductance	12	µmhos	$I_C = 1mA, V_{CB} = 5V$

NOTES:

1. These ratings are limiting values above which the serviceablity of any semiconductor device may be impaired.
2. The reverse base-to-enter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 µamps.
3. The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

INTERSIL

ITE4091-ITE4093
2N4091-2N4093, JANTX*
N-Channel JFET

FEATURES

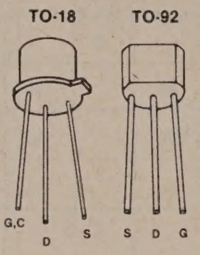
- $r_{DS(ON)} < 30$ ohms (2N4091)
- $I_{D(OFF)} < 100$ pA (JAN TX Types)
- Fast Switching

ABSOLUTE MAXIMUM RATINGS

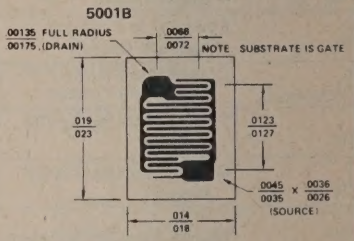
@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperatures	−55°C to +200°C
Operating Junction Temperature	−55 to +175°C
Lead Temperature (Soldering, 10 sec)	+300°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	360 mW
Linear Derating TO 18	10 mW/°C
TO 92	16 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−40 V
V_{GD} Drain to Drain Voltage	−40 V
V_{DG} Drain to Gate Voltage	40 V
I_G Gate Current	10 mA

PIN CONFIGURATIONS



CHIP TOPOGRAPHY


5001B
.00135 / .00175 FULL RADIUS (DRAIN)
0068 / 0072
NOTE SUBSTRATE IS GATE
019 / 023
0123 / 0127
0045 / 0035 x 0036 / 0026 (SOURCE)
014 / 018

ORDERING INFORMATION

TO-92	TO-18*	WAFER	DICE
ITE 4091	2N4091	2N4091/W	2N4091/D
ITE 4092	2N4092	2N4092/W	2N4092/D
ITE 4093	2N4093	2N4093/W	2N4093/D

*add JANTX to these part numbers if JANTX processing is desired.

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

Characteristic			4091		4092		4093		Unit	Test Conditions		
			Min.	Max.	Min.	Max.	Min.	Max.				
BV_{GSS}	Gate-Source Breakdown Voltage		-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$		
I_{DGO}	Drain Reverse Current			200		200		200	pA	$V_{GD} = -20\ V$, $I_S = 0$		25 C
	(Not JANTX Specified)			400		400		400	nA			150 C
I_{GSS}	Gate Reverse Current			-100		-100		-100	pA	$V_{GS} = -20\ V$, $V_{DS} = 0$		25 C
	(JANTX, ITE devices only)			-200		-200		-200	nA			150 C
$I_{D(OFF)}$	Drain Cutoff Current	JANTX Only						100	pA	$V_{DS} = 20\ V$	$V_{GS} = -6\ V$	25 C
								200	nA			150 C
						100			pA		$V_{GS} = -8\ V$	25 C
						200			nA			150 C
				100					pA		$V_{GS} = -12\ V$	25 C
				200					nA			150 C
								200	pA		$V_{GS} = -6\ V$	25 C
								400	nA			150 C
						200			pA		$V_{GS} = -8\ V$	25 C
						400			nA			150 C
				200					pA		$V_{GS} = -12\ V$	25 C
				400					nA			150 C
V_P	Gate-Source Pinch-Off Voltage		-5	-10	-2	-7	-1	-5	V	$V_{DS} = 20\ V$, $I_D = 1\ nA$		
I_{DSS}	Drain Current at Zero Gate Voltage		30		15		8		mA	$V_{DS} = 20\ V$, $V_{GS} = 0$, Pulse-Test Duration = 2 ms		
$V_{DS(ON)}$	Drain-Source ON Voltage							0.2	V	$V_{GS} = 0$	$I_D = 2.5\ mA$	
						0.2					$I_D = 4\ mA$	
				0.2							$I_D = 6.6\ mA$	
$r_{DS(ON)}$	Static Drain-Source ON Resistance			30		50		80	Ω	$V_{GS} = 0$, $I_D = 1\ mA$		
$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance			30		50		80	Ω	$V_{GS} = 0$, $I_D = 0$, $f = 1\ kHz$		
C_{iss}	Common-Source Input Capacitance			16		16		16	pF	$V_{DS} = 20\ V$, $V_{GS} = 0$, $f = 1\ MHz$		
C_{rss}		JANTX Only		5		5		5	pF	$V_{DS} = 20\ V$, $V_{GS} = 0$, $f = 1\ MHz$		
	Common-Source Reverse Transfer Capacitance			5		5		5	pF	$V_{DS} = 0$, $V_{GS} = -20\ V$, $f = 1\ MHz$		

INTERSIL

2N4117-19, 2N4117A-19A
N-Channel JFET

FEATURES

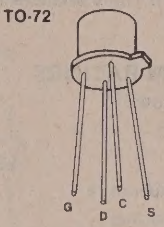
- Low Leakage – $I_{GSS} < 1$ pA
- Low Capacitance – $C_{rss} < 1.5$ pF

ABSOLUTE MAXIMUM RATINGS

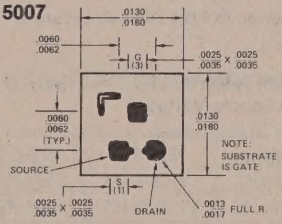
@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	300°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−40 V
V_{GD} Gate to Drain Voltage	−40 V
I_G Gate Current	50 mA

PIN CONFIGURATION



CHIP TOPOGRAPHY



ORDERING INFORMATION

TO-72	WAFER	CHIP
2N4117	2N4117/W	2N4117/D
2N4117A	2N4117A/W	2N4117A/D
2N4118	2N4118/W	2N4118/D
2N4118A	2N4118A/W	2N4118A/D
2N4119	2N4119/W	2N4119/D
2N4119A	2N4119A/W	2N4119A/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4117 2N4117A		2N4118 2N4118A		2N4119 2N4119A		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$
I_{GSS}	Gate Reverse Current		−10		−10		−10	pA	$V_{GS} = -20$ V, $V_{DS} = 0$
I_{GSS} (+100°C)	Gate Reverse Current		−25		−25		−25	nA	$V_{GS} = -20$ V, $V_{DS} = 0$
V_{GS} (off)	Gate-Source Pinch-Off Voltage	−0.6	−1.8	−1	−3	−2	−6	V	$V_{DS} = 10$ V, $I_D = 1$ nA
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	0.02	0.09	0.08	0.24	0.20	0.60	mA	$V_{DS} = 10$ V $V_{GS} = 0$
g_{fs}	Common-Source Forward Transconductance (Note 1)	70	210	80	250	100	330	μmho	$V_{DS} = 10$ V f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	60		70		90		μmho	$V_{GS} = 0$, f = 30 MHz
g_{os}	Common-Source Output Conductance		3		5		10	μmho	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz
C_{iss}	Common-Source Input Capacitance		3		3		3	pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5	pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz

NOTE: 1. Pulse test: Pulse duration of 2 ms used during test.

2N4220-2N4222
N-Channel JFET

FEATURES

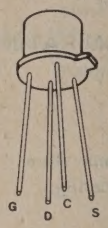
- $C_{rss} < 2$ pF
- Moderately High Forward Transconductance

ABSOLUTE MAXIMUM RATINGS
@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−30 V
V_{GD} Gate to Drain Voltage	−30 V
I_G Gate Current	10 mA

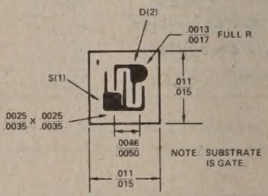
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5010



ORDERING INFORMATION

TO-72	WAFER	DICE
2N4220	2N4220/W	2N4220/D
2N4221	2N4221/W	2N4221/D
2N4222	2N4222/W	2N4222/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4220		2N4221		2N4222		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		−0.1		−0.1		−0.1	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
			−0.1		−0.1		−0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		−30		V	$I_G = -10$ μA, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4		−6		−8		$V_{DS} = 15$ V, $I_D = 0.1$ nA	
V_{GS}	Gate-Source Voltage	−0.5	−2.5	−1	−5	−2	−6	V	$V_{DS} = 15$ V, $I_D = (\ )$	
		(50)	(50)	(200)	(200)	(500)	(500)	(μA)		
I_{DSS}	Saturation Drain Current (Note 3)	0.5	3	2	6	5	15	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
g_{fs}	Common-Source Forward Transconductance (Note 3)	1000	4000	2000	5000	2500	6000	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
$\|y_{fs}\|$	Common-Source Forward Transadmittance	750		750		750				f = 100 MHz
g_{os}	Common-Source Output Conductance (Note 3)		10		20		40			f = 1 kHz
C_{iss}	Common-Source Input Capacitance		6		6		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2			

INTERSIL

2N4223, 2N4224
N-Channel JFET

FEATURES

- NF = 3 dB Typical at 200 MHz
- $C_{rss} < 2$ pF

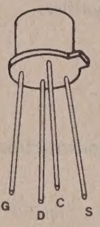
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	−30 V
Gate Current	10 mA
Drain Current	20 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature	300 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

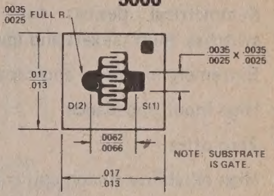
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5000



ORDERING INFORMATION

TO-72	WAFER	DICE
2N4223	2N4223/W	2N4223/D
2N4224	2N4224/W	2N4224/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4223		2N4224		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		−0.25		−0.5	nA	$V_{GS} = -20$ V, $V_{DS} = 0$	
			−0.25		−0.5	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		V	$I_G = -10\ \mu A$, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.1	−8	−0.1	−8	V	$V_{DS} = 15$ V, $I_D = (\ )$	
		(0.25)	(0.25)	(0.5)	(0.5)	(nA)		
V_{GS}	Gate-Source Voltage	−1.0	−7.0	−1.0	−7.5	V		
		(0.3)	(0.3)	(0.2)	(0.2)	(mA)		
I_{DSS}	Saturation Drain Current	3	18	2	20	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
g_{fs}	Common-Source Forward Transconductance	3000	7000	2000	7500	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
C_{iss}	Common-Source Input Capacitance (Output Shorted)		6		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2		2			
$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	2700		1700		μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 200 MHz
g_{iss}	Common-Source Input Conductance (Output Shorted)		800		800			
g_{oss}	Common-Source Output Conductance (Input Shorted)		200		200			
G_{ps}	Small Signal Power Gain	10				dB		
NF	Noise Figure		5				$V_{DS} = 15$ V, $V_{GS} = 0$, $R_{gen} = 1$ K	

INTERSIL

2N4338-2N4341
N-Channel JFET

FEATURES

- Exceptionally high figure of merit
- Radiation Immunity
- Symmetrical devices for low-level choppers, data switches, multiplexers and low noise amplifiers
- Extremely low noise and capacitance
- High input impedance
- Zero offset
- High reliability silicon epitaxial planar construction

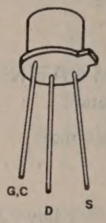
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−50 V
V_{GD} Gate to Drain Voltage	−50 V
I_G Gate Current	50 mA

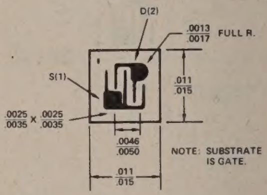
PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

5010



NOTE: SUBSTRATE IS GATE.

ORDERING INFORMATION

TO-18	WAFER	DICE
2N4338	2N4338/W	2N4338/D
2N4339	2N4339/W	2N4339/D
2N4340	2N4340/W	2N4340/D
2N4341	2N4341/W	2N4341/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

PARAMETER		2N4338		2N4339		2N4340		2N4341		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		−0.1		−0.1		−0.1		−0.1	nA	V_{GS} = −30 V, V_{DS} = 0	
			−0.1		−0.1		−0.1		−0.1	µA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		V	I_G = −1 µA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.3	−1	−0.6	−1.8	−1	−3	−2	−6		V_{DS} = 15 V, I_D = 0.1 µA	
$I_{D(off)}$	Drain Cutoff Current		0.05 (−5)		0.05 (−5)		0.05 (−5)		0.07 (−10)	nA (V)	V_{DS} = 15 V V_{GS} = ( )	
I_{DSS}	Saturation Drain Current	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	600	1800	800	2400	1300	3000	2000	4000	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		5		15		30		60			
r_{ds}	Drain-Source ON Resistance		2500		1700		1500		800	ohm	V_{DS} = 0, V_{GS} = 0	
C_{iss}	Common-Source Input Capacitance		7		7		7		7	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3		3			
NF	Noise Figure		1		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0 R_{gen} = 1 meg, BW = 200 Hz	f = 1 kHz

2N4351
N-Channel Enhancement Mode MOS FET

FEATURES

- Low ON-Resistance — 50Ω
- Low Capacitance — 1.7 pF
- High Gain — 3,000 μmhos
- High Gate Breakdown Voltage — ±125 V
- Low Threshold Voltage — 3 V

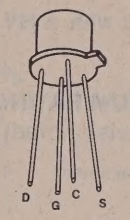
ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Operating Junction Temperature	−55°C to +150°C
Maximum Power Dissipation	
Total Dissipation at 25°C Ambient Temp	375 mW
Linear Derating Factor at 25°C Ambient Temp.	3 mW/°C
Maximum Voltages and Current	
V_{DSS} Drain to Source and Body Voltage	25 V
V_{GSS} Transient Gate to Source Voltage	±125 V
$I_{D(on)}$ Drain Current	100 mA

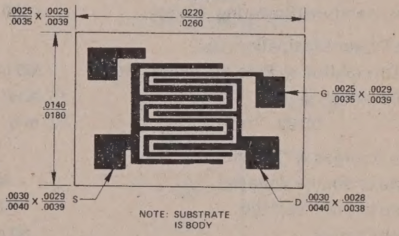
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

1003

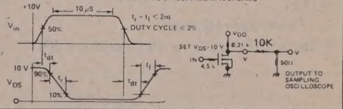

.0025/.0035 X .0029/.0039
.0220/.0260
.0140/.0180
G .0025/.0035 X .0029/.0039
.0030/.0040 X .0029/.0039 S
D .0030/.0040 X .0028/.0038
NOTE: SUBSTRATE IS BODY

ORDERING INFORMATION

TO-72	WAFER	DICE
2N4351	2N4351/W	2N4351/D

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Substrate connected to source.

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
OFF CHARACTERISTICS					
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	25		V	$I_D = 10\ \mu A$, $V_{GS} = 0$
I_{GSS}	Gate Leakage Current		10	pA	$V_{GS} = \pm 30$ V, $V_{DS} = 0$
I_{DSS}	Zero-Gate-Voltage Drain Current		10	nA	$V_{DS} = 10$ V, $V_{GS} = 0$
ON CHARACTERISTICS					
$V_{GS(TH)}$	Gate-Source Threshold Voltage	1.0	5	V	$V_{DS} = 10$ V, $I_D = 10\ \mu A$
$I_{D(on)}$	"ON" Drain Current	3		mA	$V_{GS} = 10$ V, $V_{DS} = 10$ V
$V_{DS(on)}$	Drain-Source "ON" Voltage		1.0	V	$I_D = 2$ mA, $V_{GS} = 10$ V
SMALL SIGNAL CHARACTERISTICS					
$r_{ds(on)}$	Drain-Source Resistance		300	ohms	$V_{GS} = 10$ V, $I_D = 0$, f = 1 kHz
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	1000		μmho	$V_{DS} = 10$ V, $I_D = 2$ mA, f = 1 kHz
C_{rss}	Reverse Transfer Capacitance		1.3	pF	$V_{DS} = 0$, $V_{GS} = 0$, f = 140 kHz
C_{iss}	Input Capacitance		5.0	pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 140 kHz
$C_{d(sub)}$	Drain-Substrate Capacitance		5.0	pF	$V_{D(SUB)} = 10$ V, f = 140 kHz
SWITCHING CHARACTERISTICS					
$t_{d(on)}$	Turn-On Delay		45	ns	FIGURE 1 – SWITCHING CIRCUIT and WAVEFORMS  +10V 10 μS $t_r - t_f$ < 2ns DUTY CYCLE < 2% V_{in} 50% t_{dt} 10 V 90% t_r t_f V_{DS} 10% V_{DD} SET V_{DS} = 10 V 8.21 k 10K IN 4.5 k V 50Ω OUTPUT TO SAMPLING OSCILLOSCOPE
t_r	Rise Time		65	ns	
$t_{d(off)}$	Turn-Off Delay		60	ns	
t_f	Fall Time		100	ns	

INTERSIL

ITE4391-ITE4393
2N4391-2N4393
N-Channel JFET

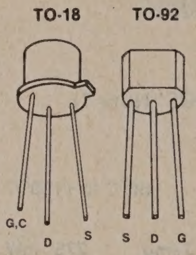
FEATURES

- $r_{ds(on)} < 30$ ohms (2N4391)
- $I_{D(off)} < 100$ pA
- Switches ±10 VAC with ±15V Supplies (2N4392, 2N4393)

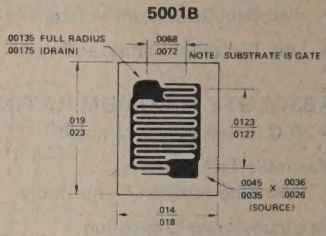
ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

@ 25°C (unless otherwise noted)	
Maximum Temperatures	
Storage Temperatures	−65°C to +200°C
Operating Junction Temperature TO 18	+200°C
TO 92	+125°
Lead Temperature (Soldering, 10 sec)	+300°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO 18	1.7 mW/°C
TO 92	3.0 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−40 V
V_{GD} Gate to Drain Voltage	−40 V
I_G Gate Current	50 mA

PIN CONFIGURATIONS



CHIP TOPOGRAPHY



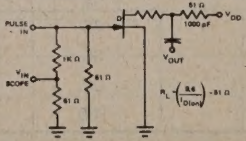
ORDERING INFORMATION

TO-92	TO-18	WAFER	DICE
ITE 4391	2N4391	2N4391/W	2N4391/D
ITE 4392	2N4392	2N4392/W	2N4392/D
ITE 4393	2N4393	2N4393/W	2N4393/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC		4391		4392		4393		UNIT	TEST CONDITIONS		
		MIN	MAX	MIN	MAX	MIN	MAX				
I_{GSS}	Gate Reverse Current		−100		−100		−100	pA	$V_{GS} = -20$ V, $V_{DS} = 0$		
			−200		−200		−200	nA			150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	$I_G = 1$ µA, $V_{DS} = 0$		
$I_{D(off)}$	Drain Cutoff Current						100	pA	$V_{DS} = 20$ V	$V_{GS} = -5$ V	
							200	nA			150°C
					100			pA		$V_{GS} = -7$ V	
					200			nA			150°C
			100					pA		$V_{GS} = -12$ V	
			200					nA			150°C
$V_{GS(f)}$	Gate-Source Forward Voltage		1		1		1	V	$I_G = 1$ mA, $V_{DS} = 0$		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−2	−5	−0.5	−3		$V_{DS} = 20$ V, $I_D = 1$ nA		
I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	$V_{DS} = 20$ V, $V_{GS} = 0$		
$V_{DS(on)}$	Drain Source ON Voltage						0.4	V	$V_{GS} = 0$	$I_D = 3$ mA	
					0.4					$I_D = 6$ mA	
			0.4							$I_D = 12$ mA	
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 1$ mA		
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz
C_{iss}	Common-Source Input Capacitance		14		14		14	pF	$V_{DS} = 20$ V, $V_{GS} = 0$		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance						3.5		$V_{DS} = 0$	$V_{GS} = -5$ V	
					3.5					$V_{GS} = -7$ V	
			3.5							$V_{GS} = -12$ V	
t_d	Turn-ON Delay Time		15		15		15	ns	$V_{DD} = 10$ V, $V_{GS(on)} = 0$		
t_r	Rise Time		5		5		5			$I_{D(on)}$	$V_{GS(off)}$
t_{off}	Turn-OFF Delay Time		20		35		50		4391	12 mA	−12 V
t_f	Fall Time		15		20		30		4392 4393	6 3	−7 −5

NOTE:
1. Pulse test required, pulse width = 300 µs, duty cycle ⩽ 3%



INPUT PULSE	SAMPLING SCOPE
RISE TIME < 0.5 ns	RISE TIME 0.4 ns
FALL TIME < 0.5 ns	INPUT RESISTANCE 50 Ω
PULSE DUTY CYCLE 1%	

ITE4416, 2N4416/A
N-Channel JFET

FEATURES

- Silicon Planar Epitaxial Construction
- Low Noise - NF = 2.0 dB max. @ 100 MHz
  NF = 4.0 dB max. @ 400 MHz
- Low Feedback Capacitancef- C_{rss} = 0.8 pF max.
- Low Output Capacitance - C_{oss} = 2.0 pF max.
- High Transconductance - g_{fs} = 4000 μmho min.
- High Power Gain - G_{ps} = 18 dB min. @ 100 MHz
  G_{ps} = 10 dB min. @ 400 MHz

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO72	−65°C to +200°C
TO92	−55°C to 125°C
Operating Junction Temperature TO72	+200°C
TO92	+125°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

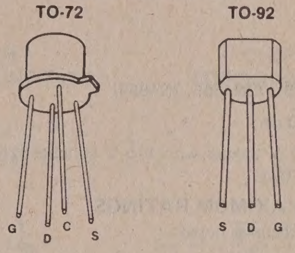
Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO 72	1.7 mW/°C
TO 92	3.0 mW/°C

Maximum Voltages & Current

	2N4416 (ITE 4116)	2N4416A
V_{GS} Gate to Source Voltage	−30V	−35V
V_{GD} Drain to Drain Voltage	−30 V	−35V
I_G Gate Current	10 V	10 mA

PIN CONFIGURATIONS



CHIP TOPOGRAPHY

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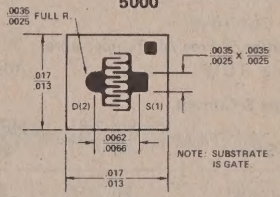


ORDERING INFORMATION

TO-92	TO-72	WAFER	DICE
ITE 4416	2N4416 2N4416A	2N4416/W 2N4416A/W	2N4416/D 2N4416A/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.1	nA	V_{GS} = −20 V, V_{DS} = 0	
			−0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−30		V	I_G = −1 μA, V_{DS} = 0	2N4416, ITE
		−35				2N4416A
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−6	V	V_{DS} = 15 V, I_D = 1 nA	2N4416, ITE
		−2.5	−6			2N4416A
I_{DSS}	Drain Current at Zero Gate Voltage	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		f = 1 kHz
g_{os}	Common-Source Output Conductance		50	μmho		
C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
C_{iss}	Common-Source Input Capacitance		4	pF		
C_{oss}	Common-Source Output Capacitance		2			

PARAMETER		100 MHz		400 MHz		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0
b_{iss}	Common-Source Input Susceptance		2500		10,000	μmho	
g_{oss}	Common-Source Output Conductance		75		100	μmho	
b_{oss}	Common-Source Output Susceptance		1000		4000	μmho	
g_{fs}	Common-Source Forward Transconductance			4000		μmho	
G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ

2N4856-2N4861
2N4856-2N4858 JAN, JTX, JTXV*
N-Channel JFET

FEATURES

- $r_{DS(ON)} < 25\Omega$ (2N4856, 2N4859)
- $I_{D(off)} < 250$ pA
- Switches ±10 V Signals with ±15 V Supplies (2N4858, 2N4861)

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO18	−65°C to +200°C
Operating Junction Temperature TO18	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation

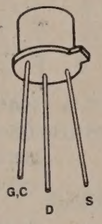
Device Dissipation @ Free Air Temperature	1.8w
Linear Derating TO18	10mW/°C

Maximum Voltages & Current

		2N4856-58	2N4859-61
V_{GS}	Gate to Source Voltage	−40 V	−30V
V_{GD}	Gate to Drain Voltage	−40 V	−30 V
I_G	Gate Current	50 mA	50 mA

PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

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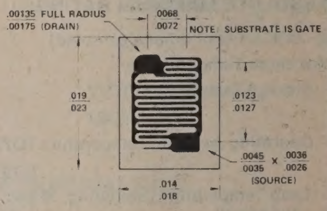


ORDERING INFORMATION

TO-18	WAFER	DICE
2B4856 *	2N4856/W	2N4856/D
2N4857 *	2N4857/W	2N4857/D
2N4858 *	2N4858/W	2N4858/D
2N4859	2N4859/W	2N4859/D
2N4860	2N4860/W	2N4860/D
2N4861	2N4861/W	2N4861/D

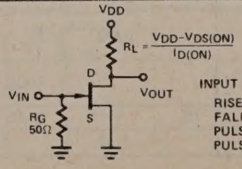
*add JAN, JTX, JTXV, to basic part number to specify these devices.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC			2N4856,59		2N4857,60		2N4858,61		UNIT	TEST CONDITIONS	
			MIN	MAX	MIN	MAX	MIN	MAX			
BV_{GSS}	Gate-Source Breakdown Voltage	2N4856-58	−40		−40		−40		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
		2N4859-61	−30		−30		−30				
I_{GSS}	Gate Reverse Current	2N4856-58		−250		−250		−250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
		2N4859-61		−500		−500		−500	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	150°C
$I_{D(off)}$	Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
				500		500		500	nA		150°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4	−10	−2	−6	−0.8	−4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
I_{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
$V_{DS(on)}$	Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\quad)$	
$r_{ds(on)}$	Drain-Source ON Resistance			25		40		60	ohm	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
C_{iss}	Common-Source Input Capacitance			18		18		18	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance			8		8		8			
t_d	Turn-ON Delay Time			6 (20) [−10]		6 (10) [−6]		10 (5) [−4]	ns (mA) [V]	$V_{DD} = 10$ V, $R_L =$ 464 Ω 2N4856,59 953 Ω 2N4857,60 1910 Ω 2N4858,61	
t_r	Rise Time			3 (20) [−10]		4 (10) [−6]		10 (5) [−4]	ns (mA) [V]	$V_{GS(on)} = 0$ $I_{D(on)} = (\ )$,	
t_{off}	Turn-OFF Time			25 (20) [−10]		50 (10) [−6]		100 (5) [−4]	ns (mA) [V]	$V_{GS(off)} = (\ )$	

NOTE:

1. Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pf

INTERSIL

2N4867/A-2N4869/A
N-Channel JFET

FEATURES

- Low Noise Voltage — $e_n \leq 5$ nV/√ Hz
- Low Leakage — $I_{GSS} \leq 0.25$ nA
- High Gain — $Y_{fs} \geq 1300 \leq 4000$ µmho

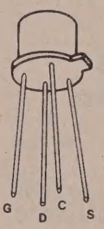
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−40 V
V_{GD} Gate to Drain Voltage	−40 V
I_G Gate Current	50 mA

PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

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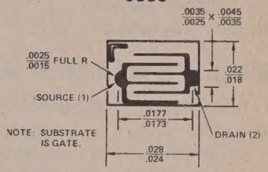


ORDERING INFORMATION

TO-72	WAFER	DICE
2N4867	2N4867/W	2N4867/D
2N4867A	2N4867A/W	2N4867A/D
2N4868	2N4868/W	2N4868/D
2N4868A	2N4868A/W	2N4868A/D
2N4869	2N4869/W	2N4869/D
2N4869A	2N4869A/W	2N4869A/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4867 2N4867A MIN	MAX	2N4868 2N4868A MIN	MAX	2N4869 2N4869A MIN	MAX	UNIT	TEST CONDITIONS		
I_{GSS}	Gate Reverse Current		−0.25		−0.25		−0.25	nA	V_{GS} = −30 V, V_{DS} = 0		
			−0.25		−0.25		−0.25	µA			150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	I_G = −1 µA, V_{DS} = 0		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.7	−2	−1	−3	−1.8	−5		V_{DS} = 20 V, I_D = 1 µA		
I_{DSS}	Saturation Drain Current (Note 1)	0.4	1.2	1	3	2.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0		
g_{fs}	Common-Source Forward Transconductance (Note 1)	700	2000	1000	3000	1300	4000	µmho	V_{DS} = 20 V, V_{GS} = 0		f = 1 kHz
g_{os}	Common-Source Output Conductance		1.5		4		10				
C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF			f = 1 MHz
C_{iss}	Common-Source Input Capacitance		25		25		25				
$\overline{e}_n$	Short Circuit Equivalent Input Noise Voltage		20		20		20	nV/√Hz	V_{DS} = 10 V, V_{GS} = 0	2N4867 Series	f = 10 Hz
			10		10		10			2N4867A Series	
			10		10		10			2N4867 Series	f = 1 kHz
			5		5		5			2N4867A Series	
NF	Spot Noise Figure		1		1		1	dB	V_{DS} = 10 V, V_{GS} = 0 R_{gen} = 20 K, 2N4867 Series 5 K, 2N4867A Series		f = 1 kHz

NOTE: 1. Pulse test duration 2 ms.

2N5018, 2N5019
P-Channel JFET

APPLICATIONS

- Analog Switches
- Commutators
- Choppers

FEATURES

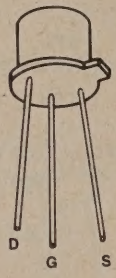
- Low Insertion Loss $r_{ds(on)} < 75\Omega$ (2N5018)
- No Offset or Error Voltages Generated by Closed Switch
- Purely Resistive

ABSOLUTE MAXIMUM RATINGS

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . . . 30 V
Gate Current . . . . 50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C) . . . . 500 mW
Storage Temperature Range . . . . −65 to +200°C
Lead Temperature (1/16″ from case for 60 seconds) . . . . 300°C

PIN CONFIGURATION

TO-18



CHIP TOPOGRAPHY

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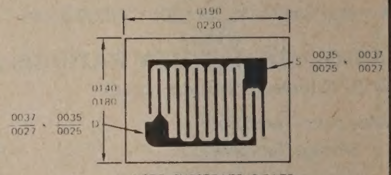


NOTE SUBSTRATE IS GATE

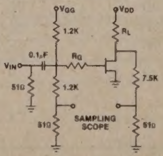
ORDERING INFORMATION

TO-18	WAFER	DICE
2N5018	2N5018/W	2N5018/D
2N5019	2N5019/W	2N5019/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic		2N5018 Min	2N5018 Max	2N5019 Min	2N5019 Max	Unit	Test Conditions	
STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
	I_{GSS}	Gate Reverse Current		2		2	nA	$V_{GS} = 15\ V$, $V_{DS} = 0$	
	$I_{D(off)}$	Drain Cutoff Current		−10		−10		$V_{DS} = -15\ V$, $V_{GS} = 12\ V$ (2N5018)	
				−10		−10	μA	$V_{GS} = 7\ V$ (2N5019)	150°C
	I_{DGO}	Drain Reverse Current		−2		−2	nA	$V_{DG} = -15\ V$, $I_S = 0$	
				−3		−3	μA		150°C
	$B_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	$V_{DS} = -15\ V$, $I_D = -1\ \mu A$	
	I_{DSS}	Saturation Drain Current	−10		−5		mA	$V_{DS} = -20\ V$, $V_{GS} = 0$	
	$V_{DS(on)}$	Drain-Source ON Voltage		−0.5		−0.5	V	$V_{GS} = 0$, $I_D = -6\ mA$ (2N5018), $I_D = -3\ mA$ (2N5019)	
DYNAMIC	$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	$I_D = -1\ mA$, $V_{GS} = 0$	
	$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	$I_D = 0$, $V_{GS} = 0$	f = 1 kHz
	C_{iss}	Common-Source Input Capacitance		45		45	pF	$VV_{DS} = -15\ V$, $V_{GS} = 0$	f = 1 MHz
	C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		$V_{DS} = 0$, $V_{GS} = 12\ V$ (2N5018), $V_{GS} = 7\ V$ (2N5019)	
	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	$V_{DD} = -6\ V$, $V_{GS(on)} = 0$	
	t_r	Rise Time		20		75			
	$t_{d(off)}$	Turn-Off Delay Time		15		25		$V_{GS(off)}$ $I_{D(on)}$ R_L 2N5018 12 V −6 mA 910Ω	
	t_f	Fall Time		50		100		2N5019 7V −3 mA 1.8K Ω	

NOTE 1: Due to symmetrical geometry these units may be operated with source and drain leads interchanged.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 100 ns
REPLETION RATE 1 MHz

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 MΩ
INPUT CAPACITANCE 1.5 pF

2N5114-2N5116 JAN, JTX
P-Channel JFET

FEATURES

- ON Resistance < 75 ohms (2N5114)
- $I_{D(off)} < 500$ pA
- Switches directly from T^2L Logic (2N5116)

GENERAL DESCRIPTION

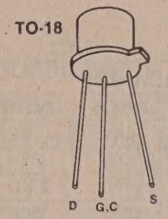
Ideal for inverting switching or "Virtual Gnd" switching into inverting input of Op. Amp. No driver is required and ±10 VAC signals can be handled using only +5V logic (T^2L or CMOS).

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

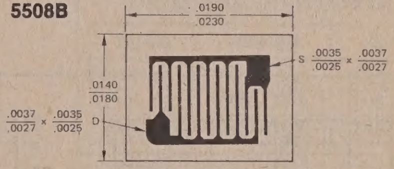
Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	500 mW
Linear Derating	3.0 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	30 V
V_{GD} Gate to Drain Voltage	30 V
I_G Gate Current	50 mA

PIN CONFIGURATION



CHIP TOPOGRAPHY

5508B



NOTE: SUBSTRATE IS GATE

ORDERING INFORMATION

TO18*	WAFER	DICE
2N5114	2N5114/W	2N5114/D
2N5115	2N5115/W	2N5115/D
2N5116	2N5116/W	2N5116/D

*add JAN, JTX to basic part number to specify these devices (To 18 package only)

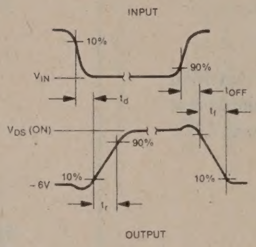
ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

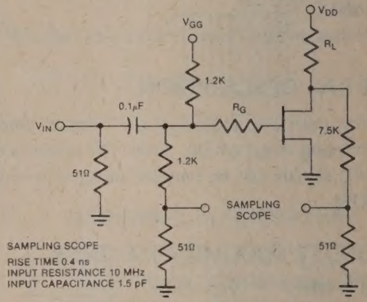
CHARACTERISTIC		2N5114		2N5115		2N5116		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
I_{GSS}	Gate Reverse Current		500		500		500	pA	$V_{GS} = 20$ V, $V_{DS} = 0$	25°C
			1.0		1.0		1.0	μA		150°C
$I_{D(OFF)}$	Drain Cutoff Current		−500		−500		−500	pA	$V_{DS} = -15$ V, V_{GS} = 2N5114 = 12 V 2N5115 = 7 V 2N5116 = 5 V	25°C
			−1.0		−1.0		−1.0	μA		150°C
V_P	Gate-Source Pinch-Off Voltage	5	10	3	6	1	4	V	$V_{DS} = -15$ V, $I_D = -1$ nA	
I_{DSS}	Drain Current at Zero Gate Voltage	−30	−90	−15	−60	−5	−25	mA	$V_{GS} = 0$, V_{DS} 2N5114 = −18 V = 2N5115 = −15 V 2N5116 = −15 V	
V_{GSSF}	Forward Gate-Source Voltage		−1		−1		−1	V	Pulse Test Duration = 2 ms $I_G = -1$ mA, $V_{DS} = 0$	
$V_{DS(ON)}$	Drain-Source ON Voltage		−1.3		−0.8		−0.6	V	$V_{GS} = 0$, I_D 2N5114 = −15 mA = 2N5115 = − 7 mA 2N5116 = − 3 mA	
$r_{DS(on)}$	Static Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0$, $I_D = -1$ mA	
$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0$, $I_D = 0$, f = 1 kHz	
	Jan TX only		75		100		175	Ω		
C_{iss}	Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = -15$ V, $V_{GS} = 0$, f = 1 MHz	
	Jan TX only		25		25		27	pF		
C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7	pF	$V_{DS} = 0$, V_{GS} 2N5114 = 12 V = 2N5115 = 7 V 2N5116 = 5 V f = 1 MHz	

SWITCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

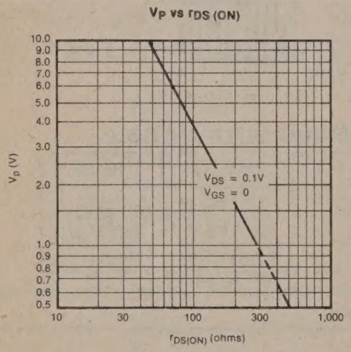
CHARACTERISTIC	2N5114	2N5115	2N5116	JAN TX 2N5114	JAN TX 2N55115	JAN TX 2N5116	UNIT
	MAX	MAX	MAX	MAX	MAX	MAX	
t_d Turn-ON Delay Time	6	10	12	6	10	25	ns
t_r Rise Time	10	20	30	10	20	35	ns
t_{off} Turn-OFF Delay Time	6	8	19	6	8	29	ns
t_f Fall Time	15	30	50	(not JAN TX specified)			ns

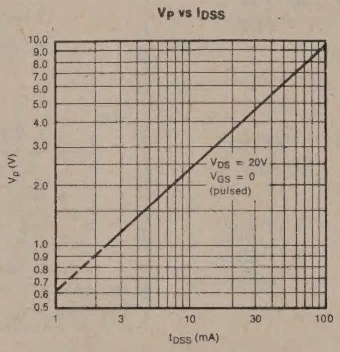
TEST CONDITIONS	2N5114	2N5115	2N5116
V_{DD}	−10V	−6V	−6V
V_{GG}	20V	12V	8V
R_L	430Ω	910Ω	2 KΩ
R_G	100Ω	220Ω	390Ω
$I_{D(ON)}$	−15mA	−7mA	−3mA
V_{IN}	−12V	−7V	−5V

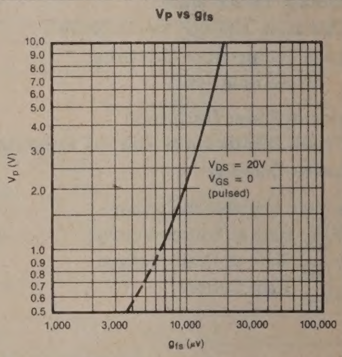

INPUT
10%
90%
V_IN
t_d
t_OFF
t_f
V_DS (ON)
90%
10%
−6V
10%
t_r
OUTPUT


V_DD
V_GG
R_L
1.2K
0.1µF
R_G
V_IN
7.5K
51Ω
1.2K
SAMPLING SCOPE
51Ω
51Ω

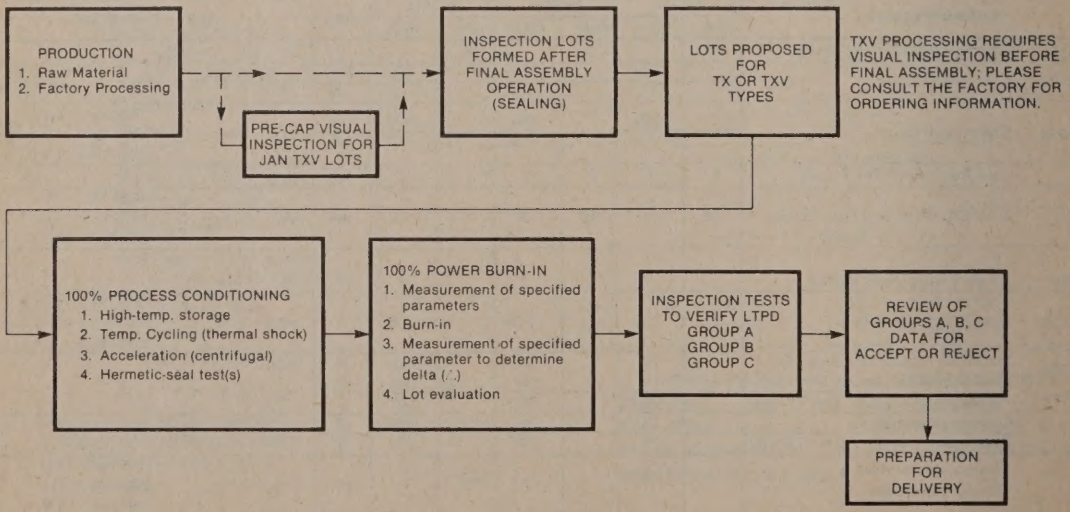
SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 MHz
INPUT CAPACITANCE 1.5 pF


V_P vs $r_{DS\,(ON)}$


V_P vs I_{DSS}


V_P vs g_{fs}

JAN TX and JAN TX V Processing


PRODUCTION
1. Raw Material
2. Factory Processing
PRE-CAP VISUAL INSPECTION FOR JAN TXV LOTS
INSPECTION LOTS FORMED AFTER FINAL ASSEMBLY OPERATION (SEALING)
LOTS PROPOSED FOR TX OR TXV TYPES
100% PROCESS CONDITIONING
1. High-temp. storage
2. Temp. Cycling (thermal shock)
3. Acceleration (centrifugal)
4. Hermetic-seal test(s)
100% POWER BURN-IN
1. Measurement of specified parameters
2. Burn-in
3. Measurement of specified parameter to determine delta (∆)
4. Lot evaluation
INSPECTION TESTS TO VERIFY LTPD GROUP A GROUP B GROUP C
REVIEW OF GROUPS A, B, C DATA FOR ACCEPT OR REJECT
PREPARATION FOR DELIVERY

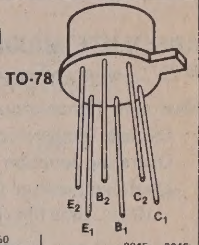
TXV PROCESSING REQUIRES VISUAL INSPECTION BEFORE FINAL ASSEMBLY; PLEASE CONSULT THE FACTORY FOR ORDERING INFORMATION.

2N5117-2N5119
Dual Monolithic PNP Transistor

ABSOLUTE MAXIMUM RATINGS (25°C unless otherwise noted) (Note 1)

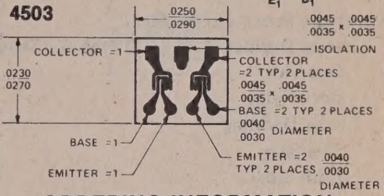
Dissipation at 25°C Case Temperature	
Each side (Note 1)	0.4W
Both sides	0.75W
Derating Factor	
Each side	2.3mW/°C
Both sides	4.3mW/°C
Voltage	
Collector to Base	45V
Collector to Emitter	45V
Emitter to Base (Note 2)	7.0V
Collector to Collector	100V
Collector Current	10mA
Storage Temperature	−65 to +200°C
Lead Temperature for 10 Seconds	+300°C

PIN CONFIGURATION



CHIP TOPOGRAPHY

4503



ORDERING INFORMATION

TO-78	WAFER	DICE
2N5117	2N5117/W	2N5117/D
2N5118	2N5118/W	2N5118/D
2N5119	2N5119/W	2N5119/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117 2N5118		2N5119		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	100	300	50			$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$
h_{FE}	DC Current Gain	100		50			$I_C = 500\ \mu A$, $V_{CE} = 5.0\ V$
h_{FE}	DC Current Gain (−55°C)	30		20			$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$
I_{CBO}	Collector Cutoff Current		0.1		0.1	nA	$I_E = 0$, $V_{CB} = 30\ V$
I_{CBO}	Collector Cutoff Current (150°C)		0.1		0.1	μA	$I_E = 0$, $V_{CB} = 30\ V$
I_{EBO}	Emitter Cutoff Current		0.1		0.1	nA	$I_C = 0$, $V_{EB} = 5.0\ V$
$I_{C_1-C_2}$	Collector-Collector Leakage		5.0		5.0	pA	$V_{CC} = 100\ V$
GBW	Current Gain Bandwith Product	100		100		MHz	$I_C = 500\ \mu A$, $V_{CE} = 10\ V$
C_{ob}	Output Capacitance		0.8		0.8	pF	$I_E = 0$, $V_{CB} = 5.0\ V$
C_{te}	Emitter Transition Capacitance		1.0		1.0	pF	$I_C = 0$, $V_{EB} = 0.5\ V$
$C_{C_1\text{-}C_2}$	Collector-Collector Capacitance		0.8		0.8	pF	$V_{CC} = 0$
$V_{CEO(sust)}$	Collector-Emitter Sustaining Voltage	45		45		V	$I_C = 1.0\ mA$, $I_B = 0$
NF	Narrow Band Noise Figure		4.0		4.0	dB	$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$ BW = 200 Hz f = 1 KHz, $R_G = 10\ K\Omega$
$V_{(BR)CBO}$	Collector Base Breakdown Voltage	45		45		V	$I_C = 10\ \mu A$, $I_E = 0$
$V_{(BR)EBO}$	Emitter Base Breakdown Voltage	7.0		7.0		V	$I_E = 10\ \mu A$, $I_C = 0$

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117		2N5118		2N5119		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	0.9	1.0						$I_C = 10\ \mu A$ to $500\ \mu A$, $V_{CE} = 5\ V$
				0.85	1.0	0.8	1.0		$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$
$V_{BE_1}-V_{BE_2}$	Base-Emitter Voltage Differential		3.0					mV	$I_C = 10\ \mu A$ to $500\ \mu A$, $V_{CE} = 5\ V$
					5.0		5.0		$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$
$I_{B_1}-I_{B_2}$	Base Current Differential		10.0		15		40	nA	$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$
$\Delta(V_{BE_1}-V_{BE_2})$	Base Voltage Differential Change with Temperature		3.0		5.0		10	μV/°C	$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$ $T_A = -55°C$ to $+125°C$
$\Delta(I_{B_1}-I_{B_2})$	Base-Current Differential Change with Temperature		0.3		0.5		1.0	nA/°C	$I_C = 10\ \mu A$, $V_{CE} = 5.0\ V$ $T_A = -55°C$ to $+125°C$

1. Maximum ratings are limiting values above which devices may be damaged. These ratings give a maximum junction temperature of 200 C.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μA.
3. Lower of two h_{FE} readings is defined as h_{FE_1}.

INTERSIL

2N5196-2N5199
Monolithic Dual N-Channel JFET

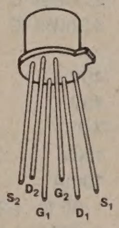
ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	2.56 mW/°C
Both Sides	4.3 mW/°C
Maximum Voltages & Currents	
V_{GS} Gate to Source Voltage	−50 V
V_{GD} Gate to Drain Voltage	−50 V
I_G Gate Current	50 mA

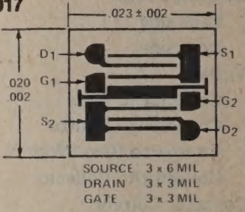
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6017



ORDERING INFORMATION

TO-71	WAFER	DICE
2N5196	2N5196/W	2N5196/D
2N5197	2N5197/W	2N5197/D
2N5198	2N5198/W	2N5198/D
2N5199	2N5199/W	2N5199/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−25	pA	V_{GS} = −30 V, V_{DS} = 0	
			−50	nA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−50		V	I_G = −1 µA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.7	−4		V_{DS} = 20 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	−0.2	−3.8		V_{DG} = 20 V, I_D = 200 µA	
I_G	Gate Operating Current		−15	pA		
			−15	nA		125°C
I_{DSS}	Saturation Drain Current (Note 1)	0.7	7	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance (Note 1)	700	1500		V_{DG} = 20 V, I_D = 200 µA	
g_{os}	Common-Source Output Conductance		50		V_{DS} = 20 V, V_{GS} = 0	
g_{os}	Common-Source Output Conductance		4		V_{DG} = 20 V, I_D = 200 µA	
C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2			
NF	Spot Noise Figure		0.5	dB		f = 100 Hz, R_G = 10 MΩ
$\overline{e}_n$	Equivalent Input Noise Voltage		0.020 20	$\frac{\mu}{\sqrt{Hz}}$		f = 1 kHz

PARAMETER		2N5196		2N5197		2N5198		2N5199		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5		5	nA	V_{DG} = 20 V, I_D = 200 µA	125°C
I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	—	V_{DS} = 20 V, V_{GS} = 0 V	
g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	—	V_{DG} = 20 V, I_D = 200 µA	f = 1 kHz
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		5		10		20		40	µV/°C		T_A = 25°C T_B = 125°C
			5		10		20		40			T_A = −55°C T_B = 25°C
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		1		1		1	µmho		f = 1 kHz

NOTE: 1. Pulse test required, pulsewidth = 300 µs, duty cycle ≤ 3%.
2. Measured at end points, T_A and T_B.

2N5397, 2N5398
N-Channel JFET

FEATURES

- G_{ps} = 10 dB Typical (Common Gate) at 450 MHz
- NF = 3.5 dB Typical at 450 MHz
- C_{rss} = 1 pF Typical

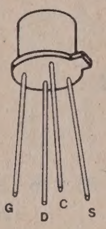
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	300°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−25 V
V_{GD} Gate to Drain Voltage	−25 V
I_G Gate Current	10 mA

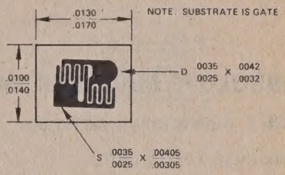
PIN CONFIGURATION

TO-72



CHIP TOPOGRAPHY

5011



ORDERING INFORMATION

TO-72	WAFER	DICE
2N5397	2N5397/W	2N5397/D
2N5398	2N5398/W	2N5398/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5397 MIN	2N5397 MAX	2N5398 MIN	2N5398 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.1		−0.1	nA	V_{GS} = −15 V, V_{DS} = 0	
			−0.1		−0.1	µA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−25		−25		V	V_{DS} = 0, I_G = −1 µA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1.0	−6.0	−1.0	−6.0		V_{DS} = 10 V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current	10	30	5	40	mA	V_{DS} = 10 V, V_{DS} = 0	
$V_{GS(f)}$	Gate-Source Forward Voltage		1		1	V	V_{DS} = 0, I_G = 1 mA	
g_{fs}	Common-Source Forward Transconductance (Note 1)	6000	10,000			µmho	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
				5500	10,000		V_{DS} = 10 V, V_{GS} = 0	
g_{oss}	Common-Source Output Conductance		200				V_{DS} = 10 V, I_D = 10 mA	
					400		V_{DS} = 10 V, V_{GS} = 0	
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			pF	V_{DS} = 10 V, I_D = 10 mA	f = 1 MHz
					1.3		V_{DS} = 10 V, V_{GS} = 0	
C_{iss}	Common-Source Input Capacitance		5.0				V_{DG} = 10 V, I_D = 10 mA	
					5.5		V_{DS} = 10 V, V_{GS} = 0	
g_{iss}	Common-Source Input Conductance		2000			µmho	V_{DG} = 10 V, I_D = 10 mA	f = 450 MHz
					3000		V_{DG} = 10 V, V_{GS} = 0	
g_{oss}	Common-Source Output Conductance		400				V_{DG} = 10 V, I_D = 10 mA	
					500		V_{DS} = 10 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	5500	9000				V_{DG} = 10 V, I_D = 10 mA	
				5000	10,000		V_{DS} = 10 V, V_{GS} = 0	
G_{ps}	Common-Source Power Gain (neutralized)	15				dB	V_{DG} = 10 V, I_D = 10 mA	
NF	Common-Source, Spot Noise Figure (neutralized)		3.5					

Note 1: Pulse test duration = 2ms

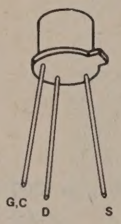
2N5432-2N5434
N-Channel JFET

FEATURES

- $r_{ds\,(on)} < 5$ ohms
- Excellent Switching — $t_{on} < 4$ ns
  $t_{off} < 6$ ns
- Low Cutoff Current — $I_{D(off)} < 200$ pA

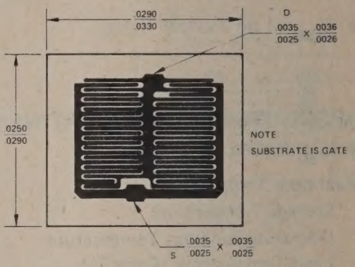
PIN CONFIGURATION

TO 52



CHIP TOPOGRAPHY

5018



ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	2.3 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−25 V
V_{GD} Gate to Drain Voltage	−25 V
I_G Gate Current	100 mA
I_D Drain Current	400 mA

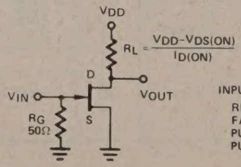
ORDERING INFORMATION

TO-52	WAFER	DICE
2N5432	2N5432/W	2N5432/D
2N5433	2N5433/W	2N5433/D
2N5434	2N5434/W	2N5434/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

	CHARACTERISTIC	2N5432		2N5433		2N5434		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		−200		−200		−200	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
			−200		−200		−200	nA		150°C
BV_{GSS}	Gate Source Breakdown Voltage	−25		−25		−25		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
			200		200		200	nA		150°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−3	−9	−1	−4	V	$V_{DS} = 5$ V, $I_D = 3$ nA	
I_{DSS}	Saturation Drain Current (Note 1)	150		100		30		mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	$V_{GS} = 0$, $I_D = 10$ mA	
$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV		
$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		30		30		30	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15			
t_d	Turn-ON Delay Time		4		4		4	ns	$V_{DD} = 1.5$ V, $V_{GS(on)} = 0$, $V_{GS(off)} = -12$ V, $I_{D(on)} = 10$ mA	
t_r	Rise Time		1		1		1			
t_{off}	Turn-OFF Delay Time		6		6		6			
t_f	Fall Time		30		30		30			

NOTE: 1. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

INTERSIL

2N5452-2N5454
Monolithic Dual N-Channel JFET

FEATURES

- Offset Voltage 5 mV
- Drift 5 μV/°C
- Low Capacitance
- Low Output Conductance — 1 μmho Max

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.

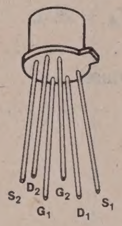
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	2.86 mW/°C
Both Sides	4.3 mW/°C
Maximum Voltages & Currents	
V_{GS} Gate to Source Voltage	−50 V
V_{GD} Gate to Drain Voltage	−50 V

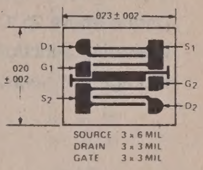
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6017



ORDERING INFORMATION

TO-71	WAFER	DICE
2N5452	2N5452/W	2N5452/D
2N5453	2N5453/W	2N5453/D
2N5454	2N5454/W	2N5454/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5452 MIN	2N5452 MAX	2N5453 MIN	2N5453 MAX	2N5454 MIN	2N5454 MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−100		−100		−100	pA	$V_{GS} = -30$ V, $V_{DS} = 0$	
			−200		−200		−200	nA		$T_A = 150°C$
BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		V	$V_{DS} = 0$, $I_G = -1\ \mu A$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1	−4.5	−1	−4.5	−1	−4.5		$V_{DS} = 20$ V, $I_D = 1$ nA	
V_{GS}	Gate-Source Voltage	−0.2	−4.2	−0.2	−4.2	−0.2	−4.2		$V_{DS} = 20$ V, $I_D = 50\ \mu A$	
$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2		$V_{DS} = 0$, $I_G = 1$ mA	
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 kHz
		1000		1000		1000				f = 100 MHz
g_{os}	Common-Source Output Conductance		3.0		3.0		3.0			f = 1 kHz
			1.0		1.0		1.0		$V_{DS} = 20$ V, $I_D = 200\ \mu A$	
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		$V_{DG} = 10$ V, $I_S = 0$	
$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 kHz
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	$V_{DS} = 20$ V, $V_{GS} = 0$ $R_G = 10\ M\Omega$	f = 100 Hz
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0		$V_{DS} = 20$ V, $V_{GS} = 0$	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	$V_{DS} = 20$ V, $I_D = 200\ \mu A$	
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0			T = 25°C to −55°C
			0.5		1.0		2.5			T = 25°C to +125°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.95	1.0			f = 1 kHz
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.25		0.25		0.25	μmhos		

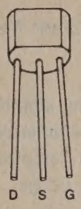
2N5457-2N5459
N-Channel JFET

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

V_{DS}	Drain-Source Voltage	25V
V_{DG}	Drain-Gate Voltage	25V
$V_{GS(r)}$	Reverse Gate-Source Voltage	25V
I_G	Gate Current	10mA
	Total Device Dissipation @ T_A = 25°C	310mW
P_D	Derate above 25°C	2.82mW/°C
T_J	Operating Junction Temperature	135°C
T_{stg}	Storage Temperature Range	−65 to +150°C

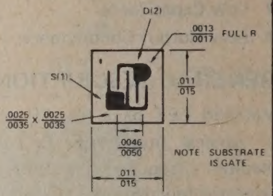
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5010



ORDERING INFORMATION

TO-92	WAFER	DICE
2N5457	2N5457/W	2N5457/D
2N5458	2N5458/W	2N5458/D
2N5459	2N5459/W	2N5459/D

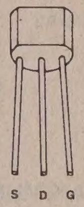
ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
OFF CHARACTERISTICS							
BV_{GSS}	Gate-Source Breakdown Voltage	-25	-60		V	I_G = −10 μA, V_{DS} = 0	
I_{GSS}	Gate Reverse Current		.05	−1.0 −200	nA	V_{GS} = −15 V, V_{DS} = 0 V_{GS} = −15 V, V_{DS} = 0, T_A = 100°C	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5 -1.0 -2.0		-6.0 -7.0 -8.0	V	V_{DS} = 15 V, I_D = 10 nA	2N5457 2N5458 2N5459
V_{GS}	Gate-Source Voltage		2.5 3.5 4.5		V	V_{DS} = 15 V, I_D = 100 μA V_{DS} = 15 V, I_D = 200 μA V_{DS} = 15 V, I_D = 400 μA	2N5457 2N5458 2N5459
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate-Voltage Drain Current	1.0 2.0 4.0	3.0 6.0 9.0	5.0 9.0 16	mA	V_{DS} = 15 V, V_{GS} = 0	2N5457 2N5458 2N5459
DYNAMIC CHARACTERISTICS							
$\lvert y_{fs}\rvert$	Forward Transfer Admittance	1000 1500 2000	3000 4000 4500	5000 5500 6000	μmho	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz	2N5457 2N5458 2N5459
$\lvert y_{os}\rvert$	Output Admittance		10	50	μmho	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz	
C_{iss}	Input Capacitance		4.5	7.0	pF	V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz	
C_{rss}	Reverse Transfer Capacitance		1.5	3.0	pF	V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz	

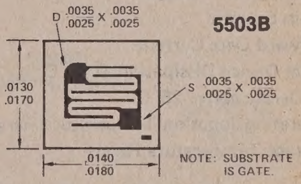
2N5460-2N5465
P-Channel JFET

PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY



NOTE: SUBSTRATE IS GATE.

ORDERING INFORMATION

TO-92	WAFER	DICE
2N5460	2N5460/W	2N5460/D
2N5461	2N5461/W	2N5461/D
2N5462	2N5462/W	2N5462/D
2N5463	2N5463/W	2N5463/D
2N5464	2N5464/W	2N5464/D
2N5465	2N5465/W	2N5465/D

MAXIMUM RATINGS

RATING	SYMBOL	2N5460 2N5461 2N5462	2N5463 2N5464 2N5465	UNITS
Drain-Gate Voltage	V_{DG}	40	60	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	40	60	Vdc
Forward Gate Current	$I_{G(f)}$	10		mAdc
Total Device Dissipation @ T_A = 25°C	P_D	310		mW
Derate above 25°C		2.82		mW/°C
Storage Temperature Range	T_{stg}	−65 to +150		°C
Operating Junction Temperature Range	T_J	−65 to +135		°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	40			Vdc	I_G = 10 μAdc, V_{DS} = 0	2N5460, 2N5461, 2N5462
		60					2N5463, 2N5464, 2N5465
$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.75		6.0	Vdc	V_{DS} = 15 Vdc, I_D = 1.0 μAdc	2N5460, 2N5463
		1.0		7.5			2N5461, 2N5464
		1.8		9.0			2N5462, 2N5465
I_{GSS}	Gate Reverse Current			5.0	na	V_{GS} = 20 Vdc, V_{DS} = 0	2N5460, 2N5461, 2N5462
				5.0	na	V_{GS} = 30 Vdc, V_{DS} = 0	2N5463, 2N5464, 2N5465
				1.0	μAdc	V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C	2N5460, 2N5461, 2N5462
				1.0	na	V_{GS} = 30 Vdc, V_{DS} = 0, T_A = 100°C	2N5463, 2N5464, 2N5465
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate Voltage Drain Current	1.0		5.0	mAdc	V_{DS} = 15 Vdc, V_{GS} = 0	2N5460, 2N5463
		2.0		9.0			2N5461, 2N5464
		4.0		16			2N5462, 2N5465
V_{GS}	Gate-Source Voltage	0.5		4.0	Vdc	V_{DS} = 15 Vdc, I_D = 0.1 mAdc	2N5460, 2N5463
		0.8		4.5		V_{DS} = 15 Vdc, I_D = 0.2 mAdc	2N5461, 2N5464
		1.5		6.0		V_{DS} = 15 Vdc, I_D = 0.4 mAdc	2N5462, 2N5465
SMALL-SIGNAL CHARACTERISTICS							
g_{fs}	Forward Transadmittance	1000		4000	μmhos	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz	2N5460, 2N5463
		1500		5000			2N5461, 2N5464
		2000		6000			2N5462, 2N5465
g_{os}	Output Admittance			75	μmhos	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz	
C_{iss}	Input Capacitance		5.0	7	pF	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz	
C_{rss}	Reverse Transfer Capacitance		1.0	2.0	pF	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz	
NF	Common-Source Noise Figure		1.0	2.5	dB	V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 100 Hz, BW = 1.0 Hz	
$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		60	115	nV/$\sqrt{Hz}$	V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz	

INTERSIL

2N5484-2N5486
N-Channel JFET

FEATURES

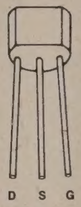
- Specified for 400 MHz Operation
- Can Be Used as a Low Capacitance Switch
- Economy Packaging
- $C_{rss} < 1.0$ pF

ABSOLUTE MAXIMUM RATINGS

Drain-Gate Voltage	25 V
Source Gate Voltage	25 V
Drain Current	30 mA
Forward Gate Current	10 mA
Total Device Dissipation @ 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature Range	–65°C to +150°C
Storage Temperature Range	–65°C to +150°C

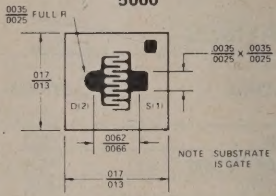
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5000



ORDERING INFORMATION

TO-92	WAFER	DICE
2N5484	2N5484/W	2N5484/D
2N5485	2N5485/W	2N5485/D
2N5486	2N5486/W	2N5486/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5484		2N5485		2N5486		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		–1.0		–1.0		–1.0	nA	$V_{GS} = -20$ V, $V_{DS} = 0$	
			–200		–200		–200			$T_A = +100°$C
BV_{GSS}	Gate-Source Breakdown Voltage	–25		–25		–25		V	$I_G = -1\ \mu$A, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.3	–3.0	–0.5	–4.0	–2.0	–6.0		$V_{DS} = 15$ V, $I_D = 10$ nA	
I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 1)	
g_{fs}	Common-Source Forward Transconductance	3000	6000	3500	7000	4000	8000	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
g_{os}	Common-Source Output Conductance		50		60		75			
$Re(y_{fs})$	Common-Source Forward Transconductance	2500								f = 100 MHz
				3000		3500				f = 400 MHz
$Re(y_{os})$	Common-Source Output Conductance		75							f = 100 MHz
					100		100			f = 400 MHz
$Re(y_{is})$	Common-Source Input Conductance		100							f = 100 MHz
					1000		1000			f = 400 MHz
C_{iss}	Common-Source Input Capacitance		5.0		5.0		5.0	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.0		1.0		1.0			
C_{oss}	Common-Source Output Capacitance		2.0		2.0		2.0			
NF	Noise Figure		2.5		2.5		2.5	dB	$V_{DS} = 15$ V, $V_{GS} = 0$, $R_G = 1$ MΩ	f = 1 kHz
			3.0						$V_{DS} = 15$ V, $I_D = 1$ mA, $R_G = 1$ kΩ	f = 100 MHz
					2.0		2.0		$V_{DS} = 15$ V, $I_D = 4$ mA, $R_G = 1$ kΩ	
					4.0		4.0			f = 400 MHz
G_{ps}	Common-Source Power Gain	16	25						$V_{DS} = 15$ V, $I_D = 1$ mA	f = 100 MHz
				18	30	18	30		$V_{DS} = 15$ V, $I_D = 4$ mA	
				10	20	10	20			f = 400 MHz

INTERSIL

2N5515-2N5524
Monolithic Dual N-Channel JFET

ABSOLUTE MAXIMUM RATINGS (Note 1)

@25°C (unless otherwise noted)

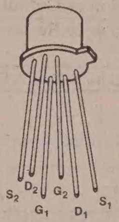
Maximum Temperatures		
Storage Temperature		-65°C to +200°C
Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation	250 mW	500 mW
@ Free Air Temperature	85°C	85°C
Linear Derating	3.85 mW/°C	7.7 mW/°C
Maximum Voltages & Current		
V_{GS} Gate to Source Voltage		-40 V
V_{GD} Gate to Drain Voltage		-40 V
I_G Gate Current		50 mA

FEATURES

- Tight Temperature Tracking — $\Delta V_{GS} < 5\ \mu V/°C$
- Tight Matching —
  - $V_{GS} < 5$ mV
  - $I_G < 10$ nA @ 125°C
  - $g_{fs} < 3\%$
  - $g_{oss} < .1\ \mu$mho
- High Common Mode-Rejection — CMRR < 100 db
- Low Noise — $e_n < 15$ nV / $\sqrt{\text{Hz}}$ @10 Hz

PIN CONFIGURATION

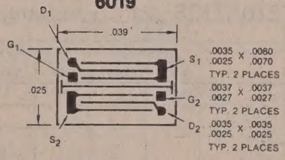
TO-71


S2
D2
G2
S1
G1
D1

CHIP TOPOGRAPHY

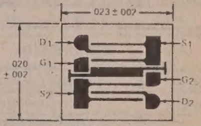
(2N5520-24)

6019


D1
G1
.039"
.025
S1
G2
D2
S2
.0035 x .0060
.0025 x .0070
TYP. 2 PLACES
.0037 x .0037
.0027 x .0027
TYP. 2 PLACES
.0035 x .0035
.0025 x .0025
TYP. 2 PLACES

(2N5515-19)

6017


.023 ± .002
.020 ± .002
D1
G1
S2
S1
G2
D2

SOURCE 3 x 6 MIL
DRAIN 3 x 3 MIL
GATE 3 x 3 MIL

ORDERING INFORMATION

TO-72	WAFER	DICE
2N5515	2N5515/W	2N5515/D
2N5516	2N5516/W	2N5516/D
2N5517	2N5517/W	2N5517/D
2N5518	2N5518/W	2N5518/D
2N5519	2N5519/W	2N5519/D
2N5520	2N5520/W	2N5520/D
2N5521	2N5521/W	2N5521/D
2N5522	2N5522/W	2N5522/D
2N5523	2N5523/W	2N5523/D
2N5524	2N5524/W	2N5524/D
2N5525	2N5525/W	2N5525/d

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current (+ 25°C) (+150°C)		−250 −250	pA nA	$V_{GS} = -30$ V, $V_{DS} = 0$	
BV_{GSS}	Gate-Source Breakdown Voltage	−40		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
V_P	Gate-Source Pinch-Off Voltage	−0.7	−4	V	$V_{DS} = 20$ V, $I_D = 1$ nA	
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	0.5	7.5	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
g_{fs}	Common-Source Forward Transconductance (Note 2)	1000	4000	μmho	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 kHz
g_{oss}	Common-Source Output Conductance		10	μmho	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 kHz
C_{rss}	Common-Source Reverse Transfer Capacitance		5	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
C_{iss}	Common-Source Input Capacitance		25	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
$\bar{e}_n$	Equivalent Input Noise Voltage 2N5515-19 2N5520-24 2N5515-24		30 15 10	nV/√Hz nV/√Hz nV/√Hz	$V_{DG} = 20$ V, $I_D = 200\ \mu A$ $V_{DG} = 20$ V, $I_D = 200\ \mu A$ $V_{DG} = 20$ V, $I_D = 200\ \mu A$	f = 10 Hz f = 10 Hz f = 1 kHz
I_G	Gate Current (+ 25°C) (+125°C)		−100 −100	pA nA	$V_{DG} = 20$ V, $I_D = 200\ \mu A$	
V_{GS}	Gate Source Voltage	−0.2	−3.8	V	$V_{DG} = 20$ V, $I_D = 200\ \mu A$	
g_{fs}	Common-Source Forward Transconductance (Note 2)	500	1000	μmho	$V_{DG} = 20$ V, $I_D = 200\ \mu A$	f = 1 kHz
g_{oss}	Common-Source Output Conductance		1	μmho	$V_{DG} = 20$ V, $I_D = 200\ \mu A$	

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I_{DSS1} I_{DSS2}	Drain Current Ratio at Zero Gate Voltage (Note 2)	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1		$V_{DS} = 20$ V, $V_{GS} = 0$
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current (+125°C)		10		10		10		10		10	nA	$V_{DG} = 20$ V, $I_D = 200\ \mu A$
g_{fs1} g_{fs2}	Transconductance Ratio (Note 2)	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1		$V_{DG} = 20$ V, $I_D = 200\ \mu A$ f = 1 KHz
$\lvert g_{oss1} - g_{oss2} \rvert$	Differential Output Conductance		0.1		0.1		0.1		0.1		0.1	μmho	$V_{DG} = 20$ V, $I_D = 200\ \mu A$ f = 1 KHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		5		10		15		15	mV	$V_{DG} = 20$ V, $I_D = 200\ \mu A$
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (T_A = +25°C to +125°C)		5		10		20		40		80	μV/°C	$V_{DG} = 20$ V, $I_D = 200\ \mu A$
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (T_A = +25 to −55°C)		5		10		20		40		80	μV/°C	$V_{DG} = 20$ V, $I_D = 200\ \mu A$
CMRR	Common Mode Rejection Ratio (Note 3)	100		100		90						dB	V_{DD} = 10 to 20 V, $I_D = 200\ \mu A$

NOTES:

1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 28mS used during test.
3. CMRR = $20 \mathrm{Log}_{10} \Delta V_{DD} / \Delta \lvert V_{GS1} - V_{GS2} \rvert$, ($\Delta V_{DD}$ = 10V)

INTERSIL

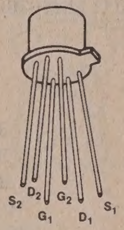
2N5564-2N5566
Dual N-Channel JFET

FEATURES

- **Specified Matching Characteristics**
- **High Gain — 7500μmho Minimum**
- **Low "ON" Resistance — 100Ω Maximum**

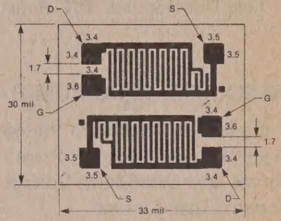
PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

6033



ORDERING INFORMATION

TO-71	WAFER	DICE
2N5564	2N5564/W	2N5564/D
2N5565	2N5564/W	2N5565/D
2N5566	2N5566/W	2N5566/D

ABSOLUTE MAXIMUM RATINGS

(25°C unless otherwise noted)

Gate-Gate Voltage .... ±80V
Gate-Drain or Gate-Source Voltage .... −40V
Gate Current.. 50mA
Device Dissipation (Each Side), $T_A = 25°C$
(Derate 2.2 mW/°C)........................... 325mW
Total Device Dissipation, $T_A = 25°C$
(Derate 3.3 mW/°C)........................... 650mW
Storage Temperature Range .... −65°C to +200°C
Lead Temperature
(1/16" from case for 10 seconds) .... 300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

	SYMBOL	PARAMETERS	CONDITIONS		MIN.	MAX.	UNIT
STATIC	I_{GSS}	Gate-Reverse Current	$V_{GS} = -20V, V_{DS} = 0$			−100	pA
				150°C		−200	nA
	BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu A, V_{DS} = 0$		−40		V
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V, I_D = 1nA$		−0.5	−3	
	$V_{GS(f)}$	Gate-Source Voltage	$V_{DS} = 0V, I_G = 2mA$			1.0	
	I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 15V, V_{GS} = 0$		5	30	mA
	$r_{DS(on)}$	Static Drain Source ON Resistance	$I_D = 1mA, V_{GS} = 0$			100	Ω
DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DG} = 15V, I_D = 2mA$	f = 1kHz	7500	12,500	μmho
				f = 100MHz	7000		
	g_{os}	Common-Source Output Conductance		f = 1kHz		45	
	C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1MHz		3	pF
	C_{iss}	Common-Source Input Capacitance				12	
	NF	Spot Noise Figure		$f = 10Hz, R_g = 1M$		1.0	dB
	$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		f = 10Hz		50	$\frac{nV}{\sqrt{Hz}}$

	SYMBOL	PARAMETERS	CONDITIONS		2N5564		2N5565		2N5566		UNIT
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	$V_{DS} = 15V, V_{GS} = 0$		0.95	1	0.95	1	0.95	1	—
	$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage				5		10		20	mV
	$\frac{\Delta\|V_{GS1}-V_{GS2}\|}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)	$V_{DS} = 15V, I_D = 2mA$	$T_A = 25°C$ $T_B = 125°C$		10		25		50	μV/°C
				$T_A = -55°C$ $T_B = 25°C$		10		25		50	
	$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	$V_{DS} = 15V, I_D = 2mA$	f = 1kHz	0.95	1	0.90	1	0.90	1	—

NOTES:

1. Pulse test required, pulse width 300μs, duty cycle ≤3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

INTERSIL

2N5638-2N5640
N-Channel JFET

FEATURES

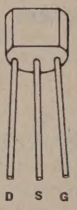
- Economy Packaging
- Fast Switching — $t_r < 5$ ns (2N5638)
- Low Drain-Source 'ON' Resistance < 30 Ω (2N5638)

ABSOLUTE MAXIMUM RATINGS

Drain-Source Breakdown Voltage	30 V
Drain-Gate Breakdown Voltage	30 V
Source-Gate Breakdown Voltage	30 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature Range	−65 to +135°C
Storage Temperature Range	−65 to +150°C

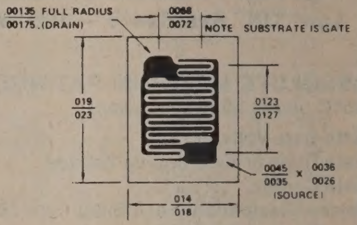
PIN CONFIGURATION

TO-92



CHIP TOPOGRAPHY

5001B


00135 / 00175 FULL RADIUS (DRAIN)
0068 / 0072
NOTE SUBSTRATE IS GATE
019 / 023
0123 / 0127
0045 / 0035 x 0036 / 0026 (SOURCE)
014 / 018

ORDERING INFORMATION

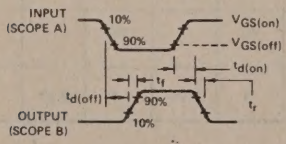
TO-92	WAFER	DICE
2N5638	2N5638/W	2N5638/D
2N5639	2N5639/W	2N5638/D
2N5640	2N5640/W	2N5640/D

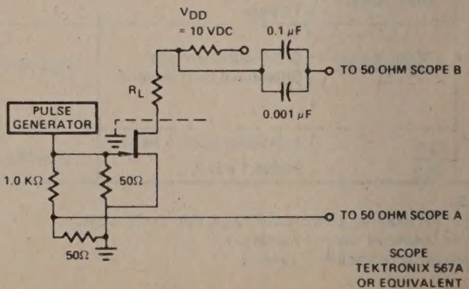
ELECTRICAL CHARACTERISTICS (25 °C unless otherwise noted)

CHARACTERISTIC		2N5638		2N5639		2N5640		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX			
BV_{GSS}	Gate Reverse Breakdown Voltage	−30		−30		−30		V	$I_G = -10\ \mu A$, $V_{DS} = 0$	
I_{GSS}	Gate Reverse Current		−1.0		−1.0		−1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
			−1.0		−1.0		−1.0	μA		$T_A = +100°C$
$I_{D(off)}$	Drain Cutoff Current		1.0		1.0		1.0	nA	$V_{DS} = 15$ V, $V_{GS} = -12$ V (2N5638) $V_{GS} = -8$ V (2N5639), $V_{GS} = -6$ V (2N5640)	
			1.0		1.0		1.0	μA		$T_A = +100°C$
I_{DSS}	Saturation Drain Current	50		25		5.0		mA	$V_{DS} = 20$ V, $V_{GS} = 0$ (Note 1)	
$V_{DS(on)}$	Drain-Source ON Voltage		0.5		0.5		0.5	V	$V_{GS} = 0$, $I_D = 12$ mA (2N5638), $I_D = 6$ mA (2N5639), $I_D = 3$ mA (2N5640)	
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$I_D = 1$ mA, $V_{GS} = 0$	
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		10		10		10	pF	$V_{GS} = -12$ V, $V_{DS} = 0$	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
$t_{d(on)}$	Turn-On Delay Time		4.0		6.0		8.0	ns	$V_{DD} = 10$ V $I_{D(on)} = 12$ mA (2N5638) $V_{GS(on)} = 0$ $I_{D(on)} = 6$ mA (2N5639) $V_{GS(off)} = -10$ V $I_{D(on)} = 3$ mA (2N5640) $R_G = 50\ \Omega$	
t_r	Rise Time		5.0		8.0		10			
t_d	Turn-OFF Delay Time		5.0		10		15			
t_f	Fall Time		10		20		30			

NOTE: 1. Pulse test PW ≤ 300 μs, duty cycle ≤ 3.0%.

$$R_L = \frac{V_{DD}}{I_D} - (r_{DS(on)} + 50)$$


INPUT (SCOPE A)
10%
90%
$V_{GS(on)}$
$V_{GS(off)}$
$t_{d(on)}$
t_f
$t_{d(off)}$
90%
t_r
OUTPUT (SCOPE B)
10%


V_{DD} = 10 VDC
0.1 μF
TO 50 OHM SCOPE B
R_L
0.001 μF
PULSE GENERATOR
1.0 KΩ
50Ω
TO 50 OHM SCOPE A
50Ω
SCOPE TEKTRONIX 567A OR EQUIVALENT

INTERSIL

2N5902-2N5909
Dual Monolithic N-Channel JFET

FEATURES

- Tracking < 5 µV/°C
- $I_G < 1$ pa
- Matched V_{GS}, $\Delta V_{GS}/\Delta T$, g_{fs}, & g_{oss}

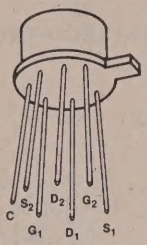
ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	10 mA
Device Dissipation (Each Side), $T_A = 25°C$ (Derate 3 mW/°C)	367 mW
Total Device Dissipation, $T_A = 25°C$ (Derate 4 mW/°C)	500 mW
Storage Temperature Range	−65°C to +150°C

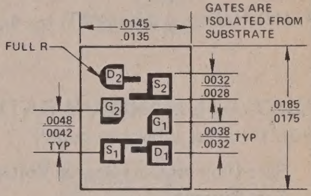
PIN CONFIGURATION

TO-99



CHIP TOPOGRAPHY

6015



ORDERING INFORMATION

TO-99	WAFER	DICE	TO-99	WAFER	DICE
2N5902	2N5902/W	2N5902/D	2N5906	2N5906/W	2N5906/D
2N5903	2N5903/W	2N5903/D	2N5907	2N5907/W	2N5907/D
2N5904	2N5904/W	2N5904/D	2N5908	2N5908/W	2N5908/D
2N5905	2N5905/W	2N5905/D	2N5909	2N5905/W	2N5909/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5902-5 MIN	2N5902-5 MAX	2N5906-9 MIN	2N5906-9 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−5		−2	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
			−10		−5	nA		125°C
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		V	$I_G = -1$ µA, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.6	−4.5	−0.6	−4.5		$V_{DS} = 10$ V, $I_D = 1$ nA	
V_{GS}	Gate Source Voltage		−4		−4		$V_{DG} = 10$ V, $I_D = 30$ µA	
I_G	Gate Operating Current		−3		−1	pA		
			−3		−1	nA		125°C
I_{DSS}	Saturation Drain Current	30	500	30	500	µA	$V_{DS} = 10$ V, $V_{GS} = 0$	
g_{fs}	Common-Source Forward Transconductance	70	250	70	250	µmho		f = 1 kHz
g_{os}	Common-Source Output Conductance		5		5			
C_{iss}	Common-Source Input Capacitance		3		3	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5			
g_{fs}	Common-Source Forward Transconductance	50	150	50	150	µmho	$V_{DG} = 10$ V, $I_D = 30$ µA	f = 1 kHz
g_{os}	Common-Source Output Conductance		1		1			
$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$	$V_{DS} = 10$ V, $V_{GS} = 0$	
NF	Spot Noise Figure		3		1	dB		f = 100 Hz $R_G = 10$ M

PARAMETER		2N5902-6 MIN	2N5902-6 MAX	2N5903-7 MIN	2N5903-7 MAX	2N5904-8 MIN	2N5904-8 MAX	2N5905-9 MIN	2N5905-9 MAX	UNIT	TEST CONDITIONS	
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		2.0		2.0		2.0		2.0	nA	$V_{DG} = 10$ V, $I_D = 30$ µA, $T_A = 125°C$	2N5902-5
			0.2		0.2		0.2		0.2			2N5906-9
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1	0.95	1	0.95	1	—	$V_{DS} = 10$ V, $V_{GS} = 0$	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1	0.95	1		$V_{DG} = 10$ V, $I_D = 30$ µA	f = 1 kHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
$\frac{\Delta \lvert V_{BS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points T_A and T_B)		5		10		20		40	µV/°C		$T_A = 25°C$ $T_B = 125°C$
			5		10		20		40			$T_A = -55°C$ $T_B = 25°C$
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		0.2		0.2		0.2		0.2	µmho		f = 1 kHz

2N5911, 2N5912
IT5911, IT5912
Dual Monolithic N-Channel JFET

FEATURES

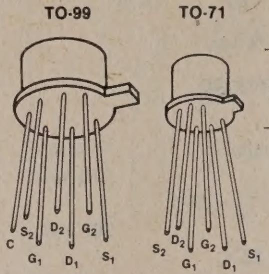
- Tracking < 20 µV/°C
- g_{fs} < 5000 µmho, 0 –100 MHz
- Matched V_{GS}, $\Delta V_{GS}/\Delta T$, I_G, g_{fs},

ABSOLUTE MAXIMUM RATINGS

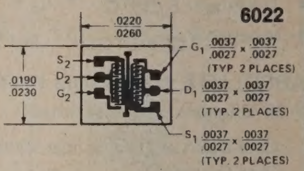
@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-25V
Gate Current	50 mA
Device Dissipation (Each Side),	367 mW
Linear Derating	3 mW/°C
Total Device Dissipation,	500 mW
Linear Derating	4 mW/°C
Storage Temperature Range	-65°C to +200°C

PIN CONFIGURATION



CHIP TOPOGRAPHY


6022
.0220
.0260
.0190
.0230
S2
D2
G2
G1 .0037/.0027 × .0037/.0027 (TYP. 2 PLACES)
D1 .0037/.0027 × .0037/.0027 (TYP. 2 PLACES)
S1 .0037/.0027 × .0037/.0027 (TYP. 2 PLACES)

ORDERING INFORMATION

TO-71	TO-99	WAFER	DICE
IT5911	2N5911	2N5911/W	2N5911/D
IT5912	2N5912	2N5912/W	2N5912/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		–100	pA	V_{GS} = –15 V, V_{DS} = 0	
			–250	nA		150°C
BV_{GSS}	Gate Reverse Breakdown Voltage	–25		V	I_G = –1 µA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1	–5		V_{DS} = 10 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	–0.3	–4		V_{DG} = 10 V, I_D = 5 mA	
I_G	Gate Operating Current		–100	pA		
			–100	nA		125°C
I_{DSS}	Saturation Drain Current (Pulsewidth 300 µs, duty cycle ≤ 3%)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	µmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
g_{os}	Common-Source Output Conductance		100			f = 1 kHz
g_{oss}	Common-Source Output Conductance		150			f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
NF	Spot Noise Figure		1	dB		f = 10 kHz R_G = 100K Ω

PARAMETER		IT, 2N5911		IT, 2N5912		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1		V_{DS} = 10 V, V_{GS} = 0 (Pulsewidth 300 µs, duty cycle ≤ 3%)	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points, T_A and T_B)		20		40	µV/°C		T_A = 25°C T_B = 125°C
			20		40			T_A = –55°C T_B = 25°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1	0.95	1			f = 1 kHz

2N6483-2N6485
Low Noise Dual Monolithic N-Channel JFET

FEATURES

- Ultra Low Noise
  $\bar{e}_n < 10\ \text{nV}/\sqrt{\text{Hz}}$ at 10 Hz
- High CMRR > 100 dB
- Low Offset
  $\Delta\ |V_{GS1} - V_{GS2}| < 5$ mV
- Tight Tracking
  $\Delta\ |V_{GS1} - V_{GS2}|/\Delta T < 5\ \mu\text{V}/^\circ\text{C}$

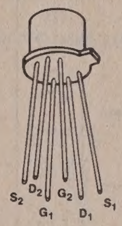
ABSOLUTE MAXIMUM RATINGS (Note 1)

(@ 25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	3.85 mW/°C
Both Sides	7.7 mW/°C
Maximum Voltages & Currents	
V_{GS} Gate to Source Voltage	-50 V
V_{GD} Gate to Drain Voltage	-50 V
$V_{G1\,G2}$ Gate to Gate Voltage	±50 V
I_G Gate Current	50 mA

PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

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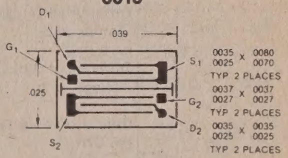


ORDERING INFORMATION

TO-71	WAFER	DICE
2N6483	2N6483/W	2N6483/D
2N6484	2N6484/W	2N6484/D
2N6485	2N6485/W	2N6485/D

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

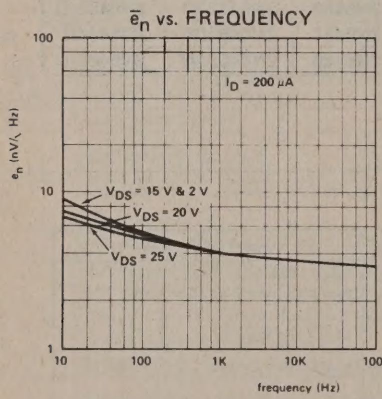
SYMBOL	CHARACTERISTICS	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		200 200	pA nA	$V_{GS} = -30$ V, $V_{DS} = 0$, $T_A = +25$°C $V_{GS} = -30$ V, $V_{DS} = 0$, $T_A = +150$°C
BV_{GSS}	Gate-Source Breakdown Voltage	50		V	$I_G = 1\ \mu$A, $V_{DS} = 0$
V_p	Gate-Source Pinch-Off Voltage	-0.7	-4.0	V	$V_{DS} = 20$ V, $I_D = 1$ nA
I_{DSS}	Drain Current at Zero Gate Voltage	0.5	7.5	mA	$V_{DS} = 20$ V, $V_{GS} = 0$ (Note 2)
g_{fs}	Common-Source Forward Transconductance	1000	4000	μmho	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 KHz (Note 2)
g_{oss}	Common-Source Output Conductance		10	μmho	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 KHz
C_{iss}	Common-Source Input Capacitance		20	pF	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3.5	pF	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz
I_G	Gate Current		100 100	pA nA	$V_{GD} = 20$ V, $I_D = 200\ \mu$A, $T_A = +25$°C $V_{DG} = 20$ V, $I_D = 200\ \mu$A, $T_A = +150$°C
V_{GS}	Gate-Source Voltage	0.2	3.8	V	$V_{DG} = 20$ V, $I_D = 200\ \mu$A
g_{fs}	Common-Source Forward Transconductance	500	1500	μmho	$V_{DG} = 20$ V, $I_D = 200\ \mu$A, f = 1 KHz (Note 2)
g_{os}	Common-Source Output Conductance		1	μmho	$V_{DG} = 20$ V, $I_D = 200\ \mu$A
$\bar{e}_n$	Equivalent Input Noise Voltage		10 5	$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$	$V_{DS} = 20$ V, $I_D = 200\ \mu$A, f = 10 Hz $V_{DS} = 20$ V, $I_D = 200\ \mu$A, f = 1 KHz

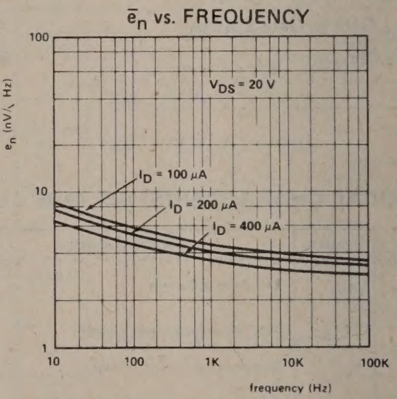
MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

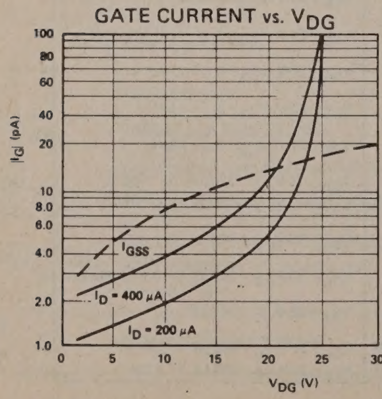
SYMBOL	CHARACTERISTIC	2N6483		2N6484		2N6485		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1	0.95	1	0.95	1	–	V_{DS} = 20 V, V_{GS} = 0 (Note 2)
$\lvert I_{G1} - I_{G2}\rvert$	Differential Gate Current		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA T_A = +125°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1	–	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
$\lvert g_{os1} - g_{os2}\rvert$	Differential Output Conductance		0.1		0.1		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz
$\lvert V_{GS1} - V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = +25°C to +125°C
$\frac{\Delta\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = -55°C to + 25°C
CMRR	Common Mode Rejection Ratio	100		100		90		dB	V_{DD} = 10 to 20 V, I_D = 200 μA (Note 3)

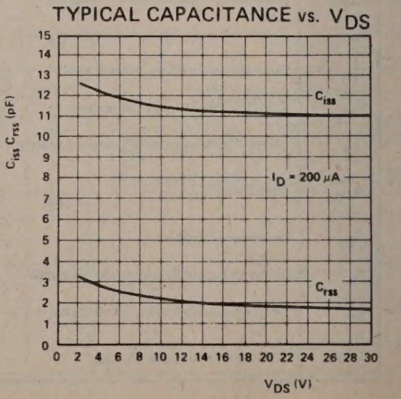
NOTES:
1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 2 ms used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta\lvert V_{GS1} - V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10 V), not included in JEDEC registration

TYPICAL OPERATING CHARACTERISTICS









IMF6485
Low Noise Dual Monolithic N-Channel JFET

FEATURES

- $\bar{e}_n < 10\text{nV}/\sqrt{\text{Hz}}$ @ 10Hz
- CMRR > 90 dB
- $\Delta\,|V_{GS1} - V_{GS2}| < 25$ mV
- $\Delta\,|V_{GS1} - V_{GS2}| < 40\ \mu V/^\circ C$

ABSOLUTE MAXIMUM RATINGS (Note 1)

(@ 25°C unless otherwise noted)

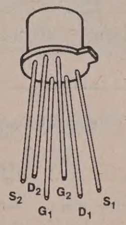
Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	3.85 mW/°C
Both Sides	7.7 mW/°C
Maximum Voltages & Currents	
V_{GS} Gate to Source Voltage	-50 V
V_{GD} Gate to Drain Voltage	-50 V
V_{G1-G2} Gate to Gate Voltage	±50 V
I_G Gate Current	50 mA

GENERAL DESCRIPTION

This N-Channel Junction FET is characterized for ultra low noise applications requiring tightly controlled and specified noise parameters at 10 Hz and 1000 Hz. Tight matching specifications make this device ideal as the input stage for low frequency differential instrumentation amplifiers.

PIN CONFIGURATION

TO-71



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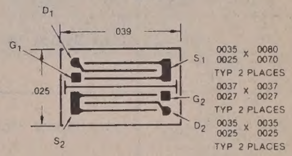


ORDERING INFORMATION

TO-71	WAFER	DICE
IMF6485	IMF6485/W	IMF6485/D

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

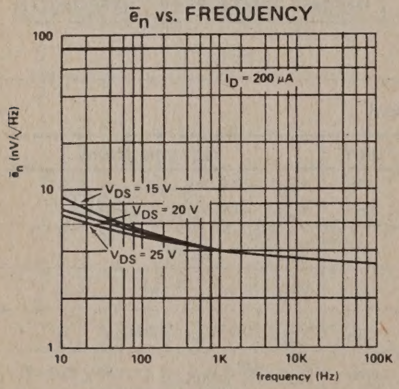
SYMBOL	CHARACTERISTICS	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		-200 -200	pA nA	$V_{GS} = -30$ V, $V_{DS} = 0$, $T_A = +25^\circ C$ $V_{GS} = -30$ V, $V_{DS} = 0$, $T_A = +150^\circ C$
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	$I_G = -1\ \mu A$, $V_{DS} = 0$
V_p	Gate-Source Pinch-Off Voltage	-0.7	-4.0	V	$V_{DS} = 20$ V, $I_D = 1$ nA
I_{DSS}	Drain Current at Zero Gate Voltage	0.5	7.5	mA	$V_{DS} = 20$ V, $V_{GS} = 0$ (Note 2)
g_{fs}	Common-Source Forward Transconductance	1000	4000	µmho	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 KHz (Note 2)
g_{oss}	Common-Source Output Conductance		10	µmho	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 KHz
C_{iss}	Common-Source Input Capacitance		20	pF	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3.5	pF	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz
I_G	Gate Current		100 100	pA nA	$V_{GD} = 20$ V, $I_D = 200\ \mu A$, $T_A = +25^\circ C$ $V_{DG} = 20$ V, $I_D = 200\ \mu A$, $T_A = +150^\circ C$
V_{GS}	Gate-Source Voltage	0.2	-3.8	V	$V_{DG} = 20$ V, $I_D = 200\ \mu A$
g_{fs}	Common-Source Forward Transconductance	500	1500	µmho	$V_{DG} = 20$ V, $I_D = 200\ \mu A$, f = 1 KHz (Note 2)
g_{os}	Common-Source Output Conductance		1	µmho	$V_{DG} = 20$ V, $I_D = 200\ \mu A$
$\bar{e}_n$	Equivalent Input Noise Voltage		15 10	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$	$V_{DS} = 20$ V, $I_D = 200\ \mu A$, f = 10 Hz $V_{DS} = 20$ V, $I_D = 200\ \mu A$, f = 1 KHz

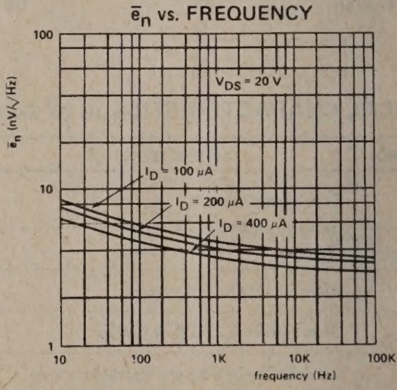
MATCHING CHARACTERISTICS (@ 25° C unless otherwise noted)

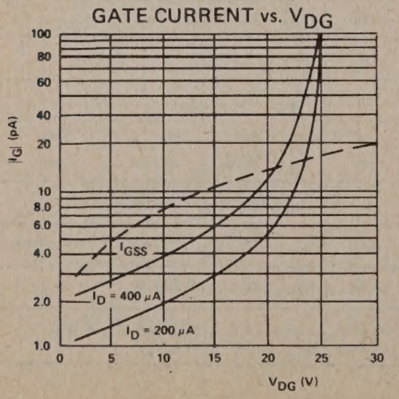
SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT	CONDITIONS
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1	–	V_{DS} = 20 V, V_{GS} = 0 (Note 2)
$\|I_{G1} - I_{G2}\|$	Differential Gate Current		10	nA	V_{DG} = 20 V, I_D = 200 μA T_A = +125° C
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	0.95	1	–	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
$\|g_{os1} - g_{os2}\|$	Differential Output Conductance		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz
$\|V_{GS1} - V_{GS2}\|$	Differential Gate-Source Voltage		25	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta\|V_{GS1} - V_{GS2}\|}{\Delta T}$	Gate-Source Voltage Differential Drift		40	μV/° C	V_{CG} = 20 V, I_D = 200 μA T_A = +25° C to +125° C
$\frac{\Delta\|V_{GS1} - V_{GS2}\|}{\Delta T}$	Gate-Source Voltage Differential Drift		40	μV/° C	V_{DG} = 20 V, I_D = 200 μA T_A = -55° C to +25° C
CMRR	Common Mode Rejection Ratio	90		dB	V_{DD} = 10 to 20 V, I_D = 200 μA (Note 3)

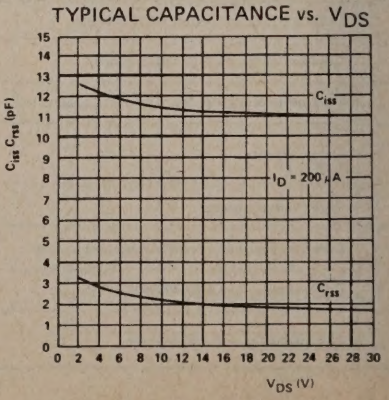
NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 2 ms used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta|V_{GS1} - V_{GS2}|$, ($\Delta V_{DD}$ = 10 V)

TYPICAL OPERATING CHARACTERISTICS









Vertical Power MOSFETs

$BV_{DSS} > 350V$, $r_{DS(on)} < 5\Omega$

Page

IVN6000KN Series 2-31

$BV_{DSS} < 100V$, $r_{DS(on)} < 0.5\Omega$

IVN5200/1HN Series 2-23
IVN5200/1KN Series 2-25
IVN5200/1TN Series 2-27
IVN5201CN Series 2-29

$BV_{DSS} < 100V$, $r_{DS(on)} < 5\Omega$

VN10KM 2-3
VN30AB Series 2-5
VN35AK Series 2-7
VN40AF Series 2-9
VN46AF Series 2-11
IVN5000/1AN Series 2-13
IVN5000/1BN Series 2-15
IVN5000/1SN Series 2-17
IVN5000/1TN Series 2-19
IVN5001AZ Series 2-21
IVN6660/61 Series 2-37
2N6660/61 Series 2-39

SELECTOR GUIDE N-CHANNEL ENHANCEMENT MODE VERTICAL POWER MOS $BV_{DSS} < 100V$

$r_{DS(on)}$ OHMS	$I_{D(on)}$ AMPS		$V_{GS(th)}$ VOLTS		P_D WATTS $T_C = 25°C$	BV_{DSS} — DRAIN-SOURCE BREAKDOWN VOLTAGE										PACKAGE
						35V MIN		40V MIN		60V MIN		80V MIN		90V MIN		
MAX	STEADY	PEAK	MIN	MAX	MIN	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	
0.5	5.0	12	0.8	2.0	50				IVN5200KND		IVN5200KNE		IVN5200KNF			TO-3
0.5	5.0	12	0.8	3.6	50				IVN5201KND		IVN5201KNE		IVN5201KNF			
0.5	4.0	10	0.8	2.0	12.5				IVN5200TND		IVN5200TNE		IVN5200TNF			TO-39
0.5	4.0	10	0.8	3.6	12.5				IVN5201TND		IVN5201TNE		IVN5201TNF			
2.5	1.2	3.0	0.8	2.0	6.25		VN35AK		IVN5000TND		IVN5000TNE		IVN5000TNF		IVN5000TNG	
2.5	1.2	3.0	0.8	—	6.25	VN35AB			IVN5001TND		IVN5001TNE		IVN5001TNF		IVN5001TNG	
3.0	1.2	3.0	0.8	2.0	6.25					IVN6660	VN66AK					
3.5	1.2	3.0	0.8	2.0	6.25						VN67AK					
3.5	1.2	3.0	0.8	—	6.25					VN67AB						
4.0	1.2	3.0	0.8	2.0	6.25									IVN6661	VN98AK	
4.5	1.2	3.0	0.8	2.0	6.25										VN99AK	
4.5	1.2	3.0	0.8	—	6.25							VN89AB				
5.0	1.2	3.0	0.8	—	6.25	VN30AB								VN90AB		
2.5	0.9	3.0	0.8	2.0	3.13				IVN5000SND		IVN5000SNE		IVN5000SNF			TO-52
2.5	0.9	3.0	0.8	3.6	3.13				IVN5001SND		IVN5001SNE		IVN5001SNF			
0.5	5.0	12	0.8	2.0	30				IVN5200HND		IVN5200HNE		IVN5200HNF			TO-66
0.5	5.0	12	0.8	3.6	30				IVN5201HND		IVN5201HNE		IVN5201HNF			
3.0	1.7	3.0	0.8	—	12			VN46AF		VN66AF						TO-202 (PLASTIC)
3.5	1.7	3.0	0.8	—	12					VN67AF						
4.0	1.7	3.0	0.8	—	12							VN88AF				
4.5	1.7	3.0	0.8	—	12							VN89AF				
5.0	1.7	3.0	0.8	—	12			VN40AF								
2.5	1.7	3.0	0.8	2.0	12				IVN5000BND		IVN5000BNE		IVN5000BNF			
2.5	1.7	3.0	0.8	3.6	12				IVN5001BND		IVN5001BNE		IVN5001BNF			
0.5	5.0	12	0.8	3.6	30				IVN5201CND		IVN5201CNE		IVN5201CNF			TO-220 (PLASTIC)
2.5	0.7	2.0	0.8	2.0	2.0				IVN5000AND		IVN5000ANE		IVN5000ANF			TO-237 (PLASTIC)
2.5	0.7	2.0	0.8	3.6	2.0				IVN5001AND		IVN5001ANE		IVN5001ANF			
—	0.5	1.0	0.3	2.5	1.0					VN10KM						
3.0	0.5	2.0	0.8	3.6	2.0					IVN5001AZE		IVN5001AZF				

$R_{DS(on)}$ OHMS	$I_{D(on)}$ AMPS		$V_{GS(th)}$ VOLTS		P_D WATTS $T_C = 25°C$	BV_{DSS}		
MAX	STEADY	PEAK	MIN	MAX	MIN	350V	400V	450V
3.0	2.25	7.5	2.0	5.0	36	IVN6000KNR	IVN6000KNS	IVN6000KNT

INTERSIL

VN10 KM
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **Directly drives inductive loads**
- **High speed, high peak current switching**
- **Inherent current sharing capability when paralleled**
- **Directly interfaces to CMOS, DTL, TTL logic**
- **Simple, straight-forward DC biasing**
- **Inherent protection from thermal runaway**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-source Voltage	60V
Drain-gate Voltage	60V
Continuous Drain Current (see note 1)	0.5A
Peak Drain Current (see note 2)	1.0V
Gate-source Forward Voltage	+15V
Gate-source Reverse Voltage	0.3V
Continuous Device Dissipation at (or below) 25°C Case Temperature	1.0W
Linear Derating Factor	8mW/°C
Operating Junction Temperature Range	−40 to +150°C
Storage Temperature Range	−40 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

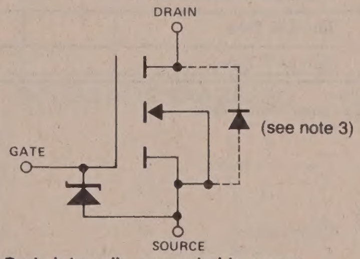
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

APPLICATIONS

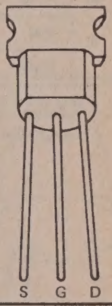
- **LED and lamp drivers**
- **TTL and CMOS to high current interface**
- **High speed switches**
- **Line drivers**
- **Relay drivers**
- **Transformer drivers**

SCHEMATIC DIAGRAM

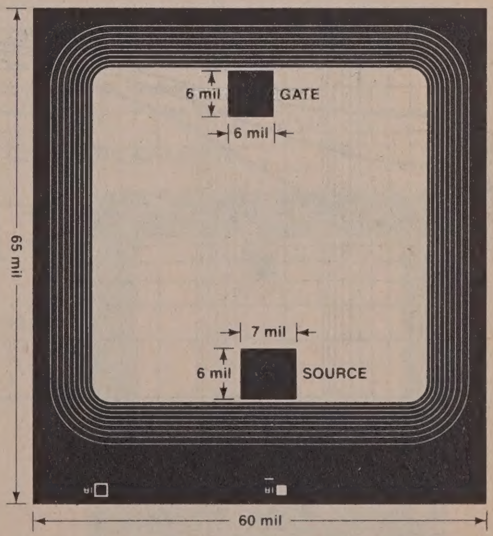
(OUTLINE DWG. TO-237)



Body internally connected to source
Drain common to tab



CHIP TOPOGRAPHY

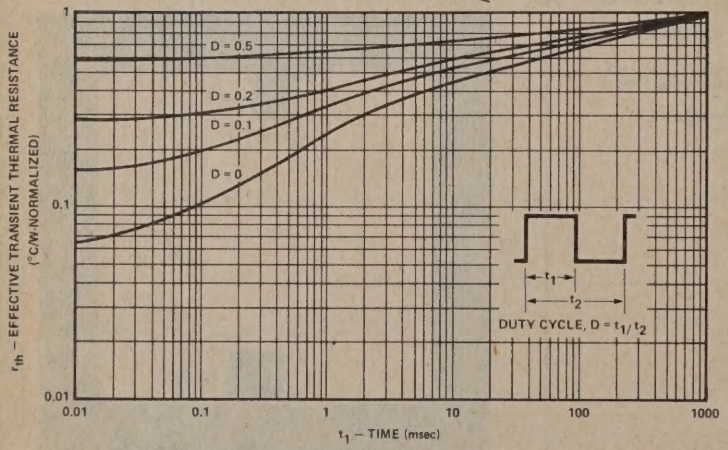


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

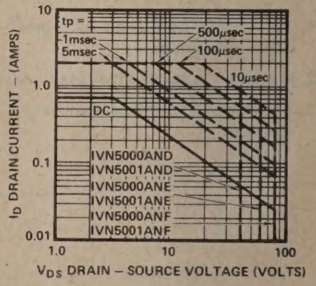
Characteristic				Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown	60			V	V_{GS} = 0V, I_D = 100 µA	
2		$V_{GS(th)}$	Gate Threshold Voltage	0.3		2.5	V	V_{DS} = V_{GS}, I_D = 1 mA	
3		I_{GSS}	Gate-Body Leakage			10	nA	V_{GS} = 10V, V_{DS} = 0	Note 2
4		I_{DSS}	Zero Gate Voltage Drain Current			10	µA	V_{DS} = 40V, V_{GS} = 0	
5		$I_{D(on)}$	ON-State Drain Current	0.25			A	V_{DS} = 25V, V_{GS} = 5V	Note 1
6				0.50				V_{DS} = 25V, V_{GS} = 10V	
7		$V_{DS(on)}$	Drain-Source ON Voltage			2.5	V	V_{GS} = 10V, I_D = 0.5A	
8	DYNAMIC	g_{fs}	Forward Transconductance	100	200		mmho	V_{DS} = 15V, I_D = 0.5A	
9		C_{iss}	Input Capacitance		48		pF	V_{DS} = 25V, f = 1 MHz	Note 2
10		C_{oss}	Output Capacitance		16				
11		C_{rss}	Feedback Capacitance		2				
12		t_{ON}	Turn-ON Time		5		ns	See Switching Times Test Circuit, page 2-42	
13		t_{OFF}	Turn-OFF Time		5				

NOTES: 1. Pulse test −80 µs pulse, 1% duty cycle.
2. Sample Test.

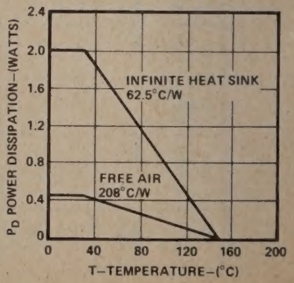
THERMAL RESPONSE



DC SAFE OPERATING REGION
Tc = 25°C



POWER DISSIPATION DERATING



Note: For other 5000 family characteristic curves, see page 2-41.

VN30AB, VN35AB, VN67AB, VN89AB, VN90AB
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **Simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS
(T_A = 25° C unless otherwise noted)

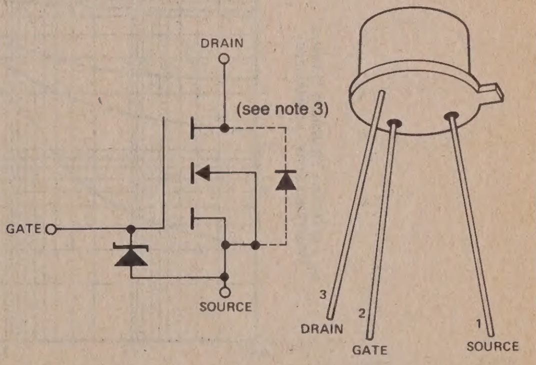
Drain-source Voltage	
VN30AB, VN35AB	35V
VN67AB	60V
VN89AB	80V
VN90AB	90V
Drain-gate Voltage	
VN30AB, VN35AB	35V
VN67AB	60V
VN89AB	80V
VN90AB	90V
Continuous Drain Current (see note 1)	1.2A
Peak Drain Current (see note 2)	3.0A
Continuous Forward Gate Current	2.0mA
Peak-gate Forward Current	100mA
Peak-gate Reverse Current	100mA
Gate-source Forward (Zener) Voltage	+15V
Gate-source Reverse (Zener) Voltage	–0.3V
Thermal Resistance, Junction to Case	20°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	6.25W
Linear Derating Factor	50mW/°C
Operating Junction Temperature Range	–55 to +150°C
Storage Temperature Range	–55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

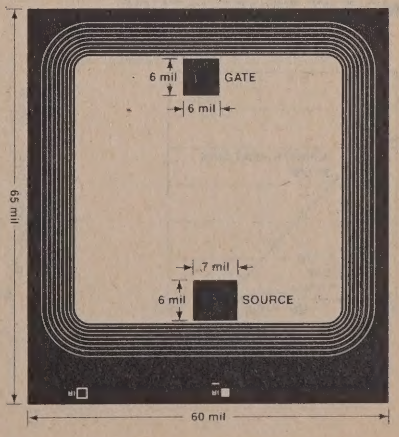
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM
(OUTLINE DWG. TO-39)



Body internally connected to source.
Drain common to case.

CHIP TOPOGRAPHY



VN30AB, VN35AB, VN67AB, VN89AB, VN90AB

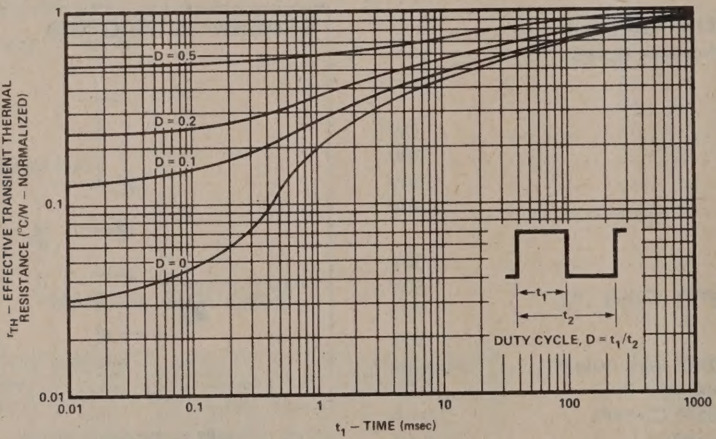
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		VN30AB			VN35AB			VN67AB			VN89AB			VN90AB			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DSS}	Drain Source Breakdown	35			35			60			80			90			V	$I_D = 10\mu A$, $V_{GS} = 0$
2		$V_{GS(th)}$	Gate Threshold Voltage	0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2			$I_D = 1.0mA$, $V_{DS} = V_{GS}$
3		I_{GSS}	Gate-Body Leakage		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5	μA	$V_{GS} = 10V$, $V_{DS} = 0$
4		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10			10			10		$V_{DS} = 25V$, $V_{GS} = 0$
5		$R_{DS(on)}$	Drain-Source ON-State Resistance (Note 1)			6.0			4.5			5.1			5.1			6.0	Ω	$V_{GS} = 5V$, $I_D = 300mA$
					2.2	5.0		2.2	2.5		2.2	3.5		2.2	4.5		2.2	5.0		$V_{GS} = 10V$, $I_D = 1.0A$
6		$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		A	$V_{DS} = 25V$, $V_{GS} = 10V$
7	DYNAMIC	g_{fs}	Forward Transconductance		250			250			250			250			250		m Ω	$V_{DS} = 25V$, $I_D = 0.5A$
8		C_{iss}	Input Capacitance (Note 2)			50			50			50			50			50	pF	$V_{GS} = 0$, $V_{DS} = 24V$, $f = 1.0MHz$
9		C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10			10			10		
10		C_{oss}	Common Source Output Capacitance (Note 2)			40			40			40			40			40		
11		t_{on}	Turn-ON Time (Note 2)		4	10		4	10		4	10		4	10		4	10	ns	
12		t_{off}	Turn-OFF Time (Note 2)		4	10		4	10		4	10		4	10		4	10		

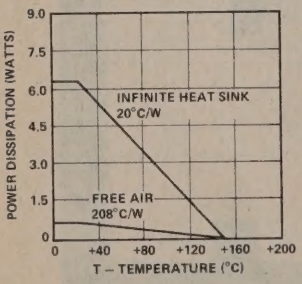
Note 1. Pulse Test — 80μs, 1% duty cycle.

Note 2. Sample Test.

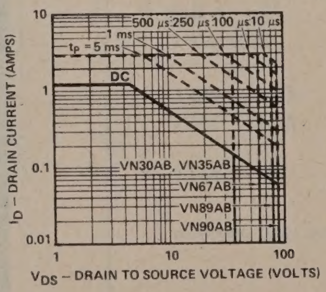
THERMAL RESPONSE



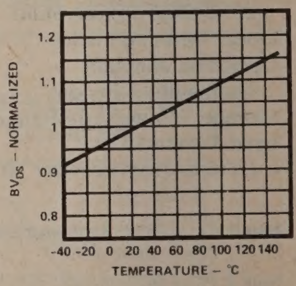
POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION
Tc = 25°C



BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE



INTERSIL

VN35AK, VN66AK, VN67AK, VN98AK, VN99AK
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high current switching
- High gain-bandwidth product
- Inherently temperature stable
- Extended safe operating area
- Simple DC biasing
- Requires almost zero current drive

APPLICATIONS

- High current analog switches
- RF power amplifiers
- Laser diode pulsers
- Line drivers
- Logic buffers
- Pulse amplifiers

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-source Voltage	
VN35AK	35V
VN66AK, VN67AK	60V
VN98AK, VN99AK	90V
Drain-gate Voltage	
VN35AK	35V
VN66AK, VN67AK	60V
VN98AK, VN99AK	90V
Continuous Drain Current (see note 1)	1.2A
Peak Drain Current (see note 2)	3.0A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	−30V
Thermal Resistance, Junction to Case	20°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	6.25W
Linear Derating Factor	50mW/°C
Operating Junction Temperature Range	−55 to +150°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

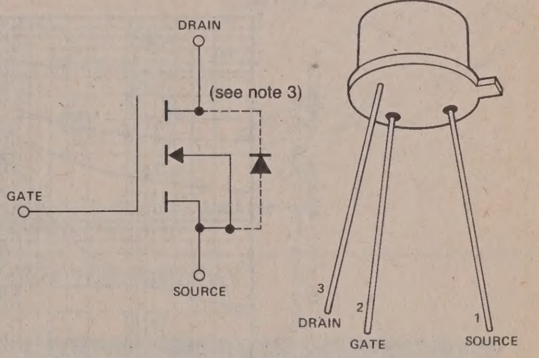
Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

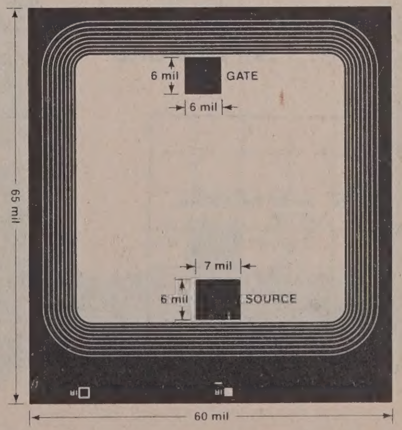
SCHEMATIC DIAGRAM

(OUTLINE DWG. TO-39)



Body internally connected to source.
Drain common to case.

CHIP TOPOGRAPHY



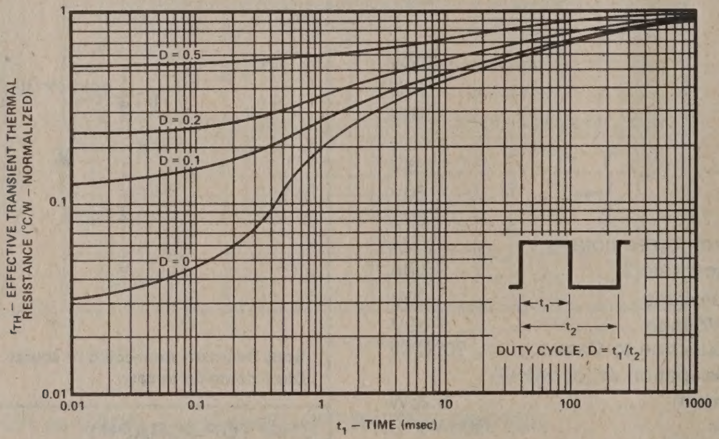
VN35AK, VN66AK, VN67AK, VN98AK, VN99AK

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

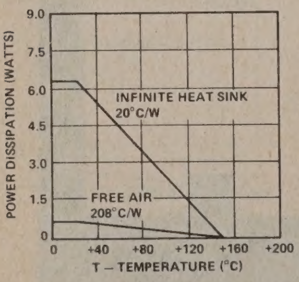
		CHARACTERISTIC		VN35AK			VN66AK VN67AK			VN98AK VN99AK			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			60			90			V	$V_{GS} = 0$, $I_D = 10\mu A$	
2		$V_{GS(th)}$	Gate-Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		$V_{DS} = V_{GS}$, $I_D = 1mA$	
3		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100		0.5	100	nA	$V_{GS} = 15V$, $V_{DS} = 0$	
4						500			500			500		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$ (Note 2)	
5		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10	µA	V_{DS} = Max. Rating, $V_{GS} = 0$	
6						500			500			500		V_{DS} = 0.8 Max. Rating, $V_{GS} = 0$, $T_A = 125°C$ (Note 2)	
7					100			100			100		nA	$V_{DS} = 25V$, $V_{GS} = 0$	
8		$I_{D(on)}$	ON-State Drain Current	1.0	2.0		1.0	2.0		1.0	2.0		A	$V_{DS} = 25V$, $V_{GS} = 10V$	
9		$V_{DS(on)}$	Drain-Source Saturation Voltage VN66AK					1.0			1.1		V	$V_{GS} = 5V$, $I_D = 0.3A$	(Note 1)
10			VN98AK					2.2	3.0		2.2	4.0		$V_{GS} = 10V$, $I_D = 1.0A$	
11			VN35AK VN67AK VN99AK		1.0			1.1			1.2			$V_{GS} = 5V$, $I_D = 0.3A$	
12					2.2	2.5		2.2	3.5		2.2	4.5		$V_{GS} = 10V$, $I_D = 1.0A$	
13	DYNAMIC	g_{fs}	Forward Transconductance	170	250		170	250		170	250		mΩ	$V_{DS} = 24V$, $I_D = 0.5A$, f = 1KHz	
14		C_{iss}	Input Capacitance		40	50		40	50		40	50	pF	$V_{GS} = 0$, $V_{DS} = 24V$, f = 1MHz	(Note 2)
15		C_{oss}	Common Source Output Capacitance		38	45		35	40		32	40			
16		C_{rss}	Reverse Transfer Capacitance		7	10		6	10		5	10			
17		t_{on}	Turn ON Time		3	8		3	8		3	8	ns		
18		t_{off}	Turn OFF Time		3	8		3	8		3	8			

Note 1. Pulse test — 80µs pulse, 1% duty cycle. **Note 2.** Sample test.

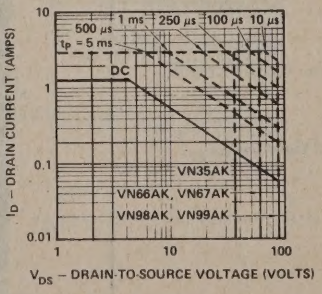
THERMAL RESPONSE



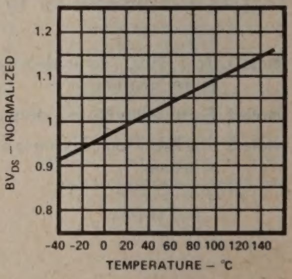
POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION Tc = 25°C



BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE



INTERSIL

VN40AF, VN67AF, VN89AF
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- Simple DC biasing
- Extended safe operating area
- Inherently temperature stable
- Reliable, low cost plastic package

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-source Voltage	
VN40AF	40V
VN67AF	60V
VN89AF	80V
Drain-gate Voltage	
VN40AF	40V
VN67AF	60V
VN89AF	80V
Continuous Drain Current (see note 1)	1.7A
Peak Drain Current (see note 2)	3.0A
Continuous Forward Gate Current	2.0mA
Peak-gate Forward Current	100mA
Peak-gate Reverse Current	100mA
Gate-source Forward (Zener) Voltage	+15V
Gate-source Reverse (Zener) Voltage	−0.3V
Thermal Resistance, Junction to Case	10.4°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	12W
Linear Derating Factor	96mW/°C
Operating Junction Temperature Range	−40 to +150°C
Storage Temperature Range	−40 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

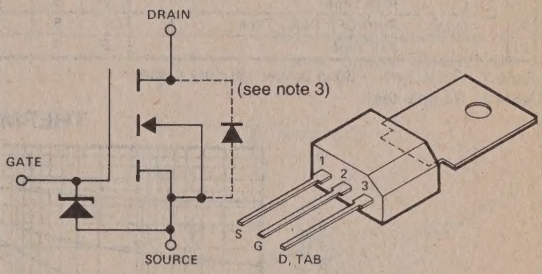
Note 2. Pulse width 80μsec, duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

APPLICATIONS

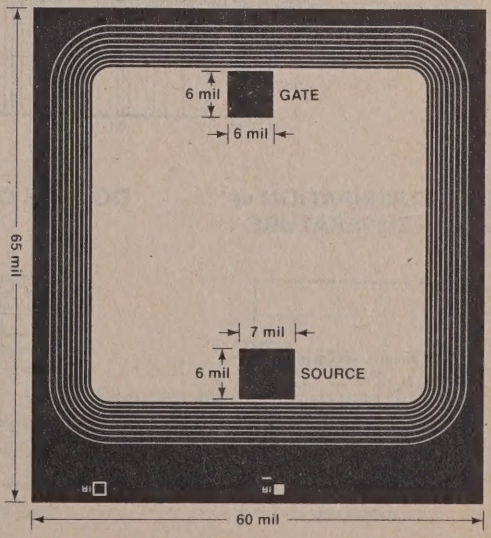
- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers
- DC motor controllers

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-202)



Body internally connected to source.
Drain common to tab.

CHIP TOPOGRAPHY

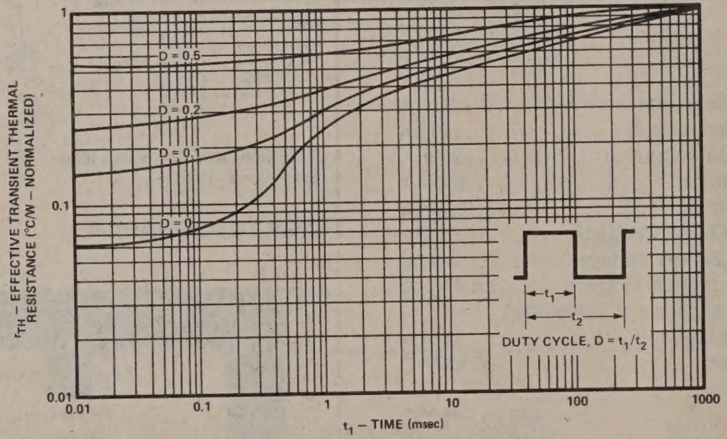


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

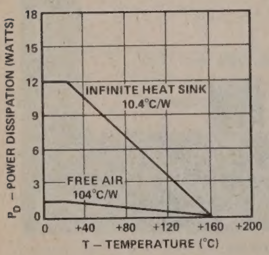
		CHARACTERISTIC		VN40AF			VN67AF			VN89AF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	V_{GS} = 0, I_D = 10μA	
2				40			60			80				V_{GS} = 0, I_D = 2.5mA	
3		$V_{GS(th)}$	Gate-Threshold Voltage	0.6	1.2		0.8	1.2		0.8	1.2			V_{DS} = V_{GS}, I_D = 1mA	
4		I_{GSS}	Gate-Body Leakage		0.01	10		0.01	10		0.01	10	μA	V_{GS} = 10V, V_{DS} = 0	
5						100			100			100		V_{GS} = 10V, V_{DS} = 0, T_A = 125°C (Note 2)	
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10		V_{DS} = Max. Rating, V_{GS} = 0	
7						100			100			100		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
8					100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	(Note 1)
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.3			0.4		V	V_{GS} = 5V, I_D = 0.1A	
11					1.0	2.0		1.0	1.7		1.4	1.9		V_{GS} = 5V, I_D = 0.3A	
12					1.0			1.0			1.3			V_{GS} = 10V, I_D = 0.5A	
13					2.2	5.0		2.2	3.5		2.2	4.5		V_{GS} = 10V, I_D = 1.0A	
14	DYNAMIC	g_m	Forward Transconductance		250			250			250		m℧	V_{DS} = 24V, I_D = 0.5A, f = 1KHz	(Note 2)
15		C_{iss}	Input Capacitance			50			50			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz	
16		C_{rss}	Reverse Transfer Capacitance			10			10			10			
17		C_{oss}	Common-Source Output Capacitance			50			50			50			
18		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5		2	5	ns		
19		t_r	Rise Time		2	5		2	5		2	5			
20		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5		2	5			
21		t_f	Fall Time		2	5		2	5		2	5			

Note 1. Pulse test — 80μs pulse, 1% duty cycle.
Note 2. Sample test.

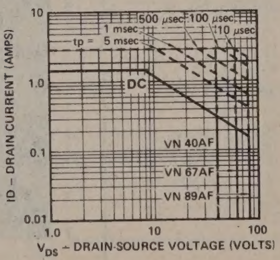
THERMAL RESPONSE



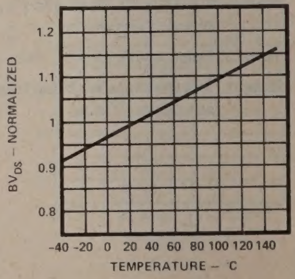
POWER DISSIPATION vs CASE TEMPERATURE



DC SAFE OPERATING REGION Tc = 25°C



BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE



VN46AF, VN66AF, VN88AF
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **Simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

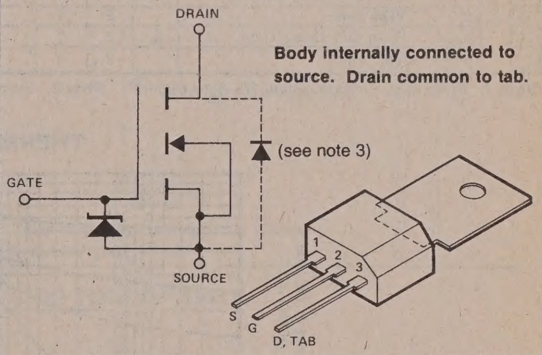
Drain-source Voltage	
VN46AF	40V
VN66AF	60V
VN88AF	80V
Drain-gate Voltage	
VN46AF	40V
VN66AF	60V
VN88AF	80V
Continuous Drain Current (see note 1)	1.7A
Peak Drain Current (see note 2)	3.0A
Continuous Forward Gate Current	2.0mA
Peak-gate Forward Current	100mA
Peak-gate Reverse Current	100mA
Gate-source Forward (Zener) Voltage	+15V
Gate-source Reverse (Zener) Voltage	−0.3V
Thermal Resistance, Junction to Case	10.4°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	12W
Linear Derating Factor	96mW/°C
Operating Junction Temperature Range	−40 to +150°C
Storage Temperature Range	−40 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

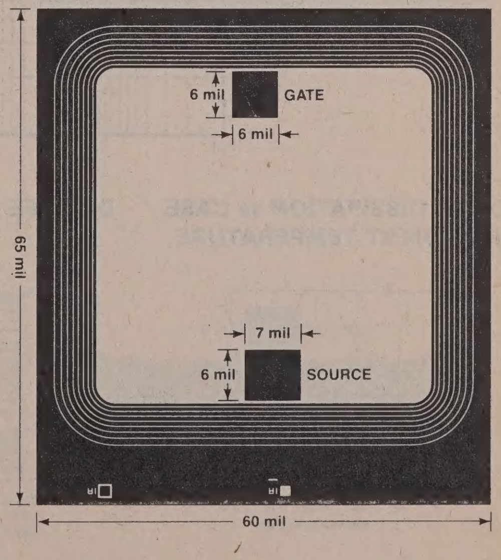
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-202)



Body internally connected to source. Drain common to tab.

CHIP TOPOGRAPHY



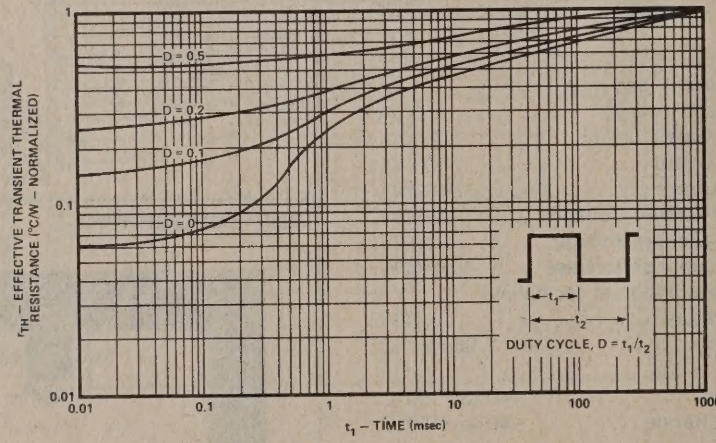
VN46AF, VN66AF, VN88AF

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

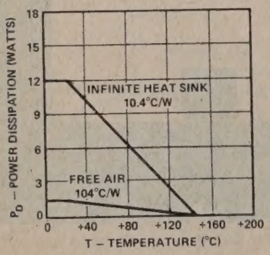
			CHARACTERISTIC	VN46AF			VN66AF			VN88AF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	$V_{GS} = 0$, $I_D = 10\mu A$	
2				40			60			80				$V_{GS} = 0$, $I_D = 2.5mA$	
3		$V_{GS(th)}$	Gate-Threshold Voltage	0.8	1.7		0.8	1.7		0.8	1.7			$V_{DS} = V_{GS}$, $I_D = 1mA$	
4		I_{GSS}	Gate-Body Leakage		0.01	10		0.01	10		0.01	10	μA	$V_{GS} = 10V$, $V_{DS} = 0$	
5						100			100			100		$V_{GS} = 10V$, $V_{DS} = 0$, $T_A = 125°C$ (Note 2)	
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10		V_{DS} = Max. Rating, $V_{GS} = 0$	
7						100			100			100		V_{DS} = 0.8 Max. Rating, $V_{GS} = 0$, $T_A = 125°C$ (Note 2)	
8					100			100			100		nA	$V_{DS} = 25V$, $V_{GS} = 0$	
9		$I_{D(on)}$	ON-State Drain Cufrent	1.0	2		1.0	2		1.0	2		A	$V_{DS} = 25V$, $V_{GS} = 10V$	(Note 1)
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.3			0.4		V	$V_{GS} = 5V$, $I_D = 0.1A$	
11					1.0	1.5		1.0	1.5		1.4	1.7		$V_{GS} = 5V$, $I_D = 0.3A$	
12					1.0			1.0			1.3			$V_{GS} = 10V$, $I_D = 0.5A$	
13					2.2	3.0		2.2	3.0		2.2	4.0		$V_{GS} = 10V$, $I_D = 1.0A$	
14	DYNAMIC	g_{fs}	Forward Transconductance	150	250		150	250		150	250		mΩ	$V_{DS} = 24V$, $I_D = 0.5A$, f = 1KHz	
15		C_{iss}	Input Capacitance			50			50			50	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0MHz	(Note 2)
16		C_{rss}	Reverse Transfer Capacitance			10			10			10			
17		C_{oss}	Common-Source Output Capacitance			50			50			50			
18		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5		2	5	ns		
19		t_r	Rise Time		2	5		2	5		2	5			
20		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5		2	5			
21		t_f	Fall Time		2	5		2	5		2	5			

Note 1. Pulse test — 80μs pulse, 1% duty cycle. **Note 2.** Sample test.

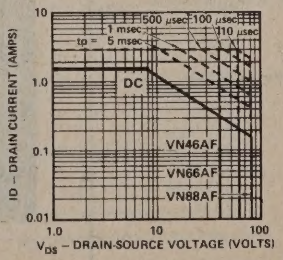
THERMAL RESPONSE



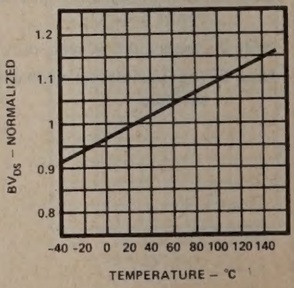
POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION Tc = 25°C



BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE



INTERSIL

IVN5000/1 AN Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high peak current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Inherent protection from thermal runaway
- Reliable, low cost plastic package

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-source Voltage	
IVN5000AND, IVN5001AND	40V
IVN5000ANE, IVN5001ANE	60V
IVN5000ANF, IVN5001ANF	80V
Drain-gate Voltage	
IVN5000AND, IVN5001AND	40V
IVN5000ANE, IVN5001ANE	60V
IVN5000ANF, IVN5001ANF	80V
Continuous Drain Current (see note 1)	0.7A
Peak Drain Current (see note 2)	2.0A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	−30V
Thermal Resistance, Junction to Case	62.5°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	2.0W
Linear Derating Factor	16mW/°C
Operating Junction Temperature Range	−40 to +150°C
Storage Temperature Range	−40 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

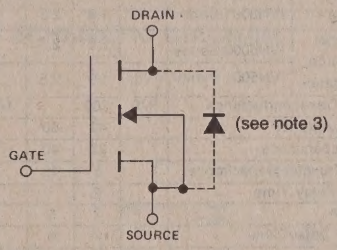
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

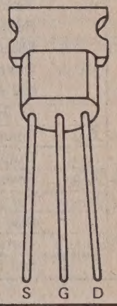
APPLICATIONS

- LED and lamp drivers
- High gain, wide-band amplifiers
- High speed switches
- Line drivers
- Logic buffers
- Pulse amplifiers

SCHEMATIC DIAGRAM

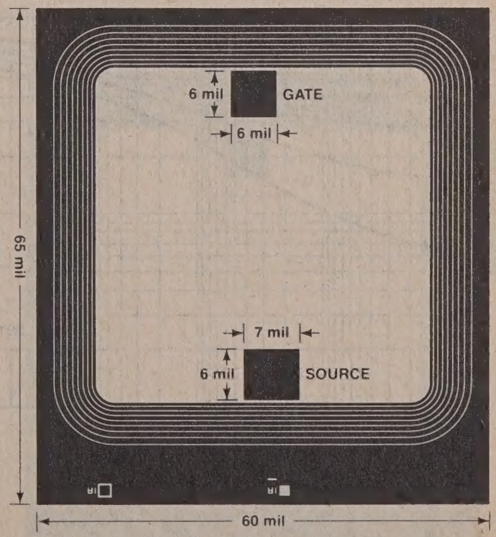
(OUTLINE DWG. TO-237)





Body internally connected to source
Drain common to tab

CHIP TOPOGRAPHY

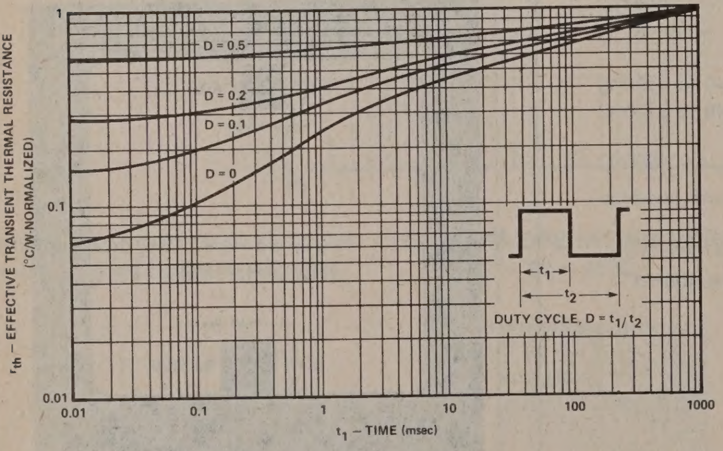


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), $V_{BS} = 0$

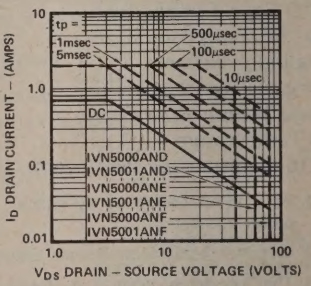
		CHARACTERISTICS			IVN5000AND IVN5001AND			IVN5000ANE IVN5001ANE			IVN5000ANF INV5001ANF			UNIT	TEST CONDITIONS		
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage		40			60			80			V	$V_{GS} = 0$, $I_D = 10\mu A$		
2		$V_{GS(th)}$	Gate Threshold Voltage	IVN5000 Series	0.8		2.0	0.8		2.0	0.8		2.0		$V_{DS} = V_{GS}$, $I_D = 1mA$		
3				IVN5001 Series	0.8		3.6	0.8		3.6	0.8		3.6				
4		I_{GSS}	Gate-Body Leakage			0.1	10		0.1	10		0.1	10	nA	$V_{GS} = 15V$, $V_{DS} = 0$		
5							50			50			50		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = +125°C$		
6		I_{DSS}	Zero Gate Voltage Drain Current				10			10			10	µA	V_{DS} = Max. Rating, $V_{GS} = 0$		
7							500			500			500		V_{DS} = 0.80 Max. Rating, $V_{GS} = 0$, $T_A = +125°C$		
8						20			20			20		nA	$V_{DS} = 24V$, $V_{GS} = 0$		
9		$I_{D(on)}$	ON-State Drain Current	IVN5000 Series	1.0	1.9		1.0	1.9		1.0	1.9		A	$V_{DS} = 24V$, $V_{GS} = 10V$		(Note 1)
10				IVN5001 Series	1.0	1.9		1.0	1.9		1.0	1.9			$V_{DS} = 24V$, $V_{GS} = 12V$		
11		$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5000AND IVN5000ANE IVN5000ANF		1.5			1.5			1.5		V	$V_{GS} = 5V$, $I_D = 0.3A$		
12						2.0	2.5		2.0	2.5		2.0	2.5		$V_{GS} = 10V$, $I_D = 1.0A$		
13				IVN5001AND INV5001ANE IVN5001ANF		1.2			1.2			1.2			$V_{GS} = 7V$, $I_D = 0.3A$		
14						1.9	2.5		1.9	2.5		1.9	2.5		$V_{GS} = 12V$, $I_D = 1.0A$		
15		$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5	Ω	$V_{GS} = 10V$	$I_D = 1.0A$	
16				IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5		$V_{GS} = 12V$		
17	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5		$V_{GS} = 10V$	$I_D = 1.0A$ f = 1KHz	
18				IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5		$V_{GS} = 12V$		
19		g_{fs}	Forward Transconductance		170	280		170	280		170	280		mʊ	$V_{DS} = 24V$, $I_D = 0.5A$, f = 1KHz		
20		C_{iss}	Input Capacitance			40	50		40	50		40	50	pF	$V_{DS} = 24V$, $V_{GS} = 0$ f = 1MHz		(Note 2)
21		C_{oss}	Output Capacitance			27	40		27	40		27	40				
22		C_{rss}	Reverse Transfer Capacitance			6	10		6	10		6	10				
23		$t_{d(on)}$	Turn-ON Delay Time			2	5		2	5		2	5	ns	See Switching Times Test Circuit, page 2-42.		(Note 2)
24		t_r	Rise Time			2	5		2	5		2	5				
25		$t_{d(off)}$	Turn-OFF Delay Time			2	5		2	5		2	5				
26		t_f	Fall Time			2	5		2	5		2	5				

Note 1. Pulse test — 80µsec, 1% duty cycle.
Note 2. Sample test.

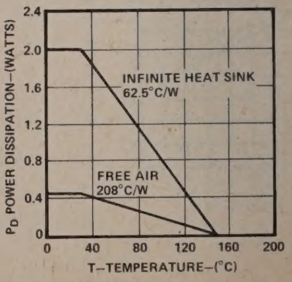
THERMAL RESPONSE



DC SAFE OPERATING REGION
Tc = 25°C



POWER DISSIPATION DERATING



Note: For other 5000 family characteristic curves, see page 2-41.

IVN5000/1 BN Series n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high peak current switching
- Inherent current sharing capability when paralleled
- Interfaces directly with CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Inherent protection from thermal runaway
- Reliable, low cost plastic package

These devices are Non-Zener equivalents of the VN40AF Series:

Original Type No. Zener Protected	Equiv. Type No. Non-Zener
VN40AF	IVN5001BND
VN46AF	IVN5001BND
VN66AF	IVN5001BNE
VN67AF	IVN5001BNE
VN88AF	IVN5001BNF
VN89AF	IVN5001BNF

ABSOLUTE MAXIMUM RATINGS

(25° C unless otherwise noted)

Drain-source Voltage
  IVN5000BND, IVN5001BND 40V
  IVN5000BNE, IVN5001BNE 60V
  IVN5000BNF, IVN5001BNF 80V
Drain-gate Voltage
  IVN5000BND, IVN5001BND 40V
  IVN5000BNE, IVN5001BNE 60V
  IVN5000BNF, IVN5001BNF 80V
Continuous Drain Current (see note 1) 1.7A
Peak Drain Current (see note 2)................ 3.0A
Gate-source Forward Voltage .... +30V
Gate-source Reverse Voltage .... -30V
Thermal Resistance, Junction to Case .... 10.4° C/W
Continuous Device Dissipation at (or below)
  25° C Case Temperature 12W
Linear Derating Factor.................. 96mW/° C
Operating Junction
  Temperature Range................-40 to +150° C
Storage Temperature Range..........-40 to +150° C
Lead Temperature
  (1/16 in. from case for 10 sec)............ +300° C

Note 1. T_C = 25° C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

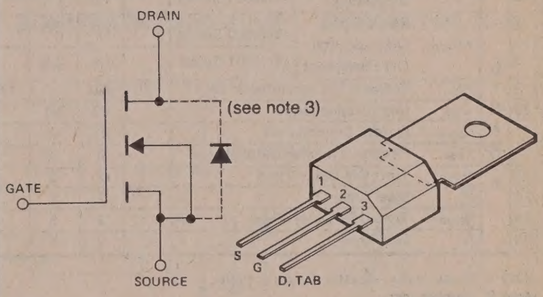
Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

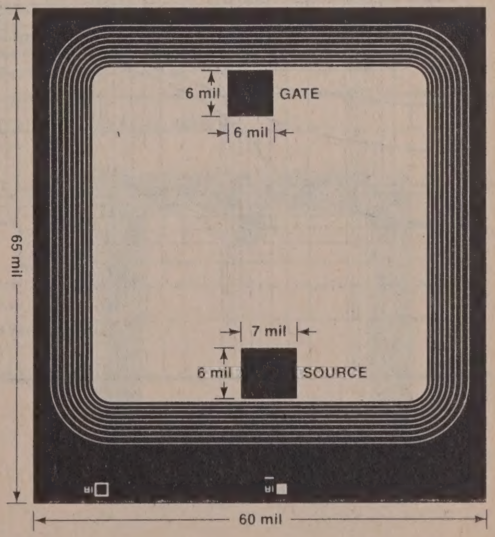
APPLICATIONS

- Switching power supplies
- DC to DC inverters
- High gain, broad-band VHF/UHF Amplifiers
- Line drivers
- Logic buffers
- Pulse amplifiers

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-202)



CHIP TOPOGRAPHY

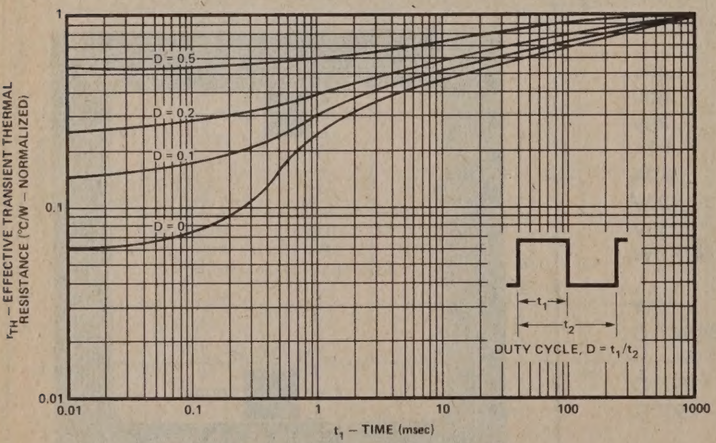


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), $V_{BS} = 0$

		CHARACTERISTICS			IVN5000BND IVN5001BND			IVN5000BNE IVN5001BNE			IVN5000BNF IVN5001BNF			UNIT	TEST CONDITIONS		
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage		40			60			80			V	$V_{GS} = 0$, $I_D = 10\mu A$		
2		$V_{GS(th)}$	Gate Threshold Voltage	IVN5000 Series	0.8		2.0	0.8		2.0	0.8		2.0		$V_{DS} = V_{GS}$, $I_D = 1mA$		
3				IVN5001 Series	0.8		3.6	0.8		3.6	0.8		3.6				
4		I_{GSS}	Gate-Body Leakage			0.1	10		0.1	10		0.1	10	nA	$V_{GS} = 15V$, $V_{DS} = 0$		
5							50			50			50		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = +125°C$		
6		I_{DSS}	Zero Gate Voltage Drain Current				10			10			10	μA	V_{DS} = Max. Rating, $V_{GS} = 0$		
7							500			500			500		V_{DS} = 0.80 Max. Rating, $V_{GS} = 0$, $T_A = +125°C$		
8						20			20			20		nA	$V_{DS} = 24V$, $V_{GS} = 0$		
9		$I_{D(on)}$	ON-State Drain Current	IVN5000 Series	1.0	1.9		1.0	1.9		1.0	1.9		A	$V_{DS} = 24V$, $V_{GS} = 10V$		(Note 1)
10				IVN5001 Series	1.0	1.9		1.0	1.9		1.0	1.9			$V_{DS} = 24V$, $V_{GS} = 12V$		
11		$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5000BND IVN5000BNE IVN5000BNF		1.5			1.5			1.5		V	$V_{GS} = 5V$, $I_D = 0.3A$		
12						2.0	2.5		2.0	2.5		2.0	2.5		$V_{GS} = 10V$, $I_D = 1.0A$		
13				IVN5001BND IVN5001BNE IVN5001BNF		1.2			1.2			1.2			$V_{GS} = 7V$, $I_D = 0.3A$		
14						1.9	2.5		1.9	2.5		1.9	2.5		$V_{GS} = 12V$, $I_D = 1.0A$		
15		$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5	Ω	$V_{GS} = 10V$	$I_D = 1.0A$	
16				IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5		$V_{GS} = 12V$		
17	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5		$V_{GS} = 10V$	$I_D = 1.0A$ f = 1KHz	
18				IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5		$V_{GS} = 12V$		
19		g_{fs}	Forward Transconductance		170	280		170	280		170	280		mΩ	$V_{DS} = 24V$, $I_D = 0.5A$, f = 1KHz		
20		C_{iss}	Input Capacitance			40	50		40	50		40	50	pF	$V_{DS} = 24V$, $V_{GS} = 0$ f = 1MHz		(Note 2)
21		C_{oss}	Output Capacitance			27	40		27	40		27	40				
22		C_{rss}	Reverse Transfer Capacitance			6	10		6	10		6	10				
23		$t_{d(on)}$	Turn-ON Delay Time			2	5		2	5		2	5	ns	See Switching Times Test Circuit, page 2-42.		(Note 2)
24		t_r	Rise Time			2	5		2	5		2	5				
25		$t_{d(off)}$	Turn-OFF Delay Time			2	5		2	5		2	5				
26		t_f	Fall Time			2	5		2	5		2	5				

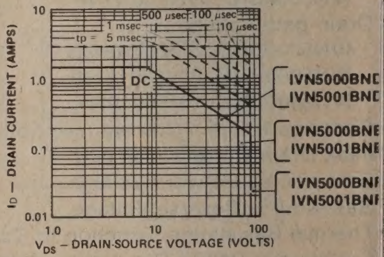
Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

THERMAL RESPONSE

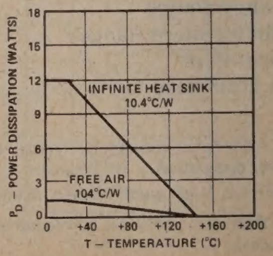


DC SAFE OPERATING REGION

T_C = 25° C



POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



Note: For other 5000 family characteristic curves, see page 2-41.

INTERSIL

IVN5000/1 SN Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high current switching
- High gain-bandwidth product
- Inherently temperature stable
- Extended Safe Operating Area
- Simple DC biasing
- Requires almost zero current drive
- Small hermetic package

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- High gain, broad-band VHF/UHF Amplifiers
- Line drivers
- Logic buffers
- Pulse amplifiers
- Motor Controls

ABSOLUTE MAXIMUM RATINGS
(T_A = 25° C unless otherwise noted)

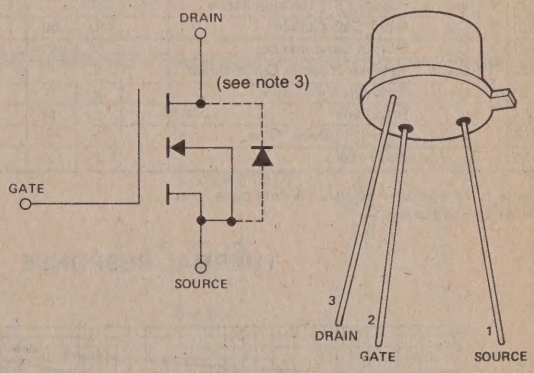
Drain-source Voltage	
IVN5000SND, IVN5001SND	40V
IVN5000SNE, IVN5001SNE	60V
IVN5000SNF, IVN5001SNF	80V
Drain-gate Voltage	
IVN5000SND, IVN5001SND	40V
IVN5000SNE, IVN5001SNE	60V
IVN5000SNF, IVN5001SNF	80V
Continuous Drain Current (see note 1)	0.9A
Peak Drain Current (see note 2)	3.0A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	−30V
Thermal Resistance, Junction to Case	40°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	3.13W
Linear Derating Factor	25mW/°C
Operating Junction Temperature Range	−55 to +150°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

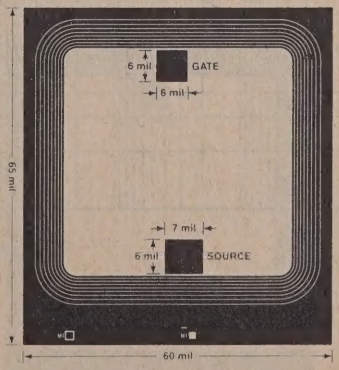
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-52)



Body internally connected to source
Drain common to case

CHIP TOPOGRAPHY



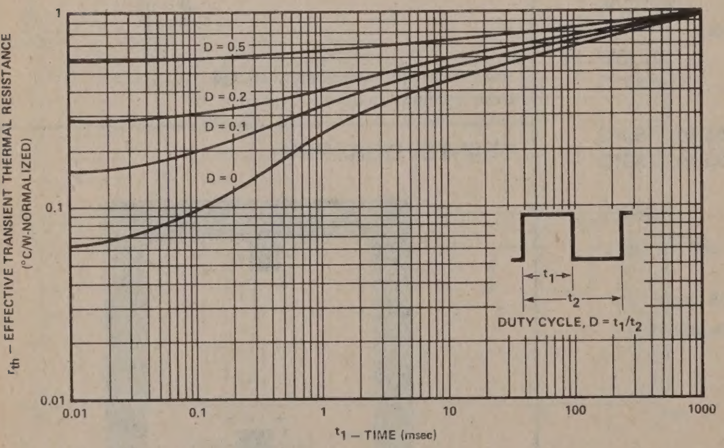
IVN5000/1 SN Series

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0

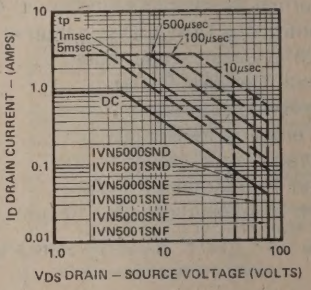
CHARACTERISTICS					IVN5000SND IVN5001SND			IVN5000SNE IVN5001SNE			IVN5000SNF INV5001SNF			UNIT	TEST CONDITIONS		
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage		40			60			80			V	V_{GS} = 0, I_D = 10μA		
2		$V_{GS(th)}$	Gate Threshold Voltage	IVN5000 Series	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA		
3				IVN5001 Series	0.8		3.6	0.8		3.6	0.8		3.6				
4		I_{GSS}	Gate-Body Leakage			0.1	10		0.1	10		0.1	10	nA	V_{GS} = 15V, V_{DS} = 0		
5							50			50			50		V_{GS} = 15V, V_{DS} = 0, T_A = +125°C		
6		I_{DSS}	Zero Gate Voltage Drain Current				10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0		
7							500			500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C		
8						20			20			20		nA	V_{DS} = 24V, V_{GS} = 0		
9		$I_{D(on)}$	ON-State Drain Current	IVN5000 Series	1.0	1.9		1.0	1.9		1.0	1.9		A	V_{DS} = 24V, V_{GS} = 10V		(Note 1)
10				IVN5001 Series	1.0	1.9		1.0	1.9		1.0	1.9			V_{DS} = 24V, V_{GS} = 12V		
11		$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5000SND IVN5000SNE IVN5000SNF		1.5			1.5			1.5		V	V_{GS} = 5V, I_D = 0.3A		
12						2.0	2.5		2.0	2.5		2.0	2.5		V_{GS} = 10V, I_D = 1.0A		
13				IVN5001SND INV5001SNE IVN5001SNF		1.2			1.2			1.2			V_{GS} = 7V, I_D = 0.3A		
14						1.9	2.5		1.9	2.5		1.9	2.5		V_{GS} = 12V, I_D = 1.0A		
15		$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5	Ω	V_{GS} = 10V	I_D = 1.0A	
16				IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5		V_{GS} = 12V		
17	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5		V_{GS} = 10V	I_D = 1.0A f = 1KHz	
18				IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5		V_{GS} = 12V		
19		g_{fs}	Forward Transconductance		170	280		170	280		170	280		mΩ	V_{DS} = 24V, I_D = 0.5A, f = 1KHz		
20		C_{iss}	Input Capacitance			40	50		40	50		40	50	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz		(Note 2)
21		C_{oss}	Output Capacitance			27	40		27	40		27	40				
22		C_{rss}	Reverse Transfer Capacitance			6	10		6	10		6	10				
23		$t_{d(on)}$	Turn-ON Delay Time			2	5		2	5		2	5	ns	See Switching Times Test Circuit, page 2-42.		(Note 2)
24		t_r	Rise Time			2	5		2	5		2	5				
25		$t_{d(off)}$	Turn-OFF Delay Time			2	5		2	5		2	5				
26		t_f	Fall Time			2	5		2	5		2	5				

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

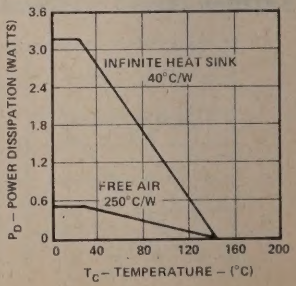
THERMAL RESPONSE



DC SAFE OPERATING REGION T_C = 25°C



POWER DISSIPATION DERATING



Note: For other 5000 family characteristic curves, see page 2-41.

INTERSIL

IVN5000/1 TN Series n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high current switching**
- **High gain-bandwidth product**
- **Inherently temperature stable**
- **Extended safe operating area**
- **Simple DC Biasing**
- **Requires almost zero current drive**

APPLICATIONS

- **High current analog switches**
- **RF power amplifiers**
- **Laser diode pulsers**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25° C unless otherwise noted)

Drain-source Voltage
IVN5000TND, IVN5001TND 40V
IVN5000TNE, IVN5001TNE 60V
IVN5000TNF, IVN5001TNF 80V
IVN5000TNG, IVN5001TNG 90V

Drain-gate Voltage
IVN5000TND, IVN5001TND 40V
IVN5000TNE, IVN5001TNE 60V
IVN5000TNF, IVN5001TNF 80V
IVN5000TNG, IVN5001TNG 90V

Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2)............... 3.0A
Gate-source Forward Voltage .... +30V
Gate-source Reverse Voltage .... -30V
Thermal Resistance, Junction to Case .... 20° C/W
Continuous Device Dissipation at (or below)
25° C Case Temperature 6.25W
Linear Derating Factor.................. 50mW/° C
Operating Junction
Temperature Range................ —55 to +150° C
Storage Temperature Range......... —55 to +150° C
Lead Temperature
(1/16 in. from case for 10 sec)............ +300° C

Note 1. T_C = 25° C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

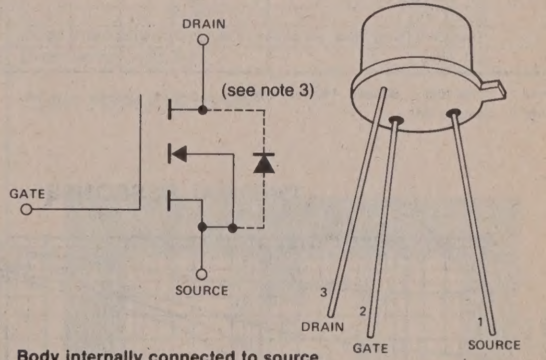
Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

These devices are non-zener improved equivalents of the following series.

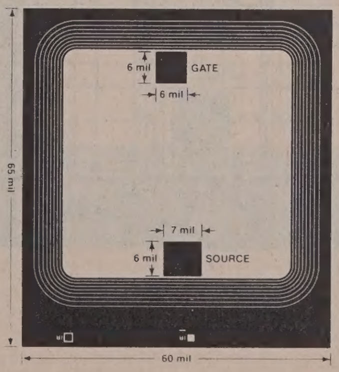
Original Type No. Zener Protected	Original Type No. No Zener Protection	Intersil Equivalent Type No. Non-Zener or Preferred Replacement
VN30AB		IVN5001TND
VN35AB		IVN5001TND
	VN35AK	IVN5000TND
	VN66AK	IVN5000TNE
VN67AB		IVN5001TNE
	VN67AK	IVN5000TNE
VN89AB		IVN5001TNF
VN90AB		IVN5001TNG
	VN98AK	IVN5000TNG
	VN99AK	IVN5000TNG
2N6659		IVN5000TND
2N6660		IVN5000TNE
2N6661		IVN5000TNG

SCHEMATIC DIAGRAM **(OUTLINE DWG. TO-39)**



Body internally connected to source.
Drain common to case.

CHIP TOPOGRAPHY

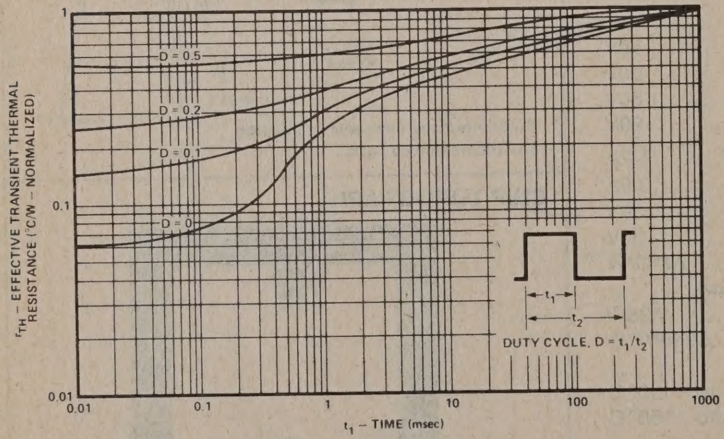


ELECTRICAL CHARACTERISTICS (T_A = 25° C unless otherwise noted), V_{BS} = 0

CHARACTERISTICS			IVN5000TND INV5001TND			IVN5000TNE IVN5001TNE			IVN5000TNF IVN5001TNF			IVN5000TNG IVN5001TNG			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
STATIC																	
BV_{DSS}	Drain-Source Breakdown Voltage		40			60			80			90			V	V_{GS} = 0, I_D = 10 μA	
$V_{GS(th)}$	Gate Threshold Voltage	IVN5000 Series	0.8		2.0	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA	
		IVN5001 Series	0.8		3.6	0.8		3.6	0.8		3.6	0.8		3.6			
I_{GSS}	Gate-Body Leakage			0.1	10		0.1	10		0.1	10		0.1	10	nA	V_{GS} = 15V, V_{DS} = 0	
					50			50			50			50		V_{GS} = 15V, V_{DS} = 0, T_A = +125° C	
I_{DSS}	Zero Gate Voltage Drain Current				10			10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
					500			500			500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125° C	
				20			20			20			20		nA	V_{DS} = 24V, V_{GS} = 0	
$I_{D(on)}$	ON-State Drain Current	IVN5000 Series	1.0	1.9		1.0	1.9		1.0	1.9		1.0	1.9		A	V_{DS} = 24V, V_{GS} = 10V[1]	
		IVN5001 Series	1.0	1.9		1.0	1.9		1.0	1.9		1.0	1.9			V_{DS} = 24V, V_{GS} = 12V[1]	
$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5000 Series		1.5			1.5			1.5			1.5		V	V_{GS} = 5V, I_D = 0.3A[1]	
				2.0	2.5		2.0	2.5		2.0	2.5		2.0	2.5		V_{GS} = 10V, I_D = 1.0A[1]	
		IVN5001 Series		1.2			1.2			1.2			1.2			V_{GS} = 7V, I_D = 0.3A[1]	
				1.9	2.5		1.9	2.5		1.9	2.5		1.9	2.5		V_{GS} = 12V, I_D = 1.0A[1]	
$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5		2.0	2.5	Ω	V_{GS} = 10V	I_D = 1.0A[1]
		IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5		1.9	2.5		V_{GS} = 12V	
DYNAMIC																	
$r_{DS(on)}$	Small-Signal Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5		2.0	2.5	Ω	V_{GS} = 10V	I_D = 1.0A[1] f = 1KHz
		IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5		1.9	2.5		V_{GS} = 12V	
g_{fs}	Forward Transconductance		170	280		170	280		170	280		170	280		mΩ	V_{DS}=24V, I_D=0.5A, f =1KHz[1]	
C_{iss}	Input Capacitance			40	50		40	50		40	50		40	50	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz (see note 2)	
C_{oss}	Output Capacitance			27	40		27	40		27	40		27	40			
C_{rss}	Reverse Transfer Capacitance			6	10		6	10		6	10		6	10			
$t_{D(on)}$	Turn-ON Delay Time			2	5		2	5		2	5		2	5	ns	See Switching Times Test Circuit, page 2-42 (see note 2)	
t_r	Rise Time			2	5		2	5		2	5		2	5			
$t_{D(off)}$	Turn-OFF Delay Time			2	5		2	5		2	5		2	5			
t_f	Fall Time			2	5		2	5		2	5		2	5			

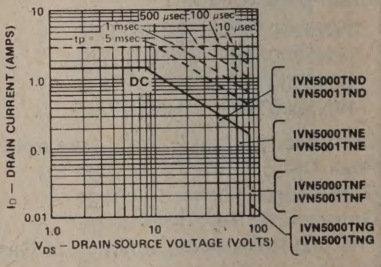
Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

THERMAL RESPONSE

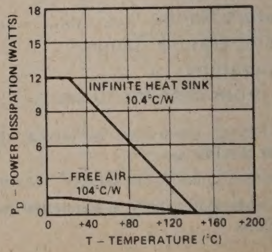


DC SAFE OPERATING REGION

T_C = 25° C



POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



Note: For other 5000 family characteristic curves, see page 2-41.

INTERSIL

IVN5001 AZ Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high peak current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Inherent protection from thermal runaway
- Reliable, low cost plastic package

ABSOLUTE MAXIMUM RATINGS
(T_A = 25° C unless otherwise noted)

Drain-source Voltage	
IVN5001 AZE	60V
IVN5001 AZF	80V
Drain-gate Voltage	
IVN5001 AZE	60V
IVN5001 AZF	80V
Continuous Drain Current (see note 1)	0.5A
Peak Drain Current (see note 2)	2.0A
Gate-source Forward Voltage	+15V
Gate-source Reverse Voltage	−0.3V
Thermal Resistance, Junction to Case	62.5°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	2.0W
Linear Derating Factor	16mW/°C
Operating Junction Temperature Range	−40 to +150°C
Storage Temperature Range	−40 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

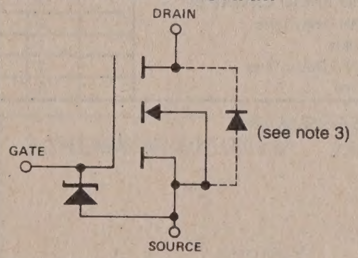
Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

APPLICATIONS

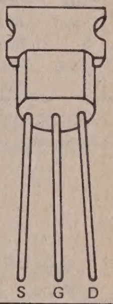
- LED and lamp drivers
- High gain, wide-band amplifiers
- High speed switches
- Line drivers
- Logic buffers
- Pulse amplifiers

SCHEMATIC DIAGRAM

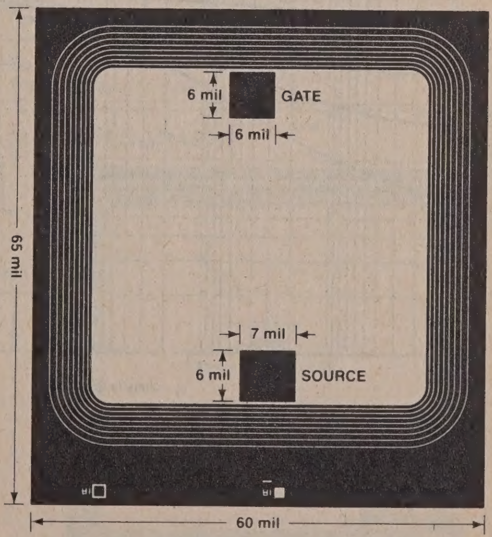


Body internally connected to source
Drain common to tab

(OUTLINE DWG. TO-237)



CHIP TOPOGRAPHY



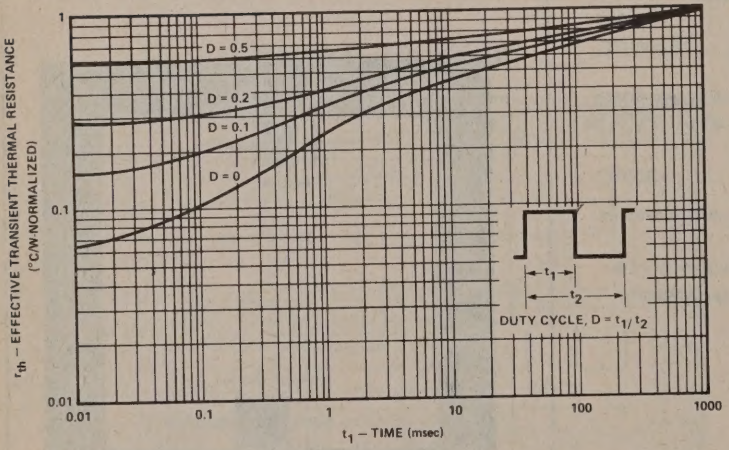
IVN5001 AZ Series

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), $V_{BS} = 0$

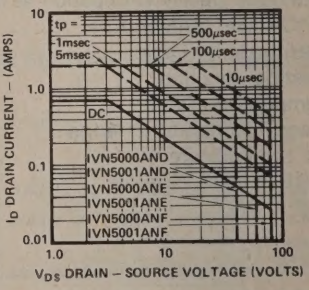
			CHARACTERISTICS	IVN5001 AZE			IVN5001 AZF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	60			80				$V_{GS} = 0$, $I_D = 10\mu A$	
2		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	0.8		2.5	V	$V_{DS} = V_{GS}$, $I_D = 1mA$	
3		I_{GSS}	Gate-Body Leakage		0.1	100		0.1	100	nA	$V_{GS} = 15V$, $V_{DS} = 0$	
4						500			500		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = +125°C$	
5		I_{DSS}	Zero Gate Voltage Drain Current			10			10	μA	V_{DS} = Max. Rating, $V_{GS} = 0$	
6						500			500		V_{DS} = 0.80 Max. Rating, $V_{GS} = 0$, $T_A = +125°C$	
7					20			20		nA	$V_{DS} = 24V$, $V_{GS} = 0$	(Note 1)
8		$I_{D(on)}$	ON-State Drain Current	1.0	1.9		1.0	1.9		A	$V_{DS} = 24V$, $V_{GS} = 12$	
9		$V_{DS(on)}$	Drain-Source Saturation Voltage		1.2			1.2		V	$V_{GS} = 7V$, $I_D = 0.3A$	
10					1.9	3.0		1.9	3.0		$V_{GS} = 12V$, $I_D = 1.0A$	
11		$r_{DS(on)}$	Static Drain-Source ON Resistance		1.9	3.0		1.9	3.0		$V_{GS} = 12V$, $I_D = 1.0A$	
12		$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance		1.9	3.0		1.9	3.0	Ω	$V_{GS} = 12V$, $I_D = 1.0A$, f = 1KHz	
13	DYNAMIC	g_{fs}	Forward Transconductance	170	280		170	280		m℧	$V_{DS} = 24V$, $I_D = 0.5A$, f = 1KHz	
14		C_{iss}	Input Capacitance		40	50		40	50	pF	$V_{DS} = 24V$, $V_{GS} = 0$ f = 1MHz	(Note 2)
15		C_{oss}	Output Capacitance		27	40		27	40			
16		C_{rss}	Reverse Transfer Capacitance		6	10		6	10			
17		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5	ns	See Switching Times Test Circuit, page 2-42	(Note 2)
18		t_r	Rise Time		2	5		2	5			
19		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5			
20		t_f	Fall Time		2	5		2	5			

NOTES: 1. Pulse test –80 μs pulse, 1% duty cycle.
2. Sample Test.

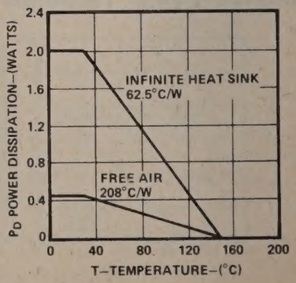
THERMAL RESPONSE



DC SAFE OPERATING REGION $T_C = 25°C$



POWER DISSIPATION DERATING



Note: For other 5000 family characteristic curves, see page 2-41.

INTERSIL

IVN5200/1 HN Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- Logic buffers
- Line drivers
- Motor controllers
- Power amplifiers

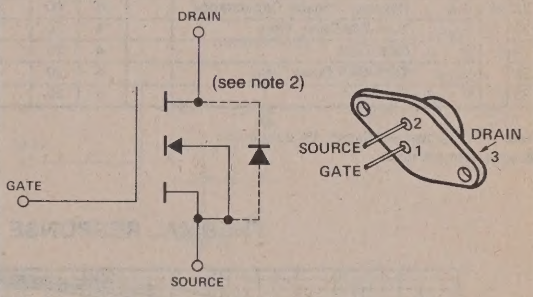
ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-source Voltage	
IVN5200HND, IVN5201HND	40V
IVN5200HNE, IVN5201HNE	60V
IVN5200HNF, IVN5201HNF	80V
Drain-gate Voltage	
IVN5200HND, IVN5201HND	40V
IVN5200HNE, IVN5201HNE	60V
IVN5200HNF, IVN5201HNF	80V
Continuous Drain Current	5.0A
Peak Drain Current (see note 1)	12A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	–30V
Thermal Resistance, Junction to Case	4.17°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	30W
Linear Derating Factor	240mW/°C
Operating Junction Temperature Range	–55 to +150°C
Storage Temperature Range	–55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. Maximum pulse width 80μsec, maximum duty cycle 1.0%

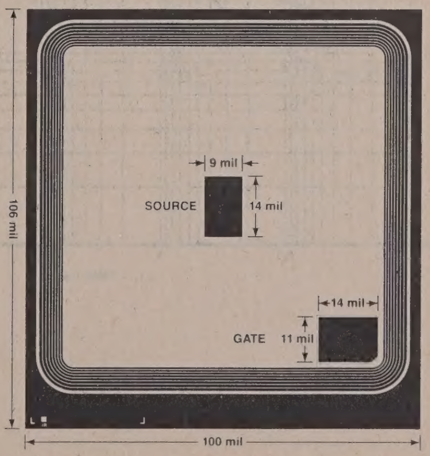
Note 2. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-66)



Body internally connected to source.
Drain common to case.

CHIP TOPOGRAPHY

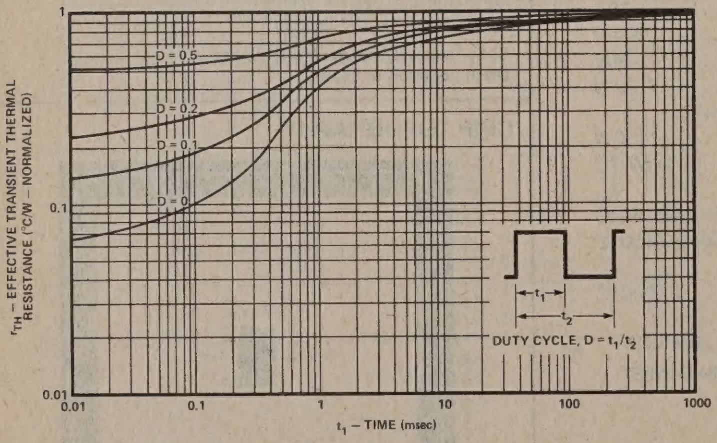


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), $V_{BS} = 0$

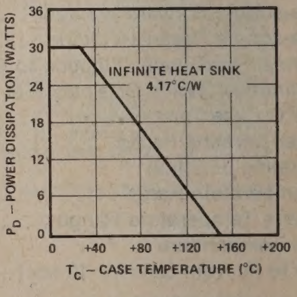
		CHARACTERISTICS			IVN5200HND IVN5201HND MIN	TYP	MAX	IVN5200HNE IVN5201HNE MIN	TYP	MAX	IVN5200HNF INV5201HNF MIN	TYP	MAX	UNIT	TEST CONDITIONS		
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage		40			60			80			V	$V_{GS} = 0$, $I_D = 100\mu A$		
2		$V_{GS(th)}$	Gate Threshold Voltage	IVN5200 Series	0.8		2.0	0.8		2.0	0.8		2.0		$V_{DS} = V_{GS}$, $I_D = 5mA$		
3				IVN5201 Series	0.8		3.6	0.8		3.6	0.8		3.6				
4		I_{GSS}	Gate-Body Leakage			0.2	20		0.2	20		0.2	20	nA	$V_{GS} = 12V$, $V_{DS} = 0$		
5							100			100			100		$V_{GS} = 12V$, $V_{DS} = 0$, $T_A = +125°C$		
6		I_{DSS}	Zero Gate Voltage Drain Current				100			100			100	μA	V_{DS} = Max. Rating, $V_{GS} = 0$		
7							5.0			5.0			5.0	mA	V_{DS} = 0.80 Max. Rating, $V_{GS} = 0$, $T_A = +125°C$		
8						100			100			100		nA	$V_{DS} = 24V$, $V_{GS} = 0$		
9		$I_{D(on)}$	ON-State Drain Current	IVN5200 Series	5.0	10		5.0	10		5.0	10		A	$V_{DS} = 24V$, $V_{GS} = 10V$		(Note 1)
10				IVN5201 Series	5.0	10		5.0	10		5.0	10			$V_{DS} = 24V$, $V_{GS} = 12V$		
11		$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5200HND IVN5200HNE IVN5200HNF		1.5			1.5			1.5		V	$V_{GS} = 5V$, $I_D = 2.0A$		
12						1.9	2.5		1.9	2.5		1.9	2.5		$V_{GS} = 10V$, $I_D = 5.0A$		
13				IVN5201HND INV5201HNE IVN5201HNF		1.2			1.2			1.2			$V_{GS} = 7V$, $I_D = 2.0A$		
14						1.8	2.5		1.8	2.5		1.8	2.5		$V_{GS} = 12V$, $I_D = 5.0A$		
15		$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50	Ω	$V_{GS} = 10V$	$I_D = 5.0A$	
16				IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50		$V_{GS} = 12V$		
17	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50		$V_{GS} = 10V$	$I_D = 5.0A$ f = 1KHz	
18				IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50		$V_{GS} = 12V$		
19		g_{fs}	Forward Transconductance		1.0	1.8		1.0	1.8		1.0	1.8		mho	$V_{DS} = 24V$, $I_D = 5.0A$, f = 1KHz		
20		C_{iss}	Input Capacitance			210	250		210	250		210	250	pF	$V_{DS} = 24V$, $V_{GS} = 0$ f = 1MHz		(Note 2)
21		C_{oss}	Output Capacitance			160	200		160	200		160	200				
22		C_{rss}	Reverse Transfer Capacitance			45	60		45	60		45	60				
23		$t_{d(on)}$	Turn-ON Delay Time			4	20		4	20		4	20	ns	$I_D = 4.0A$ See Switching Times Test Circuit, page 2-44.		(Note 2)
24		t_r	Rise Time			4	20		4	20		4	20				
25		$t_{d(off)}$	Turn-OFF Delay Time			4	20		4	20		4	20				
26		t_f	Fall Time			4	20		4	20		4	20				

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

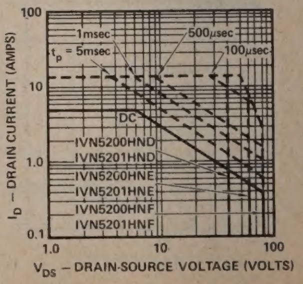
THERMAL RESPONSE



POWER DISSIPATION vs CASE TEMPERATURE



DC SAFE OPERATING REGION
Tc = 25°C



Note: For other 5200 family characteristic curves, see page 2-43.

IVN5200/1 KN Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high current switching
- Inherent current sharing capability when paralleled
- Extremely low drive currents
- Simple, straight-forward DC biasing
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current logic
- High current line drivers
- Motor controllers
- Power amplifiers

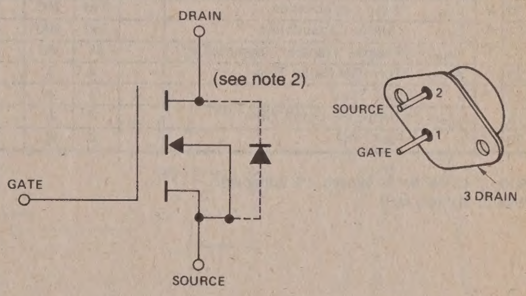
ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-source Voltage	
IVN5200KND, IVN5201KND	40V
IVN5200KNE, IVN5201KNE	60V
IVN5200KNF, IVN5201KNF	80V
Drain-gate Voltage	
IVN5200KND, IVN5201KND	40V
IVN5200KNE, IVN5201KNE	60V
IVN5200KNF, IVN5201KNF	80V
Continuous Drain Current	5.0A
Peak Drain Current (see note 1)	12A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	−30V
Thermal Resistance, Junction to Case	2.5°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	50W
Linear Derating Factor	400mW/°C
Operating Junction Temperature Range	−55 to +150°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. Maximum pulse width 80μsec, maximum duty cycle 1.0%

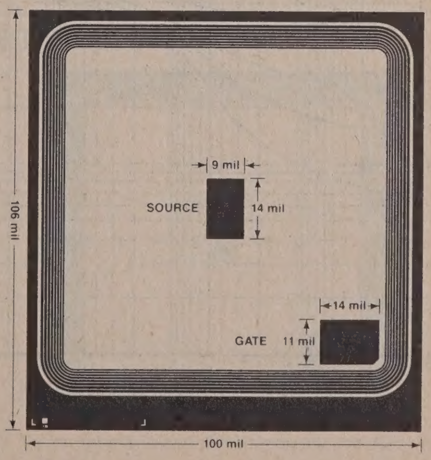
Note 2. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-3)



Body internally connected to source
Drain common to case

CHIP TOPOGRAPHY

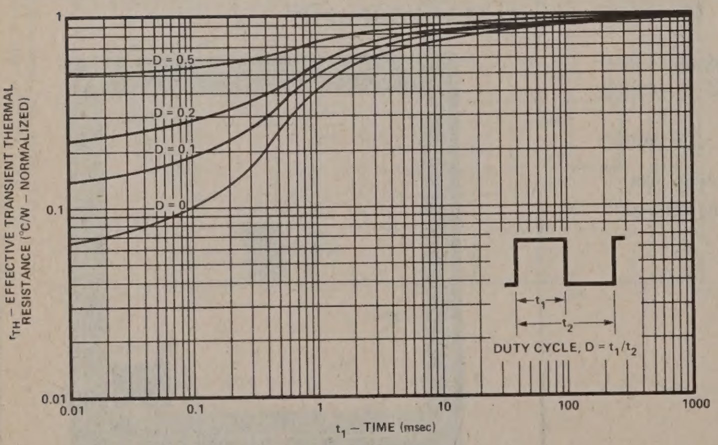


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), $V_{BS} = 0$

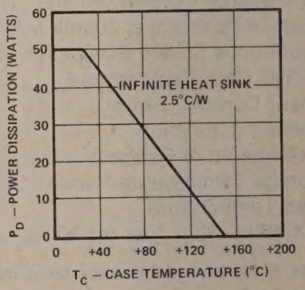
		CHARACTERISTICS			IVN5200KND IVN5201KND			IVN5200KNE IVN5201KNE			IVN5200KNF INV5201KNF			UNIT	TEST CONDITIONS		
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage		40			60			80			V	$V_{GS} = 0$, $I_D = 100\mu A$		
2		$V_{GS(th)}$	Gate Threshold Voltage	IVN5200 Series	0.8		2.0	0.8		2.0	0.8		2.0		$V_{DS} = V_{GS}$, $I_D = 5mA$		
3				IVN5201 Series	0.8		3.6	0.8		3.6	0.8		3.6				
4		I_{GSS}	Gate-Body Leakage			0.2	20		0.2	20		0.2	20	nA	$V_{GS} = 12V$, $V_{DS} = 0$		
5							100			100			100		$V_{GS} = 12V$, $V_{DS} = 0$, $T_A = +125°C$		
6		I_{DSS}	Zero Gate Voltage Drain Current				100			100			100	μA	V_{DS} = Max. Rating, $V_{GS} = 0$		
7							5.0			5.0			5.0	mA	V_{DS} = 0.80 Max. Rating, $V_{GS} = 0$, $T_A = +125°C$		
8						100			100			100		nA	$V_{DS} = 24V$, $V_{GS} = 0$		
9		$I_{D(on)}$	ON-State Drain Current	IVN5200 Series	5.0	10		5.0	10		5.0	10		A	$V_{DS} = 24V$, $V_{GS} = 10V$		(Note 1)
10				IVN5201 Series	5.0	10		5.0	10		5.0	10			$V_{DS} = 24V$, $V_{GS} = 12V$		
11		$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5200KND IVN5200KNE IVN5200KNF		1.5			1.5			1.5		V	$V_{GS} = 5V$, $I_D = 2.0A$		
12						1.9	2.5		1.9	2.5		1.9	2.5		$V_{GS} = 10V$, $I_D = 5.0A$		
13				IVN5201KND INV5201KNE IVN5201KNF		1.2			1.2			1.2			$V_{GS} = 7V$, $I_D = 2.0A$		
14						1.8	2.5		1.8	2.5		1.8	2.5		$V_{GS} = 12V$, $I_D = 5.0A$		
15		$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50	Ω	$V_{GS} = 10V$	$I_D = 5.0A$	
16				IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50		$V_{GS} = 12V$		
17	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50		$V_{GS} = 10V$	$I_D = 5.0A$ f = 1KHz	
18				IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50		$V_{GS} = 12V$		
19		g_{fs}	Forward Transconductance		1.0	1.8		1.0	1.8		1.0	1.8		mho	$V_{DS} = 24V$, $I_D = 5.0A$, f = 1KHz		(Note 2)
20		C_{iss}	Input Capacitance			210	250		210	250		210	250	pF	$V_{DS} = 24V$, $V_{GS} = 0$, f = 1MHz		
21		C_{oss}	Output Capacitance			160	200		160	200		160	200				
22		C_{rss}	Reverse Transfer Capacitance			45	60		45	60		45	60				
23		$t_{d(on)}$	Turn-ON Delay Time			4	20		4	20		4	20	ns	$I_D = 4.0A$ See Switching Times Test Circuit, page 2-44.		(Note 2)
24		t_r	Rise Time			4	20		4	20		4	20				
25		$t_{d(off)}$	Turn-OFF Delay Time			4	20		4	20		4	20				
26		t_f	Fall Time			4	20		4	20		4	20				

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

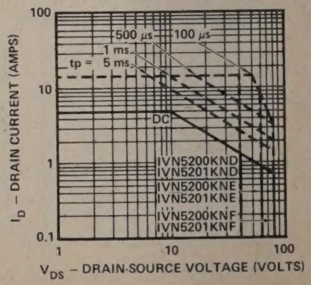
THERMAL RESPONSE



POWER DISSIPATION vs CASE TEMPERATURE



DC SAFE OPERATING REGION
Tc = 25°C



Note: For other 5200 family characteristic curves, see page 2-43.

IVN5200/1 TN Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Extended safe operating area
- Inherently temperature stable
- Low ON resistance in small package

APPLICATIONS

- High efficiency switching power supplies
- Off-line switching regulators
- High speed, high current switches
- Line drivers
- Logic buffers
- High peak current pulse amplifiers
- DC motor controllers

ABSOLUTE MAXIMUM RATINGS
(T_A = 25° C unless otherwise noted)

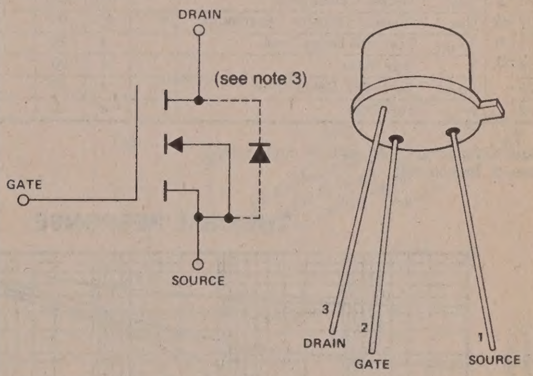
Drain-source Voltage	
IVN5200TND, IVN5201TND	40V
IVN5200TNE, IVN5201TNE	60V
IVN5200TNF, IVN5201TNF	80V
Drain-gate Voltage	
IVN5200TND, IVN5201TND	40V
IVN5200TNE, IVN5201TNE	60V
IVN5200TNF, IVN5201TNF	80V
Continuous Drain Current (see note 1)	4.0A
Peak Drain Current (see note 2)	10A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	−30V
Thermal Resistance, Junction to Case	10°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	12.5W
Linear Derating Factor	100mW/°C
Operating Junction Temperature Range	−55 to +150°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

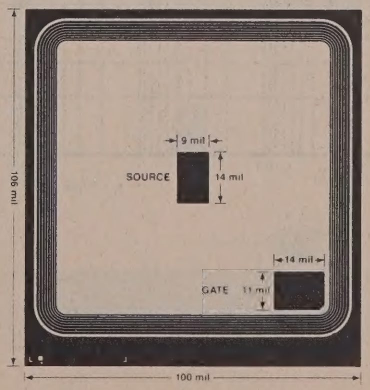
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-39)



Body internally connected to source
Drain common to case

CHIP TOPOGRAPHY

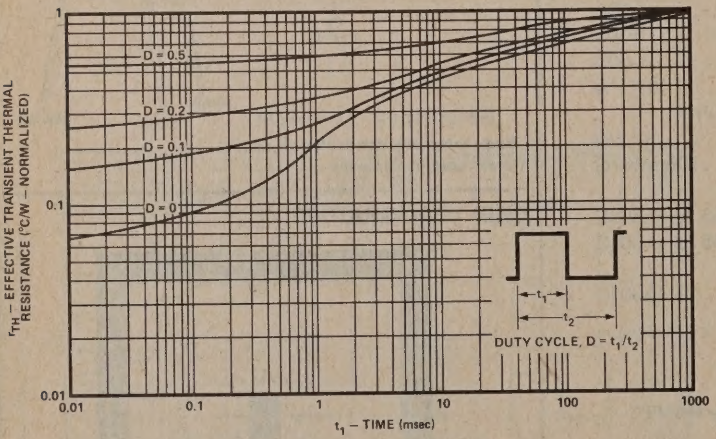


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), $V_{BS} = 0$

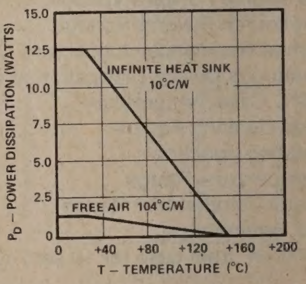
		CHARACTERISTICS			IVN5200TND IVN5201TND			IVN5200TNE IVN5201TNE			IVN5200TNF INV5201TNF			UNIT	TEST CONDITIONS	
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage		40			60			80			V	$V_{GS} = 0$, $I_D = 100\mu A$	
2		$V_{GS(th)}$	Gate Threshold Voltage	IVN5200 Series	0.8		2.0	0.8		2.0	0.8		2.0		$V_{DS} = V_{GS}$, $I_D = 5mA$	
3				IVN5201 Series	0.8		3.6	0.8		3.6	0.8		3.6			
4		I_{GSS}	Gate-Body Leakage			0.2	20		0.2	20		0.2	20	nA	$V_{GS} = 12V$, $V_{DS} = 0$	
5							100			100			100		$V_{GS} = 12V$, $V_{DS} = 0$, $T_A = +125°C$	
6		I_{DSS}	Zero Gate Voltage Drain Current				100			100			100	µA	V_{DS} = Max. Rating, $V_{GS} = 0$	
7							5.0			5.0			5.0	mA	V_{DS} = 0.80 Max. Rating, $V_{GS} = 0$, $T_A = +125°C$	
8						100			100			100		nA	$V_{DS} = 24V$, $V_{GS} = 0$	(Note 1)
9		$I_{D(on)}$	ON-State Drain Current	IVN5200 Series	5.0	10		5.0	10		5.0	10		A	$V_{DS} = 24V$, $V_{GS} = 10V$	
10				IVN5201 Series	5.0	10		5.0	10		5.0	10			$V_{DS} = 24V$, $V_{GS} = 12V$	
11		$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5200TND IVN5200TNE IVN5200TNF		1.5			1.5			1.5		V	$V_{GS} = 5V$, $I_D = 2.0A$	
12						1.9	2.5		1.9	2.5		1.9	2.5		$V_{GS} = 10V$, $I_D = 5.0A$	
13				IVN5201TND INV5201TNE IVN5201TNF		1.2			1.2			1.2			$V_{GS} = 7V$, $I_D = 2.0A$	
14						1.8	2.5		1.8	2.5		1.8	2.5		$V_{GS} = 12V$, $I_D = 5.0A$	
15		$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50	Ω	$V_{GS} = 10V$	$I_D = 5.0A$
16				IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50		$V_{GS} = 12V$	
17	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50		$V_{GS} = 10V$	$I_D = 5.0A$ f = 1KHz
18				IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50		$V_{GS} = 12V$	
19		g_{fs}	Forward Transconductance		1.0	1.8		1.0	1.8		1.0	1.8		mho	$V_{DS} = 24V$, $I_D = 5.0A$, f = 1KHz	
20		C_{iss}	Input Capacitance			210	250		210	250		210	250	pF	$V_{DS} = 24V$, $V_{GS} = 0$, f = 1MHz	(Note 2)
21		C_{oss}	Output Capacitance			160	200		160	200		160	200			
22		C_{rss}	Reverse Transfer Capacitance			45	60		45	60		45	60			
23		$t_{d(on)}$	Turn-ON Delay Time			4	20		4	20		4	20	ns	$I_D = 4.0A$ See Switching Times Test Circuit, page 2-44.	(Note 2)
24		t_r	Rise Time			4	20		4	20		4	20			
25		$t_{d(off)}$	Turn-OFF Delay Time			4	20		4	20		4	20			
26		t_f	Fall Time			4	20		4	20		4	20			

Note 1. Pulse test — 80µsec, 1% duty cycle.
Note 2. Sample test.

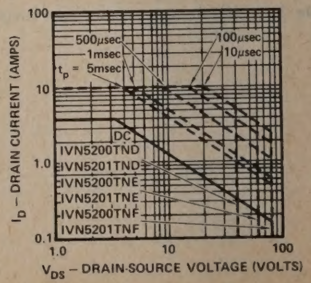
THERMAL RESPONSE



POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION
Tc = 25°C



Note: For other 5200 family characteristic curves, see page 2-43.

INTERSIL

IVN5201 CN Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high current switching**
- **Inherent current sharing capability when paralleled**
- **Directly interfaces to CMOS, DTL, TTL logic**
- **Simple, straight-forward DC biasing**
- **Extended safe operating area**
- **Reliable, low cost plastic package**

APPLICATIONS

- **Deflection coil drivers**
- **Off-line switching regulators**
- **Power amplifiers**
- **DC to DC inverters**
- **Motor controllers**
- **High current line drivers**

ABSOLUTE MAXIMUM RATINGS

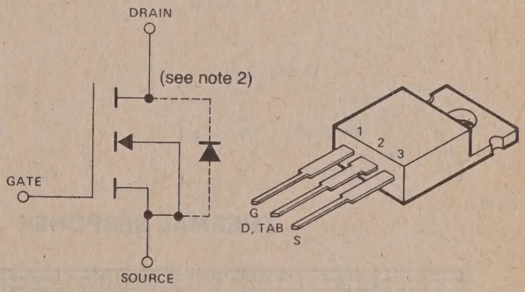
(T_A = 25° C unless otherwise noted)

Drain-source Voltage	
IVN5201CND	40V
IVN5201CNE	60V
IVN5201CNF	80V
Drain-gate Voltage	
IVN5201CND	40V
IVN5201CNE	60V
IVN5201CNF	80V
Continuous Drain Current	5.0A
Peak Drain Current (see note 1)	12A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	−30V
Thermal Resistance, Junction to Case	4.17°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	30W
Linear Derating Factor	240mW/°C
Operating Junction Temperature Range	−40 to +150°C
Storage Temperature Range	−40 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. Maximum pulse width 80μsec, maximum duty cycle 1.0%

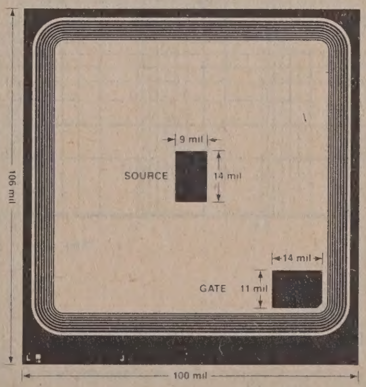
Note 2. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-220)



Body internally connected to source.
Drain common to tab.

CHIP TOPOGRAPHY



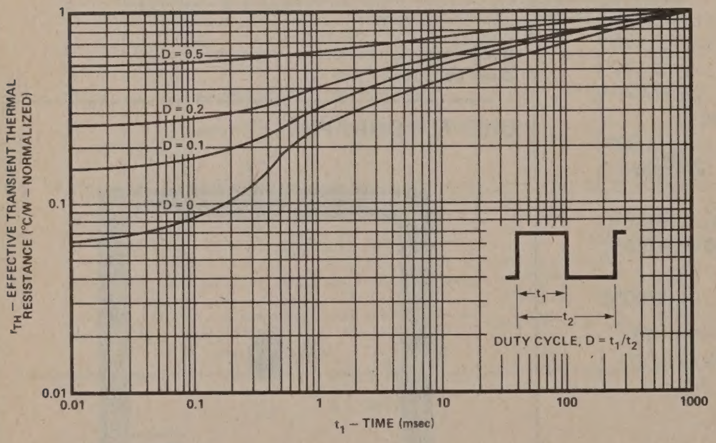
IVN5201 CN Series

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), $V_{BS} = 0$

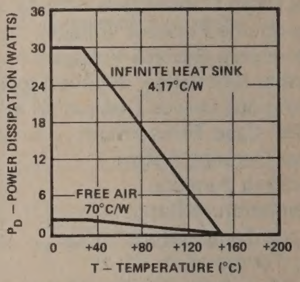
CHARACTERISTICS				IVN5201CND			IVN5201CNE			IVN5201CNF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	40			60			80			V	$V_{GS} = 0$, $I_D = 100\mu A$	
2		$V_{GS(th)}$	Gate Threshold Voltage	0.8		3.6	0.8		3.6	0.8		3.6		$V_{DS} = V_{GS}$, $I_D = 5mA$	
3		I_{GSS}	Gate-Body Leakage		0.2	20		0.2	20		0.2	20	nA	$V_{GS} = 12V$, $V_{DS} = 0$	
4						100			100			100		$V_{GS} = 12V$, $V_{DS} = 0$, $T_A = +125°C$	
5		I_{DSS}	Zero Gate Voltage Drain Current			100			100			100	µA	V_{DS} = Max. Rating, $V_{GS} = 0$	
6						5.0			5.0			5.0	mA	V_{DS} = 0.80 Max. Rating, $V_{GS} = 0$, $T_A = +125°C$	
7					100			100			100		nA	$V_{DS} = 24V$, $V_{GS} = 0$	(Note 1)
8		$I_{D(on)}$	ON-State Drain Current	5.0	10		5.0	10		5.0	10		A	$V_{DS} = 24V$, $V_{GS} = 12V$	
9		$V_{DS(on)}$	Drain-Source Saturation Voltage		1.2			1.2			1.2		V	$V_{GS} = 7V$, $I_D = 2.0A$	
10					1.8	2.5		1.8	2.5		1.8	2.5		$V_{GS} = 12V$, $I_D = 5.0A$	
11		$r_{DS(on)}$	Static Drain-Source ON Resistance		0.36	0.50		0.36	0.50		0.36	0.50	Ω	$V_{GS} = 12V$, $I_D = 5.0A$	
12	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance		0.36	0.50		0.36	0.50		0.36	0.50		$V_{GS} = 12V$, $I_D = 5.0A$ f = 1KHz	
13		g_{fs}	Forward Transconductance	1.0	1.8		1.0	1.8		1.0	1.8		mho	$V_{DS} = 24V$, $I_D = 5.0A$, f = 1KHz	
14		C_{iss}	Input Capacitance		210	250		210	250		210	250	pF	$V_{DS} = 24V$, $V_{GS} = 0$, f = 1MHz	(Note 2)
15		C_{oss}	Output Capacitance		160	200		160	200		160	200			
16		C_{rss}	Reverse Transfer Capacitance		45	60		45	60		45	60			
17		$t_{d(on)}$	Turn-ON Delay Time		4	20		4	20		4	20	ns	$I_D = 4.0A$ See Switching Times Test Circuit, page 2-44.	(Note 2)
18		t_r	Rise Time		4	20		4	20		4	20			
19		$t_{d(off)}$	Turn-OFF Delay Time		4	20		4	20		4	20			
20		t_f	Fall Time		4	20		4	20		4	20			

Note 1. Pulse test — 80µsec, 1% duty cycle.
Note 2. Sample test.

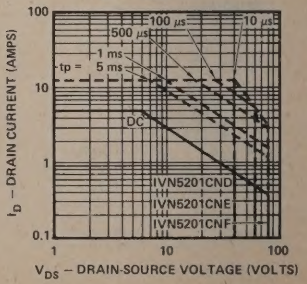
THERMAL RESPONSE



POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION
Tc = 25°C



Note: For other 5200 family characteristic curves, see page 2-43.

IVN6000 KN Series 450V n-Channel Enhancement-mode Vertical Power MOS FETs

FEATURES

- High speed, high current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS logic
- Simple, straight-forward DC biasing
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- Motor controllers
- Power amplifiers
- RF amplifiers

ABSOLUTE MAXIMUM RATINGS

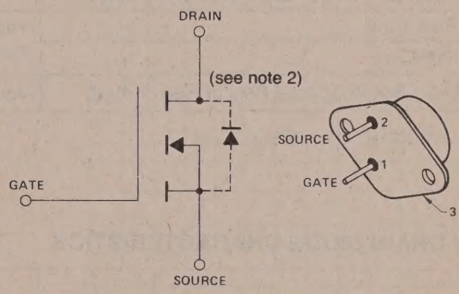
(T_A = 25° C unless otherwise noted)

Drain-source Voltage	
IVN6000KNR	350V
IVN6000KNS	400V
IVN6000KNT	450V
Drain-gate Voltage	
IVN6000KNR	350V
IVN6000KNS	400V
IVN6000KNT	450V
Continuous Drain Current	2.5A
Peak Drain Current (see note 1)	7.5A
Gate-source Voltage	±30V
Thermal Resistance, Junction to Case	3.0 ℃/W
Continuous Device Dissipation at (or below) 25 ℃ Case Temperature	41.7W
Linear Derating Factor	333mW/ ℃
Operating Junction Temperature Range	−55 to +150°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C
Body-drain Diode Continuous Forward Current	3A
Body-drain Diode Peak Forward Current	10A

Note 1. Maximum pulse width 80μsec, maximum duty cycle 1.0%

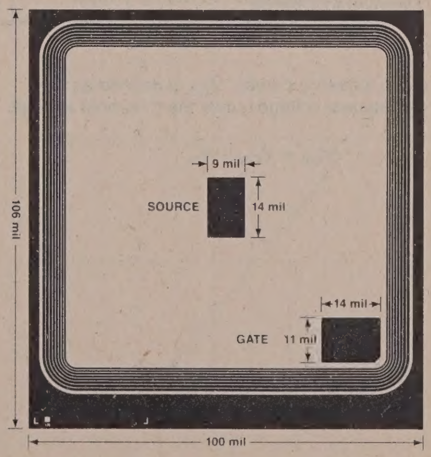
Note 2. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM



Body internally connected to source.
Drain common to case.

CHIP TOPOGRAPHY



ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage IVN6000KNR	BV_{DS}	$V_{GS} = 0V$ $I_D = 100 \mu A$	350			V
IVN6000KNS			400			
IVN6000KNT			450			
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 10$ mA	1.5		5	
Gate-Body Leakage Current	I_{GSS}	$V_{GS} = 30$ V		10	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Maximum Rating, $V_{GS} = 0V$ $T_J = 125°C$		0.2	2	mA
ON Drain Current[1]	$I_{D(on)}$	$V_{DS} = 25V$, $V_{GS} = 15V$	5	7		A
Static-Drain Source ON Resistance[1]	$r_{DS(on)}$	$V_{GS} = 15V$, $I_D = 1A$		2.5	3.0	Ω
Forward Transconductance[1]	g_{fs}	$V_{DS} = 200V$, $I_D = 1.5A$	0.8	1.0		mho
Input Capacitance	C_{iss}	$V_{DS} = 100V$, f = 1.0 MHz, $V_{GS} = 0V$		220	300	pF
Output Capacitance	C_{oss}			22	30	
Reverse Transfer Capacitance	C_{rss}			6	10	
Rise Time	t_r	$V_{DS} = 200V$, $I_D = 1.0A$, $V_{GS} = 15V$, $R_{gen} = 6\Omega$		5	10	ns
Fall Time	t_f			5	10	ns
Drain-Source Voltage Rate of Rise	dV/dt	$V_{DS} = 400V$, $V_{GS} = 0$		100		V/ns

Note: 1. Pulse Test: 80µs, 1% duty cycle.

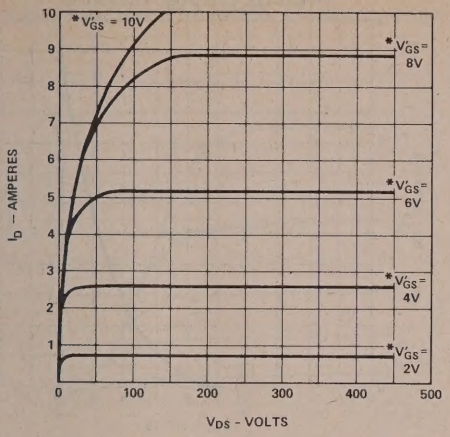
BODY-DRAIN DIODE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Forward Voltage Drop	V_f	Peak Forward Current = 2A		0.95	1.1	V
Reverse Recovery Time	t_{rr}	$I_{fwd(pk)} = I_{rev(pk)}$ Recovery to 50%		100		ns
Recovered Charge	Q_{rr}	$T_J = 150°C$, $I_{fwd(pk)} = 2A$		200		nC

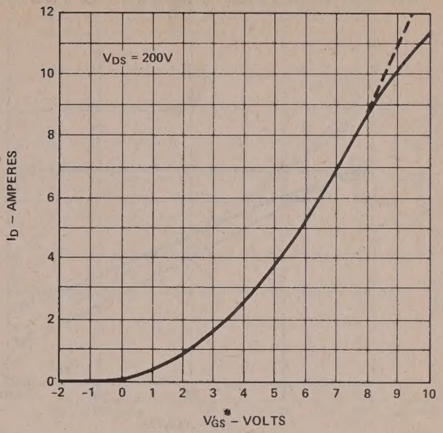
Note: In the following curves, V'_{GS} is defined as the gate-source voltage minus the threshold voltage.

$$V'_{GS} = V_{GS} - V_{th}$$

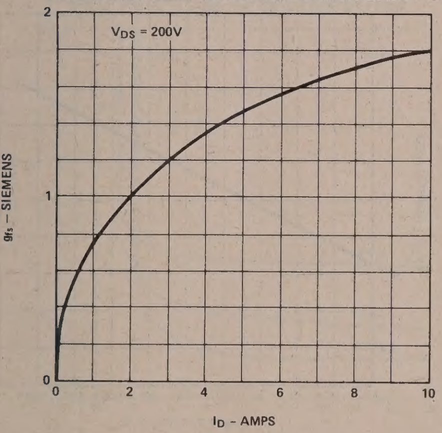
OUTPUT CHARACTERISTICS



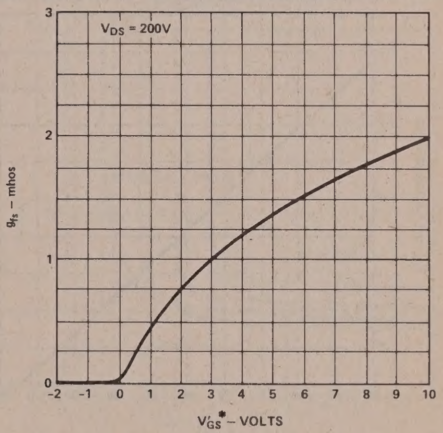
TRANSFER CHARACTERISTICS



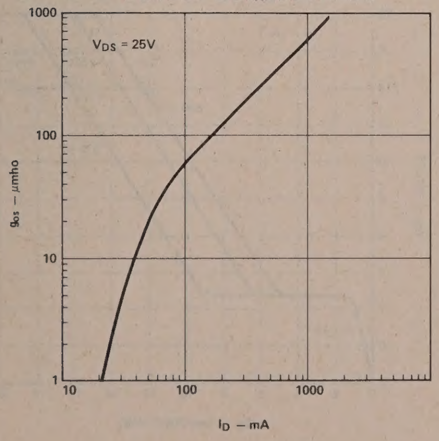
TRANSCONDUCTANCE CHARACTERISTIC



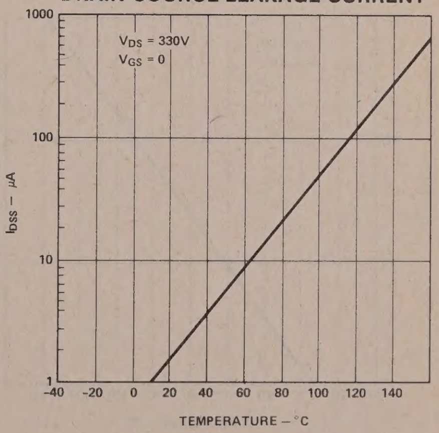
TRANSCONDUCTANCE CHARACTERISTIC



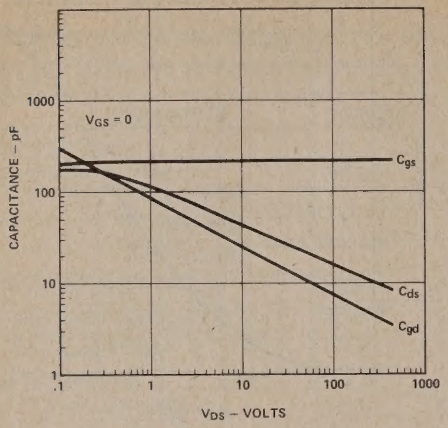
OUTPUT CONDUCTANCE



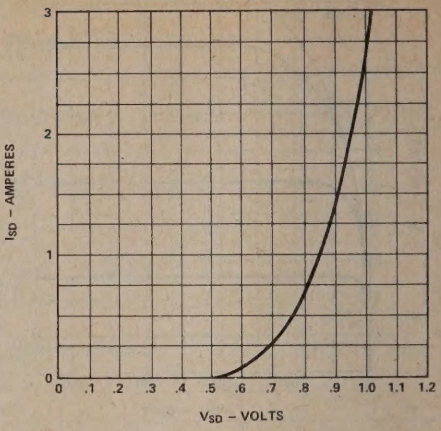
DRAIN-SOURCE LEAKAGE CURRENT



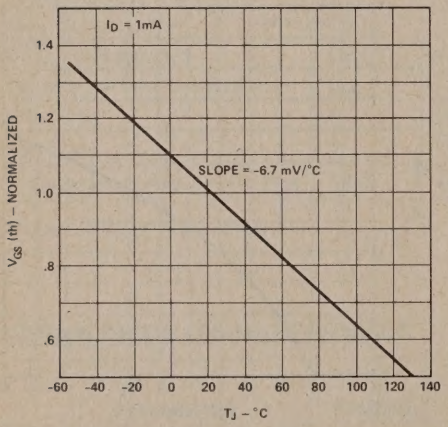
CAPACITANCE vs. DRAIN-SOURCE VOLTAGE



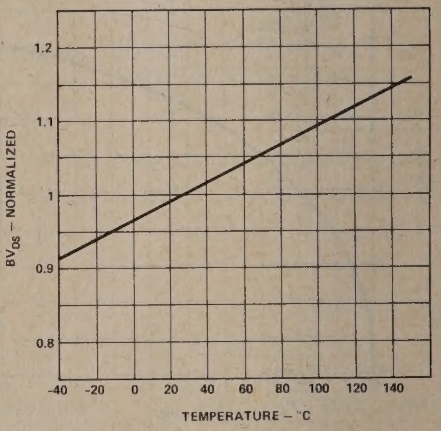
BODY-DRAIN DIODE FORWARD VOLTAGE CHARACTERISTIC



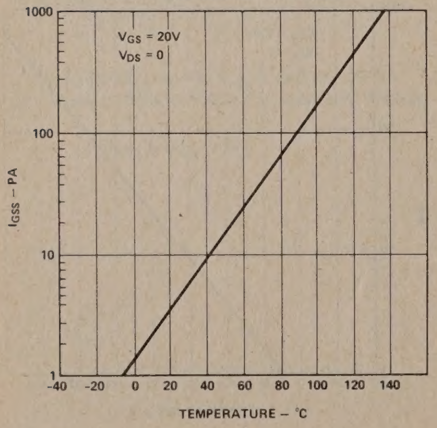
THRESHOLD VOLTAGE VS. TEMPERATURE



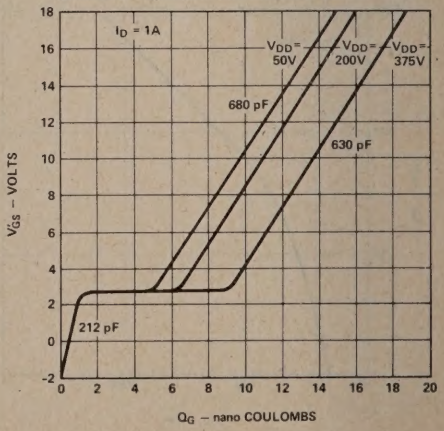
DRAIN-SOURCE BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE



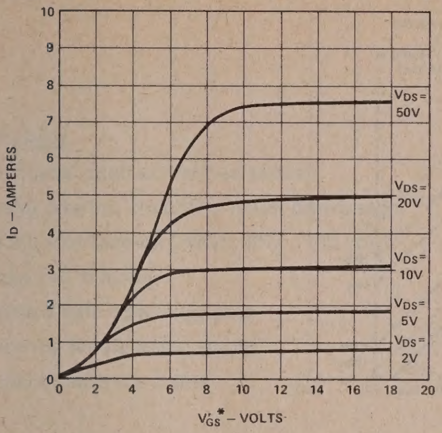
GATE LEAKAGE CURRENT



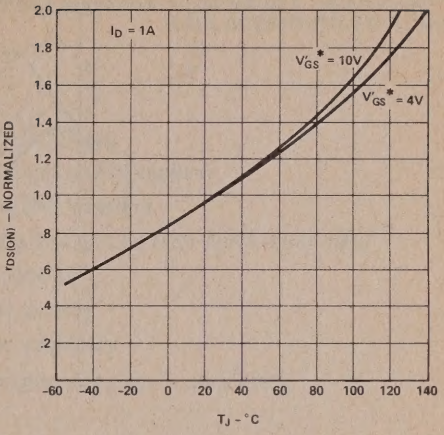
GATE DYNAMIC CHARACTERISTICS



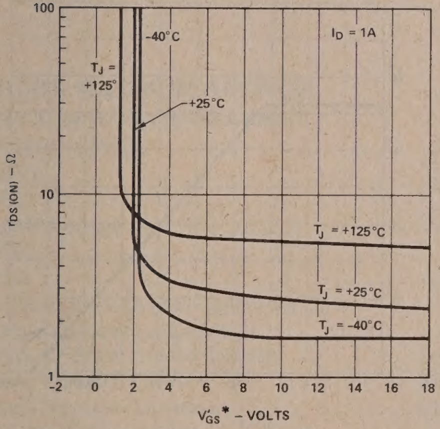
LARGE SIGNAL TRANSFER CHARACTERISTICS



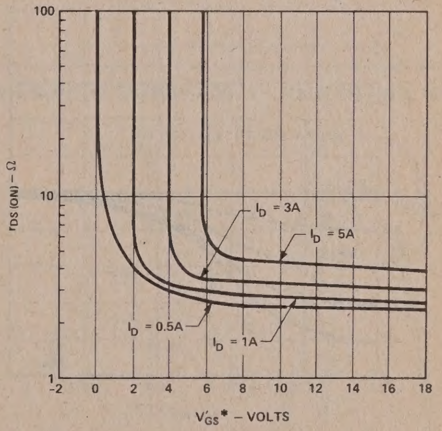
ON RESISTANCE vs. JUNCTION TEMPERATURE



ON RESISTANCE vs. V'_{GS}* AS A FUNCTION OF TEMPERATURE



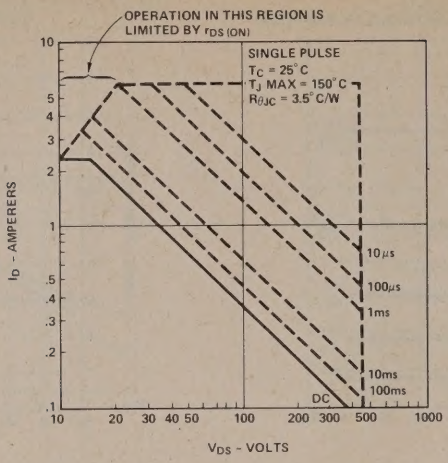
ON RESISTANCE vs. V'_{GS}* AS A FUNCTION OF I_D



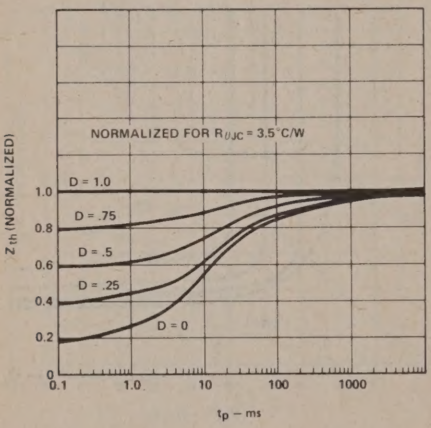
2

* $V'_{GS} = V_{GS} - V_{th}$

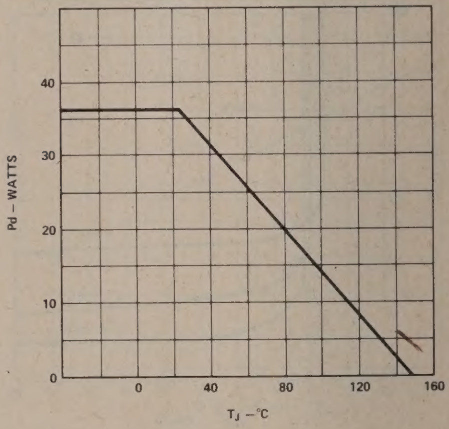
SAFE OPERATING AREA



TRANSIENT THERMAL IMPEDANCE



POWER DISSIPATION vs. TEMPERATURE DERATING



INTERSIL

IVN6660-1
n-Channel Enhancement-mode Vertical Power MOSFET
REPLACEMENTS FOR 2N6660-1

FEATURES
- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- Simple DC biasing
- Extended safe operating area
- Inherently temperature stable
- Typical t_{on} and $t_{off} < 5ns$

APPLICATIONS
- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers
- High frequency linear amplifiers

ABSOLUTE MAXIMUM RATINGS
($T_A = 25°C$ unless otherwise noted)

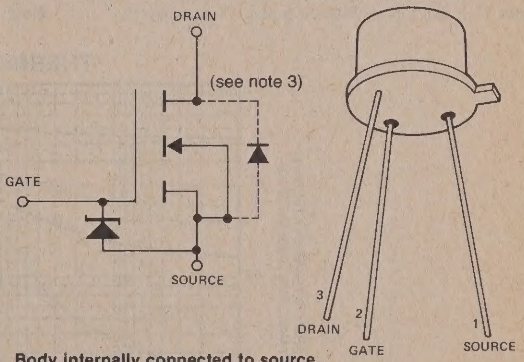
Drain-source Voltage	
IVN6660	60V
IVN6661	90V
Drain-gate Voltage	
IVN6660	60V
IVN6661	90V
Continuous Drain Current (see note 1)	1.2A
Peak Drain Current (see note 2)	3.0A
Continuous Forward Gate Current	2.0mA
Peak-gate Forward Current	100mA
Peak-gate Reverse Current	100mA
Gate-source Forward (Zener) Voltage	+15V
Gate-source Reverse (Zener) Voltage	–0.3V
Thermal Resistance, Junction to Case	20°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	6.25W
Linear Derating Factor	50mW/°C
Operating Junction Temperature Range	–55 to +150°C
Storage Temperature Range	–55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

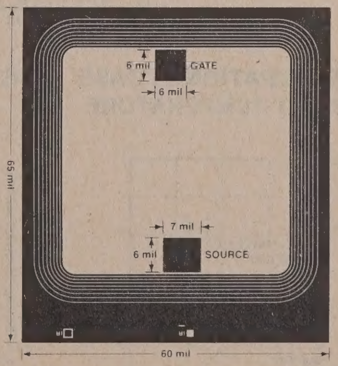
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM
(OUTLINE DWG. TO-39)



Body internally connected to source.
Drain common to case.

CHIP TOPOGRAPHY



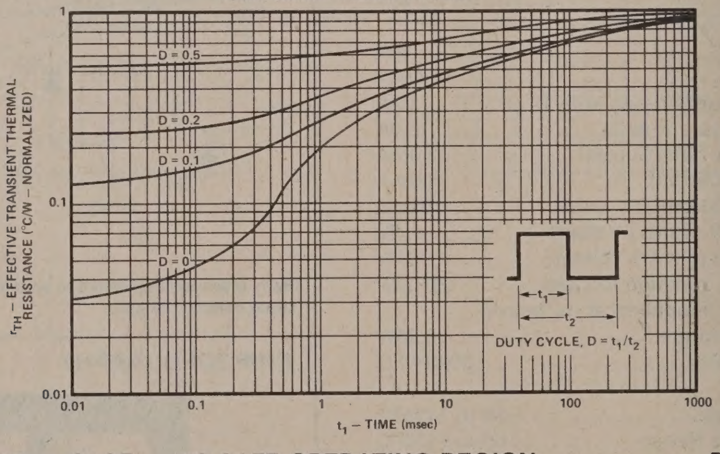
IVN6660-1

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

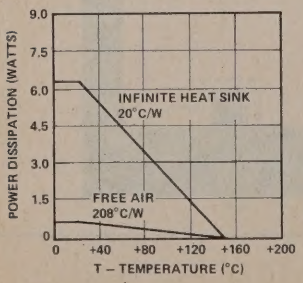
		CHARACTERISTIC		IVN6660			IVN6661			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain Source Breakdown	60			90			V	$V_{GS} = 0$, $I_D = 10\mu A$	
2				60			90				$V_{GS} = 0$, $I_D = 2.5mA$	
3		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0		$V_{DS} = V_{GS}$, $I_D = 1mA$	
4		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100	nA	$V_{GS} = 15V$, $V_{DS} = 0$	
5						500			500		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$	(Note 2)
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10	μA	V_{DS} = Max. Rating, $V_{GS} = 0$	
7						500			500		V_{DS} = 0.80 Max. Rating, $V_{GS} = 0$, $T_A = 125°C$ (Note 2)	
8					100			100		nA	$V_{DS} = 25V$, $V_{GS} = 0$	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		A	$V_{DS} = 25V$, $V_{GS} = 10V$	(Note 1)
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.4		V	$V_{GS} = 5V$, $I_D = 0.1 A$	
11					1.0	1.5		1.1	1.6		$V_{GS} = 5V$, $I_D = 0.3 A$	
12					0.9			1.3			$V_{GS} = 10V$, $I_D = 0.5 A$	
13					2.2	3.0		2.2	4.0		$V_{GS} = 10V$, $I_D = 1.0 A$	
14		$r_{DS(on)}$	Static Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0	Ω	$V_{GS} = 10V$, $I_D = 1.0 A$	
15	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0		$V_{GS} = 10V$, $I_D = 1.0 A$	f = 1KHz
16		g_{fs}	Forward Transconductance	170	250		170	250		mΩ	$V_{DS} = 24V$, $I_D = 0.5 A$	
17		C_{iss}	Input Capacitance			50			50	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0MHz	(Note 2)
18		C_{ds}	Drain-Source Capacitance			40			40			
19		C_{rss}	Reverse Transfer Capacitance			10			10		$V_{GS} = 0$, $V_{DS} = 24V$, f = 1.0MHz	
20						35			35		$V_{GS} = 0$, $V_{DS} = 0$, f = 1.0MHz	
21		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5	ns		
22		t_r	Rise Time		2	5		2	5			
23		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5			
24		t_f	Fall Time		2	5		2	5			

Note 1. Pulse test — 80μsec pulse, 1% duty cycle. **Note 2.** Sample test.

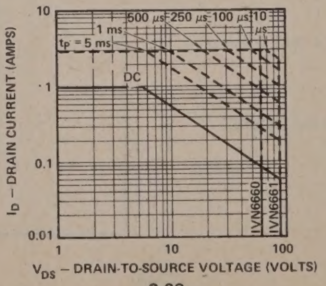
THERMAL RESPONSE



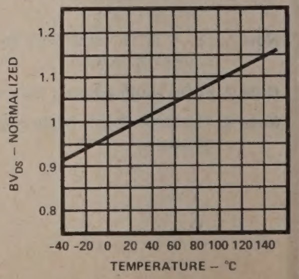
POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION Tc = 25°C



BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE



INTERSIL

2N6660-1
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **Simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**
- **Typical t_{on} and $t_{off} < 5$ns**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**
- **High frequency linear amplifiers**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

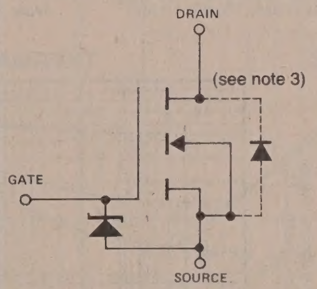
Drain-source Voltage	
IVN6660	60V
IVN6661	90V
Drain-gate Voltage	
IVN6660	60V
IVN6661	90V
Continuous Drain Current (see note 1)	2.0A
Peak Drain Current (see note 2)	3.0A
Continuous Forward Gate Current	2.0mA
Peak-gate Forward Current	100mA
Peak-gate Reverse Current	100mA
Gate-source Forward (Zener) Voltage	+15V
Gate-source Reverse (Zener) Voltage	−0.3V
Continuous Device Dissipation at (or below) 25°C Case Temperature	8.33W
Linear Derating Factor	67mW/°C
Operating Junction Temperature Range	−55 to +150°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

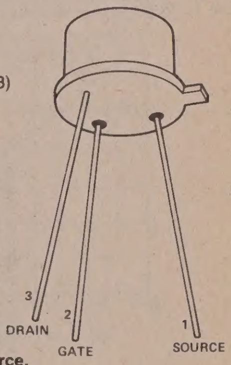
Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

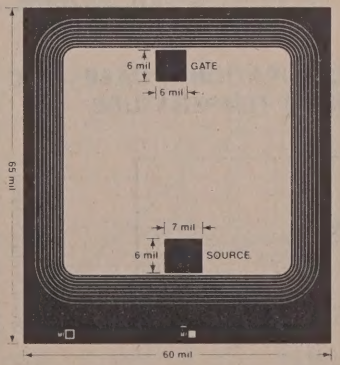
SCHEMATIC DIAGRAM (OUTLINE DWG. TO-39)





Body internally connected to source.
Drain common to case.

CHIP TOPOGRAPHY

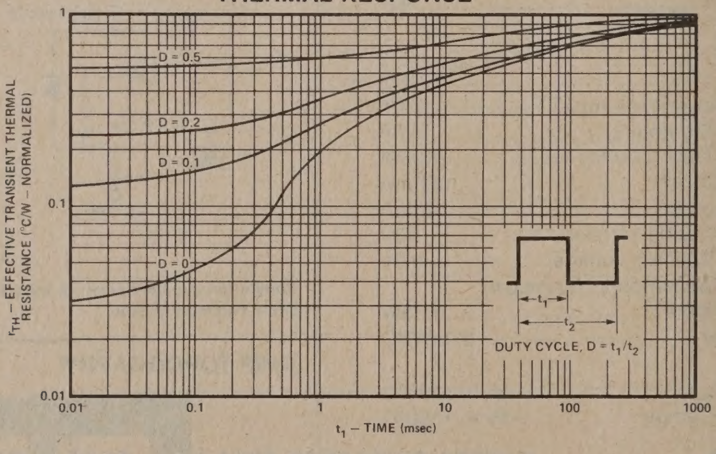


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

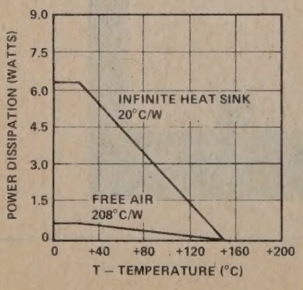
		CHARACTERISTIC		IVN6660			IVN6661			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain Source Breakdown	60			90			V	$V_{GS} = 0$, $I_D = 10\mu A$	
2				60			90				$V_{GS} = 0$, $I_D = 2.5mA$	
3		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0		$V_{DS} = V_{GS}$, $I_D = 1mA$	
4		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100	nA	$V_{GS} = 15V$, $V_{DS} = 0$	
5						500			500		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$	(Note 2)
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10	μA	V_{DS} = Max. Rating, $V_{GS} = 0$	
7						500			500		V_{DS} = 0.80 Max. Rating, $V_{GS} = 0$, $T_A = 125°C$ (Note 2)	
8					100			100		nA	$V_{DS} = 25V$, $V_{GS} = 0$	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		A	$V_{DS} = 25V$, $V_{GS} = 10V$	(Note 1)
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.4		V	$V_{GS} = 5V$, $I_D = 0.1 A$	
11					1.0	1.5		1.1	1.6		$V_{GS} = 5V$, $I_D = 0.3 A$	
12					0.9			1.3			$V_{GS} = 10V$, $I_D = 0.5 A$	
13					2.2	3.0		2.2	4.0		$V_{GS} = 10V$, $I_D = 1.0 A$	
14		$r_{DS(on)}$	Static Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0	Ω	$V_{GS} = 10V$, $I_D = 1.0 A$	
15	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0		$V_{GS} = 10V$, $I_D = 1.0 A$, f = 1KHz	
16		g_{fs}	Forward Transconductance	170	250		170	250		mΩ	$V_{DS} = 24V$, $I_D = 0.5 A$, f = 1KHz	
17		C_{iss}	Input Capacitance			50			50	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0MHz	(Note 2)
18		C_{ds}	Drain-Source Capacitance			40			40			
19		C_{rss}	Reverse Transfer Capacitance			10			10		$V_{GS} = 0$, $V_{DS} = 24V$, f = 1.0MHz	
20						35			35		$V_{GS} = 0$, $V_{DS} = 0$, f = 1.0MHz	
21		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5	ns		
22		t_r	Rise Time		2	5		2	5			
23		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5			
24		t_f	Fall Time		2	5		2	5			

Note 1. Pulse test — 80μsec pulse, 1% duty cycle. **Note 2.** Sample test.

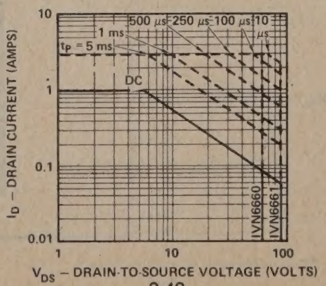
THERMAL RESPONSE



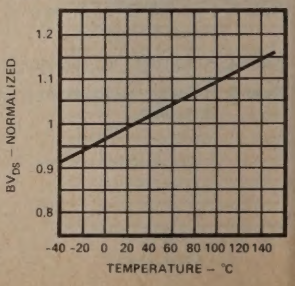
POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION Tc = 25°C

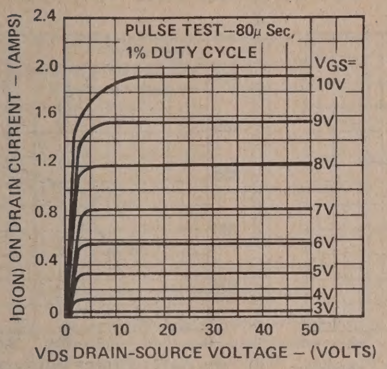


BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE

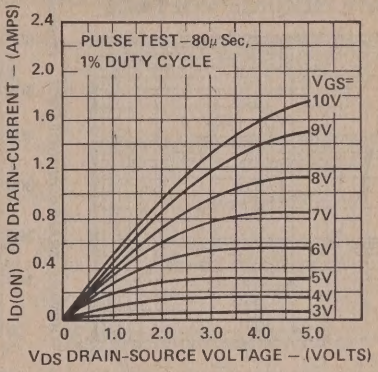


5000 Family Typical Performance Curves (25°C. unless otherwise stated)

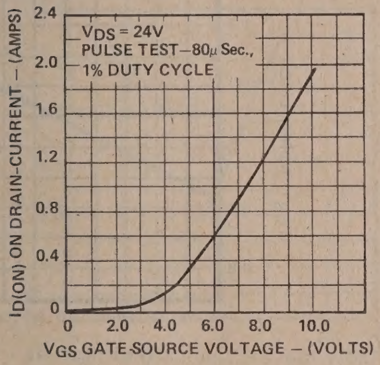
OUTPUT CHARACTERISTICS



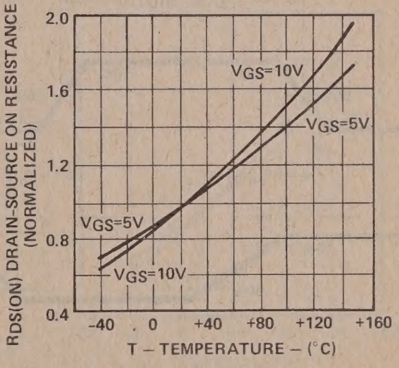
SATURATION CHARACTERISTICS



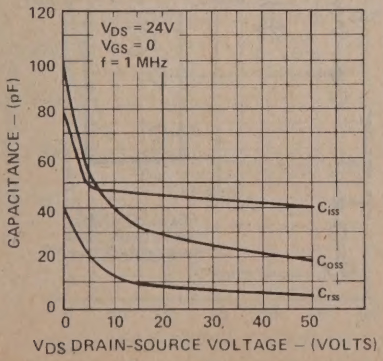
TRANSFER CHARACTERISTIC



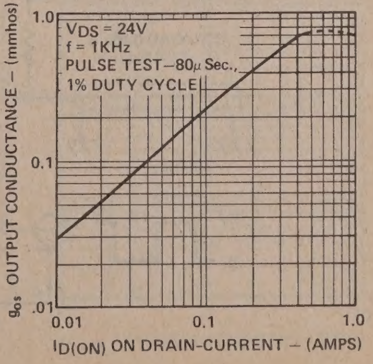
NORMALIZED DRAIN-SOURCE ON RESISTANCE vs TEMPERATURE



CAPACITANCE vs DRAIN-SOURCE VOLTAGE

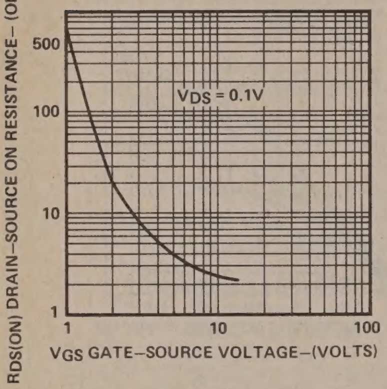


OUTPUT CONDUCTANCE vs DRAIN CURRENT

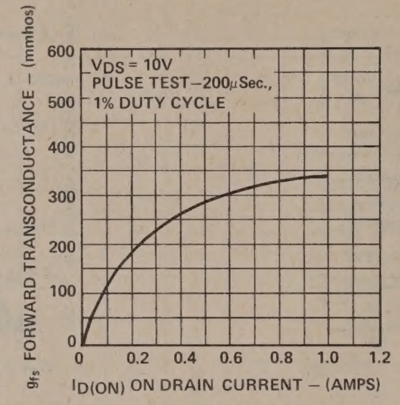


5000 Family Typical Performance Curves (25°C. unless otherwise stated)

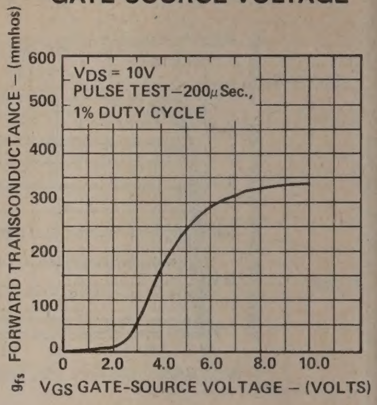
DRAIN-SOURCE ON RESISTANCE vs GATE-SOURCE VOLTAGE



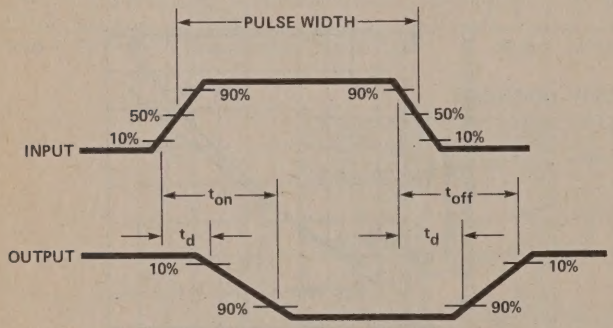
TRANSCONDUCTANCE vs DRAIN CURRENT



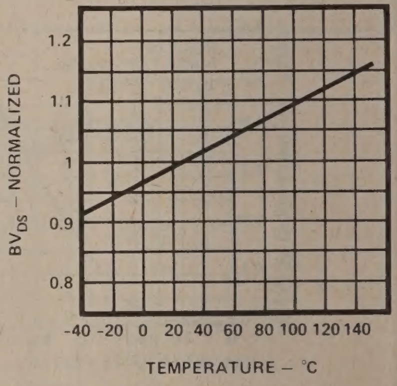
TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE



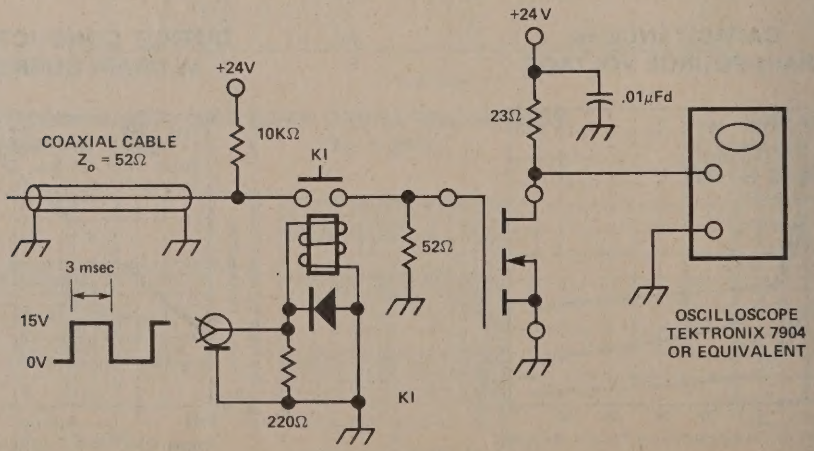
SWITCHING TIME TEST WAVEFORMS


PULSE WIDTH
90%
90%
50%
50%
10%
10%
INPUT
ton
toff
td
td
OUTPUT
10%
10%
90%
90%

BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE

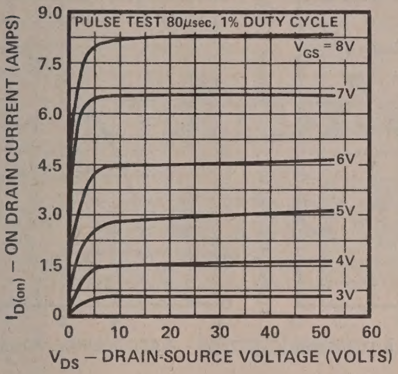


SWITCHING TIME TEST CIRCUIT

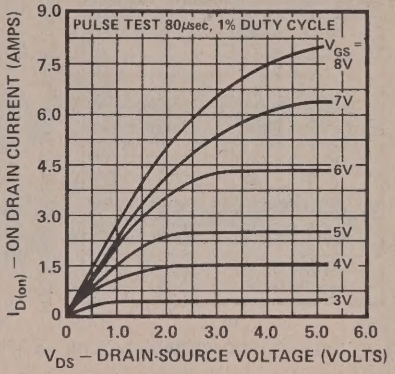

+24 V
+24V
.01μFd
23Ω
10KΩ
COAXIAL CABLE
Zo = 52Ω
KI
52Ω
3 msec
15V
0V
KI
220Ω
OSCILLOSCOPE
TEKTRONIX 7904
OR EQUIVALENT

5200 Family Typical Performance Curves (25°C. unless otherwise stated)

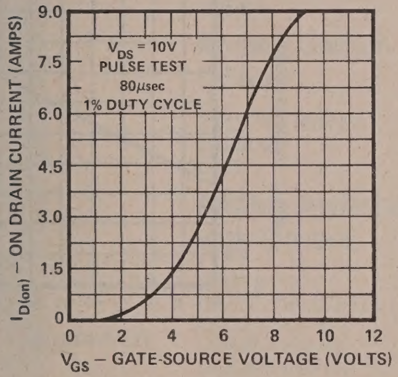
OUTPUT CHARACTERISTICS



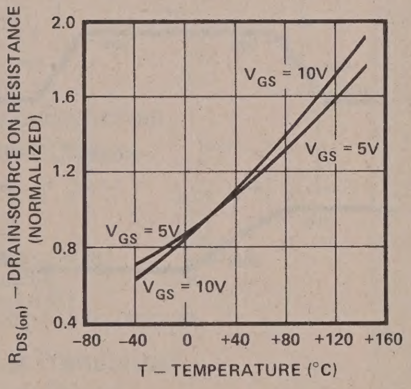
SATURATION CHARACTERISTICS



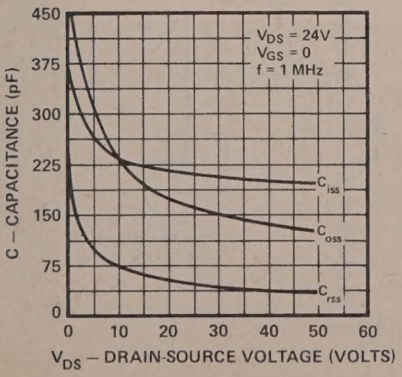
TRANSFER CHARACTERISTIC



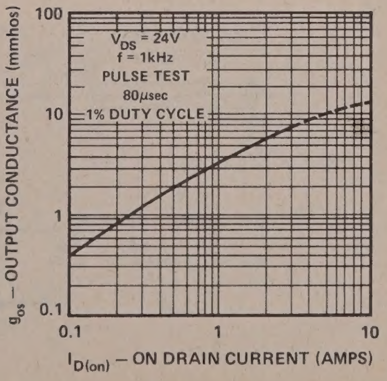
NORMALIZED DRAIN-SOURCE ON RESISTANCE vs TEMPERATURE



CAPACITANCE vs DRAIN-SOURCE VOLTAGE

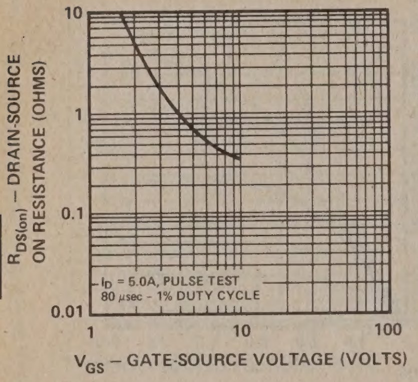


OUTPUT CONDUCTANCE vs DRAIN CURRENT

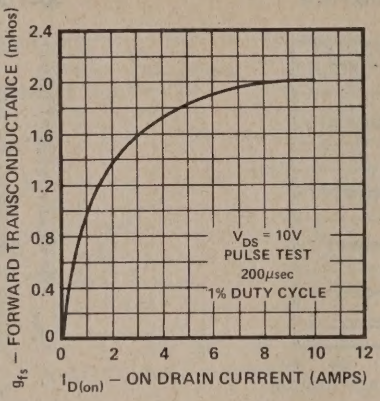


5200 Family Typical Performance Curves (25°C. unless otherwise stated)

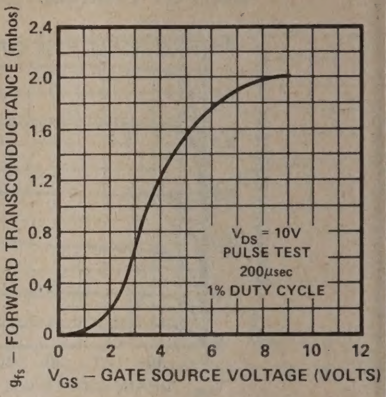
DRAIN-SOURCE ON RESISTANCE vs GATE-SOURCE VOLTAGE



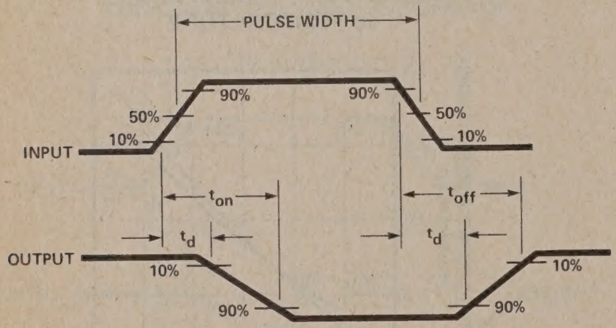
TRANSCONDUCTANCE vs DRAIN CURRENT



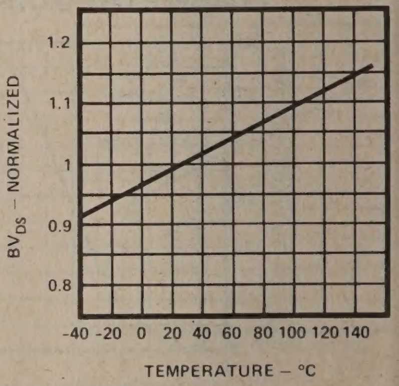
TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE



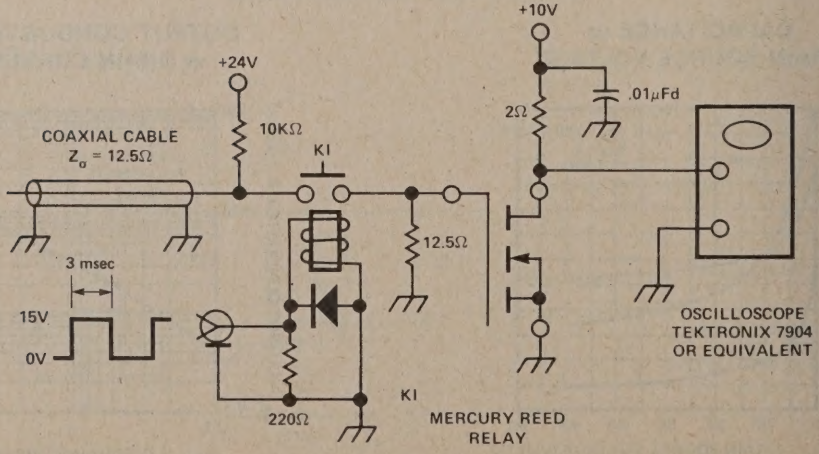
SWITCHING TIME TEST WAVEFORMS


PULSE WIDTH
90%
90%
50%
50%
10%
10%
INPUT
t_{on}
t_{off}
t_d
t_d
OUTPUT
10%
10%
90%
90%

BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE



SWITCHING TIME TEST CIRCUIT


+10V
+24V
.01μFd
2Ω
10KΩ
COAXIAL CABLE
Z_o = 12.5Ω
KI
12.5Ω
3 msec
15V
0V
220Ω
KI
MERCURY REED RELAY
OSCILLOSCOPE
TEKTRONIX 7904
OR EQUIVALENT

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TTL or CMOS to Higher Levels

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Analog Switches with Driver

Type	No. of Channels	Intersil Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} µs max	t_{off} µs max	Logic Input		Power Consumption mW
								Logic Level	Input Typ(2)	
SPST	1	IH5001	N-JFET	30	5.0	0.5	1.0	DTL, TTL, RTL	hi	78
		IH5002	N-JFET	50	5.0	0.5	1.0	DTL, TTL, RTL	hi	78
		IH5021	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5022	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5023	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5024	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5037	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5038	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5040	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5140	CMOS	50	0.1	0.1	0.075	TTL, CMOS	hi	.035
SPST	2	DG111	PMOS FET	450	−1.0	0.3	1.0	DTL, TTL, RTL	lo	163
		DG112	PMOS FET	450	−1.0	0.3	1.0	DTL, TTL, RTL	hi	152
		DG133A	N-JFET	30	1.0	0.3	0.8	DTL, TTL, RTL	hi	68
		DG134A	N-JFET	80	1.0	0.3	0.8	DTL, TTL, RTL	hi	68
		DG141A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	hi	68
		DG151A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	hi	72
		DG152A	N-JFET	50	2.0	0.3	0.8	DTL, TTL, RTL	hi	72
		DG180	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	lo	120
		DG181	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	lo	120
		DG182	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	lo	120
		DGM182	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	lo	.035
		DG433A	N-JFET	35	5.0	0.5	1.0	DTL, TTL, RTL	hi	78
		DG434A	N-JFET	80	5.0	0.5	1.0	DTL, TTL, RTL	hi	78
		DG441A	N-JFET	15	15.0	0.75	1.25	DTL, TTL, RTL	hi	78
		DG451A	N-JFET	20	15.0	0.75	1.25	DTL, TTL, RTL	hi	82
		DG452A	N-JFET	100	5.0	0.5	1.0	DTL, TTL, RTL	hi	82
		IH181	Vara FET	30	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, TTL High Level	lo	.350
		IH182	Vara FET	75	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, TTL High Level	lo	.350
		DG200	CMOS	70	1.0	0.7	0.5	DTL, TTL, RTL, CMOS, TTL High Level	lo	3.0
		IH200	CMOS	75	1.0	1.0	0.5	DTL, TTL, RTL, CMOS, TTL High Level	lo	.350
		IH5003	N-JFET	30	1.0	0.3	0.8	DTL, TTL, RTL	hi	78
		IH5004	N-JFET	50	1.0	0.3	0.8	DTL, TTL, RTL	hi	78
		IH5005	N-JFET	10	10.00	1.0	2.5	DTL, TTL, RTL	hi	78
		IH5006	N-JFET	30	1.0	0.5	1.0	DTL, TTL, RTL	hi	78
		IH5007	N-JFET	80	1.0	0.5	1.0	DTL, TTL, RTL	hi	78
		IH5017	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5018	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5019	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5020	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5033	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5034	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
		IH5035	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5036	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
		IH5041	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5048	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5141	CMOS	50	0.1	0.1	0.075	TTL, CMOS	hi	.035
SPST	3	IH5013	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5014	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5015	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5016	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5029	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5030	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
		IH5031	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5032	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
SPST	4	DG116	P-MOSFET	450	−4.0	0.3	1.0	DTL, TTL, RTL	hi	133
		DG118	P-MOSFET	450	−4.0	0.3	1.0	DTL, TTL, RTL	lo	133
		DG201	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS	lo	.350
		IH201	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS	lo	.350
		IH202	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS	hi	.350
		IH5009	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5010	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5011	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5011	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	

Analog Switches with Driver continued

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} µs max	t_{off} µs max	Logic input Logic Level	Input Typ(2)	Power Consumption mW
SPST	4	IH5025	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5026	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5027	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5028	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5052	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	lo	.350
		IH5053	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.350
SPST	5	DG123	P-MOSFET	450	−4.0	0.3	1.0	DTL, TTL, RTL	hi	133
		DG125	P-MOSFET	450	−4.0	0.3	1.0	DTL, TTL, RTL	lo	133
		DG143A	N-JFET	80	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG144A	N-JFET	30	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG146A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	(3)	84
		DG161A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	(3)	90
		DG162A	N-JFET	50	2.0	0.4	0.8	DTL, TTL, RTL	(3)	90
		DG186	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	(3)	73
		DG187	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	(3)	73
SPDT	1	DG188	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	(3)	73
		DGM188	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	(3)	.035
		DG443A	N-JFET	80	5.0	0.5	1.0	DTL, TTL, RTL	(3)	78
		DG444A	N-JFET	35	5.0	0.5	1.0	DTL, TTL, RTL	(3)	78
		DG446A	N-JFET	15	15.0	0.75	1.25	DTL, TTL, RTL	(3)	78
		DG461A	N-JFET	20	15.0	0.75	1.25	DTL, TTL, RTL	(3)	83
		DG462A	N-JFET	100	5.0	0.5	1.0	DTL, TTL, RTL	(3)	83
		IH187	Vara FET	30	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, PMOS, TTL High Level	(3)	.350
		IH188	Vara FET	75	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, PMOS, TTL High Level	(3)	.350
		IH5042	CMOS	75	1.0	0.05	0.025	DTL, TTL, RTL PMOS, CMOS	(3)	.035
		IH5050	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL PMOS, CMOS	(3)	.035
		IH5142	CMOS	50	0.1	0.175	0.125	TTL, CMOS	(3)	.035
SPDT	2	DG189	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	(3)	120
		DG190	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	(3)	120
		DG191	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	(3)	120
		DGM191	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	(3)	.035
		IH5043	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	(3)	.035
		IH5051	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	(3)	.035
		IH190	CMOS	30	0.1	0.25	0.13	TTL, CMOS, PMOS, TTL High Level	(3)	.350
		IH191	CMOS	75	0.1	0.25	0.13	TTL, CMOS, PMOS, TTL High Level	(3)	.350
		IH5143	CMOS	50	0.1	0.175	0.125	TTL, CMOS	(3)	.035
DPST	1	IH5044	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5144	CMOS	50	0.1	0.175	0.125	TTL, CMOS	hi	.035
DPST	2	DG126A	N-JFET	80	1.0	0.3	0.8	DTL, TTL, RTL	hi	68
		DG129A	N-JFET	30	1.0	0.3	0.8	DTL, TTL, RTL	hi	68
		DG140A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	hi	68
		DG153A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	hi	72
		DG154A	N-JFET	50	2.0	0.3	0.8	DTL, TTL, RTL	hi	72
		DG183	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	hi	84
		DG184	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	hi	84
		DG185	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	hi	84
		DGM185	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	hi	.035
		DG426A	N-JFET	80	5.0	0.5	1.0	DTL, TTL, RTL	hi	78
		DG429A	N-JFET	35	5.0	0.5	1.0	DTL, TTL, RTL	hi	78
		DG440A	N-JFET	15	15.0	0.75	1.25	DTL, TTL, RTL	hi	78
		DG453A	N-JFET	20	15.0	0.75	1.25	DTL, TTL, RTL	hi	83
		DG454A	N-JFET	100	5.0	0.5	1.0	DTL, TTL, RTL	hi	83
		IH184	Vara FET	30	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, PMOS	hi	.350
		IH185	Vara FET	75	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, PMOS	hi	.350
		IH5045	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	hi	.035
		IH5049	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	hi	.035
		IH5145	CMOS	50	0.1	0.175	0.125	TTL, CMOS	hi	.035
DPST	3	DG120	P-MOS FET	450	−3.0	0.3	2.0	DTL, TTL, RTL	hi	164
		DG121	P-MOS FET	450	−3.0	0.3	2.0	DTL, TTL, RTL	lo	164
DPDT	1	DG139A	N-JFET	30	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG142A	N-JFET	80	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG145A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	(3)	84
		DG163A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	(3)	90
		DG164A	N-JFET	50	2.0	0.4	0.8	DTL, TTL, RTL	(3)	90
		DG439A	N-JFET	35	5.0	0.5	1.0	DTL, TTL, RTL	(3)	78
		DG442A	N-JFET	80	5.0	0.5	1.0	DTL, TTL, RTL	(3)	78
		DG445A	N-JFET	15	15.0	0.75	1.25	DTL, TTLQ, RTL	(3)	78
		DG463A	N-JFET	20	15.0	0.75	1.25	DTL, TTL, RTL	(3)	83
		DG464A	N-JFET	100	5.0	0.5	1.0	DTL, TTL, RTL	(3)	83
		IH5046	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL CMOS, PMOS	(3)	.035
4PST	1	IH5047	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL CMOS, PMOS	hi	.035

Multiplexers

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} µs max	t_{off} µs max	Logic input		Power Consumption mW
								Logic Level	Input Typ(2)	
	1 of 8	IH6108	CMOS	300	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
	1 of 16	IH6116	CMOS	600	0.2	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
	2 of 8	IH6208	CMOS	300	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
	2 of 16	IH6216	CMOS	600	0.2	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
Fault	1 of 8	IH5108	CMOS	700	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
Protected	2 of 8	IH5208	CMOS	700	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5

Multi-Channel FET Switches

Electrical Characteristics @ +25°C—Military Temperature Devices

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ ohms max(4)	$r_{DS(on)}$ ohms max(1)	$I_{D(off)}$ na max	t_{on} ns max*	t_{off} ns max*	Logic input	
									Logic Level	Type
SPST	3	MM-455	P-MOS	200	600	0.2	50	50	P-MOS	lo
		MM-555	P-MOS	200	600	20.0	50	50	P-MOS	lo
		G-124	P-MOS	100	450	2.0	100	100	P-MOS	hi
		G-125	N-JFET	500	500	0.05	30	50	- 5V PMOS	hi
		G-126	N-JFET	250	250	0.05	30	50	-10V PMOS	hi
		G-127	N-JFET	90	90	0.1	30	50	- 5V PMOS	hi
		G-128	N-JFET	45	45	0.1	30	50	-10V PMOS	hi
		G-129	N-JFET	500	500	0.05	30	50	- 5V PMOS	hi
		G-130	N-JFET	250	250	0.05	30	50	-10V PMOS	hi
		G-131	N-JFET	90	90	0.1	30	50	- 5V PMOS	hi
SPST	4	G-132	N-JFET	45	45	0.1	30	50	-10V PMOS	hi
		G-1330	N-JFET	20	20	0.5	30	50	- 5V PMOS	hi
		G-1340	N-JFET	10	10	0.5	30	50	-10V PMOS	hi
		G-1350	N-JFET	20	20	0.5	30	50	- 5V PMOS	hi
		G-1360	N-JFET	10	10	0.5	30	50	-10V PMOS	hi
		MM-451	P-MOS	200	600	0.2	50	50	P-MOS	lo
		MM-452	P-MOS	200	600	0.2	50	50	P-MOS	lo
		MM-551	P-MOS	200	600	20.0	50	50	P-MOS	lo
		MM-552	P-MOS	200	600	20.0	50	50	P-MOS	lo
SPST	5	G-116	P-MOS	100	450	- 2.5	100	100	P-MOS	lo
		G-117	P-MOS	100	450	- 0.5	100	100	P-MOS	lo
SPST	6	G-115	P-MOS	100	450	-10.0	100	100	P-MOS	lo
		G-118	P-MOS	100	450	- 3.0	100	100	P-MOS	lo
		G-123	P-MOS	125	500	-10.0	100	100	P-MOS	lo
Diff	2	MM-450	P-MOS	200	600	0.2	50	50	P-MOS	lo
		MM-550	P-MOS	200	600	20.0	50	50	P-MOS	lo
SPST	3	G-119	P-MOS	100	450	-1.5	100	100	P-MOS	lo

*These times are dependent on the driver used.

Drivers for FET Switches

Electrical Characteristics @ +25°C—Military Temperature Devices

No. of Channels	Device No.	V_{OUT} Positive Volts	V_{OUT} Negative Volts	t_{on} ns max	t_{off} ns max	I_{in} Lo µA (max)	I_{in} Hi mA (max)	Logic Input Level	Power Consumption (mW)
2	D112	+9.9	-19.2	250	1500	1.0	1.5	TTL	103
	D113	+9.9	-19.2	250	1500	1.0	1.0	TTL	76
	D120	+9.9	-19.2	250	600	1.0	1.5	TTL	220
	D121	+9.9	-19.2	250	600	1.0	1.0	TTL	193
	IH6201	+14.0	-14.0	200	300	1.0	1.0	TTL	.350
4	D129	V_{supply}	-19.3	250	1000	200	0.25µA	TTL/DTL	55
6	D123	V_{supply}	-19.7	250	600	1.0	1.0µA	TTL/DTL	20
	D125	V_{supply}	-19.7	250	600	1.0	1.5µA	TTL	50

Notes:

1. Switch Resistance under worst case analog voltage.
2. Positive logic LO ("0") or HI ("1") voltage at driver input necessary to turn switch on.
3. Logic "0" or "1" can be arbitrarily assigned for double-throw switches.
4. Switch resistance under best case analog voltage.

VARAFET

Type	$r_{DS(on)}$ Ω max	V_p V max	$I_{s(off)}$ pA max	I_{DSS} mA min	t_{on} ns max	t_{off} ns max	Package 4 FETS/Pkg	V_{analog} V_{p-p} min	V_{inject} V_{p-p} max
IH401	30	7.5	200	45 min	50	150	16 Pin Dip	15	10
IH401A	50	5.0	200	35 min	50	150	16 Pin Dip	20	10

Lowest Quiescent Current		**Highest Speed**	**Lowest $r_{DS(on)}$**		For switches whose outputs go into the input of an OP Amp.	For switching positive signals only:
IH5040 Family and IH200 Family Monolithic CMOS driver gate conbination	**IH5140 Family** Monolithic CMOS driver gate conbination.	**IH181 Family** CMOS driver and Varafet gate.	**DG180 Family** Bipolar/MOS drive with N-JFET gate.	**DG126, DG126A Family and IH5001 Family** Bipolar driver with N-JFET gate.	**5009 Family** VIRTUAL GROUND SWITCH	**5025 Family** POSITIVE SIGNAL SWITCH
Features 1. Very low quiescent current resulting in very low power consumption. 2. Low cost. 3. Good speed with moderate $r_{DS(on)}$ and leakage. 4. Over voltage protection to ±25V. 5. Can switch up to ±13V signals with ±15V supplies.	**Features** 1. High speed switch. 2. Low quiescent current resulting in low power consumption. 3. Low leakage resulting in low error term. 4. Lower cost than the comparable speed DG180 Family. 5. Can switch signals almost to the supply rails.	**Features** 1. Low charge injection. 2. Almost as fast as 5140 and DG180 Families. 3. Very low quiescent current resulting in low power consumption. 4. Ultra low leakage.	**Features** 1. Low $r_{DS(on)}$ 2. As fast as the IH5140 Family. 3. Moderate leakage.	**Features** 1. Low $r_{DS(on)}$ 2. Only switch with true chip enable pin. 3. Low cost. 4. Moderate leakage & quiescent current specifications.	Output of switch must go into the virtual ground point of an Op Amp (unless signal is <0.7V). **Features** 1. Very low quiescent current. 2. Does not need driver; can be driven directly by TTL. 3. Low cost.	Can switch positve signals only unless a translator driver is used. **Features** 1. Very low quiescent current. 2. Does not need driver; can be driven directly by TTL. 3. Low cost.
Notes 1. TTL, DTL, CMOS and PMOS compatible. 2. 5048 through 5053 and the IH200 family are 2-chip hybrid devices with 35Ω $r_{DS(on)}$ max @ 25°C. 3. 5040 through 5047 have 75Ω $r_{DS(on)}$ max @ 25°C. 5040 SPST 5041,5048 Dual SPST 5042,5050 SPDT 5043,5051 Dual SPDT 5044 DPST 5045,5049 Dual DPST 5046 DPDT 5047 4PST 5052,5053 Quad SPST 200 Dual SPST 201,202 Quad SPST	**Notes** 1. TTL and CMOS compatible. 2. Pin compatible with the more popular members of the DG180 family. 5140 SPST 5141 Dual SPST 5142 SPDT 5143 Dual SPDT 5144 DPST 5145 Dual DPST	**Notes** 1. TTL, HTL, CMOS and PMOS compatible. 2. Pin for pin compatible with DG180 Family. IH181,182 Dual SPST IH184,185 Dual DPST IH187, 188 SPDT IH190, 191 Dual SPDT	**Notes** 1. DTL, TTL, RTL compatible 2. DG180, 183, 185 and 189 have 10Ω max on resistance but have higher leakage than others in the family. 3. DG181, 184, 187 and 190 have 30Ω max $r_{DS(on)}$. 4. DG182, 185, 188 and 191 have 75Ω max $r_{DS(on)}$. DG180, Dual SPST 181,182 DG183 Dual DPST 184,185 DG186, SPDT 187,188 DG189, Dual SPDT 190,191	**Notes** 1. "A" selection devices have higher speeds. 2. DG426/A family is a slightly downgraded version of the DG126/A series. See spec tables for comparison. DG133, 134, Dual 141, 151, SPST 152 DG126, 129, Dual 140,153, DPST 154 DG143,144, Diff. 146,161, Input 162 SPDT DG139,142, Diff. 145, 163, Input 164 DPDT IH5001, SPST 5002 IH5003, Dual 5004,5005, SPST 5006,5007	**Notes** 1. All switches in 5009 family are SPST. 2. Odd numbered devices are driven by TTL open collector logic. 3. Even numbered devices are driven by TTL low level logic. 4. Commonly used for signals going into the inverting input of Op-Amps. 5009,5010 quad. compensated 5011,5012 quad, uncompensated 5013,5014 triple, compensated 5015,5016 triple, uncompensated 5017,5018 dual, compensated 5019,5020 dual, uncompensated 5021,5022 single, compensated 5023,5024 single, uncompensated	**Notes** 1. All switches in 5025 family are SPST. 2. All devices can be driven by TTL open collector logic. All devices can be driven by low level TTL logic if input signal is less than IV. 3. Commonly used for signals going into the non-inverting input of Op-Amps. 4. Odd numbered devices have 100Ω max $r_{DS(on)}$ @ 25°C. 5. Even numbered devices have 150 max $r_{DS(on)}$ @ 25°C 5025,5026 quad, common drain 5027,5028 quad 5029,5030 triple, common drain 5031,5032 triple 5033,5034, dual, common drain 5035,5036 dual 5037,5038 single

DG111/112
2-Channel Drivers with MOS-FET Switches (Military Series −55°C to +125°C)

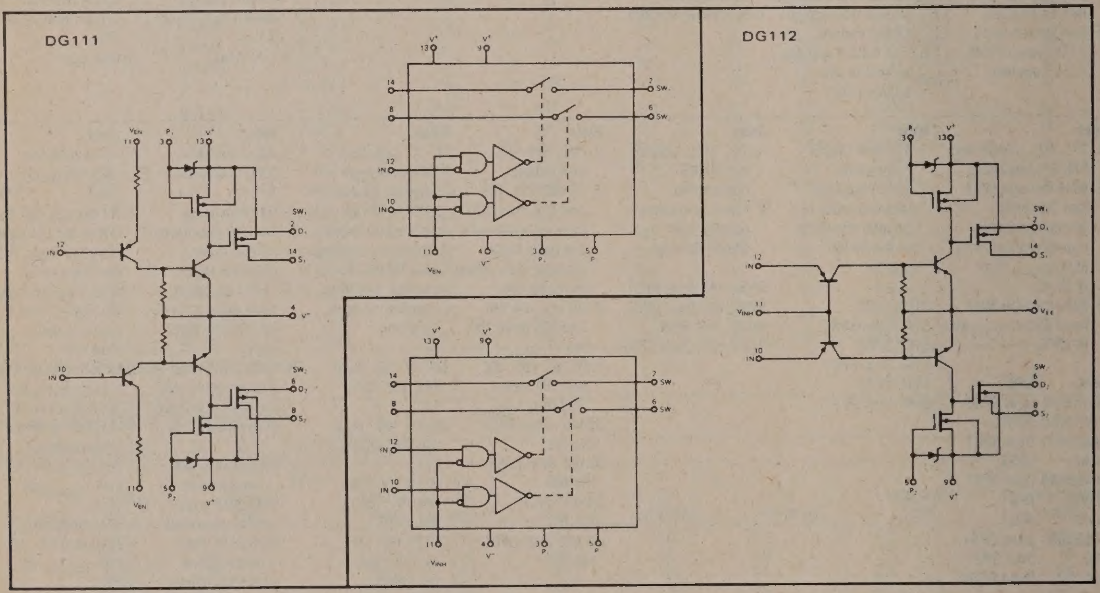
FEATURES

- Each Channel Completely Isolated
- 20V P-P Switching Capability
- Zener Diode Protected Gates
- MOS-FET Current-Source Pull-Up

GENERAL DESCRIPTION

This driver-switch series provides two completely isolated switches per package. The collector supply (V_{CC}) may be operated at different voltages for each switch. Two driver input configurations are available for inverting and non-inverting applications. For minimum propagation delay as well as optimum speed and power, a terminal is supplied for biasing the constant-current MOS-FET pull-up.

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)



ORDERING INFORMATION

DG111 A K

Package
K—14-Pin CERDIP
L—14-Pin Flat Package
P—14-Pin Ceramic DIP (Special Order Only)

Temperature Range
A — Military (−55°C to +125°C)
B — Industrial (−20°C to +85°C)

Device Chip Type

TRUTH TABLE

DG112		DG111		Switch Cond.
V_{IN}	V_{EN}	V_{IN}	V_{INH}	
L	L	L	L	OFF
H	L	L	H	ON
L	H	H	L	OFF
H	H	H	H	OFF

L = 0V, H = V^+

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter ($V^+ - V^-$) 33V
Collector to Pull-Up ($V^+ - V_P$) 33V
Drain to Emitter ($V_D - V^-$) 32V
Drain to Source ($V_D - V_S$) 28V
Source to Drain ($V_S - V_D$) 28V
Source to Emitter ($V_S - V^-$) 32V
Enable to Emitter ($V_{EN} - V^-$) 33V
Inhibit to Emitter ($V_{INH} - V^-$) 31V
Inhibit to Input ($V_{INH} - V_{IN}$) . . . . +6V
Enable to Input ($V_{EN} - V_{IN}$) . . . . ±6V

Current (Any Terminal) 30mA
Storage Temperature . . . . −65°C to +150°C
Operating Temperature . . . . −55°C to +125°C
Dissipation (Note) 750mW
Lead Temperature (Soldering, 10 sec.) . . . . 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of +70°C. Derate 10 mW/°C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

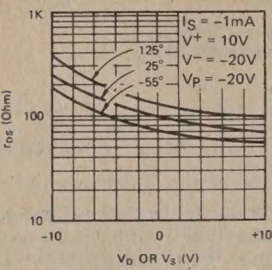
Test conditions unless otherwise specified are as follows: $V_{INH} = 0$, $V_{EN} = 4.5V$, $V^+ = 10V$, $V^- = -20V$, and $P = -20V$. Input ON and OFF test conditions are used for output and power supply specifications.

		PARAMETER (NOTE)	MAX LIMIT				CONDITIONS	
			-55°C	25°C	125°C	UNITS		
INPUT	DG111	$I_{IN(OFF)}$	10	10	20	µA	$V_{IN} = 4.1V$	
		$I_{IN(ON)}$	-0.7	-0.7	-0.7	mA	$V_{IN} = 0.5V$	
	DG112	$I_{IN(OFF)}$	1	1	100	µA	$V_{IN} = 0.4V$	
		$V_{IN(ON)}$	1.3	1.0	0.8	V	$I_{IN} = 1mA$	
OUTPUT	DG111 DG112	$r_{DS(ON)}$	100	100	125	Ω	$V_D = 10V$	$I_S = -100\ \mu A$
			200	200	250	Ω	$V_D = 0$	
			450	450	600	Ω	$V_D = -10V$	
		$I_{D(ON)}$		1	1000	nA	$V_D = 10V$, $I_S = 0$	
		$I_{D(OFF)}$		-1	-1000	nA	$V_S = 10V$, $V_D = 10V$	
		$I_{S(OFF)}$		-1	-1000	nA	$V_D = 10V$, $V_S = -10V$	
POWER SUPPLY	DG111	$I_{L(ON)}$		3		mA	One Channel ON	
	DG112	$I_{R(ON)}$		-0.5				
	DG111	$I_{CC(ON)}$		3				
	DG112	$I_{EE(ON)}$		-6				
	DG111 DG112	$I_{CC(OFF)}$		10		µA	All Channels OFF	
		$I_{L(OFF)}$		10				
		$I_{R(OFF)}$		-15				
		$I_{EE(OFF)}$		-20				
SWITCHING TIMES	DG111 DG112	t_{ON}		300		ns	See Switching Times	
		t_{OFF}		1		µs		

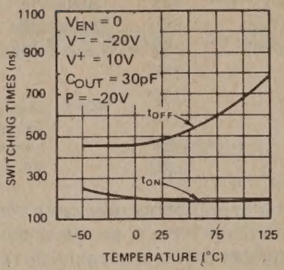
NOTE: (OFF) and (ON) subscripts refer to the conduction state of the MOS-FET switch.

TYPICAL CHARACTERISTICS

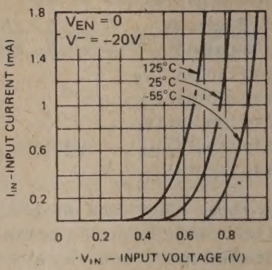
r_{DS} vs V_D OR V_S



SWITCHING TIMES vs TEMPERATURE (DG111, DG112)



I_{IN} vs V_{IN} (DG112)



APPLICATION TIPS

The recommended resistor values for interfacing with RTL, DTL, and T^{2}L Logic is shown in figs. 1 and 2.

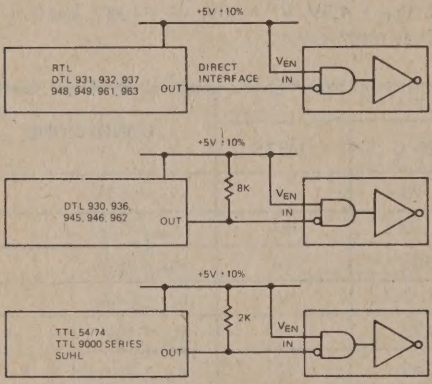

+5V ±10%
RTL
DTL 931, 932, 937
948, 949, 961, 963
OUT
DIRECT INTERFACE
V_{EN}
IN
+5V ±10%
DTL 930, 936,
945, 946, 962
OUT
8K
V_{EN}
IN
+5V ±10%
TTL 54/74
TTL 9000 SERIES
SUHL
OUT
2K
V_{EN}
IN

Figure 1. DG111 Interface

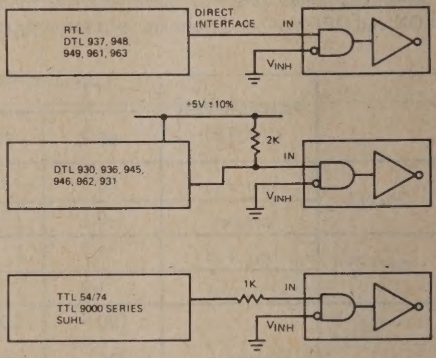
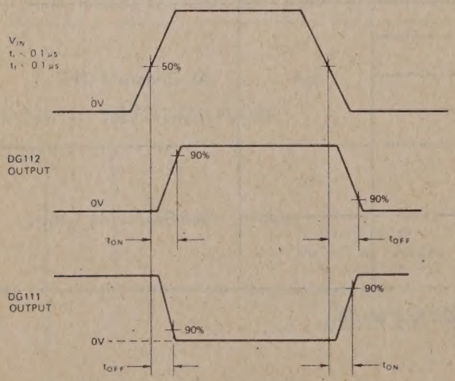

RTL
DTL 937, 948,
949, 961, 963
DIRECT INTERFACE
IN
V_{INH}
+5V ±10%
DTL 930, 936, 945,
946, 962, 931
2K
IN
V_{INH}
TTL 54/74
TTL 9000 SERIES
SUHL
1K
IN
V_{INH}

Figure 2. DG112 Interface

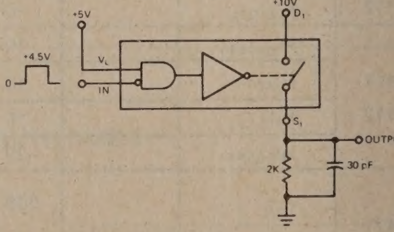
Enable Control

The V_{EN} and V_{INH} terminals can be used as a strobe or an enable control. The requirements for sinking current at V_{EN} or sourcing current at V_{INH} are: $I_{L(ON)}$ x no. of channels used, for DG111, and $I_{R(ON)}$ x no. of channels used, for the DG112. The voltage at V_{INH} must be greater than V_{IN} for $V_{IN} < 4V$. V_{INH} must be at least +4V for $V_{IN} > 4V$.

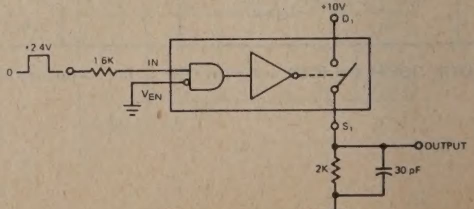
SWITCHING TIMES


V_{IN}
t_r < 0.1 μs
t_f < 0.1 μs
50%
0V
DG112 OUTPUT
90%
0V
90%
t_{ON}
t_{OFF}
DG111 OUTPUT
90%
0V
90%
t_{OFF}
t_{ON}

DG111


+5V
+10V
D_1
+4.5V
0
V_L
IN
S_1
OUTPUT
2K
30 pF

DG112


+10V
D_1
+2.4V
0
1.6K
IN
V_{EN}
S_1
OUTPUT
2K
30 pF

D112/113/120/121 2-Channel FET Switch Drivers (Military Series −55°C to + 125°C)

FEATURES

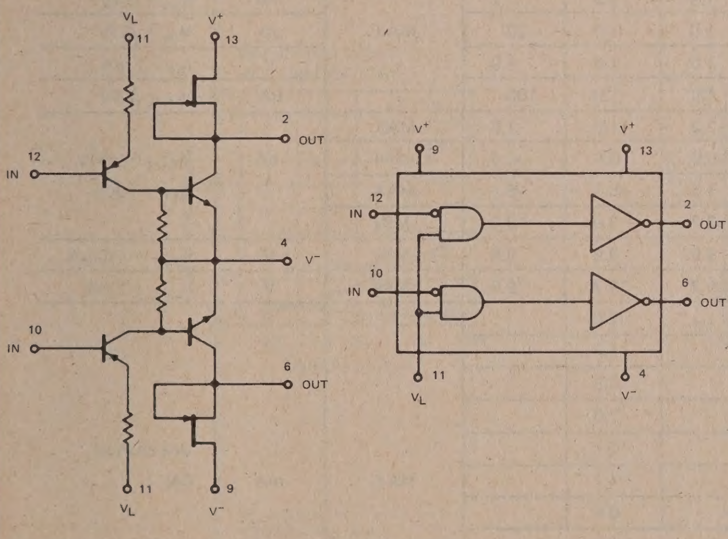
- Two separate channels
- J-FET Collector Pull-up
- Interfaces 5V Logic
- Two switching speeds to choose from

GENERAL DESCRIPTION

This series contains 2 separate channels each with J-FET collector pull-up, in one package. Two switching speeds are provided for speed-power ratio selection.

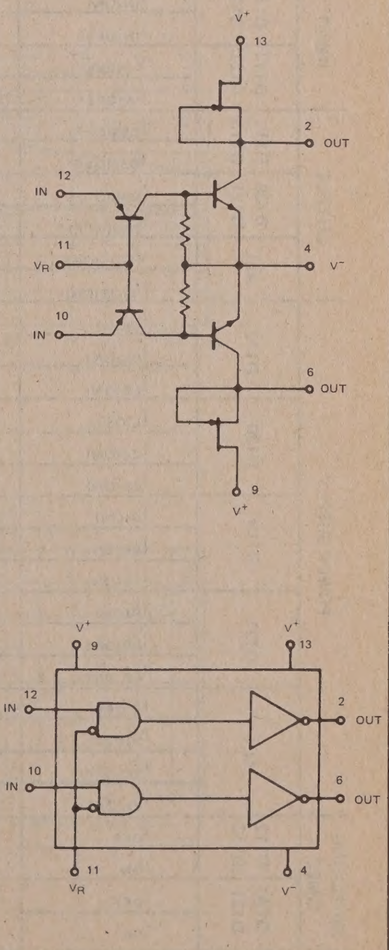
SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)

D112 & D120



V_L
11
V+
13
2
OUT
12
IN
4
V−
10
IN
6
OUT
11
V_L
9
V−
V+
9
V+
13
12
IN
2
OUT
10
IN
6
OUT
11
V_L
4
V−

D113 & D121



V+
13
2
OUT
12
IN
11
V_R
4
V−
10
IN
6
OUT
9
V+
V+
9
V+
13
12
IN
2
OUT
10
IN
6
OUT
11
V_R
4
V−

ORDERING INFORMATION

D113 A K

Package
K — 14-Pin CERDIP
L — 14-Pin Flat Pack ¼" x ¼"
P — 14-Pin Ceramic DIP (Special Order Only)

Temperature Range
A — −55°C to +125°C
B — −20°C to +85°C
C — 0°C to +70°C

Device Chip Type

Pos. Supply to Emitter ($V^+ - V^-$)	33V
Output to Emitter ($V_{OUT} - V^-$)	33V
Logic Supply to Emitter ($V_L - V^-$)	30V
Ref. to Emitter ($V_R - V^-$)	31V
Input to Ref. ($V_{IN} - V_R$)	2V
Ref. to Input ($V_R - V_{IN}$)	6V
Logic Supply to Input ($V_L - V_{IN}$)	±6V
Current (any pin)	30mA

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Dissipation (Note)	750mW
Lead Temperature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70 C. For higher temperatures; derate 10 mW/ C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

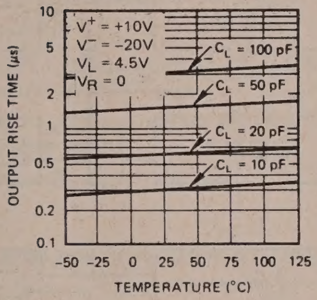
Test conditions unless otherwise specified are as follows: $V^- = -20V$, $V^+ = +10V$, $I_{OUT} = 0$, $V_L = 4.5V$, $V_R = 0$. Output and power supply measurements based on specified input conditions.

		PARAMETER (NOTE)	LIMIT					CONDITION
			−55°C	25°C	125°C	MAX/MIN	UNITS	
INPUT	D112 D120	$I_{IN(ON)}$	1.5	1.5	1.2	MAX	mA	$V_{IN} = 0.4V$
		$I_{IN(OFF)}$	1.0	1.0	20		µA	$V_{IN} = 4.1V$
	D113 D121	$V_{IN(ON)}$	1.3	1.0	0.8		V	$I_{IN} = 1$ mA
		$I_{IN(OFF)}$	1.0	1.0	100		µA	$V_{IN} = 0.4V$
OUTPUT	D112 D113	$I_{DSS(OFF)}$	−2.2	−1.8	−1,8	MAX	mA	$V_{OUT} = -20V$ $V_{EE} = -20V$
		$I_{DSS(OFF)}$	−0.6	−0.4	−0.4	MIN		
	D120 D121	$I_{DSS(OFF)}$	−7.5	−5.7	−5.1	MAX		
		$I_{DSS(OFF)}$	−3.2	−3.0	−2.0	MIN		
	ALL	$V_{OUT(OFF)}$	9.9	9.9	9.8	MIN	V	$I_{OUT} = -10$ µA
		$V_{OUT(ON)}$	−19.2	−19.2	−19.0	MIN	V	$I_{OUT} = 1$ mA
POWER SUPPLY	D112	$I_{L(ON)}$		2.0		MAX	mA	One channel ON
		$I_{CC(ON)}$		1.8				
		$I_{EE(ON)}$		3.8				
	D120	$I_{L(ON)}$		2.0				
		$I_{CC(ON)}$		5.7				
		$I_{EE(ON)}$		7.7				
	D113	$I_{R(ON)}$		0.5				
		$I_{CC(ON)}$		1.8				
		$I_{EE(ON)}$		2.8				
	D121	$I_{R(ON)}$		0.5				
		$I_{CC(ON)}$		5.7				
		$I_{EE(ON)}$		6.7				
	ALL	$I_{L(OFF)}$		250		MAX	µA	All channels OFF
		$I_{R(OFF)}$		150				
		$I_{CC(OFF)}$		50				
		$I_{EE(OFF)}$		250				
SWITCHING TIMES	D112 D113	t_{OFF}		1.5		MAX	µs	(See Switching Times)
		t_{ON}		0.25				
	D120 D121	t_{OFF}		0.60				
		t_{ON}		0.25				

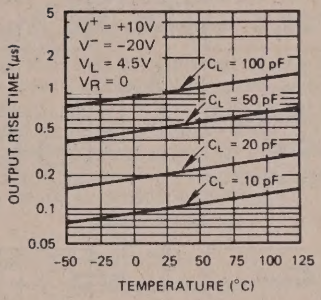
NOTE: (OFF) and (ON) subscripts refer to the conduction state of the driver

TYPICAL PERFORMANCE CURVES

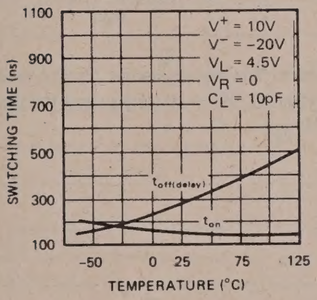
OUTPUT RISE TIME VS TEMPERATURE AND LOAD CAPACITANCE (D112, D113)



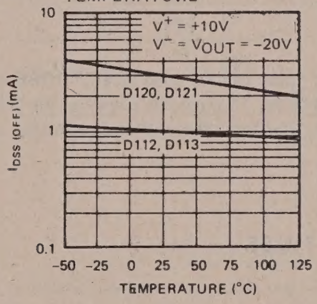
OUTPUT RISE TIME VS TEMPERATURE AND LO. CAPACITANCE (D120, D12



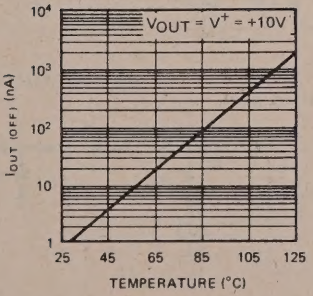
SWITCHING TIMES VS TEMPERATURE



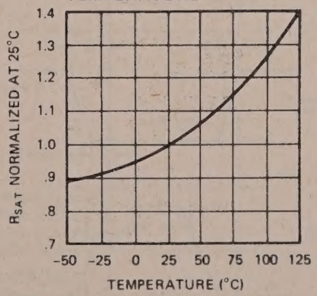
$I_{DSS(OFF)}$ VS TEMPERATURE



$I_{OUT(OFF)}$ VS TEMPERATURE



R_{SAT} VS TEMPERATURE



APPLICATION TIPS

The recommended resistors for interfacing with RTL, DTL, and T^2 L Logic is shown in figures 1 and 2.

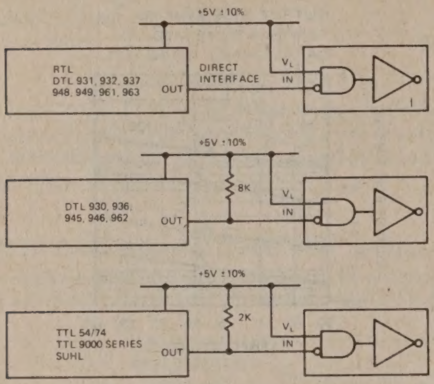

+5V ±10%
RTL
DTL 931, 932, 937
948, 949, 961, 963
OUT
DIRECT INTERFACE
V_L
IN
+5V ±10%
DTL 930, 936,
945, 946, 962
OUT
8K
V_L
IN
+5V ±10%
TTL 54/74
TTL 9000 SERIES
SUHL
OUT
2K
V_L
IN

Figure 1. D112 and D120 Interface

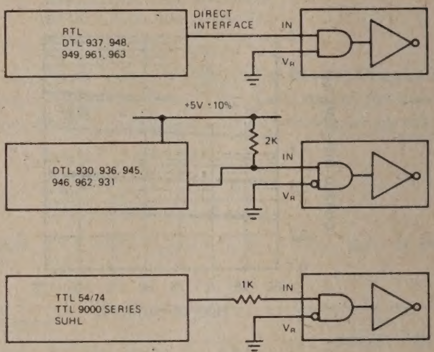
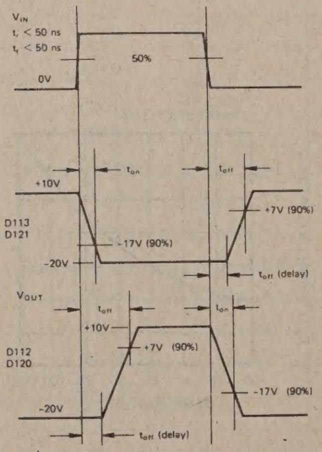

RTL
DTL 937, 948,
949, 961, 963
DIRECT INTERFACE
IN
V_R
+5V ±10%
DTL 930, 936, 945,
946, 962, 931
2K
IN
V_R
TTL 54/74
TTL 9000 SERIES
SUHL
1K
IN
V_R

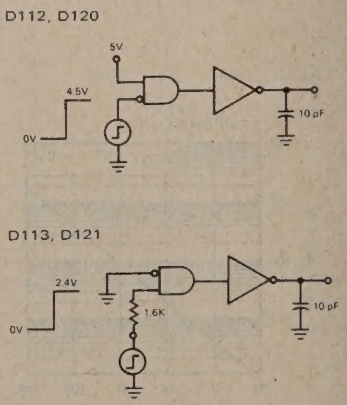
Figure 2. D113 and D121 Interface

Enable Control

The V_R and V_L pins can be used as a STROBE or an ENABLE control. The requirements for the enable driver are as follows: I_L(ON) X no. of channels used for the D112 & D120 and I_R(ON) X no. of channels used for the D113 & D121. The voltage at V_L must be greater than the voltage at V_{IN} by at least +4V.

SWITCHING TIMES




D112, D120
5V
4.5V
0V
10 pF
D113, D121
2.4V
0V
1.6K
10 pF

Circuit Diagrams

INTERSIL

G115/G123
4 and 6-Channel MOS FET Switches Industrial Series −20°C to +85°C

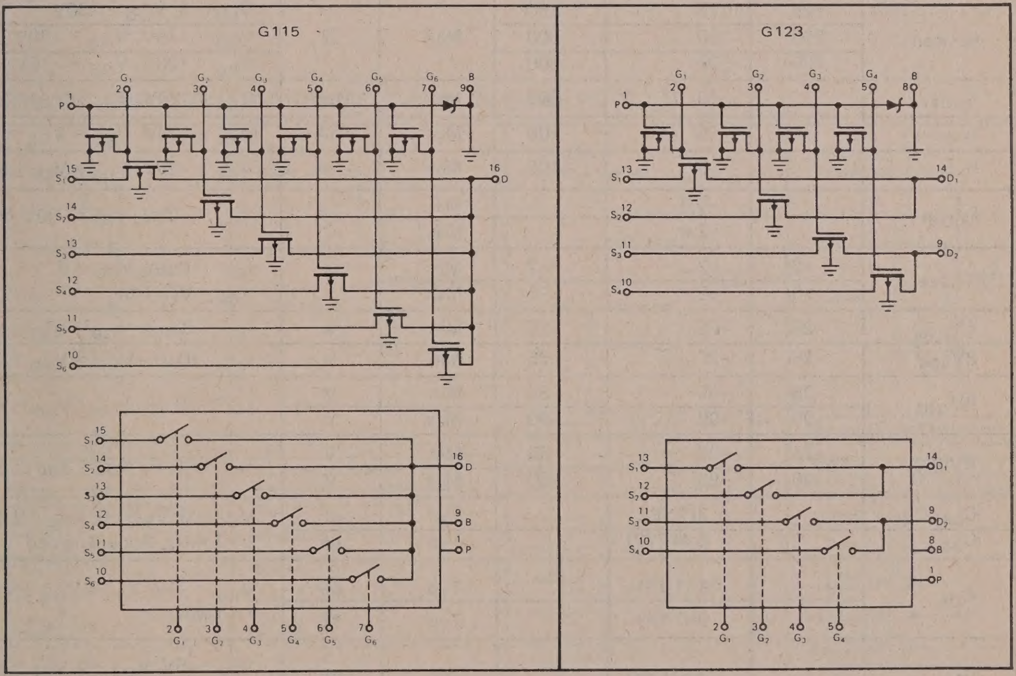
FEATURES

- Integrated MOS-FET Constant-Current Sources for Active Driver-Collector Pull-up
- Integrated Zener Diode Protection for Both Positive and Negative Spike Protection
- P-Channel Enhancement-Type Switches

GENERAL DESCRIPTION

These switches may be connected directly to the INTERSIL switch-driver D123 series without the need of any interfacing components, and are internally protected by a Zener diode integrated on the silicon chip. A MOS-FET used as a current source provides an active pull-up for faster switching capability. The active pull-up FET can be disabled without sacrificing the Zener protection of the gates.

SCHEMATICS AND PIN CONFIGURATIONS (Outline Dwgs DD, FD-2, JD, PD)



ORDERING INFORMATION

G115 A K

Package
J — 14-Pin Plastic DIP
K — 14-Pin CERDIP
L — 14-Pin Flat Package
P — 14-Pin Ceramic DIP (Special Order Only)

Temperature Range
A — Military (−55°C to +125°C)
B — Industrial (−20°C to +85°C)
C — Commercial (0°C to +70°C)

Device Chip Type

NOTE: Plastic package available in commercial and industrial temperature ranges only.

ABSOLUTE MAXIMUM RATINGS (25°C)

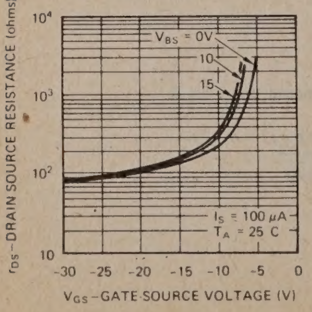
Source Current (I_S)	100mA	Body to Drain ($V_B - V_D$)	−2V to +25V
Drain Current (I_D)	100mA	Body to Gate ($V_B - V_G$)	+35V
Gate Current (I_G)	5mA	Body to Pull-up ($V_B - V_P$)	+35V
Pull-up Control Current (I_P)	100µA	Power Dissipation (derate 10mW/°C above 70°C	750mW
Body to Source ($V_B - V_S$)	−2V to +25V	Lead Temperature (soldering, 10 sec.)	300°C

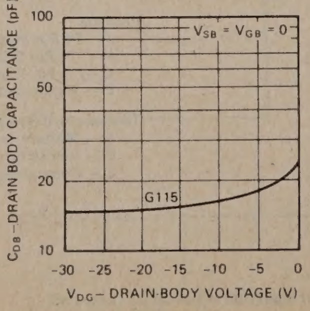
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

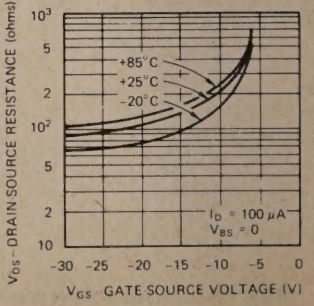
ELECTRICAL CHARACTERISTICS (per channel unless noted)

	PARAMETER	LIMITS					CONDITIONS
		−20°C	25°C	85°C	MIN/ MAX	UNITS	
G115 and G123	$r_{DS(ON)}$	125	125	150	Max	Ω	$V_{BD} = 0, V_{GD} = -30V$ I_S = 1 mA
		250	250	300			$V_{BD} = +10V, V_{GD} = -20V$
		500	500	600			$V_{BD} = +20V, V_{GD} = -10V$
	$I_{D(OFF)}$		−10	−500	Max	nA	$V_{DS} = -20V, V_{BS} = V_{GS} = V_{PS} = 0$
	$I_{S(OFF)}$		−5	−100	Max	nA	$V_{SD} = -20V, V_{BD} = V_{GD} = V_{PD} = 0$
	I_{GBS}		−5	−100	Max	nA	$V_{GB} = -20V, V_{DB} = V_{SB} = V_{PB} = 0$
	$I_{G(ON)}$		−0.8		Min	mA	$V_{GB} = -30V, V_{PB} = -30V, V_{DB} = 0$
			−2.4		Max		
	$V_{GS(th)}$	−2	−2	−2	Min	V	$I_S = -10\ \mu A, V_{DG} = 0,$ $V_{BS} = V_{PS} = 0$
		−6	−6	−6	Max		
	BV_{DSS}	−25	−25	−25	Min	V	$I_D = -10\ \mu A, V_{GB} = V_{BS} = V_{PS} = 0$
	BV_{SDS}	−25	−25	−25	Min	V	$I_S = -10\ \mu A, V_{GD} = V_{BD} = V_{PD} = 0$
	BV_{GBS}	−35	−35	−35	Min	V	$I_G = -10\ \mu A, V_{DB} = V_{SB} = V_{PB} = 0$
		−90	−90	−90	Max	V	
	BV_{PBS}	−35	−35	−35	Min	V	$I_P = -10\ \mu A, V_{DB} = V_{SB} = V_{GB} = 0$
		−90	−90	−90	Max	V	
	C_{GS}, C_{GD}		3(TYP)		Typ	pF	$V_{GB} = 0, V_{SB} = 0, V_{DB} = 0, V_{PB} = 0$
	C_{DS}		0.4(TYP)		Typ	pF	f = 1 mHz, Body Guarded
G115	C_{DB}		18 (TYP)		Typ	pF	$V_{DB} = -5V, V_{SB} = V_{GB} = V_{PB} = 0$
G123			9 (TYP)		Typ	pF	f = 1 MHz
Both	C_{SB}		3.5(TYP)		Typ	pF	$V_{SB} = -5V, V_{DB} = 0, V_{GB} = V_{PB} = 0$ f = 1 MHz

TYPICAL CHARACTERISTICS







INTERSIL

DG116/118/123/125
4 and 5-Channel Driver-MOS-FET Switch Combinations (Military Series −55°C to +125°C)

FEATURES

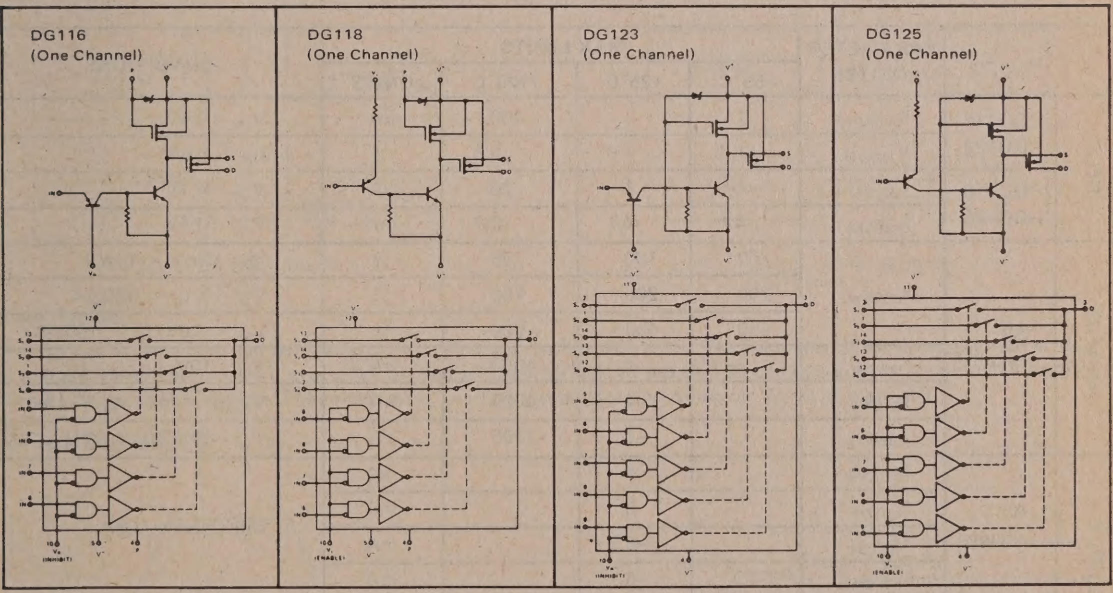
- Available With and Without Programmable Constant Current pull-up
- Zener Protection on All Gates
- P-Channel Enhancement-Type MOS-FET Switches
- Each Switch Summed to One Common Point

GENERAL DESCRIPTION

This series includes devices with four and five channel switching capability. Each channel is composed of a driver and a MOS-FET switch. Two driver versions are supplied for inverting and noninverting applications. A MOS-FET, used as a current source provides an active pull-up for faster switching.

An external biasing connection is brought out for biasing the current source for optimization of speed and power.

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)



ORDERING INFORMATION

DG116 A K

Package
K — 14-pin CERDIP
L — 14-pin Flat Package
P — 14-Pin Ceramic DIP (Special Order Only)

Temperature Range
A — Military (−55°C to +125°C)
B — Industrial (−20°C to +85°C)

Device Chip Type

TRUTH TABLE

DG116, DG123		DG118, DG125		Switch Cond.
V_{IN}	V_R	V_{IN}	V_L	
L	L	L	L	OFF
H	L	L	H	ON
L	H	H	L	OFF
H	H	H	H	OFF

L = 0V, H = +V

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter $(V^+ - V^-)$	33V
Collector to Pull-up $(V^+ - V_P)$	33V
Drain to Emitter $(V_D - V^-)$	32V
Source to Emitter $(V_S - V^-)$	32V
Drain to Source $(V_D - V_S)$	28V
Source to Drain $(V_S - V_D)$	28V
Logic to Emitter $(V_L - V^-)$	33V
Reference to Emitter $(V_R - V^-)$	31V
Reference to Input $(V_R - V_{IN})$	6V
Logic to Input $(V_L - V_{IN})$	±6V
Input to Emitter $(V_{IN} - V^-)$	33V
Current (any terminal)	30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Dissipation (Note)	750mW
Lead Temperature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

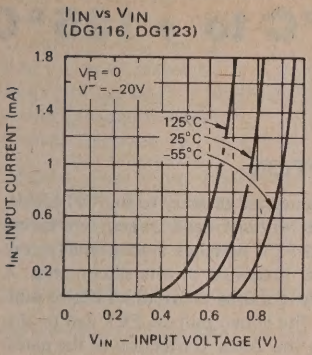
ELECTRICAL CHARACTERISTICS

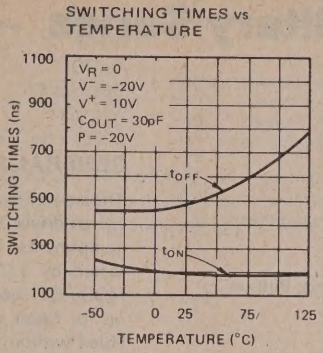
Test conditions unless specified otherwise are as follows: V_L = 4.5V, V_R = 0, V^- = −20V, and P = −20V. Input ON and OFF test conditions used for output and power supply specifications.

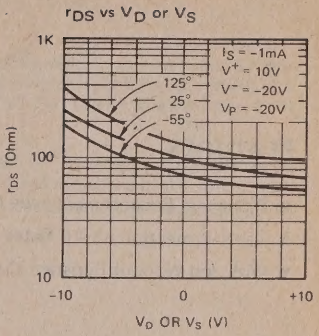
		PARAMETER (NOTE)	MAX LIMITS				CONDITIONS
			−55°C	+25°C	+125°C	UNITS	
INPUT	DG116 DG123	$I_{IN(OFF)}$	1	1	100	μA	V_{IN} = 0.4V
		$V_{IN(ON)}$	1.3	1.0	0.8	V	I_{IN} = 1 mA
	DG118 DG125	$I_{IN(OFF)}$	1	1	20	μA	V_{IN} = 4.1V
		$I_{IN(ON)}$	−0.7	−0.7	−0.7	mA	V_{IN} = 0.5V
OUTPUT	All circuits	$r_{DS(ON)}$	100	100	125	Ω	V_D = 10V, I_S = −1mA
			200	200	250	Ω	V_D = 0, I_S = −100 μA
			450	450	600	Ω	V_D = −10V, I_S = −100 μA
		$I_{D(ON)}$		4	4000	nA	V_D = 10V, $I_{S(all)}$ = 0
		$I_{D(OFF)}$		−4	−4000	nA	$V_{S(all)}$ = 10V, V_D = −10V
		$I_{S(OFF)}$		−1	−1000	nA	V_D = 10V, V_S = −10V
POWER SUPPLY	All circuits	$I_{CC(ON)}$		3		mA	One Channel (ON)
		$I_{L(ON)}$		3		mA	
		$I_{R(ON)}$		−0.5		mA	
		$I_{EE(ON)}$		−6		mA	
	All circuits	$I_{CC(OFF)}$		10		μA	All Channels (OFF)
		$I_{L(OFF)}$		10		μA	
		$I_{R(OFF)}$		−15		μA	
		$I_{EE(OFF)}$		−20		μA	
SWITCHING TIMES	All circuits	$t_{(ON)}$		0.3		μs	See Switching Times
		$t_{(OFF)}$		1		μs	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the MOS-FET switch for the given test condition.

TYPICAL CHARACTERISTICS


I_{IN} vs V_{IN} (DG116, DG123)


SWITCHING TIMES vs TEMPERATURE


r_{DS} vs V_D or V_S

APPLICATION TIPS

The recommended resistor values for interfacing RTL, DTL, and T²L Logic are shown in Figures 1 and 2.

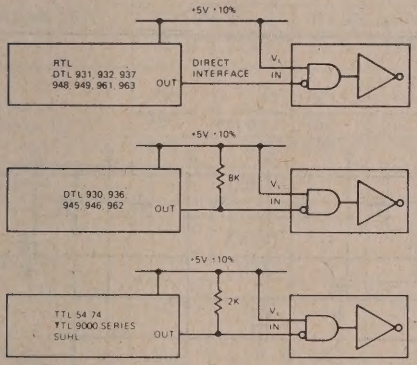

+5V ±10%
RTL
DTL 931, 932, 937
948, 949, 961, 963
OUT
DIRECT INTERFACE
VL
IN
+5V ±10%
DTL 930, 936,
945, 946, 962
OUT
8K
VL
IN
+5V ±10%
TTL 54 74
TTL 9000 SERIES
SUHL
OUT
2K
VL
IN

Figure 1. DG118 and DG125 Interface

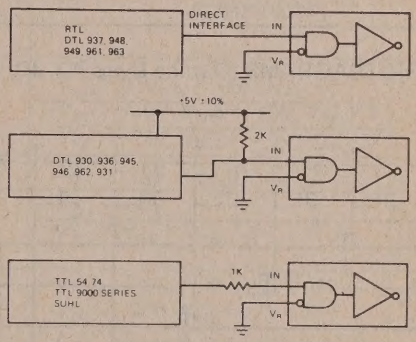
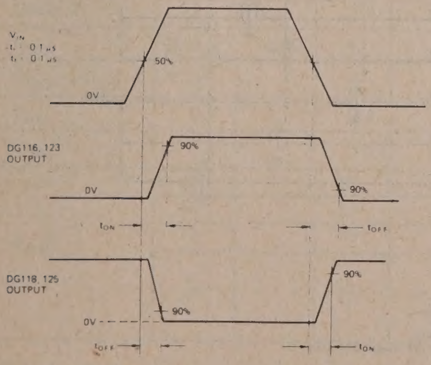

RTL
DTL 937, 948,
949, 961, 963
DIRECT INTERFACE
IN
VR
+5V ±10%
2K
IN
DTL 930, 936, 945,
946, 962, 931
VR
TTL 54 74
TTL 9000 SERIES
SUHL
1K
IN
VR

Figure 2. DG116 and DG123 Interface

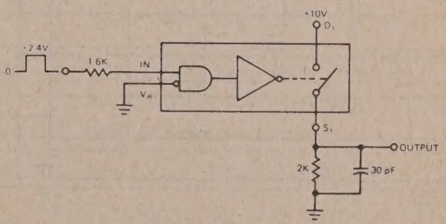
Enable Control

The V_R and V_L terminals can be used as either a Strobe or an Enable control. The requirements for sinking current at V_R or sourcing current at V_L are: $I_{L(ON)}$ x No. of channels used, for DG118 and DG125, and $I_{R(ON)}$ x No. of channels used, for the DG116 and DG123 devices. The voltage at V_L must be greater than the voltage at V_{IN} by at least +4V.

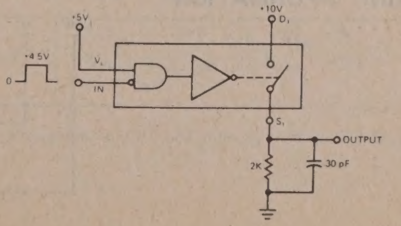
SWITCHING TIMES


VIN
tr = 0.1 μs
tf = 0.1 μs
50%
0V
DG116, 123 OUTPUT
90%
0V
90%
tON
tOFF
DG118, 125 OUTPUT
90%
0V
90%
tOFF
tON

DG116, 123


+10V
D1
+2.4V
0
1.6K
IN
VR
S1
OUTPUT
2K
30 pF

DG118, 125


+5V
+10V
D1
+4.5V
0
VL
IN
S1
OUTPUT
2K
30 pF

G116 — G119
5 and 6-Channel MOS-FET Switches Military Series −55°C to +125°C

FEATURES

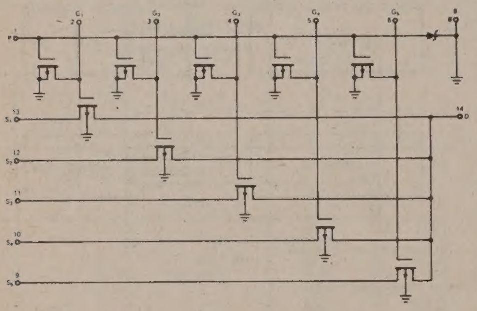
- P-Channel Enhancement-type MOS-FET Switches
- Zener Protection on All Gates
- With and Without Constant Current Source Pull-up

GENERAL DESCRIPTION

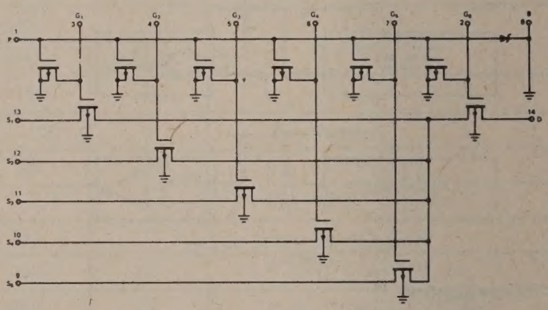
These switches may be connected directly to the INTERSIL switch-driver D123 series without need of any interfacing components. These MOS-FET switches are internally protected by a Zener diode integrated on the silicon chip. A MOS-FET used as a current source provides an active pull-up for faster switching. The active pull-up FET can be disabled without sacrificing the Zener protection of the gates.

LOGIC DIAGRAMS (Outline Dwgs PD, JD, FD-2, DD)

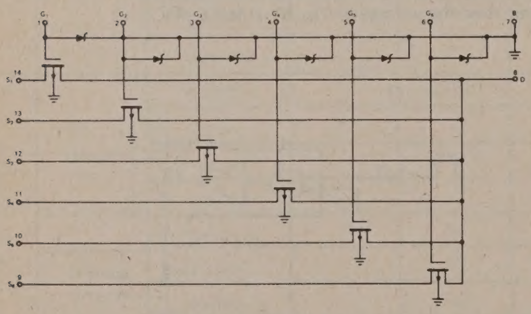
G116


G1 2
G2 3
G3 4
G4 5
G5 6
8
P 1
S1 13
14 D
S2 12
S3 11
S4 10
S5 9

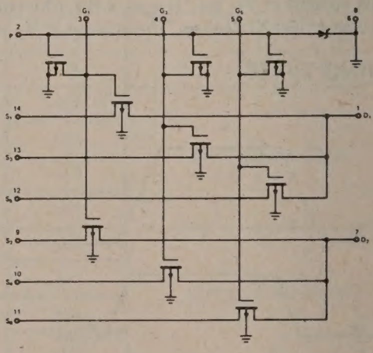
G117


G1 3
G2 4
G3 5
G4 6
G5 7
G6 2
8
P 1
S1 13
14 D
S2 12
S3 11
S4 10
S5 9

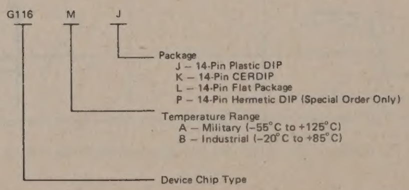
G118


G1 1
G2 2
G3 3
G4 4
G5 5
G6 6
7
S1 14
8 D
S2 13
S3 12
S4 11
S5 10
S6 9

G119


G1 3
G2 4
G3 5
6
P 2
S1 14
1 D1
S2 13
S3 12
S4 9
7 D2
S5 10
S6 11

ORDERING INFORMATION



G116 M J

Package
J – 14-Pin Plastic DIP
K – 14-Pin CERDIP
L – 14-Pin Flat Package
P – 14-Pin Hermetic DIP (Special Order Only)

Temperature Range
A – Military (−55°C to +125°C)
B – Industrial (−20°C to +85°C)

Device Chip Type

ABSOLUTE MAXIMUM RATINGS (25°C)

Source Current (I_S)	100 mA
Drain Current (I_D)	100 mA
Control Gate Current I_G	5 mA
Pull-Up Gate Current I_P	100 µA
Body Voltage (V_B) to Any Terminal	-2 to +30V
Power Dissipation (Note)	750 mW
Storage Temperature	-55°C to +150°C

Operating Temperature	-50°C to +125°C
Lead Temperature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10 mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel unless noted)

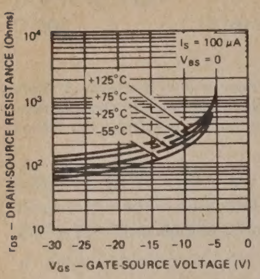
References to pull-up gate P do not apply to G118.

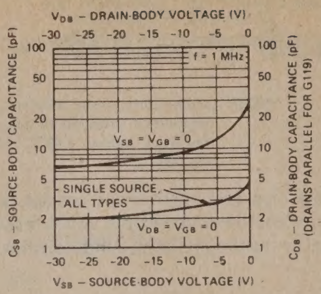
PARAMETER	LIMITS						CONDITIONS	
	G116M Series		G116C Series		MIN/MAX	UNITS		
	25°C	125°C	25°C	125°C				
$r_{DS(ON)}$ (Note 1)	100	125	125		Max	Ω	$V_{BD} = 0, V_{GD} = -30V, V_{PB} = 0$	I_S = -1mA
	200	250	250				$V_{BD} = +10V, V_{GD} = -20V, V_{PB} = 0$	
	450	600	600				$V_{BD} = +20V, V_{GD} = -10V, V_{PB} = 0$	
$I_{S(OFF)}$	-0.5	-500	-1		Max	nA	$V_{SD} = -20V, V_{BD} = V_{GD} = V_{PD} = 0$	
$I_{D(OFF)}$	-2.5	-2500	-5		Max	nA	$V_{DS} = -20V$	G116
	-3.0	-3000	-6				$V_{BD} = V_{GD} = V_{PD} = 0$	G118
	-1.5	-1500	-3					G119
	-0.5	-500	-1		Max	nA	V_{G1B} to $V_{G5B} = 0, V_{G6B} = -30V$ $V_{DB} = -20V, V_{SB} = V_{PB} = 0$	G117
BV_{DSS}	-30		-30		Min	V	$I_D = -10\ \mu A, V_{GS} = V_{BS} = V_{PS} = 0$	
BV_{SDS}	-30		-30		Min		$I_S = -10\ \mu A, V_{GD} = V_{BD} = V_{PD} = 0$	
BV_{GBS}	-30		-30		Min		$I_G = -10\ \mu A, V_{PB} = V_{SB} = V_{DB} = 0$	
	-90		-90		Max			
BV_{PBS}	-30		-30		Min		$I_P = -10\ \mu A, V_{GB} = V_{SB} = V_{DB} = 0$	
	-90		-90		Max			
$V_{GD(th)}$	-2		-2		Min		$I_S = -10\ \mu A, V_{DS} = -10V, V_{SB} = 0$	
	-6		-6		Max			
$I_{G(ON)}$ (Note 2)	-0.5		-0.3		Min	mA	$V_{GB} = -30V, V_{PB} = -30V, V_{SB} = V_{DB} = 0$	
	-2		-2.5		Max			
I_{GSS}	-0.5	-500	-1		Max	nA	$V_{GB} = -20V, V_{DS} = V_{BS} = V_{PS} = 0$	
C_{GD} or C_{GS}	3		3		Max	pF	$V_{PB} = 0, V_{BS} = 0$, or $V_{BD} = 0$	
C_{SD}	0.4		0.4		Max	pF	Body Guarded, f = 1 mHz	
C_{SB}	3.5		3.5		Max	pF	$V_{PB} = V_{GB} = V_{DB} = 0, V_{SB} = -5V$, f = 1 mHz	
C_{DB}	18		18		Max	pF	$V_{PB} = V_{GB} = V_{SB} = 0$ $V_{DB} = -5V$, f = 1 mHz	G116
	18		18					G118
	10		10					G119
	20		20		Max	pF	$V_{G6B} = -30V, V_{PB} = V_{SB} = 0$ V_{G1B} to $V_{G5B} = 0, V_{DB} = -5V$, f = 1 mHz	G117

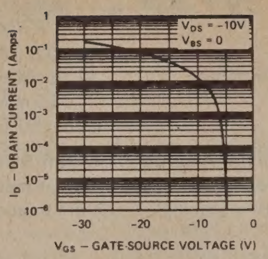
NOTE 1: For the G117 this is the resistance from each of the source terminals (5 terminals) and the one drain terminal to the internal junction of the output MOS-FETs.

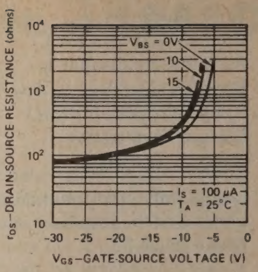
NOTE 2: Not applicable to G118.

TYPICAL CHARACTERISTICS





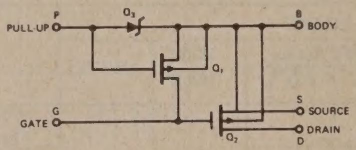




APPLICATION TIPS

Description of Analog Switch

Single Channel


P
PULL-UP
Q_3
B
BODY
Q_1
G
GATE
S
SOURCE
DRAIN
D
Q_2

G-Terminal – This is the control terminal of the switch; the voltage at this terminal determines the conduction state of Q_2. To insure conduction of Q_2 when voltages between ±10V are switched, the gate voltage (V_G) should be at least 10V more negative than the most negative voltage to be switched (–10V). Therefore, V_G should go to –20V. To insure turn-off V_G should not be less than the most positive voltage to be switched, +10V. For convenience the same potential as the body could be used.

B-Terminal – This terminal is connected to the body (substrate) of the chip and must be maintained at a voltage that is equal to or greater than the most positive voltage to be switched. This is to insure that the drain-to-body or the source-to-body junctions do not become forward biased.

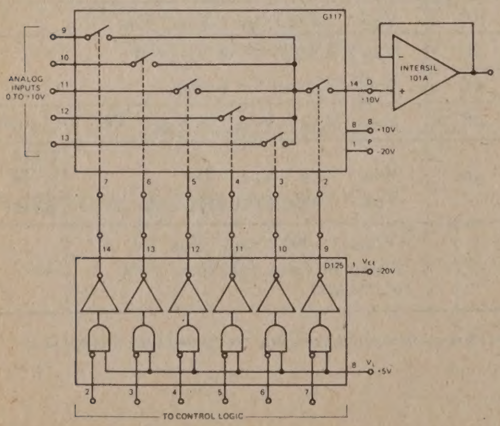
P-Terminal – The potential, with respect to the body, at this terminal determines the gate-to-source voltage of Q_1 which determines the amount of drain current available for driver-collector pull-up. Shorting terminal P to B prevents Q_1 and Q_3 from conducting, but still allows the body-to-drain junction of Q_1 to act as a forward biased diode for positive gate voltages, and to act as a Zener diode for negative voltages which exceed BV_{DSS} (–30 to –90V) for protecting the gate of Q_2.

D-Terminal – The common point of the MOS-FET switches (summing point).

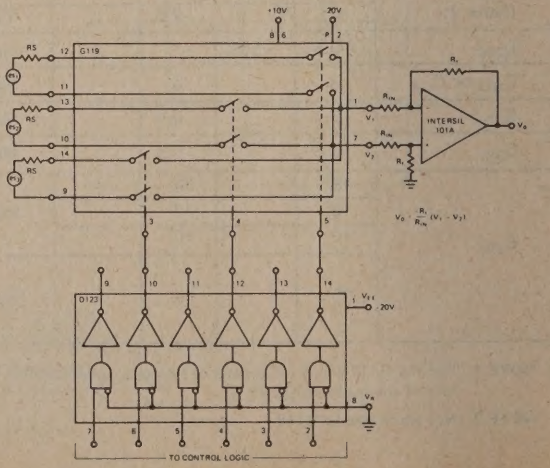
S-Terminal – This is the normally-open terminal of the MOS-FET switch and is normally used as the input.

APPLICATIONS

5-Channel Multiplexer With Series Switch


G117
ANALOG INPUTS 0 TO +10V
9
10
11
12
13
14 D
+10V
8 B +10V
1 P -20V
INTERSIL 101A
-
+
7 6 5 4 3 2
14 13 12 11 10 9
D125
1 V_{EE} -20V
8 V_L +5V
2 3 4 5 6 7
TO CONTROL LOGIC

3-Channel Differential Multiplexer


+10V
20V
B 6
P 2
RS
12
G119
e_{S1}
11
13
RS
e_{S2}
10
14
RS
e_{S3}
9
R_f
1
R_{IN}
V_1
7
R_{IN}
V_2
R_f
INTERSIL 101A
V_o
$V_O = \frac{-R_f}{R_{IN}}(V_1 - V_2)$
3 4 5
9 10 11 12 13 14
D123
1 V_{EE} -20V
8 V_R
7 6 5 4 3 2
TO CONTROL LOGIC

DG120/DG121
3-Channel Drivers with Differential Switches
Military Series −55°C to +125°C

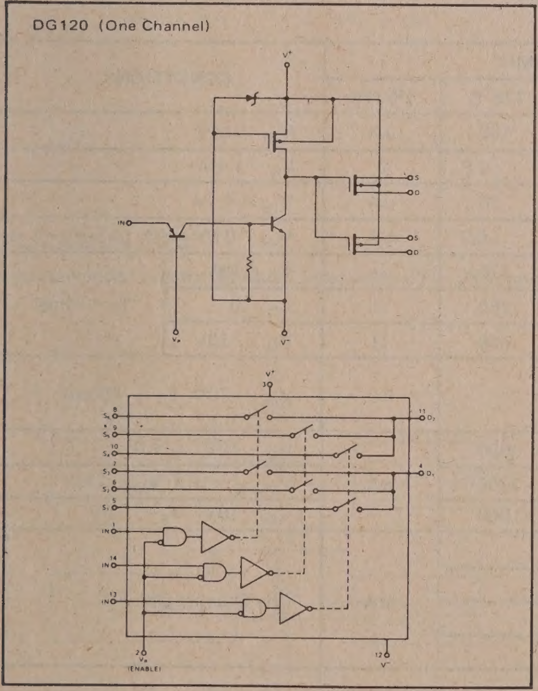
FEATURES

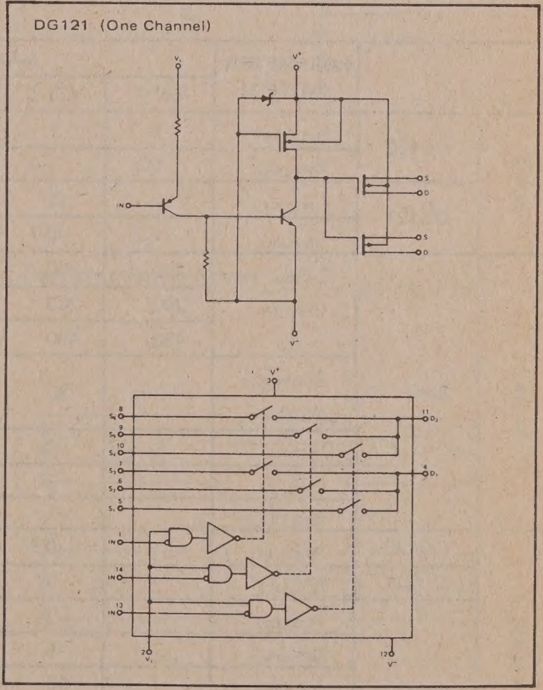
- 3-Channel With Normally-Off MOS-FET Switches in One Package
- $\Delta r_{DS(ON)}$ Matched to Better Than 30Ω.

GENERAL DESCRIPTION

This series is composed of three channels in one package. Each channel is composed of two matched MOS-FET switches for differential input requirements. Two driver configurations are available for inverting and noninverting applications. A MOS-FET used as a current source provides an active pull-up load for faster switching.

SCHEMATIC AND LOGIC DIAGRAM (Outline Dwgs DD, FD-2, JD)


DG120 (One Channel)
V+
IN
S
D
S
D
V_R
V−
3
8
9
10
7
6
5
1
14
13
11
4
D₁
D₂
IN
IN
IN
2
V_R
(ENABLE)
12
V−


DG121 (One Channel)
V_L
V+
IN
S
D
S
D
V−
3
8
9
10
7
6
5
1
14
13
11
4
D₁
D₂
IN
IN
IN
2
V_L
12
V−

ORDERING INFORMATION

DG120 A K

Package
K—14-Pin CERDIP
L—14-Pin Flat Package
P—14-Pin Ceramic DIP (Special Order Only)

Temperature Range
A — Military (−55°C to +125°C)
B — Industrial (−20°C to +85°C)

Device Chip Type

TRUTH TABLE

DG120		DG121		Switch Cond.
V_{IN}	V_R	V_{IN}	V_L	
L	L	L	L	OFF
H	L	L	H	ON
L	H	H	L	OFF
H	H	H	H	OFF

L = 0V, H = +V

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter ($V^+ - V^-$)	33V
Collector to Pull-Up ($V^+ - V_P$)	33V
Drain to Emitter ($V_D - V^-$)	32V
Source to Emitter ($V_S - V^-$)	32V
Drain to Source ($V_D - V_S$)	28V
Source to Drain ($V_S - V_D$)	28V
Logic Emitter ($V_L - V^-$)	33V
Ref. to Emitter ($V_R - V^-$)	31V
Ref. to Input ($V_R - V_{IN}$)	+6V
Logic to Input ($V_L - V_{IN}$)	±6V
Current (Any Terminal)	30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Dissipation (Note)	750mW
Lead Temperature (Soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

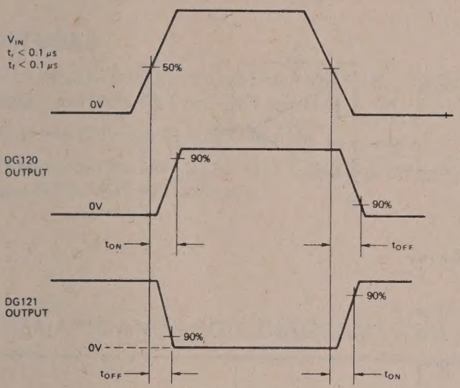
Test conditions unless otherwise specified are as follows: $V_R = 0$, $V_L = 4.5V$, $V^+ = 10V$, $V^- = -20V$. Input ON and OFF test conditions are used for output and power supply specifications.

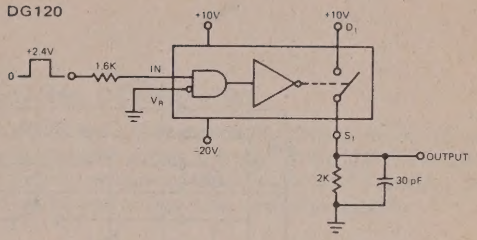
		PARAMETER (NOTE 1)	MAX LIMIT				CONDITIONS	
			−55°C	+25°C	+125°C	UNITS		
INPUT	DG120	$I_{IN(OFF)}$	1	1	100	μA	$V_{IN} = 0.4V$	
		$V_{IN(ON)}$	1.3	1.0	0.8	V	$I_{IN} = 1\ mA$	
	DG121	$I_{IN(OFF)}$	10	10	20	μA	$V_{IN} = 4.1V$	
		$I_{IN(ON)}$	−0.7	−0.7	−0.7	mA	$V_{IN} = 0.5V$	
OUTPUT	Both	$r_{DS(ON)}$	100	100	125	Ω	$V_D = 10V$	$I_S = -1mA$
			200	200	250	Ω	$V_D = 0$	
			450	450	600	Ω	$V_D = -10V$	
		$\Delta r_{DS(ON)}$ (Note 2)		30		Ω	$V_D = -10V$, $I_S = -100\mu A$	
		$I_{D(ON)}$		3	3000	nA	$V_D = 10V$, $I_S = 0$	
		$I_{D(OFF)}$		−3	−3000		$V_{S(all)} = 10V$, $V_D = -10V$	
		$I_{S(OFF)}$		−1	−1000		$V_D = 10V$, $V_S = -10V$	
POWER SUPPLY	DG120	$I_{R(ON)}$		−0.5		mA	One Channel ON	
	DG121	$I_{L(ON)}$		3				
	Both	$I_{CC(ON)}$		3				
		$I_{EE(ON)}$		−6				
		$I_{CC(OFF)}$		10		μA	All Channels OFF	
		$I_{L(OFF)}$		10				
		$I_{R(OFF)}$		−15				
		$I_{EE(OFF)}$		−20				
SWITCHING TIMES	Both	t_{ON}		300		ns	See Switching Times	
		t_{OFF}		2		μs		

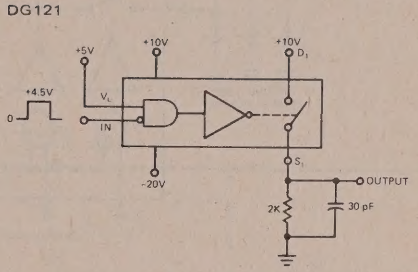
NOTE 1: (OFF) and (ON) subscripts refer to the conduction state of the MOS-FET switch.

NOTE 2: $\Delta r_{DS(ON)}$ is the resistance difference between differential switches.

SWITCHING TIMES

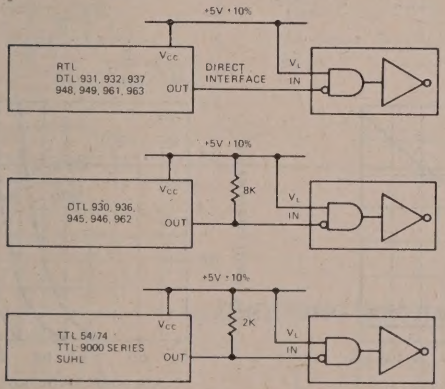


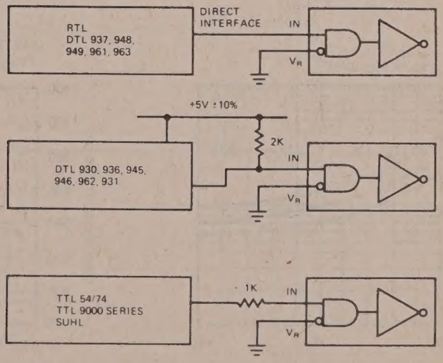

DG120
+10V
+10V
D_1
+2.4V
0
1.6K
IN
V_R
-20V
S_1
OUTPUT
2K
30 pF


DG121
+10V
+10V
D_1
+5V
V_L
+4.5V
0
IN
-20V
S_1
OUTPUT
2K
30 pF

APPLICATION TIPS

The recommended resistor values for interfacing RTL, DTL, and T^2L Logic are shown in Figures 1 and 2.

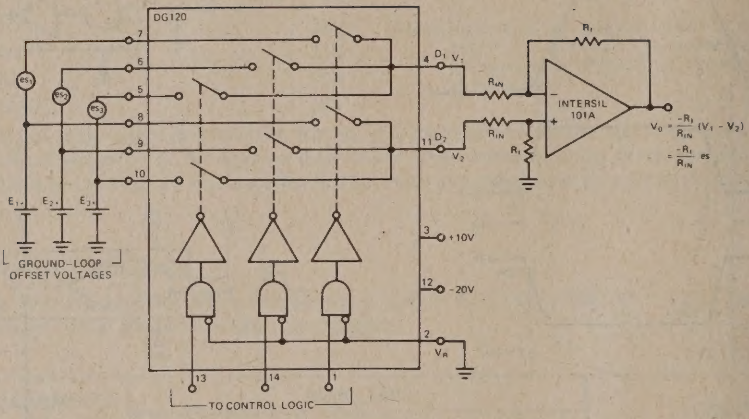

+5V ± 10%
V_{CC}
RTL
DTL 931, 932, 937
948, 949, 961, 963
OUT
DIRECT INTERFACE
V_L
IN
+5V ± 10%
V_{CC}
DTL 930, 936,
945, 946, 962
OUT
8K
V_L
IN
+5V ± 10%
V_{CC}
TTL 54/74
TTL 9000 SERIES
SUHL
OUT
2K
V_L
IN


RTL
DTL 937, 948,
949, 961, 963
DIRECT INTERFACE
IN
V_R
+5V ± 10%
DTL 930, 936, 945,
946, 962, 931
2K
IN
V_R
TTL 54/74
TTL 9000 SERIES
SUHL
1K
IN
V_R

Enable Control

The V_R and V_L terminals can be used as a strobe or an enable control. The requirements for sinking current at V_R or sourcing current at V_L are: $I_{L(ON)}$ x No. of channels used, for DG121 and $I_{R(ON)}$ x No. of channels used, for DG120. The voltage at V_L must be greater than V_{IN} for $V_{IN} < 4V$. V_L must be at least +4V for $V_{IN} > 4V$.

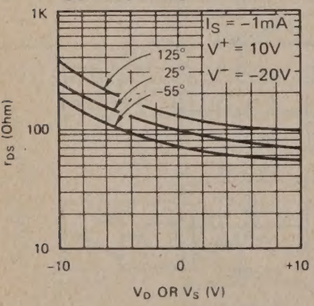
APPLICATIONS


DG120
7
6
5
8
9
10
es1
es2
es3
E1
E2
E3
GROUND-LOOP OFFSET VOLTAGES
4 D1 V1
11 D2 V2
RIN
RIN
Rf
Rf
INTERSIL 101A
Vo = -Rf/RIN (V1 - V2)
= -Rf/RIN es
3 +10V
12 -20V
2 VR
13
14
1
TO CONTROL LOGIC

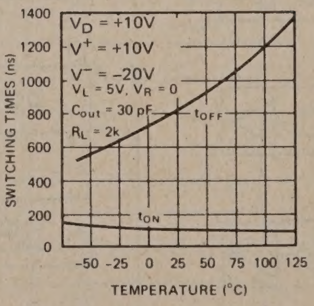
3-Channel Differential Multiplexer

TYPICAL CHARACTERISTICS

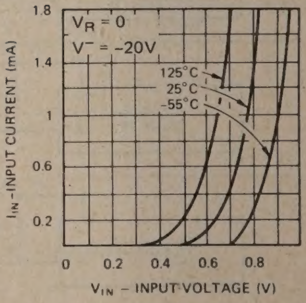
r_{DS} vs V_D or V_S



SWITCHING TIMES vs TEMPERATURE



I_{IN} vs V_{IN} (DG120)



D123/D125
6-Channel FET Switch Drivers
Military Series −55°C to +125°C

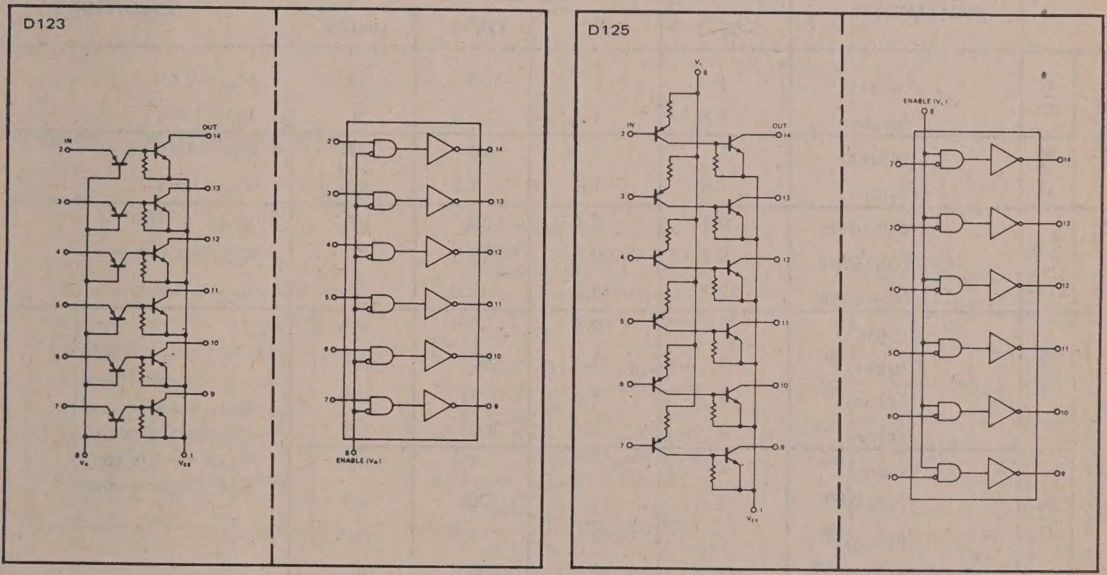
FEATURES

- Provides DC level shifting between low-level Logic and MOS-FET or J-FET switches
- External Collector Pull-ups required
- Direct interface with G116, G117, G119, G115, and G123 MOS-FET switches

GENERAL DESCRIPTION

The D123 and D125 monolithic bi-polar drivers convert low-level positive signals (0 & +5V) to the high level positive and negative voltages necessary to drive FET switches. One lead can be used to provide an enabling capability.

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)



ORDERING INFORMATION

D123 A K

Package
K – 14-Pin CERDIP
L – 14-Pin Flat Pack
P – 14-Pin Hermetic DIP (Special Order Only)

Temperature Range
A – Military (−55°C to +125°C)
B – Industrial (−20°C to +85°C)

Device Chip Type

ABSOLUTE MAXIMUM RATINGS

Input-to-Emitter Voltage ($V_{IN} - V_{EE}$)	33V
Output-to-Emitter Voltage ($V_O - V_{EE}$)	33V
Logic Supply-to-Emitter Voltage ($V_L - V_{EE}$)	27V
Input-to-Reference Voltage ($V_{IN} - V_R$)	2V
Input-to-Logic Supply Voltage ($V_{IN} - V_L$)	+6V
Reference-to-Emitter Voltage ($V_R - V_{EE}$)	31V
Maximum Dissipation (Note)	750 mW
Current (any pin)	30 mA

Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10 mW/°C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

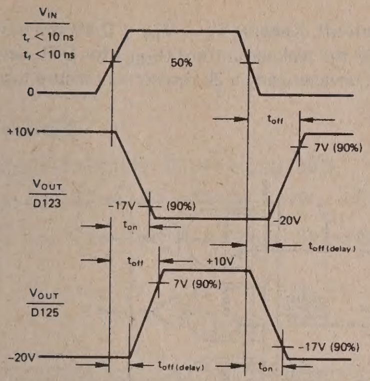
ELECTRICAL CHARACTERISTICS

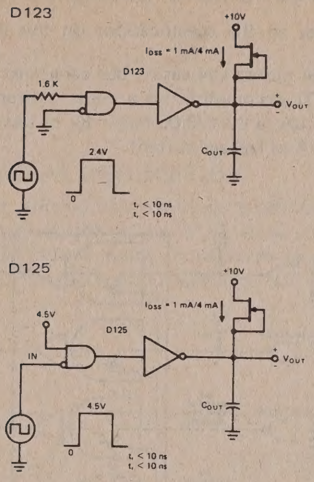
Test conditions unless otherwise specified are as follows: $V_{EE} = -20V$, $V_L = 4.5V$, $I_{OUT} = 0$, $V_R = 0$. Output and power supply measurements based on specified input conditions.

		PARAMETER	MAX LIMIT				CONDITIONS
			-55°C	25°C	125°C	UNITS	
INPUT	D123	$I_{IN(OFF)}$	1	1	100	μA	$V_{IN} = 0.4V$
		$V_{IN(ON)}$	1.3	1	0.8	V	$I_{IN} = 1$ mA
	D125	$I_{IN(OFF)}$	1	1	20	μA	$V_{IN} = 4.1V$
		$I_{IN(ON)}$	1.5	1.5	1.2	mA	$V_{IN} = 0.5V$
OUTPUT	D125 & D123	$I_{OUT(OFF)}$	0.1	0.1	10	μA	$V_{OUT} = +10V$
		$V_{OUT(ON)}$	-19.7	-19.7	-19.5	V	$I_{OUT} = 1$ mA
		$V_{OUT(ON)}$	-19.2	-19.2	-19.0	V	$I_{OUT} = 4$ mA
POWER SUPPLY	D123	$I_{R(ON)}$ (1)	0.5	0.5	0.5	mA	$I_{OUT} = 0$ for ON measurements. $V_{OUT} = +10V$ for OFF measurements.
		$I_{R(OFF)}$ (2)	1	1	150	μA	
		$I_{EE(ON)}$ (1)	1	1	1	mA	
		$I_{EE(OFF)}$ (2)	2	2	200	μA	
	D125	$I_{L(ON)}$ (1)	2	2	1.9	mA	
		$I_{L(OFF)}$ (2)	1	1	100	μA	
		$I_{EE(ON)}$ (1)	2	2	1.9	mA	
		$I_{EE(OFF)}$ (2)	2	2	200	μA	
SWITCHING TIMES	D125 & D123	$t_{(on)}$		250		ns	$I_{OUT} = 1$ mA C_{OUT}(3) = 10 pF
		$t_{(off)}$ (4)		800		ns	(See Switching Times)
		$t_{(on)}$		250		ns	$I_{OUT} = 4$ mA C_{OUT}(3) = 10 pF
		$t_{(off)}$ (5)		600		ns	(See Switching Times)

NOTES:
(1) One channel ON, 5 channels OFF.
(2) All channels OFF.
(3) Add 30 ns per pF for 1 mA and add 8 ns per pF for 4 mA for additional capacitive loading.
(4) For Dual-In-Line package add 120 ns to $t_{(off)}$.
(5) For Dual-In-Line package add 30 ns to $t_{(off)}$.

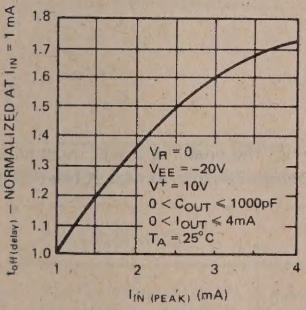
SWITCHING TIMES


V_IN
t_r < 10 ns
t_f < 10 ns
50%
0
+10V
t_off
7V (90%)
V_OUT D123
-17V
(90%)
-20V
t_on
t_off (delay)
t_off
+10V
7V (90%)
V_OUT D125
-17V (90%)
-20V
t_off (delay)
t_on

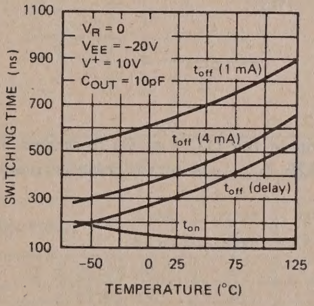

D123
+10V
I_DSS = 1 mA/4 mA
D123
1.6 K
V_OUT
C_OUT
2.4V
0
t_r < 10 ns
t_f < 10 ns
D125
+10V
I_DSS = 1 mA/4 mA
4.5V
D125
IN
V_OUT
C_OUT
4.5V
0
t_r < 10 ns
t_f < 10 ns

Circuit Diagrams

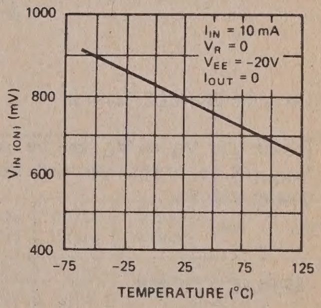
TYPICAL CHARACTERISTICS



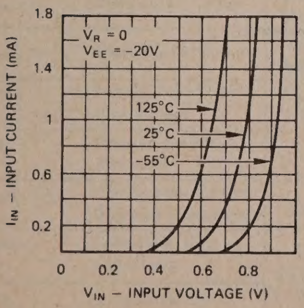
$t_{off(delay)}$ VS $I_{IN(PEAK)}$ D123



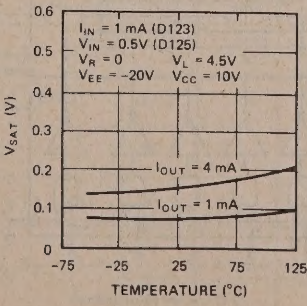
SWITCHING TIMES VS TEMPERATURE D123 AND D125 (SEE NOTES 4 AND 5)



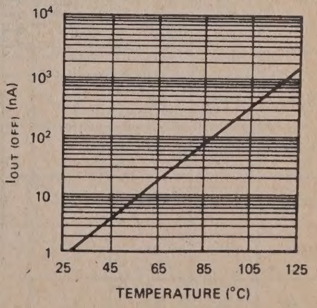
$V_{IN(ON)}$ VS TEMPERATURE D123



I_{IN} VS V_{IN} D123



V_{SAT} VS TEMPERATURE D123 AND D125



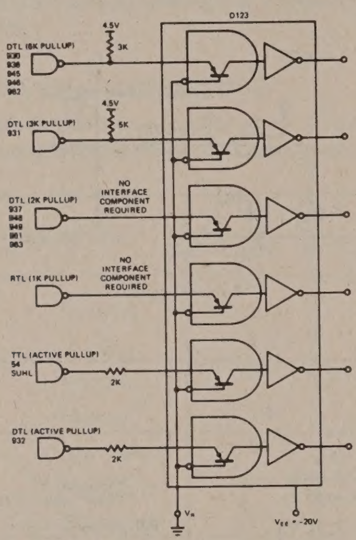
$I_{OUT(OFF)}$ VS TEMPERATURE D123 AND D125

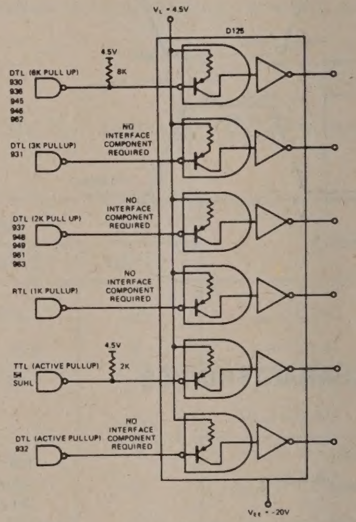
APPLICATION TIPS

Interfacing the D123 and D125

In order to meet all the specifications on this data sheet, certain requirements must be met by the drive circuitry.

The D125 can be turned ON easily, but care must be exercised to insure turn-off. Keeping $V_L - V_{IN} \leq 0.4V$ is a must to insure turn-off. To accomplish this a shunt resistor must be added to supply the leakage current (I_{CES}) for DTL devices. Since $I_{CES} = 50\ \mu A$, a 0.4V/0.05 mA = 8k or less should be used. For T^2L devices using a 2k resister will insure turn-off with up to 200 μA of leakage current.


D123
4.5V
3K
DTL (6K PULLUP)
930
936
945
946
962
4.5V
5K
DTL (3K PULLUP)
931
NO
INTERFACE
COMPONENT
REQUIRED
DTL (2K PULLUP)
937
948
949
961
963
NO
INTERFACE
COMPONENT
REQUIRED
RTL (1K PULLUP)
TTL (ACTIVE PULLUP)
54
SUHL
2K
DTL (ACTIVE PULLUP)
932
2K
V_R
V_{EE} = -20V

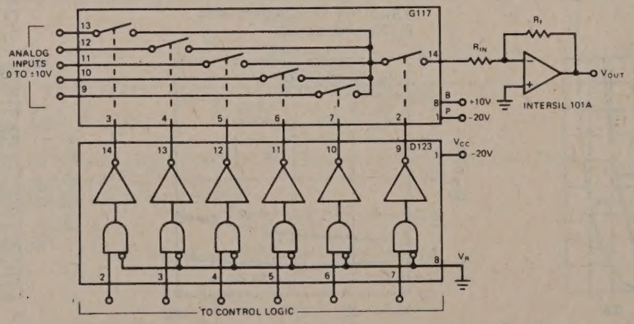

V_L = 4.5V
D125
4.5V
8K
DTL (6K PULL UP)
930
936
945
946
962
NO
INTERFACE
COMPONENT
REQUIRED
DTL (3K PULLUP)
931
NO
INTERFACE
COMPONENT
REQUIRED
DTL (2K PULL UP)
937
948
949
961
963
NO
INTERFACE
COMPONENT
REQUIRED
RTL (1K PULLUP)
4.5V
2K
TTL (ACTIVE PULLUP)
54
SUHL
NO
INTERFACE
COMPONENT
REQUIRED
DTL (ACTIVE PULLUP)
932
V_{EE} = -20V

Using the ENABLE Control

Device pins V_R or V_L, can be used to enable the D123 or D125 drivers. For the D123 the enabling driver must sink $I_{R(ON)}$ X no. of channels used. For the D125, $I_{L(ON)}$ X no. of channels used must be sourced with a voltage at least +4V greater than V_{IN}.

APPLICATIONS

Using INTERSIL'S MOS-FET SWITCH G117 with either the D123 or D125 drivers provides a reliable means of providing up to 5 channels with a series block for multiplexing applications.


G117
ANALOG
INPUTS
0 TO ±10V
13
12
11
10
9
14
3
4
5
6
7
2
8
1
B
P
+10V
-20V
R_f
R_{IN}
V_{OUT}
INTERSIL 101A
D123
14
13
12
11
10
9
1
V_{CC}
-20V
8
V_R
2
3
4
5
6
7
TO CONTROL LOGIC

5-Channel Multiplexer

G125 — G13
G1330/40/50/6
4-Channel Junction FET Switches

FEATURES

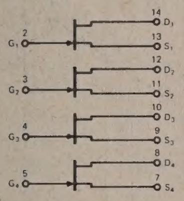
- $r_{DS(ON)} < 10$ ohms: G1340 and G1360
- $I_{D(OFF)} < 50$ pA: G125, G126, G129 and G130
- C_{DG}, $C_{SG} < 2$ pF: G125, G126, G129 and G130

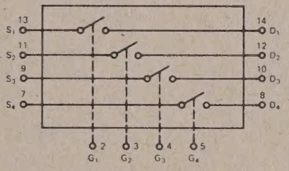
GENERAL DESCRIPTION

These switches consist of four N-Channel Junction FETS in a single package. In the G129, G130, G131, G132, G1350 and G1360 the drains are common to assist the designer in applications such as multiplexing.

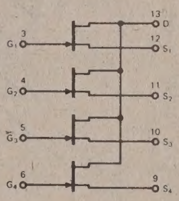
PIN CONFIGURATIONS (Outline dwgs DD, FD-2, JD)

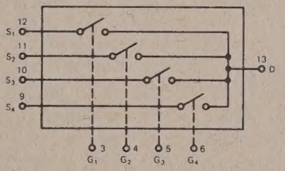
G125, G126,
G127, G128
G1330 AND G1340


2 G₁
14 D₁
13 S₁
3 G₂
12 D₂
11 S₂
4 G₃
10 D₃
9 S₃
5 G₄
8 D₄
7 S₄


13 S₁
11 S₂
9 S₃
7 S₄
14 D₁
12 D₂
10 D₃
8 D₄
2 G₁
3 G₂
4 G₃
5 G₄

G129, G130,
G131, G132
G1350 AND G1360


13 D
3 G₁
12 S₁
4 G₂
11 S₂
5 G₃
10 S₃
6 G₄
9 S₄


12 S₁
11 S₂
10 S₃
9 S₄
13 D
3 G₁
4 G₂
5 G₃
6 G₄

ELECTRICAL CHARACTERISTICS per channel (25°C unless otherwise noted)

CHARACTERISTIC		TEST CONDITIONS		G125 G129	G126 G130	G127 G131	G128 G132	G1330 G1350	G1340 G1360	UNIT	LIMIT
I_{GSS}	Gate Reverse Current	V_{GS} = -20V, V_{DS} = 0	25°C	-0.1	-0.1	-0.2	-0.2	-5.0	-5.0	nA	Max
			125°C	-0.1	-0.1	-0.2	-0.2	-5.0	-5.0	μA	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1 μA, V_{DS} = 0		-40	-40	-40	-40	-30	-30	V	Min
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = 10V, I_D = 0.1 μA		-5	-10	-5	-10	-5	-10	V	Max
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = 10V V_{GS} = -10V	25°C	0.05	0.05	0.1	0.1	0.5	0.5	nA	Max
			125°C	0.05	0.05	0.1	0.1	0.5	0.5	μA	
$I_{S(OFF)}$	Source Cutoff Current	V_{SD} = 10V V_{GD} = -10V	25°C	0.05	0.05	0.1	0.1	0.5	0.5	nA	Max
			125°C	0.05	0.05	0.1	0.1	0.5	0.5	μA	
I_{DSS}	Drain Current at Zero Gate Voltage	V_{DS} = 10V, V_{GS} = 0 (Pulsed)		0.5	2	5	10	15	30	mA	Min
r_{DS}	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0, f = 1 kHz		500	250	90	45	20	10	Ω	Max
$C_{DG} + C_{SG}$	Gate-Source plus Gate-Drain ON Capacitance	V_{GS} = 0, V_{DS} = 0, f = 1 MHz		10	10	40	40	300	300	pF	Max
C_{DG}	Drain-Gate OFF Capacitance	V_{GS} = -10V, V_{DS} = 0, f = 1 MHz		2	2	7	7	16	16	pF	Max
C_{SG}	Source-Gate OFF Capacitance			2	2	7	7	16	16	pF	Max

ABSOLUTE MAXIMUM RATINGS

Gate-Drain or Gate-Source Voltage	−40V
Gate Current	50 mA
Total Device Dissipation Free Air (Note)	500 mW
Storage Temperature Range	−65 to +150°C
Operating Temperature	−65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperatures, derate the device at the rate of 6.7 mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

G125 A K

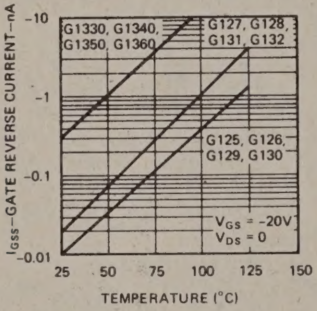
Package
- K — 14-Pin CERDIP
- L — 14-Pin Flat Pack
- P — 14-Pin Ceramic DIP (Special Order Only)

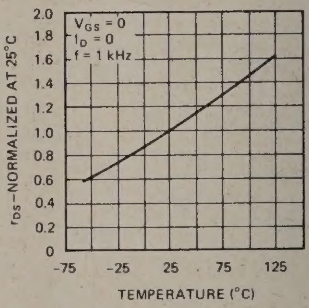
Temperature Range
- A — Military −55°C to +125°C
- B — Industrial −20°C to +85°C

Device Chip Type

NOTE: Ceramic DIP available for military temperature range only.

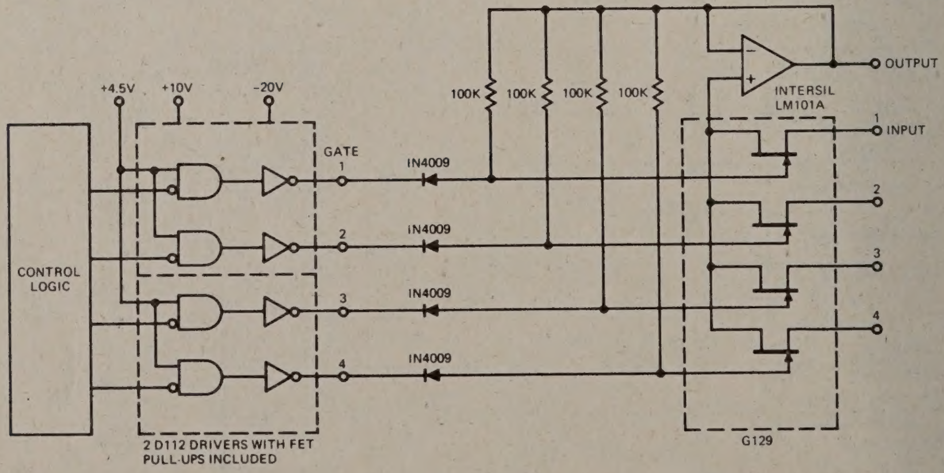
TYPICAL CHARACTERISTICS





APPLICATION

4-Channel Commutator Circuit


+4.5V
+10V
−20V
CONTROL LOGIC
GATE
1
2
3
4
IN4009
IN4009
IN4009
IN4009
100K
100K
100K
100K
INTERSIL LM101A
OUTPUT
INPUT
1
2
3
4
G129
2 D112 DRIVERS WITH FET PULL-UPS INCLUDED

INPUT RANGE: −10 to +10V
GATE: LOGIC "1" FOR SWITCH ON
LOGIC "0" FOR SWITCH OFF

INTERSIL

DG126, DG129, DG13
DG134, DG140, DG141
DG151, DG152, DG153, DG154
2-Channel Drivers with SPST and DPST FET Switches

FEATURES

- Each channel complete—interfaces with most integrated logic
- Low OFF power dissipation, 1 mW
- Switches analog signals up to 20 volts peak-to-peak
- Low $r_{DS(ON)}$, 10 ohms max on DG140/A and DG141/A
- Switching times improved 100% – 'A' Versions.

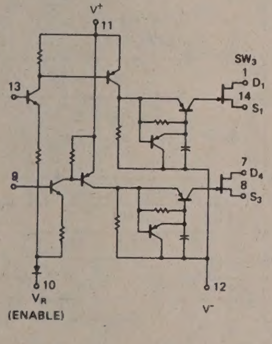
GENERAL DESCRIPTION

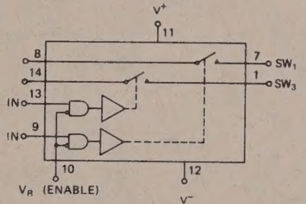
These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST or DPST junction FET switch. The driver interfaces DTL, TTL or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF.

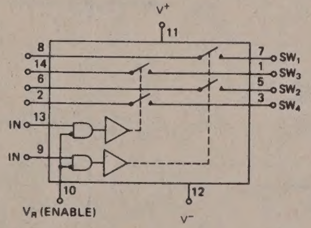
SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)

DUAL SPST

DG133($r_{DS(ON)}$ = 30 Ω)
DG134($r_{DS(ON)}$ = 80 Ω)
DG141($r_{DS(ON)}$ = 10 Ω)
DG151($r_{DS(ON)}$ = 15 Ω)
DG152($r_{DS(ON)}$ = 50 Ω)

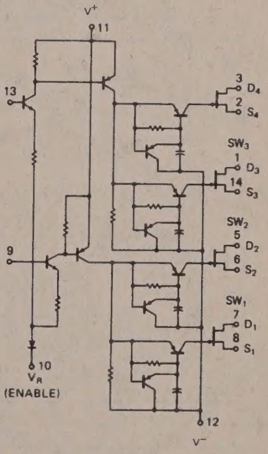

V⁺
11
13
SW₃
1
D₁
14
S₁
9
7
D₄
8
S₃
10
V_R
(ENABLE)
12
V⁻


V⁺
11
8
14
7
SW₁
1
SW₃
IN
13
IN
9
10
V_R (ENABLE)
12
V⁻


V⁺
11
8
14
6
2
7
SW₁
1
SW₃
5
SW₂
3
SW₄
IN
13
IN
9
10
V_R (ENABLE)
12
V⁻

DUAL DPST

DG126($r_{DS(ON)}$ = 80 Ω)
DG129($r_{DS(ON)}$ = 30 Ω)
DG140($r_{DS(ON)}$ = 10 Ω)
DG153($r_{DS(ON)}$ = 15 Ω)
DG154($r_{DS(ON)}$ = 50 Ω)


V⁺
11
13
3
D₄
2
S₄
SW₃
1
D₃
14
S₃
SW₂
5
D₂
6
S₂
9
SW₁
7
D₁
8
S₁
10
V_R
(ENABLE)
12
V⁻

ORDERING INFORMATION

DG126 A K

Package
K = 14-Pin CERDIP
L = 14-Pin Flat Pack
P = 14-Pin Ceramic DIP (Special Order Only)

Temperature Range
A = Military −55°C to +125°C
B = Industrial −20°C to +80°C

Device Chip Type

ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V^-$ or $V^+ - V_A$) 30V
Total Supply Voltage ($V^+ - V^-$). 36V
Pos. Supply Voltage to Ref. Voltage ($V^+ - V_R$). 25V
Ref. Voltage to Neg. Supply Voltage ($V_R - V^-$) 22V
Power Dissipation (Note) . . . . 750 mW
Current (any terminal) . . . . .30 mA

Storage Temperature . . . . –65 to +150°C
Operating Temperature . . . . –55 to +125°C
Lead Temperature (Soldering, 10 sec) . . . . 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS PER CHANNEL

Applied voltages for all test: DG126, DG129, DG133, DG134, DG140, DG141 ($V^+ = +12V$, $V^- = -18V$, $V_R = 0$) and DG151, DG152, DG153, DG154 ($V^+ = +15V$, $V^- = -15V$, $V_R = 0$). Input test condition which guarantees FET switch ON and OFF as specified is used for output and power supply specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT			UNITS	TEST CONDITIONS
				-55°	25°	125°		
INPUT	$V_{IN(ON)}$	Input Voltage–On	All Circuits	2.9 min	2.5 min	2.0 min	Volts	$V_2 = -12V$
	$V_{IN(OFF)}$	Input Voltage–Off		1.4	1.0	0.6	Volts	$V_2 = -12V$
	$I_{IN(ON)}$	Input Current		120	60	60	μA	$V_{IN} = 2.5V$
	$I_{IN(OFF)}$	Input Leakage Current		0.1	0.1	2	μA	$V_{IN} = 0.8V$
SWITCH OUTPUT	$r_{DS(ON)}$	Drain-Source On Resistance	DG126 DG134	80	80	150	Ω	
			DG129 DG133	30	30	50	Ω	$V_D = 10V$, $I_S = 1$ mA
			DG140 DG141	10	10	20	Ω	$V_D = 10V$, $I_S = -10$ mA
			DG151 DG153	15	15	30	Ω	$V_D = 7.5V$, $I_S = 1$ mA
			DG152 DG154	50	50	100	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG126 DG129 DG133 DG134		2	100	nA	$V_D = V_S = -10V$
	$I_{S(OFF)}$	Source Leakage Current			1	100	nA	$V_S = 10V$, $V_D = -10V$
	$I_{D(OFF)}$	Drain Leakage Current			1	100	nA	$V_D = 10V$, $V_S = -10V$
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG140 DG141		2	100	nA	$V_D = V_S = -10V$
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	$V_S = 10V$, $V_D = -10V$
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	$V_D = 10V$, $V_S = -10V$
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG151 DG153		2	500	nA	$V_D = V_S = -7.5V$
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	$V_S = 7.5V$, $V_D = -7.5V$
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	$V_D = 7.5V$, $V_S = -7.5V$
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG152 DG154		2	500	nA	$V_D = V_S = -7.5V$
	$I_{S(OFF)}$	Source Leakage Current			2	200	nA	$V_S = 7.5V$, $V_D = -7.5V$
	$I_{D(OFF)}$	Drain Leakage Current			2	200	nA	$V_D = 7.5V$, $V_S = -7.5V$
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		3		mA	One Driver ON, $V_{IN} = 2.5V$
	$I_{2(ON)}$	Negative Power Supply Drain Current			-1.8		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			-1.4		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	Both Drivers OFF, $V_{IN} = 0.8V$
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			-25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			-25		μA	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

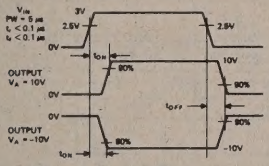
ELECTRICAL CHARACTERISTICS PER CHANNEL (cont.)

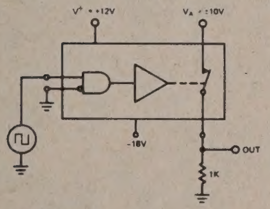
	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT -55°	25°	125°	UNITS	TEST CONDITIONS
SWITCHING	t_{ON}	Turn-On Time	DG126, DG129 DG133, DG134 DG152, DG154		600		ns	See Below
			DG126, DG129 DG133, DG134 DG152, DG154		300	500	ns	
	t_{OFF}	Turn-Off Time	DG126, DG129 DG133, DG134 DG152, DG154		1.6		μs	See Below
			DG126, DG129 DG133, DG134 DG152, DG154		0.8	1.2	μs	
	t_{ON}	Turn-On Time	DG140, DG141 DG151, DG153		1.0		μs	See Below
			DG140, DG141 DG151, DG153		0.5	0.8	μs	
	t_{OFF}	Turn-Off Time	DG140, DG141 DG151, DG153		2.5		μs	See Below
			DG140, DG141 DG151, DG153		1.25	1.8	μs	
POWER	P_{ON}	ON Driver Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5V
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1V

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

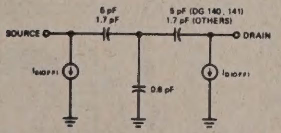
SWITCHING TIMES (at 25°C)

DG126, 129, 133, 134,
140, 141

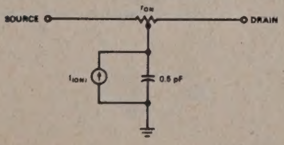



V⁺ = +12V
V_A = ±10V
-18V
OUT
1K

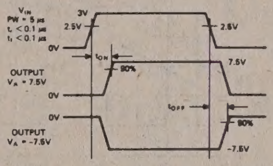
OFF MODEL

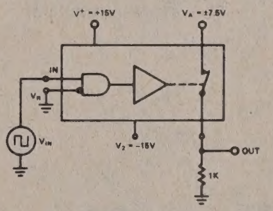

5 pF
1.7 pF
5 pF (DG 140, 141)
1.7 pF (OTHERS)
SOURCE
DRAIN
$I_{S(OFF)}$
0.8 pF
$I_{D(OFF)}$

ON MODEL

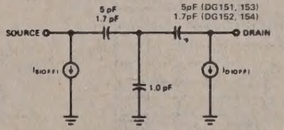

r_{ON}
SOURCE
DRAIN
I_{ON}
0.8 pF

DG151, 152, 153, 154

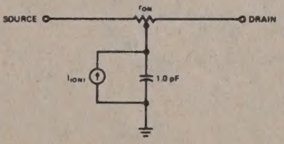



V⁺ = +15V
V_A = ±7.5V
IN
V_R
V_{IN}
V_2 = -15V
OUT
1K

OFF MODEL


5 pF
1.7 pF
5pF (DG151, 153)
1.7pF (DG152, 154)
SOURCE
DRAIN
$I_{S(OFF)}$
1.0 pF
$I_{D(OFF)}$

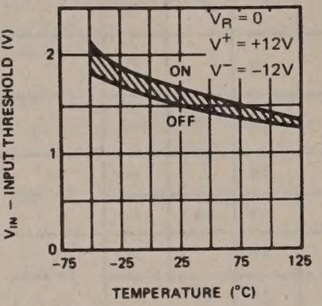
ON MODEL


r_{ON}
SOURCE
DRAIN
I_{ON}
1.0 pF

TYPICAL CHARACTERISTICS (per channel)

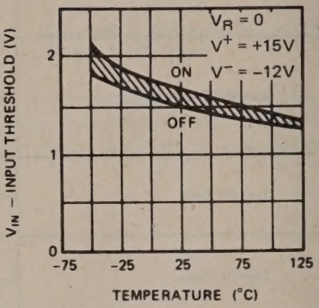
DG126, 129, 133, 134, 140, 141

V_{IN} THRESHOLD vs TEMPERATURE

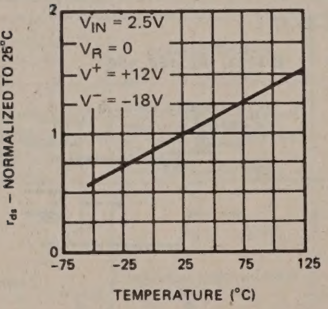


DG151, 152, 153, 154

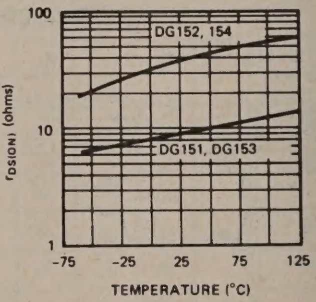
V_{IN} THRESHOLD vs TEMPERATURE



$r_{DS(ON)}$ vs TEMPERATURE (Normalized to 25°C Value)

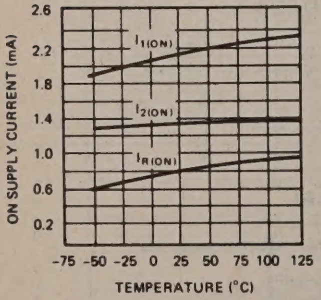


$r_{DS(ON)}$ vs TEMPERATURE

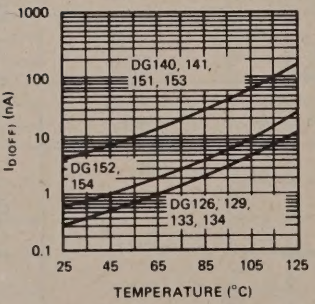


ALL CIRCUITS

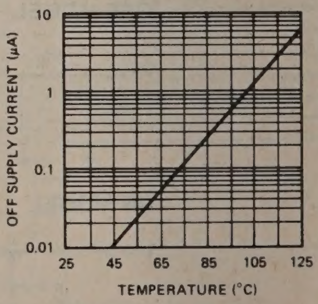
ON SUPPLY CURRENT vs TEMPERATURE



$I_{D(OFF)}$ vs TEMPERATURE



OFF SUPPLY CURRENT vs TEMPERATURE



D129
4-Channel MOS FET Switch Driver with Decode

FEATURES

- Quad Three-Input Gates Decode Binary Counter to Four Lines
- Inputs Compatible with Low Power TTL and DTL, $I_F = 200\mu A$ Max
- Output Current Sinking Capability 10mA
- External Pull-Up Elements Required
- Compatible with G115 and G123 Series Multichannel MOS FET Switches which include Current-Limiter Pull-Up FETs

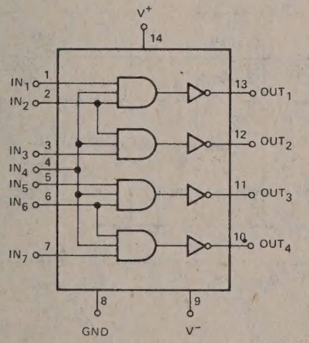
GENERAL DESCRIPTION

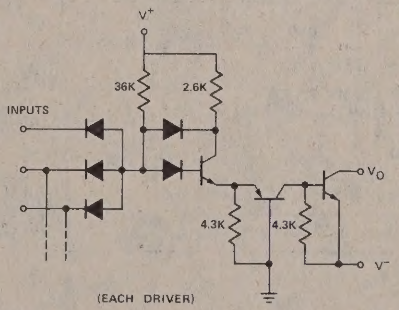
The D129 is a 4-channel driver with binary decode input. It has been designed to provide the DC level-shifting required to interface low-level logic outputs (0.7 to 2.2V) to field-effect transistor inputs (up to 50V peak-to-peak). For a 5V input logic supply, the V⁻ terminal can be set at any voltage between −5V and −30V. The output transistor is capable of sinking 10mA and will stand-off up to 50V above V⁻ in the off-state.

The ON state of the driver is controlled by a logic "1" (open) on all three input logic lines, while the OFF state of the driver is achieved by pulling any one of the three inputs to a logic "0" (ground).

The 4-channel driver is internally connected such that each one can be controlled independently or decoded from a binary counter.

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)





ORDERING INFORMATION

D129 A K

Package
K — 14-pin CERDIP
L — 14-pin Flat Pak
P — 14-pin Ceramic DIP (Special Order Only)

Temperature Range
A — −55°C to +125°C
B — −20°C to +85°C

Device Chip Type

ABSOLUTE MAXIMUM RATINGS

$V_O - V^-$ 50V
GND $- V^-$ 33V
V^+ $-$ GND 8V
V_{IN} $-$ GND . . . . ±6V
Current (any terminal) 30mA
Storage Temperature . . . . −65°C to +150°C
Operating Temperature . . . . −55°C to +125°C
Power Dissipation (note) 750mW
Lead Temperature (Soldering, 10 sec) . . . . 300°C

Note: Dissipation rating assumes device mounted with all leads welded or soldered to pc board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient termperatures.

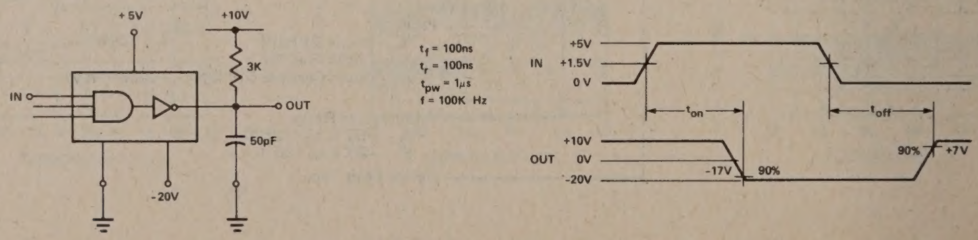
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS Test conditions unless otherwise specified $V^- = -20V$, $V^+ = 5V$

	PARAMETER		CONDITIONS		MAX LIMITS						UNIT
					D129M			D129I			
					-55°C	25°C	125°C	- 20°C	25°C	85°C	
OUT	V_{OL}	Output Voltage, Low	I_O = 10mA	V_{IN} = 2.2V, V^+ = 4.5V	-19.3	-19.3	-19	-19.25	-19.25	-19	V
	V_{OL}	Output Voltage, Low	I_O = 1mA		-19.8	-19.8	-19.75				
	I_{OH}	Output Current, High	V_O= 10V, V_{IN} = 0.7V		0.1	0.1	20	0.2	0.2	10	µA
IN	I_{INH}*	Input Current Input Voltage High	V_{IN}= 5V Input Under Test, V_{IN}= 0 All Other Inputs		0.25	0.25	5	1	1	5	µA
	I_{INL}*	Input Current, Input Voltage Low	V_{IN} = 0, V^+ = 5.5V		-250	-200	-160	-250	-225	-200	
TIME	t_{on}	Turn-ON Time	See Switching Time Test Circuit			0.25			0.3		µs
	t_{off}	Turn-OFF Time				1.0			1.5		
SUPPLY	I_{EE}	Negative Supply Current	$V^- = -20V$ $V^+ = 5.5V$	One Channel "ON"		- 2			- 2.25		mA
	I_L	Logic Supply Current				3			3.3		
	I_{EE}	Negative Supply Current		All V_{IN} = 0, All Channels "OFF"		-10			-25		µA
	I_L	Logic Supply Current				0.75			1		mA

* Per gate Input

SWITCHING TIME AND TEST CIRCUIT



INTERSIL

DG139, DG142 — DG146, DG161 — DG164

Drivers with Differentially Driven N.O. and N.C. FET Switches

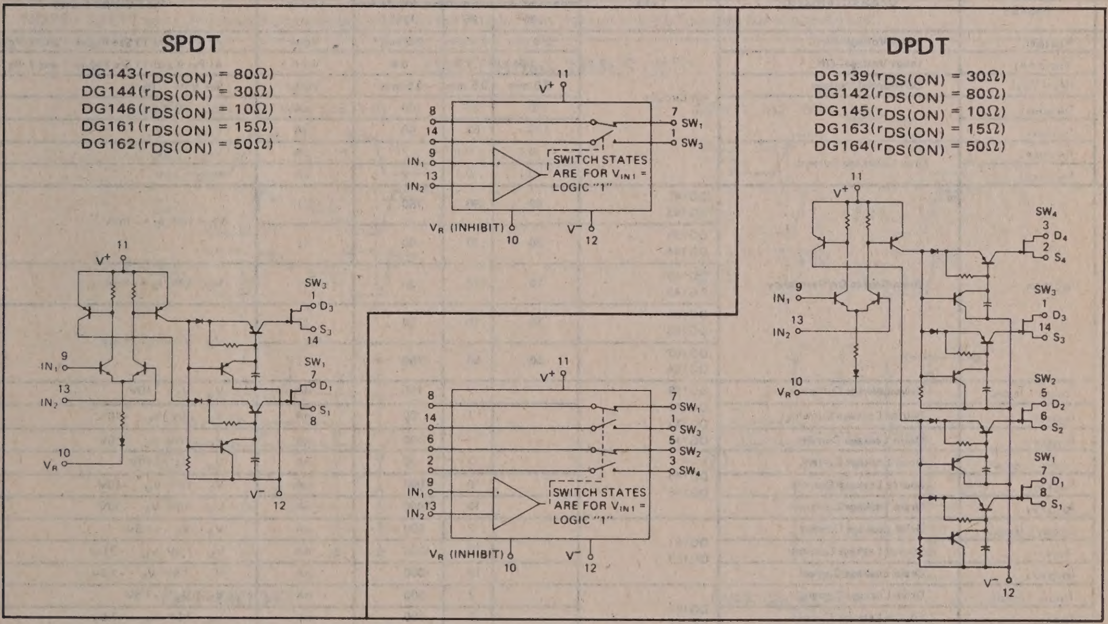
FEATURES

- Each channel complete-interfaces with most integrated logic
- Low OFF power dissipation, 1 mW
- Switches analog signals up to 20 volts peak-to-peak
- Low $r_{DS(ON)}$, 10 ohms max on DG145 and DG146

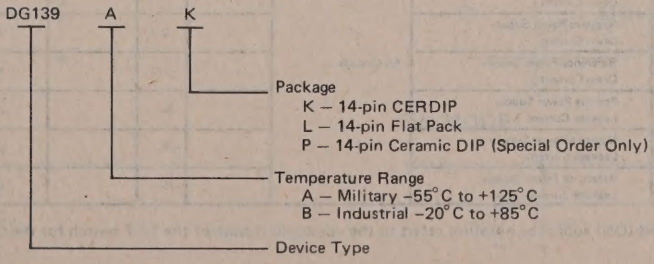
GENERAL DESCRIPTION

Each package contains a monolithic driver with differential input and 2 or 4 discrete FET switches. The driver may be treated as a special purpose differential amplifier which controls the conduction state of the FET switches. The differential output of the driver sets the switches in opposition, one pair open and the other pair closed. All switches may be opened by applying a positive control signal to the V_R terminal.

SCHEMATIC AND LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)


SPDT
DG143($r_{DS(ON)}$ = 80Ω)
DG144($r_{DS(ON)}$ = 30Ω)
DG146($r_{DS(ON)}$ = 10Ω)
DG161($r_{DS(ON)}$ = 15Ω)
DG162($r_{DS(ON)}$ = 50Ω)
DPDT
DG139($r_{DS(ON)}$ = 30Ω)
DG142($r_{DS(ON)}$ = 80Ω)
DG145($r_{DS(ON)}$ = 10Ω)
DG163($r_{DS(ON)}$ = 15Ω)
DG164($r_{DS(ON)}$ = 50Ω)
SWITCH STATES ARE FOR V_{IN1} = LOGIC "1"
V^+
11
V^-
12
V_R (INHIBIT)
10
IN_1
9
IN_2
13
V_R
SW1
SW2
SW3
SW4
8
14
7
1
6
5
2
3
D_1
S_1
D_2
S_2
D_3
S_3
D_4
S_4

ORDERING INFORMATION



Package
K – 14-pin CERDIP
L – 14-pin Flat Pack
P – 14-pin Ceramic DIP (Special Order Only)

Temperature Range
A – Military –55°C to +125°C
B – Industrial –20°C to +85°C

Device Type

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ 36V
$V_S - V^-$ 30V
$V^+ - V_S$ 30V
$V_S - V_D$ . . . . ±22V
$V_R - V^-$ 21V
Power Dissipation (Note) . . . . 750 mW
Current (any terminal) . . . . 30 mA

$V^+ - V_R$ 17V
$V^+ - V_{IN1}$ or V_{IN2} . 14V
$V_{IN1} - V_{IN2}$ . . . . . ±6V
$V_{IN1} - V_R$ . . . . ±6V
$V_{IN2} - V_R$ . . . . ±6V

Storage Temperature . . . . -65 to +150°C
Operating Temperature . . . . -55 to +125°C
Lead Temperature (soldering, 10 sec) . . . . 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Applied voltages for all tests: DG139, DG142, DG143, DG144, DG145, DG146 (V^+ = 12V, V^- = −18V, V_R = 0, V_{IN2} = 2.5V) and DG161, DG162, DG163, DG164 (V^+ = 15V, V^- = −15V, V_R = 0, V_{IN2} = 2.5V). Input test condition that guarantees FET switch ON or OFF as specified is used for output specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT			UNITS	TEST CONDITIONS
				-55°	25°	125°		
INPUT	$V_{IN(ON)}$	Input Voltage—On	All Circuits	2.9 min	2.5 min	2.0 min	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$V_{IN(OFF)}$	Input Voltage—Off		1.4	1.0	0.6	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$\lvert V_9 - V_{13} \rvert$	Differential Voltage		0.5 min	0.5 min	0.5 min	Volts	See Note 1, Pg. 4
	$I_{IN1(ON)}$	Input Current		120	60	60	μA	V_{IN1} 3.0V
	$I_{IN2(ON)}$			120	60	60	μA	V_{IN2} 2.0V
	$I_{IN1(OFF)}$	Input Leakage Current		0.1	0.1	2	μA	V_{IN1} 2.0V
	$I_{IN2(OFF)}$			0.1	0.1	2	μA	V_{IN2} 3.0V
SWITCH OUTPUT	$r_{DS(ON)}$	Drain-Source On Resistance	DG142 DG143	80	80	150	Ω	V_D = 10V, I_S = −1mA
			DG139 DG144	30	30	60	Ω	
			DG145 DG146	10	10	20	Ω	V_D = 10V, I_S = −1mA
			DG161 DG163	15	15	30	Ω	V_D = 7.5V, I_S = 1 mA
			DG162 DG164	50	50	100	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG139 DG142 DG143 DG144		2	100	nA	V_D = V_S = -10V
	$I_{S(OFF)}$	Source Leakage Current			1	100	nA	V_S = 10V, V_D = -10V
	$I_{D(OFF)}$	**Drain Leakage Current**			1	100	nA	V_D = 10V, V_S = -10V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG145 DG146		2	100	nA	V_D = V_S = -10V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S = 10V, V_D = -10V
	$I_{D(OFF)}$	**Drain Leakage Current**			10	1000	nA	V_D = 10V, V_S = -10V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG161 DG163		2	500	nA	V_D = V_S = -7.5V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S = 7.5V, V_D = -7.5V
	$I_{D(OFF)}$	**Drain Leakage Current**			10	1000	nA	V_D = 7.5V, V_S = -7.5V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG162 DG164		2	500	nA	V_D = V_S = -7.5V
	$I_{S(OFF)}$	Source Leakage Current			2	200	nA	V_S = 7.5V, V_D = -7.5V
	$I_{D(OFF)}$	**Drain Leakage Current**			2	200	nA	V_D = 7.5V, V_S = -7.5V
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		4.0		mA	V_{IN1} = 3V or V_{IN1} = 2V
	$I_{2(ON)}$	Negative Power Supply Drain Current			-2.0		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			-2.0		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	V_{IN1} = V_{IN2} = 0.8V
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			-25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			-25		μA	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

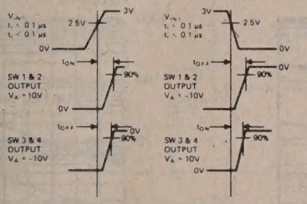
ELECTRICAL CHARACTERISTICS PER CHANNEL (cont.)

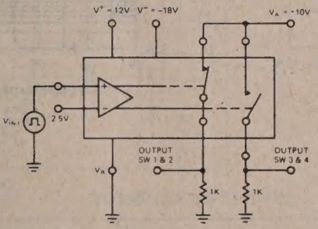
	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT			UNITS	TEST CONDITIONS
				-55°C	25°	125°		
SWITCHING	t_{ON}	Turn-On Time	DG139, DG142 DG143, DG144 DG162, DG164		0.8		μs	See Below
			DG139, DG142 DG143, DG144 DG162, DG164		0.4	0.7	μs	
	t_{OFF}	Turn-Off Time	DG139, DG142 DG143, DG144 DG162, DG164		1.6		μs	See Below
			DG139, DG142 DG143, DG144 DG162, DG164		0.8	1.2	μs	
	t_{ON}	Turn-On Time	DG145, DG146 DG161, DG163		1.0		μs	See Below
			DG145, DG146 DG161, DG163		0.5	0.8	μs	
	t_{OFF}	Turn-Off Time	DG145, DG146 DG161, DG163		2.5		μs	See Below
			DG145, DG146 DG161, DG163		1.25	1.8	μs	
POWER	P_{ON}	ON Driver Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5V
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} - 1.0V

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

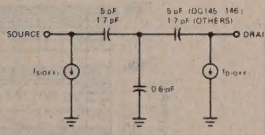
SWITCHING TIMES (25°C)

DG139, 142, 143, 144, 145, 146

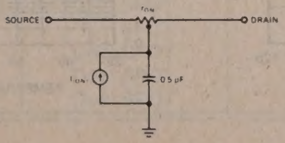



V^+ = 12V V^- = -18V
V_A = -10V
V_{IN}
2.5V
V_R
OUTPUT SW 1 & 2
OUTPUT SW 3 & 4
1K
1K

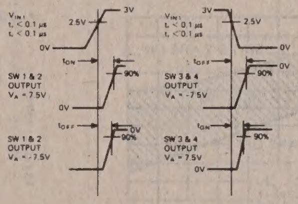
OFF MODEL

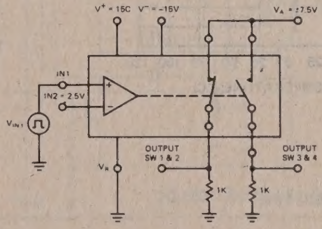

5 pF
1.7 pF
5 pF (DG145, 146)
1.7 pF (OTHERS)
SOURCE
DRAIN
$I_{S(OFF)}$
$I_{D(OFF)}$
0.6 pF

ON MODEL

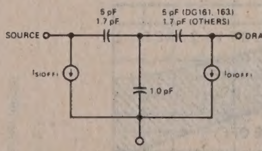

r_{ON}
SOURCE
DRAIN
I_{ON}
0.5 pF

DG161, 162, 163, 164




V^+ = 15C V^- = -15V
V_A = ±7.5V
IN1
IN2 = 2.5V
V_{IN1}
V_R
OUTPUT SW 1 & 2
OUTPUT SW 3 & 4
1K
1K

OFF MODEL


5 pF
1.7 pF
5 pF (DG161, 163)
1.7 pF (OTHERS)
SOURCE
DRAIN
$I_{S(OFF)}$
$I_{D(OFF)}$
1.0 pF

ON MODEL

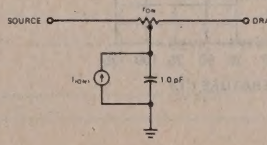

r_{ON}
SOURCE
DRAIN
I_{ON}
1.0 pF

FIGURE 1

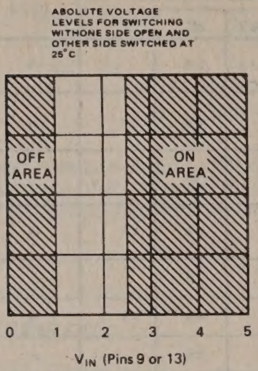
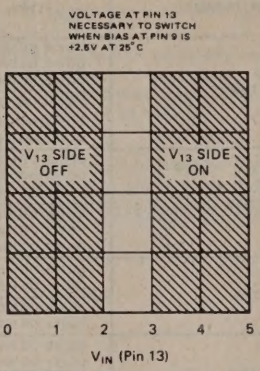

ABOLUTE VOLTAGE LEVELS FOR SWITCHING WITHONE SIDE OPEN AND OTHER SIDE SWITCHED AT 25°C
OFF AREA
ON AREA
0
1
2
3
4
5
V_{IN} (Pins 9 or 13)

FIGURE 2

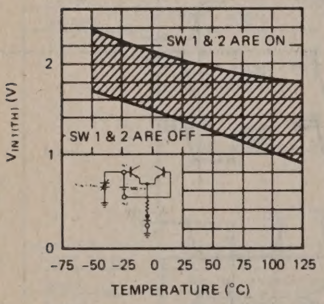

VOLTAGE AT PIN 13 NECESSARY TO SWITCH WHEN BIAS AT PIN 9 IS +2.5V AT 25°C
V_{13} SIDE OFF
V_{13} SIDE ON
0
1
2
3
4
5
V_{IN} (Pin 13)

NOTE1: An example of Absolute Minimum Differential Voltage, $|V_9 - V_{13}|$, is when V_9 = 3V and V_{13} = 2.5V, the V_9 side of the switch is ON and the V_{13} side of the switch is OFF at 25°C. Conversely, when V_9 = 2V and V_{13} = 2.5V, the V_9 side of the switch is OFF and the V_{13} side of the switch is ON at 25°C.

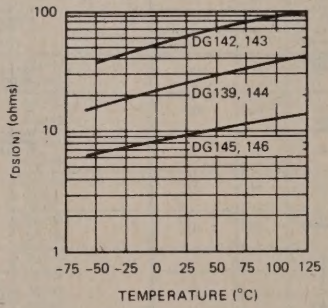
TYPICAL CHARACTERISTICS (per channel)

DG139, 142, 144, 145, 146

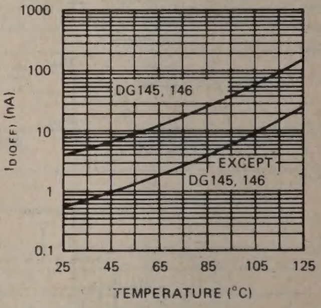
V_{IN1} THRESHOLD vs TEMPERATURE



$r_{DS(ON)}$ vs TEMPERATURE

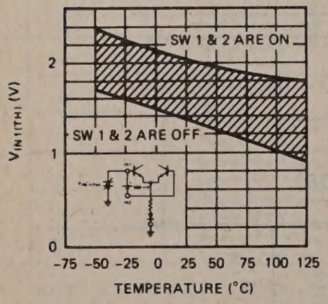


$I_{D(OFF)}$ vs TEMPERATURE

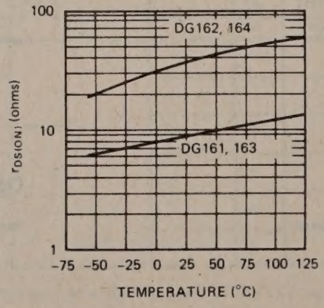


DG161, 162, 163, 164

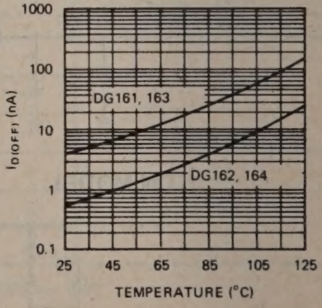
V_{IN1} THRESHOLD vs TEMPERATURE



$R_{DS(ON)}$ vs TEMPERATURE



$I_{S(OFF)}$ vs TEMPERATURE



INTERSIL

DG180-191

High-Speed Driver With Junction FET Switches

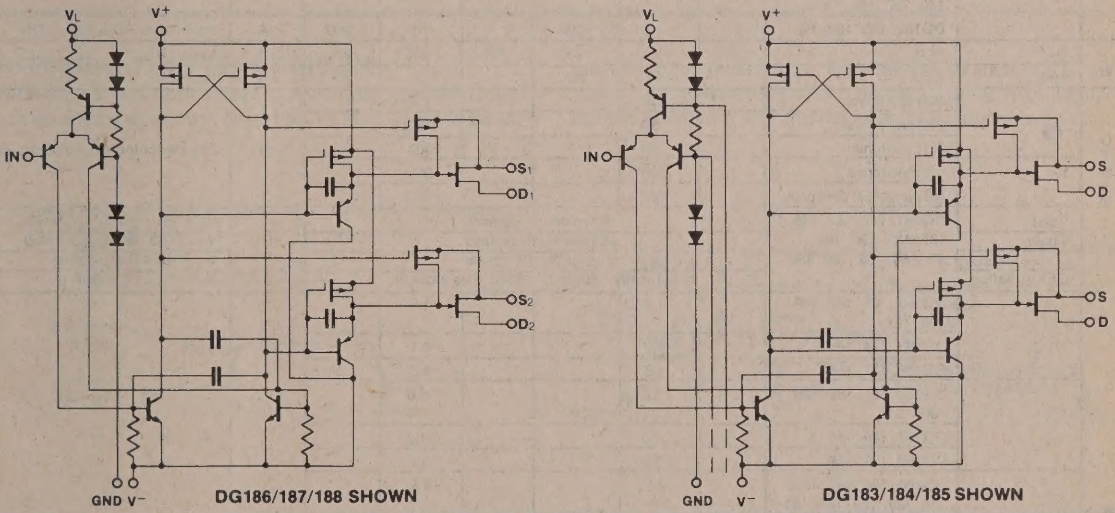
FEATURES

- **Constant ON-resistance for signals to ±10V (DG182, 185, 188, 191), to ±7.5V (all devices)**
- **±15V power supplies**
- **<2nA leakage from signal channel in both ON and OFF states**
- **TTL, DTL, RTL direct drive compatibility**
- **t_{on}, t_{off} <150ns, break-before-make action**
- **Cross-talk and open switch isolation >50dB at 10MHz (75Ω load)**

GENERAL DESCRIPTION

The DG180 thru DG191 series of analog gates consists of 2 or 4 N-channel junction-type field-effect transistors (J-FET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state, each switch conducts current equally well in both directions. In the OFF condition, the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output feedthrough is >50dB down at 10MHz, because of the low output impedance of the FET-gate driving circuit.

SCHEMATIC DIAGRAM (Typical Channel)



ONE AND TWO CHANNEL SPDT AND SPST CIRCUIT CONFIGURATION

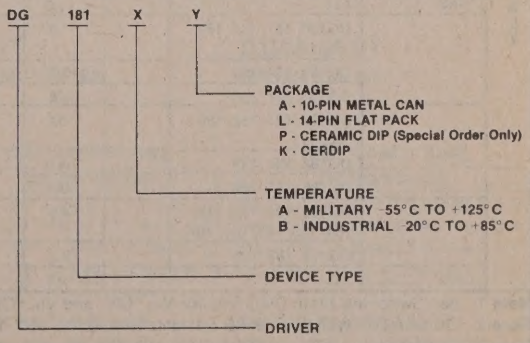
DG186/187/188 SHOWN

TWO CHANNEL DPST CIRCUIT CONFIGURATION

DG183/184/185 SHOWN

ORDERING INFORMATION

PART NUMBER	TYPE	$r_{DS(on)}$ (MAX)
DG180	Dual SPST	10
DG181	Dual SPST	30
DG182	Dual SPST	75
DG183	Dual DPST	10
DG184	Dual DPST	30
DG185	Dual DPST	75
DG186	SPDT	10
DG187	SPDT	30
DG188	SPDT	75
DG189	Dual SPDT	10
DG190	Dual SPDT	30
DG191	Dual SPDT	75



DG 181 X Y

PACKAGE
A - 10-PIN METAL CAN
L - 14-PIN FLAT PACK
P - CERAMIC DIP (Special Order Only)
K - CERDIP

TEMPERATURE
A - MILITARY −55°C TO +125°C
B - INDUSTRIAL −20°C TO +85°C

DEVICE TYPE

DRIVER

MAXIMUM RATINGS

V^+-V^- 36V
V^+-V_D 33V
V_D-V^- 33V
V_D-V_S . . . . ±22V
V_L-V^- 36V
V_L-V_{IN} 8V
V_L-GND 8V
V_{IN}-GND 8V
GND-V^- 27V
GND-V_{IN} 2V
Lead Temperature (Soldering, 10 sec) . . . . 300°C
Current (S or D) See Note 3 . . . . 200mA
Storage Temperature . . . . −65°C to +150°C
Operating Temperature . . . . −55°C to +125°C
Power Dissipation* . . . . 450 (TW), 750 (FLAT), 825 (DIP) mW

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V^- = −15V, V_L = 5V, Unless Noted)

	PARAMETER	DEVICE	A SERIES			B SERIES			UNITS	TEST CONDITIONS (Note 1)
			−55°C	+25°C	+125°C	−20°C	+25°C	+85°C		
SWITCH	$I_{S(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 10V, V_D = −10V, V^+ = 10V V^- = −20V, V_{IN} = "OFF"
		DG181, 184, 187, 190 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 7.5V, V_D = −7.5V V_{IN} = "OFF"
		DG182, 185, 188, 191		1	100		5	100	nA	V_S = 10V, V_D = −10V V_{IN} = "OFF"
	$I_{D(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 10V, V_D = −10V, V^+ = 10V V^- = −20V, V_{IN} = "OFF"
		DG181, 184, 187, 190 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 7.5V, V_D = −7.5V V_{IN} = "OFF"
		DG182, 185, 188, 191		1	100		5	100	nA	V_S = 10V, V_D = −10V V_{IN} = "OFF"
	$I_{D(on)}$ + $I_{S(on)}$	DG180, 181, 183, 184 186, 187, 189, 190		−2	−200		−10	−200	nA	V_D = V_S = −7.5V, V_{IN} = "ON"
		DG182, 185, 188, 191		−2	−200		−10	−200	nA	V_D = V_S = −10V, V_{IN} = "ON"
IN	I_{INL}	ALL	−250	−250	−250	−250	−250	−250	μA	V_{IN} = 0V
	I_{INH}	ALL		10	20		10	20	μA	V_{IN} = 5V
DYNAMIC	t_{on}	10Ω Switches		300			350		ns	See switching time test circuit
		30Ω Switches		150			180			
		75Ω Switches		250			300			
	t_{off}	10Ω Switches		250			300			
		30Ω and 75Ω Switches		130			150			
	$C_{S(off)}$	DG181, 182, 184, 185, 187, 188, 190, 191 (DG180, 183, 186, 189)	9 typical (21 typical)						pF	V_S = −5V, I_D = 0, f = 1MHz
	$C_{D(off)}$		6 typical (17 typical)							V_D = +5V, I_S = 0, f = 1MHz
	$C_{D(on)}$ + $C_{S(on)}$		14 typical (17 typical)							V_D = V_S = 0, f = 1MHz
	OFF Isolation		Typically >50dB at 10MHz (See Note 2)							R_L = 75Ω, C_L = 3pF
SUPPLY	I^+	DG180, 181, 182, 189 190, 191		1.5			1.5		mA	V_{IN} = 5V
		DG183, 184, 185		0.1			0.1			
		DG186, 187, 188		0.8			0.8			
	I^-	DG180, 181, 182, 189, 190, 191		−5.0			−5.0			
		DG183, 184, 185		−4.0			−4.0			
		DG186, 187, 188		−3.0			−3.0			
	I_L	DG180, 181, 182, 183, 184, 185, 189, 190, 191		4.5			4.5			
		DG186, 187, 188		3.2			3.2			
	I_{GND}	ALL		−2.0			−2.0			
	I^+	DG180, 181, 182, 189, 190, 191		1.5			1.5			V_{IN} = 0V
		DG183, 184, 185		3.0			3.0			
		DG186, 187, 188		0.8			0.8			
	I^-	DG180, 181, 182, 189, 190, 191		−5.0			−5.0			
		DG183, 184, 185		−5.5			−5.5			
		DG186, 187, 188		−3.0			−3.0			
	I_L	DG180, 181, 182, 183, 184, 185, 189, 190, 191		4.5			4.5			
		DG186, 187, 188		3.2			3.2			
	I_{GND}	ALL		−2.0			−2.0			

Note 1: See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditions.

Note 2: Off Isolation typically >55dB at 1MHz for DG180, 183, 186, 189.

Note 3: Saturation Drain Current for DG180, 183, 186, 189 only, typically 300mA (2msec Pulse Duration). Maximum Current on all other devices (any terminal) 30mA.

ELECTRICAL CHARACTERISTICS (CONT'D)

MAXIMUM RESISTANCES ($r_{DS(ON)}$ MAX)

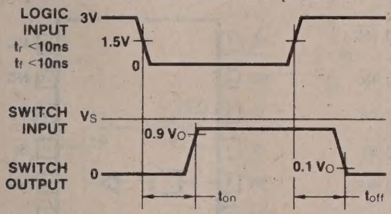
DEVICE NUMBER	MILITARY TEMPERATURE			INDUSTRIAL TEMPERATURE			UNITS	CONDITIONS (Note 1) V+ = 15V, V− = −15V, V_L = 5V	
	−55°C	+25°C	+125°C	−20°C	+25°C	+85°C			
DG180	10	10	20	15	15	25	Ω	V_D = −7.5V	I_S = −10mA V_{IN} = "ON"
DG181	30	30	60	50	50	75	Ω	V_D = −7.5V	
DG182	75	75	100	100	100	150	Ω	V_D = −10V	
DG183	10	10	20	15	15	25	Ω	V_D = −7.5V	
DG184	30	30	60	50	50	75	Ω	V_D = −7.5V	
DG185	75	75	150	100	100	150	Ω	V_D = −10V	
DG186	10	10	20	15	15	25	Ω	V_D = −7.5V	
DG187	30	30	60	50	50	75	Ω	V_D = −7.5V	
DG188	75	75	150	100	100	150	Ω	V_D = −10V	
DG189	10	10	20	15	15	25	Ω	V_D = −7.5V	
DG190	30	30	60	50	50	50	Ω	V_D = −7.5V	
DG191	75	75	150	100	100	150	Ω	V_D = −10V	

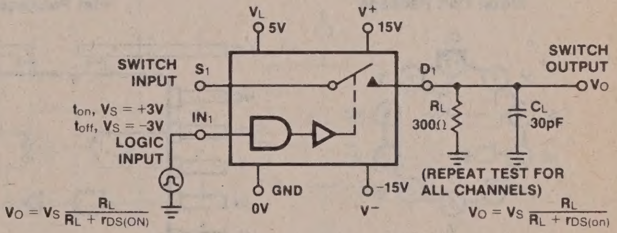
APPLICATION HINT (for design only): Normally the minimum signal handling capability of the DG180 through DG191 family is 20V peak-to-peak for the 75Ω switches and 15V peak-to-peak for the 10Ω and 30Ω switches (refer I_D and I_S tests above). For other Analog Signals, the following guidelines can be used: proper switch turn-off requires that $V^- \le V_{ANALOG}(\text{peak}) - V_p$ where $V_p = 7.5V$ for the 10Ω and 30Ω switches and $V_p = 5.0V$ for 75Ω switches e.g., −10V minimum (−peak) analog signal and a 75Ω switch ($V_p = 5V$), requires that $V^- \le -10V - 5V = -15V$.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

LOGIC INPUT FOR "OFF" TO "ON" CONDITION (DG180/181/182 SHOWN)


LOGIC INPUT
t_r <10ns
t_f <10ns
3V
1.5V
0
SWITCH INPUT
V_S
SWITCH OUTPUT
0
0.9 V_O
0.1 V_O
t_{on}
t_{off}


V_L
5V
V+
15V
SWITCH INPUT
S_1
D_1
SWITCH OUTPUT
V_O
t_{on}, V_S = +3V
t_{off}, V_S = −3V
IN_1
LOGIC INPUT
R_L
300Ω
C_L
30pF
GND
0V
−15V
V−
(REPEAT TEST FOR ALL CHANNELS)
$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$
$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$

DUAL SPST
DG180/181/182

TEST CONDITIONS

DG180/181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.0V	All Channels

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

DUAL DPST
DG183/184/185

TEST CONDITIONS

DG183/184/185	
V_{IN} "ON" = 2.0V	All Channels
V_{IN} "OFF' = 0.8V	All Channels

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

SPDT
DG186/187/188

TEST CONDITIONS

DG186/187/188	
V_{IN} "ON" = 2.0V	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.0V	Channel 2
V_{IN} "OFF" = 0.8V	Channel 1

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

DUAL SPDT
DG189/190/191

TEST CONDITIONS

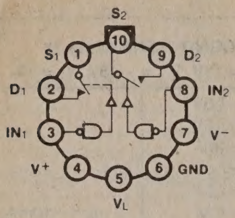
DG189/190/191	
V_{IN} "ON" = 2.0V	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.0V	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

PIN CONFIGURATIONS AND SWITCHING STATE DIAGRAM (See previous page for logic input)

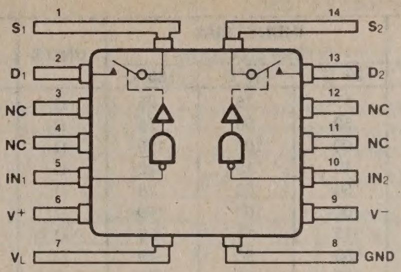
DUAL SPST (DG180, 181, 182)

Metal Can Package


S2
10
1
S1
9
D2
2
D1
8
IN2
3
IN1
7
V−
4
V+
6
GND
5
VL

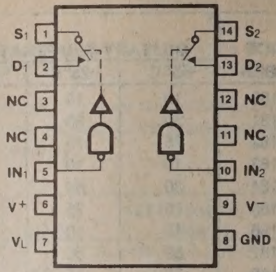
(OUTLINE DWG TO-100)

Flat Package


S1 1
D1 2
NC 3
NC 4
IN1 5
V+ 6
VL 7
14 S2
13 D2
12 NC
11 NC
10 IN2
9 V−
8 GND

(OUTLINE DWG FD-2)

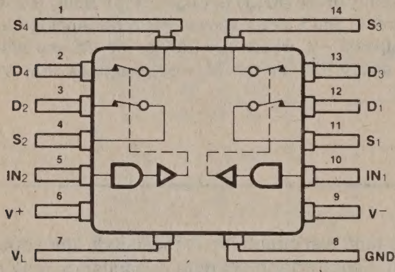
CERDIP*


S1 1
D1 2
NC 3
NC 4
IN1 5
V+ 6
VL 7
14 S2
13 D2
12 NC
11 NC
10 IN2
9 V−
8 GND

(OUTLINE DWG JD)

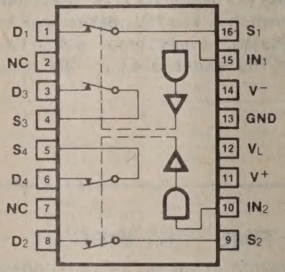
DUAL DPST (DG183, 184, 185)

Flat Package


S4 1
D4 2
D2 3
S2 4
IN2 5
V+ 6
VL 7
14 S3
13 D3
12 D1
11 S1
10 IN1
9 V−
8 GND

(OUTLINE DWG FD-2)

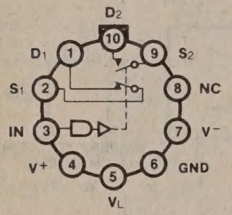
CERDIP*


D1 1
NC 2
D3 3
S3 4
S4 5
D4 6
NC 7
D2 8
16 S1
15 IN1
14 V−
13 GND
12 VL
11 V+
10 IN2
9 S2

(OUTLINE DWG JE)

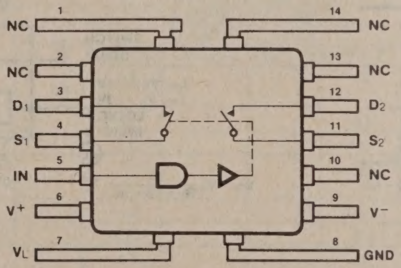
SPDT (DG186, 187, 188)

Metal Can Package


D2
10
1
D1
9
S2
2
S1
8
NC
3
IN
7
V−
4
V+
6
GND
5
VL

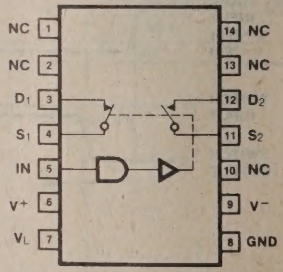
(OUTLINE DWG TO-100)

Flat Package


NC 1
NC 2
D1 3
S1 4
IN 5
V+ 6
VL 7
14 NC
13 NC
12 D2
11 S2
10 NC
9 V−
8 GND

(OUTLINE DWG FD-2)

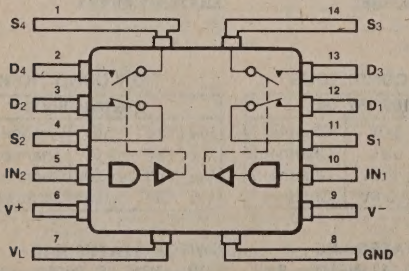
CERDIP*


NC 1
NC 2
D1 3
S1 4
IN 5
V+ 6
VL 7
14 NC
13 NC
12 D2
11 S2
10 NC
9 V−
8 GND

(OUTLINE DWG JD)

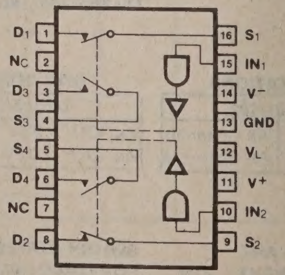
DUAL SPDT (DG189, 190, 191)

Flat Package


S4 1
D4 2
D2 3
S2 4
IN2 5
V+ 6
VL 7
14 S3
13 D3
12 D1
11 S1
10 IN1
9 V−
8 GND

(OUTLINE DWG FD-2)

CERDIP*


D1 1
Nc 2
D3 3
S3 4
S4 5
D4 6
NC 7
D2 8
16 S1
15 IN1
14 V−
13 GND
12 VL
11 V+
10 IN2
9 S2

(OUTLINE DWG JE)

*Side braize ceramic package available as special order only. Consult factory.

INTERSIL

DGM181-191
High-Speed CMOS Analog Switches

FEATURES

- Pin and Function Replacement for DG181 Family
- Meets or exceeds all DG181 family specifications with monolithic reliability
- Low power consumption
- 1nA leakage from signal channel in both ON and OFF states
- TTL, DTL, RTL direct drive capability
- t_{on}, t_{off} <150ns, break-before-make action
- Crosstalk and open load switch isolation >50dB at 10MHz (75Ω load)

GENERAL DESCRIPTION

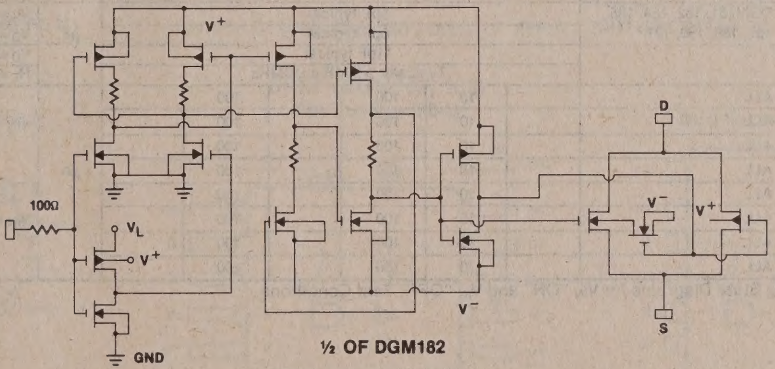
The DGM181 family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to combine the speed of the hybrid DG181 family with the reliability and low power consumption of a monolithic CMOS construction. These devices, therefore, are an ideal replacement for the DG181 family.

The DGM181 family has a high state threshold of 2.4V; devices which have a threshold of 2.0V (the DG181 specification) can be selected and are available as the DGMS series — see ordering information.

Both series meet or exceed all other specifications of the DG181 family.

No quiescent power is dissipated in either the ON or OFF state of the switch. Maximum power supply current is 10μA from any supply, and typical quiescent currents are in the 10nA range. OFF leakages are guaranteed to be less than 200pA at 25°C.

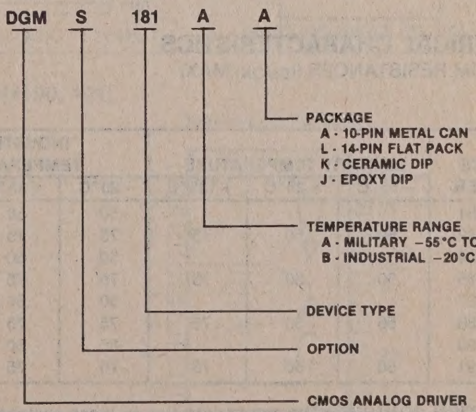
SCHEMATIC DIAGRAM (Typical Channel)


V+
100Ω
VL
V+
GND
V−
V−
V+
D
S

½ OF DGM182

ORDERING INFORMATION

TYPE	STANDARD PART NUMBER	SELECTED PART NUMBER	$r_{DS(on)}$ MAX AT 25°C
Dual SPST	DGM181BX	DGMS181BX	50
	DGM182AX	DGMS182AX	50
	DGM182BX	DGMS182BX	75
Dual DPST	DGM184BX	DGMS184BX	50
	DGM185AX	DGMS185AX	50
	DGM185BX	DGMS185BX	75
SPDT	DGM187BX	DGMS187BX	50
	DGM188AX	DGMS188AX	50
	DGM188BX	DGMS188BX	75
Dual SPDT	DGM190BX	DGMS190BX	50
	DGM191AX	DGMS191AX	50
	DGM191BX	DGMS191BX	75


DGM
S
181
A
A
PACKAGE
A - 10-PIN METAL CAN
L - 14-PIN FLAT PACK
K - CERAMIC DIP
J - EPOXY DIP
TEMPERATURE RANGE
A - MILITARY −55°C TO +125°C
B - INDUSTRIAL −20°C TO +85°C
DEVICE TYPE
OPTION
CMOS ANALOG DRIVER

MAXIMUM RATINGS

V^+-V^- 36V
V^+-V_D 33V
V_D-V^- 33V
V_D-V_S .... ±22V
V_L-V^- 36V
V_L-V_{IN} 30V
V_L-V_{GND} 20V
$V_{IN}-V_{GND}$ 20V
GND-V^- 27V
GND-V_{IN} 20V
Current (Any Terminal) 30mA
Storage Temperature .... −65°C to +150°C
Operating Temperature .... −55°C to +125°C
Power Dissipation* .... 450 (TW), 750 (FLAT), 825 (DIP) mW

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $V_L = 5V$, unless noted)

	PARAMETER	DEVICE	A SERIES −55°C	A SERIES +25°C	A SERIES +125°C	B SERIES −20°C	B SERIES +25°C	B SERIES +85°C	UNITS	TEST CONDITIONS (Note 1)
SWITCH	$I_{S(off)}$	DGM181, 184, 187, 190					2.0	100	nA	$V_S = 7.5V$, $V_D = -7.5V$ V_{IN} = "OFF"
		DGM182, 185, 188, 191		0.2	50		0.5	50	nA	$V_S = 10V$, $V_D = -10V$ V_{IN} = "OFF"
	$I_{D(off)}$	DGM181, 184, 187, 190					2.0	100	nA	$V_S = 7.5V$, $V_D = -7.5V$ V_{IN} = "OFF"
		DGM182, 185, 188, 191		0.2	50		0.5	50	nA	$V_S = 10V$, $V_D = -10V$ V_{IN} = "OFF"
	$I_{D(on)} + I_{S(on)}$	DGM181, 184, 187, 190					5.0	100	nA	$V_D = V_S = -7.5V$, V_{IN} = "ON"
		DGM182, 185, 188, 191		0.5	50		2.0	50	nA	$V_D = V_S = -10V$, V_{IN} = "ON"
IN	I_{INL}	ALL		1.0	20		10	20	µA	$V_{IN} = 0V$
	I_{INH}	ALL		1.0	20		10	20	µA	$V_{IN} = 5V$
DYNAMIC	t_{on}	DGM181, 184, 187, 190					180		ns	See switching time test circuit
		DGM182, 185, 188, 191		250			300			
	t_{off}	ALL		130			150			
	$C_{S(off)}$	DGM181, 182, 184, 185, 187, 188, 190, 191	5pF typical						pF	$V_S = -5V$, $I_D = 0$, f = 1MHz
	$C_{D(off)}$		6pF typical							$V_D = +5V$, $I_S = 0$, f = 1MHz
	$C_{D(on)} + C_{S(on)}$		11pF typical							$V_D = V_S = 0$, f = 1MHz
	OFF Isolation		Typically >50dB at 10MHz							$R_L = 75\Omega$, $C_L = 3pF$
SUPPLY	I^+	ALL		10	100		100		µA	$V_{IN} = 5V$
	I^-	ALL		10	100		100			
	I_L	ALL		10	100		100			
	I_{GND}	ALL		10	100		100			
	I^+	ALL		10	100		100			$V_{IN} = 0V$
	I^-	ALL		10	100		100			
	I_L	ALL		10	100		100			
	I_{GND}	ALL		10	100		100			

NOTE 1: See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditions.

ELECTRICAL CHARACTERISTICS

MAXIMUM RESISTANCES ($r_{DS(ON)}$ MAX)

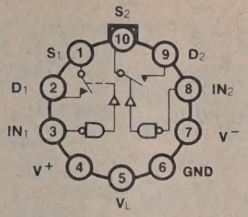
DEVICE NUMBER	MILITARY TEMPERATURE −55°C	MILITARY TEMPERATURE +25°C	MILITARY TEMPERATURE +125°C	INDUSTRIAL TEMPERATURE −20°C	INDUSTRIAL TEMPERATURE +25°C	INDUSTRIAL TEMPERATURE +85°C	UNITS	CONDITIONS (Note 1) $V^+ = 15V$, $V^- = -15V$, $V_L = 5V$	
DGM181				50	50	75	Ω	$V_D = -7.5V$	$I_S = -10mA$ V_{IN} = "ON"
DGM182	50	50	75	75	75	100	Ω	$V_D = -10V$	
DGM184				50	50	75	Ω	$V_D = -7.5V$	
DGM185	50	50	75	75	75	100	Ω	$V_D = -10V$	
DGM187				50	50	75	Ω	$V_D = -7.5V$	
DGM188	50	50	75	75	75	100	Ω	$V_D = -10V$	
DGM190				50	50	75	Ω	$V_D = -7.5V$	
DGM191	50	50	75	75	75	100	Ω	$V_D = -10V$	

APPLICATION COMMENT: The charge injection in these switches is of opposite polarity to that of the standard DG180 family, but considerably smaller.

PIN CONFIGURATIONS & SWITCHING STATE DIAGRAM

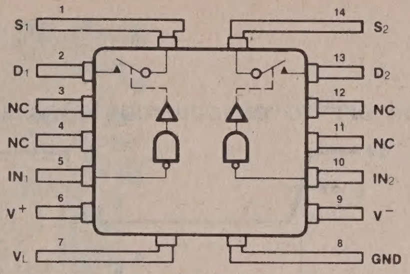
DUAL SPST (DGM181, 182)

Metal Can Package


S2
10
S1 1
9 D2
D1 2
8 IN2
IN1 3
7 V−
V+ 4
6 GND
5
VL

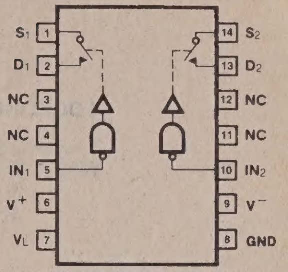
(OUTLINE DWG TO-100)

Flat Package (FD-2)


S1 1
14 S2
D1 2
13 D2
NC 3
12 NC
NC 4
11 NC
IN1 5
10 IN2
V+ 6
9 V−
VL 7
8 GND

SWITCH STATES ARE FOR LOGIC "1" INPUT

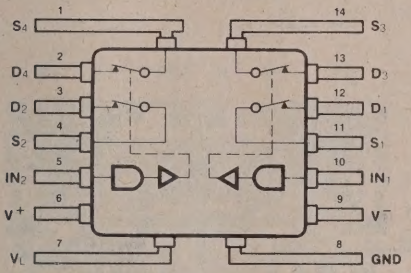
Dual-In-Line Package


S1 1
D1 2
NC 3
NC 4
IN1 5
V+ 6
VL 7
14 S2
13 D2
12 NC
11 NC
10 IN2
9 V−
8 GND

(OUTLINE DWGS DD, PD)

DUAL DPST (DGM184, 185)

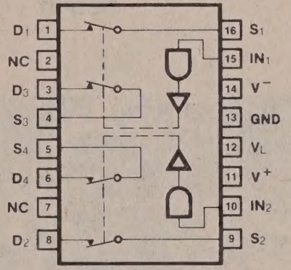
Flat Package


S4 1
14 S3
D4 2
13 D3
D2 3
12 D1
S2 4
11 S1
IN2 5
10 IN1
V+ 6
9 V−
VL 7
8 GND

(OUTLINE DWG FD-2)

SWITCH STATES ARE FOR LOGIC "1" INPUT

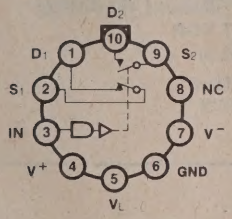
Dual-In-Line Package


D1 1
NC 2
D3 3
S3 4
S4 5
D4 6
NC 7
D2 8
16 S1
15 IN1
14 V−
13 GND
12 VL
11 V+
10 IN2
9 S2

(OUTLINE DWGS DE, PE)

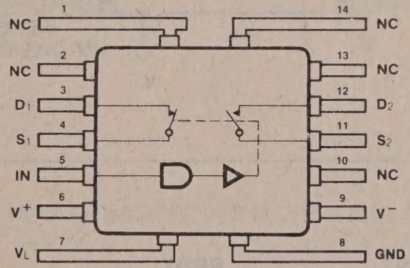
SPDT (DGM187, 188)

Metal Can Package


D2
10
D1 1
9 S2
S1 2
8 NC
IN 3
7 V−
V+ 4
6 GND
5
VL

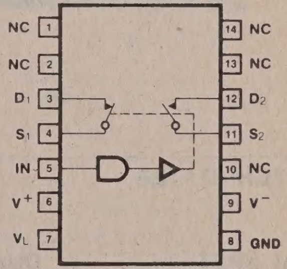
(OUTLINE DWG TO-100)

Flat Package (FD-2)


NC 1
14 NC
NC 2
13 NC
D1 3
12 D2
S1 4
11 S2
IN 5
10 NC
V+ 6
9 V−
VL 7
8 GND

SWITCH STATES ARE FOR LOGIC "1" INPUT

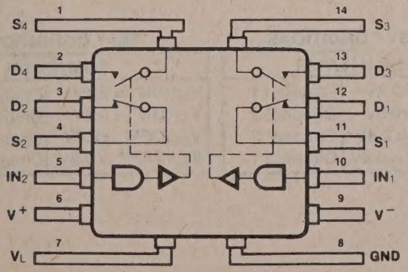
Dual-In-Line Package


NC 1
NC 2
D1 3
S1 4
IN 5
V+ 6
VL 7
14 NC
13 NC
12 D2
11 S2
10 NC
9 V−
8 GND

(OUTLINE DWGS DD, PD)

DUAL SPDT (DGM190, 191)

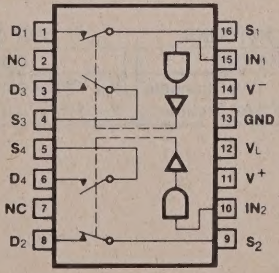
Flat Package


S4 1
14 S3
D4 2
13 D3
D2 3
12 D1
S2 4
11 S1
IN2 5
10 IN1
V+ 6
9 V−
VL 7
8 GND

(OUTLINE DWG FD-2)

SWITCH STATES ARE FOR LOGIC "1" INPUT

Dual-In-Line Package

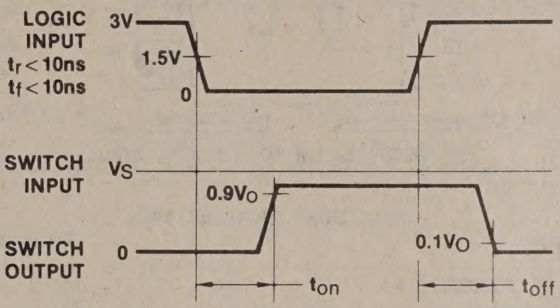

D1 1
NC 2
D3 3
S3 4
S4 5
D4 6
NC 7
D2 8
16 S1
15 IN1
14 V−
13 GND
12 VL
11 V+
10 IN2
9 S2

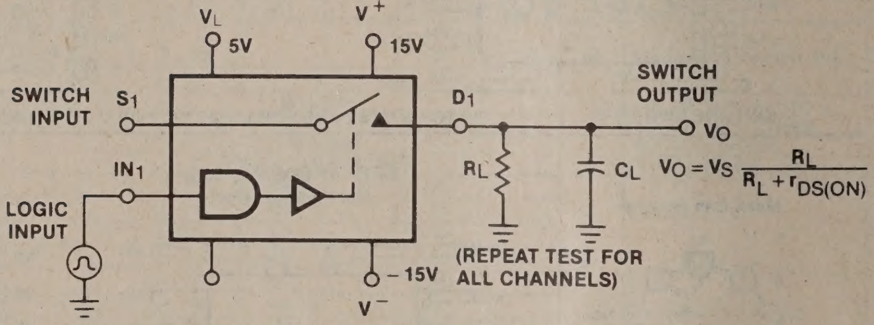
(OUTLINE DWGS DE, PE)

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

LOGIC INPUT FOR "OFF" TO "ON" CONDITION (DG180/181/182 SHOWN)


LOGIC INPUT
$t_r < 10ns$
$t_f < 10ns$
3V
1.5V
0
SWITCH INPUT
V_S
$0.9V_O$
SWITCH OUTPUT
0
$0.1V_O$
t_{on}
t_{off}


V_L
5V
V^+
15V
SWITCH INPUT
S_1
IN_1
LOGIC INPUT
D_1
SWITCH OUTPUT
V_O
R_L
C_L
$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$
– 15V
V^-
(REPEAT TEST FOR ALL CHANNELS)

SWITCH STATES

DUAL SPST
DGM181/182

DUAL DPST
DGM184/185

SPDT
DGM187/188

DUAL SPDT
DGM190/191

TEST CONDITIONS

DGM181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.4V†	All Channels

TEST CONDITIONS

DGM184/185	
V_{IN} "ON" = 2.4V†	All Channels
V_{IN} "OFF" = 0.8V	All Channels

TEST CONDITIONS

DGM187/188	
V_{IN} "ON" = 2.4V†	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.4V†	Channel 2
V_{IN} "OFF" = 0.8V	Channel 1

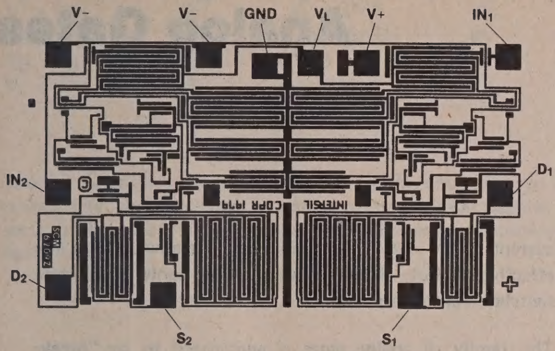
TEST CONDITIONS

DGM190/191	
V_{IN} "ON" = 2.4V†	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.4V†	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

† FOR SELECTED DEVICES, LOGIC "1" INPUT = 2.0V

DGM181-191

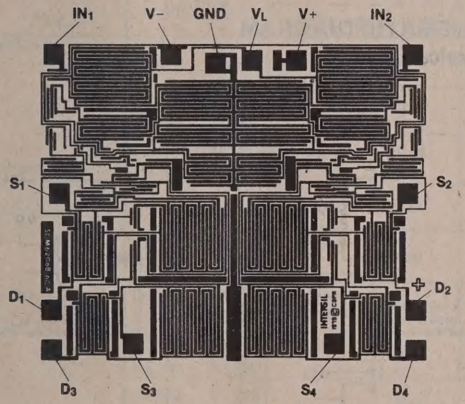
CHIP TOPOGRAPHIES


V–
V–
GND
V_L
V+
IN_1
IN_2
D_1
D_2
S_2
S_1
COPR 1979
INTERSIL

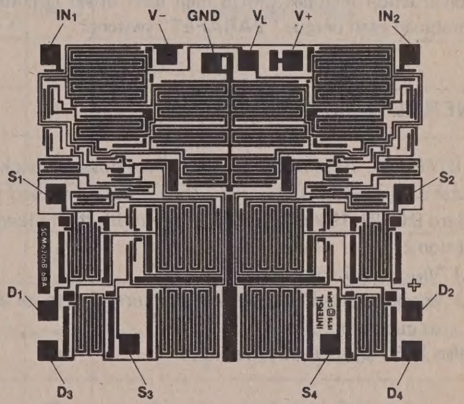
DGM181/182
91x53

CONSULT
FACTORY

DGM188


IN_1
V–
GND
V_L
V+
IN_2
S_1
S_2
D_1
D_2
D_3
S_3
S_4
D_4
INTERSIL

DGM185
91x76


IN_1
V–
GND
V_L
V+
IN_2
S_1
S_2
D_1
D_2
D_3
S_3
S_4
D_4
INTERSIL

DGM191
91x76

NOTE: BACKSIDE OF CHIP IS COMMON TO V+.

IH181 Series Low-Power, High Level Analog Gates

FEATURES

- Switches 20 Vpp Signals
- Quiescent Current Less than 100 μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching t_{off} 130ns Max, t_{on} 250ns Max.
- T^2L, HTL, CMOS, PMOS Compatible
- Low r_{DS} (ON) – 30Ω
- Construction includes CMOS high level driver circuitry combined with unique "VARAFET" switches.

GENERAL DESCRIPTION

The INTERSIL IH181/191 series is a low power version of the standard DG181/191 series. They meet or exceed the standard DG181/191 series specifications with the following exceptions:

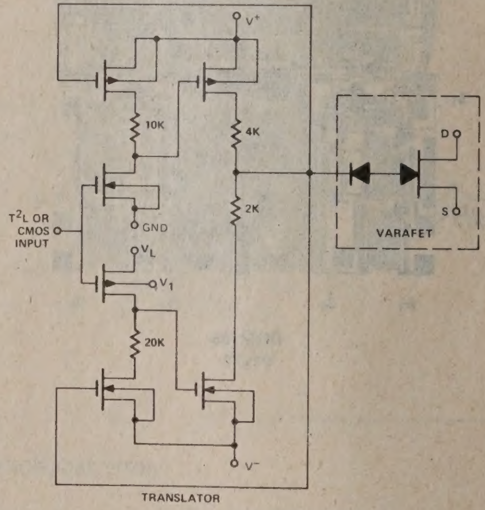
1.) V_{INH} = 2.4 volts minimum.
2.) Break-before-make switching requires t_{on} to be 250 ns maximum.

See also IH5040, IH5140 series.

The actual switching element is a unique new Intersil design, called the Varafet. The Varafet is a monolithic combination of a varactor J-Fet diode driving a conventional J-Fet. Strobing the solid state switch is accomplished by the TTL levels of a "1" being 2.4V or greater; a "0" is 0.8V or lower. The translator input circuitry will draw virtually no source or sinking current (typical pa of input current) from the TTL logic output element; thus the effective fanout, if one were to drive only solid state switches, approaches millions.

The family of analog gates is guaranteed to be "break-before-make" switching; The "off" time is faster than the "on" time. Typical turn-off times are 80 ns and typical turn-on times are 200 ns.

SCHEMATIC DIAGRAM
(Typical Channel)



MAXIMUM ON RESISTANCES – $r_{DS(ON)}$ MAX
(V^+ = 15V, V^- = −15V, V_L = 5V, I_S = 10mA, V_{INL} = 0.8V, V_{INH} = 2.4V)

	DEVICE NUMBER	MILITARY TEMPERATURE			INDUSTRIAL TEMPERATURE			UNITS	CONDITIONS
		-55°C	25°C	125°C	-20°C	25°C	85°C		
Dual SPST	IH 181	30	30	60	50	50	75	Ω	V_D = −7.5V
	IH 182	75	75	100	100	100	150	Ω	V_D = −10V
Dual DPST	IH 184	30	30	60	50	50	75	Ω	V_D = −7.5V
	IH 185	75	75	150	100	100	150	Ω	V_D = −10V
SPDT	IH 187	30	30	60	50	50	75	Ω	V_D = −7.5V
	IH 188	75	75	150	100	100	150	Ω	V_D = −10V
Dual SPDT	IH 190	30	30	60	50	50	75	Ω	V_D = −7.5V
	IH 191	75	75	150	100	100	150	Ω	V_D = −10V

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$	36V	$V_L - V_{IN}$	8V
$V^+ - V_D$	33V	$V_L - GND$	8V
$V_D - V^-$	33V	$V_{IN} - GND$	8V
$V_D - V_S$	±22V	$GND - V^-$	36V
$V_L - V^-$	36V	$V_R - V_{IN}$	2V

Current (Any Terminal)	30 mA
Storage Temperature	−65°C to 150°C
Operating Temperature	−55°C to 125°C
Power Dissipation*	450 mW

*Device mounted with all leads welded or soldered to PC board. Derate 6 mW/°C above 75°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – IH181 THROUGH IH191

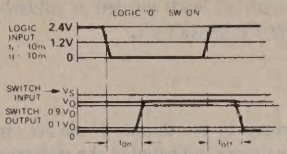
($V^+ = 15$ V, $V^- = -15$ V, $V_L = 5$ V, Unless Noted)

PARAMETER Note (1)	DEVICE	MAX LIMITS (Note 1)						UNITS	TEST CONDITIONS
		−55°C	+25°C	+125°C	−20°C	+25°C	+85°C		
SWITCH $I_{S(OFF)}$	ALL		1	100		5	100	nA	$V_S = 10V$, $V_D = -10V$, $V^+ = 10V$ $V^- = -20V$, $V_{IN} = 2.4V$
	IH 181 IH 184 IH 187 IH 190		1	100		5	100	nA	$V_S = 7.5V$, $V_D = -7.5V$ $V_{IN} = 2.4V$
	IH 182 IH 185 IH 188 IH 191		1	100		5	100	nA	$V_S = 10V$, $V_D = -10V$ $V_{IN} = 2.4V$
$I_{D(OFF)}$	ALL		1	100		5	100	nA	$V_S = 10V$, $V_D = -10V$, $V^+ = 10V$ $V^- = -20V$, $V_{IN} = 2.4V$
	IH 181 IH 184 IH 187 IH 190		1	100		5	100	nA	$V_S = 7.5V$ $V_D = -7.5V$ $V_{IN} = 2.4V$
	IH 182 IH 185 IH 188 IH 191		1	100		5	100	nA	$V_S = 10V$ $V_D = -10V$ $V_{IN} = 2.4V$
$I_{D(ON)} + I_{S(ON)}$	IH 181 IH 184 IH 187 IH 190		-2	-200		-10	-200	nA	$V_D = V_S = -7.5V$ $V_{IN} = 0.8V$
	IH 182 IH 185 IH 188 IH 191		-2	-200		-10	-200	nA	$V_D = V_S = -10V$ $V_{IN} = 0.8V$
IN I_{INL}	ALL	1	1	1	1	1	1	μA	$V_{IN} = 0V$
I_{INH}	ALL	1	1	1	1	1	1	μA	$V_{IN} = 5V$
DYNAMIC t_{on}	ALL		250			300		ns	See switching time test circuit
t_{off}	ALL		130			150		ns	
$C_{S(off)}$	ALL	9 typical						pf	$V_S = -5V$, $I_D = 0$, f = 1MHZ
$C_{D(off)}$		6 typical						pf	$V_S = -5V$, $I_D = 0$, f = 1MHZ
$C_{D(on)} + C_{S(on)}$		14 typical						pf	$V_D = V_S = 0$ f = 1MHZ
Off Isolation		Typ > 50 dB at 10 MHZ						pf	$R_L = 100\Omega$, $C_L = 3pf$
I^+	ALL	100	10	100		100		μA	Both $V_{IN} = 0V$
I^-		100	10	100		100		μA	
I_L			10			100		μA	
GROUND			10			100		μA	
I^+		100	10	100		100		μA	Both $V_{IN} = 5$ V
I^-		100	10	100		100		μA	
I_L			10			100		μA	
GROUND			10			100		μA	

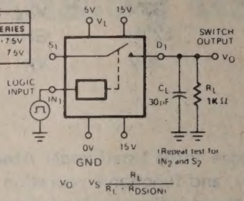
APPLICATION HINT (for design only): The minimum signal handling capability of the IH181 through IH191 family is 20V peak to peak for the 75Ω switches and 15V peak to peak for the 30Ω switches (refer I_D and I_S tests above. Proper switch turn off requires that $V^- \leqslant V_{ANALOG}$ (−peak) − V_P where $V_P \leqslant 7.5V$ for 30Ω switches and $V_P \leqslant 5.0V$ for 75Ω switches i.e., A −10V minimum (−peak) analog signal and a 75Ω switch ($V_P \leqslant 5V$), requires that $V^- \leqslant -10V - 5V = -15V$.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.


LOGIC "0" SW ON
LOGIC INPUT
t_r < 10ns
t_f < 10ns
2.4V
1.2V
0
SWITCH INPUT → V_S
V_O
SWITCH OUTPUT
0.9 V_O
0.1 V_O
0
t_{on}
t_{off}

	SWITCH INPUT	
	75Ω SERIES	30Ω SERIES
t_{on}	V_S +10V	V_S +7.5V
t_{off}	V_S 10V	V_S 7.5V


5V
15V
V_L
S_1
D_1
SWITCH OUTPUT
V_O
LOGIC INPUT
IN_1
C_L 30pF
R_L 1KΩ
0V
GND
15V
(Repeat test for IN_2 and S_2)
$V_O = V_S \frac{R_L}{R_L + R_{DS(ON)}}$

LOGIC COMPATIBILITY

The IH 181/191 family can be used with almost any logic family. It has been designed to directly interface with the popular TTL, HTL, and CMOS families. The fact that the solid state switch input current approaches zero (specification has 1 μA maximum for either high or low input states) means that one is operating along the zero load current, or zero source current line for the TTL output voltage vs. I_{load} or I_{source} current. Thus the maximum output is obtained from the TTL gate. Figures 1 and 2 show the expected (typical) output of a TTL gate vs. load and source currents and plotted as a function of temperature and power supply.

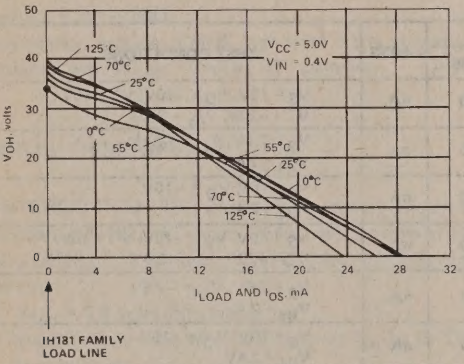


FIGURE 1. CIRCUIT ANALYSIS AND CHARACTERISTICS OF SERIES 54/74

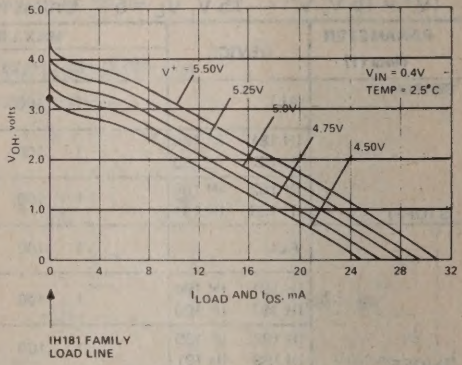


FIGURE 2.

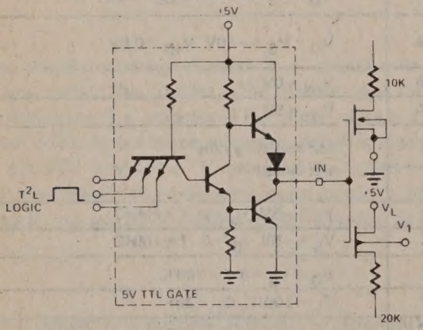

+5V
10K
T^2L LOGIC
IN
+5V
V_L
V_1
+15V OR V^+
20K
5V TTL GATE

FIGURE 3. FOR INTERFACING WITH TTL LOGIC

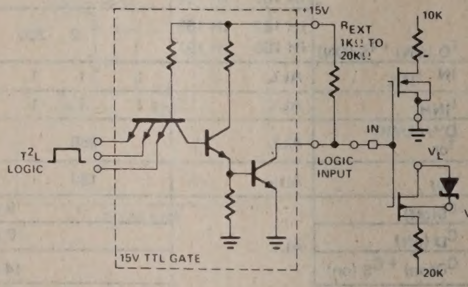

+15V
R_{EXT}
1KΩ TO 20KΩ
10K
T^2L LOGIC
IN
LOGIC INPUT
V_L
V^+
15V TTL GATE
20K

FIGURE 4. FOR INTERFACING WITH HTL OPEN COLLECTOR LOGIC

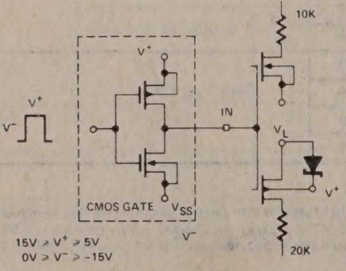

10K
V^+
V^+
V^-
IN
V_L
V^+
CMOS GATE
V_{SS}
V^-
20K
15V ≥ V^+ ≥ 5V
0V ≥ V^- ≥ −15V

FIGURE 5. FOR USE WITH CMOS LOGIC

Note:

When using HTL or CMOS logic, you will note that a Zener diode has been added between the V_L supply (normally plus 5V) and the V^+ supply (normally plus 15V). This zener is not critical and, in fact, any value between 2V and 10V will work fine. No biasing resistor is needed to establish a current through the zener. In cases where the TTL logic level may go below 2.4V, a pull-up resistor should be added between the TTL output and the plus 5V power supply.

THEORY OF OPERATION

Voltage Translator or Driver Circuit

The translator part of the IH181 family takes the low level strobe input and converts it to plus and minus 15V swing. These voltage swings are necessary to drive the output Varafets so they can switch the maximum analog input signal. As shown in Figures 6 and 7, this translation is performed without drawing any power supply quiescent current. Typical quiescent current is only the $I_{D(off)}$ leakage of the fet — this is usually in the less than 1 nA range. Whether the input strobe logic is in the "1" state or the "0" state makes no difference; the quiescent current remains leakage of FET in the off condition.

The currents previously discussed are dc currents and the obvious result is that the circuit power consumption is going to be low. For example, with plus and minus 15V power supplies, the specified maximum power consumption is 3 mW. The typical power consumption will be 30 nW. When strobing from a particular duty cycle square wave, ac currents will be drawn and the magnitude of these is dependent upon the duty cycle and the pulse repetition rate. Figure 8 shows typical ac current draw as a function of pulse repetition rate.

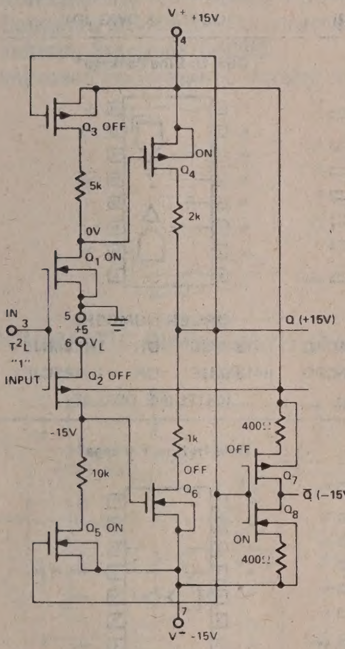


FIGURE 6. DRIVER STATES WITH T^2L "1" INPUT

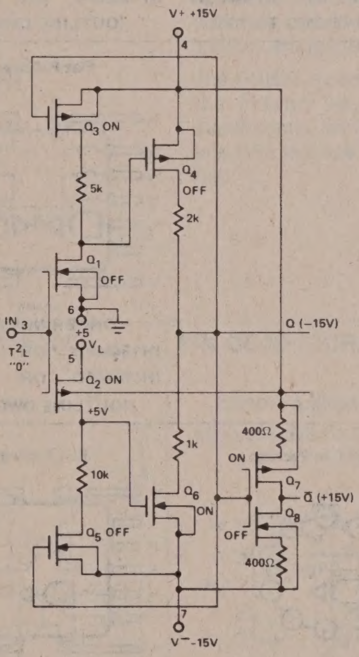


FIGURE 7. DRIVER STATES WITH T^2L "0" INPUT

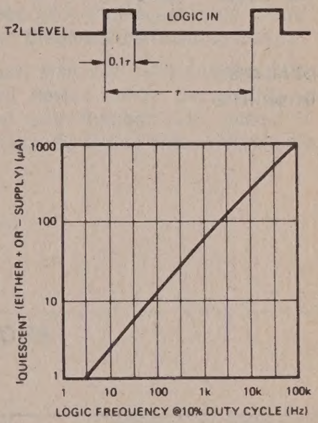


FIGURE 8. POWER SUPPLY QUIESCENT CURRENT VS. LOGIC FREQUENCY RATE

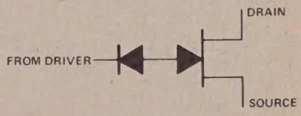


FIGURE 9. OUTPUT VARAFET

THEORY OF OPERATION (CONTINUED)

Output J-Fet or Varafet

The output J-Fet is, of course, the actual solid state switch. The translator circuit is merely a means to interface the low level TTL strobing logic into higher levels to drive the output Fet. The varafet is a monolithicially constructed combination of a varactor diode in series with the gate of an N-channel J-Fet. The driver diode (varactor diode) is needed to prevent forward biasing the output Fet during normal switching applications. Figure 9 shows a schematic of the complete varafet.

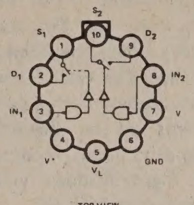
Notice that the polarity of the driver diode is such that it forms a back-to-back diode combination with the source-to-gate or drain-to-gate junctions of the FET. This makes it impossible to forward bias a source-to-gate junction during switching. The driver diode is a voltage variable capacitor whose C (capacity) vs. V (voltage across diode) plot is much greater than the C vs. V plot for either the source-to-gate or drain-to-gate FET junctions. In fact, the criteria for proper operation of the varafet is that the integral of the diode's C vs. V plot is at least equal to the sum of the C vs. V plots for the source-to-gate and drain-to-gate FET junctions. The integral of C vs. V is charge Q. C = Q/V and Q = C X V. Thus the varafet is really a charge transfer device.

SWITCHING STATE DIAGRAMS

DUAL SPST
IH181/IH182

SWITCH STATES ARE FOR LOGIC "1" INPUT

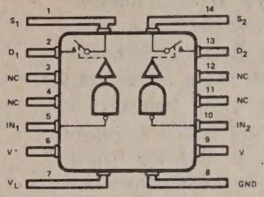
Metal Can Package


S2
S1
D2
D1
IN2
IN1
V
V+
VL
GND
1
2
3
4
5
6
7
8
9
10

TOP VIEW

ORDER NUMBERS:
IH181MTW OR IH181CTW
IH182MTW OR IH182CTW
(OUTLINE DWG TO-100)

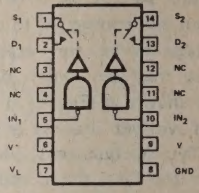
Flat Package


S1
D1
NC
NC
IN1
V+
VL
S2
D2
NC
NC
IN2
V
GND
1
2
3
4
5
6
7
8
9
10
11
12
13
14

TOP VIEW

ORDER NUMBERS:
IH181MFD OR IH181CFD
IH182MFD OR IH182CFD
(OUTLINE DWG FD-2)

Dual-In-Line Package*

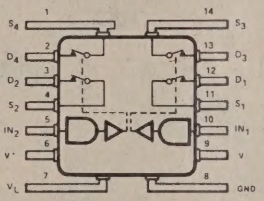

S1
D1
NC
NC
IN1
V+
VL
S2
D2
NC
NC
IN2
V
GND
1
2
3
4
5
6
7
8
9
10
11
12
13
14

TOP VIEW

ORDER NUMBERS:
IH181MID OR IH181CJD
IH182MJD OR IH182CJD
(OUTLINE DWG JD)

DUAL DPST
IH184/IH185

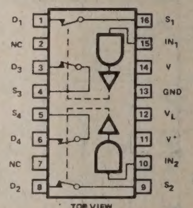
Flat Package


S4
D4
D2
S2
IN2
V+
VL
S3
D3
D1
S1
IN1
V
GND
1
2
3
4
5
6
7
8
9
10
11
12
13
14

TOP VIEW

ORDER NUMBERS:
IH184MFD OR IH184CFD
IH185MFD OR IH185CFD
(OUTLINE DWG FD-2)

Dual-In-Line Package*

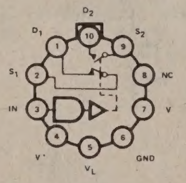

D1
NC
D3
S3
S4
D4
NC
D2
S1
IN1
V
GND
VL
V+
IN2
S2
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

TOP VIEW

ORDER NUMBERS:
IH184MJE OR IH184CJE
IH185MJE OR IH185CJE
(OUTLINE DWG JE)

SPDT
IH187/IH188

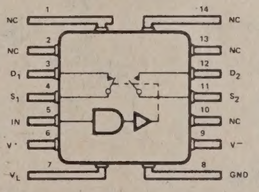
Metal Can Package


D2
D1
S2
S1
NC
IN
V
V+
VL
GND
1
2
3
4
5
6
7
8
9
10

TOP VIEW

ORDER NUMBERS:
IH187MTW OR IH187CTW
IH188MTW OR IH188CTW
(OUTLINE DWG TO-100)

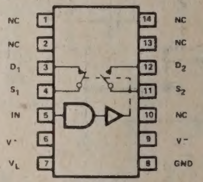
Flat Package


NC
NC
D1
S1
IN
V+
VL
NC
NC
D2
S2
NC
V−
GND
1
2
3
4
5
6
7
8
9
10
11
12
13
14

TOP VIEW

ORDER NUMBERS:
IH187MFD OR IH187CFD
IH188MFD OR IH188CFD
(OUTLINE DWG FD-2)

Dual-In-Line Package*

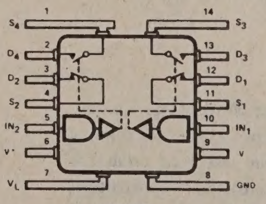

NC
NC
D1
S1
IN
V+
VL
NC
NC
D2
S2
NC
V−
GND
1
2
3
4
5
6
7
8
9
10
11
12
13
14

TOP VIEW

ORDER NUMBERS:
IH187MJD OR IH187CJD
IH188MJD OR IH188CJD
(OUTLINE DWG JD)

DUAL SPDT
IH190/IH191

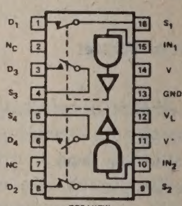
Flat Package


S4
D4
D2
S2
IN2
V+
VL
S3
D3
D1
S1
IN1
V
GND
1
2
3
4
5
6
7
8
9
10
11
12
13
14

TOP VIEW

ORDER NUMBERS:
IH190MFD OR IH190CFD
IH191MFD OR IH191CFD
(OUTLINE DWG FD-2)

Dual-In-Line Package*


D1
NC
D3
S3
S4
D4
NC
D2
S1
IN1
V
GND
VL
V+
IN2
S2
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

TOP VIEW

ORDER NUMBERS:
IH190MJE OR IH190CJE
IH191MJE OR IH191CJE
(OUTLINE DWG JE)

***Side braise ceramic packages special order only. Consult factory.**

DG200/IH5200
CMOS Dual SPST Analog Switches

FEATURES

- Switches Greater Than 28Vpp Signals With ±15V Supplies
- Quiescent Current Less Than 100μA
- Break-Before-Make Switching t_{off} 100nsec, t_{on} 500nsec Typical
- T²L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG200)
- Improved Performance Version (IH5200)

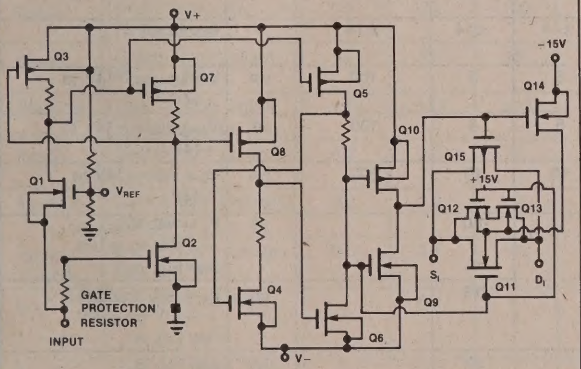
GENERAL DESCRIPTION

The DG200/IH5200 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by INTERSIL's CMOS technology.

Key performance advantages of these devices are TTL compatibility, low-power operation (quiescent current less than 100μA), and guaranteed Break-Before-Make switching.

The DG200 is completely spec and pin-out compatible with the industry standard device, while the IH5200 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

SCHEMATIC DIAGRAM (½ DG200/IH5200)

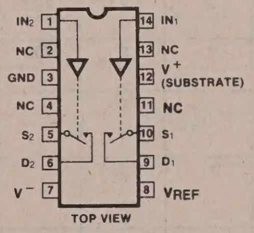

V+
−15V
Q3
Q7
Q5
Q14
Q10
Q8
Q15
+15V
Q1
VREF
Q12
Q13
Q2
S1
D1
Q11
Q4
Q9
GATE PROTECTION RESISTOR
INPUT
Q6
V−

ORDERING INFORMATION

INDUSTRY STANDARD PART	IMPROVED SPEC DEVICE	PACKAGE	TEMPERATURE RANGE
DG200AA	IH5200MTW	10-Pin Metal Can	−55 to +125°C
DG200AK	IH5200MJD	14-Pin CERDIP	−55 to +125°C
DG200AL	IH5200MFD	14-Pin Flat Pak	−55 to +125°C
DG200BA	IH5200ITW	10-Pin Metal Can	−25 to +85°C
DG200BK	IH5200IJD	14-Pin CERDIP	−25 to +85°C
DG200BL	IH5200IFD	14-Pin Flat Pak	−25 to +85°C
DG200CJ	IH5200CPD	14-Pin Epoxy DIP	0 to +70°C

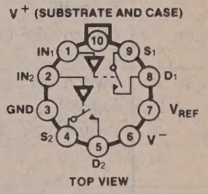
PIN CONFIGURATIONS

CERDIP & EPOXY DUAL-IN-LINE PACKAGE


IN2 1
NC 2
GND 3
NC 4
S2 5
D2 6
V− 7
14 IN1
13 NC
12 V+ (SUBSTRATE)
11 NC
10 S1
9 D1
8 VREF
TOP VIEW

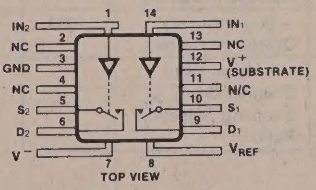
(OUTLINE DWGS JD, PD)

METAL CAN PACKAGE


V+ (SUBSTRATE AND CASE)
10
IN1 1
9 S1
IN2 2
8 D1
GND 3
7 VREF
S2 4
6 V−
5
D2
TOP VIEW

(OUTLINE DWG TO-100)

FLAT PACKAGE


1
14
IN2 2
NC 3
GND 4
NC 5
S2 6
D2
V−
7
8
13 IN1
12 NC
11 V+ (SUBSTRATE)
10 N/C
9 S1
D1
VREF
TOP VIEW

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

(OUTLINE DWG FD-2)

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$	<33V
$V^+ - V_D$	<30V
$V_D - V^-$	<30V
$V_D - V_S$	< ±22V
V_{IN}-GND	<20V

Current (Any Terminal)	>30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation	450mW

(All Leads Soldered to a P.C. Board.) Derate 6mW/°C Above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DG200

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$)

PER CHANNEL		MIN./MAX. LIMITS							TEST
		MILITARY			COMMERCIAL/INDUSTRIAL				
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0/−25°C	+25°C	+70°C/+85°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(on)}$	Drain-Source On Resistance	70	70	100	80	80	100	Ω	$I_S = 1mA$, $V_{ANALOG} = \pm 10V$
$r_{DS(on)}$	Channel-to-Channel $R_{DS(on)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±14	±14	±14	±14	±14	±14	V	$I_S = 10mA$
$I_{D(OFF)}$	Switch OFF Leakage Current	2	2	100	5	5	100	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{S(OFF)}$	Switch OFF Leakage Current	2	2	100	5	5	100	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{D(ON)} + I_{S(ON)}$	Switch ON Leakage Current	2	2	200	10	10	200	nA	$V_D = V_S = -14V$ to $+14V$
t_{on}	Switch "ON" Time		1.0			1.0		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
t_{off}	Switch "OFF" Time		0.5			0.5		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C
I_{V1}	+ Power Supply Quiescent Current	1000	1000	2000	1000	1000	2000	μA	$V_{IN} = 0V$ or $V_{IN} = 5V$
I_{V2}	− Power Supply Quiescent Current	1000	1000	2000	1000	1000	2000	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

TEST CIRCUITS

Figure A

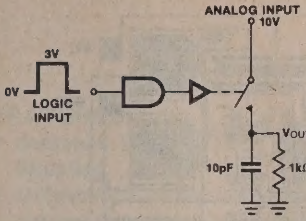


Figure B

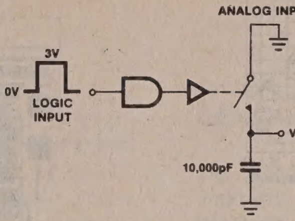
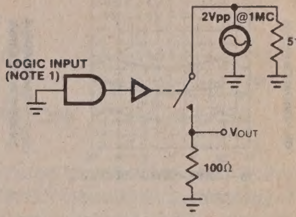


Figure C



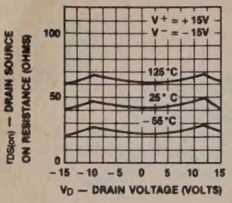
IH5200

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$, V_{REF} open)

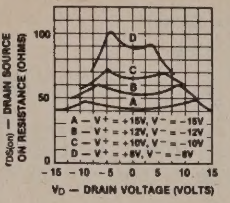
PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL/INDUSTRIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0/−25°C	+25°C	+70°C/+85°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(on)}$	Drain-Source On Resistance	70	70	100	80	80	100	Ω	$I_S = 1mA$, $V_{ANALOG} = \pm 10V$
$r_{DS(on)}$	Channel-to-Channel $R_{DS(on)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±14	±14	±14	±14	±14	±14	V	$I_S = 10mA$
$I_{D(OFF)}$	Switch OFF Leakage Current	0.2	0.2	50	1	1	50	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{S(OFF)}$	Switch OFF Leakage Current	0.2	0.2	50	1	1	50	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{D(ON)} + I_{S(ON)}$	Switch ON Leakage Current	0.5	0.5	100	1	1	100	nA	$V_D = V_S = -14V$ to $+14V$
t_{on}	Switch "ON" Time		0.7			0.8		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
t_{off}	Switch "OFF" Time		0.25			0.4		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
$Q_{(INJ.)}$	Charge Injection		5			10		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1MHz, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C
I_{V1}	+ Power Supply Quiescent Current	250	200	150	300	250	200	μA	$V_{IN} = 0V$ or $V_{IN} = 5V$
I_{V2}	− Power Supply Quiescent Current	10	10	100	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

TYPICAL CHARACTERISTICS

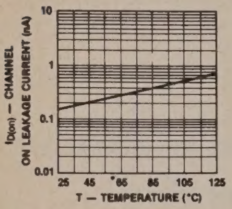
$r_{DS(on)}$ vs V_D and Temperature



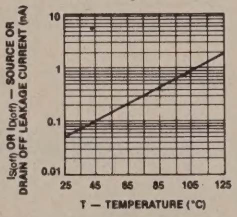
$r_{DS(on)}$ vs V_D and Power Supply Voltage



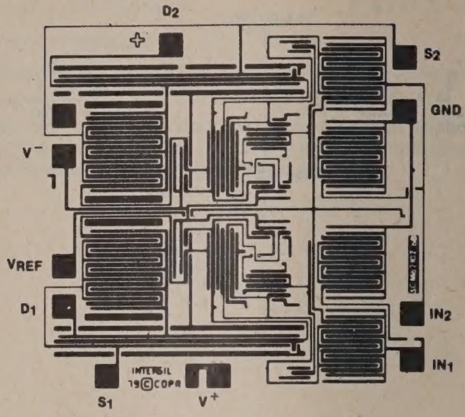
$I_{D(on)}$ vs Temperature*



$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*



CHIP TOPOGRAPHY



NOTE: Backside of chip of common to V+.

APPLICATIONS

Application Hints

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15	−15	Open	2.4/0.8	−15 to +15
+12	−12	Open or 1.4V	2.4/0.8	−12 to +12
+10	−10	1.4V	2.4/0.8	−10 to +10
+8*	−8	1.4V	2.4/0.8	−8 to +8

*Operation below ±8V is not recommended.

Logic Inputs

Logic input circuitry protects the input MOS gate from transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply; negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection it should be limited to less than 4.7kΩ to ensure switching with worst case current spikes.

The Function of V_{REF}

V_{REF} is an internal connection which allows the user to establish the logic threshold voltage at which the switch changes state. The actual threshold voltage is equal to the voltage on the V_{REF} pin; V_{REF} is internally connected for a 1.4V threshold at $V^+ = +15V$. For other thresholds and/or supply voltages, V_{REF} may be connected to a voltage source or resistive divider whose output voltage is equal to the desired threshold. The internal impedance of V_{REF} is 21kΩ ±30%.

Additionally, to adjust V_{REF}, a single pullup resistor can be used from the V_{REF} pin to a positive supply voltage to shunt the upper internal divider resistor. The equation below shows the calculation of the shunt resistor for the desired logic threshold voltage — this calculation is based on nominal internal resistor values, which are ±30% in absolute magnitude. The adjusted trip point voltage (V_{REF}) should be limited to an upper level of 5V to avoid input logic switching transition hysteresis.

$$R_{SHUNT} = \frac{R1 \times R2 \left(\frac{V^+}{V_{tr}} - 1 \right)}{R1 - R2 \left(\frac{V^+}{V_{tr}} - 1 \right)}$$

Calculation of R_{SHUNT}

Where $R1 \cong 220k\Omega$: nominal values,

$R2 \cong 23k\Omega$ ±30% run-to-run

Example: for $V^+ = 15V$, $V_{TRIP} = 5V$, using nominal R1, R2 calculation $R_{SHUNT} = 58k\Omega$.

INTERSIL

IH200
CMOS Analog Gate

FEATURES

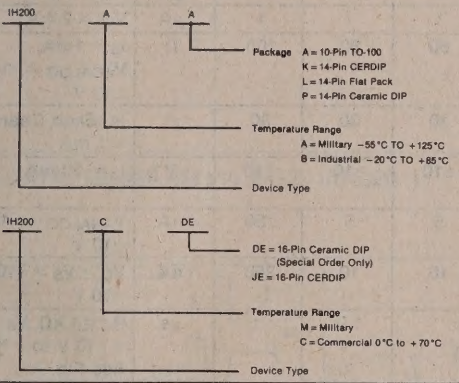
- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 10μA**
- **Overvoltage Protection to ±25V**
- **Break-Before-Make Switching: t_{OFF} 200 nsec, t_{ON} 400nsec Typical**
- **T²L, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**

GENERAL DESCRIPTION

The IH200 solid state analog gate is designed using an improved, high voltage CMOS monolithic technology. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The INTERSIL CMOS technology has eliminated this serious systems problem.

Key performance advantages of the IH200 are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 10μA. Also designed into the IH200 is guaranteed Break-Before-Make switching. This is logically accomplished by extending the t_{ON} time (400 nsec TYP.) such that it exceeds t_{OFF} time (200 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

ORDERING INFORMATION



IH200 A A

Package A = 10-Pin TO-100
K = 14-Pin CERDIP
L = 14-Pin Flat Pack
P = 14-Pin Ceramic DIP

Temperature Range
A = Military −55°C TO +125°C
B = Industrial −20°C TO +85°C

Device Type

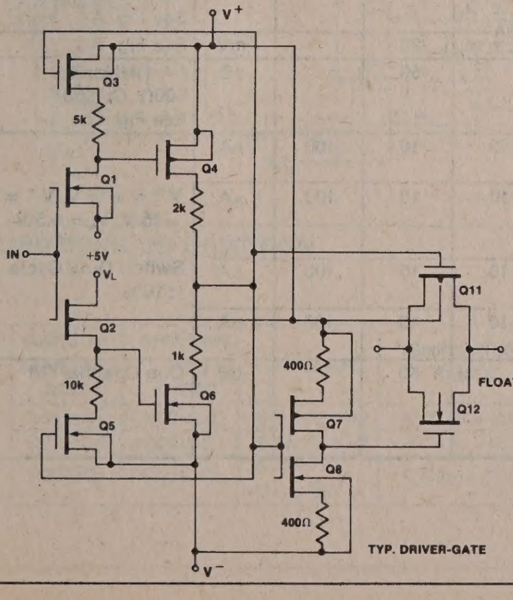
IH200 C DE

DE = 16-Pin Ceramic DIP
(Special Order Only)
JE = 16-Pin CERDIP

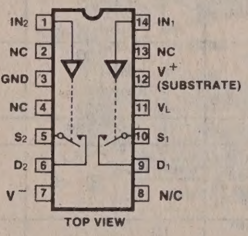
Temperature Range
M = Military
C = Commercial 0°C to +70°C

Device Type

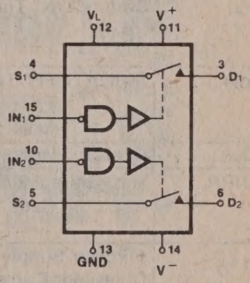
FUNCTIONAL DIAGRAM


V+
Q3
5k
Q4
Q1
2k
IN
+5V
VL
Q11
Q2
1k
400Ω
FLOATS
10k
Q6
Q12
Q5
Q7
Q8
400Ω
TYP. DRIVER-GATE
V−

PIN CONFIGURATIONS

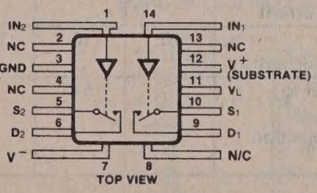

IN2 1
NC 2
GND 3
NC 4
S2 5
D2 6
V− 7
14 IN1
13 NC
12 V+ (SUBSTRATE)
11 VL
10 S1
9 D1
8 N/C
TOP VIEW

OUTLINE DWGS
DD, JD

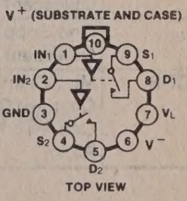

VL 12
V+ 11
4 S1
3 D1
15 IN1
10 IN2
5 S2
6 D2
13 GND
14 V−

OUTLINE DWGS
DE, JE

SWITCH STATES ARE FOR LOGIC
"1" INPUT (POSITIVE LOGIC)


1
14
IN2
2
NC
3
GND
4
NC
5
S2
6
D2
V−
7
8
IN1
13
NC
12
V+ (SUBSTRATE)
11
VL
10
S1
9
D1
N/C
TOP VIEW

OUTLINE DWG
FD-2


V+ (SUBSTRATE AND CASE)
10
IN1 1
9 S1
IN2 2
8 D1
GND 3
7 VL
S2 4
6 V−
5
D2
TOP VIEW

OUTLINE DWG
TO-100

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) .... <30mA
Storage Temperature .... −65°C to +150°C
Operating Temperature .... −55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C
Lead Temperature (Soldering, 10 sec) .... 300°C

V^+-V^- .... <33V
V^+-V_D .... <30V
V_D-V^- .... <30V
V_D-V_S .... <±22V
V_L-V^- .... <33V
V_L-V_{IN} .... <30V
V_L-GND .... <20V
V_{IN}-GND .... <20V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8 V
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4 V
$r_{DS(ON)}$	Drain-Source On Resistance	75	75	100	80	80	100	Ω	I_S = 1mA, V_{ANALOG} = −10 V to ±10 V
$r_{DS(ON)}$	Channel to Channel R_{DS}(ON) Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1 mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±11	±11	±11	±10	±10	±10	V	I_S = 10 mA
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	250	nA	V_{ANALOG} = −10 V to +10 V
$I_{D(ON)}$ $+I_{S(ON)}$	Switch On Leakage Current	2	2	200	10	10	250	nA	$V_D = V_S$ = −10 V to +10 V
t_{ON}	Switch "ON" Time		1.0			1.0		μs	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
t_{OFF}	Switch "OFF" Time		0.5			0.5		μs	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤5pF See Fig. C
I^+_Q	+ Power Supply Quiescent Current	10	10	100	10	10	100	μA	$V^+ = +15$ V, $V^- = -15$ V, $V_L = +5$ V Switch Duty Cycle <10%
I^-_Q	−Power Supply Quiescent Current	10	10	100	10	10	100	μA	
I_{LVQ}	+5 V Supply Quiescent Current	10	10	100	10	10	100	μA	
I_{GND}	Gnd Supply Quiescent Current	10	10	100	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

INTERSIL

DG201/IH5201
Quad SPST CMOS Analog Switches

FEATURES

- **Switches Greater Than 28V_{p-p} Signals With ±15V Supplies**
- **Quiescent Current Less Than 100μA**
- **Break-Before-Make Switching t_{off} = 100nsec, t_{on} = Typically 500nsec**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **Industry Standard (DG201)**
- **Improved Performance Version IH5201**

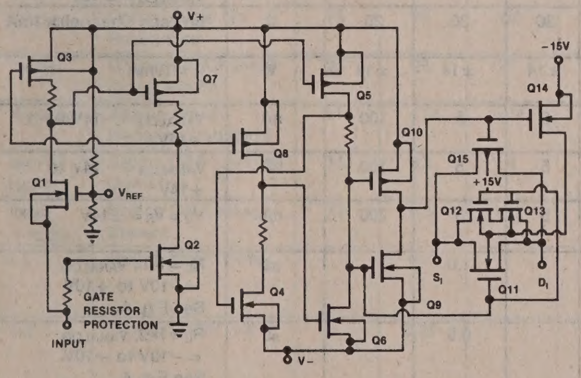
GENERAL DESCRIPTION

The DG201/IH5201 solid-state analog gates are designed using an improved, high-voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid-state switches. Destructive latch-up of solid-state analog gates has been eliminated by INTERSIL's CMOS technology.

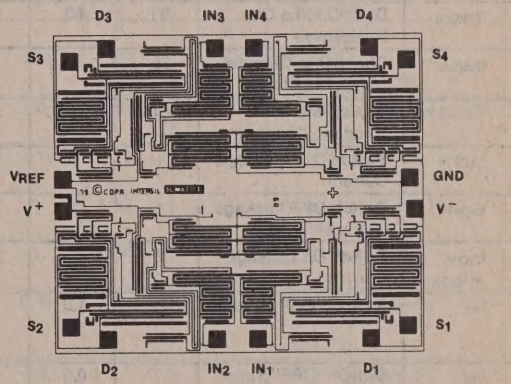
Key performance advantages of these devices are TTL compatibility, low-power operation (quiescent current less than 100μA), and guaranteed break-before-make switching.

The DG201 is completely spec and pin-out compatible with the industry standard device, while the IH5201 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

SCHEMATIC DIAGRAM (¼ DG201/IH5201)


V+
Q3
Q7
Q5
−15V
Q14
Q10
Q15
+15V
Q8
Q1
V_{REF}
Q12
Q13
Q2
S
D
Q11
Q4
Q9
GATE
RESISTOR
PROTECTION
INPUT
Q6
V−

CHIP TOPOGRAPHY


D3
IN3
IN4
D4
S3
S4
VREF
GND
V+
V−
S2
S1
D2
IN2
IN1
D1

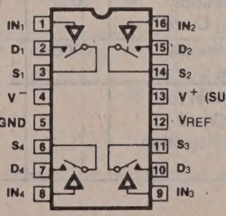
NOTE: Backside of chip common to V+.

ORDERING INFORMATION

INDUSTRY STANDARD PART	IMPROVED SPEC DEVICE	PACKAGE	TEMPERATURE RANGE
DG201AK	IH5201MJE	16-Pin CERDIP	−55°C to +125°C
DG201BK	IH5201IJE	16-Pin CERDIP	−20°C to +85°C
DG201CJ	IH5201CPE	16-Pin Plastic DIP	0°C to +70°C

PIN CONFIGURATIONS (Outline dwgs JE, PE)

DUAL-IN-LINE PACKAGE


IN1 1
D1 2
S1 3
V− 4
GND 5
S4 6
D4 7
IN4 8
16 IN2
15 D2
14 S2
13 V+ (SUBSTRATE)
12 VREF
11 S3
10 D3
9 IN3

SWITCH OPEN FOR LOGIC "1" INPUT

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$	<33V
$V^+ - V_D$	<30V
$V_D - V^-$	<30V
$V_D - V_S$	< ±22V
$V_{REF} - V^-$	<33V
$V_{REF} - V_{IN}$	<30V
V_{REF}-GND	<20V
V_{IN}-GND	<20V

Current (Any Terminal)	<30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation	450mW

Derate 6mW/°C Above 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DG201

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0°C	+25°C	+70°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	µA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	µA	$V_{IN} = 2.4V$
$r_{DS(ON)}$	Drain-Source On Resistance	80	80	125	100	100	125	Ω	$I_S = 1mA$, $V_{ANALOG} = \pm 10V$
$r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1mA
V_{ANALOG}	Analog Signal Handling Capability	±14	±14	±14	±14	±14	±14	V	$I_S = 10mA$
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	$V_{ANALOG} = -14V$ to +14V
$I_{S(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	$V_{ANALOG} = -14V$ to +14V
$I_{D(ON)} + I_{S(ON)}$	Switch On Leakage Current	2	2	200	5	5	200	nA	$V_D = V_S = \pm 14V$
t_{on}	Switch "ON" Time		1.0			1.0		µs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to +10V See Fig. A
t_{off}	Switch "OFF" Time		0.5			0.5		µs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to +10V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C
I_Q^+	+ Power Supply Quiescent Current	2000	1000	2000	2000	1000	2000	µA	$V_{IN} = 0V$ or 5V
I_Q^-	− Power Supply Quiescent Current	2000	1000	2000	2000	1000	2000	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

TEST CIRCUITS

Figure A

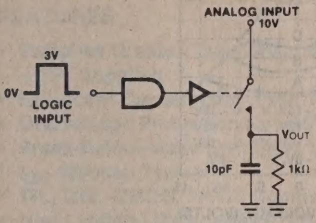

ANALOG INPUT
10V
3V
0V
LOGIC INPUT
VOUT
10pF
1kΩ

Figure B

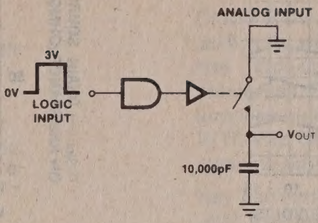
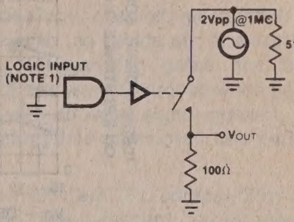

ANALOG INPUT
3V
0V
LOGIC INPUT
VOUT
10,000pF

Figure C

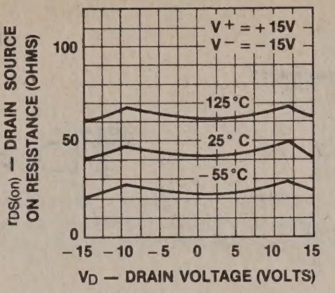

2Vpp @1MC
51Ω
LOGIC INPUT
(NOTE 1)
VOUT
100Ω

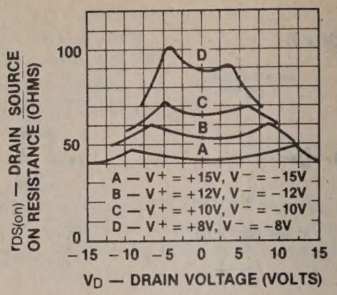
IH5201

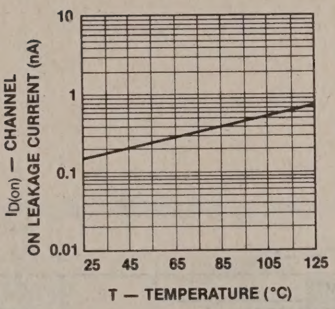
ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$)

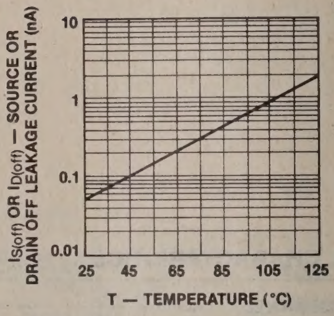
PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0°C	+25°C	+70°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(ON)}$	Drain-Source On Resistance	75	75	100	100	100	125	Ω	$I_S = 1mA$, $V_{ANALOG} = \pm 10V$
$r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1mA
V_{ANALOG}	Analog Signal Handling Capability	±14	±14	±14	±14	±14	±14	V	$I_S = 10mA$
$I_{D(OFF)}$/ $I_{S(OFF)}$	Switch OFF Leakage Current	0.2	0.2	50	1	1	50	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{D(ON)}$ $+ I_{S(ON)}$	Switch ON Leakage Current	0.5	0.5	100	1	1	100	nA	$V_D = V_S = \pm 14V$
t_{on}	Switch "ON" Time		0.5			0.75		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
t_{off}	Switch "OFF" Time		0.25			0.3		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
$Q_{(INJ.)}$	Charge Injection		5			10		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C
I_Q^+	+ Power Supply Quiescent Current	1000	750	600	1500	1000	1000	μA	$V_{IN} = 0V$ to $5V$
I_Q^-	− Power Supply Quiescent Current	10	10	100	20	20	200	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

TYPICAL CHARACTERISTICS









APPLICATIONS

Application Hints

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	VREF Reference Pin Connection (V)	VIN Logic Input Voltage VINH Min/ VINL Max (V)	VS or VD Analog Voltage Range (V)
+15	−15	Open	2.4/0.8	−15 to +15
+12	−12	Open or 1.4V	2.4/0.8	−12 to +12
+10	−10	1.4V	2.4/0.8	−10 to +10
+8*	−8	1.4V	2.4/0.8	−8 to +8

*Operation below ±8V is not recommended.

Logic Inputs

Logic input circuitry protects the input MOS gate from transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply; negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection it should be limited to less than 4.7kΩ to ensure switching with worst case current spikes.

The Function of V_{REF}

V_{REF} is an internal connection which allows the user to establish the logic threshold voltage at which the switch changes state. The actual threshold voltage is equal to the voltage on the V_{REF} pin; V_{REF} is internally connected for a 1.4V threshold at $V^+ = +15V$. For other thresholds and/or supply voltages, V_{REF} may be connected to a voltage source or resistive divider whose output voltage is equal to the desired threshold. The internal impedance of V_{REF} is 21kΩ ±30%.

Additionally, to adjust V_{REF}, a single pullup resistor can be used from the V_{REF} pin to a positive supply voltage to shunt the upper internal divider resistor. The equation below shows the calculation of the shunt resistor for the desired logic threshold voltage — this calculation is based on nominal internal resistor values, which are ±30% in absolute magnitude. The adjusted trip point voltage (V_{REF}) should be limited to an upper level of 5V to avoid input logic switching transition hysteresis.

$$R_{SHUNT} = \frac{R1 \times R2 \left(\frac{V^+}{V_{tr}} - 1 \right)}{R1 - R2 \left(\frac{V^+}{V_{tr}} - 1 \right)}$$

Calculation of R_{SHUNT}

Where $R1 \cong 220k\Omega$: nominal values,
$R2 \cong 23k\Omega$ ±30% run-to-run

Example: for $V^+ = 15V$, $V_{TRIP} = 5V$, using nominal R1, R2 calculation $R_{SHUNT} = 58k\Omega$.

INTERSIL

IH201/IH202
CMOS Analog Gate

FEATURES

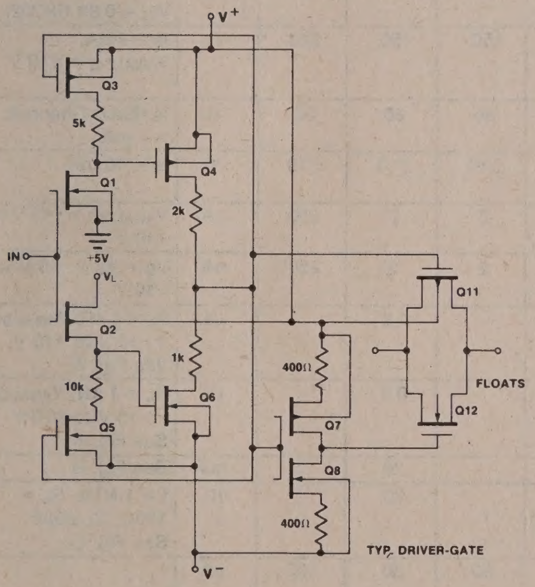
- **Switches Greater Than 20$V_{p\text{-}p}$ Signals With ±15V Supplies**
- **Quiescent Current Less Than 10μA**
- **Overvoltage Protection to ±25V**
- **Break-Before-Make Switching t_{OFF} 200nsec, t_{ON} 400nsec Typical**
- **T²L, DTL, DMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **IH201 Four Normally Closed Switches**
- **IH202 Four Normally Open Switches**
- **Low Leakage Typical <100pA**

GENERAL DESCRIPTION

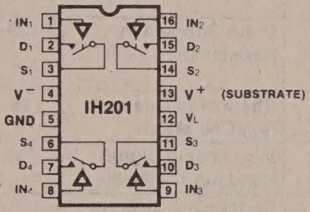
The IH201/2 Solid State Analog Gate is designed using an improved, high voltage CMOS technology. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device and the destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The INTERSIL CMOS technology has eliminated this serious systems problem.

Key performance of the IH201 are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 10μA. Also designed into the IH201/2 is guaranteed Break-Before-Make switching. This is logically accomplished by extending the t_{ON} time (400nsec Typical) such that it exceeds t_{OFF} time (200nsec Typical). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel-to-channel shorting during switching.

FUNCTIONAL DIAGRAM

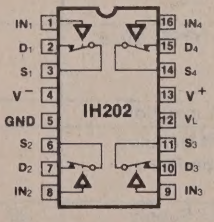

V+
Q3
5k
Q4
Q1
2k
IN
+5V
VL
Q11
Q2
1k
400Ω
FLOATS
10k
Q6
Q12
Q5
Q7
Q8
400Ω
TYP. DRIVER-GATE
V−

PIN CONFIGURATION


IN1 1
D1 2
S1 3
V− 4
GND 5
S4 6
D4 7
IN4 8
16 IN2
15 D2
14 S2
13 V+ (SUBSTRATE)
12 VL
11 S3
10 D3
9 IN3
IH201

ORDER NUMBERS:
IH201MDE OR IH201CDE

SWITCH STATES ARE
FOR LOGIC "1" INPUT


IN1 1
D1 2
S1 3
V− 4
GND 5
S2 6
D2 7
IN2 8
16 IN4
15 D4
14 S4
13 V+
12 VL
11 S3
10 D3
9 IN3
IH202

ORDER NUMBERS:
IH202MDE OR IH202CDE

ORDERING INFORMATION

IH201 M JE

PACKAGE DE = 16-PIN CERAMIC DIP (Special Order Only)
JE = 16-PIN CERDIP

TEMPERATURE RANGE
M = MILITARY −55°C TO +125°C
C = COMMERCIAL 0°C TO +70°C

DEVICE CHIP TYPE

MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal)	<30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board)	
Derate 6mW/°C Above 70°C	
Lead Temperature (Soldering, 10 sec)	300°C

$V^+ - V^-$	<33V
$V^+ - V_D$	<30V
$V_D - V^-$	<30V
$V_D - V_S$	<±22V
$V_L - V^-$	<33V
$V_L - V_{IN}$	<30V
V_L-GND	<20V
V_{IN}-GND	<20V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$.)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8 V (IH201), V_{IN} = 2.4V (IH202)
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4 V (IH201), V_{IN} = 0.8V (IH202)
$r_{DS(ON)}$	Drain-Source On Resistance	100	100	200	150	150	200	Ω	I_S = 1mA, V_{ANALOG} = ±10 V
$r_{DS(ON)}$	Channel to Channel R_{DS}(ON) Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1 mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±11	±11	±11	±10	±10	±10	V	I_S = 10 mA
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	200	2	2	250	nA	V_{ANALOG} = −10 V to +10 V
$I_{D(ON)}$ $+I_{S(ON)}$	Switch On Leakage Current	2	2	200	2	2	250	nA	$V_D = V_S$ = −10 V to +10 V
t_{ON}	Switch "ON" Time		1.0			1.0		μs	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
t_{OFF}	Switch "OFF" Time		0.5			0.5		μs	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤5pF See Fig. C
I^+_Q	+ Power Supply Quiescent Current	20	20	100	30	30	100	μA	V^+ = +15 V, V^- = −15 V, V_L = +5V Switch Duty Cycle < 10%
I^-_Q	−Power Supply Quiescent Current	20	20	100	30	30	100	μA	
I_{VQ}	+5 V Supply Quiescent Current	20	20	100	30	30	100	μA	
I_{GND}	Gnd Supply Quiescent Current	20	20	100	20	20	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

TEST CIRCUITS

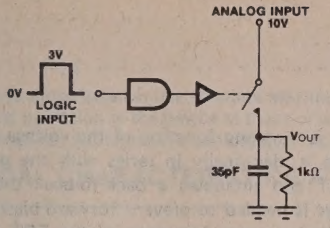

ANALOG INPUT
10V
3V
0V
LOGIC INPUT
VOUT
35pF
1kΩ

Figure A

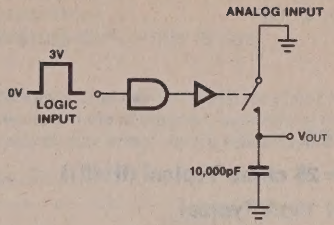

ANALOG INPUT
3V
0V
LOGIC INPUT
VOUT
10,000pF

Figure B

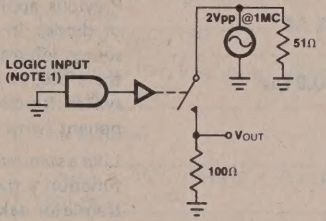

2Vpp @1MC
51Ω
LOGIC INPUT (NOTE 1)
VOUT
100Ω

Figure C

INTERSIL

IH401/IH401A
VARAFET Switch

FEATURES

- $r_{DS(on)} = 25$ ohms Typical (IH401)
- $I_{D(off)}$ of 10pA Typical
- Switching Times of 25ns for t_{on} and 75ns for t_{off} ($R_L = 1k\Omega$)
- Built-In Overvoltage Protection to Plus or Minus 25V
- Charge Injection of 3mV Typical into 0.01μF Capacitor
- $C_{iss} < 1pF$ Typical
- Can Be Used for Hybrid Construction

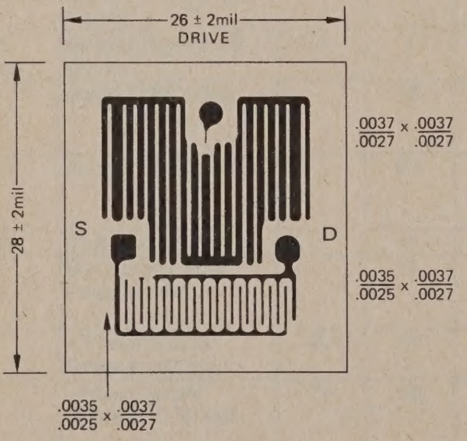
GENERAL DESCRIPTION

The IH401 is made up of 4 monolithically constructed combinations of a varactor type diode and an N-channel Junction FET. The FET itself is very similar to the popular 2N4391, and the driver diode is a specially designed diode, such that its capacity is a strong function of the voltage across it. The driver diode is electrically in series with the gate of the N-channel FET and simulates a back-to-back diode structure; this structure is needed to prevent forward biasing the source-to-gate or drain-to-gate junctions of the FET when used in switching applications.

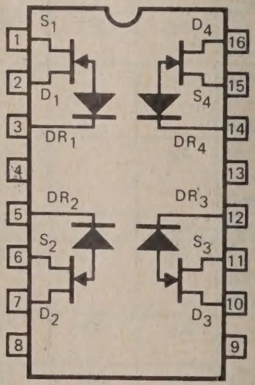
Previous applications of Junction FETs required the addition of diodes, in series with the gate, and then perhaps a gate-to-source referral resistor or a capacitor in parallel with the diode; therefore, at least 3 components were required to perform the switch function. The IH401 does this same job in one component (with a great deal better performance characteristics).

Like a standard FET, to practically perform a solid state switch function a translator should be added to drive the diode. This translator takes the T^2L levels and converts them to voltages required to drive the diode/FET system (typically a 0V to −15V translation and a 3V to +15V shift). With ±15V power supplies, the IH401 will typically switch $18_{p\text{-}p}$ at any frequency from DC to 20MHz, with less than 30 ohms $r_{DS(on)}$. The IH401A will typically switch $22V_{p\text{-}p}$ with less than 50 ohms $r_{DS(on)}$.

TOPOGRAPHY


26 ± 2mil
DRIVE
28 ± 2mil
S
D
.0037/.0027 x .0037/.0027
.0035/.0025 x .0037/.0027
.0035/.0025 x .0037/.0027

SCHEMATIC/PIN CONFIGURATION
(Outline Dwg JE)



ORDERING INFORMATION

CERDIP Package: IH401JE
IH401AJE

IH401/IH401A

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 35V
V^+ 35V
V^- 35V
V^+ to V_{IN} 40V

Operating Temperature . . . . −55°C to +125°C
Storage Temperature . . . . −65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise specified)

SYMBOL	CHARACTERISTIC	CONDITIONS	IH401			UNIT
			MIN	TYP	MAX	
$r_{DS(on)}$	Switch "on" Resistance	$V_{DRIVE} = 15V$, $V_{DRAIN} = -7.5V$ $I_D = 10mA$		20	30	Ω
V_P	Pinch-Off Voltage	$I_D = 1\ nA$, $V_{DS} = 10V$	4	6	7.5	V
$I_{D(off)}$	Switch "off" Current or "off" Leakage	$V_{DRIVE} = -15V$, $V_{SOURCE} = -7.5V$, $V_{DRAIN} = +7.5V$		10	200	pa
$I_{D(off)}$	Switch "off" Leakage at 125°C	Same as Above		0.25	50	na
$I_{S(off)}$	Switch "off" Current	$V_{DRIVE} = -15V$, $V_{DRAIN} = -7.5V$, $V_{SOURCE} = +7.5V$		10	200	pa
$I_{S(off)}$	Switch "off" Leakage at 125°C	Same as Above		0.3	50	na
$I_{D(on)}$ + $I_{S(on)}$	Switch Leakage when Turned "on"	$V_D = V_S = -7.5V$, $V_{DRIVE} = +15V$		0.02	2	na
V_{analog}	AC Input Voltage Range without Distortion	See Figure B	15	18		$V_{p\text{-}p}$
V_{inject}	Charge Injection Amplitude	See Figure C		3	10	$mV_{p\text{-}p}$
BV_{diode}	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	$V_D = V_S = -V$, $I_{DRIVE} = 1\ \mu A$, $V_{DRIVE} = 0V$	−30	−45		V
BV_{GSS}	Gate to Source or Gate to Drain Reverse Breakdown Voltage	$V_{DRIVE} = -V$, $V_D = V_S = 0V$, $I_{DRIVE} = 1\ \mu A$	30	41		V
I_{DSS}	Maximum Current Switch can Deliver (Pulsed)	$V_{DRIVE} = 15V$, $V_S = 0V$, $V_D = +10V$	45	70		mA
t_{on}	Switch "on" time (Note 1)	See Figure A		25	50	ns
t_{off}	Switch "off" time (Note 1)	See Figure A		75	150	ns

NOTE 1: Driving waveform must be >100ns rise and fall time.

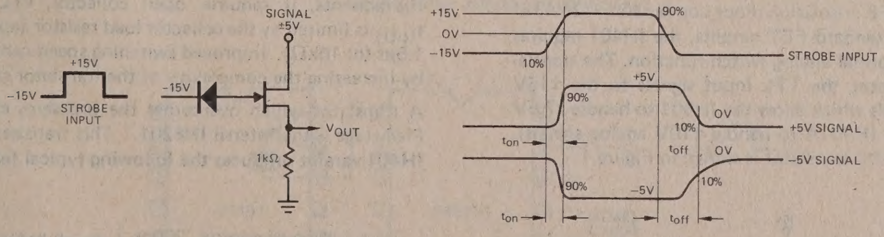


FIGURE A

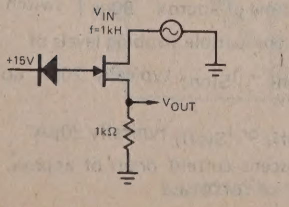


FIGURE B

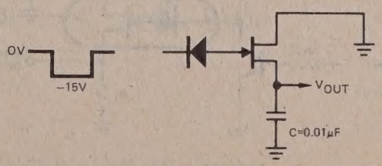


FIGURE C

ADDED NOTE:

The IH401A lends itself very well to hybrid construction i.e.; chip requirement.

ELECTRICAL CHARACTERISTICS AT 25° C (unless otherwise specified)

SYMBOL	CHARACTERISTIC	CONDITIONS	IH401A			UNIT
			MIN	TYP	MAX	
$r_{DS(on)}$	Switch "on" Resistance	$V_{DRIVE} = 15V$, $V_{DRAIN} = -10V$, $I_D = 10mA$		35	50	Ω
V_P	Pinch-Off Voltage	$I_D = 1$ nA, $V_{DS} = 10V$	3	4	5	V
$I_{D(off)}$	Switch "off" Current or "off" Leakage	$V_{DRIVE} = -15V$, $V_{SOURCE} = -10V$, $V_{DRAIN} = +10V$		10	200	pa
$I_{D(off)}$	Switch "off" Leakage at 125°C	Same as Above		0.25	50	na
$I_{S(off)}$	Switch "off" Current	$V_{DRIVE} = -15V$, $V_{DRAIN} = -10V$, $V_{SOURCE} = +10V$		10	200	pa
$I_{S(off)}$	Switch "off" Leakage at 125°C	Same as Above		0.3	50	na
$I_{D(on)} +$ $I_{S(on)}$	Switch Leakage when Turned "on"	$V_D = V_S = -10V$, $V_{DRIVE} = +15V$		0.02	2	na
V_{analog}	AC Input Voltage Range without Distortion	See Figure B	20	22		$V_{p\text{-}p}$
V_{inject}	Charge Injection Amplitude	See Figure C		3	10	$mV_{p\text{-}p}$
BV_{diode}	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	$V_D = V_S = -V$, $I_{DRIVE} = 1\ \mu A$, $V_{DRIVE} = 0V$	−30	−45		V
BV_{GSS}	Gate to Source or Gate to Drain Reverse Breakdown Voltage	$V_{DRIVE} = -V$, $V_D = V_S = 0V$, $I_{DRIVE} = 1\ \mu A$	30	41		V
I_{DSS}	Maximum Current Switch can Deliver (Pulsed)	$V_{DRIVE} = 15V$, $V_S = 0V$, $V_D = +10V$	35	55		mA
t_{on}	Switch "on" time (Note 1)	See Figure A		25	50	ns
t_{off}	Switch "off" time (Note 1)	See Figure A		75	150	ns

NOTE: Driving waveform must be >100ns rise and fall time.

APPLICATIONS

IH401 FAMILY

In general, the IH401 family can be used in any application formally using a JFET/isolation diode combination (2N4391 or similar). Like standard FET circuits, the IH401 requires a translator for normal analog switch function. The translator is used to boost the TTL input signals to the ±15V analog supply levels which allow the IH401 to handle ±7.5V analog signals (or IH401A to handle ±10V analog signals). A typical simple PNP translator is shown in Figure 1.

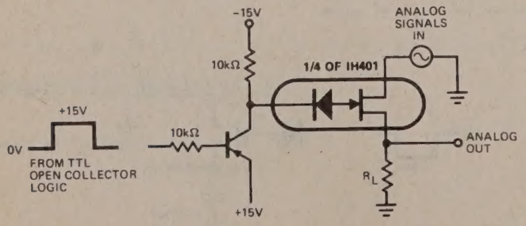
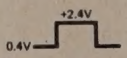


FIGURE 1

Although this simple PNP circuit represents a minimum of components, it requires open collector TTL input and $t_{(off)}$ is limited by the collector load resistor (approximately 1.5μs for 10kΩ). Improved switching speed can be obtained by increasing the complexity of the translator stage.

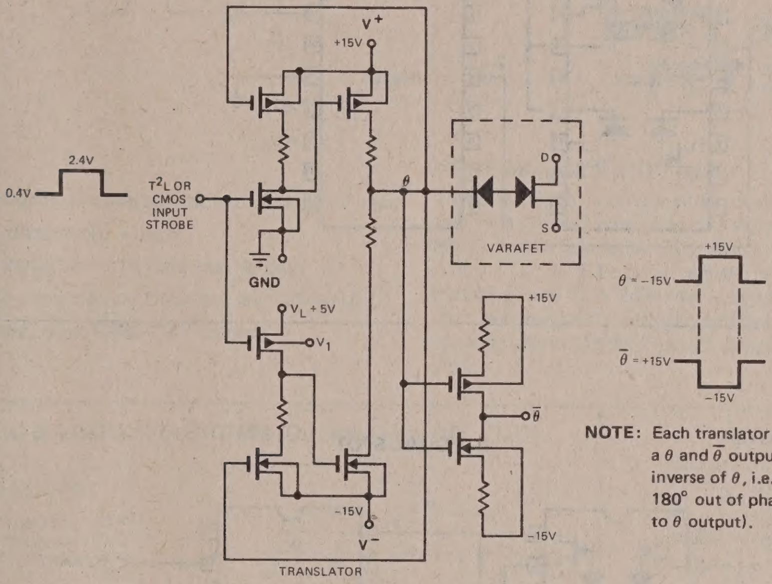
A translator which overcomes the problems of the simple PNP stage is the Intersil IH6201.* This translator driving an IH401 varafet produces the following typical features:

- t_{on} time of approx. 200ns } break before make
- t_{off} time of approx. 80ns } switch
- TTL compatible strobing levels of 

- $I_{D(on)} + I_{S(on)}$ typically 20pA up to ±10V analog signals
- $I_{D(off)}$ or $I_{S(off)}$ typically 20pA
- Quiescent current drain of approx. 100nA in either "on" or "off" case

APPLICATIONS (Cont.)

*The IH6201 is a dual translator (two independent translators per package) constructed from monolithic CMOS technology. The schematic of one-half IH6201, driving one-fourth of an IH401, is shown in Figure 2.

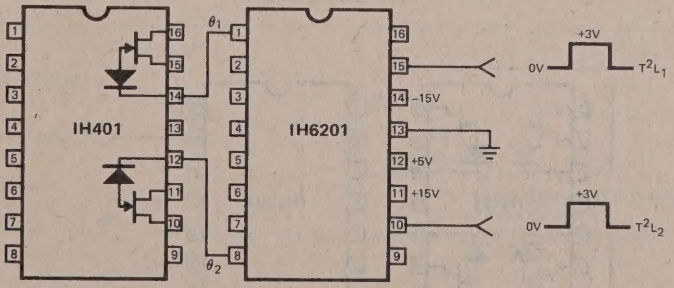

V+
+15V
2.4V
0.4V
T²L OR CMOS INPUT STROBE
GND
V_L +5V
V1
−15V
V−
TRANSLATOR
θ
D
S
VARAFET
+15V
θ̄
−15V
+15V
θ = −15V
θ̄ = +15V
−15V

NOTE: Each translator output has a θ and $\bar{\theta}$ output. $\bar{\theta}$ is just the inverse of θ, i.e., ($\bar{\theta}$ output is 180° out of phase with respect to θ output).

FIGURE 2

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See III.)

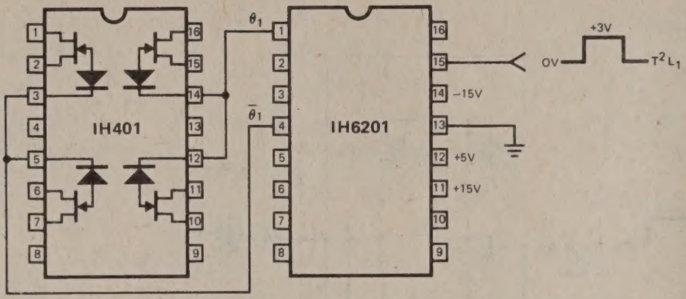
I. DUAL SPST ANALOG SWITCH


IH401
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
θ1
θ2
IH6201
1
2
3
4
5
6
7
8
16
15
14 −15V
13
12 +5V
11 +15V
10
9
+3V
0V
T²L1
+3V
0V
T²L2

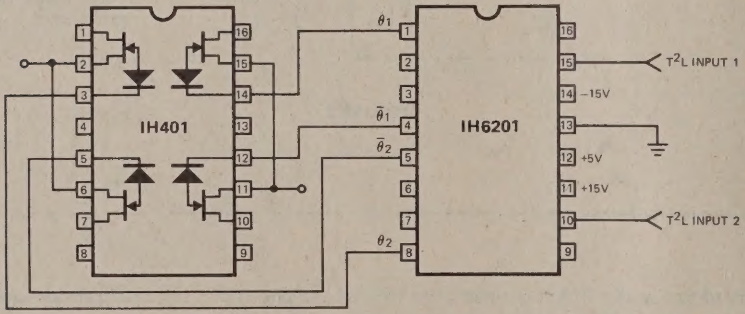
NOTE: Either switch is turned on when strobe input goes high.

APPLICATIONS (Cont.)

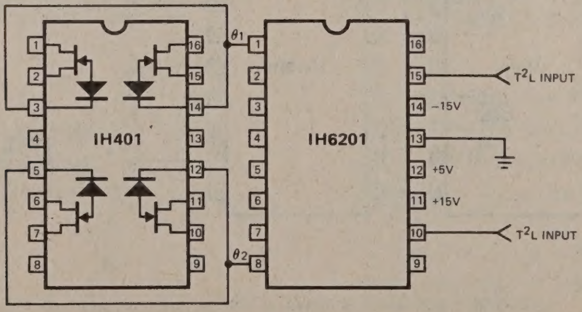
II. DPDT ANALOG SWITCH


IH401
IH6201
θ1
θ̄1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
−15V
+5V
+15V
+3V
0V
T²L1

III. DUAL SPOT


IH401
IH6201
θ1
θ̄1
θ̄2
θ2
−15V
+5V
+15V
T²L INPUT 1
T²L INPUT 2

IV. DUAL DPST


IH401
IH6201
θ1
θ2
T²L INPUT
−15V
+5V
+15V
T²L INPUT

INTERSIL

DG426/A, DG429/A, DG433/A, DG434/A, DG440/A, DG441/A, DG451/A, DG452/A, DG453/A, DG454/A

2-Channel Drivers with SPST and DPST FET Switches

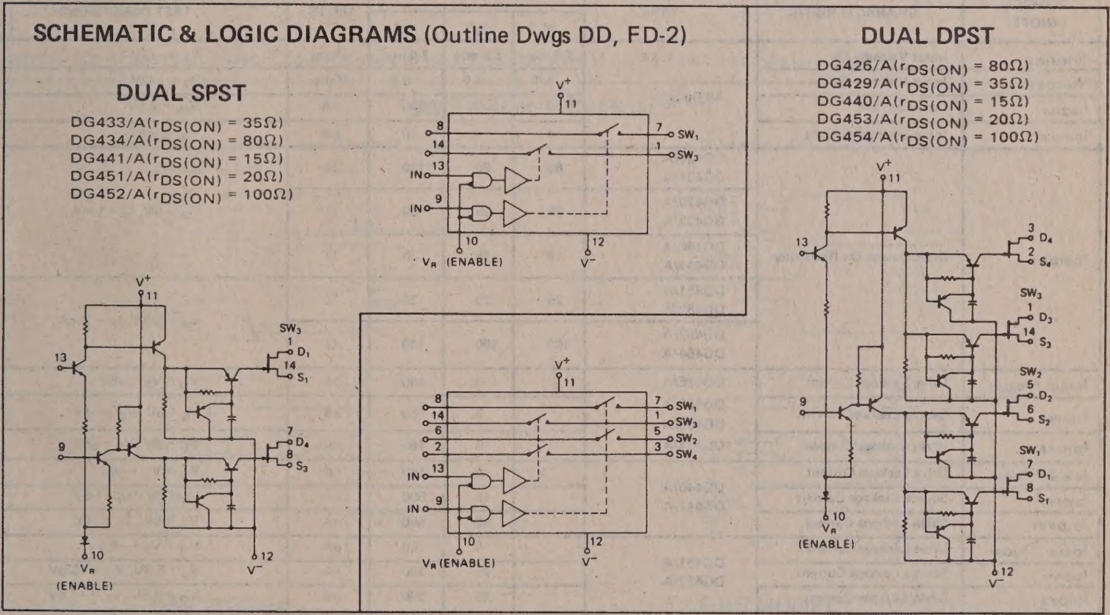
FEATURES

- Each channel complete—interfaces with most integrated logic
- Low OFF power dissipation, — 1mW
- Switches analog signals up to 16 volts peak-to-peak
- Low $r_{DS(ON)}$, 15 ohms max on DG440/A and DG441/A
- Switching times improved 100%—"A" versions

GENERAL DESCRIPTION

These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST or DPST junction FET switch. The driver interfaces DTL, TTL or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF.

SCHEMATIC & LOGIC DIAGRAMS (Outline Dwgs DD, FD-2)



DUAL SPST

DG433/A($r_{DS(ON)} = 35\Omega$)
DG434/A($r_{DS(ON)} = 80\Omega$)
DG441/A($r_{DS(ON)} = 15\Omega$)
DG451/A($r_{DS(ON)} = 20\Omega$)
DG452/A($r_{DS(ON)} = 100\Omega$)

DUAL DPST

DG426/A($r_{DS(ON)} = 80\Omega$)
DG429/A($r_{DS(ON)} = 35\Omega$)
DG440/A($r_{DS(ON)} = 15\Omega$)
DG453/A($r_{DS(ON)} = 20\Omega$)
DG454/A($r_{DS(ON)} = 100\Omega$)

ORDERING INFORMATION

DG426 A C L

- Package
  - L — 14-Pin Flatpak
  - P — 14-Pin Ceramic DIP (Special Order Only)
  - K — 14-Pin CERDIP
- Commercial Temperature Range (0°C to +70°C)
- Option
- Device Type Number

ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V^-$ or $V^+ - V_A$)	28V
Total Supply Voltage ($V^+ - V^-$)	32V
Pos. Supply Voltage to Ref. Voltage ($V^+ - V_R$)	18V
Ref. Voltage to Neg. Supply Voltage ($V_R - V^-$)	21V
Power Dissipation (Note)	750 mW
Current (any terminal)	30 mA
Storage Temperature	−65 to +150°C
Operating Temperature	−65 to +150°C
Lead Temperature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS PER CHANNEL

Applied voltages for all tests: DG426, DG429, DG433, DG434, DG440, DG441, ($V^+ = +12V$, $V^- = -18V$, $V_R = 0$) and DG451, DG452, DG453, DG454 ($V^+ = +15V$, $V^- = -15V$, $V_R = 0$). Input test condition which guarantees FET switch ON and OFF as specified is used for output and power supply specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT			UNITS	TEST CONDITIONS
				0°	25°	70°		
INPUT	$V_{IN(ON)}$	**Input Voltage—On**	All Circuits	2.9 min	2.5 min	2.0 min	Volts	$V_2 = -12V$
	$V_{IN(OFF)}$	**Input Voltage—Off**		1.4	1.0	0.8	Volts	$V_2 = -12V$
	$I_{IN(ON)}$	Input Current		150	100	100	μA	$V_{IN} = 2.5V$
	$I_{IN(OFF)}$	Input Leakage Current		4	4	10	μA	$V_{IN} = 0.8V$
SWITCH OUTPUT	$r_{DS(ON)}$	**Drain-Source On Resistance**	DG426/A DG434/A	80	80	130	Ω	$V_D = 8V, I_S = 1\ mA$
			DG429/A DG433/A	35	35	50	Ω	
			DG440/A DG441/A	15	15	25	Ω	
			DG451/A DG453/A	20	20	30	Ω	$V_D = 5.5V, I_S = 1\ mA$
			DG452/A DG454/A	100	100	140	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG426/A DG429/A DG433/A DG434/A		5	160	nA	$V_D = V_S = -8V$
	$I_{S(OFF)}$	Source Leakage Current			5	160	nA	$V_S = 8V, V_D = -8V$
	$I_{D(OFF)}$	**Drain Leakage Current**			5	160	nA	$V_D = 8V, V_S = -8V$
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG440/A DG441/A		5	160	nA	$V_D = V_S = -8V$
	$I_{S(OFF)}$	Source Leakage Current			15	500	nA	$V_S = 8V, V_D = -8V$
	$I_{D(OFF)}$	**Drain Leakage Current**			15	500	nA	$V_D = 8V, V_S = -8V$
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG451/A DG453/A		5	100	nA	$V_D = V_S = -5.5V$
	$I_{S(OFF)}$	Source Leakage Current			15	300	nA	$V_S = 5.5V, V_D = -5.5V$
	$I_{D(OFF)}$	**Drain Leakage Current**			15	300	nA	$V_D = 5.5V, V_S = -5.5V$
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG452/A DG454/A		5	100	nA	$V_D = V_S = -5.5V$
	$I_{S(OFF)}$	Source Leakage Current			5	100	nA	$V_S = 5.5V, V_D = -5.5V$
	$I_{D(OFF)}$	**Drain Leakage Current**			5	100	nA	$V_D = 5.5V, V_S = -5.5V$
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		3.5		mA	One Driver ON, $V_{IN} = 2.5V$
	$I_{2(ON)}$	Negative Power Supply Drain Current			−2.0		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			−1.5		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	Both Drivers OFF, $V_{IN} = 0.8V$
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			−25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			−25		μA	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

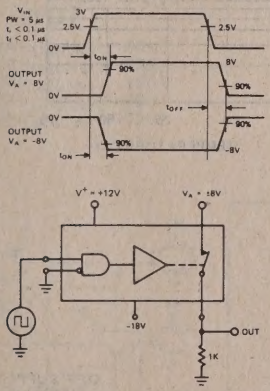
ELECTRICAL CHARACTERISTICS PER CHANNEL (cont.)

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT			UNITS	TEST CONDITIONS
				0°	25°	70°		
SWITCHING	t_{ON}	Turn-On Time	DG426, DG429 DG433, DG434 DG452, DG454		1.0		μs	See Below
			DG426A, DG429A DG433A, DG434A DG452A, DG454A		0.5	0.7	μs	
	t_{OFF}	Turn-Off Time	DG426, DG429 DG433, DG434 DG452, DG454		2.0		μs	See Below
			DG426A, DG429A DG433A, DG434A DG452A, DG454A		1.0	1.3	μs	
	t_{ON}	Turn-On Time	DG440, DG441 DG451, DG453		1.5		μs	See Below
			DG440A, DG441A DG451A, DG453A		.75	1.3	μs	
	t_{OFF}	Turn-Off Time	DG440, DG441 DG451, DG453		2.5		μs	See Below
			DG440A, DG441A DG451A, DG453A		1.25	1.8	μs	
POWER	P_{ON}	ON Drive Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5V
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1.0V

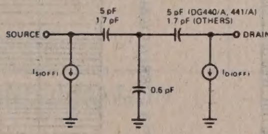
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (at 25°C)

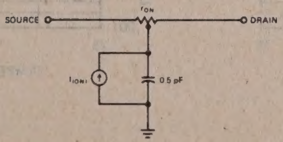
DG426/A, 429/A, 433/A, 434/A, 440/A, 441/A


V_{IN}
PW = 5 μs
t_r < 0.1 μs
t_f < 0.1 μs
3V
2.5V
2.5V
0V
t_{ON}
8V
90%
OUTPUT
V_A = 8V
0V
90%
t_{OFF}
0V
90%
OUTPUT
V_A = -8V
90%
-8V
t_{ON}
V^+ = +12V
V_A = ±8V
-18V
OUT
1K

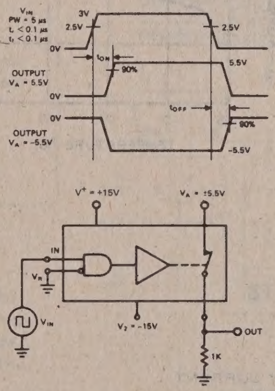
OFF MODEL


5 pF
1.7 pF
5 pF (DG440/A, 441/A)
1.7 pF (OTHERS)
SOURCE
DRAIN
$I_{S(OFF)}$
0.6 pF
$I_{D(OFF)}$

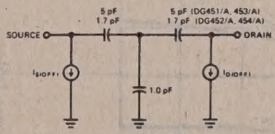
ON MODEL


r_{ON}
SOURCE
DRAIN
$I_{(ON)}$
0.5 pF

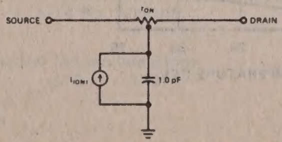
DG451/A, 452/A, 453/A, 454/A


V_{IN}
PW = 5 μs
t_r < 0.1 μs
t_f < 0.1 μs
3V
2.5V
2.5V
0V
t_{ON}
5.5V
90%
OUTPUT
V_A = 5.5V
0V
t_{OFF}
0V
90%
OUTPUT
V_A = -5.5V
-5.5V
V^+ = +15V
V_A = ±5.5V
IN
V_R
V_{IN}
V_2 = -15V
OUT
1K

OFF MODEL


5 pF
1.7 pF
5 pF (DG451/A, 453/A)
1.7 pF (DG452/A, 454/A)
SOURCE
DRAIN
$I_{S(OFF)}$
1.0 pF
$I_{D(OFF)}$

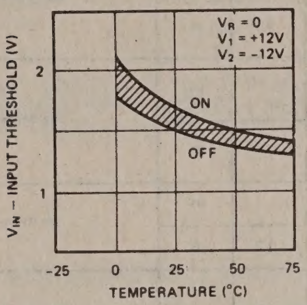
ON MODEL


r_{ON}
SOURCE
DRAIN
$I_{(ON)}$
1.0 pF

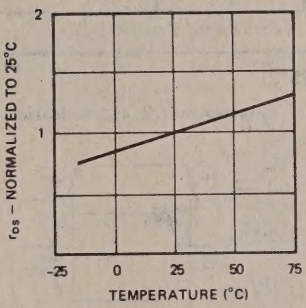
TYPICAL CHARACTERISTICS (per channel)

DG426/A, 429/A, 433/A, 434/A, 440/A, 441/A

V_{IN} THRESHOLD vs TEMPERATURE

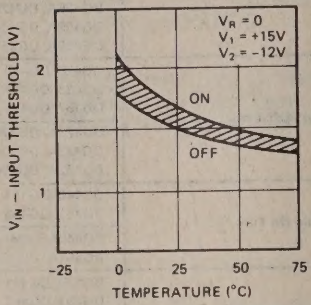


$r_{DS(ON)}$ vs TEMPERATURE (Normalized to 25°C Value)

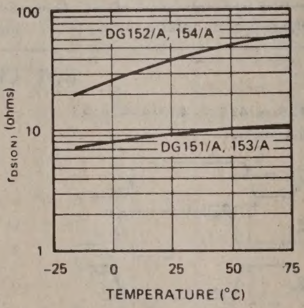


DG451/A, 452/A, 453/A, 454/A

V_{IN} THRESHOLD vs TEMPERATURE

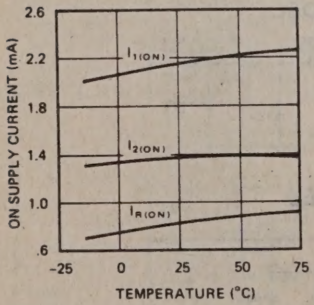


$I_{D(OFF)}$ vs TEMPERATURE

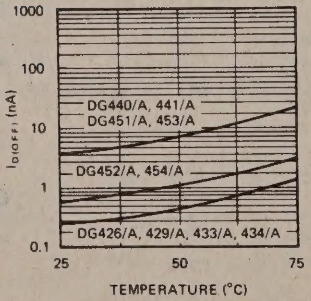


ALL CIRCUITS

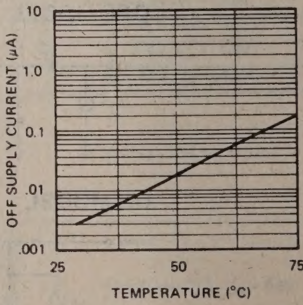
ON SUPPLY CURRENT vs TEMPERATURE



$r_{DS(ON)}$ vs TEMPERATURE



OFF SUPPLY CURRENT vs TEMPERATURE



DG439/A, DG442/A — DG446/A, DG461/A — DG464/A
Drivers with Differentially Driven N.O. and N.C. FET Switches

FEATURES

- Each channel complete—interfaces with most integrated logic
- Low OFF power dissipation,—1mW
- Switches analog signals up to 16 volts peak-to-peak
- Low $r_{DS(ON)}$, 15 ohms max on DG445/A and DG446/A
- Switching times improved 100%—"A" circuits

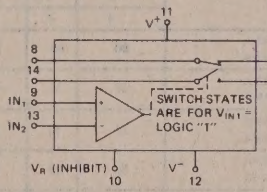
GENERAL DESCRIPTION

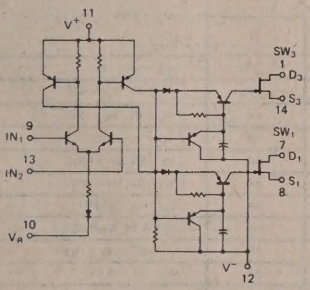
Each package contains a monolithic driver with differential input and 2 or 4 discrete FET switches. The driver may be treated as a special purpose differential amplifier which controls the conduction state of the FET switches. The differential output of the driver sets the switches in opposition, one pair open and the other pair closed. All switches may be opened by applying a positive control signal to the V_R terminal.

SCHEMATIC & LOGIC DIAGRAMS (Outline Dwgs DD, FD-2, JD)

SPDT

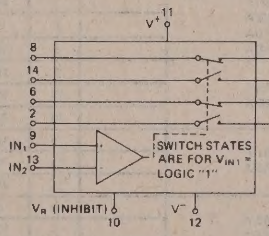
DG443/A($r_{DS(ON)}$ = 80Ω)
DG444/A($r_{DS(ON)}$ = 35Ω)
DG446/A($r_{DS(ON)}$ = 15Ω)
DG461/A($r_{DS(ON)}$ = 20Ω)
DG462/A($r_{DS(ON)}$ = 100Ω)

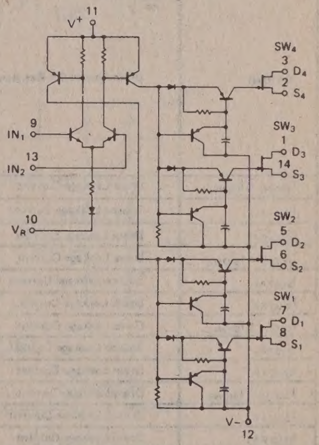

11
V+
8
14
7 SW1
1 SW3
9
IN1
13
IN2
SWITCH STATES ARE FOR VIN1 = LOGIC "1"
VR (INHIBIT)
10
V−
12


11
V+
SW3
1
D3
S3
14
SW1
7
D1
S1
8
9
IN1
13
IN2
10
VR
V−
12

DPDT

DG439/A($r_{DS(ON)}$ = 35Ω)
DG442/A($r_{DS(ON)}$ = 80Ω)
DG445/A($r_{DS(ON)}$ = 15Ω)
DG463/A($r_{DS(ON)}$ = 20Ω)
DG464/A($r_{DS(ON)}$ = 100Ω)


11
V+
8
14
6
2
7 SW1
1 SW3
5 SW2
3 SW4
9
IN1
13
IN2
SWITCH STATES ARE FOR VIN1 = LOGIC "1"
VR (INHIBIT)
10
V−
12


11
V+
SW4
3
D4
2
S4
SW3
1
D3
14
S3
SW2
5
D2
6
S2
SW1
7
D1
8
S1
9
IN1
13
IN2
10
VR
V−
12

ORDERING INFORMATION

DG439 A C L

Package L-14 Pin Flatpak
P-14 Ceramic DIP (Special Order Only)
K-14 Pin CERDIP

Commercial Temperature Range (0°C to +70°C)

Option

Device Type Number

DG439/A Family

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$	32V	$V^+ - V_R$	16V
$V_S - V^-$	28V	$V^+ - V_{IN1}$ or V_{IN2}	14V
$V^+ - V_S$	28V	$V_{IN1} - V_{IN2}$	±5V
$V_S - V_D$	±21V	$V_{IN1} - V_R$	±5V
$V_R - V^-$	20V	$V_{IN2} - V_R$	±5V

Power Dissipation (Note)	750 mW
Current (any terminal)	30 mA
Operating Temperature	-55 to +125°C
Lead Temperature (soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Applied voltages for all tests: DG439/A, DG442/A, DG443/A, DG444/A, DG445/A, DG446/A, ($V^+ = 12V$, $V^- = -18V$, $V_R = 0$, $V_{IN2} = 2.5V$) and DG461A, DG462/A, DG463/A, DG464/A ($V^+ = 15V$, $V^- = -15V$, $V_R = 0$, $V_{IN2} = 2.5V$). Input test condition that guarantees FET switch ON or OFF as specified is used for output specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT			UNITS	TEST CONDITIONS
				-55°	25°	125°		
INPUT	$V_{IN(ON)}$	Input Voltage—On	All Circuits	2.9 min	2.5 min	2.0 min	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$V_{IN(OFF)}$	Input Voltage—Off		1.4	1.0	0.8	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$\lvert V_9 - V_{13}\rvert$	Differential Voltage		0.5 min	0.5 min	0.5 min	Volts	See Note 1, Pg. 4
	$I_{IN1(ON)}$	Input Current		150	100	100	μA	V_{IN1} 3.0V
	$I_{IN2(ON)}$			150	100	100	μA	V_{IN2} = 2.0V
	$I_{IN1(OFF)}$	Input Leakage Current		4	4	10	μA	V_{IN1} = 2.0V
	$I_{IN2(OFF)}$			4	4	10	μA	V_{IN2} = 3.0V
SWITCH OUTPUT	$r_{DS(ON)}$	Drain-Source On Resistance	DG442/A DG443/A	80	80	130	Ω	$V_D = 10V$, $I_S = 1$ mA
			DG439/A DG444/A	35	35	50	Ω	
			DG445/A DG446/A	15	15	25	Ω	
			DG461/A DG463/A	20	20	30	Ω	$V_D = 7.5V$, $I_S = 1$ mA
			DG462/A DG464/A	100	100	140	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG439/A DG442/A DG443/A DG444/A		5	160	nA	$V_D = V_S = -8V$
	$I_{S(OFF)}$	Source Leakage Current			5	160	nA	$V_S = 8V$, $V_D = -8V$
	$I_{D(OFF)}$	Drain Leakage Current			5	160	nA	$V_D = 8V$, $V_S = -8V$
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG445/A DG446/A		5	160	nA	$V_D = V_S = -8V$
	$I_{S(OFF)}$	Source Leakage Current			15	500	nA	$V_S = 8V$, $V_D = -8V$
	$I_{D(OFF)}$	Drain Leakage Current			15	500	nA	$V_D = 8V$, $V_S = -8V$
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG461/A DG463/A		5	100	nA	$V_D = V_S = -5.5V$
	$I_{S(OFF)}$	Source Leakage Current			15	300	nA	$V_S = 5.5V$, $V_D = -5.5V$
	$I_{D(OFF)}$	Drain Leakage Current			15	300	nA	$V_D = 5.5V$, $V_S = -5.5V$
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG462/A DG464/A		5	100	nA	$V_D = V_S = -5.5V$
	$I_{S(OFF)}$	Source Leakage Current			5	100	nA	$V_D = 5.5V$, $V_S = -5.5V$
	$I_{D(OFF)}$	Drain Leakage Current			5	100	nA	$V_D = 5.5V$, $V_S = -5.5V$
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		3.5		mA	$V_{IN1} = 3V$ or $V_{IN1} = 2V$
	$I_{2(ON)}$	Negative Power Supply Drain Current			-2.0		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			-1.5		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	$V_{IN1} = V_{IN2} = 0.8V$
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			-25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			-25		μA	

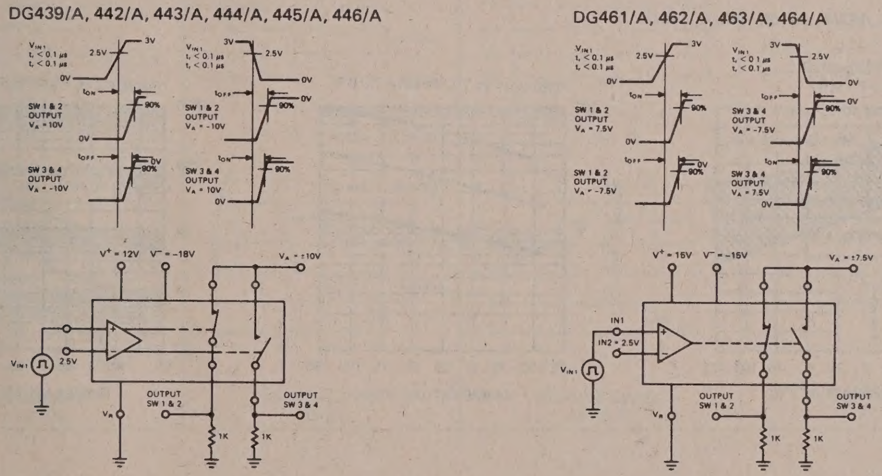
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

ELECTRICAL CHARACTERISTICS PER CHANNEL (cont.)

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT			UNITS	TEST CONDITIONS
				-55°C	25°	125°		
SWITCHING	t_{ON}	Turn-On Time	DG439, DG442 DG443, DG444 DG462, DG464		1.0		µs	See Below
			DG439A, DG442A DG443A, DG444A DG462A, DG464A		0.5	0.7	µs	
	t_{OFF}	Turn-Off Time	DG439, DG442 DG443, DG444 DG462, DG464		2.0		µs	See Below
			DG439A, DG442A DG443A, DG444A DG462A, DG464A		1.0	1.3	µs	
	t_{ON}	Turn-On Time	DG445, DG446 DG461, DG463		1.5		µs	See Below
			DG445A, DG446A DG461A, DG463A		.75	1.3	µs	
	t_{OFF}	Turn-Off Time	DG445, DG446 DG461, DG463		2.5		µs	See Below
			DG445A, DG446A DG461A, DG463A		1.25	1.8	µs	
POWER	P_{ON}	ON Driver Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5V
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1.0V

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

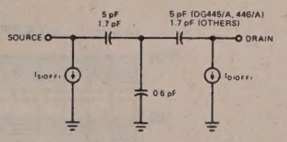
SWITCHING TIMES (25°C)


DG439/A, 442/A, 443/A, 444/A, 445/A, 446/A

DG461/A, 462/A, 463/A, 464/A

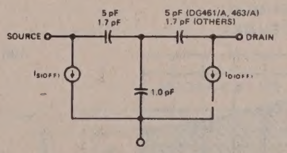
V_{IN1}
t_r < 0.1 µs
t_f < 0.1 µs
3V
2.5V
0V
t_{ON}
t_{OFF}
90%
SW 1 & 2 OUTPUT V_A = 10V
SW 1 & 2 OUTPUT V_A = -10V
SW 3 & 4 OUTPUT V_A = -10V
SW 3 & 4 OUTPUT V_A = 10V
SW 1 & 2 OUTPUT V_A = 7.5V
SW 1 & 2 OUTPUT V_A = -7.5V
SW 3 & 4 OUTPUT V_A = -7.5V
SW 3 & 4 OUTPUT V_A = 7.5V
V^+ = 12V V^- = -18V
V_A = ±10V
V^+ = 15V V^- = -15V
V_A = ±7.5V
IN1
IN2 = 2.5V
V_A
OUTPUT SW 1 & 2
OUTPUT SW 3 & 4
1K

OFF MODEL



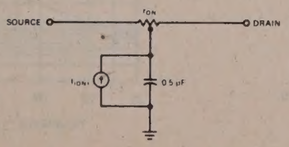
5 pF
1.7 pF
5 pF (DG445/A, 446/A)
1.7 pF (OTHERS)
SOURCE
DRAIN
$I_{S(OFF)}$
$I_{D(OFF)}$
0.6 pF

OFF MODEL



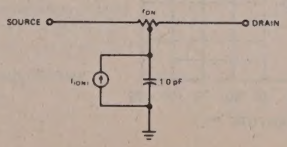
5 pF
1.7 pF
5 pF (DG461/A, 463/A)
1.7 pF (OTHERS)
SOURCE
DRAIN
$I_{S(OFF)}$
$I_{D(OFF)}$
1.0 pF

ON MODEL



r_{ON}
SOURCE
DRAIN
$I_{(ON)}$
0.5 pF

ON MODEL



r_{ON}
SOURCE
DRAIN
$I_{(ON)}$
1.0 pF

FIGURE 1

ABSOLUTE VOLTAGE LEVELS FOR SWITCHING WITHONE SIDE OPEN AND OTHER SIDE SWITCHED AT 25°C

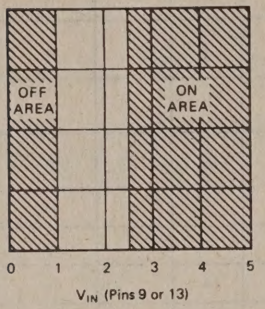
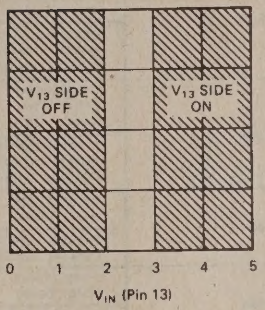


FIGURE 2

VOLTAGE AT PIN 13 NECESSARY TO SWITCH WHEN BIAS AT PIN 9 IS +2.5V AT 25°C

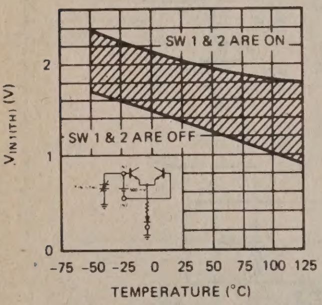


NOTE1: An example of Absolute Minimum Differential Voltage, $|V_9 - V_{13}|$, is when $V_9 = 3V$ and $V_{13} = 2.5V$, the V_9 side of the switch is ON and the V_{13} side of the switch is OFF at 25°C. Conversely, when $V_9 = 2V$ and $V_{13} = 2.5V$, the V_9 side of the switch is OFF and the V_{13} side of the switch is ON at 25°C.

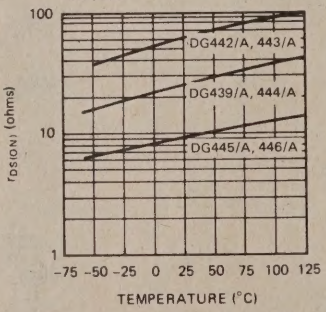
TYPICAL CHARACTERISTICS (per channel)

DG439/A, 442/A, 443/A, 444/A, 445/A, 446/A

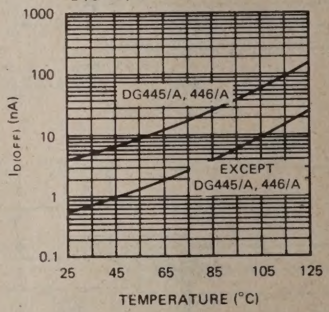
V_{IN1} THRESHOLD vs TEMPERATURE



$r_{DS(ON)}$ vs TEMPERATURE

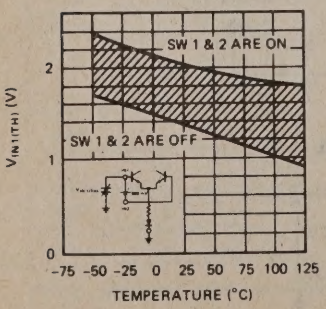


$I_{D(OFF)}$ vs TEMPERATURE

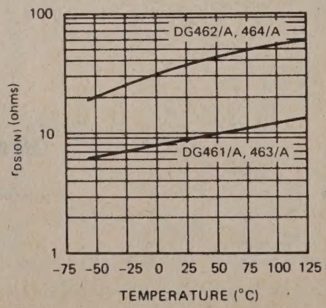


DG461/A, 462/A, 463/A, 464/A

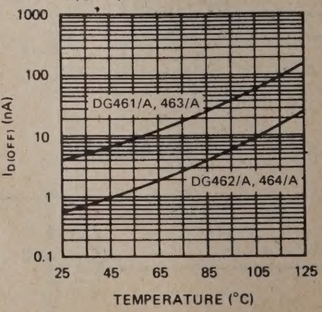
V_{IN1} THRESHOLD vs TEMPERATURE



$R_{DS(ON)}$ vs TEMPERATURE



$I_{S(OFF)}$ vs TEMPERATURE



INTERSIL

MM450/MM550, MM451/MM551
MM452/MM552, MM455/MM555
MOS-FET Switches

FEATURES

- Large Analog Input – ±10V
- Low Supply Voltage – V_{BULK} = +10V
  V_{GG} = –20V
- Typical ON Resistance – V_{IN} = –10V, 150Ω
  V_{IN} = +10V, 75Ω
- Low Leakage Current – 200 pA @ 25°C
- Input Gate Protection

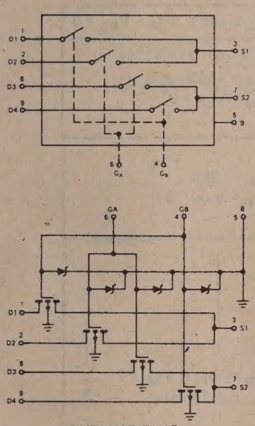
GENERAL DESCRIPTION

The MM450, and MM550 series each contain p channel MOS enhancement mode transistors. These devices are useful in airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors (V_{TH} = 2 volts) permits operations with large analog input swings (±10 volts) at low gate voltages (–20 volts).

Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk.

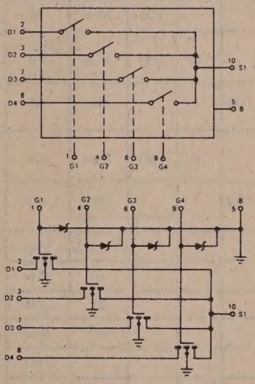
CONNECTION DIAGRAMS

MM450, MM550 Dual Differential Switch



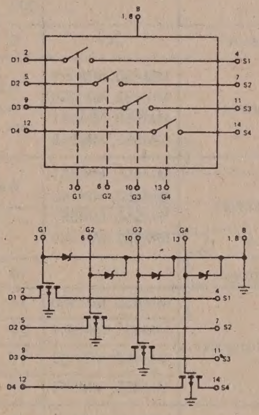
OUTLINE DWG
TO-100

MM451, MM551 Four Channel Switch



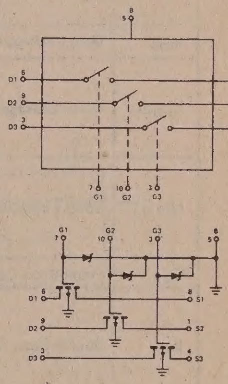
OUTLINE DWG
TO-100

MM452, MM552 Four MOS Transistor Package



OUTLINE DWGS
JE,FD-2

MM455, MM555 Three MOS Transistor Package



OUTLINE DWG
TO-100

ORDERING INFORMATION

MM 4 50 F

Package F – 14 Pin Flatpak
J – 16 Pin CERDIP
H – 10 Pin Metal Can

Device Type

Temperature Range
4 – (–55°C to +125°C)
5 – (0°C to 70°C)

Analog Switch

ABSOLUTE MAXIMUM RATINGS (Note 1)

Gate Voltage (V_{GG})	+14.5V to −30V
Bulk Voltage (V_{BULK})	+14V
Analog Input (V_{IN})	+14V to −20V
Power Dissipation	200 mW
Operating Temperature	
MM450, MM451, MM452, MM455	−55°C to +125°C
MM550, MM551, MM552, MM555	0°C to 70°C
Storage Temperature	−65°C to +150°C
Lead Tempertature (soldering, 10 sec.)	300°C

NOTE 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C for FD package and 6.5 mW/°C for TW package.

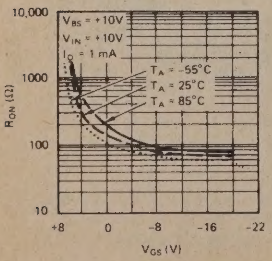
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel unless noted)

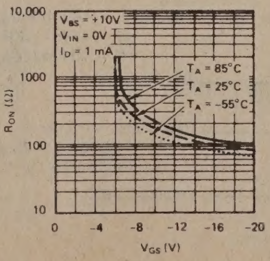
SYMBOL	CHARACTERISTICS	TYPE	LIMITS						CONDITIONS	
			25°	70°	85°	125°	MIN MAX	UNITS		
V_{IN}	Analog Input Voltage	All	±10				Max	V		
$V_{GS(Th)}$	Threshold Voltage	All	1.5				Min	V	V_{DG} = 0	
			3.0				Max		I_D = 10 μA	
$r_{DS(ON)}$	Drain-Source On Resistance	All	600		600		Max	Ω	V_{IN} = −10V	I_D = 1 mA V_B = 10V V_{GS} = −20V
			200		200		Max	Ω	V_{IN} = +10V	
I_{GBS}	Gate Leakage Current	All	5			100	Max	nA	V_{GS} = −25V, V_{BS} = V_{DS} = 0	
$I_{D(OFF)}$	Drain Leakage Current	MM450, MM451 MM452, MM455	0.2		40	200	Max	nA	V_{DB} = −25V V_{GB} = V_{SB} = 0	
		MM550, MM551 MM552, MM555	20	100			Max	nA		
$I_{S(OFF)}$	Source Leakage Current	MM450, MM451 MM452, MM455	0.4		40	400	Max	nA	V_{SB} = −25V V_{DB} = V_{GB} = 0	
		MM550, MM551 MM552, MM555		100			Max	nA		
C_{DB}	Drain-Body Capacitance	All	10				pF	Max	V_{DB} = V_{GB} = V_{SB} = 0 f = 1 MHz	
C_{SB}	Source-Body Capacitance	MM450, MM550	14				pF	Max		
		MM451, MM551	24				pF	Max		
		MM452, MM552	11				pF	Max		
		MM455, MM555	11				pF	Max		
C_{GB}	Gate-Body Capacitance	MM450, MM550	13				pF	Max		
		MM451, MM551	8				pF	Max		
		MM452, MM552	9				pF	Max		
		MM455, MM555	9				pF	Max		
C_{GS}	Gate-Source Capacitance	All	5				pF	Max		

TYPICAL PERFORMANCE CURVES

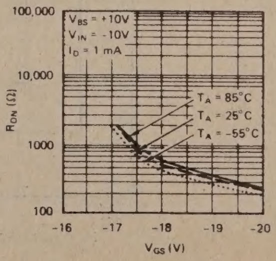
$r_{DS(on)}$ vs V_{GS}



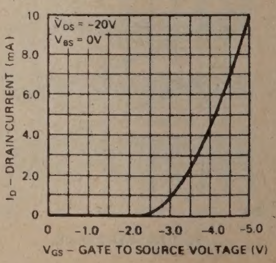
$r_{DS(on)}$ vs V_{GS}



$r_{DS(on)}$ vs V_{GS}



DRAIN CURRENT vs GATE TO SOURCE VOLTAGE



INTERSIL

IH5001/IH5002
1-Channel Driver with SPST FET Switch AND Gate Available

FEATURES

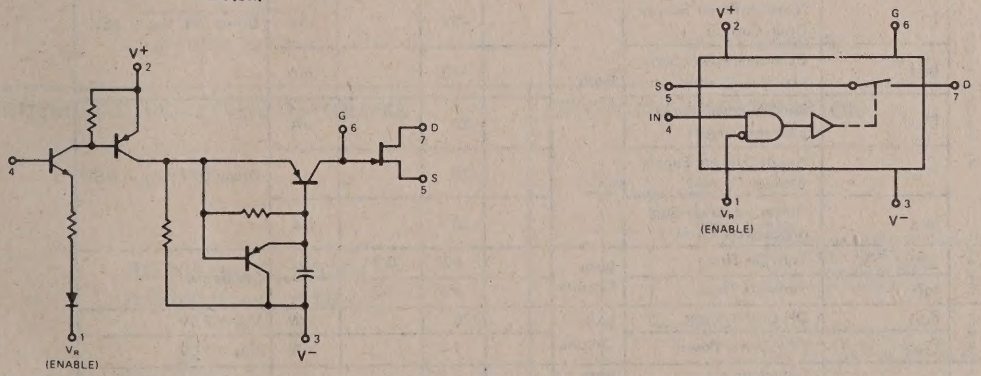
- Gate Lead Available for Nulling Charge Injection Voltage
- Channel Complete—Interfaces With Most Integrated Logic
- Low OFF Power Dissipation, −1 mW
- Low $r_{DS(on)}$, 30Ω Max on IH5001
- Switches Analog Signals up to 16 Volts Peak-to-Peak

GENERAL DESCRIPTION

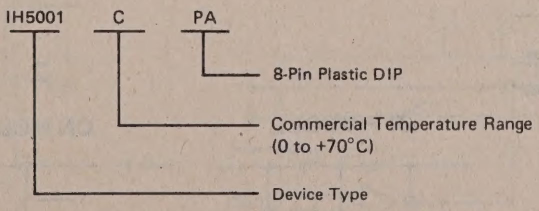
These switching circuits contain one channel in one package, the channel consisting of a driver circuit controlling a SPST junction FET switch. The driver interfaces DTL, TTL, or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF. The gate lead of the FET has been brought out to enable the application of a referral resistor for nulling offset voltage due to charge injection.

SCHEMATIC & LOGIC DIAGRAM (Outline Dwg PA)

IH5001 ($r_{DS(on)}$ = 30Ω)
IH5002 ($r_{DS(on)}$ = 50Ω)


V+
2
4
G
6
D
7
S
5
1
V_R
(ENABLE)
3
V−
V+
2
G
6
S
5
IN
4
D
7
1
V_R
(ENABLE)
3
V−

ORDERING INFORMATION


IH5001
C
PA
8-Pin Plastic DIP
Commercial Temperature Range
(0 to +70°C)
Device Type

ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V^-$ or $V^\pm V_A$)	28V
Total Supply Voltage ($V^+ - V^-$)	32V
Pos. Supply Voltage to Ref. Voltage ($V^+ - V_R$)	18V
Ref. Voltage to Neg. Supply Voltage ($V_R - V^-$)	21V
Power Dissipation (Note)	500mW
Current (Any Terminal)	30mA
Storage Temperature	−65 to +150°C
Operating Temperature	0 to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

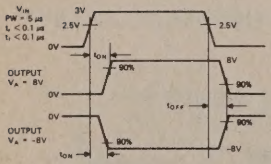
ELECTRICAL CHARACTERISTICS

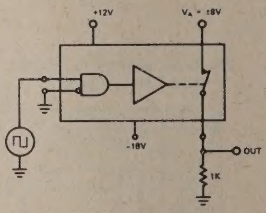
Applied voltages for all tests: V+ = +12V, V− = −18V. Input test condition which guarantees FET switch ON or OFF as specified is used for output and power supply specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX LIMIT			UNITS	TEST CONDITIONS
				0°	25°	70°		
INPUT	$V_{IN(ON)}$	**Input Voltage-ON**	Both Circuits	2.9 min	2.5 min	2.0 min	Volts	$V^- = -12V$
	$V_{IN(OFF)}$	**Input Voltage-OFF**		1.4	1.0	0.8	Volts	$V^- = -12V$
	$I_{IN(ON)}$	Input Current		150	100	100	μA	$V_{IN} = 2.5V$
	$I_{IN(OFF)}$	Input Leakage Current		4	4	10	μA	$V_{IN} = 0.8V$
SWITCHING OUTPUT	$V_{DS(ON)}$	**Drain-Source ON Resistance**	IH5001	30	30	50	Ω	$V_D = 8V, I_S = 1\ mA$
			IH5002	50	50	85	Ω	
	$I_{D(ON)}+I_{S(ON)}$	Drive Leakage Current	Both Circuits		5	160	nA	$V_D = V_S = -8V$
	$I_{S(OFF)}$	Source Leakage Current			5	160	nA	$V_S = 8V, V_D = -8V$
	$I_{D(OFF)}$	**Drain Leakage Current**			5	160	nA	$V_D = 8V, V_S = -8V$
POWER SUPPLY	$I+$	Positive Power Supply Drain Current	Both Circuits		3.5		mA	Driver ON, $V_{IN} = 2.5V$
	$I-$	Negative Power Supply Drain Current			−2.0		mA	
	I_{REF}	Reference Power Supply Drain Current			−1.5		mA	
	I^+_{LK}	Positive Power Supply Leakage Current			25		μA	Driver OFF, $V_{IN} = 0.8V$
	I^-_{LK}	Negative Power Supply Leakage Current			−25		μA	
	I_{RLK}	Reference Power Supply Leakage Current			−25		μA	
SWITCH	t_{on}	**Turn-On Time**	Both Circuits		0.5	0.7	μs	See Below
	t_{off}	**Turn-Off Time**			1.0	1.3	μs	
POWER	P_{ON}	ON Driver Power	Both Circuits		175		mW	$V_{IN} = 2.5V$
	P_{OFF}	OFF Driver Power			1		mW	$V_{IN} = 1.0V$
FET	VGSSF	Gate Source Forward Voltage	Both Circuits		1.5		Volts	$I_G = 1.0\ mA, V_{DS} = 0$

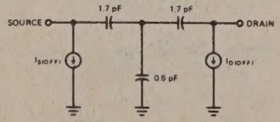
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (at 25°C)

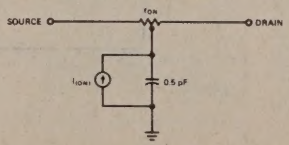




OFF MODEL



ON MODEL



INTERSIL

IH5003/IH5004
2-Channel Drivers with SPST FET Switches AND Gate Available

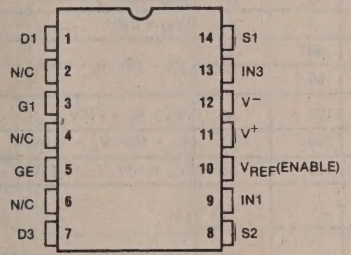
FEATURES

- Gate Lead Available for Nulling Charge Injection Voltage
- Each Channel Complete—Interfaces With Most Integrated Logic
- Low OFF Power Dissipation, −1 mW
- Switches Analog Signals up to 20 Volts Peak-to-Peak
- Low $r_{DS(ON)}$, 30Ω Max on IH5003

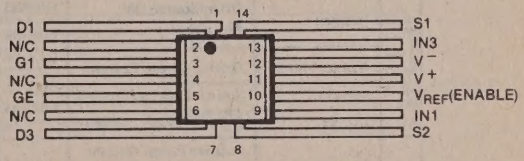
GENERAL DESCRIPTION

These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST junction FET switch. The driver interfaces DTL, TTL, or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF. The gate lead of the FETs has been brought out to enable the application of a referral resistor for nulling out offset voltage due to charge injection.

PIN CONFIGURATIONS


D1 1
N/C 2
G1 3
N/C 4
GE 5
N/C 6
D3 7
14 S1
13 IN3
12 V−
11 V+
10 VREF(ENABLE)
9 IN1
8 S2

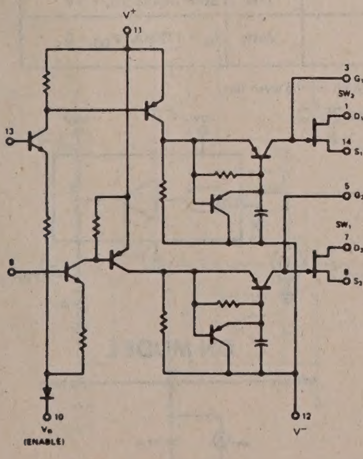
OUTLINE DWGS JD, DD, PD


1 14
D1
N/C
G1
N/C
GE
N/C
D3
2 13
3 12
4 11
5 10
6 9
7 8
S1
IN3
V−
V+
VREF(ENABLE)
IN1
S2

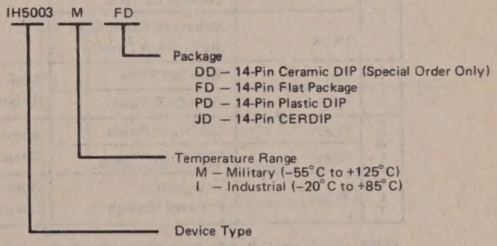
OUTLINE DWG FD-2

SCHEMATIC AND LOGIC DIAGRAMS

IH5003 ($r_{DS(on)}$ = 30Ω)
IH5004 ($r_{DS(on)}$ = 50Ω)


V+
11
13
3 G1
SW3
1 D1
14 S1
5 G3
SW1
7 D3
8 S3
8
10
VR
(ENABLE)
12
V−

ORDERING INFORMATION

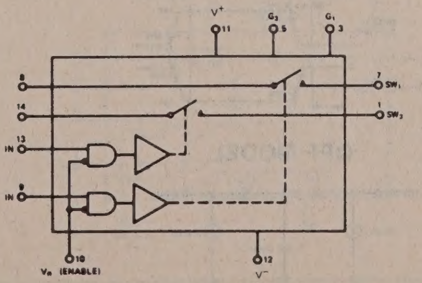

IH5003 M FD

Package
DD — 14-Pin Ceramic DIP (Special Order Only)
FD — 14-Pin Flat Package
PD — 14-Pin Plastic DIP
JD — 14-Pin CERDIP

Temperature Range
M — Military (−55°C to +125°C)
I — Industrial (−20°C to +85°C)

Device Type

NOTE: Military temperature range not available in plastic package.


V+
11
G3
5
G1
3
8
7 SW1
14
1 SW3
13
IN
8
IN
10
VR (ENABLE)
12
V−

ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V^-$ or $V^+ - V_A$)	30V
Total Supply Voltage ($V^+ - V^-$)	36V
Pos. Supply Voltage to Ref. Voltage ($V^+ - V_R$)	25V
Ref. Voltage to Neg. Supply Voltage ($V_R - V^-$)	22V
Power Dissipation (Note)	750 mW
Current (Any Terminal)	30 mA
Storage Temperature	−65 to +150°C
Operating Temperature	−55 to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

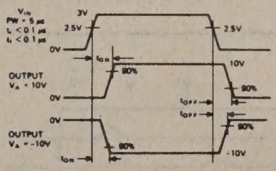
ELECTRICAL CHARACTERISTICS

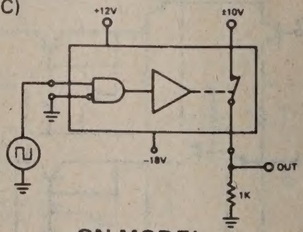
Applied Voltages for all tests: $V^+ = +12V$, $V^- = -18V$, GND = 0. Input test condition which guarantees FET switch ON or OFF as specified is used for output and power supply specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX LIMIT			UNITS	TEST CONDITIONS
				-55°	25°	125°		
INPUT	$V_{IN(ON)}$	**Input Voltage-ON**	Both Circuits	**2.9 min**	**2.5 min**	**2.0 min**	Volts	$V^- = -12V$
	$V_{IN(OFF)}$	**Input Voltage-OFF**		**1.4**	**1.0**	**0.6**	Volts	$V^- = -12V$
	$I_{IN(ON)}$	Input Current		120	60	60	μA	$V_{IN} = 2.5V$
	$I_{IN(OFF)}$	Input Leakage Current		0.1	0.1	2	μA	$V_{IN} = 0.8V$
SWITCHING OUTPUT	$r_{DS(ON)}$	**Drain-Source ON Resistance**	IH5003	**30**	**30**	**50**	Ω	$V_D = 10V$, $I_S = 1$ mA
			IH5004	**50**	**50**	**85**	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	Both Circuits		2	100	nA	$V_D = V_S = -10V$
	$I_{S(OFF)}$	Source Leakage Current			1	100	nA	$V_S = 10V$, $V_D = -10V$
	$I_{D(OFF)}$	Drain Leakage Current			1	100	nA	$V_D = 10V$, $V_S = -10V$
POWER SUPPLY	I^+	Positive Power Supply Drain Current	Both Circuits		3		mA	One Driver ON, $V_{IN} = 2.5V$
	I^-	Negative Power Supply Drain Current			−1.8		mA	
	I_{REF}	Reference Power Supply Drain Current			−1.4		mA	
	I^+_{LK}	Positive Power Supply Leakage Current			25		μA	Both Drivers OFF $V_{IN} = 0.8V$
	I^-_{LK}	Negative Power Supply Leakage Current			−25		μA	
	I_{RLK}	Reference Power Supply Leakage Current			−25		μA	
SWITCH	t_{on}	**Turn-ON Time**	Both Circuits		**0.3**	**0.5**	μs	See Below
	t_{off}	**Turn-OFF Time**			**0.8**	**1.2**	μs	
POWER	P_{ON}	ON Driver Power	Both Circuits		175		mW	Both Inputs $V_{IN} = 2.5$
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs $V_{IN} = 1V$
FET	$V_{GS(f)}$	Gate Source Forward Voltage	Both Circuits		1.5		Volts	$I_G = 1.0$ mA, $V_{DS} = 0$

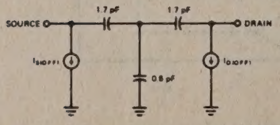
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (at 25°C)

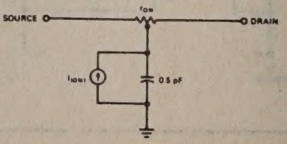




OFF MODEL



ON MODEL



IH5005 — IH5007
2-Channel Drivers with SPST FET Switches Gate Available AND

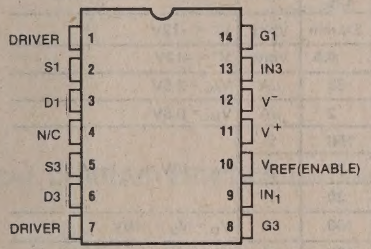
FEATURES

- Gate Lead Available for Nulling Charge Injection Voltage
- Expansion Capability Available
- Each Channel Complete—Interfaces With Most Integrated Logic
- Low OFF power dissipation, 1 mW
- Low $r_{DS(ON)}$, 10Ω Max on IH5005

GENERAL DESCRIPTION

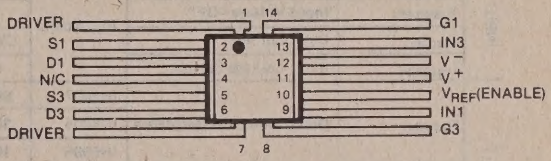
These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST junction FET switch. The driver interfaces DTL, TTL, or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and Logic "0" turns it OFF. The gate lead of the FETs has been brought out to enable the application of a referral resistor for nulling offset voltage due to charge injection. Driver points are brought out to provide for the addition of external FETs for expansion capability.

PIN CONFIGURATIONS



DRIVER 1
S1 2
D1 3
N/C 4
S3 5
D3 6
DRIVER 7
14 G1
13 IN3
12 V⁻
11 V⁺
10 VREF(ENABLE)
9 IN1
8 G3

OUTLINE DWG
DD, PD, JD

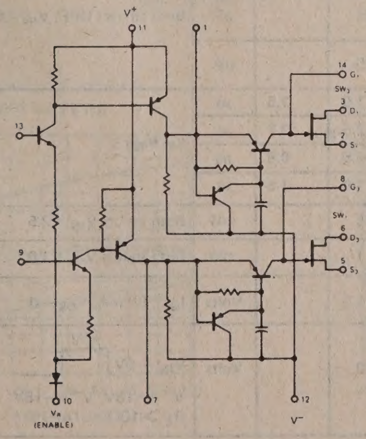


DRIVER
S1
D1
N/C
S3
D3
DRIVER
1
14
2
3
4
5
6
13
12
11
10
9
7
8
G1
IN3
V⁻
V⁺
VREF(ENABLE)
IN1
G3

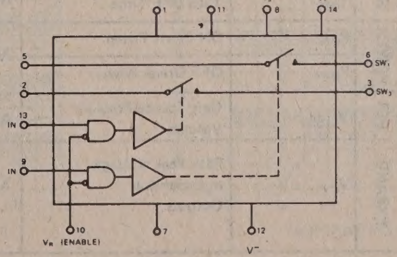
OUTLINE DWG
FD-2

SCHEMATIC AND LOGIC DIAGRAMS

IH5005 ($r_{DS(on)}$ = 10Ω)
IH5006 ($r_{DS(on)}$ = 30Ω)
IH5007 ($r_{DS(on)}$ = 80Ω)



V⁺
11
1
13
14
G₁
SW₁
3
D₁
2
S₁
8
G₃
SW₃
6
D₃
5
S₃
9
10
7
12
V_R
(ENABLE)
V⁻



V⁺
G₃
G₁
1
11
8
14
5
2
13
IN
9
IN
6
SW₁
3
SW₃
10
7
12
V_R (ENABLE)
V⁻

ORDERING INFORMATION

IH5005 M FD

Package
DD – 14-Pin Ceramic DIP (Special Order Only)
FD – 14-Pin Flat Pack
PD – 14-Pin Plastic
JD – 14-Pin CERDIP

Temperature Range
M = Military (−55°C to +125°C)
I = Industrial (−20°C to +85°C)
C = Commercial (0°C to +70°C)

Device Type

NOTE: Military temperature range not available in plastic package.

ABSOLUTE MAXIMUM RATINGS

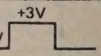
Analog Signal Voltage ($V_A - V^-$ or $V^+ - V_A$)	30V
Total Supply Voltage ($V^+ - V^-$)	36V
Pos. Supply Voltage to Ref. Voltage ($V^+ - V_R$)	25V
Ref. Voltage to Neg. Supply Voltage ($V_R - V^-$)	22V
Power Dissipation (Note)	750 mW
Current (Any Terminal)	30 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−65°C to +125°C
Lead Temperature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

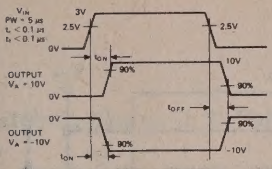
ELECTRICAL CHARACTERISTICS

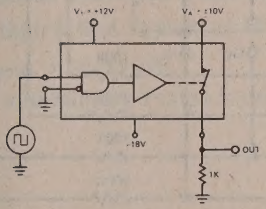
Applied Voltages for all tests $V^+ = +12V$, $V^- = -18V$, $V_R = 0$. Input test condition which guarantees FET switch ON or OFF as specified is used for output and power supply specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT			UNITS	TEST CONDITIONS
				−55°	25°	125°		
INPUT	$V_{IN(ON)}$	**Input Voltage—ON**	All Circuits	2.9 min	2.5 min	2.0 min	Volts	$V^- = -12V$
	$V_{IN(OFF)}$	**Input Voltage—OFF**		1.4	1.0	0.6	Volts	$V^- = -12V$
	$I_{IN(ON)}$	Input Current		120	60	60	μA	$V_{IN} = 2.5V$
	$I_{IN(OFF)}$	Input Leakage Current		0.1	0.1	2	μA	$V_{IN} = 0.8V$
SWITCH OUTPUT	$r_{DS(ON)}$	**Drain-Source On Resistance**	IH5007	80	80	150	Ω	$V_D = 10V$, $I_S = 1$ mA
			IH5006	30	30	50	Ω	
			IH5005	10	10	20	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	IH5006 IH5007		2	100	nA	$V_D = V_S = -10V$
	$I_{S(OFF)}$	Source Leakage Current			1	100	nA	$V_S = 10V$, $V_D = -10V$
	$I_{D(OFF)}$	**Drain Leakage Current**			1	100	nA	$V_D = 10V$, $V_S = -10V$
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	IH5005		2	100	nA	$V_D = V_S = -10V$
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	$V_S = 10V$, $V_D = -10V$
	$I_{D(OFF)}$	**Drain Leakage Current**			10	1000	nA	$V_D = 10V$, $V_S = -10V$
POWER SUPPLY	I^+	Positive Power Supply Drain Current	All Circuits		3		mA	One Driver ON, $V_{IN} = 2.5V$
	I^-	Negative Power Supply Drain Current			−1.8		mA	
	I_{REF}	Reference Power Supply Drain Current			−1.4		mA	
	I^+_{LK}	Positive Power Supply Leakage Current			25		μA	Both Drivers OFF, $V_{IN} = 0.8V$
	I^-_{LK}	Negative Power Supply Leakage Current			−25		μA	
	I_{RLK}	Reference Power Supply Leakage Current			−25		μA	
SWITCHING	t_{on}	**Turn-ON Time**	IH5005		1.0	1.5	μs	See Page 3
	t_{off}	**Turn-OFF Time**			2.5	3.7	μs	
	t_{on}	**Turn-ON Time**	IH5006 IH5007		0.5	0.8	μs	
	t_{off}	**Turn-OFF Time**			1.0	1.5	μs	
POWER	P_{ON}	ON Driver Power	All Circuits		175		mW	Both Inputs $V_{IN} = 2.5$
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs $V_{IN} = 1.0$
FET	V_{GSSF}	Gate Source Forward Voltage	All Circuits		1.5		Volts	$I_G = 1.0$ mA, $V_{DS} = 0$
EXPAND	$V_{P\text{-}P}$	Peak-Peak Voltage at Expansion Outputs	All Circuits		30		Volts	$V_{IN} = 0V$  $V^+ = +18V$, $V^- = -18V$, $R_L \geq 10\Omega$

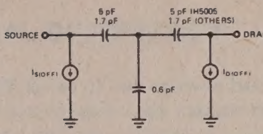
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (at 25°C)

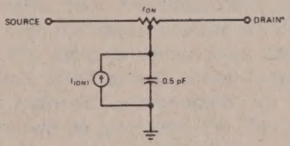

V_IN
PW = 5 μs
t_r < 0.1 μs
t_f < 0.1 μs
3V
2.5V
2.5V
0V
t_ON
90%
10V
OUTPUT
V_A = 10V
0V
90%
t_OFF
0V
90%
OUTPUT
V_A = -10V
90%
-10V
t_ON


V+ = +12V
V_A = ±10V
-18V
OUT
1K

OFF MODEL

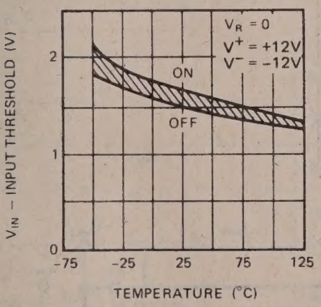

6 pF
1.7 pF
5 pF IH5005
1.7 pF (OTHERS)
SOURCE
DRAIN
I_S(OFF)
0.6 pF
I_D(OFF)

ON MODEL

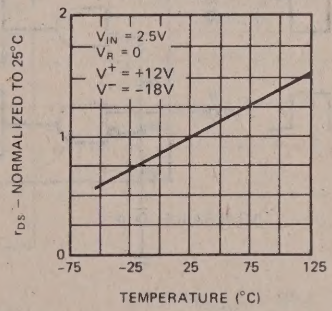

r_ON
SOURCE
DRAIN*
I_(ON)
0.5 pF

TYPICAL CHARACTERISTICS (per channel)

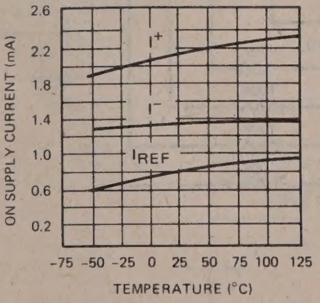
V_{IN} THRESHOLD vs TEMPERATURE



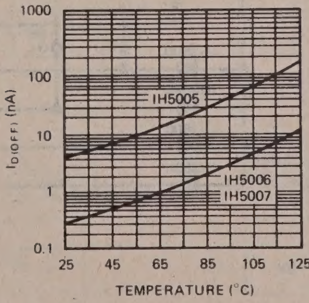
$r_{DS(ON)}$ vs TEMPERATURE (Normalized to 25°C Value)



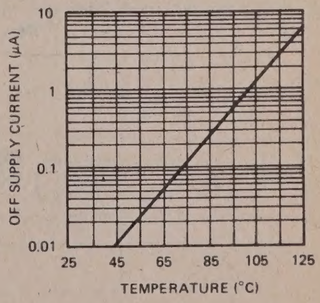
ON SUPPLY CURRENT vs TEMPERATURE



$I_{D(OFF)}$ vs TEMPERATURE

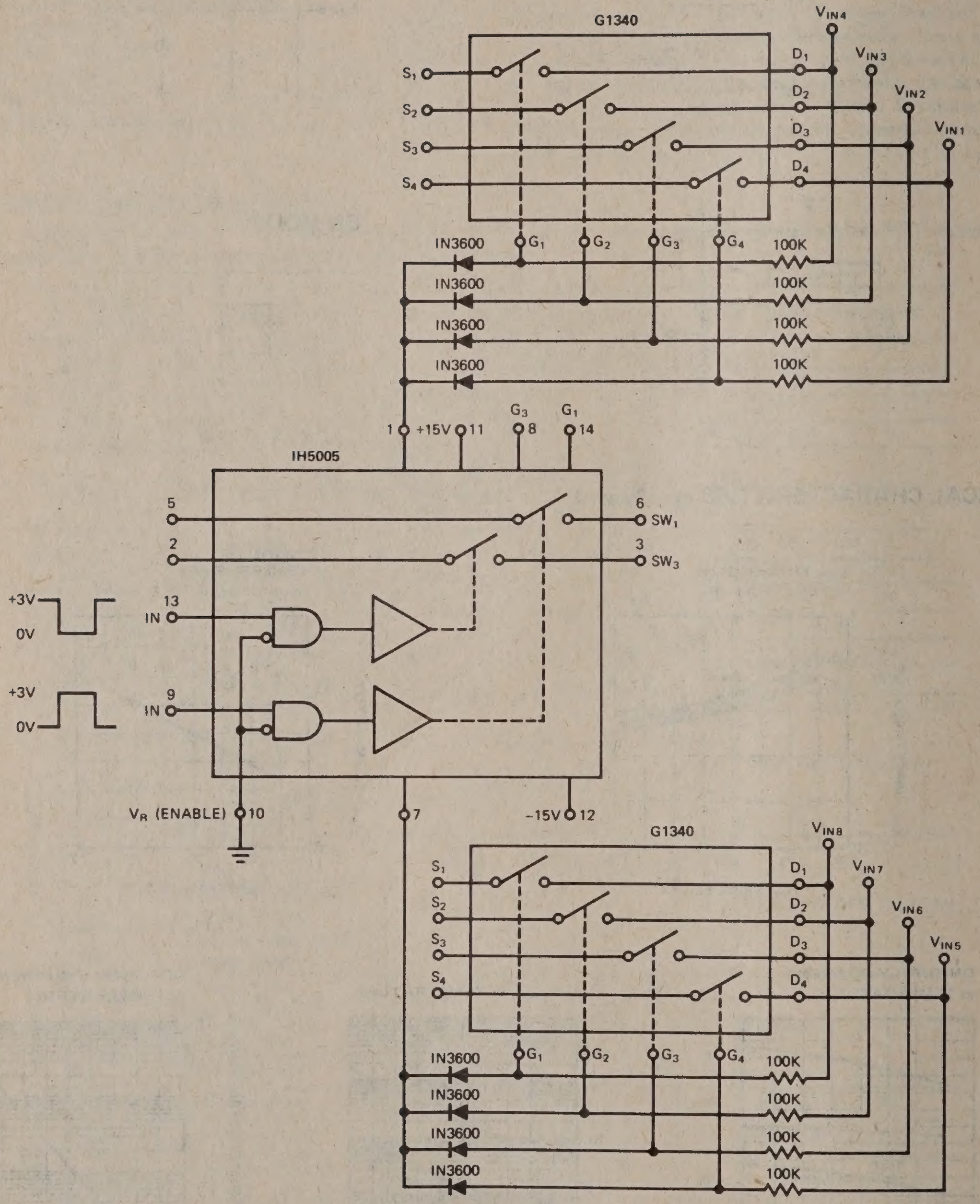


OFF SUPPLY CURRENT vs TEMPERATURE



APPLICATION

Expansion Capability IH5005


G1340
V_{IN4}
V_{IN3}
V_{IN2}
V_{IN1}
S_1
S_2
S_3
S_4
D_1
D_2
D_3
D_4
G_1
G_2
G_3
G_4
IN3600
100K
1
+15V
11
G_3
8
G_1
14
IH5005
5
2
6
3
SW_1
SW_3
+3V
0V
13
IN
9
IN
V_R (ENABLE)
10
7
−15V
12
G1340
V_{IN8}
V_{IN7}
V_{IN6}
V_{IN5}

INTERSIL

IH5009 — IH5024
Virtual Ground Analog Switches

FEATURES

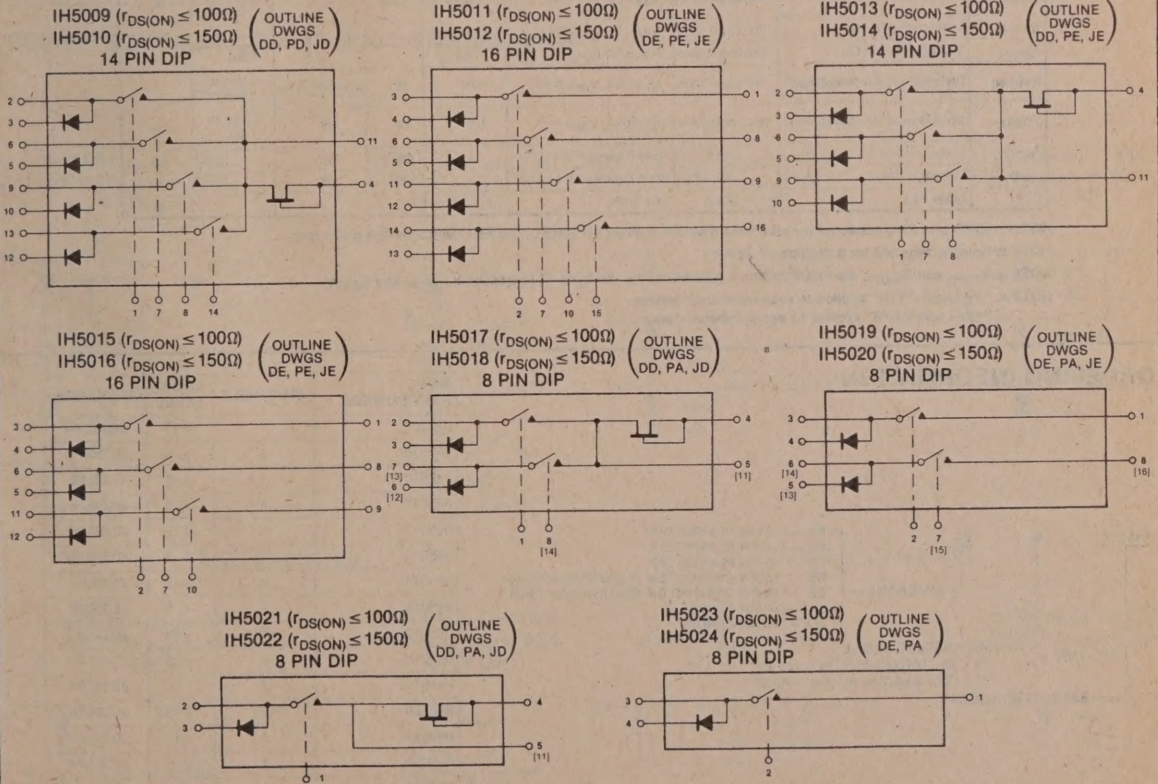
- **Switches Analog Signals up to 20 Volts Peak-to-Peak**
- **Each Channel Complete — Interfaces with Most Integrated Logic**
- **Switching Speeds Less than 0.5μs**
- **$I_{D(OFF)}$ Less than 500pA Typical at 70°C**
- **Effective $r_{ds(ON)}$ — 5Ω to 50Ω**
- **Commercial and Military Temperature Range Operation**

GENERAL DESCRIPTION

The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from T^2L open collector logic (15 volts) while the even numbered devices are driven directly from low level T^2L logic (5 volts). Each channel simulates a SPDT switch. SPST switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (0V). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

PIN CONNECTIONS


IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP
(OUTLINE DWGS DD, PD, JD)

IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP
(OUTLINE DWGS DE, PE, JE)

IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP
(OUTLINE DWGS DD, PE, JE)

IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP
(OUTLINE DWGS DE, PE, JE)

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DD, PA, JD)

IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DE, PA, JE)

IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DD, PA, JD)

IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DE, PA)

(Note: Numbers in brackets refer to CERDIP packages.)

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage....................... 30V
Negative Analog Signal Voltage.................... −15V
Diode Current 10mA
Power Dissipation (Note)......................... 500mW
Storage Temperature .... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

Operating Temperature
5009C Series............................ 0°C to +70°C
5009M Series...................... −55°C to +125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE (Note 4)	TEST CONDITIONS (Note 2)	SPECIFICATION LIMIT −55°C (M) 0°C (C) MIN/MAX	25°C TYP.	25°C MIN/MAX	+125°C (M) +70°C (C) MIN/MAX	UNITS
$I_{IN(ON)}$	Input Current-ON	All	$V_{IN} = 0V$, $I_D = 2mA$	0.1	.01	0.1	100	μA
$I_{IN(OFF)}$	Input Current-OFF	5V Logic Ckts	$V_{IN} = +4.5V$, $V_A = \pm 10V$	0.2	.04	0.1	10	nA
$I_{IN(OFF)}$	Input Current-OFF	15V Logic Ckts	$V_{IN} = +11V$, $V_A = \pm 10V$	0.2	.04	0.2	10	nA
$V_{IN(ON)}$	Channel Control Voltage-ON	5V Logic Ckts	See Figure 5, Note 3	0.5		0.5	0.5	V
$V_{IN(ON)}$	Channel Control Voltage-ON	15V Logic Ckts	See Figure 6, Note 3	1.5		1.5	1.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	5V Logic Ckts	See Figure 5, Note 3	4.5		4.5	4.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	15V Logic Ckts	See Figure 6, Note 3	11.0		11.0	11.0	V
$I_{D(OFF)}$	Leakage Current-OFF	5V Logic Ckts	$V_{IN} = +4.5V$, $V_A = \pm 10V$	0.2	.02	0.2	10	nA
$I_{D(OFF)}$	Leakage Current-OFF	15V Logic Ckts	$V_{IN} = +11V$, $V_A = \pm 10V$	0.2	.02	0.2	10	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	$V_{IN} = 0V$, $I_S = 1mA$	1.0	0.30	1.0	1000 (M) 200 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	$V_{IN} = 0V$, $I_S = 1mA$	0.5	0.10	0.5	500 (M) 100 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	$V_{IN} = 0V$, $I_S = 2mA$	1.0		1.0	10	μA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	$V_{IN} = 0V$, $I_S = 2mA$	2.0		2.0	1000	nA
$r_{DS(ON)}$	Drain-Source ON-Resistance	5V Logic Ckts	$I_D = 2mA$, $V_{IN} = 0.5V$	150	90	150	385 (M) 240 (C)	Ω
$r_{DS(ON)}$	Drain-Source ON-Resistance	15V Logic Ckts	$I_D = 2mA$, $V_{IN} = 1.5V$	100	60	100	250 (M) 160 (C)	Ω
$t_{(on)}$	Turn-ON Time	All	See Figures 3 & 4		150	500		ns
$t_{(off)}$	Turn-OFF Time	All	See Figures 3 & 4		300	500		ns
CT	Cross Talk	All	f = 100Hz		120			dB

NOTE 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

NOTE 2: Refer to Figure 2 for definition of terms.

NOTE 3: $V_{IN(ON)}$ and $V_{IN(OFF)}$ are test conditions guaranteed by the tests of respectively $r_{DS(ON)}$ and $I_{D(OFF)}$.

NOTE 4: "5V Logic CKTS" applies to even-numbered devices.
"15V Logic CKTS" applies to odd-numbered devices.

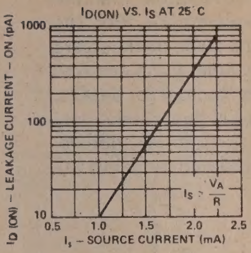
ORDERING INFORMATION

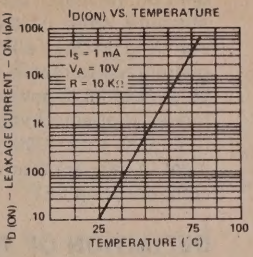
IH50XX M DE
- DE — PACKAGE
  - PA — 8-PIN PLASTIC DIP
  - PD — 14-PIN PLASTIC DIP
  - PE — 16-PIN PLASTIC DIP
  - DD — 14-PIN CERAMIC DIP (Special Order Only)
  - DE — 16-PIN CERAMIC DIP (Special Order Only)
  - JD — 14-PIN CERDIP
  - JE — 16-PIN CERDIP
- M — TEMPERATURE RANGE
  - M = MILITARY (−55°C to +125°C)
  - C = COMMERCIAL (0°C to +70°C)
- IH50XX — BASIC PART NUMBER

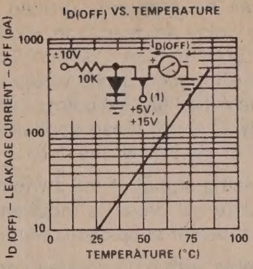
BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5009	4	+15	JD,DD,PD
IH5010	4	+ 5	JD,DD,PD
IH5011	4	+15	JE,DE,PE
IH5012	4	+ 5	JE,DE,PE
IH5013	3	+15	JD,DD,PD
IH5014	3	+ 5	JD,DD,PD
IH5015	3	+15	JE,DE,PE
IH5016	3	+ 5	JE,DE,PE
IH5017	2	+15	JD,DD,PA
IH5018	2	+ 5	JD,DD,PA
IH5019	2	+15	JE,DE,PA
IH5020	2	+ 5	JE,DE,PA
IH5021	1	+15	JD,DD,PA
IH5022	1	+ 5	JD,DD,PA
IH5023	1	+15	JE,DE,PA
IH5024	1	+ 5	JE,DE,PA

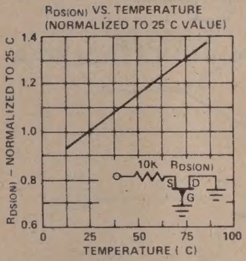
NOTE: Mil-Temperature range (−55°C to +125°C) available ceramic packages only.

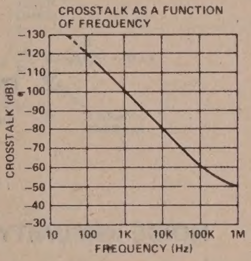
TYPICAL ELECTRICAL CHARACTERISTICS (per channel)



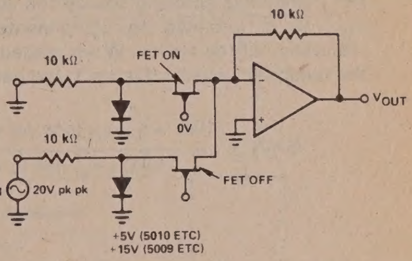








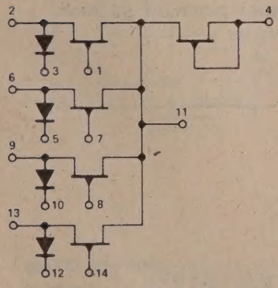
CROSSTALK MEASUREMENT CIRCUIT


10 kΩ
10 kΩ
FET ON
0V
V_{OUT}
10 kΩ
V_{IN}
20V pk pk
FET OFF
+5V (5010 ETC)
+15V (5009 ETC)

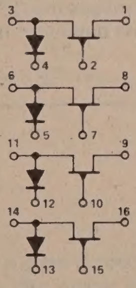
DEVICE SCHEMATICS AND PIN CONNECTIONS

FOUR CHANNEL

IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

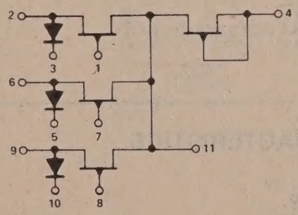

2
4
3
1
6
11
5
7
9
10
8
13
12
14

IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

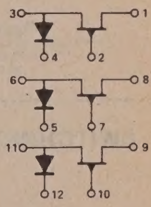

3
1
4
2
6
8
5
7
11
9
12
10
14
16
13
15

THREE CHANNEL

IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

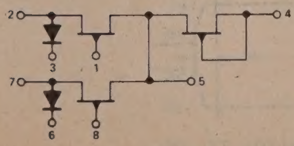

2
4
3
1
6
5
7
9
11
10
8

IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

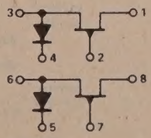

3
1
4
2
6
8
5
7
11
9
12
10

TWO CHANNEL

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

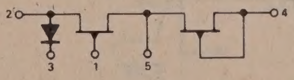


IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

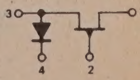


SINGLE CHANNEL

IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



THEORY OF OPERATION

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories; those which are less than ±200mV, and those which are greater than ±200mV. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed.

By limiting the analog signal at the switching point to ±200mV, no external driver is required and the need for additional power supplies is eliminated.

Devices are available with both common drains and with uncommitted drains.

Those devices which feature common drains have another FET in addition to the channel switches. This FET, which has gate and source connected such that $V_{GS} = 0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 1) the gain is given by

$$\text{GAIN} = \frac{10\text{k}\Omega + r_{DS(ON)}\ \text{(compensator)}}{10\text{k}\Omega + r_{DS}\ \text{(switch)}}$$

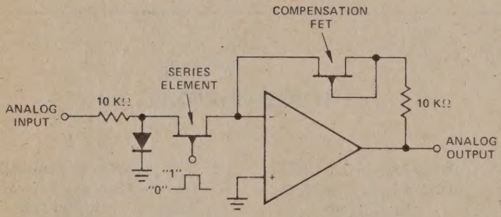

COMPENSATION FET
SERIES ELEMENT
ANALOG INPUT
10 KΩ
10 KΩ
ANALOG OUTPUT
"1"
"0"

Figure 1. Use of Compensation FET

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. Contact factory for details. Since the absolute value of $r_{DS(ON)}$ is guaranteed only to be less than 100Ω or 150Ω, a substantial improvement in gain accuracy can be obtained by using the compensating FET.

DEFINITION OF TERMS

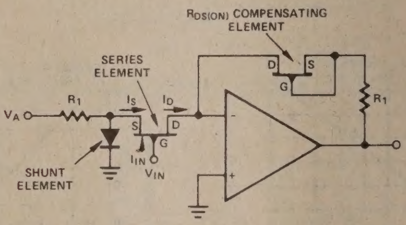

RDS(ON) COMPENSATING ELEMENT
SERIES ELEMENT
VA
R1
IS
ID
D
S
G
IIN
VIN
SHUNT ELEMENT
R1

Figure 2.

NOISE IMMUNITY

The advantage of SPDT switching is high noise immunity when the series elements is OFF. For example, if a ±10V analog input is being switched by T²L open collector logic, the series switch is OFF when the logic level is at +15 volts. At this time, the diode conducts and holds the source at approximately +0.7 volts with an AC impedance to ground of 25 ohms. Thus random noise superimposed on the +10 volt analog input will not falsely trigger the FET since the noise voltage will be shunted to ground.

When switching a negative voltage, the input further increases the OFF voltage beyond pinch-off, so there is no danger of the FET turning on.

SWITCHING CHARACTERISTICS

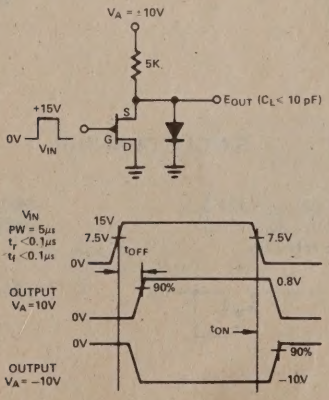

VA = ±10V
5K
EOUT (CL < 10 pF)
+15V
0V
VIN
S
G
D
VIN
PW = 5µs
tr <0.1µs
tf <0.1µs
15V
7.5V
0V
tOFF
7.5V
OUTPUT
VA=10V
90%
0.8V
0V
tON
0V
90%
OUTPUT
VA= –10V
–10V

Figure 3. High Level Logic

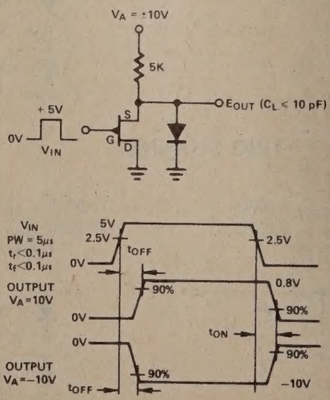

VA = ±10V
5K
EOUT (CL < 10 pF)
+ 5V
0V
VIN
S
G
D
VIN
PW = 5µs
tr<0.1µs
tf<0.1µs
5V
2.5V
0V
tOFF
2.5V
OUTPUT
VA=10V
90%
0.8V
90%
0V
tON
0V
90%
OUTPUT
VA=–10V
90%
tOFF
–10V

Figure 4. Standard DTL, TTL, RTL

LOGIC INTERFACE CIRCUITS

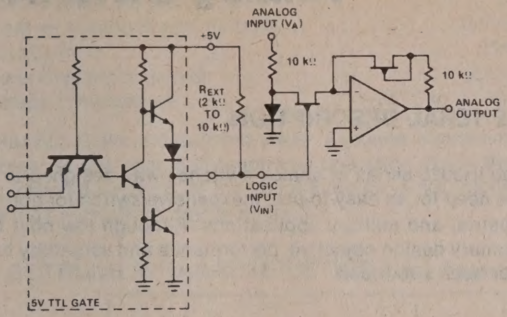

ANALOG INPUT (V_A)
+5V
10 kΩ
10 kΩ
R_{EXT} (2 kΩ TO 10 kΩ)
ANALOG OUTPUT
LOGIC INPUT (V_{IN})
5V TTL GATE

Figure 5. Interfacing with +5V Logic

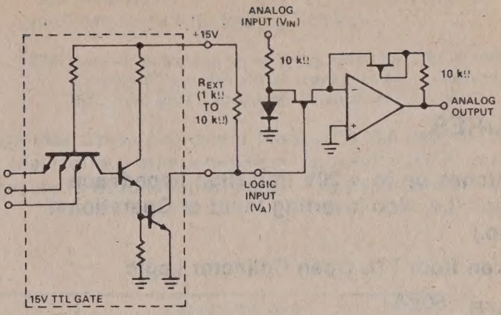
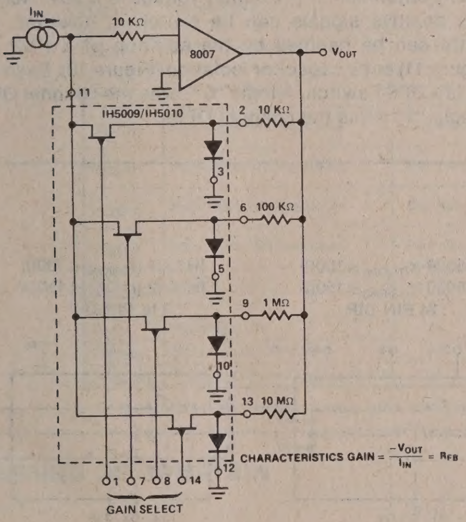
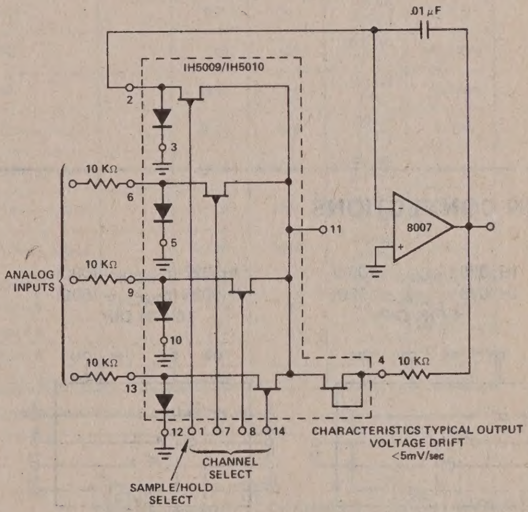

ANALOG INPUT (V_{IN})
+15V
10 kΩ
10 kΩ
R_{EXT} (1 kΩ TO 10 kΩ)
ANALOG OUTPUT
LOGIC INPUT (V_A)
15V TTL GATE

Figure 6. Interfacing with +15V Open Collector Logic

APPLICATIONS (Note)


I_{IN}
10 KΩ
8007
V_{OUT}
11
IH5009/IH5010
2
10 KΩ
3
6
100 KΩ
5
9
1 MΩ
10
13
10 MΩ
12
CHARACTERISTICS GAIN = $\frac{-V_{OUT}}{I_{IN}}$ = R_{FB}
1
7
8
14
GAIN SELECT


.01 μF
IH5009/IH5010
2
3
10 KΩ
6
5
11
8007
ANALOG INPUTS
10 KΩ
9
10
10 KΩ
13
4
10 KΩ
12
1
7
8
14
CHARACTERISTICS TYPICAL OUTPUT VOLTAGE DRIFT <5mV/sec
CHANNEL SELECT
SAMPLE/HOLD SELECT

NOTE: Additional applications information is given in Application Bulletins A003 "Understanding and Applying the Analog Switch" and A004 "The 5009 Series of Low Cost Analog Switches". See also September '79 issue of Product Engineering "Analog Switching" by Paresh Maniar.

INTERSIL

IH5025 — IH5038
Positive Signal Analog Switches

FEATURES

- **Switches up to +20V into High Impedance Loads (i.e. Non-Inverting Input of Operational Amp.)**
- **Driven from TTL Open Collector Logic**
- **$I_{D(OFF)} < 50pA$**
- **$r_{DS(ON)} < 150\Omega$**
- **$r_{DS(ON)}$ Match < 50Ω Channel to Channel**
- **Switching Speeds < 100ns**

GENERAL DESCRIPTION

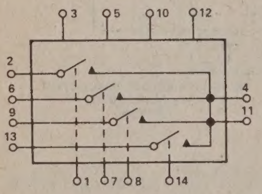
The IH5025 series of analog switches was designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver.

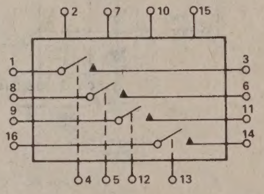
The entire family is designed to be driven from TTL open collector logic (15V), but can be driven from 5V logic if signal input is less than 1V. Alternatively, 20V switching is readily obtainable if TTL supply voltage is +25V. Normally, only positive signals can be switched; however, up to ±10V can be handled by the addition of a PNP stage (Figure 11) or by capacitor isolation (Figure 10). Each channel is a SPST switch. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

PIN CONNECTIONS

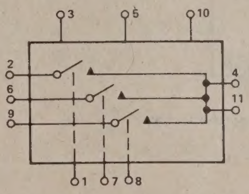
IH5025 ($r_{DS(ON)} \leq 100\Omega$)
IH5026 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



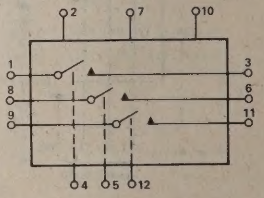
IH5027 ($r_{DS(ON)} \leq 100\Omega$)
IH5028 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



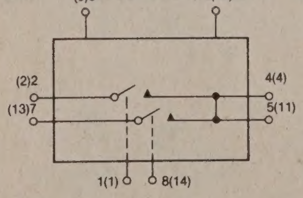
IH5029 ($r_{DS(ON)} \leq 100\Omega$)
IH5030 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



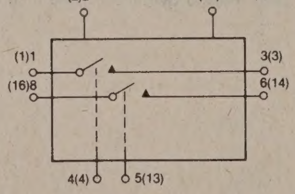
IH5031 ($r_{DS(ON)} \leq 100\Omega$)
IH5032 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



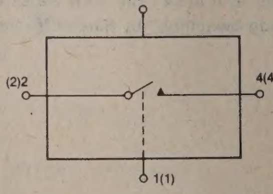
IH5033 ($r_{DS(ON)} \leq 100\Omega$)
IH5034 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5035 ($r_{DS(ON)} \leq 100\Omega$)
IH5036 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5037 ($r_{DS(ON)} \leq 100\Omega$)
IH5038 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



NUMBERS IN PARENTHESES INDICATE CERAMIC PACKAGE PIN-OUT

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage	25V
Negative Analog Signal Voltage	−0.5VDC
Drain Current	25mA
Power Dissipation (Note)	500mW
Storage Temperature	−65°C to +150°C
Operating Temperature	
5025C Series	0°C to +70°C
5025M Series	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE	TEST CONDITIONS	SPECIFICATION LIMIT −55°C (M) 0°C (C)	25°C TYP.	25°C MIN/MAX	+125°C (M) +70°C (C)	UNITS MIN/MAX
$I_{IN(ON)}$	Input Current-ON	All	$V_{IN} = 0V$		0.30	1.0	100 (M) 25 (C)	nA (max)
$I_{IN(OFF)}$	Input Current-OFF	All	$V_{IN} = 15V$		0.20	1.0	50 (M) 10 (C)	nA (max)
$V_{IN(ON)}$	Channel Control Voltage-ON	All	See Figure 1	1.5		1.5	1.5	V (max)
$V_{IN(OFF)}$	Channel Control Voltage-OFF	All	See Figure 1	14.0		14.0	14.0	V (min)
$I_{D(OFF)}$	Leakage Current-OFF	All	$V_{IN} = 15V$		0.06	0.5	100 (M) 10 (C)	nA (max)
$I_{D(ON)}$	Leakage Current-ON	Odd Nos.	$V_{IN} = 0V$		1.00	10.0	5000 (M) 250 (C)	nA (max)
$I_{D(ON)}$	Leakage Current-ON	Even Nos.	$V_{IN} = 0V$		0.10	1.0	500 (M) 25 (C)	nA (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.	$V_{IN} = 0.5V$, $I_D = 1mA$		60.00	100.0	250 (M) 150 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.	$V_{IN} = 0.5V$, $I_D = 1mA$		90.00	150.0	385 (M) 240 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.	$V_{IN} = 1.0V$, $I_D = 1mA$		85.00	160.0	420 (M) 250 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.	$V_{IN} = 1.0V$, $I_D = 1mA$		110.00	200.0	400 (M) 250 (C)	Ω (max)
$t_{(on)}$	Turn-ON Time	All	See Figure 2		0.10	0.2	0.4	μs (max)
$t_{(off)}$	Turn-OFF Time	All	See Figure 2		0.10	0.2	0.4	μs (max)
$Q_{(INJ)}$	Charge Injection	All	See Figure 3		7.00	20.0		mV_{p-p} (max)
$V_{A(OFF)}$	Cross Coupling Rejection	All	See Figure 4		0.10	1.0		mV_{p-p} (max)
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match	All	$V_{IN} = 0.5V$, $I_D = 1mA$		25.00	50.0	50	Ω (max)

NOTE 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

ORDERING INFORMATION

IH50XX M DE

PACKAGE
- **PA — 8-PIN PLASTIC DIP**
- **PD — 14-PIN PLASTIC DIP**
- **PE — 16-PIN PLASTIC DIP**
- **DD — 14-PIN CERAMIC DIP (Special Order Only)**
- **DE — 16-PIN CERAMIC DIP (Special Order Only)**
- **JD — 14-PIN CERDIP**
- **JE — 16-PIN CERDIP**

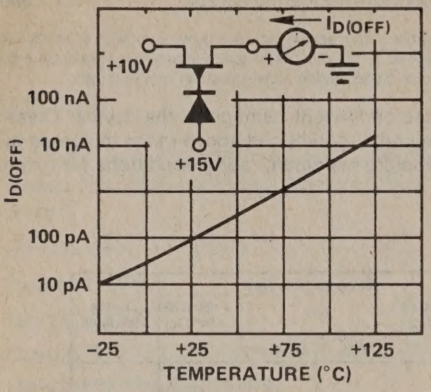
TEMPERATURE RANGE
M = MILITARY (−55°C to +125°C)
C = COMMERCIAL (0°C to +70°C)

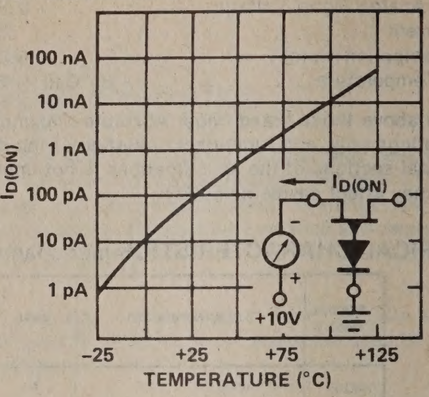
BASIC PART NUMBER

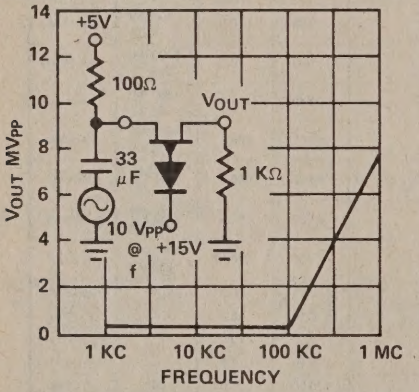
BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5025	4	+15	JD,DD,PD
IH5026	4	+ 5	JD,DD,PD
IH5027	4	+15	JE,DE,PE
IH5028	4	+ 5	JE,DE,PE
IH5029	3	+15	JD,DD,PD
IH5030	3	+ 5	JD,DD,PD
IH5031	3	+15	JE,DE,PE
IH5032	3	+ 5	JE,DE,PE
IH5033	2	+15	JD,DD,PA
IH5034	2	+ 5	JD,DD,PA
IH5035	2	+15	JE,DE,PA
IH5036	2	+ 5	JE,DE,PA
IH5037	1	+15	JD,DD,PA
IH5038	1	+ 5	JD,DD,PA

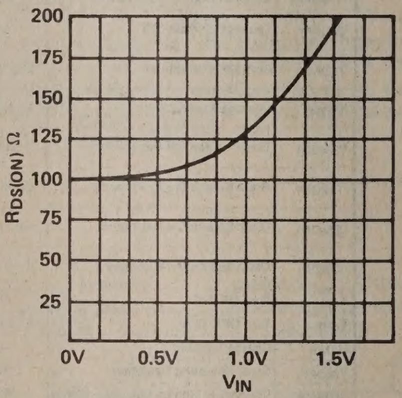
NOTE: Mil-Temperature range (−55°C to +125°C) available in ceramic packages only.

TYPICAL ELECTRICAL CHARACTERISTICS (per channel)

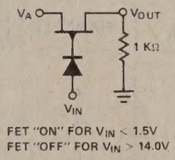

$I_{D(OFF)}$ VS. TEMPERATURE


$I_{D(ON)}$ VS. TEMPERATURE


CROSS COUPLING REJECTION VS. FREQUENCY


$R_{DS(ON)}$ VS. V_{IN}

TEST CIRCUITS


V_A
V_OUT
1 KΩ
V_IN

FET "ON" FOR $V_{IN} < 1.5V$
FET "OFF" FOR $V_{IN} > 14.0V$

Figure 1

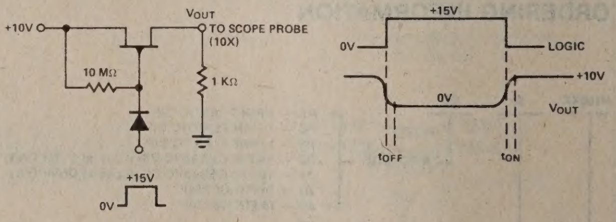

+10V
V_OUT
TO SCOPE PROBE (10X)
10 MΩ
1 KΩ
+15V
0V
+15V
0V
LOGIC
+10V
0V
V_OUT
t_OFF
t_ON

Figure 2

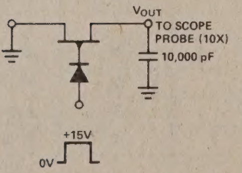

V_OUT
TO SCOPE PROBE (10X)
10,000 pF
+15V
0V

Figure 3

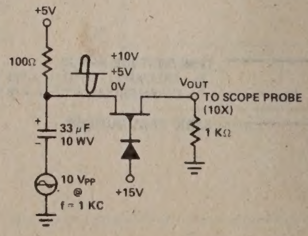
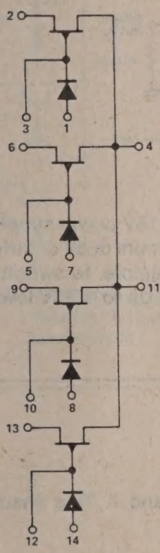

+5V
100Ω
+10V
+5V
0V
V_OUT
TO SCOPE PROBE (10X)
33 μF 10 WV
1 KΩ
10 V_PP @ f = 1 KC
+15V

Figure 4

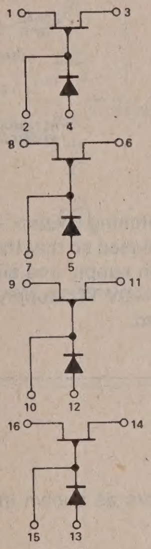
DEVICE SCHEMATICS

FOUR CHANNEL

IH5025 ($r_{DS(ON)} \leq 100\Omega$)
IH5026 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

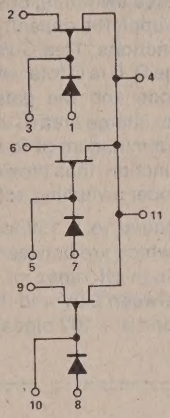

2
3
1
6
4
5
7
9
11
10
8
13
12
14

IH5027 ($r_{DS(ON)} \leq 100\Omega$)
IH5028 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

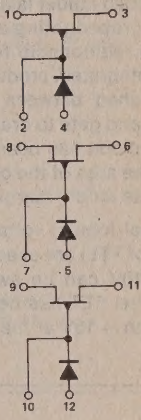

1
3
2
4
8
6
7
5
9
11
10
12
16
14
15
13

THREE CHANNEL

IH5029 ($r_{DS(ON)} \leq 100\Omega$)
IH5030 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

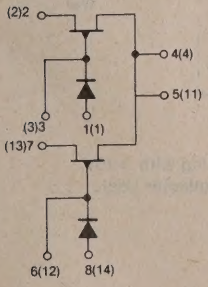

2
4
3
1
6
11
5
7
9
10
8

IH5031 ($r_{DS(ON)} \leq 100\Omega$)
IH5032 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

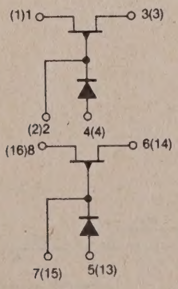

1
3
2
4
8
6
7
5
9
11
10
12

TWO CHANNEL

IH5033 ($r_{DS(ON)} \leq 100\Omega$)
IH5034 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

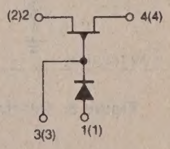

(2)2
4(4)
5(11)
(3)3
1(1)
(13)7
6(12)
8(14)

IH5035 ($r_{DS(ON)} \leq 100\Omega$)
IH5036 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP


(1)1
3(3)
(2)2
4(4)
(16)8
6(14)
7(15)
5(13)

SINGLE CHANNEL

IH5037 ($r_{DS(ON)} \leq 100\Omega$)
IH5038 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



Numbers in parentheses indicate CERAMIC PACKAGE LAYOUT

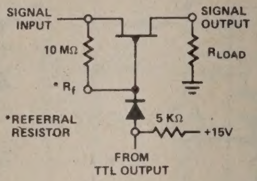
THEORY OF OPERATION

The IH5025 series differs from the IH5009 series in that they may be driven by floating outputs. This family is generally used when operating into the non-inverting input of an operational amplifier, while the IH5009 series is used in operations where the output feeds into the inverting (virtual ground) input.

The IH5025 model is a basic charge area switching device, in that proper gating action depends upon the capacity vs. voltage relationship for the diode junctions. This C vs. V, when integrated, produces total charge Q. It is Q total which is switched between the series diode and the gate to source and gate to drain junctions. The charge area (C vs. V) for the diode has been chosen to be a minimum of four (4) times the area of the gate to source junction, thus providing adequate safety margins to insure proper switching action.

If normal logical voltage levels of ground to +15V (open collector TTL) are used, only signals which are between 0V and +10V can be switched. The pinch-off range of the P-Channel FET has been selected between 2.0V and 3.9V; thus with +15V at the logical input, and a +10V signal input, 1.1V of margin exists for turn-off. When the IH5025 is used with 5V TTL logic, a maximum of +1V can be switched.

The gate of each FET has been brought out so that a "referral resistor" can be placed between gate and source. This is used to minimize charge injection effects. The connection is shown below:



For switching levels > +10V, the +15V power supply must be increased so that there is a minimum of 5V of difference between supply and signal. For example, to switch +15V level, +20V TTL supply is required. Up to +20V levels can be gated.

LOGIC INTERFACE CIRCUITS

When operating with TTL logic it is necessary to use pull-up resistors as shown in Figures 6 and 7. This ensures the necessary positive voltages for proper gating action.

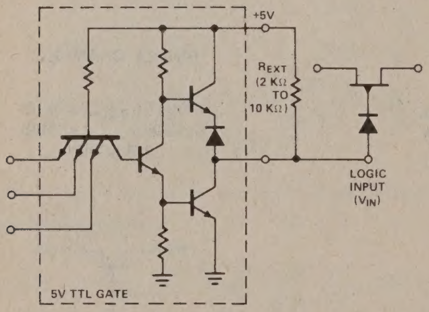


Figure 5. Interfacing with +5V Logic

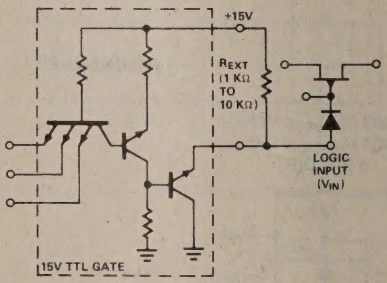


Figure 6. Interfacing with +15V Open Collector Logic

APPLICATIONS

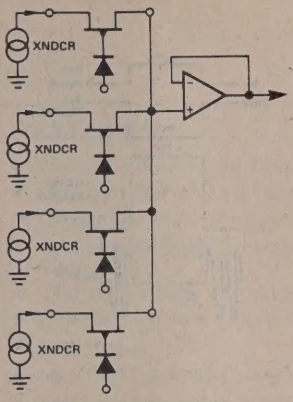

XNDCR
XNDCR
XNDCR
XNDCR

Figure 7. Multiplexer from Positive Output Transducers

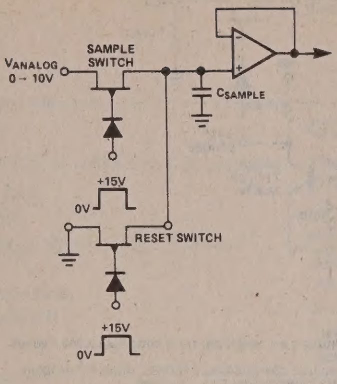

VANALOG
0 → 10V
SAMPLE SWITCH
CSAMPLE
+15V
0V
RESET SWITCH
+15V
0V

Figure 8. Sample and Hold Switch

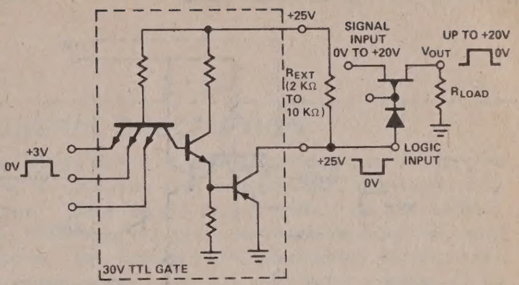
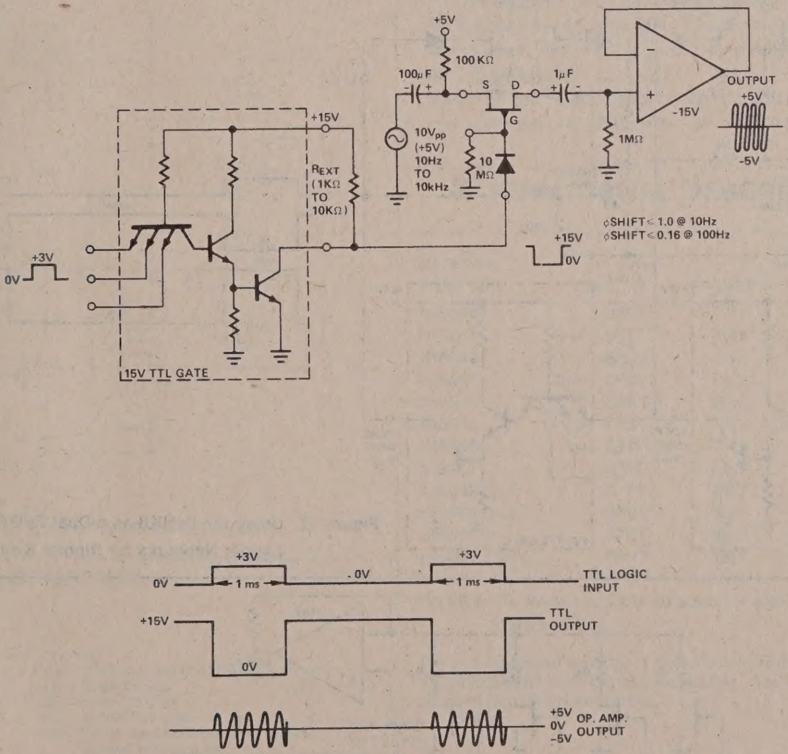

+25V
SIGNAL INPUT 0V TO +20V
UP TO +20V
VOUT
0V
REXT (2 KΩ TO 10 KΩ)
RLOAD
+3V
0V
LOGIC INPUT
+25V
0V
30V TTL GATE

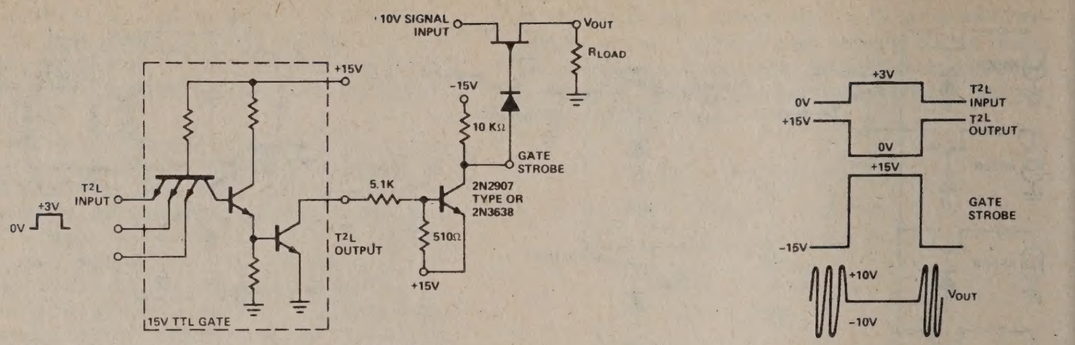
Figure 9. Switching up to +20V Signals with T²L Logic


+5V
100 KΩ
100μ F
S
D
1μ F
OUTPUT
+5V
-5V
-15V
+15V
G
10Vpp (+5V) 10Hz TO 10kHz
10 MΩ
1MΩ
REXT (1KΩ TO 10KΩ)
+3V
0V
φSHIFT ≤ 1.0 @ 10Hz
φSHIFT ≤ 0.16 @ 100Hz
+15V
0V
15V TTL GATE
+3V
+3V
0V
1 ms
0V
1 ms
TTL LOGIC INPUT
+15V
0V
TTL OUTPUT
+5V
0V
-5V
OP. AMP. OUTPUT

NOTE: TO SWITCH ±10 VAC (20Vpp): (1) INCREASE ±5V SUPPLY TO +10V.
(2) INCREASE TTL SUPPLY FROM +15V TO +25V.

Figure 10. Switching Bipolar Signals with T²L Logic

APPLICATIONS (Cont.)


10V SIGNAL INPUT
VOUT
RLOAD
+15V
-15V
10 KΩ
GATE STROBE
T2L INPUT
+3V
0V
5.1K
2N2907 TYPE OR 2N3638
T2L OUTPUT
510Ω
+15V
15V TTL GATE
+3V
0V
T2L INPUT
+15V
T2L OUTPUT
0V
+15V
GATE STROBE
-15V
+10V
VOUT
-10V

ADVANTAGES OVER FIGURE NO. 10 METHOD

A. DC LEVELS OF UP TO ± 10V CAN BE SWITCHED, AS WELL AS AC SIGNALS UP TO 100 KC; NO. 10 METHOD SWITCHES ONLY AC RANGE OF 10 Hz TO 10 kHz.

B. CKT IS NOW BREAK BEFORE MAKE

DISADVANTAGES:

A. PNP CKT DRAWS 3 mA, WHEN ON; THUS ADDS 3 mA X 30V = 90 mW POWER DISS.

B. t_{ON} TIME WILL BE CONSIDERABLY SLOWED DOWN FROM 100 ns (BEFORE IN FIGURE NO. 10) TO 1 - 2 μs NOW.

Figure 11. Switching Bipolar Signals with T2L Logic (Alternate Method)

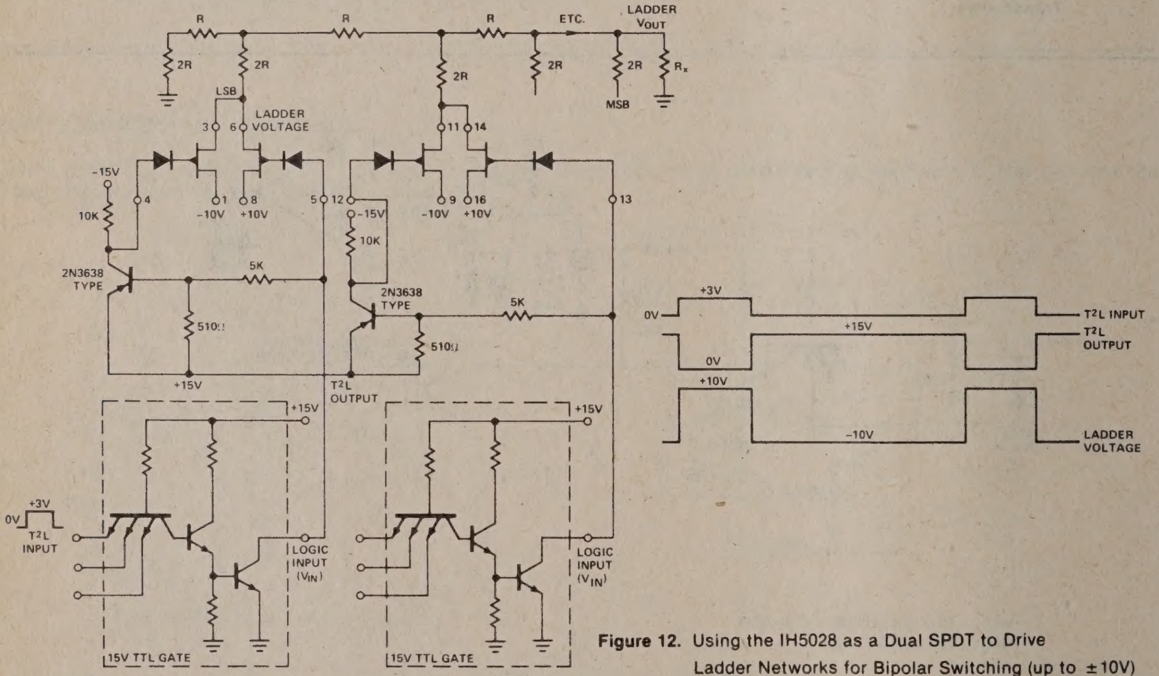
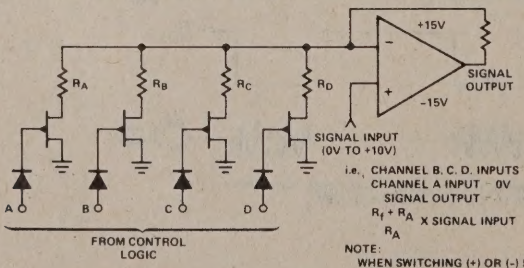

R
R
R
ETC.
LADDER VOUT
2R
2R
2R
2R
2R
Rx
LSB
MSB
LADDER VOLTAGE
3
6
11
14
-15V
4
1
8
-10V
+10V
5
12
-15V
9
16
-10V
+10V
13
10K
10K
2N3638 TYPE
5K
510Ω
+15V
2N3638 TYPE
5K
510Ω
T2L OUTPUT
+15V
+15V
+15V
+3V
0V
T2L INPUT
LOGIC INPUT (VIN)
LOGIC INPUT (VIN)
15V TTL GATE
15V TTL GATE
+3V
0V
T2L INPUT
+15V
T2L OUTPUT
0V
+10V
-10V
LADDER VOLTAGE

Figure 12. Using the IH5028 as a Dual SPDT to Drive Ladder Networks for Bipolar Switching (up to ±10V)


+15V
-
+
-15V
RA
RB
RC
RD
SIGNAL OUTPUT
SIGNAL INPUT (0V TO +10V)
A
B
C
D
FROM CONTROL LOGIC

i.e., CHANNEL B, C, D, INPUTS = +15V;
CHANNEL A INPUT = 0V
SIGNAL OUTPUT =
$\frac{R_f + R_A}{R_A}$ X SIGNAL INPUT

NOTE:
WHEN SWITCHING (+) OR (-) SIGNAL INPUTS,A SCHEME SIMILAR TO FIGURES 10 OR 11 SHOULD BE USED.

Figure 13. Gain Control with High Input Impedance

INTERSIL

IH5040-IH5051 Family High Level CMOS Analog Gates

FEATURES

- Switches Greater Than 20Vpp Signals With ±15V Supplies
- Quiescent Current Less Than 1μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching t_{off} 200 nsec, t_{on} 300 nsec Typical
- T^2L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Low $r_{DS(on)}$ – 35Ω
- New DPDT & 4PST Configurations
- Complete Monolithic Construction IH5040 through IH5047

FUNCTIONAL DIAGRAM

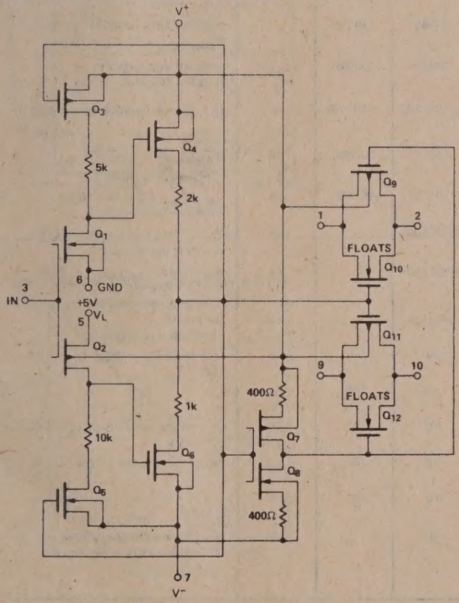


FIGURE 1. TYPICAL DRIVER, GATE — IH5042

ORDERING INFORMATION

IH5040 M JE

Package
DE – 16-Pin Ceramic DIP (Special Order Only)
FE – 16-Pin Flatpak
JE – 16-Pin CERDIP
PE – 16-Pin Plastic DIP
TW – TO-99 Metal Can (IH5041/2, IH5044, IH5048, IH5050 Only)

Temperature Range
M – Military –55°C to +125°C
C – Commercial 0°C to +70°C

Basic Part Number

GENERAL DESCRIPTION

The IH5040 family of solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The IH5040 CMOS technology has eliminated this serious systems problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1μA. Also designed into the 5040 is guaranteed Break-Before-Make switching, which is accomplished by extending the t_{on} time (300 nsec TYP.) so that it exceeds t_{off} time (200 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FUNCTIONAL DESCRIPTION

INTERSIL PART NO.	TYPE	$r_{DS(on)}$	PIN/FUNCTIONAL EQUIVALENT (Note 1)
IH5040	SPST	75Ω	
IH5041	Dual SPST	75Ω	
IH5042	SPDT	75Ω	DG 188AA/BA
IH5043	Dual SPDT	75Ω	DG 191AP/BP
IH5044	DPST	75Ω	
IH5045	Dual DPST	75Ω	DG 185AP/BP
IH5046	DPDT	75Ω	
IH5047	4PST	75Ω	
IH5048 Dual	SPST	35Ω	
IH5049 Dual	DPST	35Ω	DG 184AP/BP
IH5050	SPDT	35Ω	DG 187AA/BA
IH5051 Dual	SPDT	35Ω	DG 190AP/BP

NOTE 1. See Switching State diagrams for applicable package equivalency.

Pin and functional equivalent monolithic versions of the DG181, DG182, DG187 and DG188 are available. See data sheet for this and also IH181 to IH191.

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal)	< 30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board) Derate 6mW/°C Above 70°C	
Lead Temperature (Soldering, 10 sec)	300°C

$V^+ - V^-$	< 33V
$V^+ - V_D$	< 30V
$V_D - V^-$	< 30V
$V_D - V_S$	< ±22V
$V_L - V^-$	< 33V
$V_L - V_{IN}$	< 30V
V_L-GND	< 20V
V_{IN}-GND	< 20V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, $V^+ = +15$ V, $V^- = -15$ V, $V_L = +5$ V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4 V Note 1
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8 V Note 1
$r_{DS(on)}$	Drain–Source On Resistance	75(35)	75(35)	150(60)	80 (45)	80 (45)	130 (45)	Ω	(IH5048 Thru IH5051) I_S = 1mA, V_{ANALOG} = -10 V to +10 V
$\Delta r_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match	25(15)	25 (15)	25(15)	30(15)	30(15)	30(15)	Ω	(IH5048 thru IH5051) I_S (Each Channel) = 1 mA,
V_{ANALOG}	Min. Analog Signal Handling Capability	±11(±10)	±11(±10)	±11(±10)	±10(±10)	±10(±10)	±10(±10)	V	I_S = 10 mA (IH5048 thru IH5051)
$I_{D(OFF)}$	Switch OFF Leakage Current	1(1)	1(1)	100(100)	5(5)	5(5)	100(100)	nA	V_{ANALOG} = -10 V to +10 V (IH5048 thru IH5051
$I_{D(ON)}$ $+I_{S(ON)}$	Switch On Leakage Current	2(2)	2(2)	200(200)	10 (10)	10 (10)	100(200)	nA	$V_D = V_S$ = -10 V to + 10 V (IH5048 thru IH5051)
t_{on}	Switch "ON" Time		500(250)			500(300)		ns	R_L = 1 kΩ, V_{ANALOG} = -10 V to +10 V See Fig. A
t_{off}	Switch "OFF" Time		250(150)			250(150)		ns	R_L = 1 kΩ, V_{ANALOG} = -10 V to +10 V See Fig. A (IH5048 thru IH5051)
$Q_{(INJ.)}$	Charge Injection		15 (10)			20 (10)		mV	See Fig. B (IH5048 thru IH5051)
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, $C_L \leq 5$ pF See Fig. C
I^+_Q	+ Power Supply Quiescent Current	1	1	10	10	10	100	μA	
I^-_Q	− Power Supply Quiescent Current	1	1	10	10	10	100	μA	$V^+ = +15$ V, $V^- = -15$ V, $V_L = +5$ V $V_L = +5$ V
I^-_{LQ}	+5 V Supply Quiescent Current	1	1	10	10	10	100	μA	Switch Duty Cycle ≤ 10%
I_{GND}	Gnd Supply Quiescent Current	1	1	10	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches as per Fig. E

TEST CIRCUITS

FIG. A

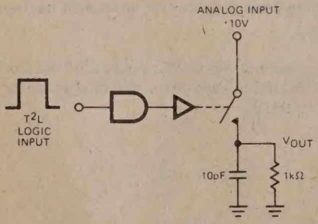


FIG. B

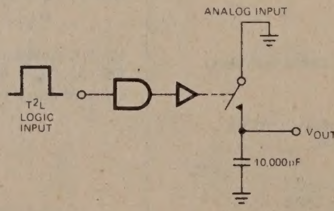
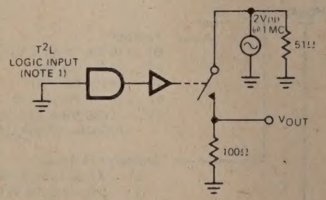


FIG. C



NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

TYPICAL ELECTRICAL CHARACTERISTICS (Per Channel)

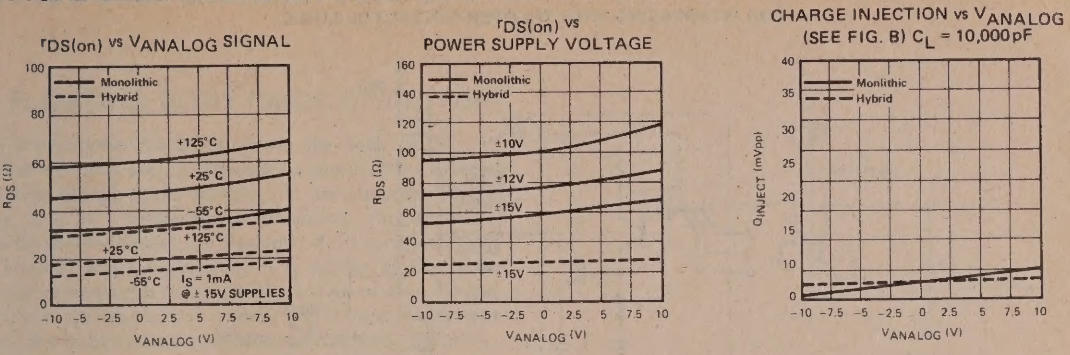


FIGURE D

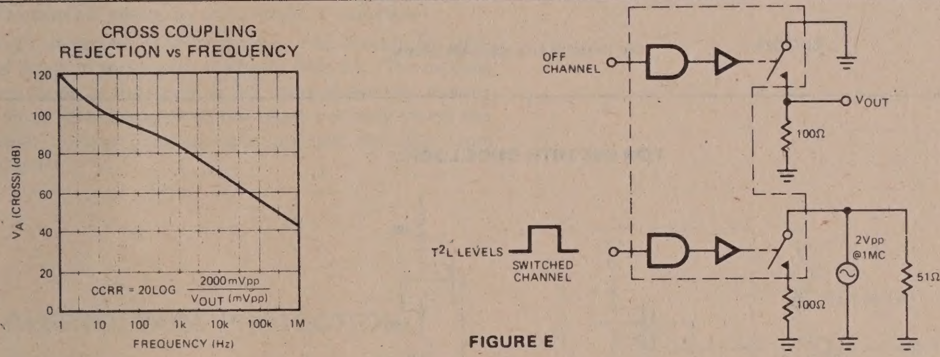


FIGURE E

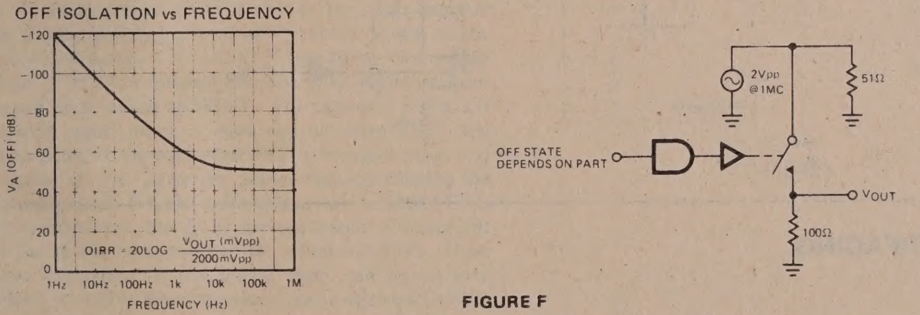


FIGURE F

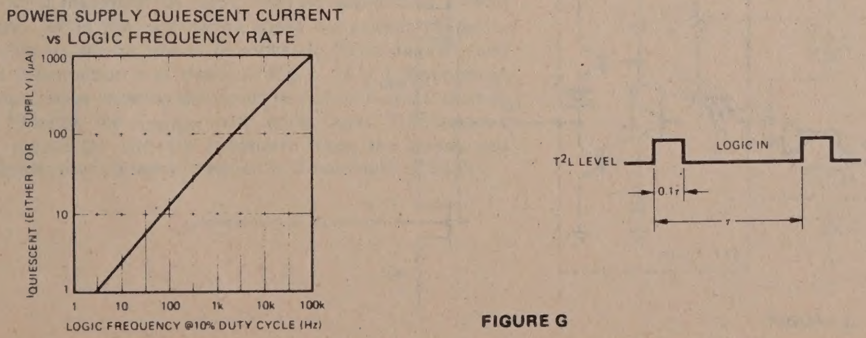
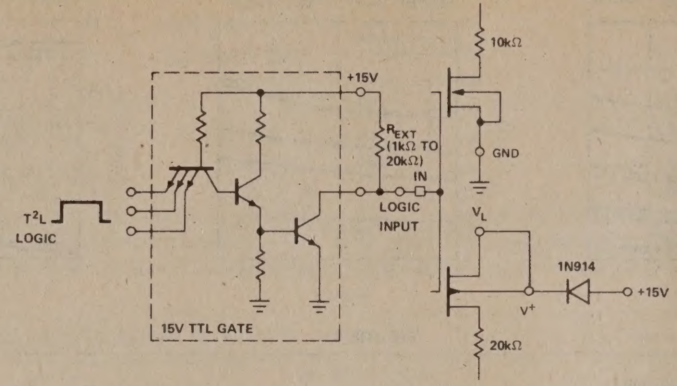


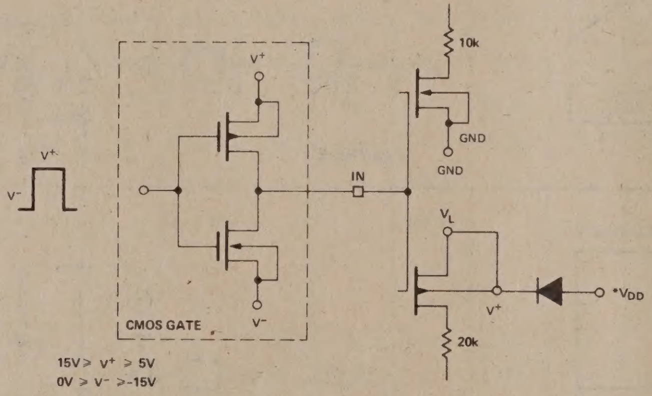
FIGURE G

FOR INTERFACING WITH T²L OPEN COLLECTOR LOGIC.

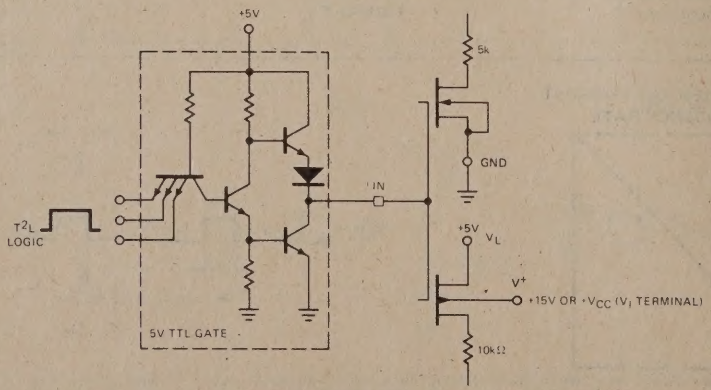

10kΩ
+15V
R_{EXT} (1kΩ TO 20kΩ)
IN
LOGIC INPUT
GND
V_L
1N914
+15V
V^+
20kΩ
T²L LOGIC
15V TTL GATE

TYP. EXAMPLE FOR +15V CASE SHOWN

FOR USE WITH CMOS LOGIC.


10k
V^+
GND
GND
V^+
V^-
IN
V_L
V^+
$*V_{DD}$
V^-
CMOS GATE
20k
15V ≥ V+ ≥ 5V
0V ≥ V− ≥ -15V

LOGIC INTERFACING


+5V
5k
GND
IN
T²L LOGIC
+5V
V_L
V^+
+15V OR +V_{CC} (V_L TERMINAL)
10kΩ
5V TTL GATE

THEORY OF OPERATION

A. FLOATING BODY CMOS STRUCTURE

In a conventional C-MOS structure, the body of the "n" channel device is tied to the negative supply, thus forming a reverse biased diode between the drain/source and the body (Fig. J). Under certain conditions this diode can become forward biased; for example, if the supplies are off (at ground) and a negative input is applied to the drain. This can have serious consequences for two reasons. Firstly, the diode has no current limiting and if excessive current flows, the circuit may be permanently damaged. Secondly, this diode forms part of a parasitic SCR in the conventional C-MOS structure. Forward biasing the diode causes the SCR to turn on, giving rise to a "latch-up" condition.

Intersil's improved C-MOS process incorporates an additional diode in series with the body (Fig. K). The cathode of this diode is then tied to V+, thus effectively floating the body. The inclusion of this diode not only blocks the excessive current path, but also prevents the SCR from turning on.

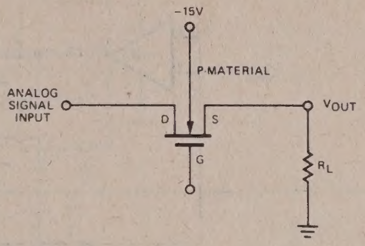


FIGURE J

B. OVERVOLTAGE PROTECTION

The floating body construction inherently provides overvoltage protection. In the conventional C-MOS process, the body of all N-channel FETs is tied to the most negative power supply and the body of all P-channel devices to the most positive supply (i. e., ±15V). Thus, for an overvoltage spike of > ±15V, a forward bias condition exists between drain and body of the MOSFET. For example, in Fig. J if the analog signal input is more negative than −15V, the drain to body of the N-channel FET is forward biased and destruction of the device can result. Now by floating the body, using diode D1, the drain to body of the MOSFET is still forward biased, but D1 is reversed biased so no current flows (up to the breakdown of D1 which is ≥ 40V). Thus, negative excursions of the analog signal can go up to a maximum of −25V. When the signal goes positive (≥ +15V, D1 is forward biased, but now the drain to body junction is reversed for the N-channel FET; this allows the signal to go to a maximum of +25V with no appreciable current flow. While the explanation above has been restricted to N-channel devices, the same applies to P-channel FETs and the construction is as shown in Fig. L. Fig. L describes an output stage showing the paralleling of an N and P channel to linearize the $r_{DS(ON)}$ with signal input. The presence of diodes D1 and D2 effectively floats the bodies and provides over voltage protection to a maximum of ±25V.

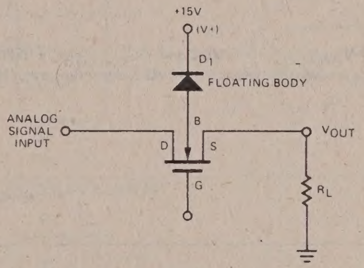


FIGURE K

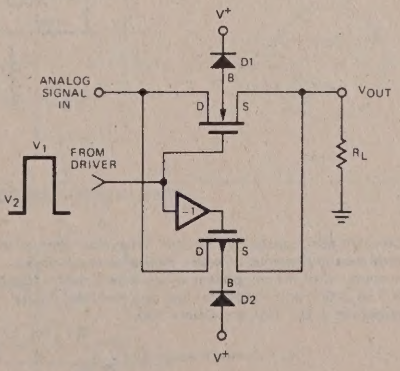
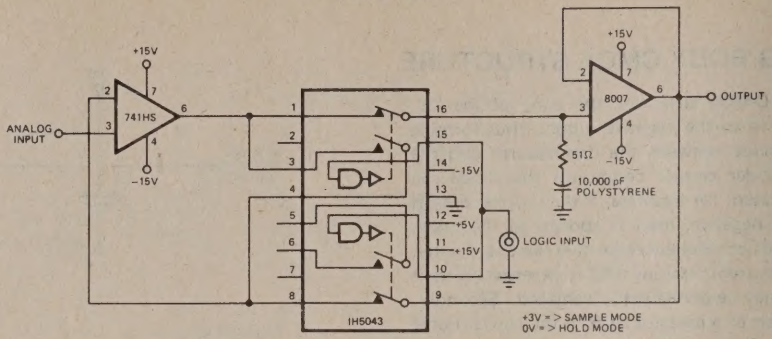


FIGURE L

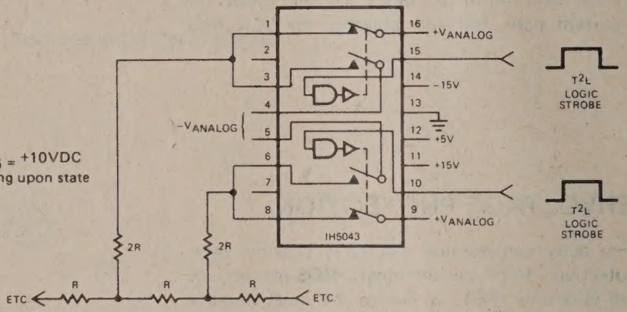
APPLICATIONS

IMPROVED SAMPLE & HOLD USING IH5043

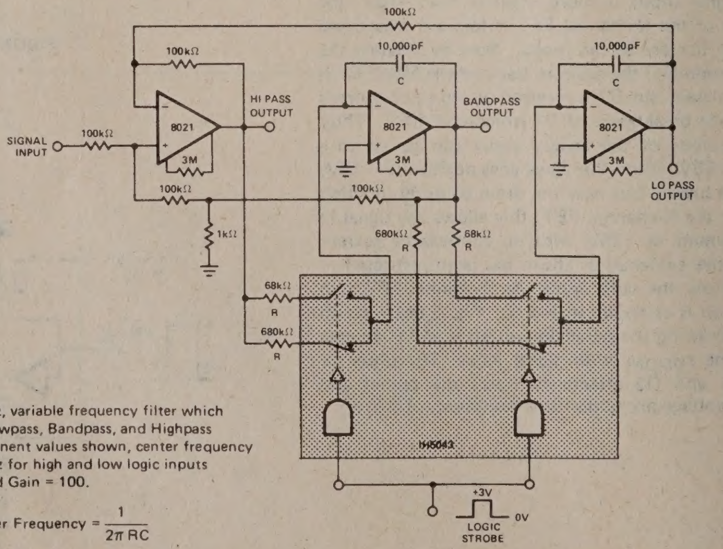

+15V
741HS
ANALOG INPUT
−15V
IH5043
+15V
8007
OUTPUT
51Ω
−15V
10,000 pF POLYSTYRENE
−15V
+5V
+15V
LOGIC INPUT
+3V = > SAMPLE MODE
0V = > HOLD MODE

USING THE CMOS SWITCH TO DRIVE AN R/2R LADDER NETWORK (2 LEGS)

EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.


+VANALOG
−15V
−VANALOG
+5V
+15V
+VANALOG
IH5043
T2L LOGIC STROBE
T2L LOGIC STROBE
2R
2R
R
R
R
ETC.
ETC.

DIGITALLY TUNED LOW POWER ACTIVE FILTER


100kΩ
100kΩ
10,000pF
C
10,000pF
C
HI PASS OUTPUT
BANDPASS OUTPUT
LO PASS OUTPUT
SIGNAL INPUT
100kΩ
8021
8021
8021
3M
3M
3M
100kΩ
100kΩ
1kΩ
680kΩ R
68kΩ R
68kΩ R
680kΩ R
IH5043
+3V
0V
LOGIC STROBE

Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

SWITCHING STATE DIAGRAMS

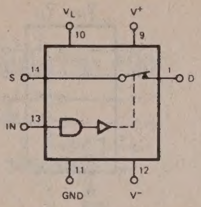
SWITCH STATES ARE FOR LOGIC "1" INPUT

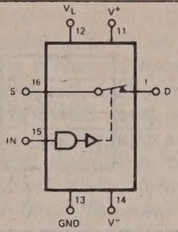
(OUTLINE DWG FE-2)

(OUTLINE DWGS DE, JE, PE)

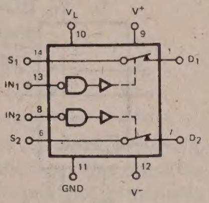
(OUTLINE DWG TO-100)

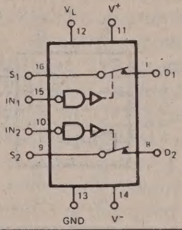
SPST
IH5040 ($r_{DS(on)} < 75\Omega$)

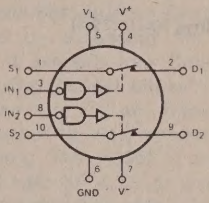

VL
V+
10
9
S
11
1
D
IN
13
11
12
GND
V−


VL
V+
12
11
S
16
1
D
IN
15
13
14
GND
V−

DUAL SPST
IH5041 ($r_{DS(on)} < 75\Omega$)

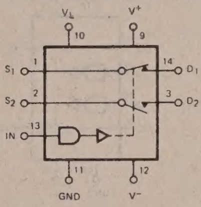

VL
V+
10
9
S1
14
1
D1
IN1
13
IN2
8
S2
6
7
D2
11
12
GND
V−

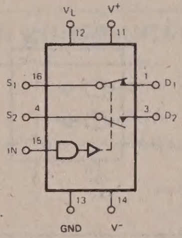

VL
V+
12
11
S1
16
1
D1
IN1
15
IN2
10
S2
9
8
D2
13
14
GND
V−

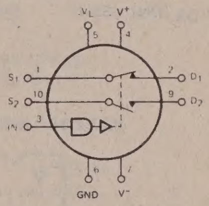

VL
V+
5
4
S1
1
2
D1
IN1
3
IN2
8
S2
10
9
D2
6
7
GND
V−

SPDT
IH5042 ($r_{DS(on)} < 75\Omega$)

(DG188 EQUIVALENT)

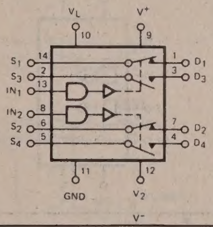

VL
V+
10
9
S1
1
14
D1
S2
2
3
D2
IN
13
11
12
GND
V−

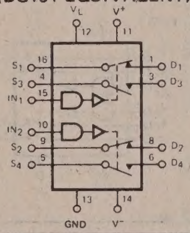

VL
V+
12
11
S1
16
1
D1
S2
4
3
D2
IN
15
13
14
GND
V−


VL
V+
5
4
S1
1
2
D1
S2
10
9
D2
IN
3
6
7
GND
V−

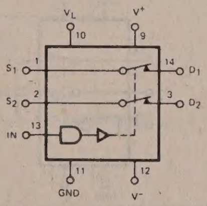
DUAL SPDT
IH5043 ($r_{DS(on)} < 75\Omega$)

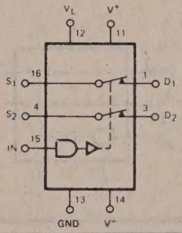
(DG191 EQUIVALENT)

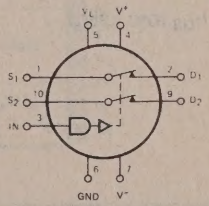

VL
V+
10
9
S1
14
1
D1
S3
2
3
D3
IN1
13
IN2
8
S2
6
7
D2
S4
5
4
D4
11
12
GND
V2
V−


VL
V+
12
11
S1
16
1
D1
S3
4
3
D3
IN1
15
IN2
10
S2
9
8
D2
S4
5
6
D4
13
14
GND
V−

DPST
IH5044 ($r_{DS(on)} < 75\Omega$)

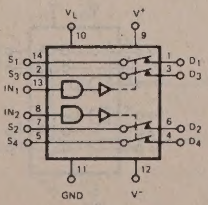

VL
V+
10
9
S1
1
14
D1
S2
2
3
D2
IN
13
11
12
GND
V−

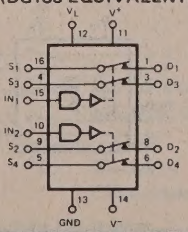

VL
V+
12
11
S1
16
1
D1
S2
4
3
D2
IN
15
13
14
GND
V−


VL
V+
5
4
S1
1
2
D1
S2
10
9
D2
IN
3
6
7
GND
V−

DUAL DPST
IH5045 ($r_{DS(on)} < 75\Omega$)

(DG185 EQUIVALENT)


VL
V+
10
9
S1
14
1
D1
S3
2
3
D3
IN1
13
IN2
8
S2
7
6
D2
S4
5
4
D4
11
12
GND
V−

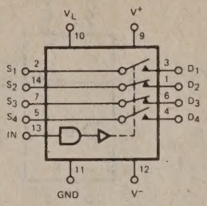

VL
V+
12
11
S1
16
1
D1
S3
4
3
D3
IN1
15
IN2
10
S2
9
8
D2
S4
5
6
D4
13
14
GND
V−

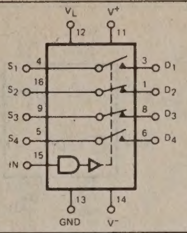
SWITCHING STATE DIAGRAMS (Cont.)

SWITCH STATES
ARE FOR LOGIC "1" INPUT

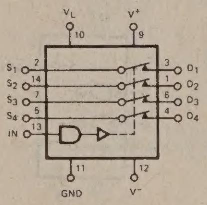
FLAT PACKAGE (FD) DIP (DE) PACKAGE TO-100

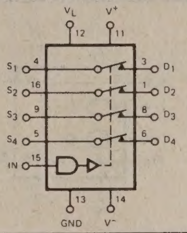
DPDT
IH5046 (r_{DS} (ON) <75Ω)


VL
V+
10
9
S1 2
S2 14
S3 7
S4 5
IN 13
3 D1
1 D2
6 D3
4 D4
11
12
GND
V−

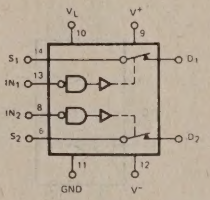

VL
V+
12
11
S1 4
S2 16
S3 9
S4 5
IN 15
3 D1
1 D2
8 D3
6 D4
13
14
GND
V−

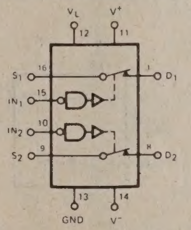
4PST
IH5047 (r_{DS} (ON) <75Ω)

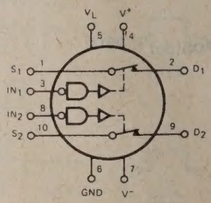

VL
V+
10
9
S1 2
S2 14
S3 7
S4 5
IN 13
3 D1
1 D2
6 D3
4 D4
11
12
GND
V−


VL
V+
12
11
S1 4
S2 16
S3 9
S4 5
IN 15
3 D1
1 D2
8 D3
6 D4
13
14
GND
V−

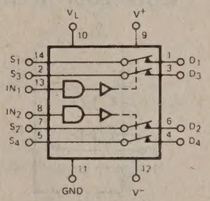
DUAL SPST
IH5048 (r_{DS} (ON) <35Ω)


VL
V+
10
9
S1 14
IN1 13
IN2 8
S2 6
D1
D2
11
12
GND
V−

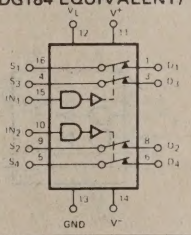

VL
V+
12
11
S1 16
IN1 15
IN2 10
S2 9
1 D1
8 D2
13
14
GND
V−


VL
V+
5
4
S1 1
IN1 3
IN2 8
S2 10
2 D1
9 D2
6
7
GND
V−

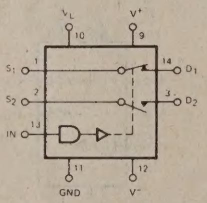
DUAL DPST
IH5049 (r_{DS} (ON) <35Ω)

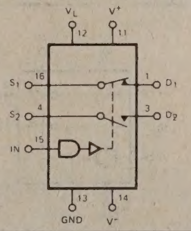

VL
V+
10
9
S1 14
S3 2
IN1 13
IN2 8
S2 7
S4 5
1 D1
3 D3
6 D2
4 D4
11
12
GND
V−

(DG184 EQUIVALENT)

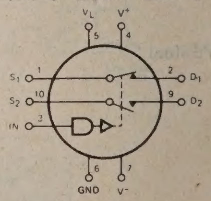

VL
V+
12
11
S1 16
S3 4
IN1 15
IN2 10
S2 9
S4 5
1 D1
3 D3
8 D2
6 D4
13
14
GND
V−

SPDT
IH5050 (r_{DS} (ON) <35Ω)

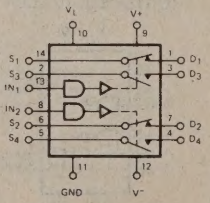

VL
V+
10
9
S1 1
S2 2
IN 13
14 D1
3 D2
11
12
GND
V−


VL
V+
12
11
S1 16
S2 4
IN 15
1 D1
3 D2
13
14
GND
V−

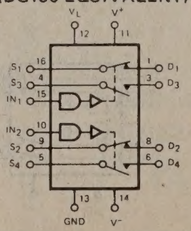
(DG187 EQUIVALENT)


VL
V+
5
4
S1 1
S2 10
IN 3
2 D1
9 D2
6
7
GND
V−

DUAL SPDT
IH5051 (r_{DS} (ON) <35Ω)


VL
V+
10
9
S1 14
S3 2
IN1 13
IN2 8
S2 6
S4 5
1 D1
3 D3
7 D2
4 D4
11
12
GND
V−

(DG190 EQUIVALENT)


VL
V+
12
11
S1 16
S3 4
IN1 15
IN2 10
S2 9
S4 5
1 D1
3 D3
8 D2
6 D4
13
14
GND
V−

INTERSIL

IH5052/IH5053
CMOS Analog Gates

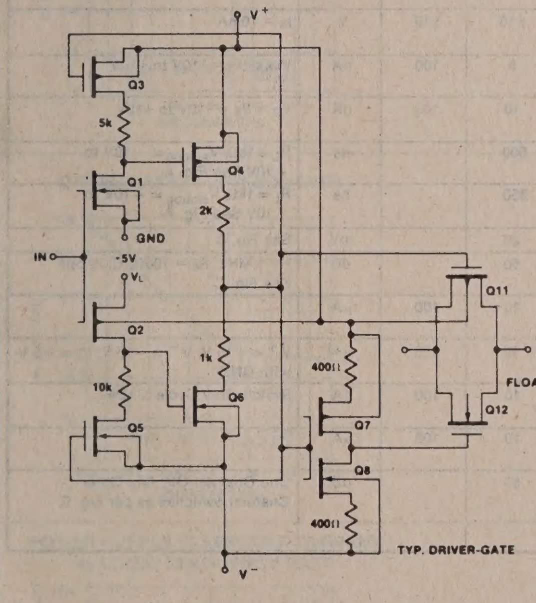
FEATURES

- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 10μA**
- **Overvoltage Protection to ±25V**
- **Break-Before-Make Switching t_{off} 100nsec, t_{on} 250nsec Typical**
- **T²L, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **IH5052 4 Normally Closed Switches**
- **IH5053 4 Normally Open Switches**

GENERAL DESCRIPTION

The IH5052/3 solid state analog gates are designed using an improved, high voltage CMOS technology. This provides ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and the destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The INTERSIL CMOS technology has eliminated this serious systems problem. Key performance advantages are TTL compatible and ultra low-power operation. The quiescent current requirement is less than 10μA. Also designed into the IH5052/3 is guaranteed Break-Before-Make switching. This is logically accomplished by extending the t_{ON} time (400nsec TYP.) such that it exceeds t_{OFF} time (200nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON and eliminates the need for external logic required to avoid channel to channel shorting during switching. The IH5052 is designed to have switch closure with Logic "0" (0.8V or less) and the IH5053 is designed to close switches with a Logical "1" (2.4V or more).

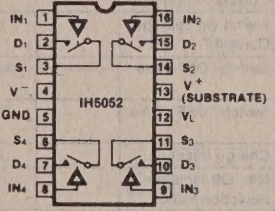
FUNCTIONAL DIAGRAM


V+
Q3
5k
Q1
Q4
2k
GND
IN
-5V
VL
Q2
Q11
1k
400Ω
10k
Q6
FLOATS
Q12
Q5
Q7
Q8
400Ω
TYP. DRIVER-GATE
V−

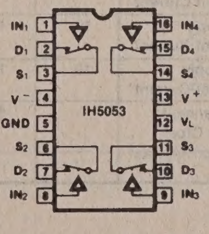
PIN CONFIGURATIONS

OUTLINE DWGS
DE, JE

DUAL-IN-LINE PACKAGE


IN₁ 1
D₁ 2
S₁ 3
V⁻ 4
GND 5
S₄ 6
D₄ 7
IN₄ 8
IH5052
16 IN₂
15 D₂
14 S₂
13 V+ (SUBSTRATE)
12 VL
11 S₃
10 D₃
9 IN₃

SWITCH STATES ARE
FOR LOGIC "1" INPUT


IN₁ 1
D₁ 2
S₁ 3
V⁻ 4
GND 5
S₂ 6
D₂ 7
IN₂ 8
IH5053
16 IN₄
15 D₄
14 S₄
13 V+
12 VL
11 S₃
10 D₃
9 IN₃

ORDERING INFORMATION

IH505X C JE

Package JE = 16-Pin CERDIP
DE = 16-Pin Ceramic DIP (Special Order Only)

Temperature Range
M = Military
C = Commercial

Basic Part Number

MAXIMUM RATINGS

Current (Any Terminal)	<30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board)	
Derate 6 mW/°C Above 70°C	
Lead Temperature (Soldering, 10 sec)	300°C

$V^+ - V^-$	<33V
$V^+ - V_D$	<30V
$V_D - V^-$	<30V
$V_D - V_S$	< ±22V
$V_L - V^-$	<33V
$V_L - V_{IN}$	<30V
V_L-GND	<20V
V_{IN}-GND	<20V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, GND = 0V)

PER CHANNEL		MIN./MAX. LIMITS							TEST CONDITIONS
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4V (IH5053) = 0.8V (IH5052)
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8V (IH5053) = 2.4V (IH5052)
$r_{DS(ON)}$	Drain-Source On Resistance	75	75	100	80	80	100	Ω	I_S = 1mA, V_{analog} = −10V to +10V
$\Delta r_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1 mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±11	±11	±11	±10	±10	±10	V	I_S = 10mA
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	V_{ANALOG} = −10V to +10V
$I_{D(ON)}$ $+I_{S(ON)}$	Switch On Leakage Current	2	2	200	10	10	100	nA	$V_D = V_S$ = −10V to +10V
t_{ON}	Switch "ON" Time		500			500		ns	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. A
t_{OFF}	Switch "OFF" Time		250			250		ns	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤ 5pF See Fig. C
I^+	+ Power Supply Quiescent Curent	10	10	100	10	10	100	μA	
I^-	− Power Supply Quiescent Current	10	10	100	10	10	100	μA	$V^+ = +15$ V, $V^- = -15$ V, $V_L = +5$ V with GND
I_{VL}	+5V Supply Quiescent Current	10	10	100	10	10	100	μA	Switch Duty Cycle ≤ 10%
I_{GND}	Gnd Supply Quiescent Current	10	10	100	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches as per Fig. E

TEST CIRCUITS

FIG. A

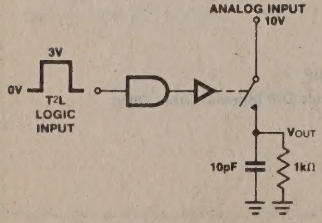


FIG. B

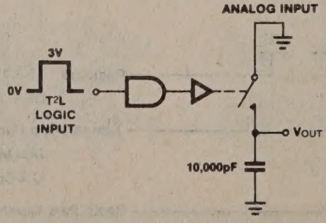
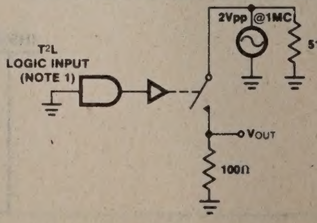


FIG. C



TYPICAL ELECTRICAL CHARACTERISTICS (Per Channel)

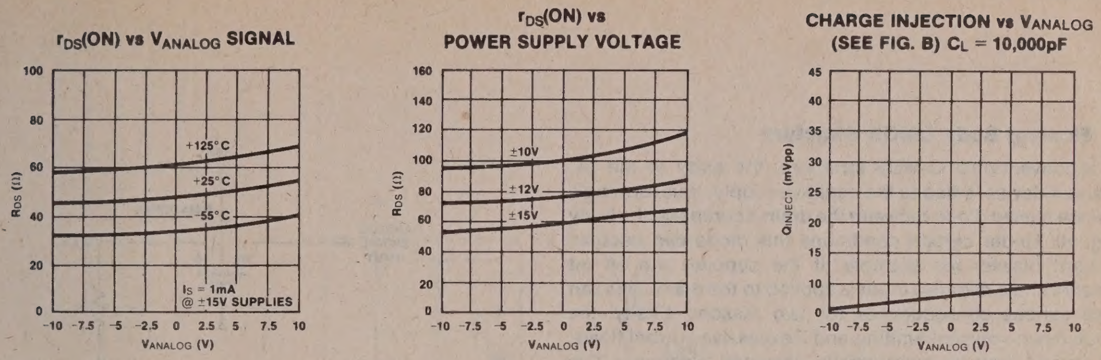
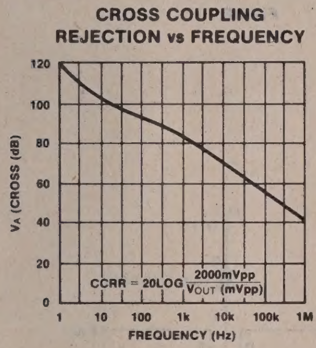


FIGURE D



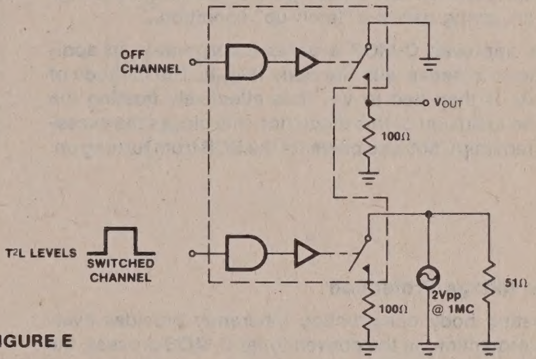
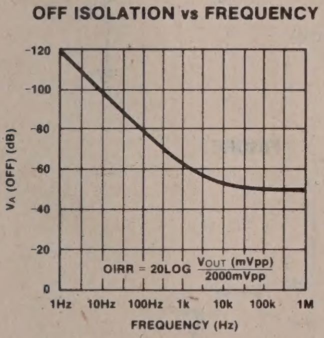

OFF
CHANNEL
V_{OUT}
100Ω
T²L LEVELS
SWITCHED
CHANNEL
51Ω
2Vpp
@ 1MC
100Ω

FIGURE E



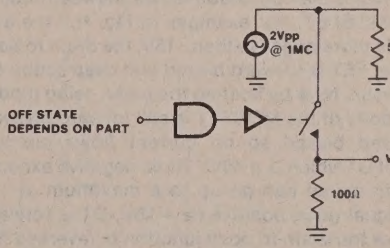
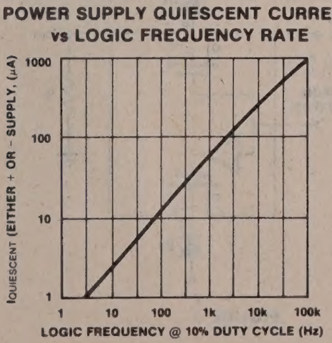

2Vpp
@ 1MC
51Ω
OFF STATE
DEPENDS ON PART
V_{OUT}
100Ω

FIGURE F



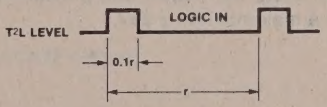

T²L LEVEL
LOGIC IN
0.1r
r

FIGURE G

THEORY OF OPERATION

A. Floating Body CMOS Structure

In a conventional C-MOS structure, the body of the "n" channel device is tied to the negative supply, thus forming a reverse biased diode between the drain/source and the body (Fig. H). Under certain conditions this diode can become forward biased; for example, if the supplies are off (at ground) and a negative input is applied to the drain. This can have serious consequences for two reasons. Firstly, the diode has no current limiting and if excessive current flows, the circuit may be permanently damaged. Secondly, this diode forms part of a parasitic SCR in the conventional C-MOS structure. Forward biasing the diode causes the SCR to turn on, giving rise to a "latch-up" condition.

Intersil's improved C-MOS process incorporates an additional diode in series with the body (Fig. I). The cathode of this diode is then tied to V+, thus effectively floating the body. The inclusion of this diode not only blocks the excessive current path, but also prevents the SCR from turning on.

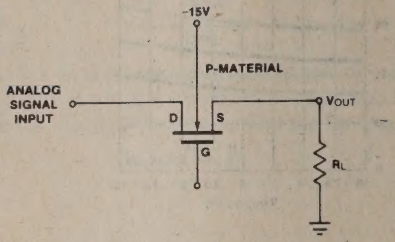


FIGURE H

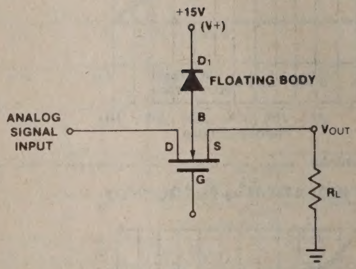


FIGURE I

B. Overvoltage Protection

The floating body construction inherently provides overvoltage protection. In the conventional C-MOS process, the body of all N-channel FETs is tied to the most negative power supply and the body of all P-channel devices to the most positive supply (i.e., ±15V). Thus, for an overvoltage spike of > ±15V, a forward bias condition exists between drain and body of the MOSFET. For example, in Fig. H if the analog signal input is more negative than −15V, the drain to body of the N-channel FET is forward biased and destruction of the device can result. Now by floating the body, using diode D1, the drain to body of the MOSFET is still forward biased, but D1 is reversed biased so no current flows (up to the breakdown of D1 which is ≥ 40V). Thus, negative excursions of the analog signal can go up to a maximum of −25V. When the signal goes positive (≥ +15V, D1 is forward biased, but now the drain to body junction is reversed for the N-channel FET; this allows the signal to go to a maximum of +25V with no appreciable current flow. While the explanation above has been restricted to N-channel devices, the same applies to P-channel FETs and the construction is as shown in Fig. J. Fig. J describes an output stage showing the paralleling of an N and P-channel to linearize the $r_{DS(on)}$ with signal input. The presence of diodes D1 and D2 effectively floats the bodies and provides overvoltage protection to a maximum of ±25V.

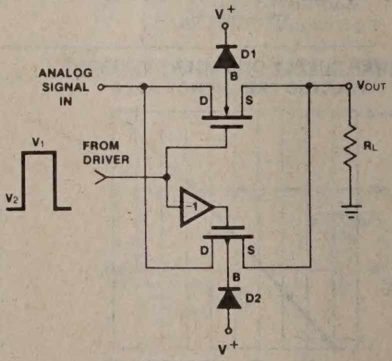
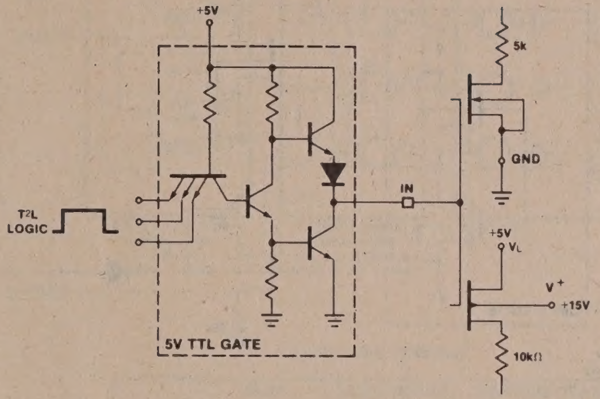
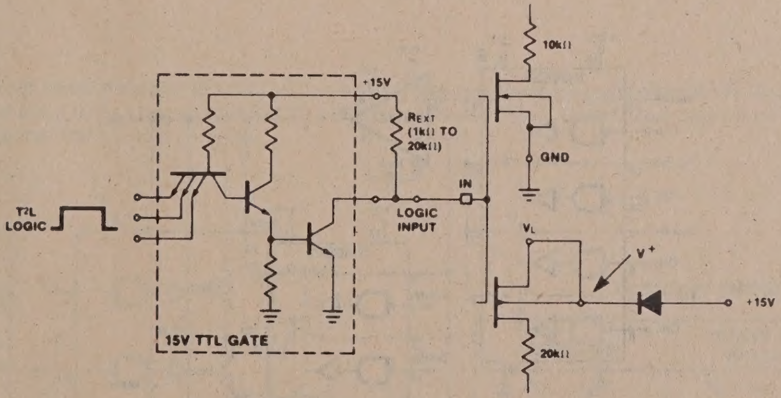


FIGURE J

LOGIC INTERFACING

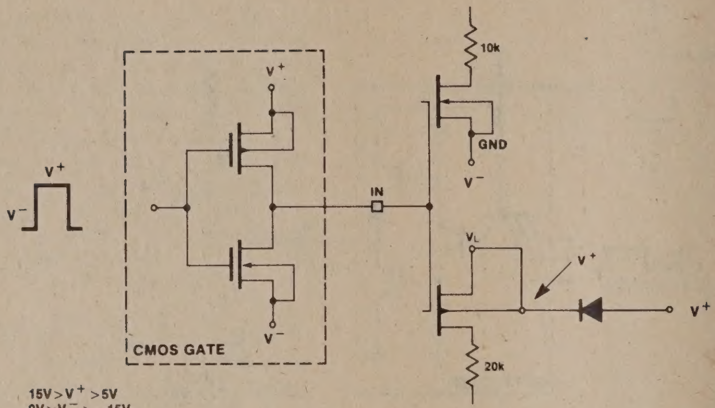

+5V
5k
GND
IN
T2L
LOGIC
+5V
VL
V+
+15V
10kΩ
5V TTL GATE

FOR INTERFACING WITH T2L OPEN COLLECTOR LOGIC.


+15V
REXT
(1kΩ TO
20kΩ)
10kΩ
GND
IN
T2L
LOGIC
LOGIC
INPUT
VL
V+
+15V
20kΩ
15V TTL GATE

TYP. EXAMPLE FOR +15V CASE SHOWN

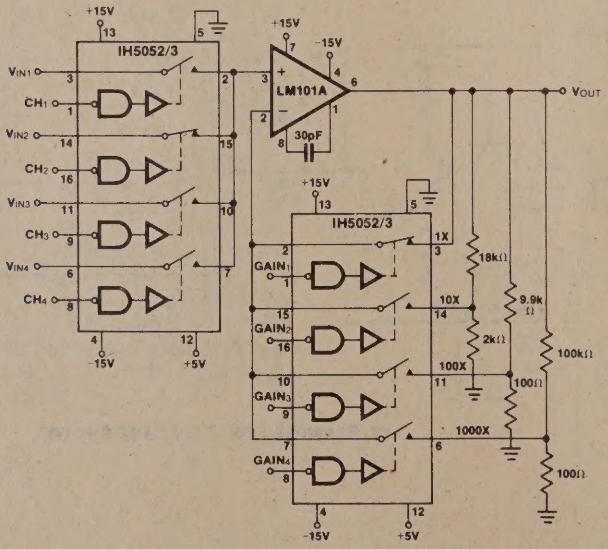
FOR USE WITH CMOS LOGIC.


V+
V−
V+
V−
CMOS GATE
IN
10k
GND
V−
VL
V+
V+
20k

15V > V+ > 5V
0V > V− > −15V

APPLICATIONS

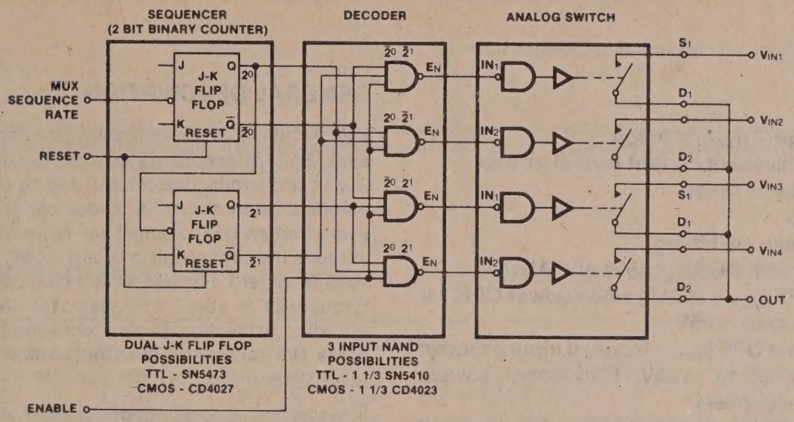
PROGRAMMABLE GAIN NON-INVERTING AMPLIFIER WITH SELECTABLE INPUTS


+15V
13
5
IH5052/3
VIN1
3
CH1
1
VIN2
14
CH2
16
VIN3
11
CH3
9
VIN4
6
CH4
8
2
15
10
7
4
−15V
12
+5V
+15V
7
−15V
4
3
+
LM101A
6
2
−
1
8
30pF
VOUT
+15V
13
5
IH5052/3
2
GAIN1
1
1X
3
15
GAIN2
16
10X
14
10
GAIN3
9
100X
11
7
GAIN4
8
1000X
6
4
−15V
12
+5V
18kΩ
2kΩ
9.9kΩ
100Ω
100kΩ
100Ω

ACTIVE LOW PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY

APPLICATIONS (Continued)

4-CHANNEL SEQUENCING MUX

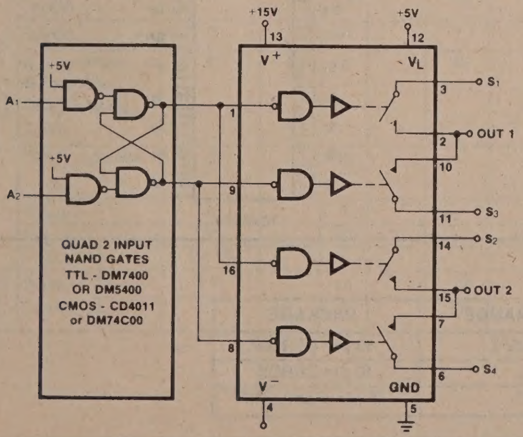

SEQUENCER
(2 BIT BINARY COUNTER)
DECODER
ANALOG SWITCH
MUX SEQUENCE RATE
RESET
ENABLE
J-K FLIP FLOP
J
K
Q
RESET
2^0
$\overline{2^0}$
2^1
$\overline{2^1}$
EN
IN_1
IN_2
S_1
D_1
D_2
V_{IN1}
V_{IN2}
V_{IN3}
V_{IN4}
OUT
DUAL J-K FLIP FLOP POSSIBILITIES
TTL - SN5473
CMOS - CD4027
3 INPUT NAND POSSIBILITIES
TTL - 1 1/3 SN5410
CMOS - 1 1/3 CD4023

Truth Table (IH5052)

ENABLE	MUX SEQUENCE RATE	SEQUENCER OUTPUT 2^0	SEQUENCER OUTPUT 2^1	SWITCH STATES (– DENOTES OFF) SW1	SW2	SW3	SW4
0	0	0	0	—	—	—	—
1	0	0	0	ON	—	—	—
1	1 pulse	1	0	—	ON	—	—
1	2 pulses	0	1	—	—	—	—
1	3 pulses	1	1	—	—	—	ON
1	4 pulses	0	0	ON	—	—	—

A Latching DPDT

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_2 turns S_1 and S_2 ON, a HIGH to A_1 turns S_3 and S_4 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.


+15V
+5V
13
12
V^+
V_L
+5V
A_1
A_2
1
9
16
8
3
2
10
11
14
15
7
6
S_1
OUT 1
S_3
S_2
OUT 2
S_4
V^-
GND
4
5
QUAD 2 INPUT NAND GATES
TTL - DM7400 OR DM5400
CMOS - CD4011 or DM74C00

Truth Table (IH5052)

COMMAND A_2	COMMAND A_1	STATE OF SWITCHES AFTER COMMAND S_3 & S_4	S_1 & S_2
0	0	same	same
0	1	on	off
1	0	off	on
1	1	INDETERMINATE	

IH5108

8-Channel Fault Protected CMOS Analog Multiplexer

FEATURES

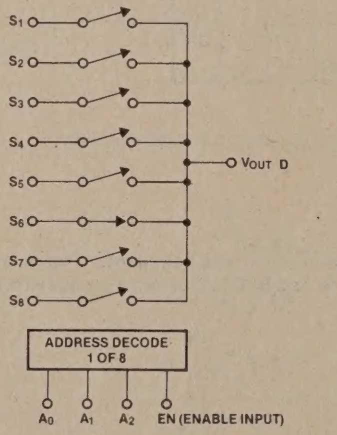
- Ultra low leakage — $I_{D(off)} \leq 100pA$
- Power supply quiescent current less than 1mA
- ±13V analog signal range
- No SCR latchup
- Break-before-make switching
- Pin compatible with DG508, HI508 and AD7508
- All channels OFF ($I_{ILK} \leq 100nA$) when power OFF, for analog signals up to ±25V
- Any channel turns OFF ($I_{ILK} \leq 100nA$) if input exceeds supply rails by up to ±25V. Throughput always < ±14V (±15V supplies)
- TTL and CMOS compatible binary address and enable inputs

GENERAL DESCRIPTION

The IH5108 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the DG508 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 3-bit address code together with the ENable input allows selection of any one channel or none at all. These 4 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

FUNCTIONAL DIAGRAM



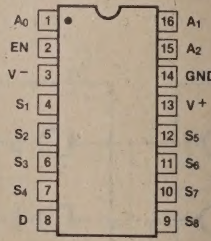
3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN HI
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (Outline drawing JE, PE)



TOP VIEW

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5108MJE	−55°C to +125°C	16 pin CERDIP
IH5108CJE	0°C to 70°C	16 pin CERDIP
IH5108CPE	0°C to 70°C	16 pin plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground . . . . −15V to 15V
V_S or V_D to V^+ . . . . +25V, −40V
V_S or V_D to V^- . . . . −25V, +40V
V^+ to Ground 16V
V^- to Ground . . . . −16V
Current (Any Terminal) 20mA

Operating Temperature . . . . −55 to 125°C
Storage Temperature . . . . −65 to 150°C
Power Dissipaton (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS						UNIT	TEST CONDITIONS	
					M SUFFIX			C SUFFIX					
					−55°C	25°C	125°C	0°C	25°C	70°C			
SWITCH	$r_{DS(on)}$	S to D	8	700	1000	1000	1500	1200	1200	1800	Ω	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on
			8	500	1000	1000	1500	1200	1200	1800		$V_D = -10V$ $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(on)}$			5							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(off)}$	S	8	0.002		0.05	50		0.1	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
			8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(off)}$	D	1	0.03		0.1	100		0.2	100		$V_D = 10V$, $V_S = -10V$	
			1	0.03		0.1	100		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(on)}$	D	8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
			8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
FAULT	I_S with Power OFF	S	8	1	10	10	1000	50	50	5000	nA	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, A_0, A_1, $A_2 = 0V$,or 5V	
	I_S with Overvoltage	S	8	1	10	10	1000	50	50	5000		$V_{IN} = \pm 25V$, $V_O = \pm 10V$	
IN	$I_{EN(on)}$ $I_{A(on)}$ or	A_0, A_1, A_2, or	4	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
	$I_{EN(off)}$ $I_{A(off)}$	EN	4	.01		10	30		10	30		$V_A = 15V$ or 0V	
DYNAMIC	$t_{transition}$	D		0.3		1					μs	See Figure 1	
	t_{open}	D		0.2								See Figure 2	
	$t_{on(EN)}$	D		0.6		1.5						See Figure 3	
	$t_{off(EN)}$	D		0.4		1							
	t_{on}−t_{off} Break-Before-Make Delay Settling Time	D	8	50		25			10		ns	$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, Figure 4	
	"OFF" Isolation	D		60							dB	$V_{EN} = 0$, $R_L = 200Ω$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 KHz	
	$C_{S(off)}$	S		5							pF	$V_S = 0$	$V_{EN} = 0V$, f = 140 KHz to 1 MHz
	$C_{D(off)}$	D		25								$V_D = 0$	
	$C_{DS(off)}$	D to S		1								$V_S = 0$, $V_D = 0$	
SUPP	Supply Current +	I^+	1	40		200			1000		μA	All V_A, $V_{EN} = 0.15V$	
	Supply Current −	I^-	1	2		100			1000				

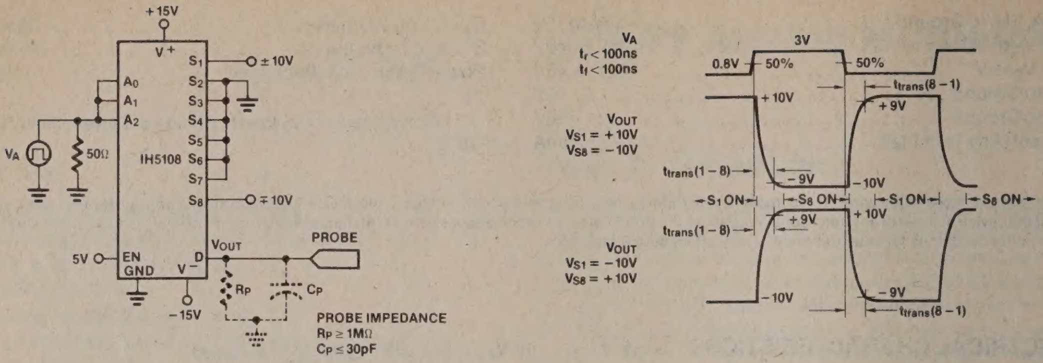

+15V
V+
S1
S2
S3
S4
S5
S6
S7
S8
± 10V
∓ 10V
A0
A1
A2
VA
50Ω
IH5108
5V
EN
GND
V−
D
−15V
VOUT
PROBE
RP
CP
PROBE IMPEDANCE
RP ≥ 1MΩ
CP ≤ 30pF
VA
tr < 100ns
tf < 100ns
3V
0.8V
50%
50%
VOUT
VS1 = +10V
VS8 = −10V
+10V
+9V
−9V
−10V
ttrans(8 − 1)
ttrans(1 − 8)
S1 ON
S8 ON
S1 ON
S8 ON
+10V
+9V
VOUT
VS1 = −10V
VS8 = +10V
−10V
−9V
ttrans(1 − 8)
ttrans(8 − 1)

Figure 1. $t_{transition}$ Switching Test

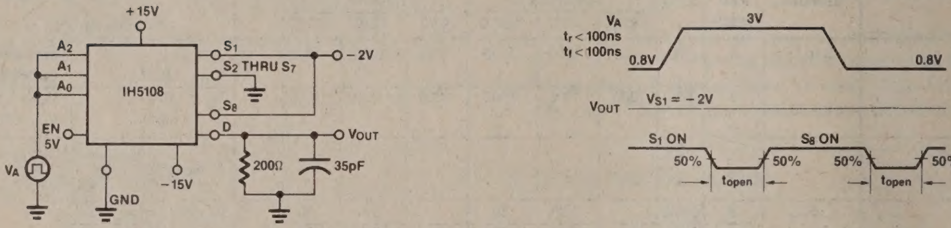

+15V
A2
A1
A0
S1
S2 THRU S7
−2V
S8
D
VOUT
IH5108
EN
5V
VA
200Ω
35pF
−15V
GND
VA
tr < 100ns
tf < 100ns
3V
0.8V
0.8V
VOUT
VS1 = −2V
S1 ON
S8 ON
50%
50%
50%
50%
topen
topen

Figure 2. t_{open} (Break-Before-Make) Switching Test

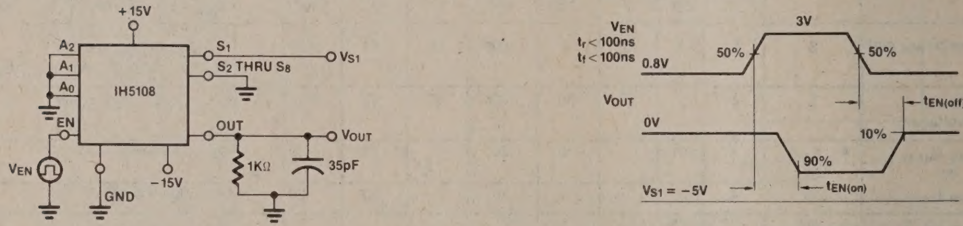

+15V
A2
A1
A0
S1
S2 THRU S8
VS1
IH5108
EN
OUT
VOUT
VEN
1KΩ
35pF
−15V
GND
VEN
tr < 100ns
tf < 100ns
3V
0.8V
50%
50%
VOUT
0V
tEN(off)
10%
90%
VS1 = −5V
tEN(on)

Figure 3. t_{on} and t_{off} Switching Test

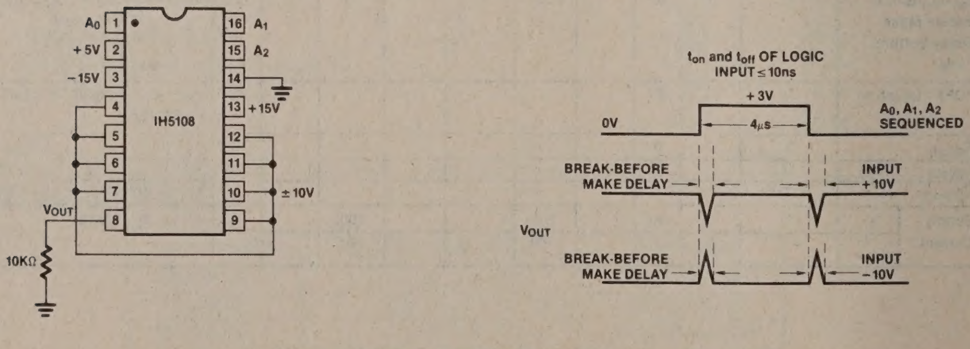

A0
1
+5V
2
−15V
3
4
5
6
7
VOUT
8
16
A1
15
A2
14
13
+15V
12
11
10
9
± 10V
IH5108
10KΩ
ton and toff OF LOGIC INPUT ≤ 10ns
+3V
0V
4μs
A0, A1, A2 SEQUENCED
BREAK-BEFORE MAKE DELAY
INPUT +10V
VOUT
BREAK-BEFORE MAKE DELAY
INPUT −10V

Figure 4. Break-Before-Make Delay Test

DETAILED DESCRIPTION

The IH5108, like all Intersil's multiplexers, contains a set of CMOS switches forming the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5108 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special treatment that many multiplexer enable inputs require for proper logic swings. This identical circuit treatment of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important, difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches, and while this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5108 uses a novel series arrangement of the p- and n-channel switches (Figure 5) combined with a dielectrically isolated process to obviate these problems.

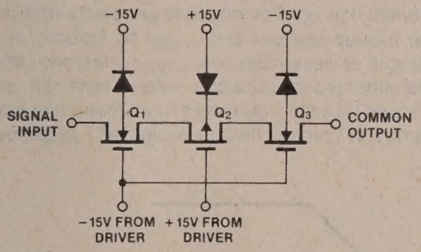
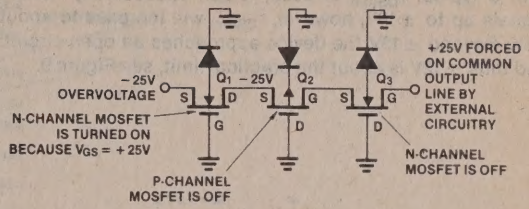

−15V
+15V
−15V
SIGNAL INPUT
Q1
Q2
Q3
COMMON OUTPUT
−15V FROM DRIVER
+15V FROM DRIVER

Figure 5. Series Connection of Channel Switches

Within the normal analog signal band, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 6). Thus protection is provided to any input or output channel against overvoltage on any (or several) input or output channels even in the absence of multiplexer supply voltages, and applies up to the breakdown voltage of the respective switches, drawing only leakage currents. Figure 7 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 8).

(a) OVERVOLTAGE WITH MUX POWER OFF


−25V OVERVOLTAGE
Q1
−25V
Q2
Q3
S
D
S
G
S
G
G
D
D
+25V FORCED ON COMMON OUTPUT LINE BY EXTERNAL CIRCUITRY
N-CHANNEL MOSFET IS TURNED ON BECAUSE V_{GS} = +25V
P-CHANNEL MOSFET IS OFF
N-CHANNEL MOSFET IS OFF

(b) OVERVOLTAGE WITH MUX POWER ON

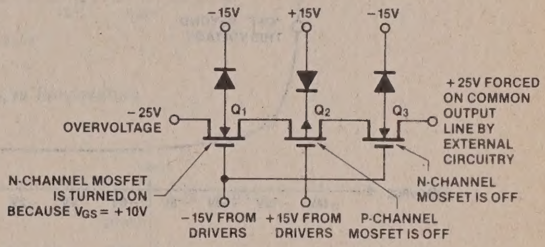

−15V
+15V
−15V
−25V OVERVOLTAGE
Q1
Q2
Q3
+25V FORCED ON COMMON OUTPUT LINE BY EXTERNAL CIRCUITRY
N-CHANNEL MOSFET IS TURNED ON BECAUSE V_{GS} = +10V
−15V FROM DRIVERS
+15V FROM DRIVERS
P-CHANNEL MOSFET IS OFF
N-CHANNEL MOSFET IS OFF

Figure 6. Overvoltage Protection

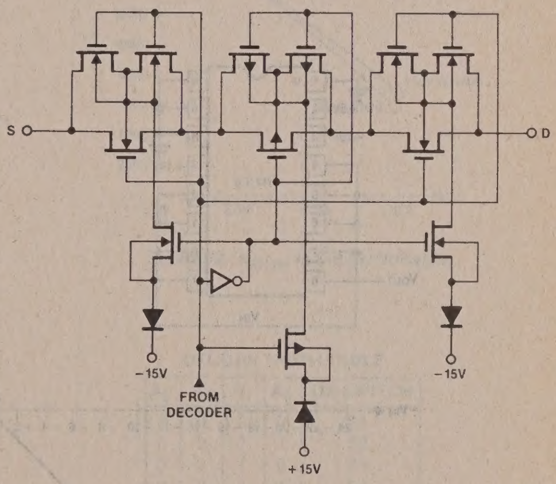

S
D
−15V
−15V
FROM DECODER
+15V

Figure 7. Detailed Channel Switch Schematic

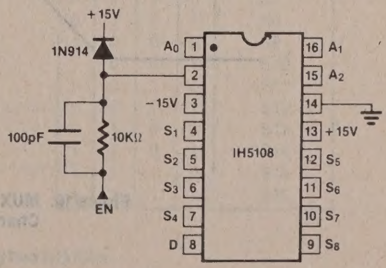

+15V
1N914
100pF
10KΩ
EN
A0 1
2
−15V 3
S1 4
S2 5
S3 6
S4 7
D 8
IH5108
16 A1
15 A2
14
13 +15V
12 S5
11 S6
10 S7
9 S8

Figure 8. Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5108 is designed to handle signals in the ±10V range, with a typical $r_{DS(on)}$ of 600Ω; it can successfully handle signals up to ±13V, however, $r_{DS(on)}$ will increase to about 1.8K. Beyond ±13V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 9.

Figure 10 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 11 gives the ON resistance variation with temperature.

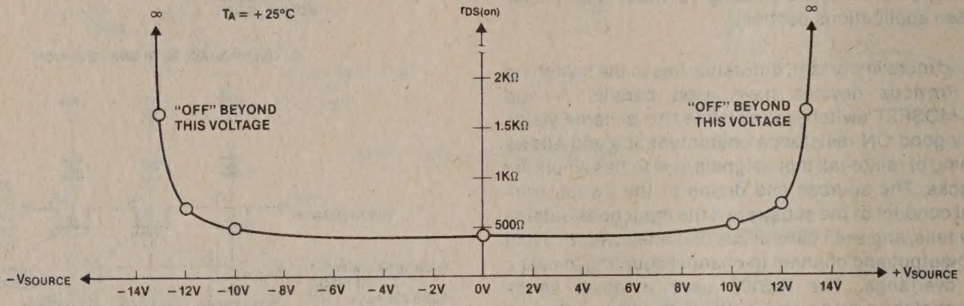


Figure 9. $r_{DS(on)}$ vs Signal Input Voltage @ $T_A = +25°C$

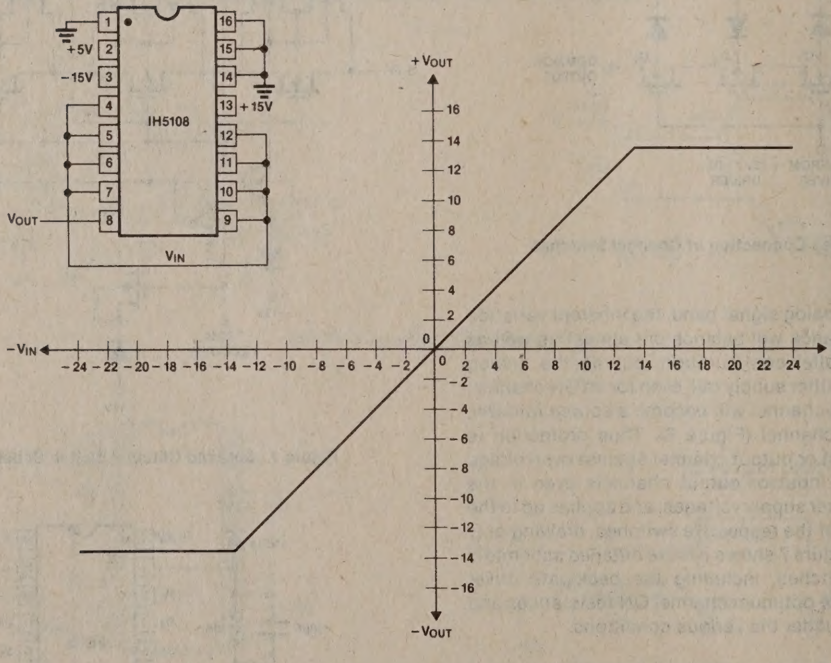


Figure 10. MUX Output Voltage vs Input Voltage
Channel 1 Shown; All Channels Similar

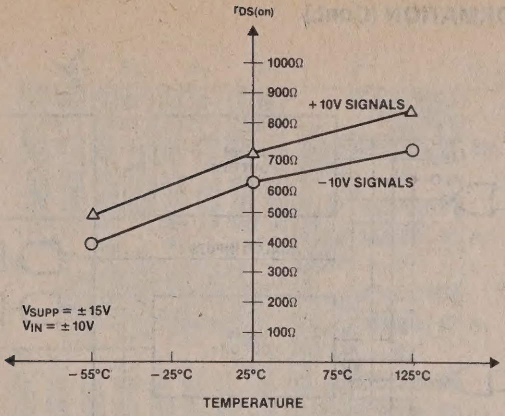


Figure 11. Typical $r_{DS(on)}$ vs Temperature

USING THE IH5108 WITH SUPPLIES OTHER THAN ±15V

The IH5108 will operate successfully with supply voltages from ±5V to ±15V; $r_{DS(on)}$ increases as supply voltage decreases, see Figure 12. Leakage currents, however, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic levels will remain TTL compatible.

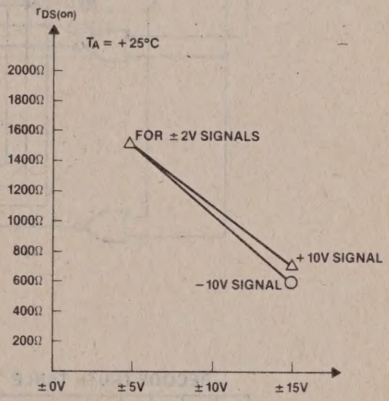
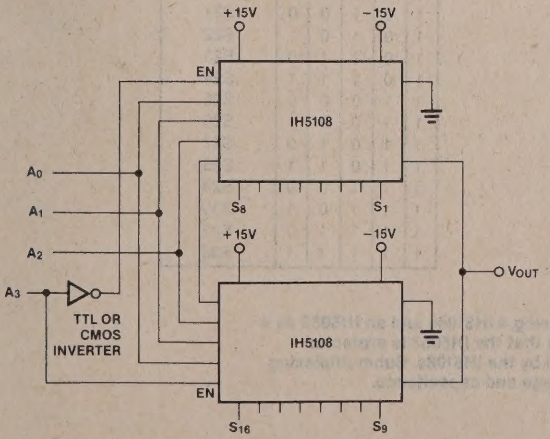


Figure 12. $r_{DS(on)}$ vs Supply Voltages

IH5108 APPLICATIONS INFORMATION

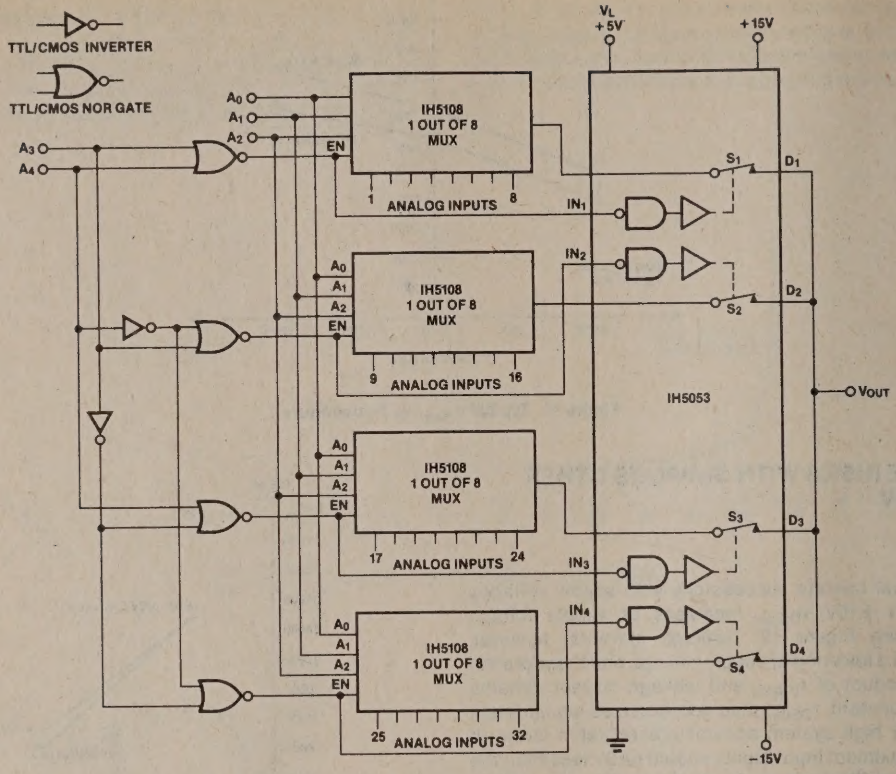


DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	S1
0	0	0	1	S2
0	0	1	0	S3
0	0	1	1	S4
0	1	0	0	S5
0	1	0	1	S6
0	1	1	0	S7
0	1	1	1	S8
1	0	0	0	S9
1	0	0	1	S10
1	0	1	0	S11
1	0	1	1	S12
1	1	0	0	S13
1	1	0	1	S14
1	1	1	0	S15
1	1	1	1	S16

Figure 13. 1 of 16 channel multiplexer using two IH5108s. Overvoltage protection is maintained between all channels, as is break-before-make switching.

IH5108 APPLICATIONS INFORMATION (Cont.)


TTL/CMOS INVERTER
TTL/CMOS NOR GATE
A_0
A_1
A_2
A_3
A_4
EN
IH5108
1 OUT OF 8
MUX
1 ANALOG INPUTS 8
9 ANALOG INPUTS 16
17 ANALOG INPUTS 24
25 ANALOG INPUTS 32
V_L +5V
+15V
−15V
IN_1
IN_2
IN_3
IN_4
S_1
S_2
S_3
S_4
D_1
D_2
D_3
D_4
IH5053
V_{OUT}

DECODE TRUTH TABLE

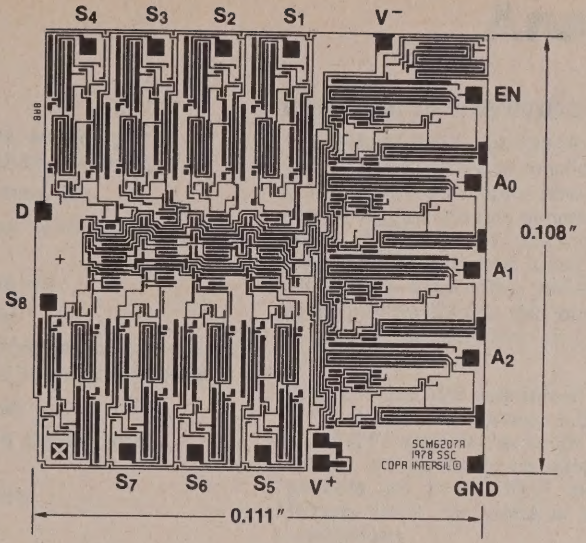
A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 14. 1 of 32 multiplexer using 4 IH5108s and an IH5053 as a submultiplexer. Note that the IH5053 is protected against overvoltages by the IH5108s. Submultiplexing reduces output leakage and capacitance.

CHIP TOPOGRAPHY


S_4
S_3
S_2
S_1
V^-
EN
A_0
0.108″
A_1
A_2
D
S_8
S_7
S_6
S_5
V^+
GND
0.111″
SCM6207A
1978 SSC
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NOTES:

3

INTERSIL

IH5140 Family High Level CMOS Analog Gates

FEATURES

- Super fast break before make switching t_{on} 80ns typ, t_{off} 50ns typ (SPST switches)
- Power supply currents less than 1μA
- OFF leakages less than 100pA @ 25°C guaranteed
- Non-latching with supply turn-off
- Single monolithic CMOS chip
- Plug-in replacements for IH5040 family and part of the DG180 family to upgrade speed and leakage
- Greater than 1MHz toggle rate
- Switches greater than 20Vp-p signals with ±15V supplies
- T^2L, CMOS direct compatibility

GENERAL DESCRIPTION

The IH5140 Family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to build the fastest switches now available. These switches can be toggled at a rate of greater than 1 MHz with super fast t_{on} times (80ns typical) and faster t_{off} times (50ns typical), guaranteeing break before make switching. This family of switches therefore combines the speed of the hybrid FET DG 180 Family with the reliability and low power consumption of a monolithic CMOS construction.

OFF leakages are guaranteed to be less than 100pA at 25°C. No quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 1μA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic gates. It is pin compatible with Intersil's IH5040 Family and part of the DG180/190 Family as shown in the switching state diagrams.

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range
IH5140 MJE	SPST	16 Pin CERDIP	-55°C to 125°C
IH5140 CJE	SPST	16 Pin CERDIP	0°C to 70°C
IH5140 CPE	SPST	16 Pin Plastic DIP	0°C to 70°C
IH5140 MFD	SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 MJE	Dual SPST	16 Pin CERDIP	-55°C to 125°C
IH5141 CJE	Dual SPST	16 Pin CERDIP	0°C to 70°C
IH5141 CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C
IH5141 MFD	Dual SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 CTW	Dual SPST	TO-100	0°C to 70°C
IH5141 MTW	Dual SPST	TO-100	-55°C to 125°C
IH5142 MJE	SPDT	16 Pin CERDIP	-55°C to 125°C
IH5142 CJE	SPDT	16 Pin CERDIP	0°C to 70°C
IH5142 CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5142 MFD	SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5142 CTW	SPDT	TO-100	0°C to 70°C
IH5142 MTW	SPDT	TO-100	-55°C to 125°C
IH5143 MJE	Dual SPDT	16 Pin CERDIP	-55°C to 125°C
IH5143 CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C
IH5143 CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5143 MFD	Dual SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5144 MJE	DPST	16 Pin CERDIP	-55°C to 125°C
IH5144 CJE	DPST	16 Pin CERDIP	0°C to 70°C
IH5144 CPE	DPST	16 Pin Plastic DIP	0°C to 70°C
IH5144 MFD	DPST	14 Pin Flat Pack	-55°C to 125°C
IH5144 CTW	DPST	TO-100	0°C to 70°C
IH5144 MTW	DPST	TO-100	-55°C to 125°C
IH5145 MJE	Dual DPST	16 Pin CERDIP	-55°C to 125°C
IH5145 CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C
IH5145 CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C
IH5145 MFD	Dual DPST	14 Pin Flat Pack	-55°C to 125°C

Note:
1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

FUNCTIONAL DIAGRAM

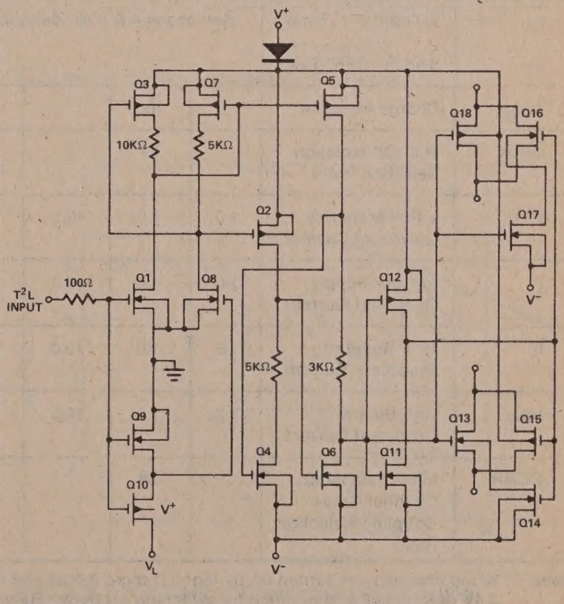


FIGURE 1. Typical Driver/Gate — IH5142

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) .... < 30 mA
Storage Temperature ...... -65°C to +150°C
Operating Temperature .... -55°C to +125°C
Power Dissipation .... 450 mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C
Lead Temperature (Soldering 10 sec.) .. 300°C

$V^+ - V^-$ <33V
$V^+ - V_D$ <30V
$V_D - V^-$ <30V
$V_D - V_S$ <±22V
$V_L - V^-$ <33V
$V_L - V_{IN}$ <30V
V_L <20V
V_{IN} <20V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
I_{INH}	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4$ V Note 1
I_{INL}	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8$ V Note 1
$r_{DS(on)}$	Drain—Source On Resistance	50	50	75	75	75	100	Ω	$I_S = -10$ mA $V_{ANALOG} = -10$ V to $+10$ V
$\Delta r_{DS(on)}$	Channel to Channel $r_{DS(on)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = -10 mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±11	±11	±11	±10	±10	±10	V	$I_S = 10$ mA
$I_{D(off)}^+$	Switch OFF Leakage	0.1	0.1	20	0.5	0.5	20	nA	$V_D = +10$ V, $V_S = -10$ V
$I_{S(off)}$	Current	0.1	0.1	20	0.5	0.5	20		$V_D = -10V$, $V_S = +10$ V
$I_{D(on)}^+$ $I_{S(on)}$	Switch On Leakage Current	0.2	0.2	40	1	1	40	nA	$V_D = V_S = -10$ V to $+10$ V
t_{on}	Switch "ON" Time	See pages 4 & 5 for switching time specifications and timing diagrams.							
t_{off}	Switch "OFF" Time								
$Q_{(INJ.)}$	Charge Injection		100			150		PC	See Fig. 4, Note 2
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, $R_L = 100\Omega$, $C_L \leq 5$ pF See Fig. 5, Note 2
I^+	+ Power Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	$V^+ = +15$ V, $V^- = -15$ V, $V_L = +5$ V Switch Duty Cycle < 10% See Fig. 6
I^-	- Power Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	
I_L	+5 V Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	
I_{GND}	Gnd Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches See Fig. 7, Note 2

Note: 1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.

2. Charge injection, OFF isolation, and Channel to Channel isolation are only sample tested in production.

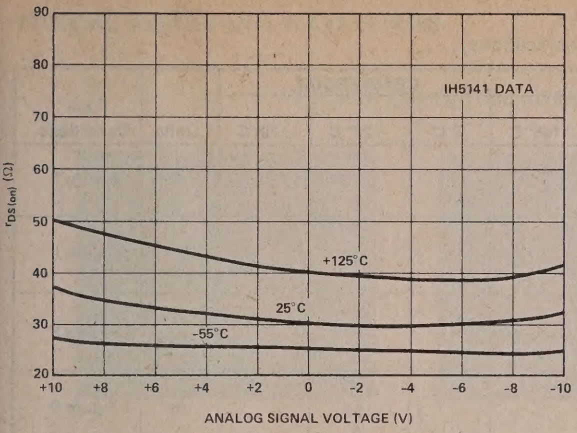


FIGURE 2. $r_{DS(on)}$ **vs. Temp., @ ±15V, +5V Supplies.**

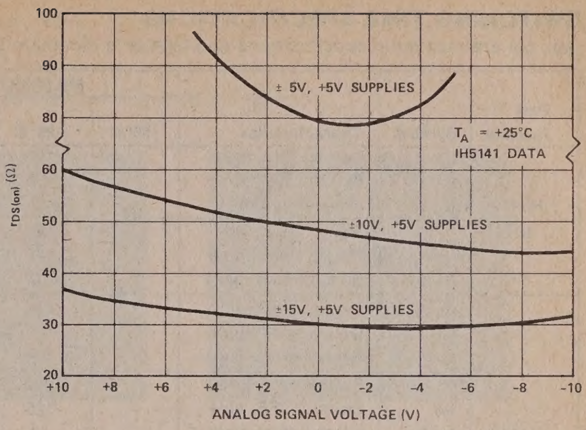


FIGURE 3. $r_{DS(on)}$ **vs. Power Supplies.**

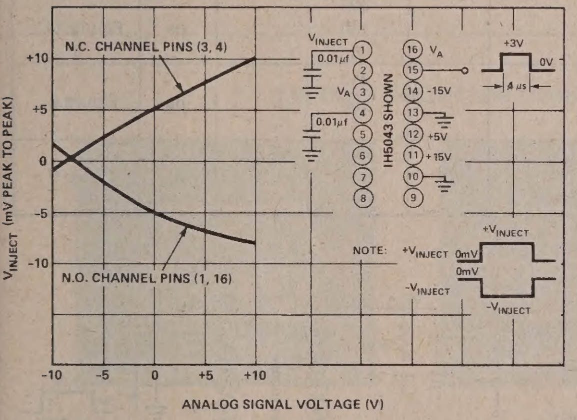


FIGURE 4. Charge Injection vs. Analog Signal.

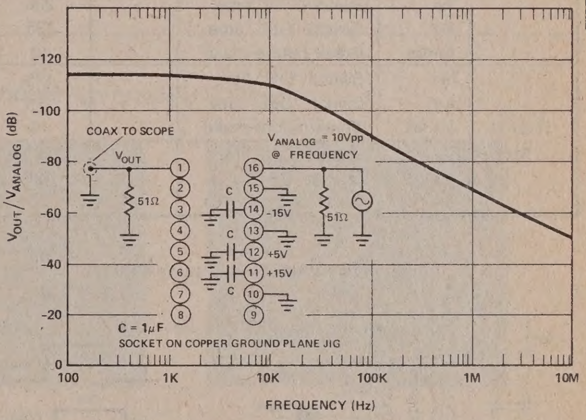


FIGURE 5. "OFF" Isolation vs. Frequency.

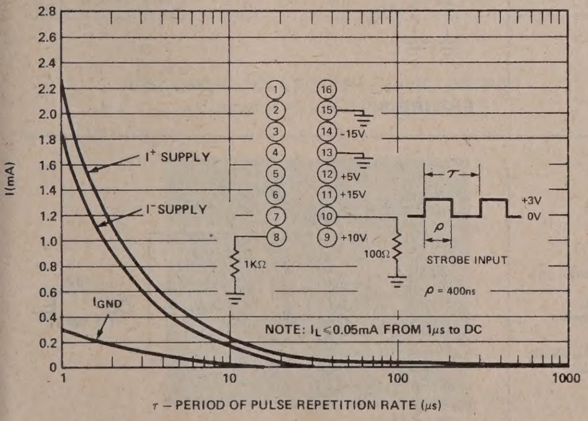


FIGURE 6. Power Supply Currents vs. Logic Strobe Rate.

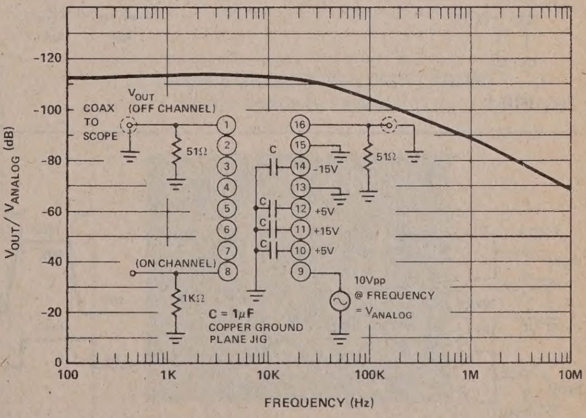


FIGURE 7. Channel to Channel Cross Coupling Rejection vs. Frequency.

SWITCHING TIME SPECIFICATIONS

(t_{on}, t_{off} are maximum specifications and t_{on}-t_{off} is minimum specifications)

Part Number	Symbol	Characteristics	MILITARY -55° C	MILITARY +25° C	MILITARY +125° C	COMMERCIAL 0° C	COMMERCIAL +25° C	COMMERCIAL +70° C	Units	Test Conditions
IH5140-5141	t_{on}	Switch "ON" time		100			150		ns	Figure 8
	t_{off}	Switch "OFF" time		75			125			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		150			175		ns	Figure 9
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
IH5142-5143	t_{on}	Switch "ON" time		175			250		ns	Figure 8
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		200			300		ns	Figure 9
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		175			250		ns	Figure 10
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		200			300		ns	Figure 11
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
IH5144-5145	t_{on}	Switch "ON" time		175			250		ns	Figure 8
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			
	t_{on}	Switch "ON" time		200			300		ns	Figure 9
	t_{off}	Switch "OFF" time		125			150			
	t_{on}-t_{off}	Break-before-make		10			5			

NOTE: SWITCHING TIMES ARE MEASURED @ 90% PTS.

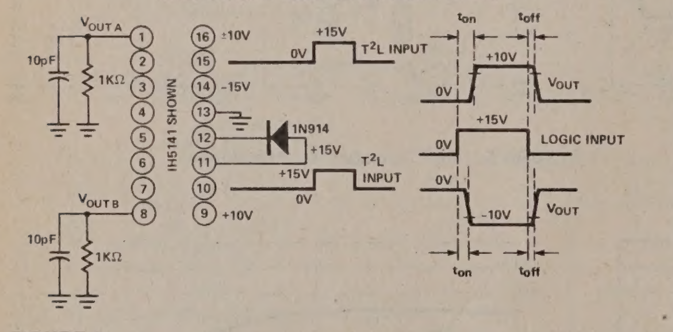

VOUT A
10pF
1KΩ
VOUT B
10pF
1KΩ
IH5141 SHOWN
1
2
3
4
5
6
7
8
16 ±10V
15
14 -15V
13
12
11
10
9 +10V
1N914
+15V
+15V
0V
T²L INPUT
+15V
0V
T²L INPUT
ton
toff
+10V
0V
VOUT
+15V
0V
LOGIC INPUT
0V
-10V
VOUT
ton
toff

FIGURE 8.

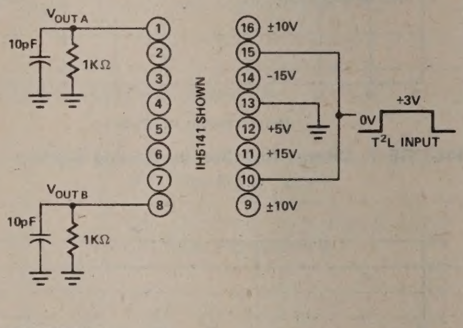

VOUT A
10pF
1KΩ
VOUT B
10pF
1KΩ
IH5141 SHOWN
1
2
3
4
5
6
7
8
16 ±10V
15
14 -15V
13
12 +5V
11 +15V
10
9 ±10V
+3V
0V
T²L INPUT

FIGURE 9.

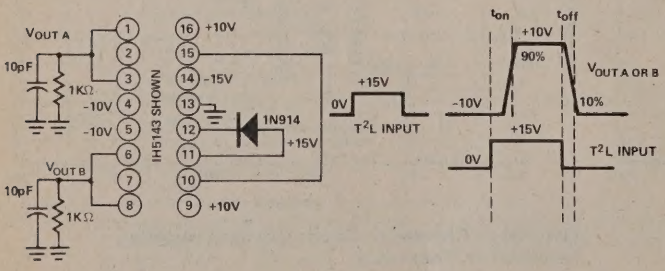

VOUT A
10pF
1KΩ
-10V
-10V
VOUT B
10pF
1KΩ
1
2
3
4
5
6
7
8
IH5143 SHOWN
16 +10V
15
14 -15V
13
12
11
10
9 +10V
1N914
+15V
+15V
0V
T²L INPUT
ton
toff
+10V
90%
-10V
10%
VOUT A OR B
+15V
0V
T²L INPUT

FIGURE 10.

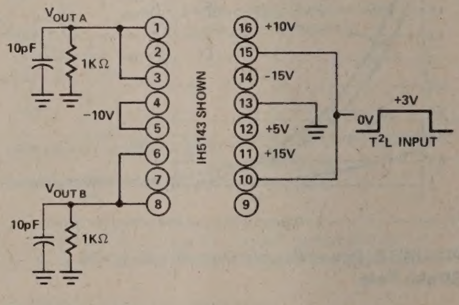
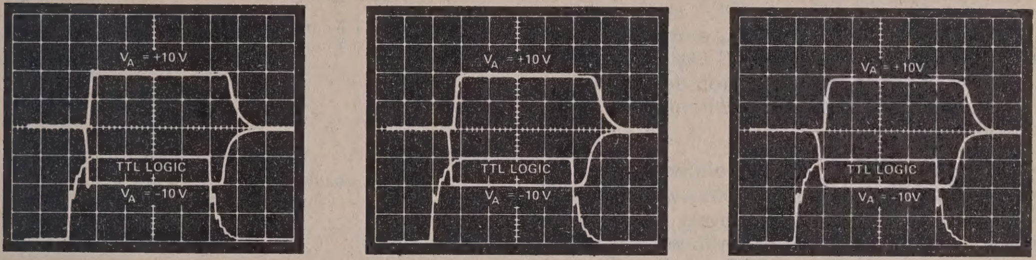

VOUT A
10pF
1KΩ
-10V
VOUT B
10pF
1KΩ
1
2
3
4
5
6
7
8
IH5143 SHOWN
16 +10V
15
14 -15V
13
12 +5V
11 +15V
10
9
+3V
0V
T²L INPUT

FIGURE 11.

TYPICAL SWITCHING WAVEFORMS

SCALE: VERT. = 5V/DIV.
HORIZ. = 100ns/DIV.

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 8)

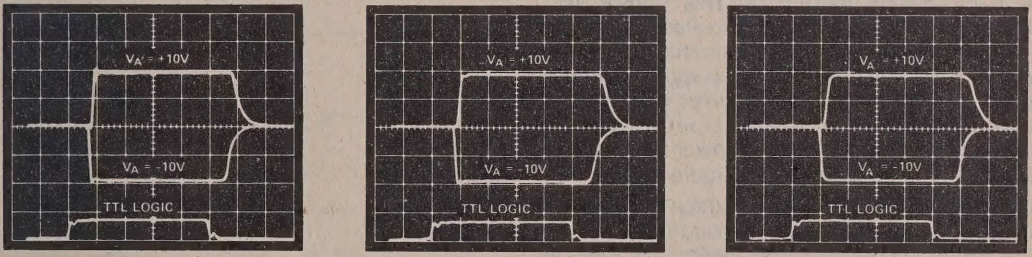


-55°C

+25°C

+125°C

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 9)

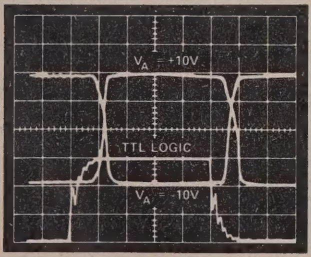


-55°C

+25°C

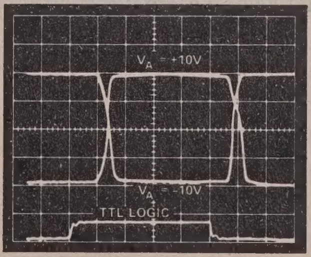
+125°C

TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 10)



+25°C

TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 11)



+25°C

APPLICATION NOTE

To maximize switching speed on the IH5140 family use TTL open collector logic (15V with a 1kΩ or less collector resistor). This configuration will result in (SPST) t_{on} and t_{off} times of 80ns and 50ns, for signals between -10V and +10V. The SPDT and DPST switches are approximately 30ns slower in both t_{on} and t_{off} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns → 100ns delays).

When driving the IH5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus t_{on} is about 105ns, and t_{off} 75ns for SPST switches, and 135ns and 105ns (t_{on}, t_{off}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if ±5V strobe levels are used instead of the usual 0V→+3.0V drive. Pin 13 is taken to -5V instead of the usual GND and strobe input is taken from +5V to -5V levels as shown in Figure 12.

The typical channel of the IH5140 family consists of both P and N-channel MOS-FETs. The N-channel MOS-FET uses a "Body Puller" FET to drive the body to -15V(±15V supplies) to get good breakdown voltages when the switch is in the off state (See Fig. 13). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the on state producing a fairly constant $R_{DS(ON)}$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 14.

Current will flow from -10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 15. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.

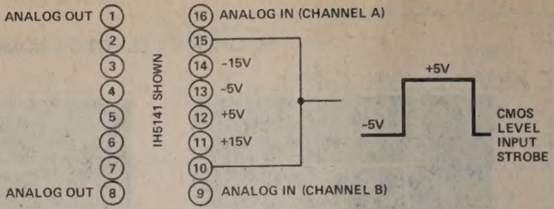

ANALOG OUT ①
②
③
④
⑤
⑥
⑦
ANALOG OUT ⑧
IH5141 SHOWN
⑯ ANALOG IN (CHANNEL A)
⑮
⑭ -15V
⑬ -5V
⑫ +5V
⑪ +15V
⑩
⑨ ANALOG IN (CHANNEL B)
+5V
-5V
CMOS LEVEL INPUT STROBE

FIGURE 12.

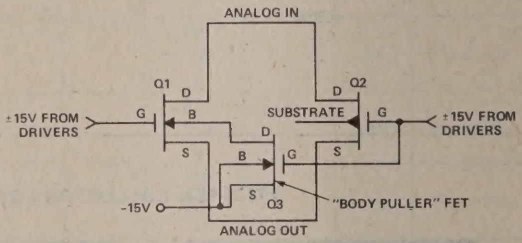

ANALOG IN
Q1
D
D
Q2
±15V FROM DRIVERS
G
B
SUBSTRATE
G
±15V FROM DRIVERS
D
S
B
G
S
S
Q3
-15V
"BODY PULLER" FET
ANALOG OUT

FIGURE 13.

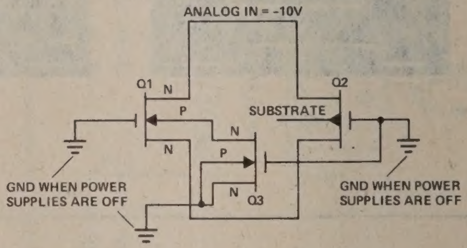

ANALOG IN = -10V
Q1
N
Q2
P
SUBSTRATE
N
N
P
N
Q3
GND WHEN POWER SUPPLIES ARE OFF
GND WHEN POWER SUPPLIES ARE OFF

FIGURE 14.

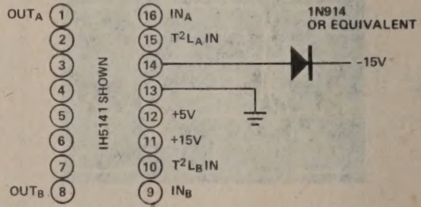

OUTA ①
②
③
④
⑤
⑥
⑦
OUTB ⑧
IH5141 SHOWN
⑯ INA
⑮ T²LA IN
⑭
⑬
⑫ +5V
⑪ +15V
⑩ T²LB IN
⑨ INB
1N914 OR EQUIVALENT
-15V

FIGURE 15.

APPLICATIONS

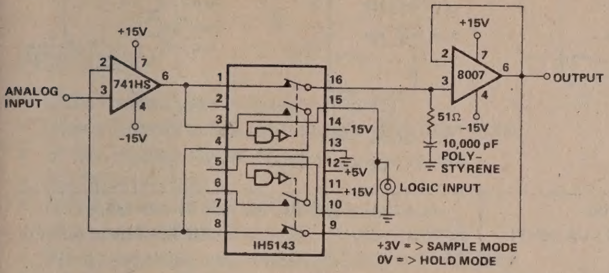
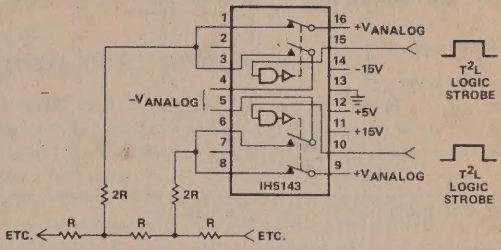
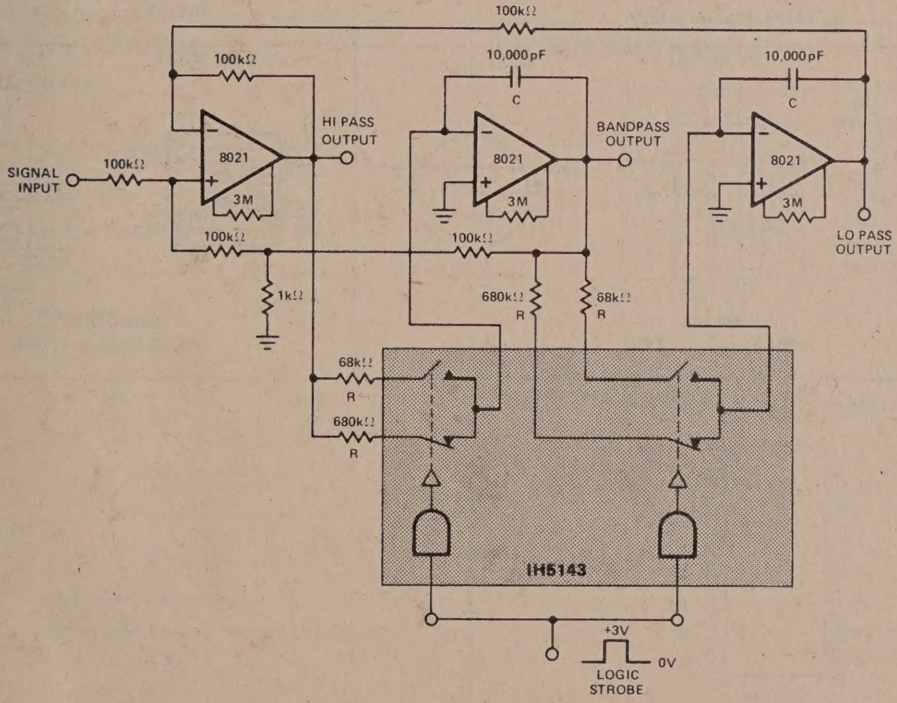

+15V
2
7
3
741HS
6
4
ANALOG INPUT
-15V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
-15V
+5V
+15V
IH5143
+15V
2
7
3
8007
6
4
OUTPUT
51Ω
-15V
10,000 pF POLY-STYRENE
LOGIC INPUT
+3V = > SAMPLE MODE
0V = > HOLD MODE

FIGURE 16. Improved Sample and Hold Using IH5143


1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
+VANALOG
-15V
+5V
+15V
+VANALOG
-VANALOG
IH5143
T²L LOGIC STROBE
T²L LOGIC STROBE
2R
2R
R
R
R
ETC.
ETC.

EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

FIGURE 17. Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)


100kΩ
100kΩ
10,000pF
C
10,000pF
C
SIGNAL INPUT
100kΩ
8021
3M
HI PASS OUTPUT
8021
3M
BANDPASS OUTPUT
8021
3M
LO PASS OUTPUT
100kΩ
100kΩ
1kΩ
680kΩ R
68kΩ R
68kΩ R
680kΩ R
IH5143
+3V
0V
LOGIC STROBE

CONSTANT GAIN, CONSTANT Q, VARIABLE FREQUENCY FILTER WHICH PROVIDES SIMULTANEOUS LOWPASS, BANDPASS, AND HIGHPASS OUTPUTS. WITH THE COMPONENT VALUES SHOWN, CENTER FREQUENCY WILL BE 235Hz AND 23.5Hz FOR HIGH AND LOW LOGIC INPUTS RESPECTIVELY, Q = 100, AND GAIN = 100.

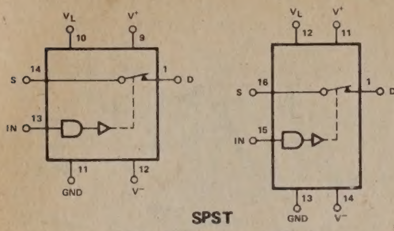
$$f_n = \text{CENTER FREQUENCY} = \frac{1}{2\pi RC}$$

FIGURE 18. Digitally Tuned Low Power Active Filter.

SWITCHING STATE DIAGRAMS

SWITCH STATES ARE FOR LOGIC "1" INPUT

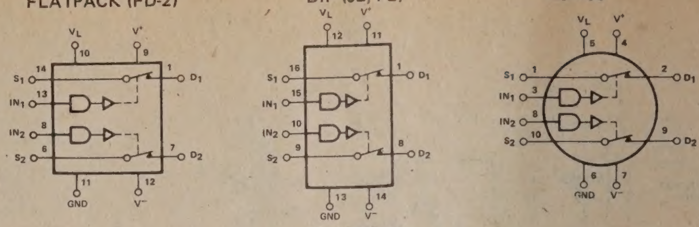
FLATPACK (FD-2) DIP (JE, PE)


V_L 10
V^+ 9
S 14
D 1
IN 13
GND 11
V^- 12
V_L 12
V^+ 11
S 16
D 1
IN 15
GND 13
V^- 14

SPST

IH5140 ($r_{DS(on)} < 75\Omega$)

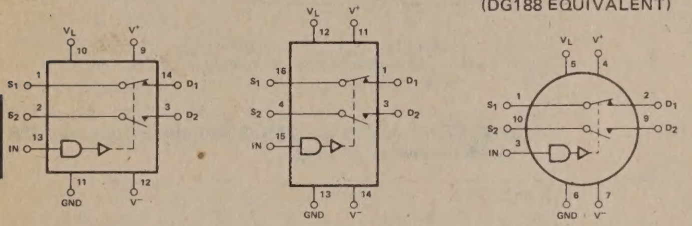
FLATPACK (FD-2) DIP (JE, PE) TO-100


V_L 10
V^+ 9
S_1 14
D_1 1
IN_1 13
IN_2 8
S_2 6
D_2 7
GND 11
V^- 12
V_L 12
V^+ 11
S_1 16
D_1 1
IN_1 15
IN_2 10
S_2 9
D_2 8
GND 13
V^- 14
V_L 5
V^+ 4
S_1 1
D_1 2
IN_1 3
IN_2 8
S_2 10
D_2 9
GND 6
V^- 7

DUAL SPST

IH5141 ($r_{DS(on)} < 75\Omega$)

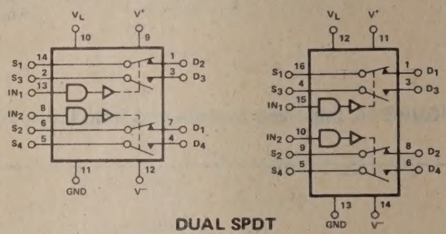
FLATPACK (FD-2) DIP (JE, PE) TO-100 (DG188 EQUIVALENT)


V_L 10
V^+ 9
S_1 1
D_1 14
S_2 2
D_2 3
IN 13
GND 11
V^- 12
V_L 12
V^+ 11
S_1 16
D_1 1
S_2 4
D_2 3
IN 15
GND 13
V^- 14
V_L 5
V^+ 4
S_1 1
D_1 2
S_2 10
D_2 9
IN 3
GND 6
V^- 7

SPDT

IH5142 ($r_{DS(on)} < 75\ \Omega$)

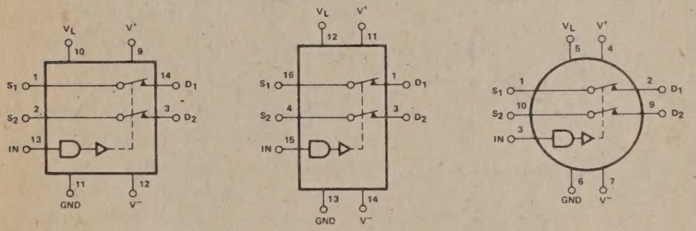
FLATPACK (FD-2) DIP (JE, PE) (DG191 EQUIVALENT)


V_L 10
V^+ 9
S_1 14
D_2 1
S_3 2
D_3 3
IN_1 13
IN_2 8
S_2 6
D_1 7
S_4 5
D_4 4
GND 11
V^- 12
V_L 12
V^+ 11
S_1 16
D_1 1
S_3 4
D_3 3
IN_1 15
IN_2 10
S_2 9
D_2 8
S_4 5
D_4 6
GND 13
V^- 14

DUAL SPDT

IH5143 ($r_{DS(on)} < 75\Omega$)

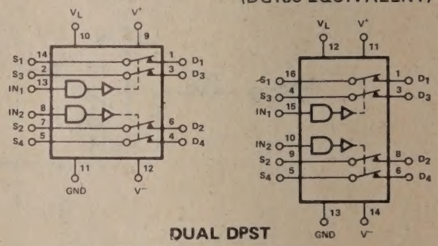
FLATPACK (FD-2) DIP (JE, PE) TO-100


V_L 10
V^+ 9
S_1 1
D_1 14
S_2 2
D_2 3
IN 13
GND 11
V^- 12
V_L 12
V^+ 11
S_1 16
D_1 1
S_2 4
D_2 3
IN 15
GND 13
V^- 14
V_L 5
V^+ 4
S_1 1
D_1 2
S_2 10
D_2 9
IN 3
GND 6
V^- 7

DPST

IH5144 ($r_{DS(on)} < 75\Omega$)

FLATPACK (FD-2) DIP (JE, PE) (DG185 EQUIVALENT)


V_L 10
V^+ 9
S_1 14
D_1 1
S_3 2
D_3 3
IN_1 13
IN_2 8
S_2 7
D_2 6
S_4 5
D_4 4
GND 11
V^- 12
V_L 12
V^+ 11
S_1 16
D_1 1
S_3 4
D_3 3
IN_1 15
IN_2 10
S_2 9
D_2 8
S_4 5
D_4 6
GND 13
V^- 14

DUAL DPST

IH5145 ($r_{DS(on)} < 75\Omega$)

INTERSIL

IH5208
4-Channel Differential Fault Protected CMOS Analog Multiplexer

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

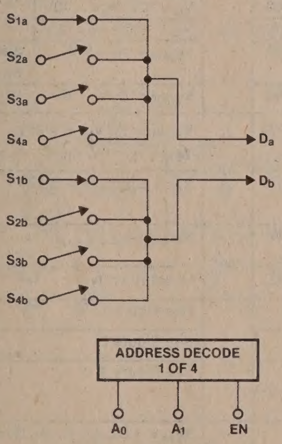
- Ultra low leakage — $I_{D(off)} \leq 100pA$
- Power supply quiescent current less than 1mA
- ±13V analog signal range
- No SCR latchup
- Break-before-make switching
- TTL and CMOS compatible strobe control
- Pin compatible with HI509, DG509 and AD7509
- All channels OFF ($I_{ILK} \leq 100nA$) when power OFF, for analog signals up to ±25V
- Any channel turns OFF ($I_{ILK} \leq 100nA$) if input exceeds supply rails by up to ±25V. Throughput always < ±14V (±15V supplies)
- TTL and CMOS compatible binary address and enable inputs

GENERAL DESCRIPTION

The IH5208 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the DG509 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

FUNCTIONAL DIAGRAM



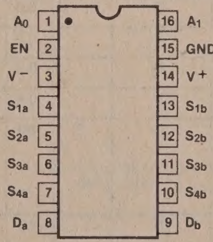
2 LINE BINARY STROBE INPUTS
(0 0) AND EN = 1
ABOVE EXAMPLE SHOWS CHANNELS 1a and 1b ON

DECODE TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (Outline drawing JE, PE)



TOP VIEW

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5208MJE	−55°C to +125°C	16 pin CERDIP
IH5208CJE	0°C to 70°C	16 pin CERDIP
IH5208CPE	0°C to 70°C	16 pin plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground .... −15V, +15V
V_S or V_D to V^+ .... +25V, −40V
V_S or V_D to V^- .... −25V, +40V
V^+ to Ground 16V
V^- to Ground .... −16V
Current (Any Terminal) 20mA

Operating Temperature .... −55 to 125°C
Storage Temperature .... −65 to 150°C
Power Dissipaton (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS						UNIT	TEST CONDITIONS	
					M SUFFIX			C SUFFIX					
					−55°C	25°C	125°C	0°C	25°C	70°C			
SWITCH	$r_{DS(on)}$	S to D	8	700	1000	1000	1500	1200	1200	1800	Ω	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on
			8	500	1000	1000	1500	1200	1200	1800		$V_D = -10V$ $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(on)}$			5							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(off)}$	S	8	0.002		0.05	50		0.1	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
			8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(off)}$	D	1	0.03		0.1	100		0.2	100		$V_D = 10V$, $V_S = -10V$	
			1	0.03		0.1	100		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(on)}$	D	8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
			8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
FAULT	I_S with Power OFF	S	8	1	10	10	1000	50	50	5000	nA	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, A_0, A_1, $A_2 = 0V$ or 5V	
	I_S with Overvoltage	S	8	1	10	10	1000	50	50	5000		$V_{IN} = \pm 25V$, $V_O = \pm 10V$	
IN	$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1, EN	4	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
			4	.01		10	30		10	30		$V_A = 15V$ or 0V	
DYNAMIC	$t_{transition}$	D		0.3		1					μs	See Figure 1	
	t_{open}	D		0.2								See Figure 2	
	$t_{on(EN)}$	D		0.6		1.5						See Figure 3	
	$t_{off(EN)}$	D		0.4		1							
	t_{on}−t_{off} Break-Before-Make Delay Settling Time	D	8	50		25			10		ns	$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, Figure 4	
	"OFF" Isolation	D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 KHz	
	$C_{S(off)}$	S		5							pF	$V_S = 0$	$V_{EN} = 0V$, f = 140 KHz to 1 MHz
	$C_{D(off)}$	D		25								$V_D = 0$	
	$C_{DS(off)}$	D to S		1								$V_S = 0$, $V_D = 0$	
SUP	Supply Current +	V^+	1	40		200			1000		μA	All V_A, $V_{EN} = 0$ or 5V	
	Supply Current −	V^-	1	2		100			1000				

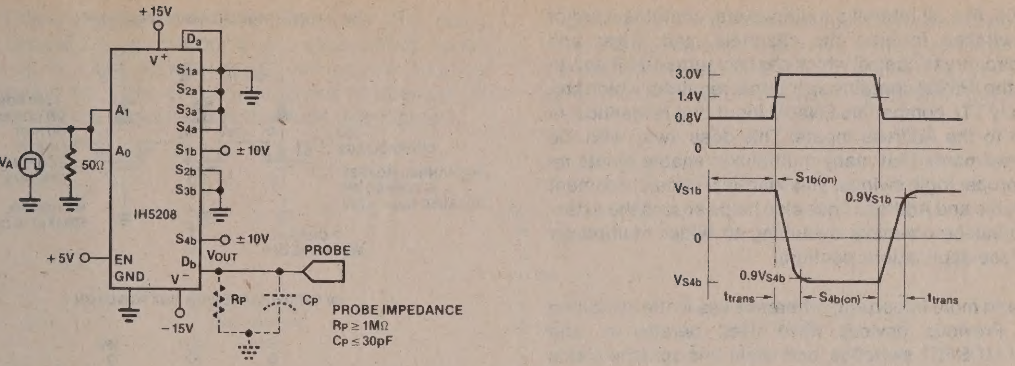

+15V
Da
V+
S1a
S2a
S3a
S4a
A1
A0
VA
50Ω
S1b
± 10V
S2b
S3b
IH5208
S4b
± 10V
+5V
EN
Db
VOUT
PROBE
GND
V−
RP
CP
−15V
PROBE IMPEDANCE
RP ≥ 1MΩ
CP ≤ 30pF
3.0V
1.4V
0.8V
0
VS1b
S1b(on)
0.9VS1b
0
VS4b
0.9VS4b
ttrans
S4b(on)
ttrans

Figure 1. t_{trans} Switching Test

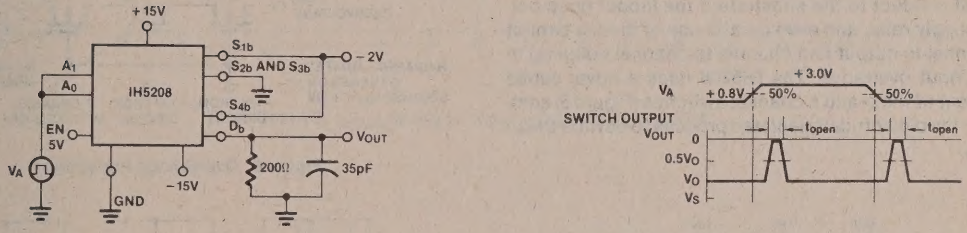

+15V
S1b
−2V
S2b AND S3b
A1
A0
IH5208
S4b
EN
5V
Db
VOUT
VA
−15V
200Ω
35pF
GND
+3.0V
VA
+0.8V
50%
50%
SWITCH OUTPUT
VOUT
topen
topen
0
0.5VO
VO
VS

Figure 2. t_{open} (Break-Before-Make) Switching Test

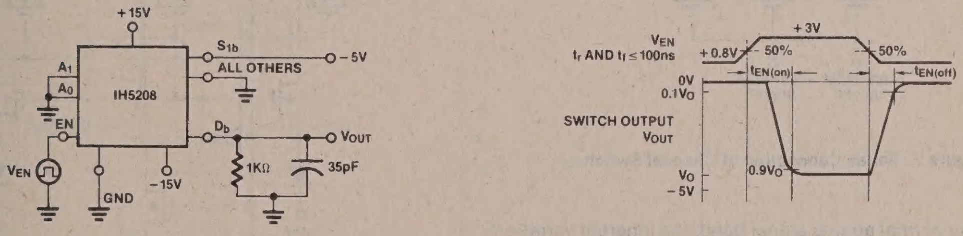

+15V
S1b
−5V
ALL OTHERS
A1
A0
IH5208
EN
Db
VOUT
VEN
−15V
1KΩ
35pF
GND
+3V
VEN
tr AND tf ≤ 100ns
+0.8V
50%
50%
tEN(on)
tEN(off)
0V
0.1VO
SWITCH OUTPUT
VOUT
VO
0.9VO
−5V

Figure 3. t_{on} and t_{off} Switching Test

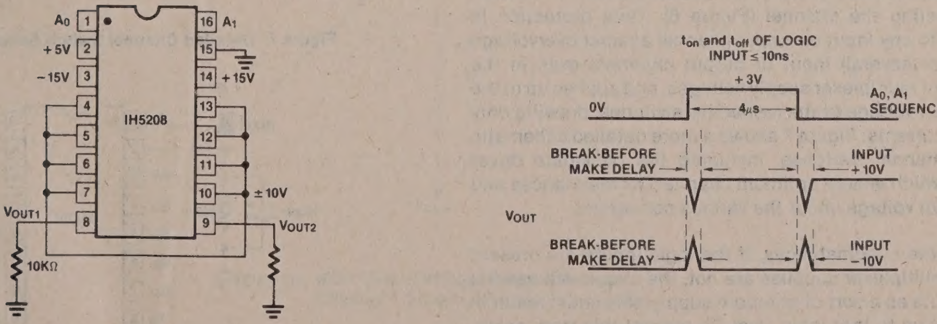

A0
1
16
A1
+5V
2
15
−15V
3
14
+15V
4
13
IH5208
5
12
6
11
7
10
± 10V
VOUT1
8
9
VOUT2
10KΩ
ton and toff OF LOGIC
INPUT ≤ 10ns
+3V
0V
4μs
A0, A1
SEQUENCED
BREAK-BEFORE
MAKE DELAY
INPUT
+10V
VOUT
BREAK-BEFORE
MAKE DELAY
INPUT
−10V

Figure 4. Break-Before-Make Delay Test

DETAILED DESCRIPTION

The IH5208, like all Intersil's multiplexers, contains a set of CMOS switches forming the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5208 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special treatments that many multiplexer enable inputs require for proper logic swings. This identical circuit treatment of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important, difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches, and while this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the inpout goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5208 uses a novel series arrangement of the p- and n-channel switches (Figure 5) combined with the dielectrically isolated process to obviate these problems.

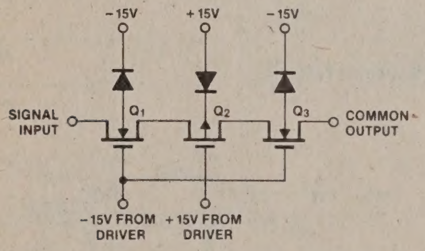
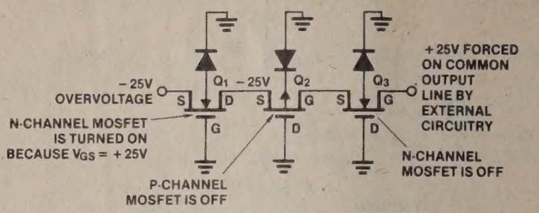

−15V
+15V
−15V
SIGNAL INPUT
Q_1
Q_2
Q_3
COMMON OUTPUT
−15V FROM DRIVER
+15V FROM DRIVER

Figure 5. Series Connection of Channel Switches

Within the normal analog signal band, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 6). Thus protection is provided to any input or output channel against overvoltage on any (or several) input or output channels even in the absence of multiplexer supply voltages, and applies up to the breakdown voltage of the respective switches, drawing only leakage currents. Figure 7 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 8).

(a) OVERVOLTAGE WITH MUX POWER OFF


−25V OVERVOLTAGE
Q_1
−25V
Q_2
Q_3
S
D
S
G
S
G
G
D
D
+25V FORCED ON COMMON OUTPUT LINE BY EXTERNAL CIRCUITRY
N-CHANNEL MOSFET IS TURNED ON BECAUSE V_{GS} = +25V
P-CHANNEL MOSFET IS OFF
N-CHANNEL MOSFET IS OFF

(b) OVERVOLTAGE WITH MUX POWER ON

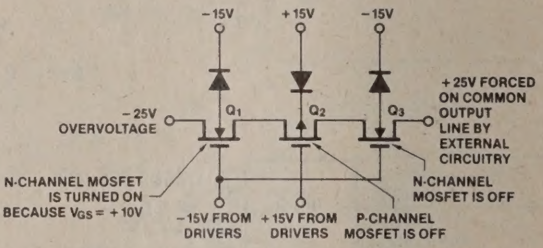

−15V
+15V
−15V
−25V OVERVOLTAGE
Q_1
Q_2
Q_3
+25V FORCED ON COMMON OUTPUT LINE BY EXTERNAL CIRCUITRY
N-CHANNEL MOSFET IS TURNED ON BECAUSE V_{GS} = +10V
−15V FROM DRIVERS
+15V FROM DRIVERS
P-CHANNEL MOSFET IS OFF
N-CHANNEL MOSFET IS OFF

Figure 6. Overvoltage Protection

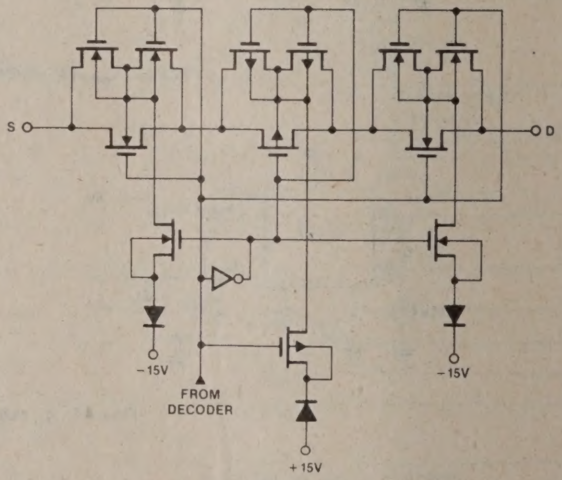

S
D
−15V
−15V
FROM DECODER
+15V

Figure 7. Detailed Channel Switch Schematic

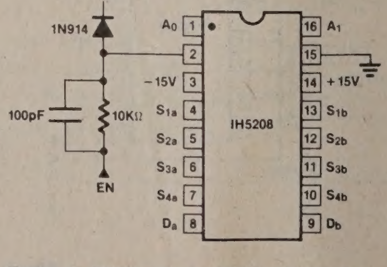

+15V
1N914
100pF
10KΩ
EN
A_0 1
2
−15V 3
S_{1a} 4
S_{2a} 5
S_{3a} 6
S_{4a} 7
D_a 8
IH5208
16 A_1
15
14 +15V
13 S_{1b}
12 S_{2b}
11 S_{3b}
10 S_{4b}
9 D_b

Figure 8. Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5208 is designed to handle signals in the ± 10V range, with a typical $r_{DS(on)}$ of 600Ω; it can successfully handle signals up to ± 13V, however, $r_{DS(on)}$ will increase to about 1.8K. Beyond ± 13V the device approaches an open circuit, and thus ± 12V is about the practical limit, see Figure 9.

Figure 10 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 11 gives the ON resistance variation with temperature.

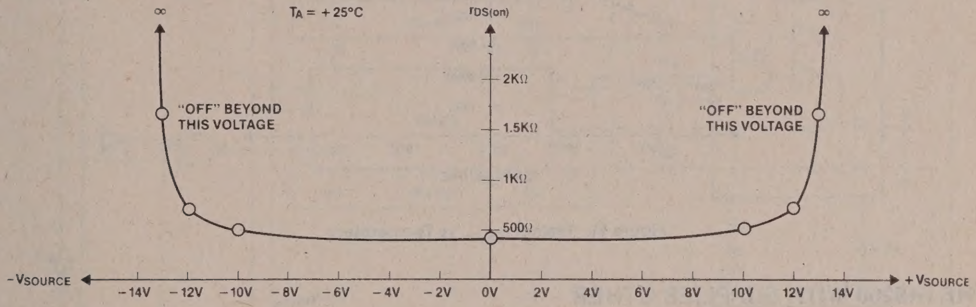


Figure 9. $r_{DS(on)}$ vs Signal Input Voltage @ T_A = + 25°C

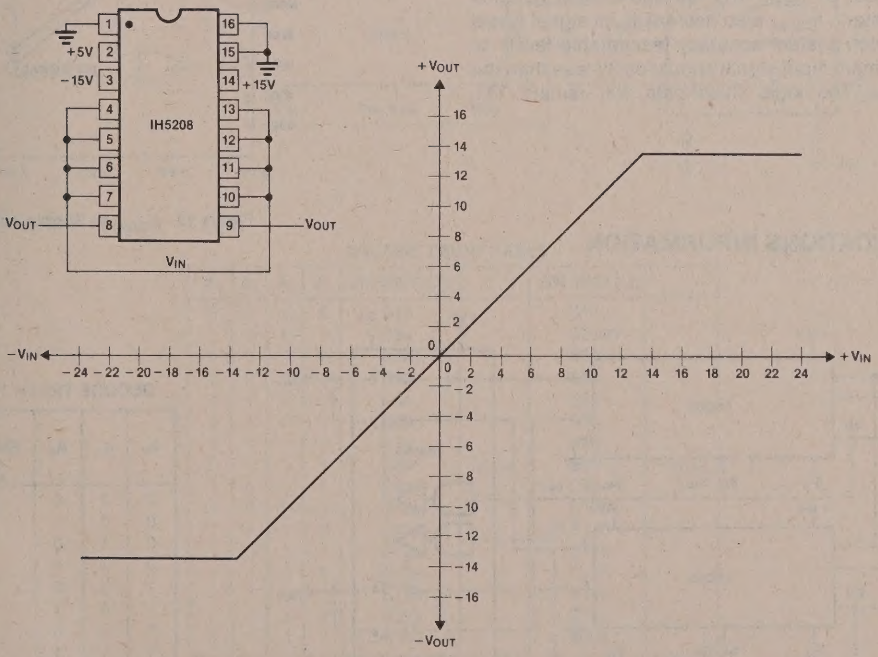


Figure 10. MUX Output Voltage vs Input Voltage
Channel 1 Shown; All Channels Similar

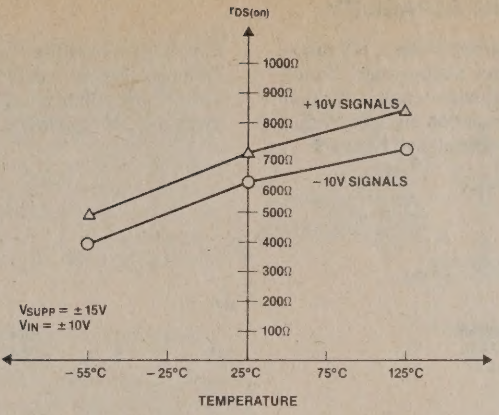


Figure 11. Typical $r_{DS(on)}$ vs Temperature

USING THE IH5208 WITH SUPPLIES OTHER THAN ±15V

The IH5208 will operate successfully with supply voltages from ±5V to ±15V; $r_{DS(on)}$ increases as supply voltage decreases, see Figure 12. Leakage currents, however, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic thresholds will remain TTL compatible.

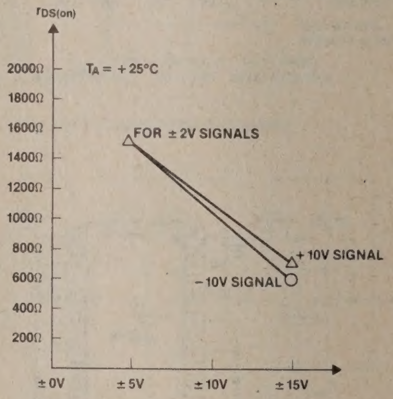
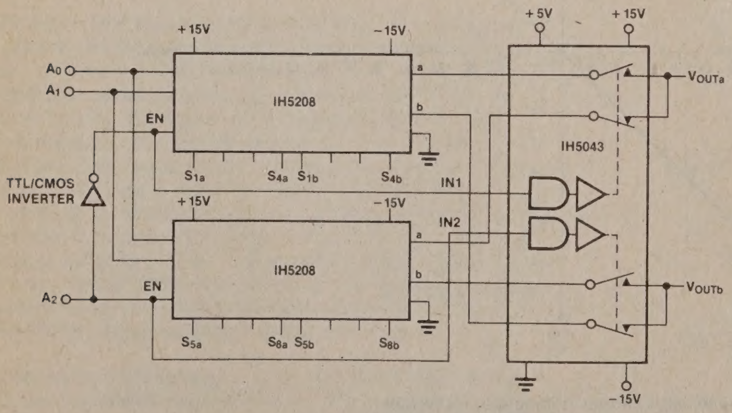


Figure 12. $r_{DS(on)}$ vs Supply Voltages

IH5208 APPLICATIONS INFORMATION

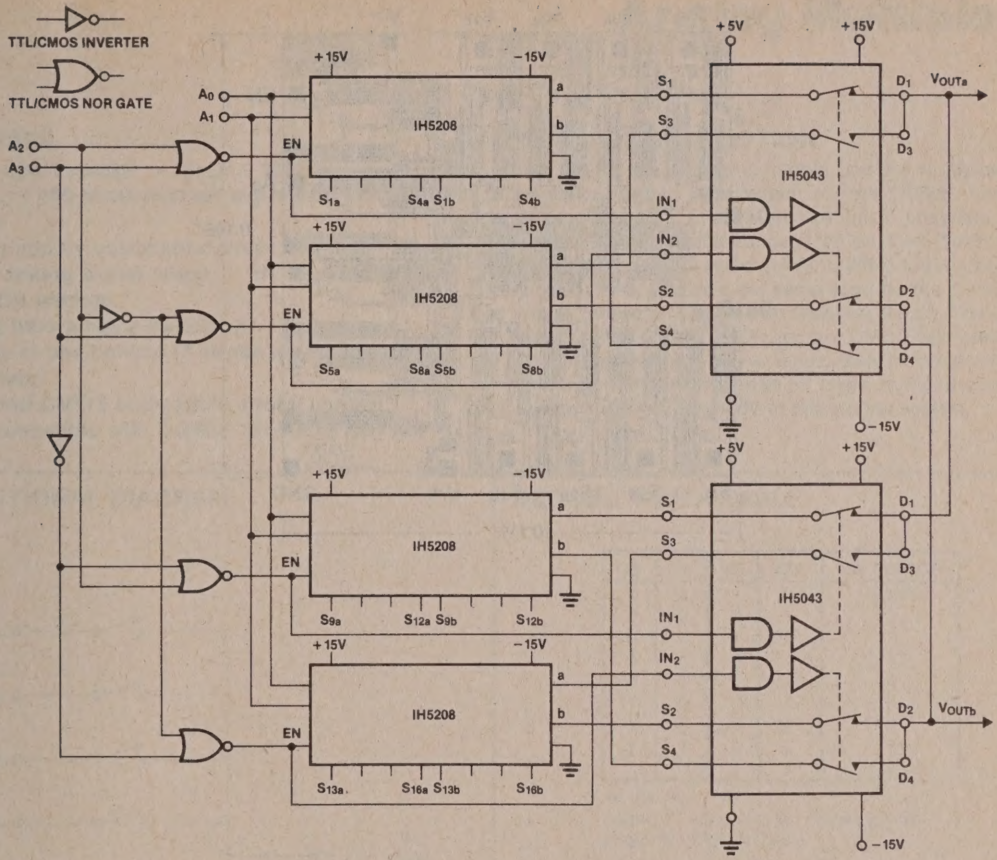

+15V
−15V
A0
A1
EN
IH5208
a
b
S1a
S4a
S1b
S4b
TTL/CMOS INVERTER
+15V
−15V
IH5208
a
b
EN
A2
S5a
S8a
S5b
S8b
IN1
IN2
+5V
+15V
IH5043
VOUTa
VOUTb
−15V

DECODE TRUTH TABLE

A_2	A_1	A_0	ON SWITCH PAIR
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Figure 13. 2 of 16 channel multiplexer using two IH5208s. Overvoltage protection and break-before-make switching are extended to all channels.

IH5208 APPLICATIONS INFORMATION (Cont.)

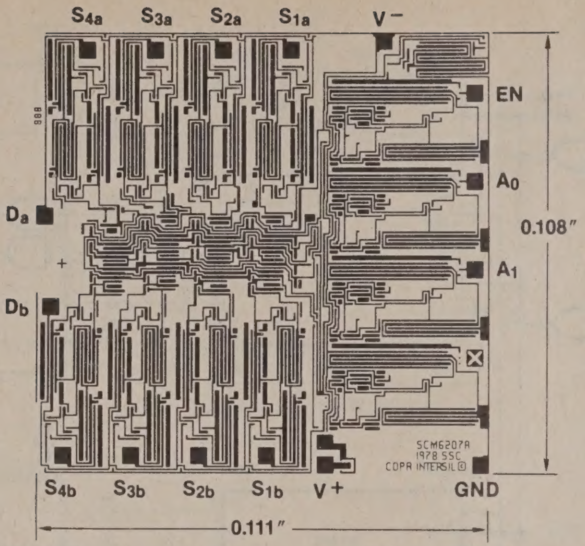

TTL/CMOS INVERTER
TTL/CMOS NOR GATE
A0
A1
A2
A3
+15V
−15V
+5V
IH5208
IH5043
EN
a
b
S1a
S4a S1b
S4b
S5a
S8a S5b
S8b
S9a
S12a S9b
S12b
S13a
S16a S13b
S16b
S1
S2
S3
S4
IN1
IN2
D1
D2
D3
D4
VOUTa
VOUTb

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH		ON SWITCH	
0	0	0	0	S1a	V_{OUTa}	S1b	V_{OUTb}
0	0	0	1	S2a		S2b	
0	0	1	0	S3a		S3b	
0	0	1	1	S4a		S4b	
0	1	0	0	S5a		S5b	
0	1	0	1	S6a		S6b	
0	1	1	0	S7a		S7b	
0	1	1	1	S8a		S8b	
1	0	0	0	S9a		S9b	
1	0	0	1	S10a		S10b	
1	0	1	0	S11a		S11b	
1	0	1	1	S12a		S12b	
1	1	0	0	S13a		S13b	
1	1	0	1	S14a		S14b	
1	1	1	0	S15a		S15b	
1	1	1	1	S16a		S16b	

Figure 14. Submultiplexed 2 of 32 system. The two IH5043s are overvoltage protected by the IH5208s. Submultiplexing reduces output capacitance and leakage currents.

CHIP TOPOGRAPHY


S_{4a}
S_{3a}
S_{2a}
S_{1a}
V−
EN
A_0
0.108″
A_1
D_a
D_b
SCM6207A
1978 SSC
COPR INTERSIL ©
S_{4b}
S_{3b}
S_{2b}
S_{1b}
V+
GND
0.111″

IH6108
8 Channel CMOS Analog Multiplexer

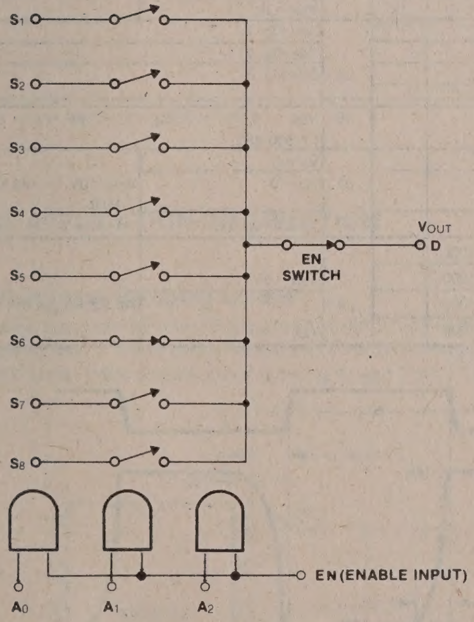
FEATURES

- **Ultra Low Leakage — $I_{D(off)} \leq 100pA$**
- **$r_{DS(on)} < 400$ ohms over full signal and temperature range**
- **Power supply quiescent current less than $100\mu A$**
- **±14V analog signal range**
- **No SCR latchup**
- **Break before make switching**
- **Binary strobe control (3 strobe inputs control 8 channels)**
- **TTL and CMOS compatible strobe control**
- **Pin compatible with DG508, HI-508 & AD7508**

GENERAL DESCRIPTION

The IH6108 is a CMOS monolithic, one of 8 multiplexer. The part is a plug-in replacement for the DG508. Three line binary decoding is used so that the 8 channels can be controlled by 3 strobe inputs; additionally a fourth input is provided to use as a system enable. When the enable input is high (5V) the channels are sequenced by the 3 line strobe inputs, and when low (0V) all channels are off. The 3 strobe inputs are controlled by TTL logic or CMOS logic elements, a "0" corresponding to any voltage greater than 2.4V. Note that the enable input (EN) must be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM



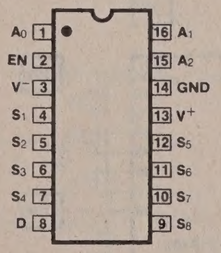
3 LINE BINARY STROBE INPUTS
(1 0 1) AND EN @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON.

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
x	x	x	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2
Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (Outline drawings DE, PE)



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6108MDE	−55°C to +125°C	16 pin ceramic DIP
IH6108CDE	0°C to 70°C	16 pin ceramic DIP
IH6108CPE	0°C to 70°C	16 pin plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground	−15V to 15V
V_S or V_D to V^+	0, −32V
V_S or V_D to V^-	0, 32V
V^+ to Ground	16V
V^- to Ground	−16V
Current (Any Terminal)	30 mA
Current (Analog Drain)	20 mA
Current (Analog Source)	20 mA
Operating Temperature	−55 to 125°C
Storage Temperature	−65 to 150°C
Power Dissipation (Package)*	1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V^1$, Ground = 0V, unless otherwise specified.

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS						UNIT	TEST CONDITIONS	
					M SUFFIX			C SUFFIX					
					−55°C	25°C	125°C	0°C	25°C	70°C			
SWITCH	$r_{DS(ON)}$	S to D	8	180	300	300	400	350	350	450	Ω	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on
			8	150	300	300	400	350	350	450		$V_D = -10V$, $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg}}$ $V_S = \pm 10V$	
	$I_{S(OFF)}$	S	8	0.002		0.05	50		0.1	50	NA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
			8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(OFF)}$	D	1	0.03		0.1	100		0.2	100		$V_D = 10V$, $V_S = -10V$	
			1	0.03		0.1	100		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(ON)}$	D	8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
			8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
INPUT	$I_{AN(ON)}$ or $I_{A(on)}$	A_0, A_1 or A_2 Inputs	3	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
	$I_{AN(OFF)}$ $I_{A(off)}$		3	.01		10	30		10	30		$V_A = 15V$ or 0V	
	I_A	A_0 A_1 A_2	3			−10	−30		−10	−30		$V_{EN} = 5V$	All $V_A = 0$ (Strobe pins)
		En	1			−10	−30		−10	−30		$V_{EN} = 0$	
DYNAMIC	$t_{transition}$	D		0.3		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(En)}$	D		0.6		1.5						See Fig. 3	
	$t_{off(En)}$	D		0.4		1							
	"OFF" Isolation	D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 kHz	
	$C_{s(off)}$	S		5							pF	$V_S = 0$	$V_{EN} = 0V$. f = 140 kHz to 1 MHz
	$C_{d(off)}$	D		25								$V_D = 0$	
	$C_{DS(off)}$	D to S		1								$V_S = 0$, $V_D = 0$	
SUPPLY	Supply Current +	I^+	1	40		200			1000		μA	$V_{EN} = 5V$	All $V_A = 0$ OR 5V
	Supply Current −	I^-	1	2		100			1000				
	Standby Current +	I^+_{SB}	1	1		100			1000			$V_{EN} = 0$	
	Standby Current −	I^-_{SB}	1	1		100			1000				

NOTE 1: See Enable Input Strobing Levels, Section 1.

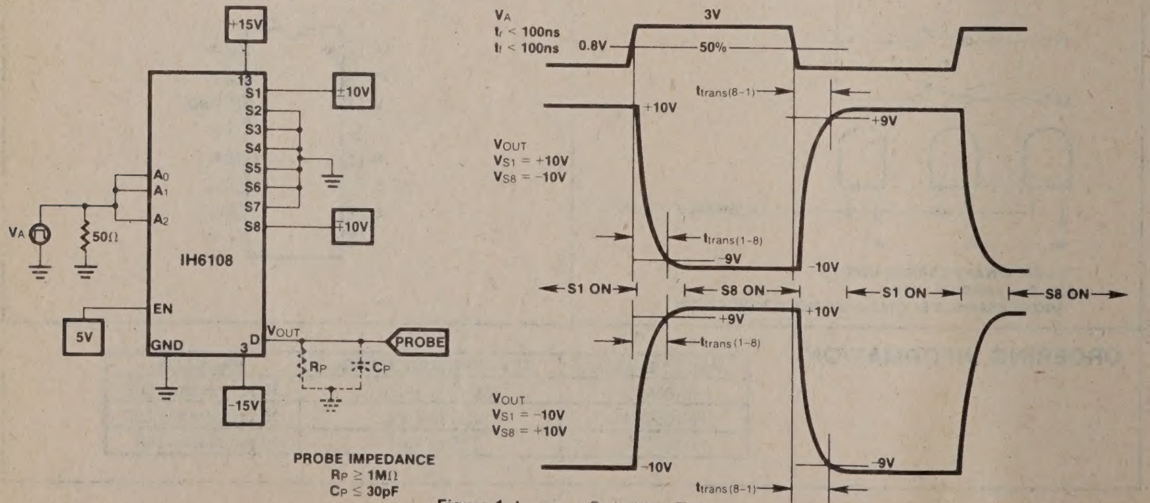

+15V
13
S1
S2
S3
S4
S5
S6
S7
S8
±10V
∓10V
A0
A1
A2
VA
50Ω
IH6108
EN
5V
GND
3
D
VOUT
PROBE
RP
CP
−15V
PROBE IMPEDANCE
RP ≥ 1MΩ
CP ≤ 30pF
VA
tr < 100ns
tf < 100ns
0.8V
3V
50%
ttrans(8-1)
+10V
+9V
VOUT
VS1 = +10V
VS8 = −10V
ttrans(1-8)
−9V
−10V
S1 ON
S8 ON
S1 ON
S8 ON
+9V
+10V
ttrans(1-8)
VOUT
VS1 = −10V
VS8 = +10V
−10V
−9V
ttrans(8-1)

Figure 1. $t_{transition}$ Switching Test

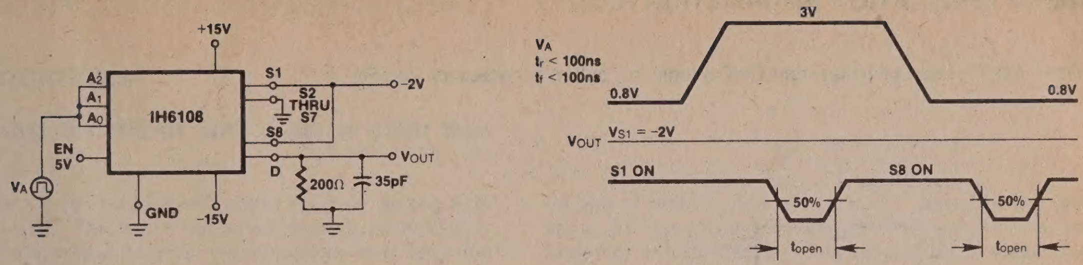

+15V
A2
A1
A0
IH6108
EN
5V
VA
GND
-15V
S1
S2
THRU
S7
S8
D
-2V
VOUT
200Ω
35pF
VA
tr < 100ns
tf < 100ns
3V
0.8V
0.8V
VOUT
VS1 = -2V
S1 ON
S8 ON
50%
50%
topen
topen

Figure 2. t_{open} Break-Before-Make Switching Test

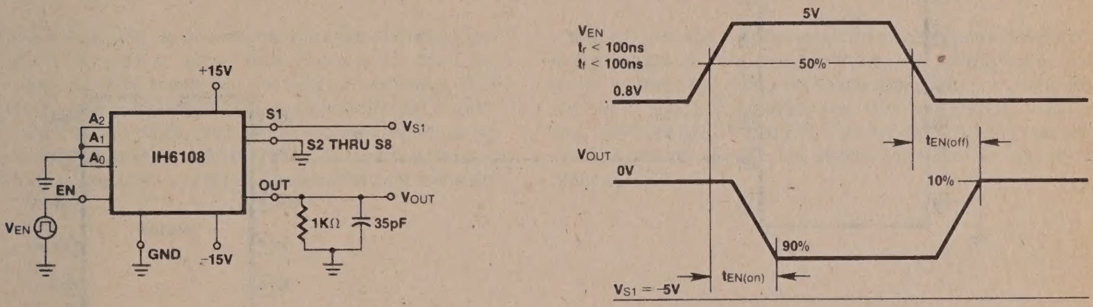

+15V
A2
A1
A0
IH6108
EN
VEN
GND
-15V
S1
VS1
S2 THRU S8
OUT
VOUT
1KΩ
35pF
VEN
tr < 100ns
tf < 100ns
5V
50%
0.8V
VOUT
0V
tEN(off)
10%
90%
tEN(on)
VS1 = -5V

Figure 3. t_{on} and t_{off} Switching Test

IH6108 APPLICATION INFORMATION

I. Enable Input Strobing Levels

The enable input on the IH6108 requires a minimum of +4.5V to trigger to the "1" state and a maximum of +0.8V to trigger to the "0" state. If the enable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 4)

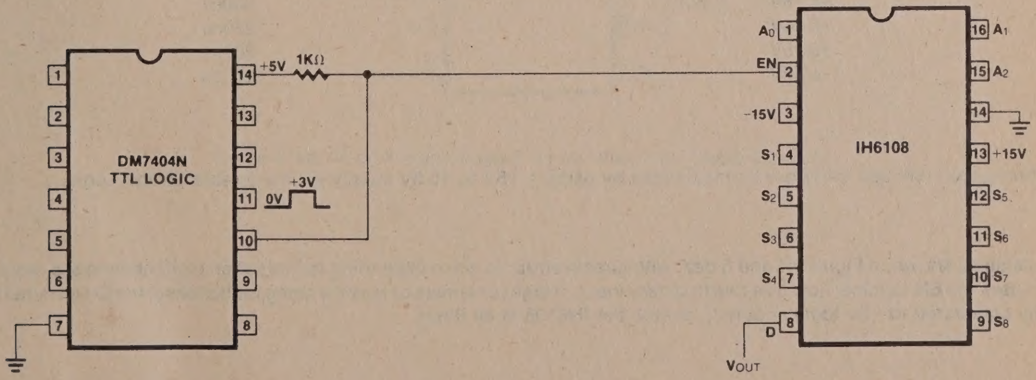

DM7404N
TTL LOGIC
1
2
3
4
5
6
7
14
13
12
11
10
9
8
+5V
1KΩ
+3V
0V
IH6108
A0 1
EN 2
-15V 3
S1 4
S2 5
S3 6
S4 7
D 8
VOUT
16 A1
15 A2
14
13 +15V
12 S5
11 S6
10 S7
9 S8

Figure 4. Enable Input Strobing from TTL Logic

IH6108 APPLICATION INFORMATION (CONT.)

When the EN input is driven from CMOS logic, no pullup is necessary, see Fig. 5.

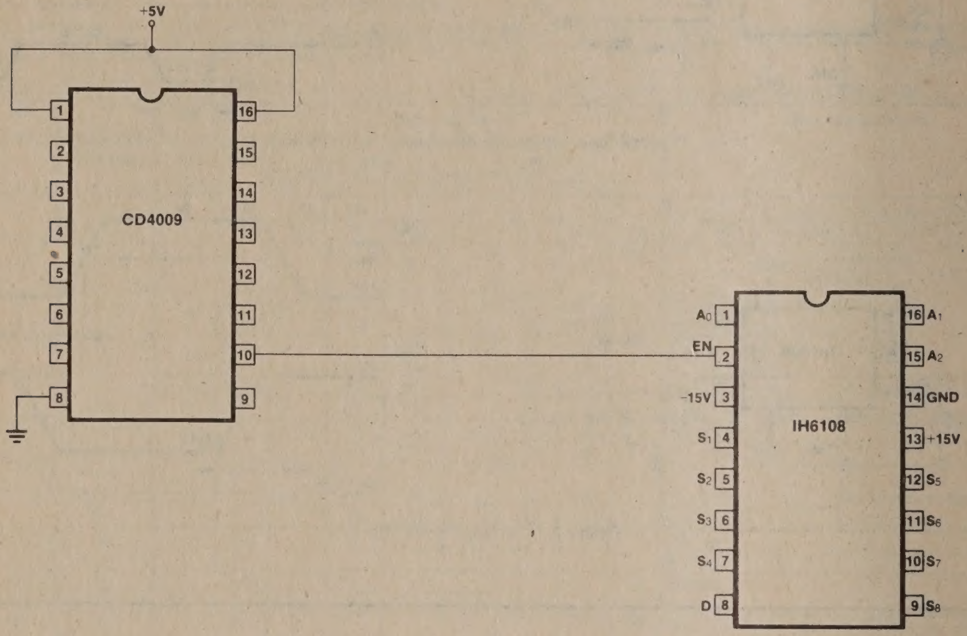

+5V
CD4009
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
IH6108
A0 1
EN 2
-15V 3
S1 4
S2 5
S3 6
S4 7
D 8
16 A1
15 A2
14 GND
13 +15V
12 S5
11 S6
10 S7
9 S8

Figure 5. Enable Input Strobing from CMOS Logic

The supply voltage of the CD4009 affects the switching speed of the IH6108; the same is true for TTL supply voltage levels. The chart below shows the effect, on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY VOLTAGE	TYPICAL t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the Enable Strobe Logic.

The examples shown in Figures 4 and 5 deal with enable strobing when expanding to more than eight channels is required; in these cases the EN terminal acts as a fourth binary input. If eight channels or less are being multiplexed, the EN terminal can be directly connected to +5V logic supply to enable the IH6108 at all times.

IH6108 APPLICATION INFORMATION (CONT.)

APPLICATIONS

II. Using the IH6108 with supplies other than ±15V

The IH6108 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done the binary input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 13) via a silicon diode as shown in Figure 6. When using this type of configuration, a further requirement must be met - the strobe levels at A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 6 the EN voltage is 11.3V which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6108 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6108 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN. (See Figure 7) A 1μF capacitor can be placed across the diode to minimize switching glitches.

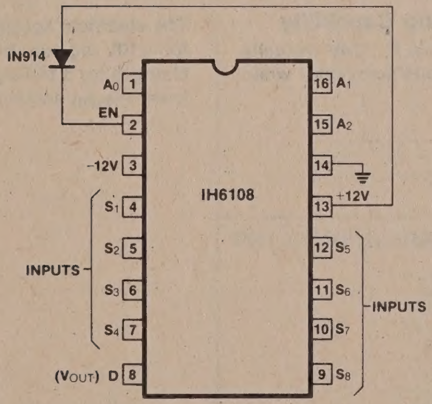


Figure 6. IH6108 Connection Diagram for less than ±15V Supply Operation.

IH6108 APPLICATION INFORMATION (CONT.)

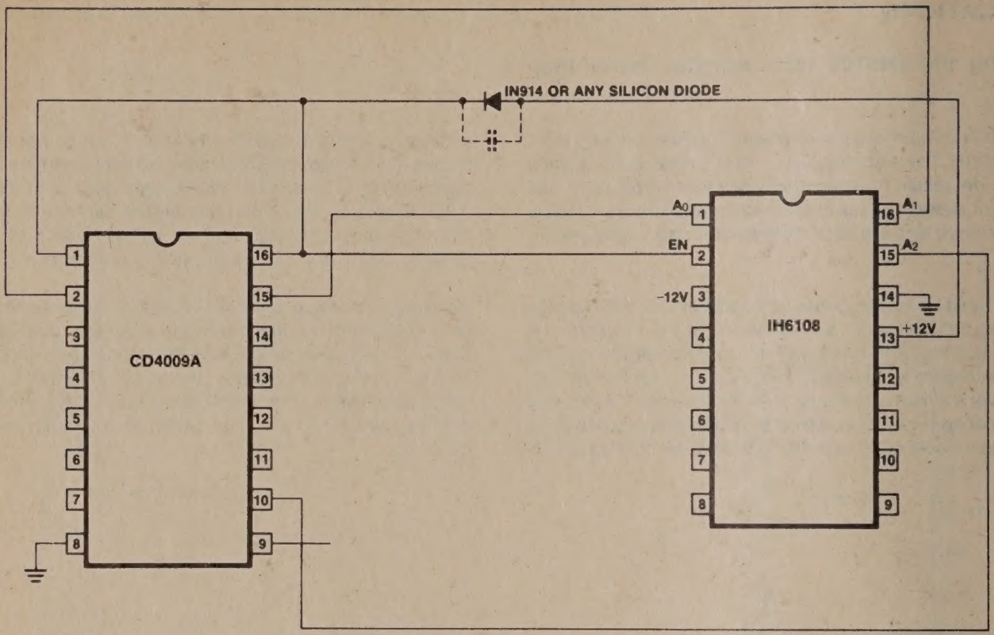

IN914 OR ANY SILICON DIODE
CD4009A
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
A0
EN
-12V
IH6108
A1
A2
+12V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9

Figure 7. IH6108 Connection Diagram with Enable Input Strobing for less than ±15V Supply Operation.

III. Peak-to-Peak Signal Handling Capability

The IH6108 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6108 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

IH6116
16 Channel CMOS Analog Multiplexer (One out of 16)

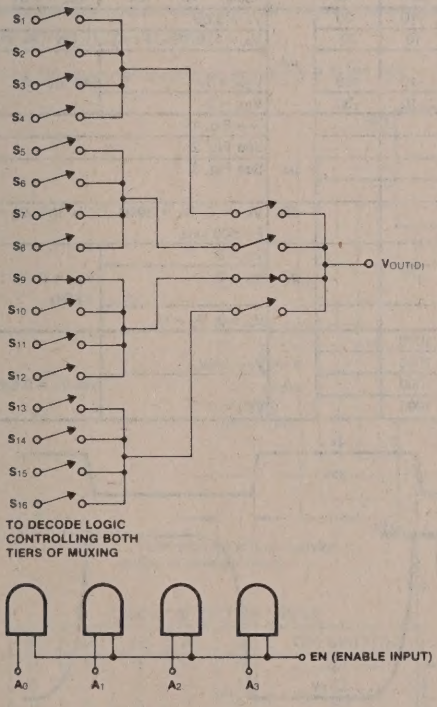
FEATURES

- **Pin compatible with DG506, HI-506 & AD7506**
- **Ultra Low Leakage — $I_{D(off)} \le 100pA$**
- **±11 analog signal range**
- **$r_{DS(on)}$ <700 ohms over full signal and temperature range**
- **Break before make switching**
- **TTL and CMOS compatible strobe control**
- **Binary strobe control (4 strobe inputs control 16 channels)**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than $100\mu A$**
- **No SCR latchup**

GENERAL DESCRIPTION

The IH6116 is a CMOS monolithic, one of 16 multiplexer. The part is a plug-in replacement for the DG506. Four line binary decoding is used so that the 16 channels can be controlled by 4 strobe inputs; additionally a fifth input is provided to use as a system enable. When the enable input is high (5V) the channels are sequenced by the 4 line strobe inputs, and when low (0V), all channels are off. The 4 strobe inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the enable input (EN) must be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM


S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
VOUT(D)
TO DECODE LOGIC CONTROLLING BOTH TIERS OF MUXING
EN (ENABLE INPUT)
A0
A1
A2
A3

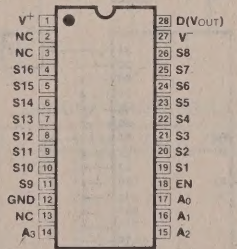
4 LINE BINARY STROBE INPUTS
(0 0 0 1) AND EN @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 9 TURNED ON

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
x	x	x	x	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \ge 3.0V$ $V_{ENH} \ge 4.5V$
Logic "0" = $V_{AL} \le 0.8V$

PIN CONFIGURATION (Outline drawings DI, PI)


V+ 1
NC 2
NC 3
S16 4
S15 5
S14 6
S13 7
S12 8
S11 9
S10 10
S9 11
GND 12
NC 13
A3 14
28 D(VOUT)
27 V−
26 S8
25 S7
24 S6
23 S5
22 S4
21 S3
20 S2
19 S1
18 EN
17 A0
16 A1
15 A2

TOP VIEW
V+ COMMON TO SUBSTRATE

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6116MDI	−55°C to +125°C	28 pin Ceramic DIP
IH6116CDI	0°C to 70°C	28 pin Ceramic DIP
IH6116CPI	0°C to 70°C	28 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground .... −15V to 15V
V_S or V_D to V^+ .... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground .... −16V
Current (Any Terminal) 30mA
Current (Analog Drain) 20mA
Current (Analog Source) 20mA
Operating Temperature .... −55 to 125°C
Storage Temperature .... −65 to 150°C
Power Dissipation (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V^1$, Ground = 0V, unless otherwise specified.

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS						UNIT	TEST CONDITIONS	
					M SUFFIX			C SUFFIX					
					−55°C	25°C	125°C	0°C	25°C	70°C			
SWITCH	$r_{DS(ON)}$	S to D	16	480	600	600	700	650	650	750	Ω	$V_D = 10V$, $I_S = -10mA$	Sequence each switch on
			16	300	600	600	700	650	650	750		$V_D = -10V$, $I_S = 10mA$	$V_{AL} = 0.8V$, $V_{AH} = 3V$
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(OFF)}$	S	16	0.01		0.1	50		0.2	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
			16	0.01		0.1	50		0.2	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(OFF)}$	D	1	0.1		0.2	100		0.4	100		$V_D = 10V$, $V_S = -10V$	
			1	0.1		0.2	100		0.4	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(ON)}$	D	16	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
			16	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 3V$
INPUT	$I_{A(on)}$ or $I_{A(off)}$	A_0 A_1 A_2 A_3	4	.01		−10	−30		−10	−30	µA	$V_A = 3.0V$	
			4	.01		10	30		10	30		$V_A = 15V$	
	I_A		4			−10	−30		−10	−30		$V_{EN} = 5V$	All $V_A = 0$
		EN	1			−10	−30		−10	−30		$V_{EN} = 0$	
DYNAMIC	t_{trans}	D		0.6		1					µs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{EN(on)}$	D		0.8		1.5						See Fig. 3	
	$t_{EN(off)}$	D		0.3		1							
	"OFF" Isolation	D		60							dB	$V_{EN} = 0$, $R_L = 200Ω$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 kHz	
	$C_s(OFF)$	S		5							pF	$V_S = 0$	$V_{EN} = 0$, f = 140 kHz to 1 MHz
	$C_d(OFF)$	D		40								$V_D = 0$	
	$C_{ds}(OFF)$	D to S		1								$V_S = 0$, $V_D = 0$	
SUPPLY	Supply Current +	I^+	1	55		200			1000		µA	$V_{EN} = 5V$	All $V_A = 0$ OR 3V
	Supply Current −	I^-	1	2		100			1000				
	Standby Current +	I^+_{SB}	1	1		100			1000			$V_{EN} = 0$	
	Standby Current −	I^-_{SB}	1	1		100			1000				

NOTE 1: See Section V. Enable Input Strobing Levels.

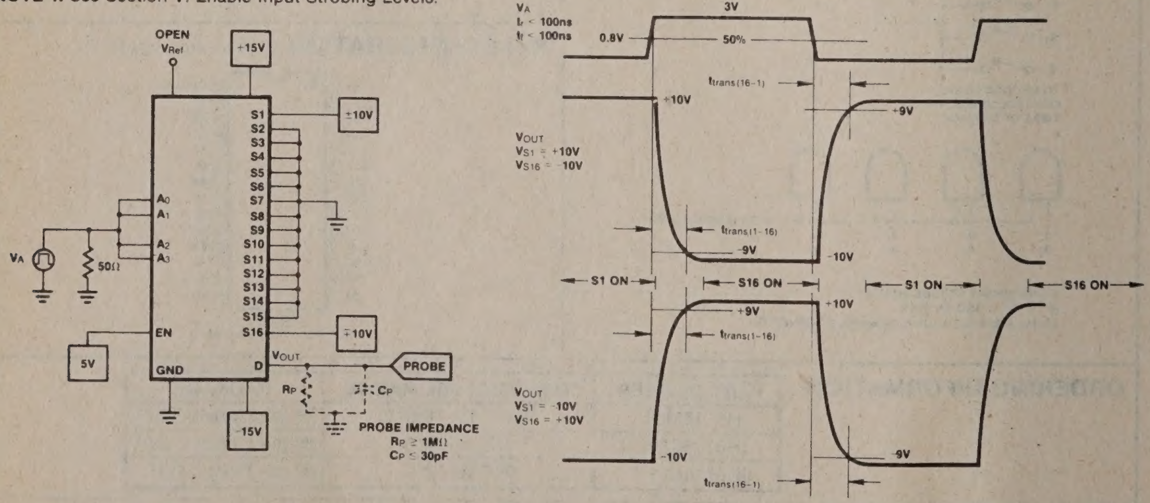

OPEN
V_{Ref}
+15V
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
±10V
∓10V
A_0
A_1
A_2
A_3
V_A
50Ω
EN
5V
GND
D
−15V
V_{OUT}
PROBE
R_P
C_P
PROBE IMPEDANCE
$R_P \geq 1MΩ$
$C_P \leq 30pF$
V_A
$t_r < 100ns$
$t_f < 100ns$
3V
0.8V
50%
$t_{trans(16-1)}$
+10V
+9V
V_{OUT}
$V_{S1} = +10V$
$V_{S16} = -10V$
$t_{trans(1-16)}$
−9V
−10V
S1 ON
S16 ON
S1 ON
S16 ON
+10V
+9V
$t_{trans(1-16)}$
V_{OUT}
$V_{S1} = -10V$
$V_{S16} = +10V$
−10V
−9V
$t_{trans(16-1)}$

Figure 1

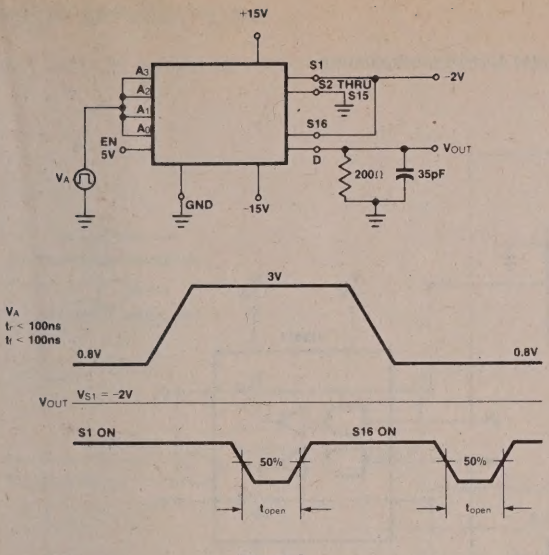

+15V
A3
A2
A1
A0
EN
5V
VA
S1
S2 THRU S15
-2V
S16
D
VOUT
200Ω
35pF
GND
-15V
3V
VA
tr < 100ns
tf < 100ns
0.8V
0.8V
VOUT
VS1 = -2V
S1 ON
S16 ON
50%
50%
topen
topen

Figure 2

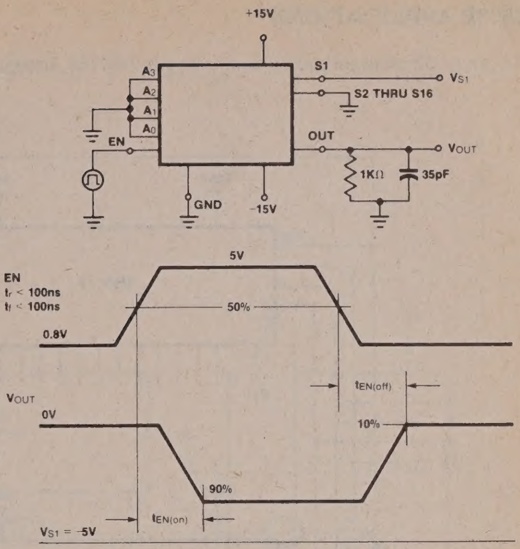
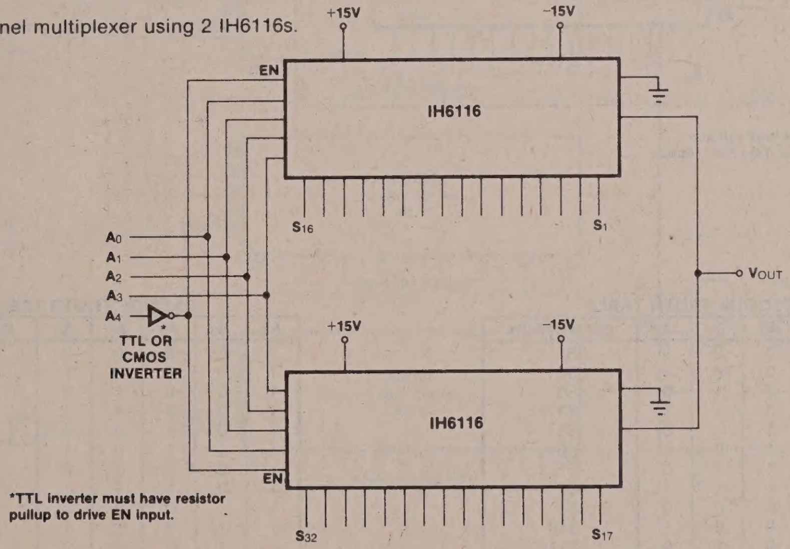

+15V
A3
A2
A1
A0
EN
S1
VS1
S2 THRU S16
OUT
VOUT
1KΩ
35pF
GND
-15V
5V
EN
tr < 100ns
tf < 100ns
50%
0.8V
tEN(off)
VOUT
0V
10%
90%
tEN(on)
VS1 = -5V

Figure 3

IH6116 APPLICATIONS

I. 1 out of 32 channel multiplexer using 2 IH6116s.


+15V
-15V
EN
IH6116
S16
S1
A0
A1
A2
A3
A4
TTL OR CMOS INVERTER
VOUT
+15V
-15V
IH6116
EN
S32
S17

*TTL inverter must have resistor pullup to drive EN input.

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

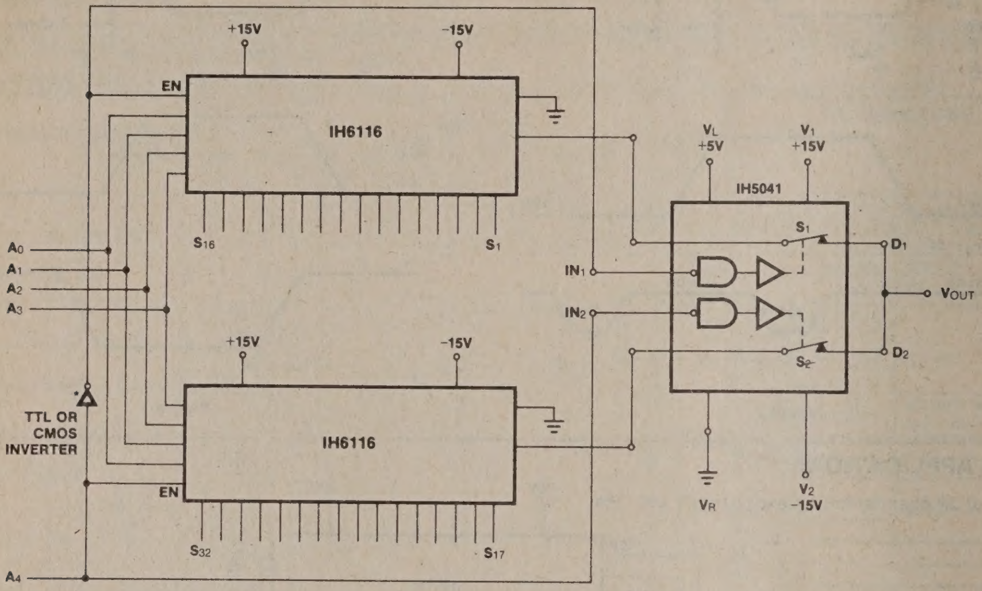
DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 4

IH6116 APPLICATIONS

II. 1 out of 32 channel multiplexer using 2 IH6116s; using an IH5041 for submultiplexing.


+15V
−15V
EN
IH6116
S16
S1
A0
A1
A2
A3
*
TTL OR CMOS INVERTER
+15V
−15V
IH6116
EN
S32
S17
A4
IN1
IN2
VL +5V
V1 +15V
IH5041
S1
S2
D1
D2
VOUT
VR
V2 −15V

*TTL gate must have resistor pullup to +5V to drive "EN" input.

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 5

IH6116 APPLICATIONS

III. 1 out of 64 multiplexer using 4 1/16s and IH5053 as submultiplexer.

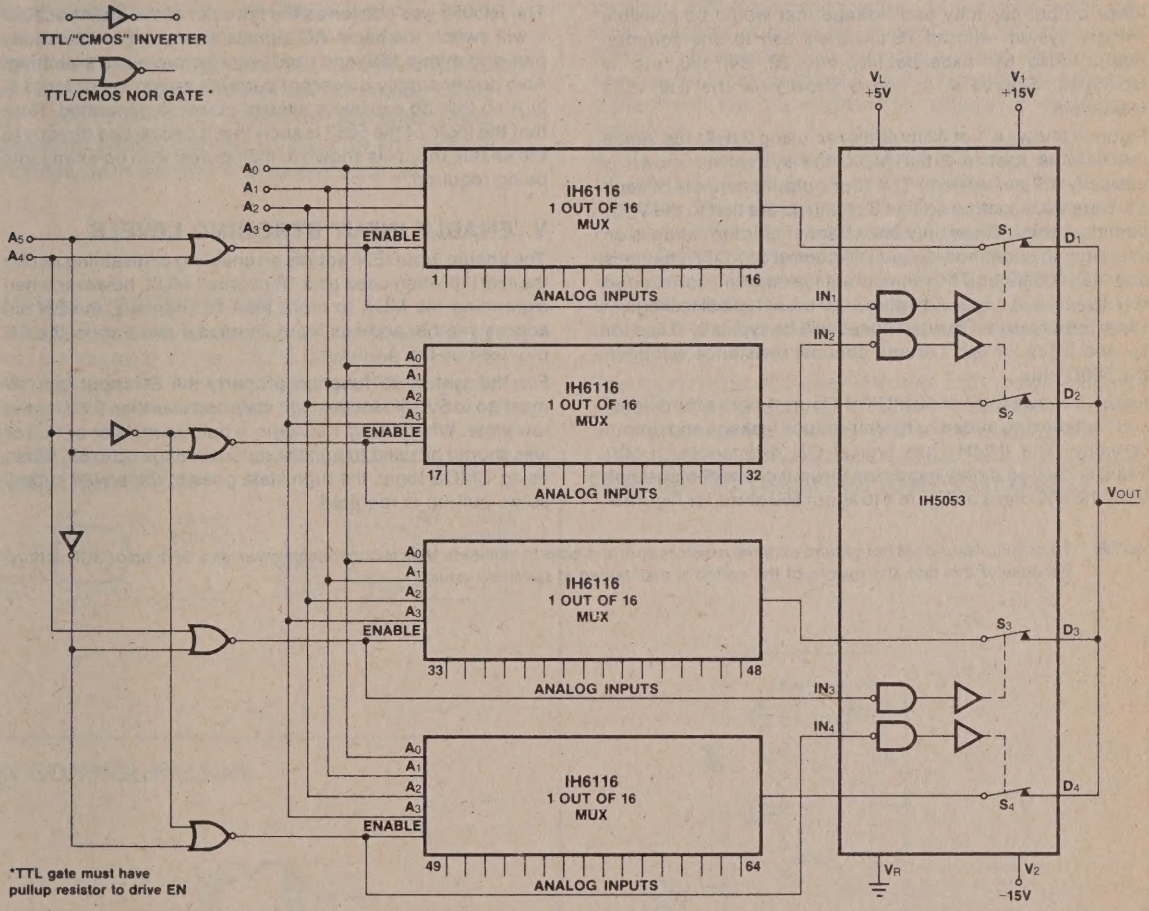

TTL/"CMOS" INVERTER
TTL/CMOS NOR GATE *
A0
A1
A2
A3
A5
A4
ENABLE
IH6116
1 OUT OF 16
MUX
1
16
ANALOG INPUTS
17
32
33
48
49
64
VL
+5V
V1
+15V
S1
S2
S3
S4
D1
D2
D3
D4
IN1
IN2
IN3
IN4
IH5053
VOUT
VR
V2
−15V
*TTL gate must have
pullup resistor to drive EN

Figure 6

IV. GENERAL NOTE ON EXPANDABILITY OF IH6116

The IH6116 is a two tier multiplexer, where sixteen input channels are routed to a common output in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied together. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this is lower output capacity and leakage that would be possible using a system with all 16 channels tied to one common output. Also the expandability into 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the IH6116 is expanded.

Figure 4 shows a 1 of 32 multiplexer, using 2 IH6116s. Since the 6116 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. The four output channels of each 6116 are tied together so that 8 channels are tied to the V_{OUT} common point. Since only one channel of information is on at a time, the common output will consist of 7 OFF channels and 1 ON channel. Thus the output leakage will correspond to 7 $I_{D(offs)}$ and 1 $I_{D(on)}$, or about 1.0 nA of typical leakage at room temperature. Thruput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}. Thruput channel resistance will be in the 500Ω area.

Figure 5 shows the 1 of 32 MUX of Figure 4, with a third tier of submultiplexing added to further reduce leakage and output capacity. The IH5041 has typical ON resistances of 50Ω (max. is 75Ω) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2 nA.

Figure 6 shows a 1 of 64 MUX using 3 tier MUXing (similar to Figure 5). The Intersil IH5053 is used to get the third tier of MUXing. The V_{OUT} point will see 3 OFF channels and 1 ON channel at any one time, so that the typical leakages will be about 0.4 nA. Thruput channel resistance will be in the 550 ohm area with thruput switching speeds about 1.3μs for ON time and 0.8μs for OFF time.

The IH5053 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6116 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are on the order of 1-2μA so that no excessive system power is generated. Note that the logic of the 5053 is such that it can be tied directly to the enable input (as shown in the figures) with no extra logic being required.

V. ENABLE INPUT STROBING LEVELS

The enable input (EN) acts as an enabling or disabling pin for the IH6116 when used as a 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 4 and 5 show the EN pin used as the A4 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up resistor of 1kΩ or less should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.

IH6201
Dual CMOS Driver/ Voltage Translator

FEATURES

- **Driven direct from TTL or CMOS logic**
- **Translates logic levels up to 30V levels**
- **Switches $20V_{ACPP}$ signals when used in conjunction with Intersil IH401A Varafet (as an analog gate)**
- **$t_{ON} \leq 300nS$ & $t_{OFF} \leq 200nS$ for 30V level shifts**
- **Quiescent supply current ≤ 100μa for any state (d.c.)**
- **Provides both normal & inverted outputs**

GENERAL DESCRIPTION

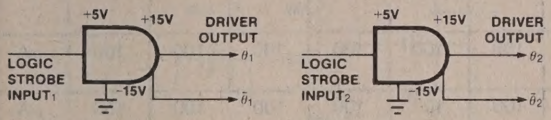
The IH6201 is a CMOS, Monolithic, Dual Voltage Translator; it takes the low level TTL or CMOS logic level and converts them to higher levels (i.e. to ±15V swings). This translator is typically used in making solid state switches, or analog gates.

When used in conjunction with the Intersil IH401 family Varafets, the combination makes a complete solid state switch capable of switching signals up to 22Vpp and up to 20MHz in frequency. This switch is a "break-before-make" type (i.e. t_{off} time < t_{on} time). The combination has typical $t_{off} \approx 80nS$ and typ. $t_{on} \approx 200nS$ for signals up to 20Vpp in amplitude.

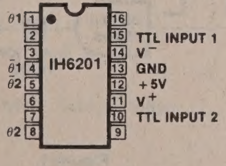
A TTL "1" input strobe will force the θ driver output up to V^+ level; the $\bar{\theta}$ output will be driven down to the V^- level. When the TTL input goes to "0", the θ output goes to V^- and $\bar{\theta}$ goes to V^+; thus θ and $\bar{\theta}$ are 180° out of phase with each other. These complementary outputs can be used to create a wide variety of functions such as SPDT and DPDT switches, etc.; alternatively the complementary outputs can be used to drive an N and P channel Mosfet, to make a complete Mosfet analog gate.

The driver typically uses +5V and ±15V power supplies; however a wide range of V^+ and V^- is possible, however $V^+ > 5V$ is necessary for the driver to work properly.

BLOCK DIAGRAM


+5V
+15V
DRIVER OUTPUT
θ1
LOGIC STROBE INPUT1
-15V
θ̄1
+5V
+15V
DRIVER OUTPUT
θ2
LOGIC STROBE INPUT2
-15V
θ̄2

PIN CONFIGURATION


θ1 1
2
3
θ̄1 4
θ̄2 5
6
7
θ2 8
IH6201
16
15 TTL INPUT 1
14 V−
13 GND
12 +5V
11 V+
10 TTL INPUT 2
9

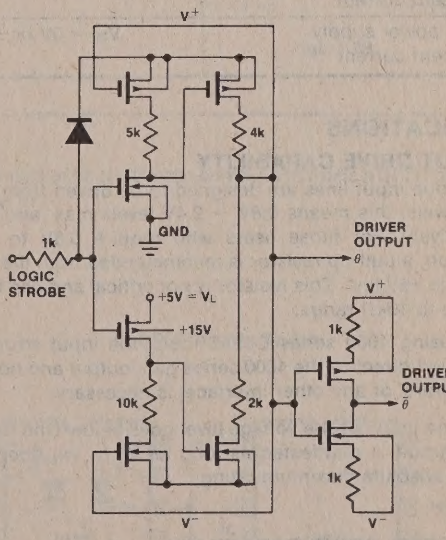
OUTLINE DWGS
DE, JE, PE

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE
*IH6201CDE	0°C to 70°C
*IH6201MDE	−55°C → +125°C
IH6201CJE	0°C to 70°C
IH6201MJE	−55°C to 125°C
IH6201CPE	0°C to 70°C

*Special Order Only

SCHEMATIC DIAGRAM (ONE CHANNEL)


V+
5k
4k
GND
1k
LOGIC STROBE
DRIVER OUTPUT
θ
+5V = VL
+15V
V+
1k
DRIVER OUTPUT
θ̄
10k
2k
1k
V−
V−

ABSOLUTE MAXIMUM RATINGS

V^+ to V^-	35V
V^+	35V
V^-	35V
V^+ to V_{IN}	40V
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$

ITEM	CONDITIONS	IH6201CDE			IH6201MDE			UNITS
		−25°C	+25°C	+85°C	−55°C	+25°C	+125°C	
θ or $\bar{\theta}$ driver output swing	$V_{IN} = 0V$ $\overset{+3V}{\sqcap}$ fig. 2B	28	28	28	28	28	28	Vpp
V_{IN} strobe level ("1") for proper translation	$\theta \geq 14V$ $\bar{\theta} \geq -14V$	3.0	3.0	3.0	2.4	2.4	2.4	$V_{D.C.}$
V_{IN} strobe level ("0") for proper translation	$\theta \geq -14V$ $\bar{\theta} \geq 14V$	0.4	0.4	0.4	0.8	0.8	0.8	$V_{D.C.}$
I_{IN} input strobe current draw (for 0V → 5V range)	V_{IN} = 0V or +5V	1	1	1	1	1	1	μA
t_{on} time	$V_{IN} = 0V$ $\overset{3V}{\underset{4\mu s}{\sqcap}}$ $C_L = 30pf$ switching turn-on time fig. 2B	400	400	400	300	300	300	nS
t_{off} time	$V_{IN} = 0V$ $\overset{+3V}{\underset{4\mu s}{\sqcap}}$ $C_L = 30pf$ switching turn-off time fig. 2B	300	300	300	200	200	200	nS
I^+ (V^+) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA
I^- (V^-) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA
I_L (V_L) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA

APPLICATIONS

I. INPUT DRIVE CAPABILITY

The strobe input lines are designed to be driven from TTL logic levels; this means 0.8V → 2.4V levels max. and min. respectively. For those users who require 0.8V to 2.0V operation, a pull-up resistor is recommended from the TTL output to +5V line. This resistor is not critical and can be in the 1kΩ to 10kΩ range.

When using 4000 series CMOS logic, the input strobe is connected direct to the 4000 series gate output and no pull up resistors, or any other interface, is necessary.

When the input strobe voltage level goes below Gnd (i.e. to −15V) circuit is unaffected as long as V^+ to V_{IN} does not exceed absolute maximum rating.

II. OUTPUT DRIVE CAPABILITY

The translator output is designed to drive the Intersil IH401 family of Varafets; these are N-channel J-FETS with built-in driver diodes. Driver diodes are necessary to isolate the signal source from the driver/translator output; this prevents forward biasing between the signal input and the +Vcc supply. The IH6201 will drive any J-FET provided some sort of isolation is added i.e.

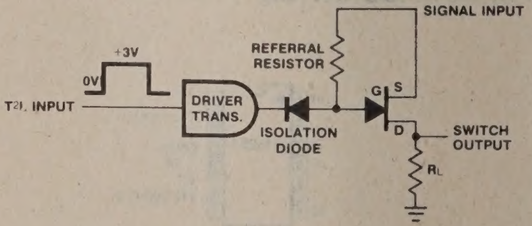


Figure 1

You will notice in Figure 1 that a "referral" resistor has been added from 2N4391 gate to its source. This resistor is needed to compensate for inadequate charge area curve for isolation diode (i.e. if C vs. V plot for diode ≤ 2 [C vs. V plot for output J-FET] switch won't function; then adding this resistor overcomes this condition. The "referral" resistor is normally in the 100kΩ to 1MΩ range and is not too critical.

III. MAKING A COMPLETE SOLID STATE SWITCH THAT CAN HANDLE 20Vpp SIGNALS

The limitation on signal handling capability comes from the output gating device. When a J-FET is used, it's the pinch-off of the J-FET acting with the V^- supply that does the

APPLICATIONS, CONTINUED

limiting. In fact max. signal handling capability = 2 $(V_p + (V^-))$ Vpp where V_p = pinch-off voltage of J-FET chosen. i.e. $V_p = 7V$, $V^- = -15V$ ∴ max. signal handling = 2 (7V + (−15V)) Vpp = 2(7V−15)pp=2(−8Vpp)=16Vpp. Obviously to get ≥ 20Vpp, $V_p \geq 5V$ with $V^- = -15V$. Another simple way to get 20Vpp with $V_p = 7V$, is to increase V^- to −17V. In fact using $V^+ = +12V$ or +15V and setting $V^- = -18V$ allows one to switch 20Vpp with any member of IH401 family. The advantage of using the $V_p = 7V$ pinch-off (along with unsymmetrical supplies) over the $V_p = 5V$ pinch-off (and ±15V supplies) is that you will have a much lower $R_{DS(ON)}$ resistance for the V_p=7V fet.(i.e. for the 2N4391 fet

$r_{DS(ON)} \approx 22\Omega$, $r_{DS(ON)} \approx 35\Omega$)
$V_p = 7V$ $V_p = 5V$

The IH6201 is a dual translator, each containing 4 CMOS FETs. The schematic of one-half IH6201, driving one-fourth of an IH401, is shown in Figure 2A.

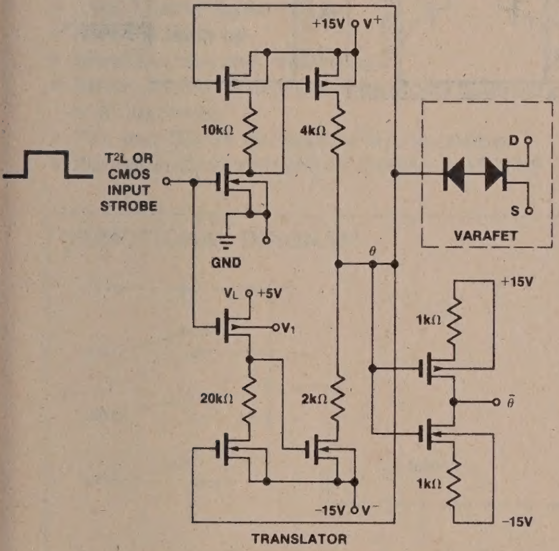
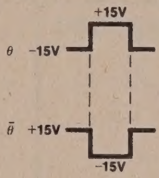

+15V V+
10kΩ
4kΩ
T²L OR CMOS INPUT STROBE
D
S
VARAFET
GND
θ
VL +5V
V1
+15V
1kΩ
20kΩ
2kΩ
θ̄
1kΩ
−15V V−
−15V
TRANSLATOR

Figure 2A


+15V
θ −15V
θ̄ +15V
−15V

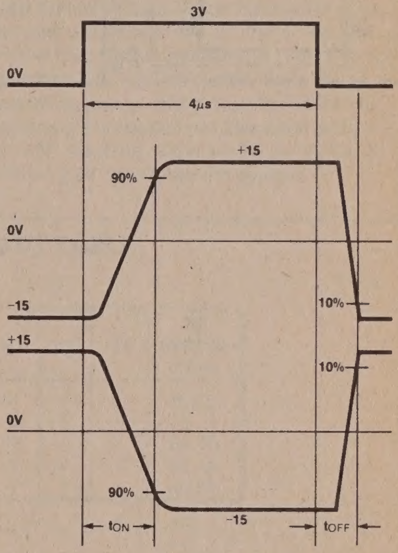
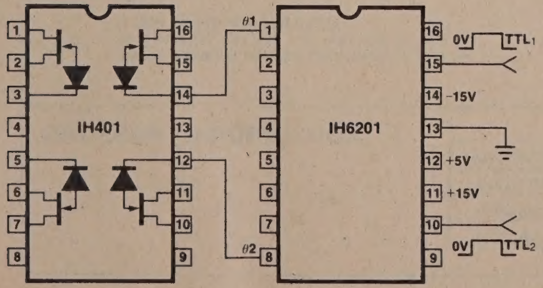


Figure 2B

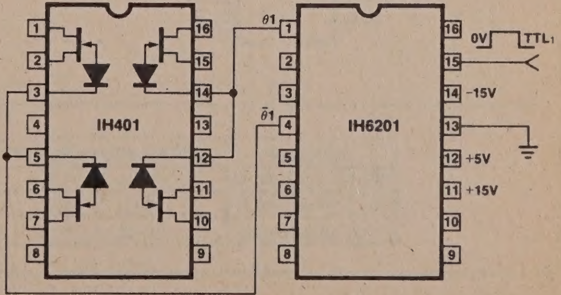
NOTE: Each translator output has a θ and θ̄ output. θ is just the inverse of θ̄.

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See III.)

I. Dual SPST Analog Switch


IH401
IH6201
θ1
θ2
0V TTL1
−15V
+5V
+15V
0V TTL2

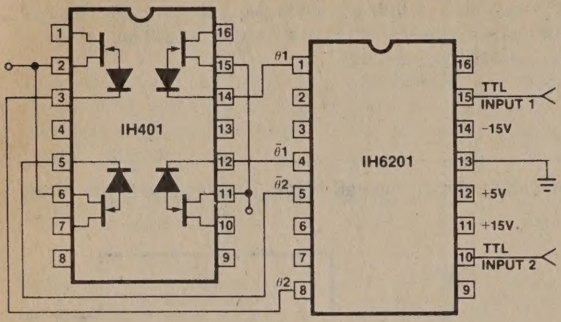
II. DPDT Analog Switch


IH401
IH6201
θ1
θ̄1
0V TTL1
−15V
+5V
+15V

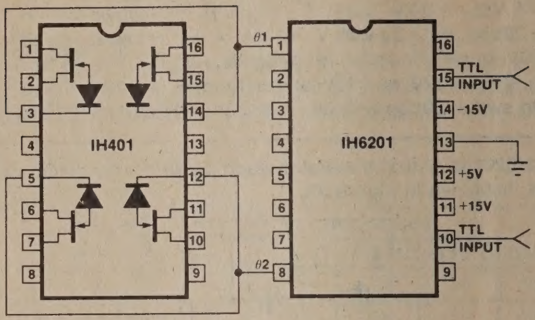
NOTE: Either switch is turned on when strobe input goes high.

APPLICATIONS, CONTINUED

III. Dual SPDT


IH401
IH6201
θ1
θ̄1
θ̄2
θ2
TTL INPUT 1
TTL INPUT 2
-15V
+5V
+15V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

IV. Dual DPST


IH401
IH6201
θ1
θ2
TTL INPUT
TTL INPUT
-15V
+5V
+15V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

IH6208
4-Channel Differential CMOS Analog Multiplexer

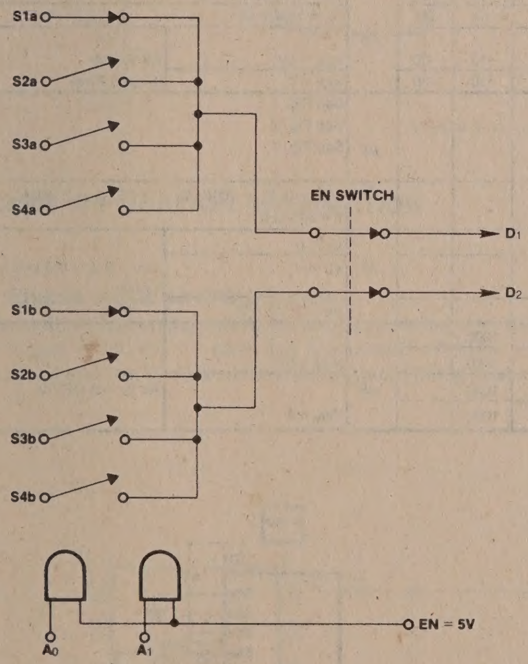
FEATURES

- Ultra low leakage — $I_{D(off)} \leq 100pA$
- $r_{DS(on)} < 400$ ohms over full signal and temperature range
- Power supply quiescent current less than $100\mu A$
- ±14V analog signal range
- No SCR latch up
- Break before make switching
- Binary strobe control (2 strobe inputs controls 2 out of 8 channels).
- TTL and CMOS compatible strobe control
- Pin compatible with HI509, DG509 & AD7509

GENERAL DESCRIPTION

The IH6208 is a monolithic 2 of 8 CMOS multiplexer. The part is a plug-in replacement for the DG509. Two line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided to use as a system enable. When the enable input is high (5V) the channels are sequenced by the 2 line binary inputs, and when low (0V) all channels are off. The 2 strobe inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the enable input (EN) must be taken to 5V to enable the system, and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM



2 LINE BINARY STROBE INPUTS
(0 0) AND EN = 5V (EN = "1" FOR +5V, "0" FOR 0V)
ABOVE EXAMPLE SHOWS CHANNELS 1a & 1b ON.

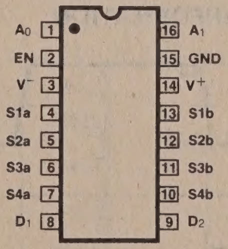
DECODE TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1

LOGIC "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
LOGIC "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (Outline drawings DE, PE)



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6208MDE	−55°C to +125°C	16 pin Ceramic DIP
IH6208CDE	0°C to 70°C	16 pin Ceramic DIP
IH6208CPE	0°C to 70°C	16 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground .... −15V, V_1
V_S or V_D to V^+ .... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground .... −16V
Current (Any Terminal) .... 30 mA
Current (Analog Drain) .... 20 mA
Current (Analog Source) .... 20 mA
Operating Temperature .... −55 to 125°C
Storage Temperature .... −65 to 150°C
Power Dissipation (Package)* .... 1200 mW
*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V^1$, Ground = 0V, unless otherwise specified.

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS						UNIT	TEST CONDITIONS	
					M SUFFIX			C SUFFIX					
					−55°C	25°C	125°C	0°C	25°C	70°C			
SWITCH	$r_{DS(ON)}$	S to D	8	180	300	300	400	350	350	450	Ω	$V_D = 10V$, $I_S = -1.0$ mA	Sequence each switch on $V_{AL} = 0.8V$, $V_{AH} = 2.4V$
			8	150	300	300	400	350	350	450		$V_D = -10V$, $I_S = -1.0$ mA	
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(OFF)}$	S	8	0.002		0.05	50		0.1	50	NA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
			8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(OFF)}$	D	2	0.03		0.1	50		0.2	100		$V_D = 10V$, $V_S = -10V$	
			2	0.03		0.1	50		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(ON)}$	D	8	0.1		0.2	50		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on $V_{AL} = 0.8V$, $V_{AH} = 2.4V$
			8	0.1		0.2	50		0.4	100		$V_{S(All)} = V_D = -10V$	
INPUT	$I_{A(on)}$		2	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
	$I_{A(off)}$		2	.01		10	30		10	30		$V_A = 15V$ or 0V	
	I_A	A0, A1	2			−10	−30		−10	−30		$V_{EN} = 5V$	All $V_A = 0$ (Strobe Pins)
		EN	1			−10	−30		−10	−30		$V_{EN} = 0$	
DYNAMIC	t_{trans}	D		0.3		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{EN(on)}$	D		0.6		1.5						See Fig. 3	
	$t_{EN(off)}$	D		0.4		1							
	"OFF" Isolation	D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3$ pF, $V_S = 3$ VRMS, f = 500 kHz	
	$C_{s(off)}$	S		5							pF	$V_S = 0$	$V_{EN} = 0$, f = 140 kHz to 1 MHz
	$C_{d(off)}$	D		12								$V_D = 0$	
	$C_{ds(off)}$	D to S		1								$V_S = 0$, $V_D = 0$	
SUPPLY	Supply Current +	I^+	1	40		200			1000		μA	$V_{EN} = 5V$	All V_A = 0 OR 5V
	Supply Current −	I^-	1	2		100			1000				
	Standby Current +	I^+_{SB}	1	1		100			1000			$V_{EN} = 0$	
	Standby Current −	I^-_{SB}	1	1		100			1000				

NOTE 1: See Section I Enable Input Strobing Levels.

SWITCHING INFORMATION

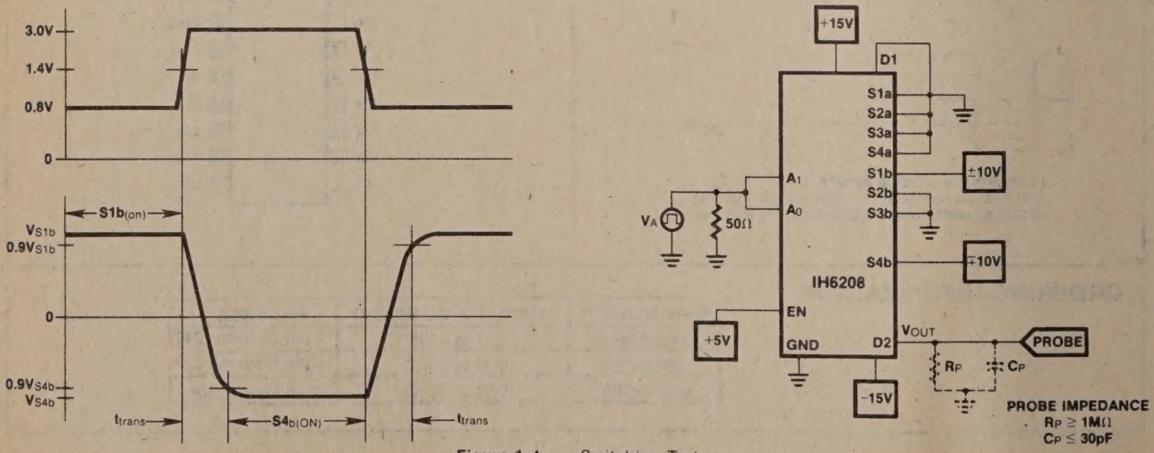


Figure 1. t_{trans} Switching Test

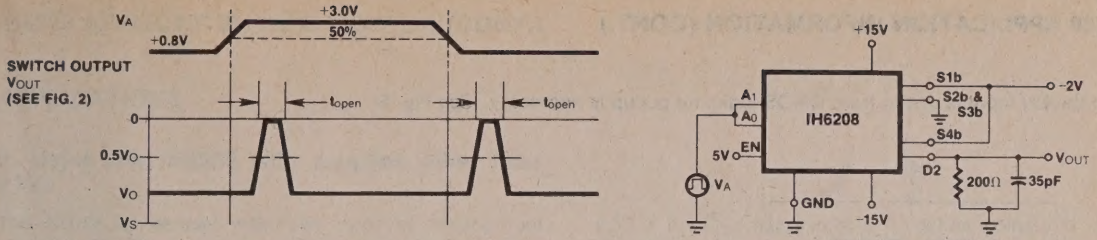

VA
+3.0V
50%
+0.8V
SWITCH OUTPUT
VOUT
(SEE FIG. 2)
topen
topen
0
0.5VO
VO
VS
+15V
IH6208
A1
A0
EN
5V
VA
S1b
S2b &
S3b
S4b
D2
-2V
VOUT
200Ω
35pF
GND
-15V

Figure 2. t_{open} (Break-Before-Make) Switching Test

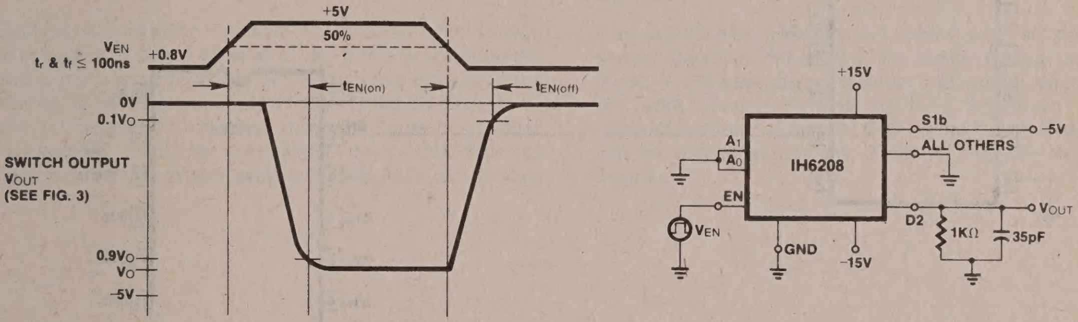

+5V
50%
VEN
tr & tf ≤ 100ns
+0.8V
tEN(on)
tEN(off)
0V
0.1VO
SWITCH OUTPUT
VOUT
(SEE FIG. 3)
0.9VO
VO
-5V
+15V
IH6208
A1
A0
EN
VEN
S1b
ALL OTHERS
-5V
VOUT
D2
1KΩ
35pF
GND
-15V

Figure 3. t_{on} and t_{off} Switching Test

IH6208 APPLICATION INFORMATION

I. Enable Input Strobing Levels

The enable input on the IH6208 requires a minimum of +4.5V to trigger it into the "1" state and a maximum of +0.8V to trigger it into the "0" state. If the enable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 4).

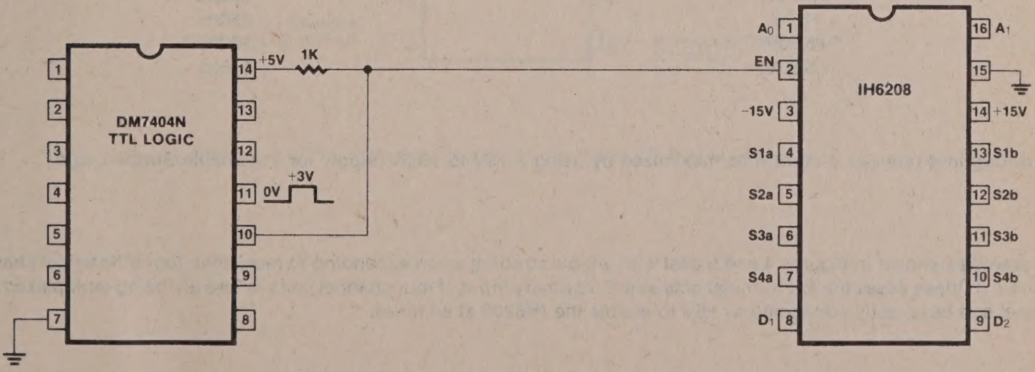

DM7404N
TTL LOGIC
1
2
3
4
5
6
7
8
9
10
11
12
13
14
+5V
1K
+3V
0V
IH6208
A0
EN
-15V
S1a
S2a
S3a
S4a
D1
A1
+15V
S1b
S2b
S3b
S4b
D2
16
15

Figure 4. Enable Input Strobing from TTL Logic

IH6208 APPLICATION INFORMATION (CONT.)

When the EN input is driven from CMOS logic, no pullup is necessary. (See Fig. 5)

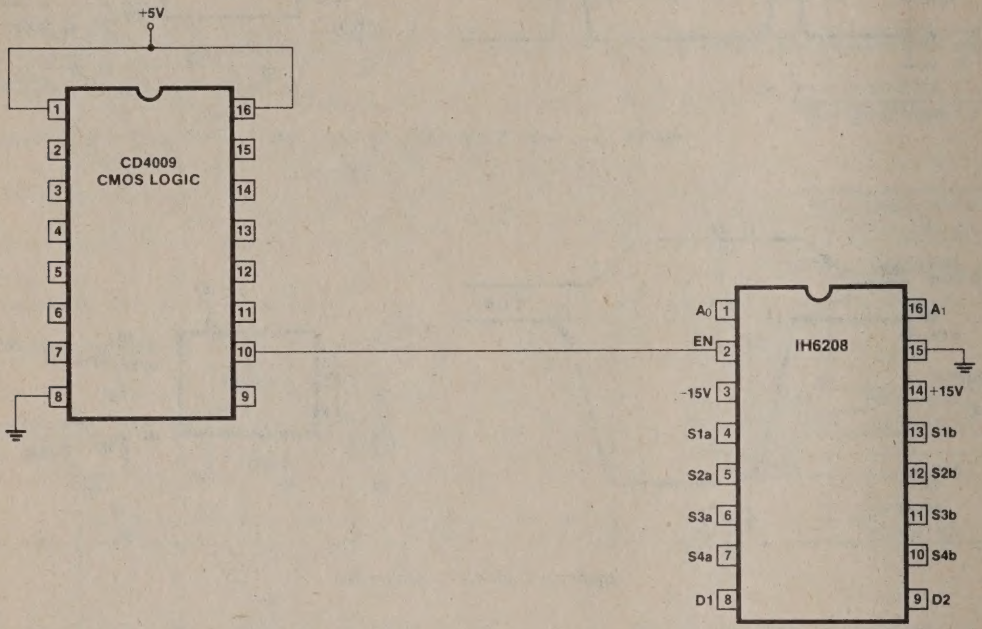

+5V
CD4009
CMOS LOGIC
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
IH6208
A0 1
EN 2
-15V 3
S1a 4
S2a 5
S3a 6
S4a 7
D1 8
16 A1
15
14 +15V
13 S1b
12 S2b
11 S3b
10 S4b
9 D2

Figure 5

The supply voltage of the CD4009 affects the switching speed of the IH6208; the same is true for TTL supply voltage levels. The chart below shows the effect on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY	TYPICAL t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.0V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the Enable Strobe Logic.

The examples shown in Figures 4 and 5 deal with enable strobing when expanding to more than four differential channels is required; in these cases the EN terminal acts as a third binary input. If four channel pairs or less are being multiplexed, the EN terminal can be directly connected to +5V to enable the IH6208 at all times.

IH6208 APPLICATION INFORMATION (CONT.)

APPLICATIONS

II. Using the IH6208 with supplies other than ±15V

The IH6208 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done the binary input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 14) via a silicon diode as shown in Figure 6. A further requirement must be met when using this type of configuration; the strobe levels at A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 6 the EN voltage is 11.3V, which means that logic high at A0 and A1 is ≈ +8.8V (logic low continues to be ≈ 0.8V). In this configuration the IH6208 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6208 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN (See Figure 7). A 1μF capacitor can be placed across the diode to minimize switching glitches.

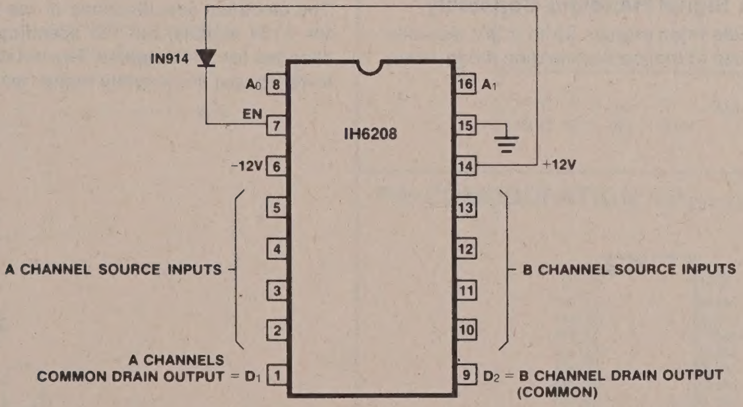


Figure 6. IH6208 Connection Diagram for less than ±15V Supply Operation.

IH6208 APPLICATION INFORMATION

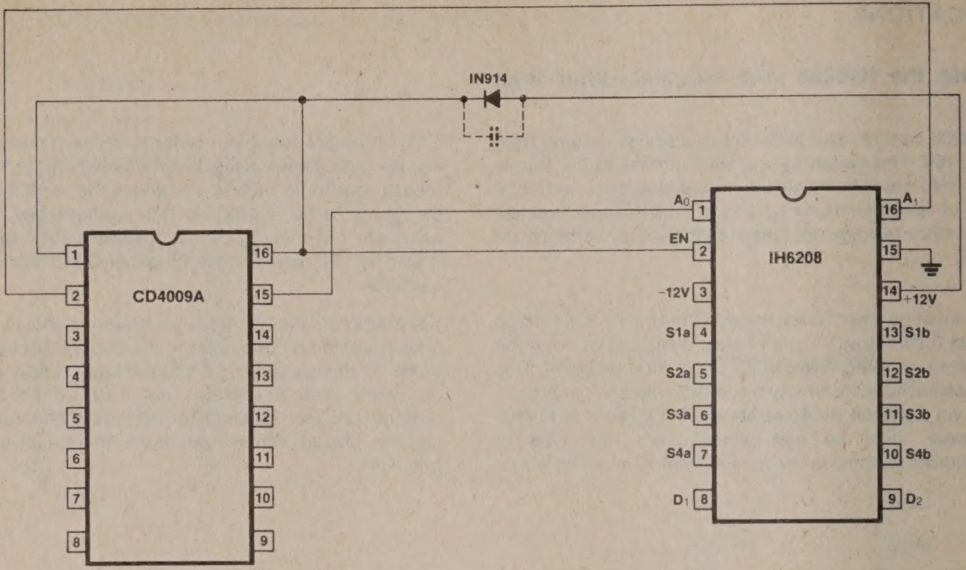

IN914
CD4009A
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
IH6208
A0
EN
-12V
S1a
S2a
S3a
S4a
D1
A1
+12V
S1b
S2b
S3b
S4b
D2

Figure 7. IH6208 Connection Diagram with Enable Input Strobing for less than ±15V Supply Operation.

III. Peak-to-Peak Signal Handling Capability

The IH6208 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6208 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

INTERSIL

IH6216
8-Channel Differential CMOS Analog Multiplexer

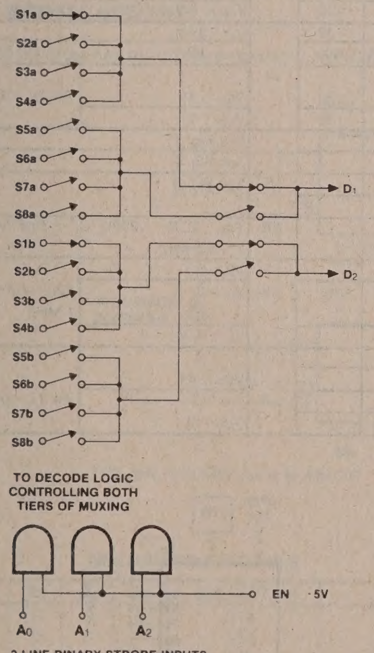
FEATURES

- **Pin compatible with HI507, DG507 & AD7507**
- **±11V analog signal range**
- **$r_{DS(on)} < 700$ ohms over full signal and temperature range**
- **Break before make switching**
- **TTL and CMOS compatible strobe control**
- **Binary strobe control (3 strobe inputs controls 2 out of 16 channels).**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than 100μA**
- **No SCR latch up**
- **Very low leakage $I_{D(off)} \leq 100pA$**

GENERAL DESCRIPTION

The IH6216 is a CMOS monolithic 2 of 16 multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs; additionally a fourth input is provided to use as a system enable. When the enable input is high (5V) the channels are sequenced by the 3 line binary inputs, and when low (0V) all channels are off. The 3 strobe inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the enable input (EN) must be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM


S1a
S2a
S3a
S4a
S5a
S6a
S7a
S8a
S1b
S2b
S3b
S4b
S5b
S6b
S7b
S8b
D1
D2
TO DECODE LOGIC CONTROLLING BOTH TIERS OF MUXING
EN
5V
A0
A1
A2

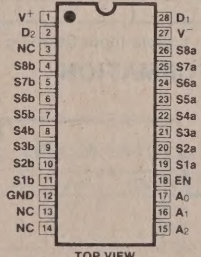
3 LINE BINARY STROBE INPUTS
(0 0 0) AND EN = 5V
ABOVE EXAMPLE SHOWS CHANNELS 1a & 1b ON.

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "1" = $V_{AH} > 3V$ $V_{ENH} > 4.5V$
LOGIC "0" = $V_{AL} < 0.8V$

PIN CONFIGURATION (Outline drawings DI, PI)


V+ 1
D2 2
NC 3
S8b 4
S7b 5
S6b 6
S5b 7
S4b 8
S3b 9
S2b 10
S1b 11
GND 12
NC 13
NC 14
28 D1
27 V−
26 S8a
25 S7a
24 S6a
23 S5a
22 S4a
21 S3a
20 S2a
19 S1a
18 EN
17 A0
16 A1
15 A2

TOP VIEW
V_1 COMMON TO SUBSTRATE

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6216MDI	−55°C to +125°C	28 pin Ceramic DIP
IH6216CDI	0°C to 70°C	28 pin Ceramic DIP
IH6216CPI	0°C to 70°C	28 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground .... −15V, V_1
V_S or V_D to V^+.................................. 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground .... −16V
Current (Any Terminal) .... 30 mA
Current (Analog Drain) .... 20 mA
Current (Analog Source) .... 20 mA
Operating Temperature .... −55 to 125°C
Storage Temperature .... −65 to 150°C
Power Dissipation (Package)* 1200mW
Lead Temperature (Soldering 10 sec) .... 300°C

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C

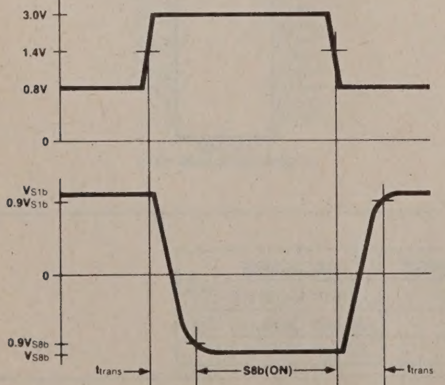
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

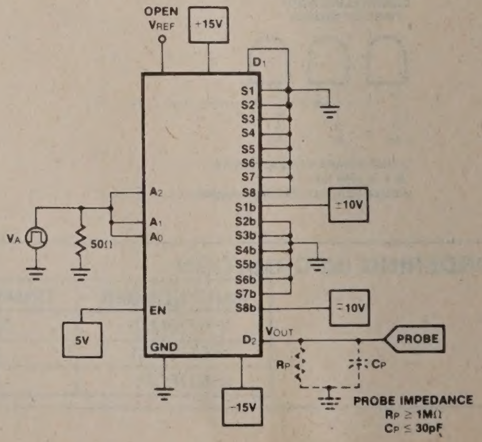
ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V^1$, Ground = 0V, unless otherwise specified.

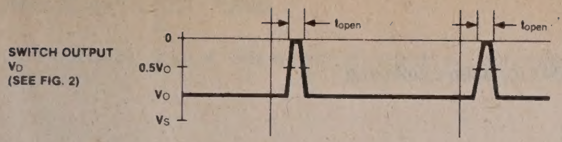
	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS						UNIT	TEST CONDITIONS	
					M SUFFIX			C SUFFIX					
					−55°C	25°C	125°C	0°C	25°C	70°C			
SWITCH	$r_{DS(ON)}$	S to D	16	480	600	600	700	650	650	750	Ω	$V_D = 10V$, $I_S = -10mA$	Sequence each switch on $V_{AL} = 0.8V$, $V_{AH} = 3V$
			16	300	600	600	700	650	650	750		$V_D = -10V$, $I_S = 10mA$	
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg}}$ $V_S = \pm 10V$	
	$I_{S(OFF)}$	S	16	0.01		0.1	50		0.2	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
			16	0.01		0.1	50		0.2	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(OFF)}$	D	2	0.1		0.2	100		0.4	100		$V_D = 10V$, $V_S = -10V$	
			2	0.1		0.2	100		0.4	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(ON)}$	D	16	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on $V_{AL} = 0.8V$, $V_{AH} = 3V$
			16	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	
INPUT	$I_{A(on)}$ or $I_{A(off)}$		3	.01		−10	−30		−10	−30	μA	$V_A = 3.0V$	
			3	.01		10	30		10	30		$V_A = 15V$	
	I_A	A_0 A_1 A_2 A_3	3			−10	−30		−10	−30		$V_{EN} = 5V$	All $V_A = 0$
		EN	1			−10	−30		−10	−30		$V_{EN} = 0$	
DYNAMIC	t_{trans}	D		0.6		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(En)}$	D		0.8		1.5						See Fig. 3	
	$t_{off(En)}$	D		0.3		1							
	"OFF" Isolation	D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3$ pF, $V_S = 3$ VRMS, f = 500 kHz	
	C_s	S		5							pF	$V_S = 0$	$V_{EN} = 0$, f = 140 kHz to 1 MHz
	$C_{d(off)}$	D		20								$V_D = 0$	
	C_{ds}	D to S		1								$V_S = 0$, $V_D = 0$	
SUPPLY	Supply Current +	I^+	1	55		200			1000		μA	$V_{EN} = 5V$	All V_A = 0 OR 3V
	Supply Current −	I^-	1	2		100			1000				
	Standby Current +	I^+_{SB}	1	1		100			1000			$V_{EN} = 0$	
	Standby Current −	I^-_{SB}	1	1		100			1000				

NOTE 1: See Section V. Enable Input Strobing Levels.

SWITCHING INFORMATION







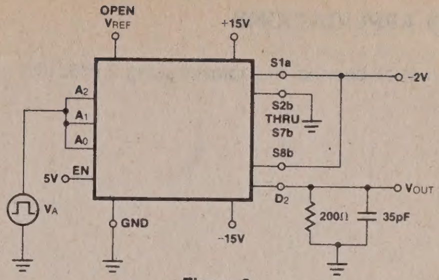
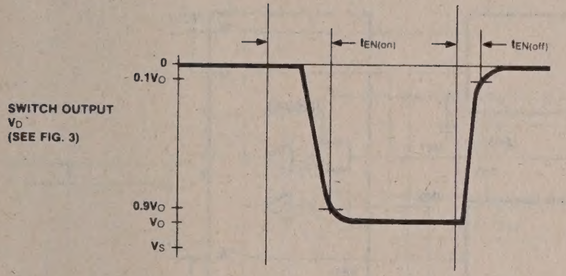

OPEN
V_{REF}
+15V
S1a
-2V
A_2
A_1
A_0
S2b
THRU
S7b
S8b
5V
EN
V_A
D2
V_{OUT}
GND
-15V
200Ω
35pF

Figure 2



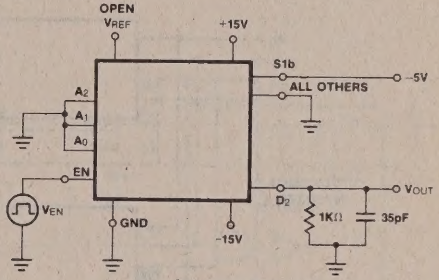
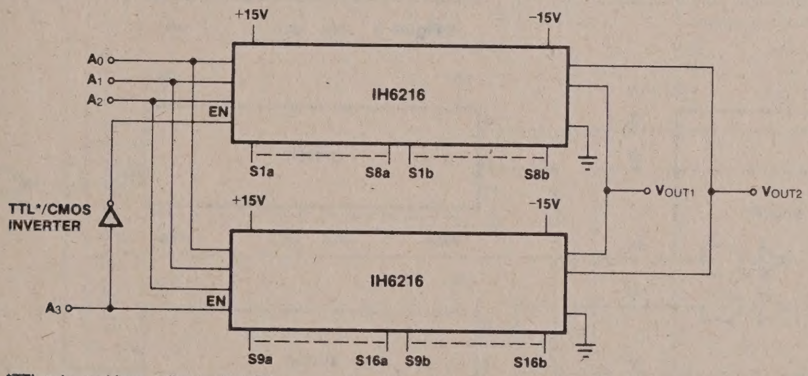

OPEN
V_{REF}
+15V
S1b
-5V
ALL OTHERS
A_2
A_1
A_0
EN
V_{EN}
D2
V_{OUT}
GND
-15V
1KΩ
35pF

Figure 3

IH6216 APPLICATIONS

I. 2 out of 32 channel multiplexer using 2 IH6216s.


+15V
-15V
A_0
A_1
A_2
IH6216
EN
S1a
S8a
S1b
S8b
V_{OUT1}
V_{OUT2}
TTL*/CMOS
INVERTER
+15V
-15V
IH6216
EN
A_3
S9a
S16a
S9b
S16b

*TTL gate must have pullup to drive EN

Figure 4

DECODE TRUTH TABLE

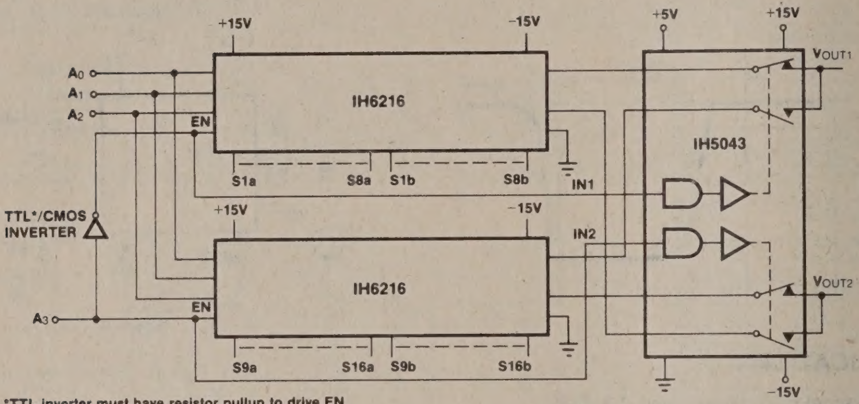
A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1a	V_{OUT1}
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1b	V_{OUT2}
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

IH6216 APPLICATIONS

II. 2 out of 32 channel multiplexer using 2 IH6216s; with an IH5043 for submultiplexing.


+15V
−15V
+5V
+15V
VOUT1
A0
A1
A2
EN
IH6216
IH5043
S1a
S8a
S1b
S8b
IN1
TTL*/CMOS INVERTER
+15V
−15V
IN2
VOUT2
IH6216
A3
EN
S9a
S16a
S9b
S16b
−15V

*TTL inverter must have resistor pullup to drive EN

Figure 5

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1a	VOUT1
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1b	VOUT2
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

IH6216 APPLICATIONS

III. 2 out of 64, using 4 IH6216s and 2 IH5043s as submultiplexers.

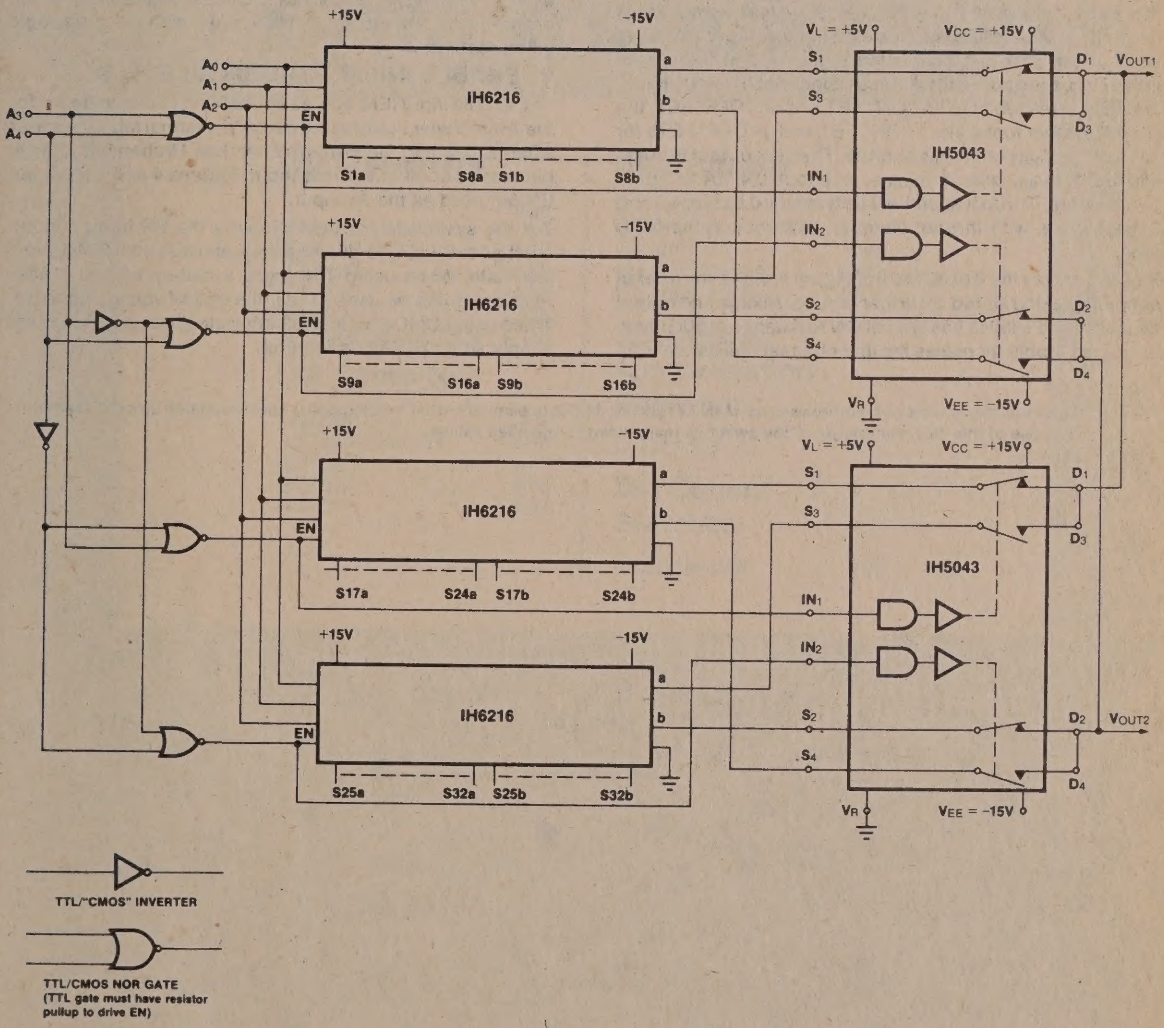

+15V
−15V
A0
A1
A2
A3
A4
EN
IH6216
a
b
S1a
S8a
S1b
S8b
S9a
S16a
S9b
S16b
S17a
S24a
S17b
S24b
S25a
S32a
S25b
S32b
VL = +5V
VCC = +15V
S1
S2
S3
S4
IN1
IN2
D1
D2
D3
D4
IH5043
VR
VEE = −15V
VOUT1
VOUT2
TTL/"CMOS" INVERTER
TTL/CMOS NOR GATE
(TTL gate must have resistor pullup to drive EN)

Figure 6

IV. GENERAL NOTE ON EXPANDABILITY OF IH6216

The IH6216 is a two tier multiplexer where 8 pairs of input channels are routed to a pair of outputs in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied in pairs. Thus 20 switches are needed to handle the 16 channels of information. The advantages of this are lower output capacity and leakage than would be possible using a system with all 8 channels tied to one common output. Also the expandability into 2 out of 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the IH6216 is expanded.

Figure 4 shows a 2 of 32 multiplexer using 2 IH6216s. Since the 6216 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. Corresponding output points of each of the 6216 are connected together, and the enable input strobe is used as the A_3 input. Since each output (pins 2 and 28) corresponds to an "ON" FET and an "OFF" FET, the overall system looks like 1 "ON" FET and 3 "OFF" FETs for each of the V_{out1} and V_{out2} outputs. Thus the output leakage will be 1 $I_{D(on)}$ plus 3 $I_{D(off)}$s or about 0.4 nA at room temperature. Thruput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}, with thruput channel resistance in the 500Ω area.

Figure 5 shows the 2 of 32 MUX of Figure 4, with a third tier of submultiplexing added to further reduce leakage and output capacity. The IH5043 has typical ON resistance of 50Ω (max. is 75Ω) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2 nA.

Figure 6 shows a 2 of 64 MUX using 3 tier MUXing (similar to Figure 5). The Intersil IH5043 is used for the third tier of MUXing. Each V_{out} point will see 3 OFF channels and 1 ON channel at any time, so that the typical leakages will be about 0.4 nA. Thruput channel resistance will be in the 550Ω area and thruput switching speeds will be about 1.3μs for ON time and 0.8μs for OFF time.

The IH5043 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6216 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are typically 1-2μA so that no excessive system power is generated. Note that the logic of the 5043 is such that it can be tied directly to the enable input (as shown in the figures) with no extra logic being required.

V. ENABLE INPUT STROBING LEVELS

The enable input (EN) acts as an enabling or disabling pin for the IH6216 when used as a 2 out of 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 4 and 5 show the EN pin used as the A_3 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up of 1kΩ or less resistor should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes up to the power supply so no pull-up is required.

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.

Data Acquisition

A/D Converters

	Page
LD110/111/114	4-4
ICL7109	4-26
ICL7126	4-50
ICL7135	4-58
ICL8052/3	4-135
ICL8068/8052A/7104	4-118

D/A Converters

ADC0801-4	4-9
AD7520/21/30/31	4-68
AD7523	4-74
AD7533	4-78
AD7541	4-82

DVM Circuits

ICL7106/7	4-17
ICL7116/17	4-42
ICL8052/7101	4-96
ICL8052/71C03	4-104
ICL8068/71C03	4-104

Successive Approximation Registers

AM25(L)02/3/4	4-11

D/A Current Switches

ICL8018/19/20	4-88

Integrating Analog-to-Digital Converters for Display

Maximum Electrical Specification at 25°C unless otherwise noted.

	Single Chip				Two Chip System*		
Model	**New ICL7126**	**New ICL7135**	**ICL7106/ICL7116**	**ICL7107/ICL7117**	**ICL8052/ ICL8053**	**ICL8068A/ 71C03A**	**ICL8052A/ 71C03A**
Resolution	±3½ digit	±4½ digit	±3½ digit	±3½ digit	Depends on counter used	±4½ digit	±4½ digit
Accuracy							
Nonlinearity	±1 count	±1 count	±1 count	±1 count	±0.002%	±1 count	±1 count
Zero Input Reading	±0.000	±0.000	±0.000	±0.000	±0.000	±0.0000	±0.0000
Ratiometric Reading	±1.000	±1.000	±1.000	±1.000	±1.000	±1.0000	±1.0000
$V_{IN}=V_{REF}$	±1 count	±1 count	±1 count	±1 count	±1 count	±1 count	±1 count
Rollover Error	±1 count	±1 count	±1 count	±1 count	±1 count	±1 count	±1 count
Stability							
Offset vs Temperature	1μV/°C	1μV/°C	1μV/°C	1μV/°C	5μV/°C	2μV/°C	2μV/°C
Gain vs Temperature	5 ppm/°C	5 ppm/°C	5 ppm/°C	5 ppm/°C	15 ppm/°C	5 ppm/°C	5 ppm/°C
Conversion Time	0.1 to 3 conv/sec	0.1 to 15 conv/sec	0.1 to 15 conv/sec	0.1 to 15 conv/sec	0.1 to 30 conv/sec	0.1 to 30 conv/sec	0.1 to 30 conv/sec
Analog Input							
Voltage Range	±200 mV to ±2V	±2V	±200 mV to ±2V	±200 mV to ±2V	±2V	±200 mV to ±2V	±2V
Impedance	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{9}\Omega$	$10^{9}\Omega$	$10^{9}\Omega$
Leakage Current	2pA	3pA	2pA	3pA	30pA	200pA	10pA
Noise (peak-to-peak)	15μV typ	15μV typ	15μV typ	15μV typ	20μV typ	2μV typ	20μV typ
Digital Input			Display Hold (7116)	Display Hold (7117)			
Digital Outputs							
Format	Direct 7 segment LCD display	Multiplex BCD	Direct 7 segment LCD display	Direct 7 segment LED display Comm Anode	Depends on counter used	Multiplex BCD	Multiplex BCD
Logic Level	AC: 4.5V down from V+	TTL/CMOS	AC: 4.5V down from V +	DTL/TTL/CMOS	Depends on counter used	TTL/CMOS	TTL/CMOS
Power Supply							
Voltage	+9V	±5V	+9V	±5V	±15V; +5V	±15V; +5V	±15V; +5V
Current	100μA	1.8mA	1.8mA	1.8mA	12mA	20mA; 30mA	18mA; 3mA
Package	40 pin DIP	28 pin DIP	40 pin DIP	40 pin DIP	(2) 14 pin DIP	14 pin DIP 28 pin DIP	14 pin DIP 28 pin

*Also available LD110/111/114 and 8052/7101 (not recommended for new designs).

Integrating Analog-to-Digital Converters for Data Acquisition

Type	Single Chip		Two Chip System***			
Model	**ADC0801-4**	**ICL7109**	**ICL8052/8068** ICL7104-12**	**ICL8052A/8068 ICL7104-14**	**ICL8052A/8068 ICL7104-16**	**ICL8052A/8068 ICL71C03**
Resolution	8-bit	±12-Bit Binary	±12-Bit	±14-Bit	±16-Bit	±4½-(3½) Digit BCD
Accuracy	±¼/½/½/1LSB	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count
Microprocessor Compatible	Yes	Yes	Yes	Yes	Yes	Yes
Output	Programmable: 1. Latched parallel 3 state Binary 2. One 8-bit byte	Programmable: 1. Latched parallel 3 state Binary 2. Controlled 2-8 bit bytes	Programmable: 1. Latched parallel 3 state Binary 2. Controlled 2-8 Bit Byte for ICL7104-12/14 3-8 Bit Byte for ICL7104-16			Multiplexed BCD
Control Lines	Run/Hold, Busy, Byte Enables, Mode, Load, Send Enable, Out of Range					Run/Hold, Busy, Strobe, OR, UR
Conversion Time	100μs	10ms	2ms	8ms	33ms	3ms
UART Compatible	Yes	Yes	Yes	Yes	Yes	Yes
Noise (Typical)	—	15μV	3μV (8068)	2μV (8068)	2μV (8068)	2μV (8068)
Input Current	—	10pA	30pA (8052)	30pA (8052)	30pA (8052)	10pA (8052A)
Input Voltage Range	5V span	±400mV to ±4.1V	±50mV to ±10V	±100mV to ±10V	±200mV to ±10V	±200mV to ±2V

**ICL7109 recommended as more cost effective in most applications.

***ICL8052/8068 and ICL8053 can be combined as analog portion of dual-slope A/D converter under μp control. See ICL8052/8068 and ICL 7104-16 for performance characteristics.

Digital-to-Analog Converters*

Maximum Electrical Specification at 25°C unless otherwise noted.

Model	AD7523	AD7533	AD7520 (7530)	AD7521 (7531)	AD7541
Resolution	8 bit	10 bit	10 bit	12 bit	12 bit
Accuracy	J/K/L	J/K/L	J/K/L	J/K/L	J/K/L
Linearity	0.2%/0.1%/0.05%	0.2%/0.1%/0.05%	0.2%/0.1%/0.05%	0.2%/0.1%/0.05%	0.2%/0.01%/0.01%
Zero Offset	50 µA	200 nA	200 nA (300 nA)	200 nA (300 nA)	50 nA
Full Scale Reading	1.5% max	1.4%	0.3% typ	0.3% typ	0.3%
Stability					
Gain vs. Temp	10 ppm/°C	10 ppm/°C	10 ppm/°C	10 ppm/°C	10 ppm/°C
Linearity vs. Temp	2 ppm/°C	2 ppm/°C	2 ppm/°C	2 ppm/°C	2 ppm/°C
Setting Time to ±0.05% F.S.	150ns	600 ns typ	500 ns typ	500 ns typ	1 µs
Input Code Logic Compatibility option	DTL/TTL/CMOS Binary Offset Binary	DTL/TTL/CMOS Binary Offset Binary	DTL/TTL/CMOS Binary Offset Binary	DTL/TTL/CMOS Binary Offset Binary	DTL/TTL/CMOS Binary Offset Binary
Power Supply					
Voltage	+ 5 to + 16V	+ 5 to + 15V	+ 5 to + 15V	+ 5 to + 15V	+ 5 to + 16V
Current	100 µA	2mA	2mA	2mA	2mA
Package	16 pin DIP	16 pin DIP	16 pin DIP	18 pin DIP	18 pin DIP

*R2R Ladder Multiplying Type

Successive Approximation Registers AM25(L)02/25(L)03/25(L)04

8 (2502/2503) and 12 bit (2504) successive approximation registers can be used as serial to parallel counter or ring counter. Contains storage and control for SAR A to D converters.

Quad Current Switches ICL8018/8019/8020

High speed precision current switches for use in current summing D/A converters. Can be purchased individually or in matched sets with accuracies of 0.01% (ICL8018), 0.1% (ICL8019), or 1.0% (ICL8020)

Sample and Hold

Type	V_{analog} (V_{p-p})	t_{acq}** (µs)	V_{inject}** (mV)	V_{os} (mV)	Drift Rate (mV/sec)
IH5110	±7.5	6	5	40	5
IH5111	±10	6	5	40	5
IH5112	±7.5	6	5	10	5
IH5113	±10	6	5	10	5
IH5114	±7.5	6	5	5	5
IH5115	±10	6	5	5	5

**C_{STO} = 0.01 µF

Monolithic Voltage Converter—The ICL7660

Converts positive voltage into negative over a range of + 1.5V through + 10V. May be cascaded for higher negative output voltages, paralleled for greater output current, used as a positive voltage multiplier, or any combination of the above. Typical supply current is 170 µA, and output source resistance is 55Ω at T_A = 25°C and I_O = 20 mA.

LD110/LD111
3½-Digit A/D Converter Set
LD114 Multiple-Option Digital Processor

FEATURES

- Accuracy 0.05% Of Reading ±1 Count
- Two Voltage Ranges — 1.999 V and 199.9 mV
- Sampling Rates up to 12 Samples/Second
- FET Input for $Z_{in} > 1000\ M\Omega$
- Auto-Zero Minimizes Effects of Offset, Drift and Temperature
- Auto-Polarity
- Multiplexed Parallel BCD or Serial BCD Output (LD114)
- Active High or Active Low Logic Outputs (LD114)
- Overrange and Underrange Signals Available for Auto-Ranging Capability.
- ÷512 Output Available for Phase Locked Loop Clock (LD114)
- TTL Compatible Outputs

GENERAL DESCRIPTION

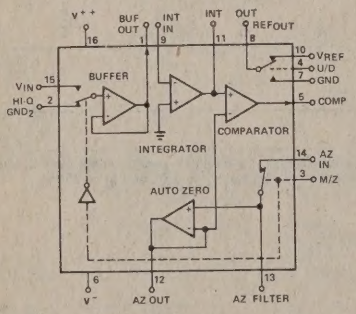
The monolithic LD111 analog processor contains a bipolar comparator, a bipolar integrating amplifier, two MOS-FET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. A wide range of conversion rates (1/3 to 12 samples per second) as well as two voltage ranges can be accommodated using externally determined RC time constants. All amplifiers are internally compensated.

The PMOS LD110/LD114 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3½ digits of BCD data as well as overrange, underrange and polarity information.

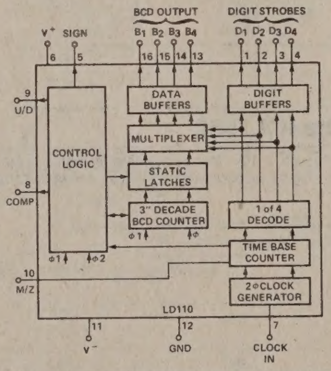
In the LD110, nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2, and 4.

In the LD114, ten push-pull output buffers (capable of driving one standard TTL load) provide the clock frequency ÷512, sign, digit strobe and multiplexed BCD data. Four data output format options allow the user to tailor the BCD output to his circuit requirements.

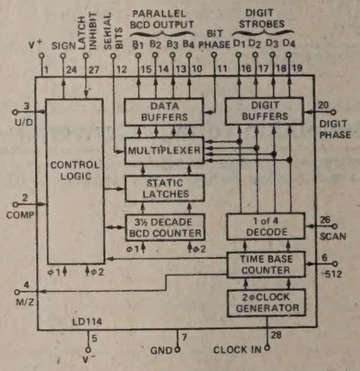
LD111
ANALOG PROCESSOR

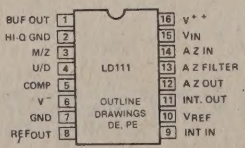

V++
BUF OUT
INT IN
INT OUT
REFOUT
16
1
9
11
8
10
VREF
4
U/D
7
GND
5
COMP
15
VIN
HI-Q GND2
2
BUFFER
INTEGRATOR
COMPARATOR
14
AZ IN
3
M/Z
AUTO ZERO
6
12
13
V−
AZ OUT
AZ FILTER

LD110
DIGITAL PROCESSOR


BCD OUTPUT
DIGIT STROBES
V+
SIGN
B1 B2 B3 B4
D1 D2 D3 D4
6
5
16
15
14
13
1
2
3
4
9
U/D
8
COMP
10
M/Z
CONTROL LOGIC
DATA BUFFERS
DIGIT BUFFERS
MULTIPLEXER
STATIC LATCHES
3½ DECADE BCD COUNTER
1 of 4 DECODE
TIME BASE COUNTER
2φCLOCK GENERATOR
φ1
φ2
LD110
11
12
7
V−
GND
CLOCK IN

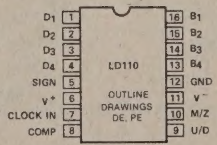
LD114
DIGITAL PROCESSOR


LATCH INHIBIT
SERIAL BITS
PARALLEL BCD OUTPUT
BIT PHASE
DIGIT STROBES
V+
SIGN
B1 B2 B3 B4
D1 D2 D3 D4
1
24
27
12
15
14
13
10
11
16
17
18
19
3
U/D
2
COMP
4
M/Z
CONTROL LOGIC
DATA BUFFERS
DIGIT BUFFERS
MULTIPLEXER
STATIC LATCHES
3½ DECADE BCD COUNTER
1 of 4 DECODE
TIME BASE COUNTER
2φCLOCK GENERATOR
φ1
φ2
20
DIGIT PHASE
26
SCAN
6
÷512
LD114
5
V−
7
GND
28
CLOCK IN


BUF OUT 1
HI-Q GND 2
M/Z 3
U/D 4
COMP 5
V− 6
GND 7
REFOUT 8
16 V++
15 VIN
14 A Z IN
13 A Z FILTER
12 A Z OUT
11 INT. OUT
10 VREF
9 INT IN
LD111
OUTLINE DRAWINGS DE, PE

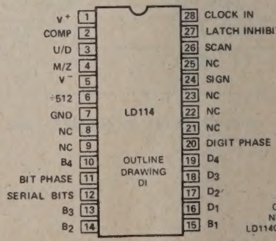
ORDER NUMBER
LD111CJ-PLASTIC
LD111CP-CERAMIC

TOP VIEW


D1 1
D2 2
D3 3
D4 4
SIGN 5
V+ 6
CLOCK IN 7
COMP 8
16 B1
15 B2
14 B3
13 B4
12 GND
11 V−
10 M/Z
9 U/D
LD110
OUTLINE DRAWINGS DE, PE

ORDER NUMBER
LD110CJ-PLASTIC
LD111CP-CERAMIC

TOP VIEW


V+ 1
COMP 2
U/D 3
M/Z 4
V− 5
÷512 6
GND 7
NC 8
NC 9
B4 10
BIT PHASE 11
SERIAL BITS 12
B3 13
B2 14
28 CLOCK IN
27 LATCH INHIBIT
26 SCAN
25 NC
24 SIGN
23 NC
22 NC
21 NC
20 DIGIT PHASE
19 D4
18 D3
17 D2
16 D1
15 B1
LD114
OUTLINE DRAWING DI

ORDER NUMBER
LD114CR-CERAMIC

TOP VIEW

ABSOLUTE MAXIMUM RATINGS

V_{IN} . . . . ±5.0V
$V^{++} - V^-$ (LD111) 30V
V^+ 6V
$V^+ - V^-$ (LD110/LD114) 20V
Voltage on any pin relative to V^+ (LD114) . . 0.3V to −20V
V_{REF} . . . . V^{++}

Operating Temperature . . . . 0 to 70°C
Storage Temperature . . . . −65°C to 150°C
Power Dissipation (Package, LD110/LD111)* 750mW
Power Dissipation (Package, LD114)* 1200mW

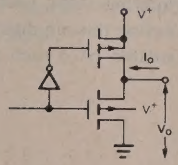
*Device mounted with all leads welded or soldered to PC Board, Derate 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS $V^{++} = 12V$, $V^+ = 5V$, $V^- = 5V$, $V_{REF} = 8.2V$, $T_A = 25°C$.

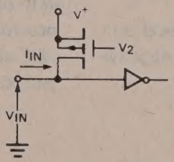
	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	Clock Frequency	f_{IN}	50% Duty Cycle		30.7		kHz
	Input Bias Current	I_{IN}	$T_A = 25°$ C		4		pA
			$T_A = 70°$ C		40		
	Normal Mode Rejection	NMR	$f_L = 60$ Hz		40		dB
	Clock Input Current, Low	I_{CL}	V_{CLOCK} in = 0.4 V			-500	μA
	Comparator	I_{INL}	$V_{INL} = -12$ V			-100	
	Latch Inhibit	I_{INL}	$V_{INL} = -12$ V		180	-600	
	Format Option Inputs	I_{INH}	$V_{INH} = V_{SS}$		25	400	
OUTPUT	Measure/Zero Voltage, Low	V_{OL1}	$I_{OL} = 150$ μA			0.4	V
	Measure/Zero Voltage, High	V_{OH1}	$I_{OH} = -200$ μA	2.4			
	Up/Down Logic Voltage, Low	V_{OL2}	$I_{OL} = 250$ μA			0.4	
	Up/Down Logic Voltage, High	V_{OH2}	$I_{OH} = -200$ μA	2.4			
	Digits, Bits, Sign Voltage, ÷512*	V_{OL3}	$I_{OL} = 1.6$ mA			0.4	
	Analog Comparator Voltage	V_{OH3}	$I_{OH} = -100$ μA	2.4			
	Data Bit Voltage, High	V_{OH4}	$I_{OH} = -200$ μA	2.4			
	Digits, Sign Voltage, ÷512*	V_{OH5}	$I_{OH} = -800$ μA	2.4			
SWITCH	ON Resistance, Auto Zero Switch	$r_{DS(on)}$	$V_{AZ(in)} = -4.0$ V, $I_S = -50$ μA		11	50	kΩ
	ON Resistance, Up/Down Switch	$r_{DS(on)}$	$I_S = 1$ mA		650	3000	Ω
	Up/Down Switch Temperature Coefficient	TC			0.20	0.50	%/°C
SUPPLY	Supply Current, LD111	I^{++}			2.2	3.5	mA
	Supply Current, LD111	I_A^-			-1.8	-3.0	
	Supply Current, LD110/114	I_D^-			-17	-23	
	Supply Current, LD110/114	I^+			17.4	24	
	Power Supply Rejection Ratio, V^{++}	$PSRR_1$		80	85		dB
	Power Supply Rejection Ratio, V^-	$PSRR_2$		60	65		
	Reference Current Rejection Ratio		$R_{REF} = R_2 = 100K\Omega$, $V_{IN} = 2V$	35	41		nA/LSB

*÷512 output applicable to LD114 only

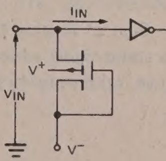
INPUT/OUTPUT SCHEMATICS



OUTPUT BUFFERS
(Digits, Bits, Sign, 512, M/Z, U/D)



COMPARATOR, CLOCK, LATCH INHIBIT INPUTS



FORMAT OPTION INPUTS
(Bit Phase, Digit Phase, Scan, Serial Bits)

DESCRIPTION OF PIN FUNCTIONS (LD110/LD114)

V^+ – Positive Supply Voltage. Recommended level is +5 volts ± 10%.

V^- – Negative Supply Voltage. Recommended level is –12 volts ±10%.

CLOCK IN – This input accepts a TTL or MOS level clock to drive the synchronous digital circuitry. Acceptable duty cycles on the external clock range from 30% high, 70% low to 70% high, 30% low for clock frequencies from 2 kHz to 75 kHz. Although any clock frequency between 2 kHz and 75 kHz may be used, clock frequencies that are integer divisions of $2048F_L$ ($F_{IN} = 2084F_L/n$, n = 2, 3, 4, 51, F_L = Line Frequency) provide measure and zero periods that are integer multiples of the line frequency period ($T_{zero} = n/F_L$, $T_{measure} = 2n/F_L$). Line frequency interference is minimized by the selection of one of these 50 frequencies.

This input has an active pull-up to V^+.

M/Z – Measure/Zero Logic Output. This 0 to 5 volt logic output successively provides Autozero and Measurement intervals of 2048 and 4096 clock periods respectively. This output is compatible with CMOS logic and directly interfaces with the LD111 analog processor.

÷512 (LD114) – This TTL compatible output (1 standard load) provides the necessary clock frequency division for a phase locked loop digital clock. The line frequency rejection will be held at the maximum level (>80 dB) when locked to the line frequency.

U/D – Up/Down Logic Output. This output has logic levels of 0 to +5 volts to provide pulse-width modulation of the reference current when used with the LD111 analog processor. This output is CMOS compatible.

COMP – Analog Comparator Input. This input has an active pull-up to V^+ for a comparator "high" state. This pin must be pulled down to V^- for a "low" comparator state.

An End-of-Conversion Signal can be decoded from the three interconnecting logic lines (M/Z, U/D, Comp) using the following CMOS logic.

$\overline{M/Z + U/D + Comp}$ = E.O.C.

SIGN – Sign of Analog Input Polarity. This TTL level output is a static signal which is either 0 or V^+ for a negative or positive input polarity respectively.

BIT PHASE (*LD114) – The bit outputs will be active high (positive) logic if this pin is left open or connected to V^-. The application of V^+ to this pin will give a complemented output (negative logic).

DIGIT PHASE (*LD114) – The Digit Strobe outputs will be of positive logic if this pin is left open or connected to V^- (an active pull-down is internally connected to V^-). Applying V^+ to this pin will complement the outputs to give negative logic. Negative logic may simplify interfacing with Common Anode LED, Gas Discharge and Liquid Crystal Displays.

B_1, B_2, B_3, B_4 – BCD Data Bit Output. B_4 represents the most significant bit and B_1 the least significant bit of the BCD output. Bit 4 of digit 4 goes high for an underrange condition (less than 100 counts). These outputs are compatible with 1 standard TTL load.

MUX Underrange = $B_4 \cdot D_4$ (5% of full scale)

D_1, D_2, D_3, D_4 – Digit Strobe Outputs. D_4 is the most significant and D_1 the least significant digit of the 3½ digit output. The digit strobes are each selected in turn when the BCD data bits for that digit appear at the bit outputs.

MUX Overrange = $\overline{D_1 + D_2 + D_3 + D_4}$ (100% of full scale, count ⩾2000).

SCAN (*LD114) – Sequential/Interlace Digit Scan. The digit strobe format will be an interlaced format of digits 1, 3, 2 and 4 if this pin is left open or is connected to V^-. This format is useful for display digits packaged two to an envelope and which require an interdigit blanking period eg. (Beckman Displays). By alternating from envelope, an interdigit blanking period is effectively provided.

The application of V^+ to this pin will give a sequencial scan of digits 1, 2, 3 and 4. This format may be more useful in interfacing with data acquisition equipment.

LATCH INHIBIT (*LD114) – Connecting this pin to V_2 will prevent updating of the internal static latches, thus providing a "hold" function. Leaving this pin disconnected will allow the latches to be updated once each sampling period.

DESCRIPTION OF PIN FUNCTIONS (LD110/LD114) Cont.

SERIAL BITS (*LD114)—Parallel/Serial Bit Output Format. The BCD data bits for each digit will appear simultaneously with the digit strobe if the parallel bit option is selected.

This format is useful for driving multiplexed displays. The parallel bit format is available when this pin is left open or connected to V^-.

The application of V^+ to this pin will put all of the BCD data bits in a serial order at the bit 4 output.

Bit outputs 1, 2, and 3 contain time markers to identify the data. The most significant bit of the last digit (D_4) is identified by a marker at the bit 2 output. The least significant bit of the first Digit (D_1) is identified by a marker at bit 3. Bit 1 shows a marker for the least significant bit of each digit.

All output format options are independent of one another (i.e., the serial bit output can have either sequential or interlace scan, Positive or Negative logic).

(*For LD110, action is described for "pin left open".)

DESCRIPTION OF PIN FUNCTIONS – LD111

BUF OUT – The output of this unity gain input buffer amplifier is applied to the integrator summing node through a scaling resistor R_2. The value of this resistor is typically 10 KΩ for a 200.0 mV full-scale and 100 KΩ for a 2.000 V full-scale. The digital output is inversely proportional to the value of this resistor,

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \; \frac{R_1}{R_2} \; 8192$$

HI-QUALITY GND – This pin, typically connected to a High Quality Ground point for single ended inputs **CAN BE USED AS THE INVERTING INPUT FOR DIFFERENTIAL SIGNALS.** The digital output will be $V_{IN} - V_{HI} - Q$. When using this differential mode, it is important that resistor R_3 equal Resistor R_2 for proper operation.

M/Z – Measure/Zero Logic Input. Internal level shifting drivers operate the PMOS switches in response to this digital signal.

U/D – Up/Down Logic Input. The logic signal applied to this pin operates a SPDT switch to provide Quantized pulses of charge to the integrator.

COMP – This analog comparator output is an open collector configuration which goes to V^- when "low."

V^- – Negative Supply Voltage. Recommended level is −12V ± 10%.

GND – Analog Processor Ground.

REF_{out} – This voltage output of the SPDT U/D switch, converted to a current by resistor R_1, supplies the reference current to the integrator.

INT. IN – Integrator Summing Node.

V_{REF} – A stable positive reference voltage (5 to 11 V) applied to this pin is the standard to which the input voltage V_{IN} is measured. Ratio measurements can be made by applying a variable to this input (1.0 to 11V).

INT. OUT – The output of the integrating amplifier is made available for application to the Auto-Zero amplifier by means of resistor R_4.

AZ OUT – The output of the unity gain Auto-Zero Amplifier provides a second negative reference current to the integrator through resistor R_3.

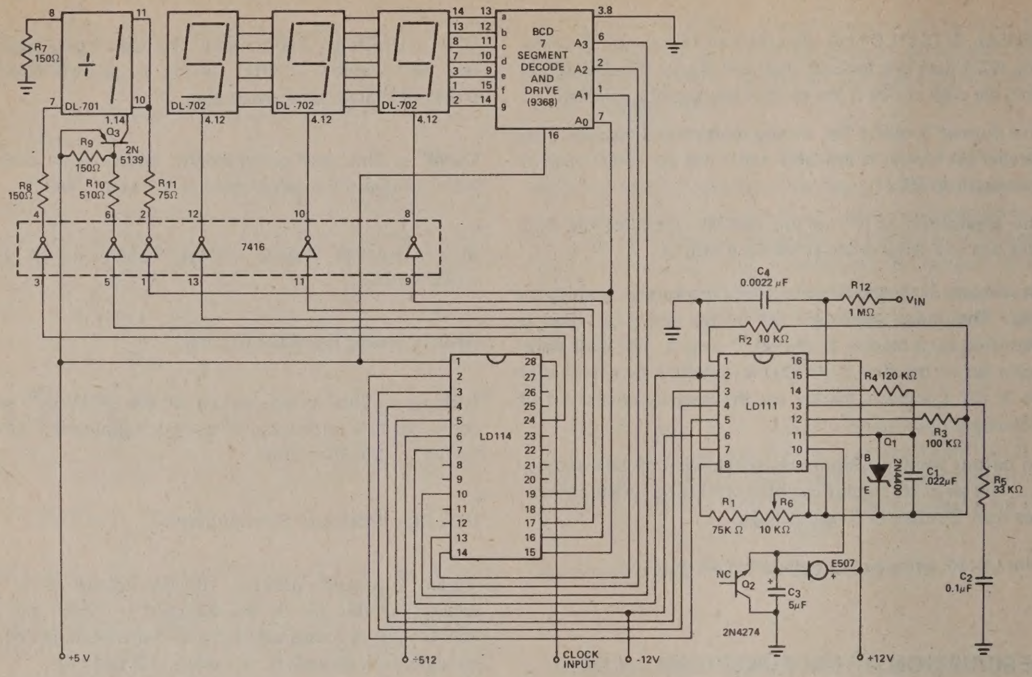
AZ FILTER – The RC filter (R_5 and C_{STRG}) connected to this pin stores. D.C. voltage components to balance amplifier offset and drift components.

AZ IN – This input is switched into the AZ filter during the Zeroing interval.

V_{IN} – Analog Voltage Input. The A/D System digitizes the voltage appearing at this input.

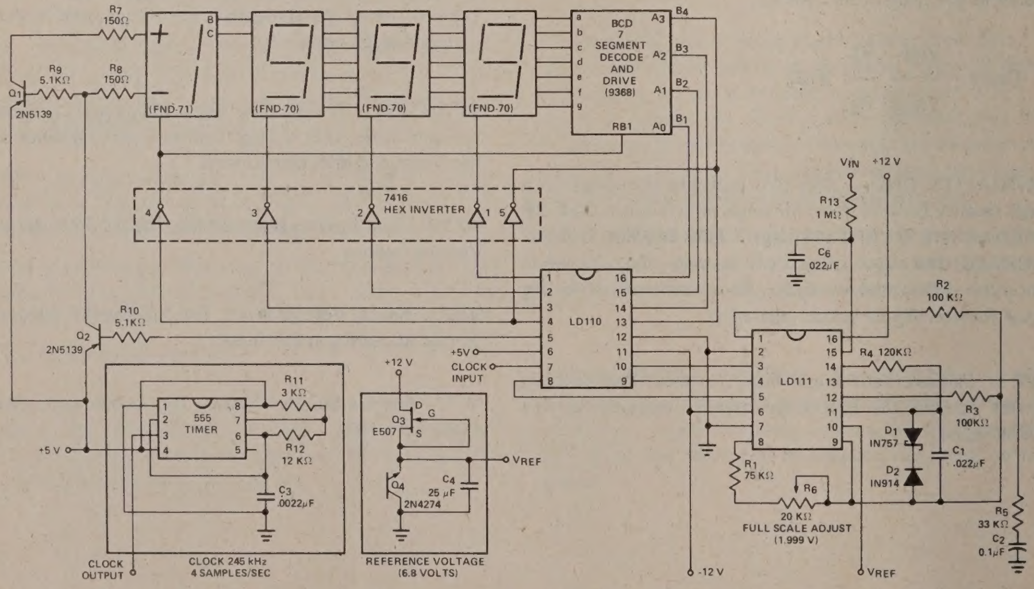
V^{++} – Positive Supply Voltage. The recommended level is +12 volts ± 10%.

APPLICATIONS LD111/LD114


R7 150Ω
DL-701
DL-702
DL-702
DL-702
BCD 7 SEGMENT DECODE AND DRIVE (9368)
A3
A2
A1
A0
3.8
Q3 2N 5139
R9 150Ω
R8 150Ω
R10 510Ω
R11 75Ω
1.14
4.12
7416
LD114
LD111
C4 0.0022 μF
R12 1 MΩ
VIN
R2 10 KΩ
R4 120 KΩ
R3 100 KΩ
Q1 2N4400
C1 .022μF
R5 33 KΩ
R1 75K Ω
R6 10 KΩ
E507
NC
Q2 2N4274
C3 5μF
C2 0.1μF
+5 V
÷512
CLOCK INPUT
-12V
+12V

3½ Digit DVM (±200.0 mV)

APPLICATIONS LD110/LD111


R7 150Ω
R9 5.1KΩ
R8 150Ω
Q1 2N5139
(FND-71)
(FND-70)
(FND-70)
(FND-70)
BCD 7 SEGMENT DECODE AND DRIVE (9368)
A3
A2
A1
A0
RB1
B4
B3
B2
B1
7416 HEX INVERTER
LD110
LD111
R10 5.1KΩ
Q2 2N5139
+5V
CLOCK INPUT
+12 V
555 TIMER
R11 3 KΩ
R12 12 KΩ
C3 .0022μF
+5 V
CLOCK OUTPUT
CLOCK 245 kHz 4 SAMPLES/SEC
Q3 E507
Q4 2N4274
C4 25 μF
VREF
REFERENCE VOLTAGE (6.8 VOLTS)
VIN
+12 V
R13 1 MΩ
C6 .022μF
R2 100 KΩ
R4 120KΩ
R3 100KΩ
D1 IN757
D2 IN914
C1 .022μF
R1 75 KΩ
R6 20 KΩ FULL SCALE ADJUST (1.999 V)
R5 33 KΩ
C2 0.1μF
-12 V
VREF

3½ Digit DVM (±2.000 Volts)

INTERSIL

ADC0801–ADC0804
8-Bit Microprocessor Compatible A/D Converters

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

- **MCS-48 and MCS-80/85 bus compatible–no interfacing logic required**
- **Conversion time < 100 μs**
- **Easy interface to all microprocessors**
- **Will operate "stand alone"**
- **Differential analog voltage inputs**
- **Bandgap voltage references**
- **TTL compatible inputs and outputs**
- **ON-chip clock generator**
- **0V to 5V analog voltage input range (single +5V supply)**
- **No zero adjust required**

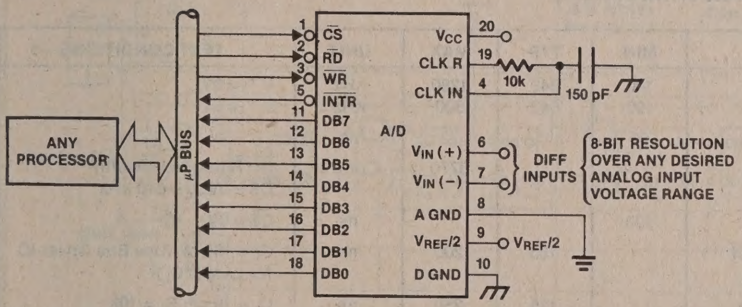
GENERAL DESCRIPTION

The ADC0801 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, hence no interfacing is required.

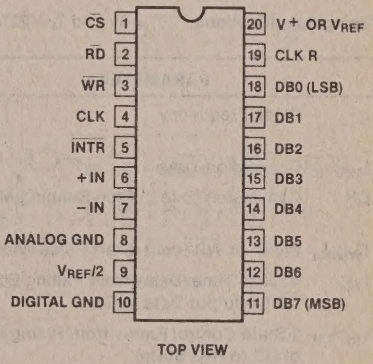
A differential analog voltage input allows increasing the common-mode-rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The ADC0801 family is available in the industry standard 20 pin CERDIP packages.

TYPICAL APPLICATION


ANY PROCESSOR
μP BUS
A/D
CS
RD
WR
INTR
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
1
2
3
5
11
12
13
14
15
16
17
18
VCC
CLK R
CLK IN
VIN (+)
VIN (−)
A GND
VREF/2
D GND
20
19
4
6
7
8
9
10
10k
150 pF
DIFF INPUTS
8-BIT RESOLUTION OVER ANY DESIRED ANALOG INPUT VOLTAGE RANGE
VREF/2

PIN CONFIGURATION


CS 1
RD 2
WR 3
CLK 4
INTR 5
+IN 6
−IN 7
ANALOG GND 8
VREF/2 9
DIGITAL GND 10
20 V+ OR VREF
19 CLK R
18 DB0 (LSB)
17 DB1
16 DB2
15 DB3
14 DB4
13 DB5
12 DB6
11 DB7 (MSB)
TOP VIEW

ORDERING INFORMATION

PART	ERROR	TEMPERATURE RANGE	PACKAGE	ORDER NUMBER
ADC0801	± 1/4 bit adjusted full scale	0°C to +70°C −40°C to +85°C −55°C to +125°C	20 pin CERDIP 20 pin CERDIP 20 pin CERDIP	ADC0801LCN ADC0801LCD ADC0801LD
ADC0802	± 1/2 bit no adjust	0°C to +70°C −40°C to +85°C −55°C to +125°C	20 pin CERDIP 20 pin CERDIP 20 pin CERDIP	ADC0802LCN ADC0802LCD ADC0802LD
ADC0803	± 1/2 bit adjusted full scale	0°C to +70°C −40°C to +85°C −55°C to +125°C	20 pin CERDIP 20 pin CERDIP 20 pin CERDIP	ADC0803LCN ADC0803LCD ADC0803LD
ADC0804	± 1 bit no adjust	0°C to +70°C −40°C to +85°C	20 pin CERDIP 20 pin CERDIP	ADC0804LCN ADC0804LCD

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.5V
Voltage at Any Input	−0.3V to (V^+ +0.3V)
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

OPERATING RATINGS

Temperature Range	
ADC0801/02/03LD	−55°C to +125°C
ADC0801/02/03/04LCD	−40°C to +85°C
ADC0801/02/03/04LCN	0°C to +70°C
Supply Voltage Range	4.5V to 6.5V

ELECTRICAL CHARACTERISTICS

Converter Specifications: $V^+ = 5V$, $V_{REF}/2 = 2.500V$, $T_{MIN} \le T_A \le T_{MAX}$ and $f_c = 640$ kHz unless otherwise stated.

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
ADC0801: Total Adjusted Error			±1/4	LSB	With Full Scale Adjust
ADC0802: Total Unadjusted Error			±1/2	LSB	Completely Unadjusted
ADC0803: Total Adjusted Error			±1/2	LSB	With Full Scale Adjust
ADC0804: Total Unadjusted Error			±1	LSB	Completely Unadjusted
$V_{REF}/2$ Input Resistance	1.0	1.3		kΩ	Input Resistance at Pin 9
Analog Input Voltage Range	GND − 0.05		V^+ + 0.05	V	
DC Common-Mode Rejection		±1/16	±1/8	LSB	Over Analog Input Voltage Range
Power Supply Sensitivity		±1/16	±1/8	LSB	$V^+ = 5V \pm 10\%$ Over Allowed Input Voltage Range

Timing Specifications: $V^+ = 5V$ and $T_A = 25°C$ unless otherwise stated.

PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS
f_c	Clock Frequency	100 100	640 640	1280 800	kHz kHz	$V^+ = 6V$, $V^+ = 5V$
t_{conv}	Conversion Time	66		73	ns	
CR	Conversion Rate In Free-Running Mode			8770	Conv/S	$\overline{\text{INTR}}$ tied to $\overline{\text{WR}}$ with $\overline{\text{CS}} = 0V$, $f_c = 640$ kHz
$t_{W(\overline{WR})L}$	Width of $\overline{\text{WR}}$ Input (Start Pulse Width)	100			ns	$\overline{\text{CS}} = 0V$
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{\text{RD}}$ to Output Data Valid)		135	200	ns	$C_L = 100$ pF (Use Bus Driver IC for Larger C_L)
t_{1H}, t_{0H}	3-State Control (Delay from Rising Edge of $\overline{\text{RD}}$ to Hi-Z State)		125	250	ns	$C_L = 10$ pF, $R_L = 10k$
t_{WI}	Delay from Falling Edge of $\overline{\text{WR}}$ to Reset of $\overline{\text{INTR}}$		300	450	ns	
C_{IN}	Input Capacitance of Logic Control Inputs		5	7.5	pF	
C_{OUT}	3-State Output Capacitance (Data Buffers)		5	7.5	pF	

AM2502/3/4
AM25L02/3/4
Successive Approximation Registers

FEATURES

- **Contains all the storage and control for successive approximation A to D converters.**
- **Provision for register extension or truncation.**
- **Can be operated in START-STOP or continuous conversion mode.**
- **100% reliability assurance testing in compliance with MIL-STD-883.**
- **Can be used as serial-to-parallel counter or ring counters.**
- **Electrically tested and optically inspected dice for the assemblers of hybrid products.**

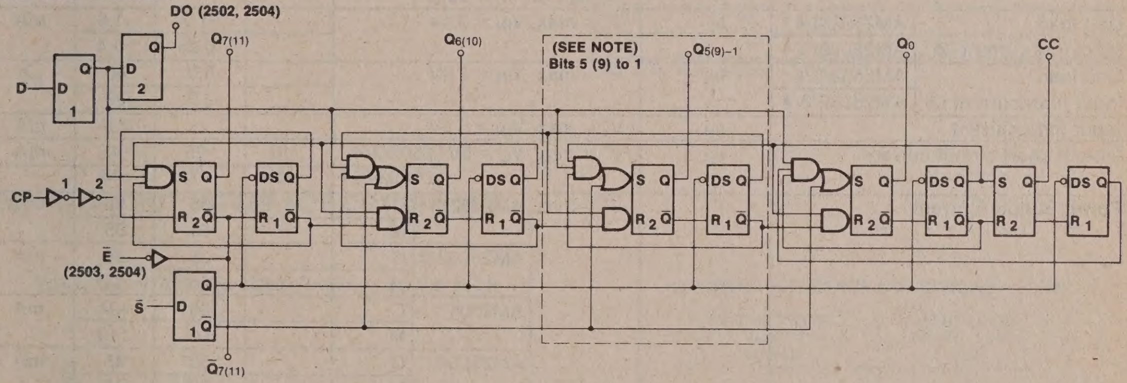
GENERAL DESCRIPTION

The AM2502/3/4 are 8-bit and 12-bit TTL Successive Approximation Registers. They contain all the digital control and storage necessary for successive approximation analog to digital conversion and can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches which act as the control elements and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW to HIGH transition. Externally the device acts as a special purchase serial to parallel converter which accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the 2502 and 2504 when the clock goes from LOW to HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time data enters the register bit the next less significant bit is set to a LOW, ready for the next iteration.

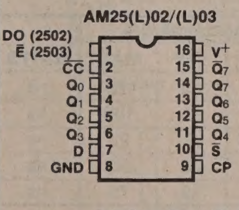
The AM25L02/L03/L04 are low power equivalents of the AM2502/03/04.

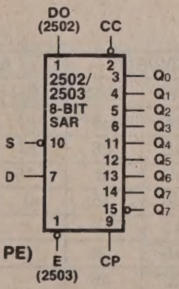
LOGIC DIAGRAM


DO (2502, 2504)
$Q_{7(11)}$
$Q_{6(10)}$
(SEE NOTE)
Bits 5 (9) to 1
$Q_{5(9)-1}$
Q_0
CC
D
Q
D
1
Q
D
2
CP
1
2
S Q
$R_2\bar{Q}$
DS Q
$R_1\bar{Q}$
S
R 2
R 1
Ē
(2503, 2504)
Q
S̄
D
$1\bar{Q}$
$\bar{Q}_{7(11)}$

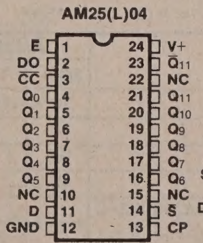
NOTES
1. CELL LOGIC IS REPEATED FOR REGISTER STAGES.
   Q_5 TO Q_1 2502/3
   Q_9 TO Q_1 2504
2. NUMBERS IN PARENTHESES ARE FOR 2504

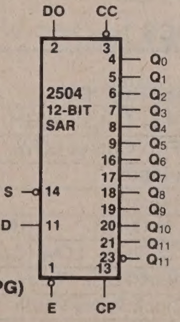
PIN CONFIGURATIONS AND LOGIC SYMBOLS


AM25(L)02/(L)03
DO (2502)
Ē (2503)
1
16
V+
C̄C̄
2
15
$\bar{Q}_7$
Q_0
3
14
Q_7
Q_1
4
13
Q_6
Q_2
5
12
Q_5
Q_3
6
11
Q_4
D
7
10
S̄
GND
8
9
CP

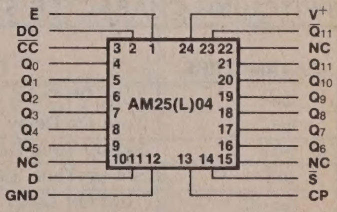

DO
(2502)
CC
1
2
3
2502/
2503
8-BIT
SAR
Q_0
4
Q_1
5
Q_2
6
Q_3
S
10
11
Q_4
12
Q_5
D
7
13
Q_6
14
Q_7
15
$\bar{Q}_7$
1
9
E
(2503)
CP

(outline dwg JE, PE)


AM25(L)04
E
1
24
V+
DO
2
23
$\bar{Q}_{11}$
C̄C̄
3
22
NC
Q_0
4
21
Q_{11}
Q_1
5
20
Q_{10}
Q_2
6
19
Q_9
Q_3
7
18
Q_8
Q_4
8
17
Q_7
Q_5
9
16
Q_6
NC
10
15
NC
D
11
14
S̄
GND
12
13
CP


DO
CC
2
3
4
Q_0
5
Q_1
2504
12-BIT
SAR
6
Q_2
7
Q_3
8
Q_4
9
Q_5
16
Q_6
S
14
17
Q_7
18
Q_8
19
Q_9
D
11
20
Q_{10}
21
Q_{11}
23
$\bar{Q}_{11}$
1
13
E
CP

(outline d' 'g JG, PG)


E
DO
C̄C̄
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
NC
D
GND
3 2 1
24 23 22
4
21
5
20
6
19
7
18
8
17
9
16
10 11 12
13 14 15
AM25(L)04
V+
$\bar{Q}_{11}$
NC
Q_{11}
Q_{10}
Q_9
Q_8
Q_7
Q_6
NC
S̄
CP

(outline dwg FG)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V^+
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA
Storage Temperature	−65°C to +150°C
Operating Temperatures	
M devices	−55°C to +125°C
C devices	0°C to +70°C
Lead Temperature (soldering, 10s)	300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS $V^+ = 5V$, T_A = Operating Temperature Range unless otherwise specified

PARAMETER		SYMBOL	TEST CONDITIONS			LIMITS			UNIT
						MIN.	TYP.(1)	MAX.	
Output high voltage		V_{OH}	V^+ = min, $I_{OH} = -0.48mA$ $V_{IN} = V_{IL}$ or V_{IH}			2.4	3.6		V
Output low voltage		V_{OL}	V^+ = min, $I_{OH} = 0.96mA$ $V_{IN} = V_{IL}$ or V_{IH}				0.2	0.4	V
Input high voltage		V_{IH}	Guaranteed input logic HIGH voltage for all inputs			2.0			V
Input low voltage		V_{IL}	Guaranteed input logic LOW voltage for all inputs					0.8	V
Unit load input low current (2)	AM2502/3/4	I_{IL}	V^+ = max, $V_{IN} = 0.4V$				−1.0	−1.6	mA
	AM25L02/3/4						−0.25	−0.4	
Unit load input high current (2)	AM2502/3/4	I_{IH}	V^+ = max, $V_{IN} = 2.4V$				6.0	40	μA
	AM25L02/3/4						2.0	20	
Input high current		I_{IH}	V^+ = max, $V_{IN} = 5.5V$					1.0	mA
Output short circuit current		I_{SC}	V^+ = max, $V_O = 0V$	2502/3/4		−10	−25	−45	mA
				25L02/3/4		−3	−7	−16	
Power Supply Current		I^+	V^+ = max	AM2502/3	C		65	95	mA
					M		65	85	
				AM25L02/3	C		25	35	mA
					M		25	33	
				AM2504	C		90	124	mA
					M		90	110	
				AM25L04	C		30	45	mA
					M		30	42	

NOTES: 1. Typical limits are with $V^+ = 5.0V$, $T_A = 25°C$ and maximum loading.
2. Actual input currents are obtained by multiplying unit load current by input load factor (see Loading Rules).

SWITCHING CHARACTERISTICS $T_A = 25°C$, $V^+ = 5.0V$, $C_L = 15pF$

PARAMETERS	DESCRIPTION		AM2502/3/4			AM25L02/3/4			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd+}	Turn Off Delay CP to Output HIGH		10	26	38	20	75	110*	ns
t_{pd-}	Turn On Delay CP to Output LOW		10	18	28	20	75	100	ns
$t_s(D)$	Set-up Time Data Input		−10	4	8	−15	8	20	ns
$t_s(\overline{S})$	Set-up Time Start Input		0	9	16	0	20	25	ns
$t_{pd+}(E)$	Turn Off Delay E to $Q_{7(11)}$	(AM25(L)03/4)		13	19		50	75	ns
$t_{pd-}(E)$	Turn On Delay E to $Q_{7(11)}$ LOW	$C_P = H$, $\overline{S} = L$		16	24		60	75	ns
$t_{pwL}(CP)$	Minimum LOW Clock Pulse Width			28	46		100	150	ns
$t_{pwH}(CP)$	Minimum HIGH Clock Pulse Width			12	20		70	100	ns
f_{max}	Maximum Clock Frequency		15	25		3.5	5.0		MHz

*Q_{11}, $\overline{Q}_{11}$ 30 ns slower

25(L)02/3 LOADING RULES (IN UNIT LOADS)

INPUT/ OUTPUT	PIN NO.'s	INPUT UNIT LOAD LOW	INPUT UNIT LOAD HIGH	FANOUT OUTPUT HIGH	FANOUT OUTPUT LOW
$\overline{E}$ (2503)	1	2	2	—	—
DO (2502)	1	—	—	12	6
$\overline{CC}$	2	—	—	12	6
Q_0	3	—	—	12	6
Q_1	4	—	—	12	6
Q_2	5	—	—	12	6
Q_3	6	—	—	12	6
D	7	2	2	—	—
GND	8	—	—	—	—
CP	9	1	1	—	—
$\overline{S}$	10	1	2	—	—
Q_4	11	—	—	12	6
Q_5	12	—	—	12	6
Q_6	13	—	—	12	6
$\overline{Q_7}$	14	—	—	12	6
Q_7	15	—	—	12	6
V^+	16	—	—	—	—

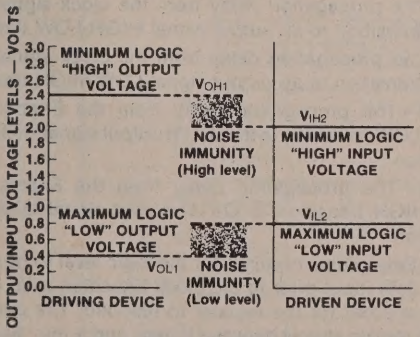
25(L)04 LOADING RULES (IN UNIT LOADS)

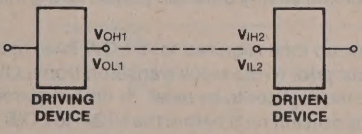
INPUT/ OUTPUT	PIN NO.'s	INPUT UNIT LOAD LOW	INPUT UNIT LOAD HIGH	FANOUT OUTPUT HIGH	FANOUT OUTPUT LOW
$\overline{E}$	1	2	2	—	—
DO	2	—	—	12	6
$\overline{CC}$	3	—	—	12	6
Q_0	4	—	—	12	6
Q_1	5	—	—	12	6
Q_2	6	—	—	12	6
Q_3	7	—	—	12	6
Q_4	8	—	—	12	6
Q_5	9	—	—	12	6
NC	10	—	—	—	—
D	11	2	2	—	—
GND	12	—	—	—	—
CP	13	1	1	—	—
$\overline{S}$	14	1	2	—	—
NC	15	—	—	—	—
Q_6	16	—	—	12	6
Q_7	17	—	—	12	6
Q_8	18	—	—	12	6
Q_9	19	—	—	12	6
Q_{10}	20	—	—	12	6
$\overline{Q_{11}}$	21	—	—	12	6
NC	22	—	—	—	—
Q_{11}	23	—	—	12	6
V^+	24	—	—	—	—

NC = No Connection

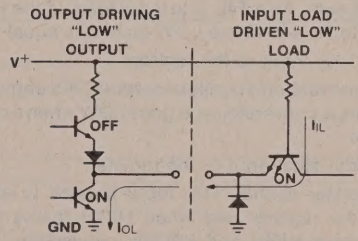
INPUT/OUTPUT INTERFACE CONDITIONS

VOLTAGE INTERFACE CONDITIONS — LOW & HIGH

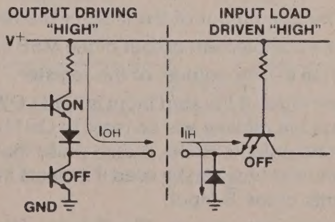



VOH1
VOL1
VIH2
VIL2
DRIVING DEVICE
DRIVEN DEVICE

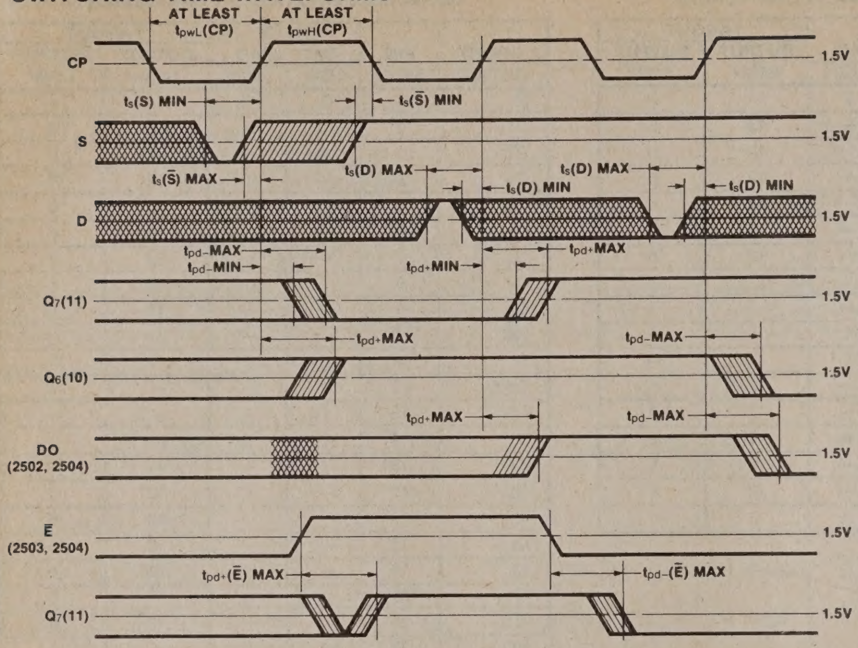
CURRENT INTERFACE CONDITIONS — LOW


OUTPUT DRIVING "LOW" OUTPUT
INPUT LOAD DRIVEN "LOW" LOAD
V+
OFF
ON
IIL
GND
IOL

CURRENT INTERFACE CONDITIONS — HIGH


OUTPUT DRIVING "HIGH"
INPUT LOAD DRIVEN "HIGH"
V+
ON
IOH
IIH
OFF
OFF
GND

SWITCHING TIME WAVEFORMS



ENABLE TO Q_7(11)
CP = H WHEN ENABLE CHANGES

APPLIES ONLY WHEN START-SIGNAL APPLIED DURING PREVIOUS CLOCK PERIOD.

KEY TO TIMING DIAGRAM

WAVE-FORM	INPUTS	OUTPUTS
═	MUST BE STEADY	WILL BE STEADY
▧	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▩	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H—HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I—Input.

L—LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O—Output.

FUNCTIONAL TERMS:

Fan-Out—The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T²L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP—The clock input of the register.

$\overline{CC}$—The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D—The serial data input of the register.

$\overline{E}$—The register enable. This input is used to expand the length of the register and when HIGH forces the Q_7(11) register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

Q_7(11)—The true output of the MSB of the register.

$\overline{Q}_7$(11)—The complement output of the MSB of the register.

Q_i, i = 7(11) to 0-The outputs of the register.

$\overline{S}$—The start input. If the start input is held LOW for at least a clock period the register will be reset to Q_7(11) LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

DO—The serial data output. (The D input delayed one bit.)

OPERATIONAL TERMS:

I_{IL}—Forward input load current.

I_{OH}—Output HIGH current, forced out of output V_{OH} test.

I_{OL}—Output LOW current, forced into the output in V_{OL} test.

I_{IH}—Reverse input load current.

Negative Current—Current flowing out of the device.

Positive Current—Current flowing into the device.

V_{IH}—Minimum logic HIGH input voltage.

V_{IL}—Maximum logic LOW input voltage.

V_{OH}—Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL}—Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level.)

t_{pd-}—The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+}—The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

t_{pd-}($\overline{E}$)—The propagation delay from the Enable signal HIGH-LOW transition to the Q_7(11) output signal HIGH-LOW transition.

t_{pd+}($\overline{E}$)—The propagation delay from the Enable signal LOW-HIGH transition to Q_7(11) output signal LOW-HIGH transition.

t_s(D)—Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max, and t_s min. before the clock.

t_s($\overline{S}$)—Set-up time required for a LOW level to be present at the $\overline{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on $\overline{S}$ before the HIGH to LOW clock transition to prevent resetting.

t_{pw}(CP)—The minimum clock pulse width (LOW or HIGH) required for proper register operation.

AM25(L)02/3 TRUTH TABLE

TIME	INPUTS			OUTPUTS									
t_n	D	S	E	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	CC
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

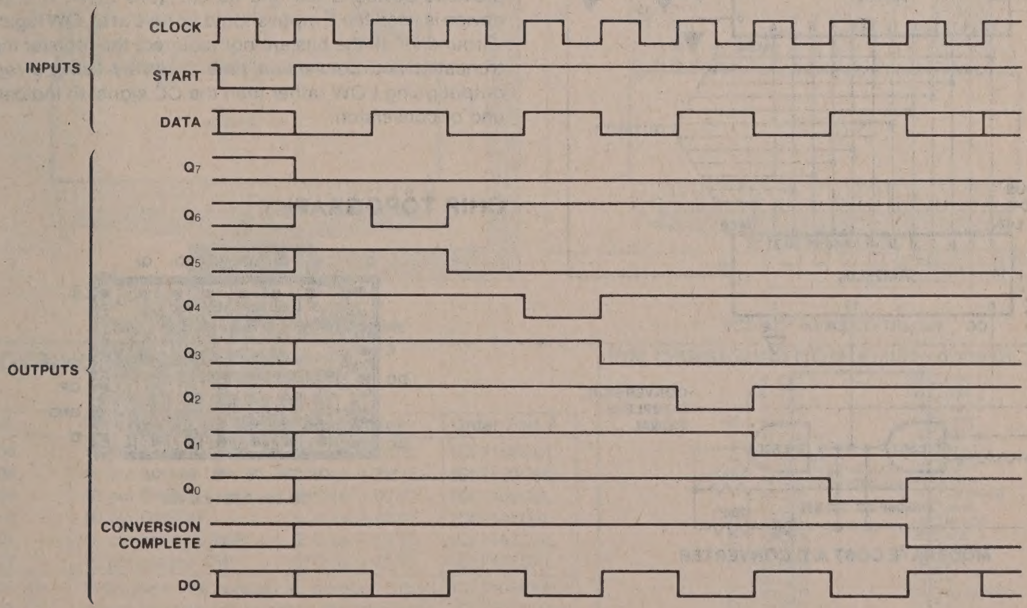
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: Truth Table for 25(L)04 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with current switches which are either active high or active low. If active low current switches are used, the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If active high current switches are used then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±1/2 LSB the comparator must be biased. If active high current switches are used, the comparator should be biased +1/2 LSB and if the current switches are active low, the comparator must be biased −1/2 LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can also be used to perform 2's complement conversion by offsetting the comparator 1/2 full range +1/2 LSB and using the complement of the MSB $Q_7(11)$ as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

AM25(L)02/3 TIMING CHART



Note: Arbitrary Conversion shown. Timing chart for AM25(L)04 is extended to include 12 outputs, starting with Q_{11}.

ORDERING INFORMATION

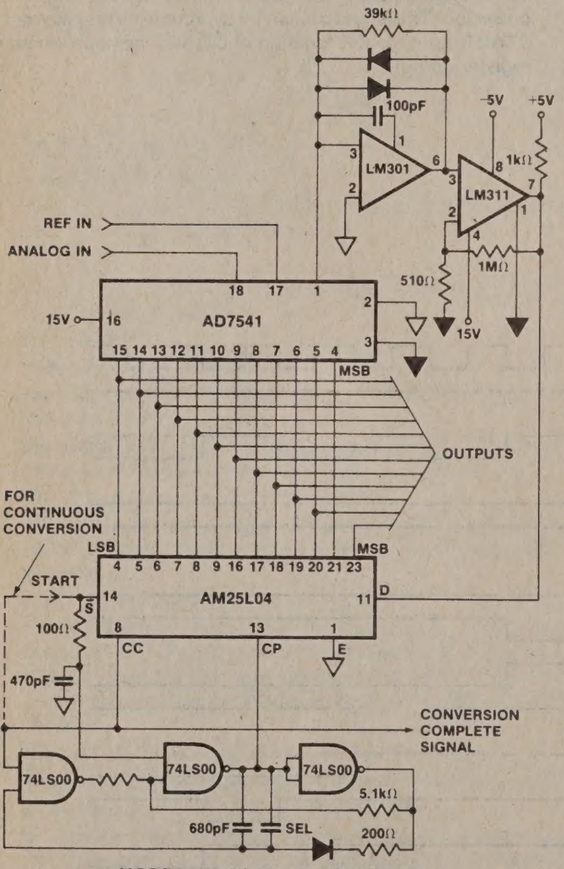
PART	16 PIN CERDIP	16 PIN PLASTIC DIP	DICE	
AM2502C	AM2502DC	AM2502PC	AM2502XC	
AM2502M	AM2502DM		AM2502XM	
AM2503C	AM2503DC	AM2503PC	AM2503XC	
AM2503M	AM2503DM		AM2503XM	
	24 pin CERDIP	24 pin plastic DIP	24 pin Flatpak	Dice
AM2504C	AM2504DC	AM2504PC		AM2504XC
AM2504M	AM2504DM		AM2504FM	AM2504XM

To order "L" devices, insert "L" following "25"; e.g., AM25L02DM

NOTES: C - Commercial Temperature Range (0°C to +70°C)
M - Military Temperature Range (−55°C to +125°C)

CIRCUIT DESCRIPTION

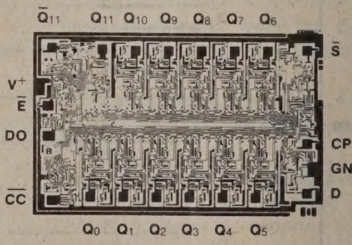
The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a START signal.


39kΩ
100pF
LM301
LM311
−5V
+5V
1kΩ
1MΩ
510Ω
15V
REF IN
ANALOG IN
15V
AD7541
18 17 1 2 3 16
15 14 13 12 11 10 9 8 7 6 5 4
MSB
OUTPUTS
FOR CONTINUOUS CONVERSION
LSB
MSB
4 5 6 7 8 9 16 17 18 19 20 21 23
START
S
14
AM25L04
11
D
100Ω
8
13
1
CC
CP
E
470pF
CONVERSION COMPLETE SIGNAL
74LS00
74LS00
74LS00
5.1kΩ
680pF
SEL
200Ω

MODERATE COST A/D CONVERTER

To allow two's complement conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the 2503 and 2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the START signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

CHIP TOPOGRAPHY


$\overline{Q}_{11}$
Q_{11} Q_{10} Q_9 Q_8 Q_7 Q_6
$\overline{S}$
V+
$\overline{E}$
DO
$\overline{CC}$
CP
GND
D
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5

Die size 0.95" x 0.142"

ICL7106/7107
3½ Digit Single Chip A/D Converter

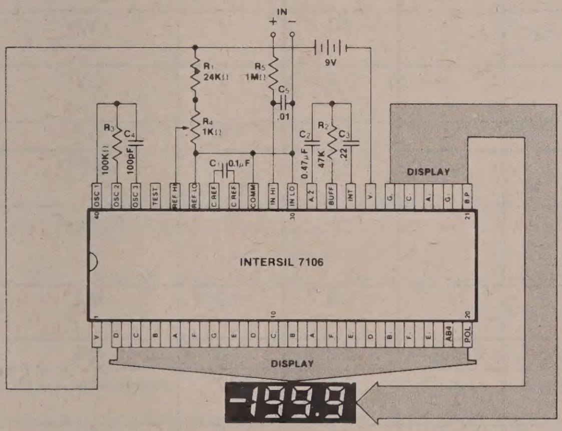
FEATURES

- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA typical input current.**
- **True differential input and reference.**
- **Direct display drive - no external components required. — LCD ICL7106**
  — LED ICL7107
- **Low noise - less than 15μV p-p.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**
- **Evaluation Kit available.**

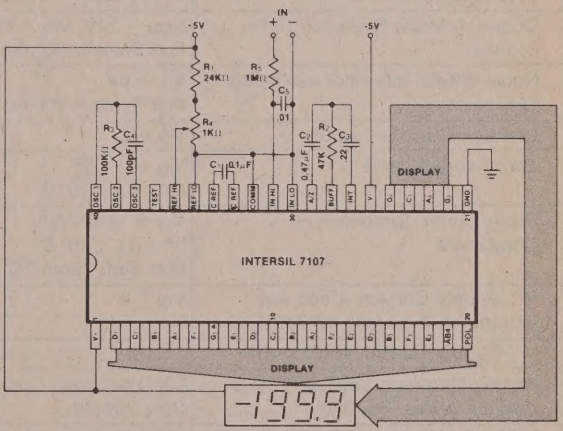
GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3-1/2 digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7106), enabling a high performance panel meter to be built with the addition of only 7 passive components and a display.


IN
+
−
9V
R1
24KΩ
R5
1MΩ
C5
.01
R3
100KΩ
C4
100pF
R4
1KΩ
C1
0.1μF
C2
0.47μF
R2
47K
C3
.22
DISPLAY
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMM
IN HI
IN LO
A/Z
BUFF
INT
V
G
C
A
G
BP
40
30
21
INTERSIL 7106
1
10
20
V
D
C
B
A
F
G
E
D
C
B
A
F
E
D
B
F
E
AB4
POL
DISPLAY
-199.9

ICL7106 with Liquid Crystal Display

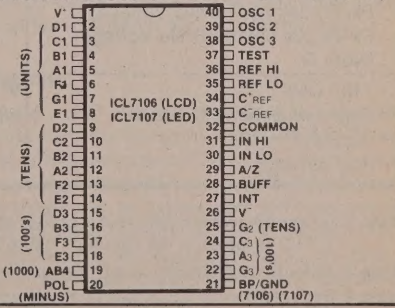

IN
+
−
-5V
-5V
R1
24KΩ
R5
1MΩ
C5
.01
R3
100KΩ
C4
100pF
R4
1KΩ
C1
0.1μF
C2
0.47μF
R2
47K
C3
.22
DISPLAY
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMM
IN HI
IN LO
A/Z
BUFF
INT
V
G
C
A
G
GND
40
30
21
INTERSIL 7107
1
10
20
V
D
C
B
A
F
G
E
D
C
B
A
F
E
D
B
F
E
AB4
POL
DISPLAY
-199.9

ICL7107 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7106	40 pin ceramic DIP	0°C to +70°C	ICL7106CDL
7106	40 pin plastic DIP	0°C to +70°C	ICL7106CPL
7106	40 pin CERDIP	0°C to +70°C	ICL7106CJL
7107	40 pin CERDIP	0°C to +70°C	ICL7107CJL
7107	40 pin ceramic DIP	0°C to +70°C	ICL7107CDL
7107	40 pin plastic DIP	0°C to +70°C	ICL7107CPL
7106 Kit 7107 Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware. See page 10.		ICL7106EV/Kit ICL7107EV/Kit

PIN CONFIGURATION (Outline dwgs DL, JL, PL)


V+ 1
D1 2
C1 3
B1 4
A1 5
F1 6
G1 7
E1 8
D2 9
C2 10
B2 11
A2 12
F2 13
E2 14
D3 15
B3 16
F3 17
E3 18
(1000) AB4 19
POL 20
(MINUS)
(UNITS)
(TENS)
(100's)
ICL7106 (LCD)
ICL7107 (LED)
40 OSC 1
39 OSC 2
38 OSC 3
37 TEST
36 REF HI
35 REF LO
34 C+REF
33 C−REF
32 COMMON
31 IN HI
30 IN LO
29 A/Z
28 BUFF
27 INT
26 V−
25 G2 (TENS)
24 C3
23 A3
22 G3
(100's)
21 BP/GND
(7106) (7107)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+)
ICL7106 .... 15V
ICL7107 .... +6V
Supply Voltage (V^-)
ICL7106 .... 15V
ICL7107 .... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) .... V^+ to V^-
Clock Input
ICL7106 .... Test to V^+
ICL7107 .... Gnd to V^+

Power Dissipation (ICL7106 Note 2; ICL7107 Note 1)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature .... 0°C to +70°C
Storage Temperature .... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) .... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current | Input	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0V Segment voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25°C, f_{clock} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion below.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

TEST CIRCUITS

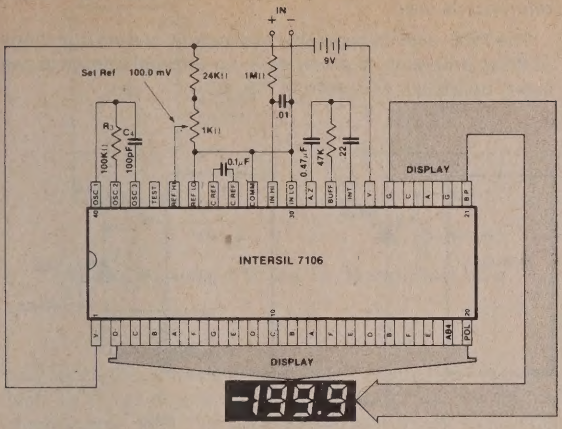

IN
Set Ref 100.0 mV
24K
1M
9V
.01
1K
0.1μF
0.47μF
47K
.22
100K
100pF
DISPLAY
INTERSIL 7106
-199.9

Figure 1: 7106

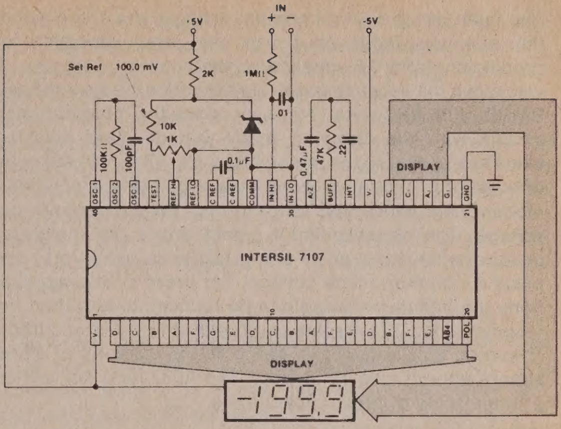

IN
+5V
-5V
Set Ref 100.0 mV
2K
1M
10K
1K
.01
0.1μF
0.47μF
47K
.22
100K
100pF
DISPLAY
INTERSIL 7107
-1999

Figure 2: 7107

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL 7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) deintegrate (DE).

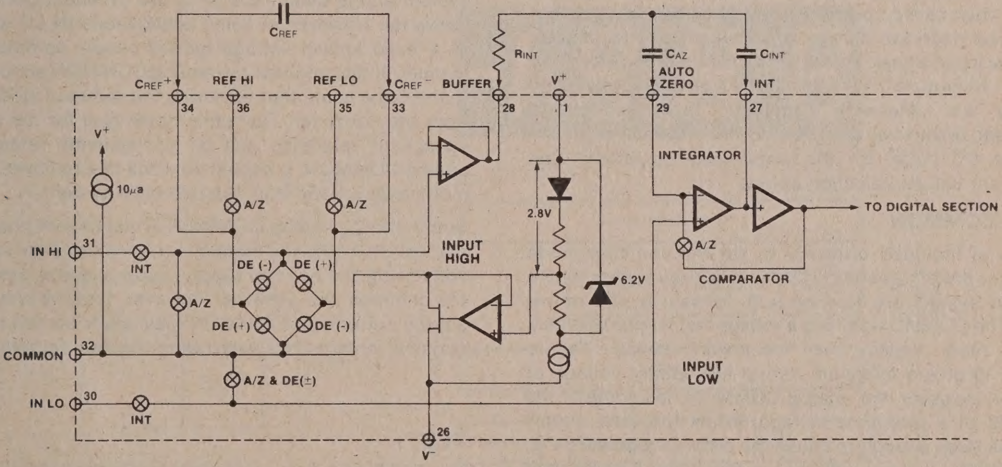

CREF
CREF+
REF HI
REF LO
CREF−
BUFFER
RINT
V+
CAZ
AUTO ZERO
CINT
INT
34
36
35
33
28
1
29
27
INTEGRATOR
10μa
A/Z
2.8V
TO DIGITAL SECTION
IN HI
31
INT
DE (-)
DE (+)
INPUT HIGH
COMPARATOR
6.2V
DE (+)
DE (-)
COMMON
32
A/Z & DE(±)
INPUT LOW
IN LO
30
26
V−

Figure 3: Analog Section of 7106/7107

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $(\frac{V_{IN}}{V_{REF}})$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Values Selection below).

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80μVp-p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

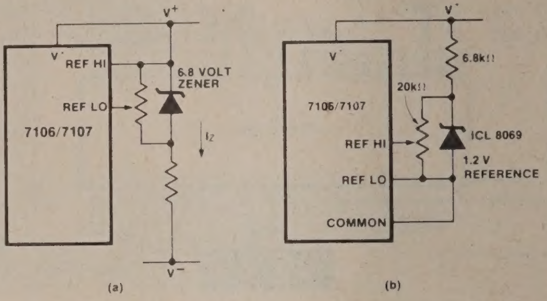


Figure 4: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7106 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

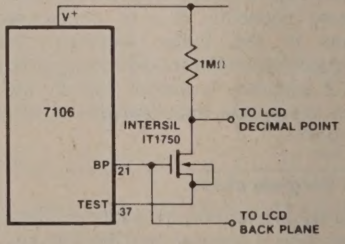


Figure 5: Simple Inverter for Fixed Decimal Point

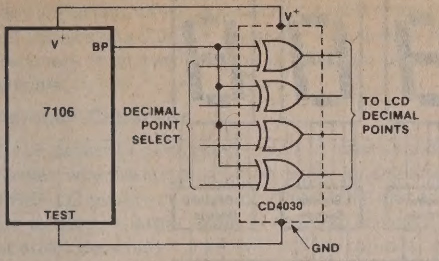

V+
V+
BP
7106
DECIMAL POINT SELECT
TO LCD DECIMAL POINTS
TEST
CD4030
GND

Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled high (to V+) all segments will be turned on and the display should read - 1888. The TEST pin will sink about 10mA under these conditions.

Caution: on the 7106, in the lamp test mode, the segments have a constant d-c voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

DIGITAL SECTION

Figures 7 and 8 show the digital section for the 7106 and 7107, respectively. In the 7106, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases neglible d-c voltage exists across the segments.

Figure 8 is the Digital Section of the 7107. It is identical to the 7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

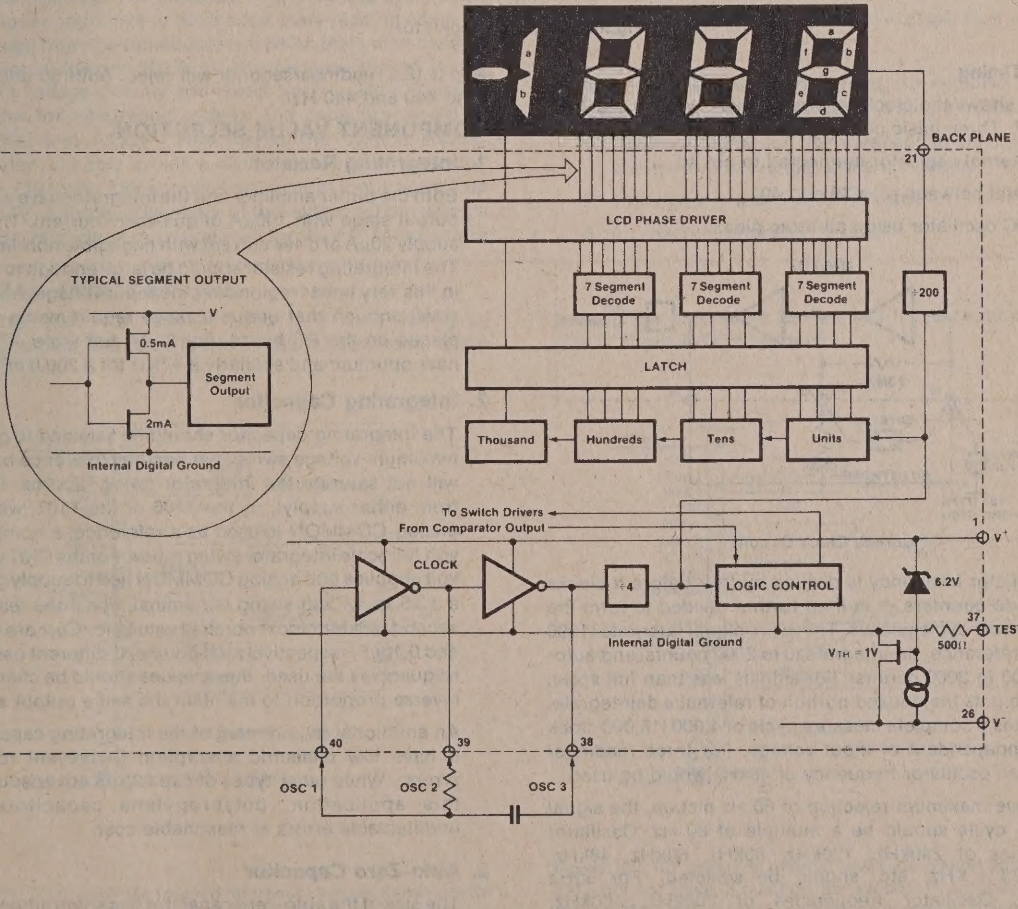

a
b
a
f
b
g
e
c
d
BACK PLANE
21
LCD PHASE DRIVER
7 Segment Decode
7 Segment Decode
7 Segment Decode
÷200
LATCH
Thousand
Hundreds
Tens
Units
TYPICAL SEGMENT OUTPUT
V+
0.5mA
Segment Output
2mA
Internal Digital Ground
To Switch Drivers
From Comparator Output
CLOCK
÷4
LOGIC CONTROL
1
V+
6.2V
37
TEST
500Ω
Internal Digital Ground
V_TH = 1V
26
V−
40
39
38
OSC 1
OSC 2
OSC 3

Figure 7: Digital Section 7106

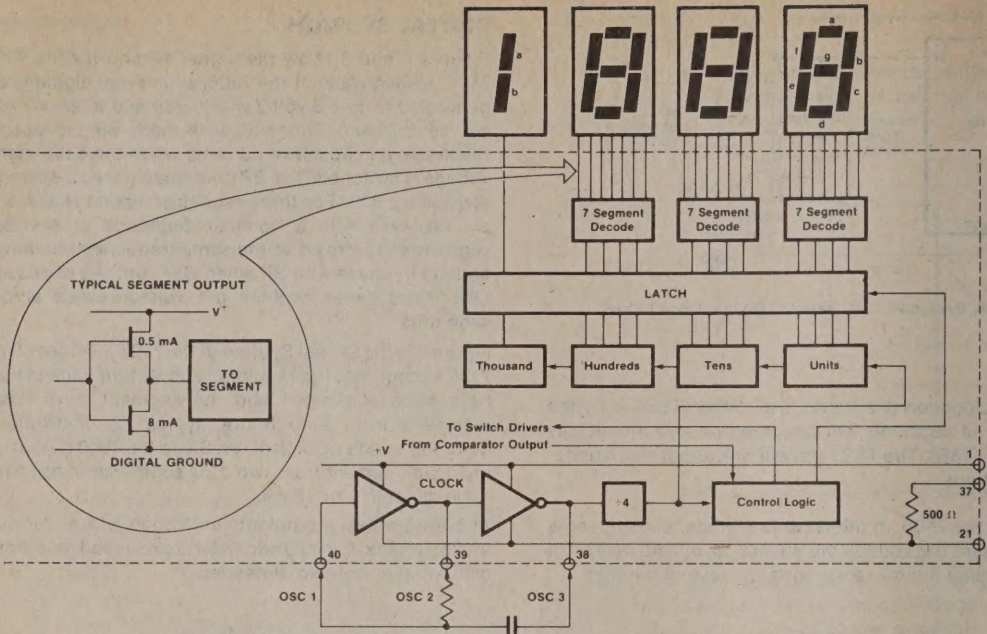

a
b
f
g
e
c
d
TYPICAL SEGMENT OUTPUT
V+
0.5 mA
TO SEGMENT
8 mA
DIGITAL GROUND
7 Segment Decode
7 Segment Decode
7 Segment Decode
LATCH
Thousand
Hundreds
Tens
Units
To Switch Drivers
From Comparator Output
+V
CLOCK
÷4
Control Logic
1
V+
37
TEST
500 Ω
21
DIGITAL GROUND
40
39
38
OSC 1
OSC 2
OSC 3

Figure 8: Digital Section 7107

System Timing

Figure 9 shows the clocking arrangement used in the 7106 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

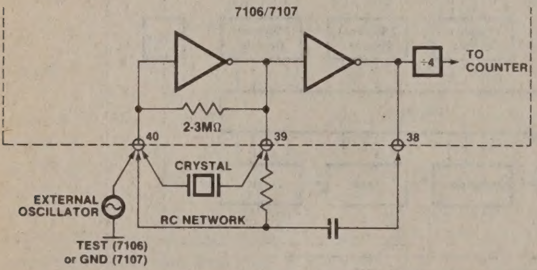

7106/7107
÷4
TO COUNTER
2-3MΩ
40
39
38
CRYSTAL
EXTERNAL OSCILLATOR
RC NETWORK
TEST (7106) or GND (7107)

Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33⅓ kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66⅔ kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470KΩ is near optimum and similarly a 47KΩ for a 200.0 mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7106 or the 7107, when the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7107 with ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 100KΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{.45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = .341V. Suitable values for integrating resistor and capacitor would be 120KΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this sytem occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7. 7107 Power Supplies

The 7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

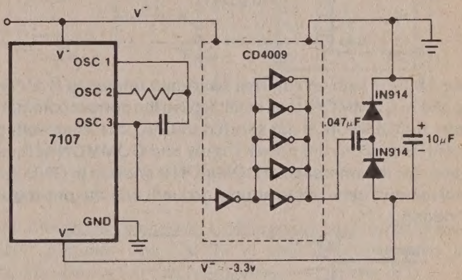

V⁺
V⁺
OSC 1
OSC 2
OSC 3
7107
GND
V⁻
CD4009
.047μF
IN914
IN914
10μF
V⁻ = -3.3v

Figure 10: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7106 and 7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

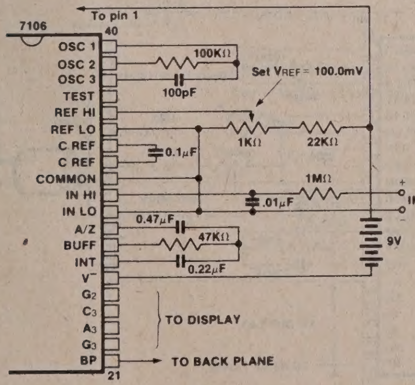

To pin 1
7106
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
BP
21
100KΩ
100pF
Set VREF = 100.0mV
1KΩ
22KΩ
0.1μF
1MΩ
.01μF
IN
+
-
9V
0.47μF
47KΩ
0.22μF
TO DISPLAY
TO BACK PLANE

Figure 11: 7106 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

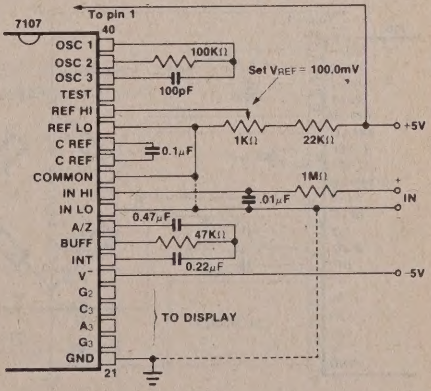

To pin 1
7107
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
GND
21
100KΩ
100pF
Set VREF = 100.0mV
1KΩ
22KΩ
+5V
0.1μF
1MΩ
.01μF
IN
+
0.47μF
47KΩ
0.22μF
-5V
TO DISPLAY

Figure 12: 7107 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

TYPICAL APPLICATIONS (Contd.)

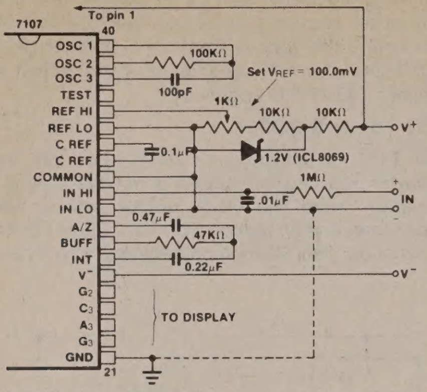

7107
To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
GND
21
100KΩ
100pF
Set VREF = 100.0mV
1KΩ
10KΩ
10KΩ
V+
0.1μF
1.2V (ICL8069)
1MΩ
.01μF
IN
0.47μF
47KΩ
0.22μF
V⁻
TO DISPLAY

Figure 13: 7107 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply ground) and the pre-regulator is over-ridden.

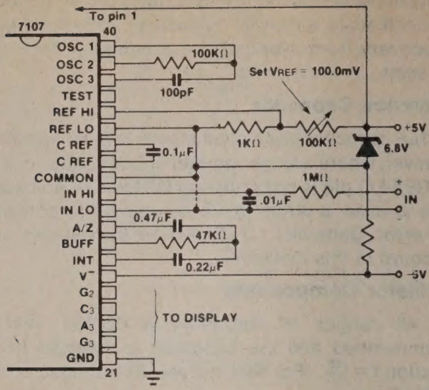

7107
To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
GND
21
100KΩ
100pF
Set VREF = 100.0mV
1KΩ
100KΩ
+5V
6.8V
0.1μF
1MΩ
.01μF
IN
0.47μF
47KΩ
0.22μF
-5V
TO DISPLAY

Figure 14: 7107 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 12, IN LO may be tied to either COMMON or GND.

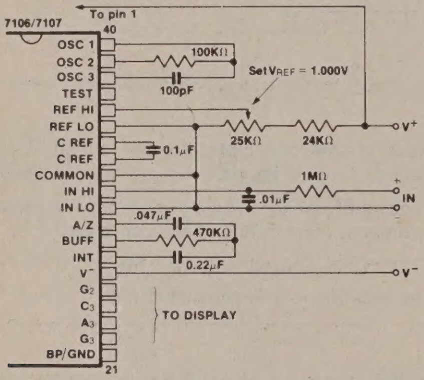

7106/7107
To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
BP/GND
21
100KΩ
100pF
Set VREF = 1.000V
25KΩ
24KΩ
V+
0.1μF
1MΩ
.01μF
IN
.047μF
470KΩ
0.22μF
V⁻
TO DISPLAY

Figure 15: 7106/7107: Recommended component values for 2.000V full scale.

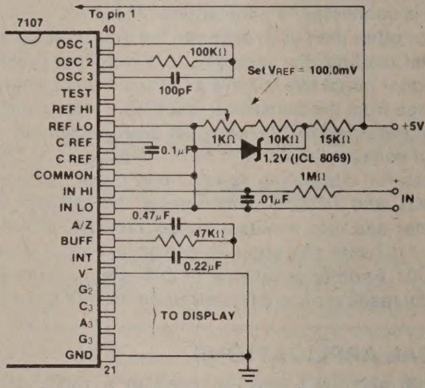

7107
To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
GND
21
100KΩ
100pF
Set VREF = 100.0mV
1KΩ
10KΩ
15KΩ
+5V
1.2V (ICL 8069)
0.1μF
1MΩ
.01μF
IN
0.47μF
47KΩ
0.22μF
TO DISPLAY

Figure 16: 7107 operated from single +5V supply. An external reference must be used in this application, since the voltage between V+ and V⁻ is insufficient for correct operation of the internal reference.

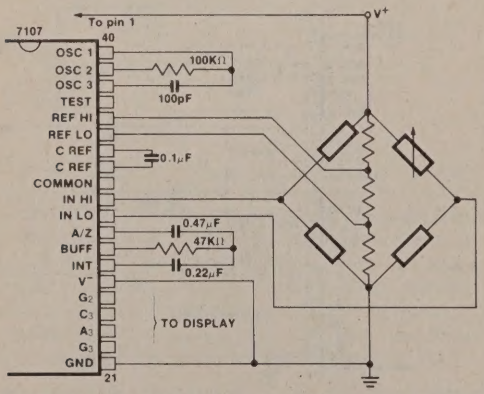

7107
To pin 1
40
V+
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
GND
21
100KΩ
100pF
0.1μF
0.47μF
47KΩ
0.22μF
TO DISPLAY

Figure 17: 7107 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

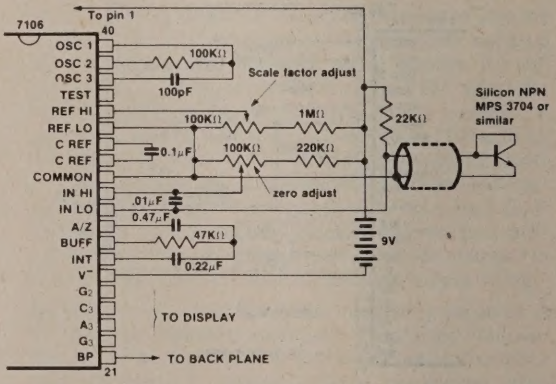

7106
To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
BP
21
100KΩ
100pF
Scale factor adjust
100KΩ
1MΩ
22KΩ
Silicon NPN MPS 3704 or similar
0.1μF
100KΩ
220KΩ
zero adjust
.01μF
0.47μF
47KΩ
0.22μF
9V
TO DISPLAY
TO BACK PLANE

Figure 18: 7106 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

TYPICAL APPLICATIONS (Contd.)

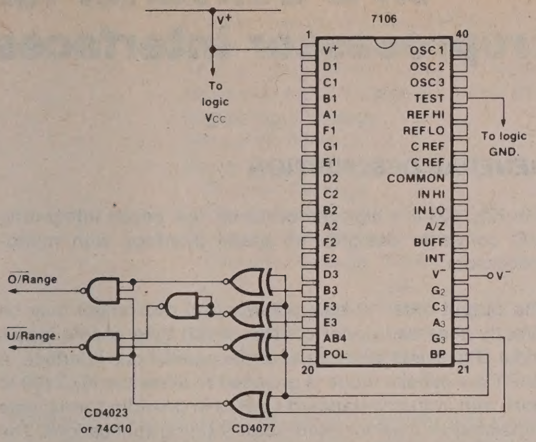

V+
7106
1
40
To logic VCC
V+
D1
C1
B1
A1
F1
G1
E1
D2
C2
B2
A2
F2
E2
D3
B3
F3
E3
AB4
POL
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V−
G2
C3
A3
G3
BP
20
21
To logic GND.
V−
O/Range
U/Range
CD4023 or 74C10
CD4077

Figure 19: Circuit for developing Underrange and Overrange signals from 7106 outputs.

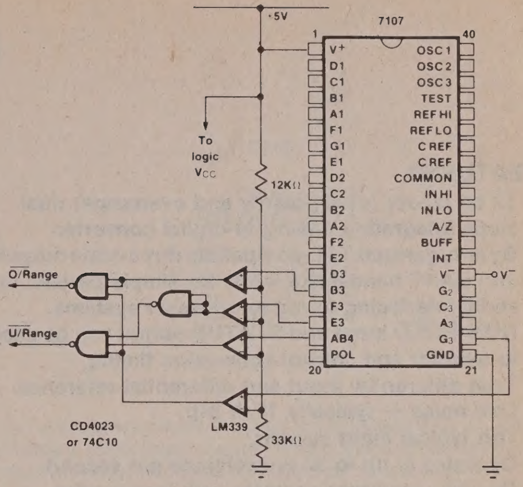

+5V
7107
1
40
To logic VCC
12KΩ
V+
D1
C1
B1
A1
F1
G1
E1
D2
C2
B2
A2
F2
E2
D3
B3
F3
E3
AB4
POL
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V−
G2
C3
A3
G3
GND
20
21
V−
O/Range
U/Range
CD4023 or 74C10
LM339
33KΩ

Figure 20: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

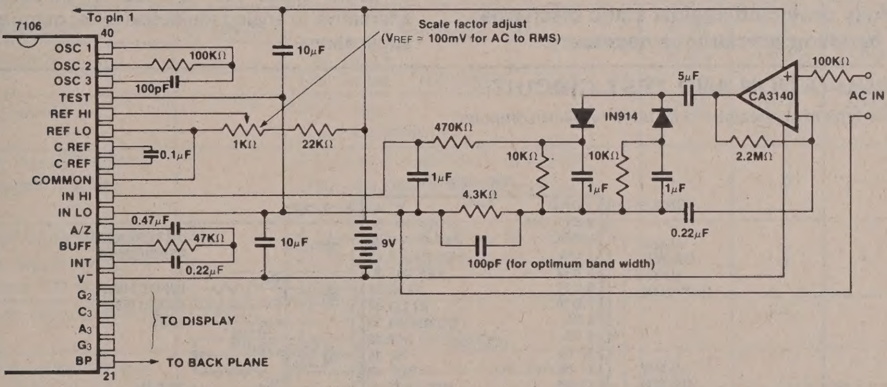

7106
To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V−
G2
C3
A3
G3
BP
21
100KΩ
100pF
10µF
Scale factor adjust
(VREF = 100mV for AC to RMS)
1KΩ
22KΩ
0.1µF
470KΩ
1µF
4.3KΩ
100pF (for optimum band width)
10KΩ
10KΩ
1µF
1µF
IN914
5µF
CA3140
100KΩ
AC IN
2.2MΩ
0.22µF
0.47µF
47KΩ
10µF
9V
0.22µF
TO DISPLAY
TO BACK PLANE

Figure 21: AC to DC Converter with 7106. TEST is used as a common mode reference level to ensure compatibility with most op-amps.

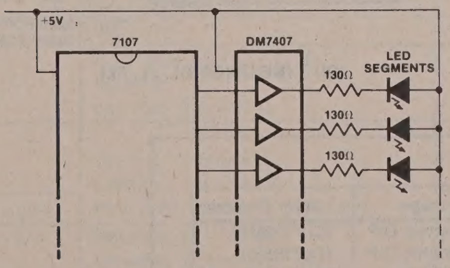

+5V
7107
DM7407
LED SEGMENTS
130Ω
130Ω
130Ω

Figure 22: Display Buffering for increased drive current. Requires four DM7407 Hex Buffers. Each buffer is capable of sinking 40 mA.

INTERSIL

ICL7109 12 Bit Binary A/D Converter for Microprocessor Interfaces

FEATURES

- **12 bit binary (plus polarity and overrange) dual slope integrating analog-to-digital converter.**
- **Byte-organized TTL-compatible three-state outputs and UART handshake mode for simple parallel or serial interfacing to microprocessor systems.**
- **RUN/$\overline{\text{HOLD}}$ input and STATUS output can be used to monitor and control conversion timing.**
- **True differential input and differential reference.**
- **Low noise — typically 15μV p-p.**
- **1pA typical input current.**
- **Operates at up to 30 conversions per second.**
- **On-chip oscillator operates with inexpensive 3.58MHz TV crystal giving 7.5 conversions per second for 60Hz rejection. May also be operated as RC oscillator for other clock frequencies.**
- **Fabricated using MAX-CMOS™ technology combining analog and digital functions on a single low power LSI CMOS chip.**
- **All inputs fully protected against static discharge; no special handling precautions necessary.**

GENERAL DESCRIPTION

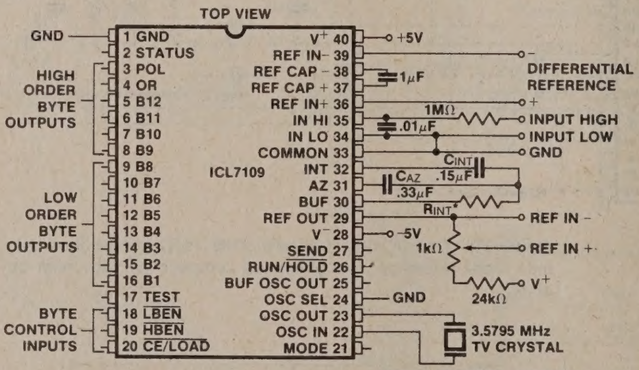
The ICL7109 is a high performance, low power integrating A/D converter designed to easily interface with microprocessors.

The output data (12 bits, polarity and overrange) may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. A UART handshake mode is provided to allow the ICL7109 to work with industry-standard UARTs in providing serial data transmission, ideal for remote data logging applications. The RUN/HOLD input and STATUS output allow monitoring and control of conversion timing.

The ICL7109 provides the user with the high accuracy, low noise, low drift, versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than 1μV/°C, maximum input bias current of 10pA, and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

PIN CONFIGURATION AND TEST CIRCUIT:

(See Figure 1 for typical connection to a UART or Microcomputer)


TOP VIEW
GND
HIGH ORDER BYTE OUTPUTS
LOW ORDER BYTE OUTPUTS
BYTE CONTROL INPUTS
1 GND
2 STATUS
3 POL
4 OR
5 B12
6 B11
7 B10
8 B9
9 B8
10 B7
11 B6
12 B5
13 B4
14 B3
15 B2
16 B1
17 TEST
18 LBEN
19 HBEN
20 CE/LOAD
ICL7109
V+ 40
REF IN− 39
REF CAP − 38
REF CAP + 37
REF IN+ 36
IN HI 35
IN LO 34
COMMON 33
INT 32
AZ 31
BUF 30
REF OUT 29
V− 28
SEND 27
RUN/HOLD 26
BUF OSC OUT 25
OSC SEL 24
OSC OUT 23
OSC IN 22
MODE 21
+5V
1μF
−
DIFFERENTIAL REFERENCE
+
1MΩ
.01μF
INPUT HIGH
INPUT LOW
GND
CINT .15μF
CAZ .33μF
RINT*
REF IN −
−5V
1kΩ
REF IN +
V+
24kΩ
GND
3.5795 MHz TV CRYSTAL

*R_{INT} = 20kΩ FOR 0.2V REF
= 200kΩ FOR 2.0V REF

(OUTLINE DWGS DL, JL, PL)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
7109	−55°C to +125°C	40-Pin Ceramic DIP	ICL7109MDL
7109	−20°C to +85°C	40-Pin Ceramic DIP	ICL7109IDL
7109	−20°C to +85°C	40-Pin CERDIP	ICL7109IJL
7109	0°C to 70°C	40-Pin Plastic DIP	ICL7109CPL

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+)	+6.2V
Negative Supply Voltage (GND to V^-)	−9V
Analog Input Voltage (Lo or Hi) (Note 1)	V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1)	V^+ to V^-
Digital Input Voltage (Pins 2-27) (Note 2)	$V^+ + 0.3V$ GND − 0.3V
Power Dissipation (Note 3)	
Ceramic Package	1W @ +85°C
Plastic Package	500mW @ +70°C
Operating Temperature	
Ceramic Package (MDL)	$-55°C \le T_A \le +125°C$
(IDL)	$-25°C \le T_A \le +85°C$
Plastic Package (CPL)	$0°C \le T_A \le +70°C$
Storage Temperature	$-55°C \le T_A \le +125°C$
Lead Temperature (soldering, 60 sec.)	+300°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE I OPERATING CHARACTERISTICS

All parameters with $V^+ = +5V$, $V^- = -5V$, GND = 0V, $T_A = 25°C$, unless otherwise indicated.
Test circuit as shown on page 1.

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading		$V_{IN} = 0.0V$ Full Scale = 409.6mW	-0000_8	$\pm 0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ $V_{REF} = 204.8mV$	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	−1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	−1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V $V_{IN} = 0V$ Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	VCMR	Input Hi, Input Lo, Common	$V^- + 1.5$		$V^+ - 1.0$	V
Noise (p-p value not exceeded 95% of time)	e_n	$V_{IN} = 0V$ Full Scale = 409.6mV		15		μV
Leakage current at Input	I_{ILK}	$V_{IN} = 0$ All devices 25°C ICL7109CPL $0°C \le T_A \le +70°C$ ICL7109IDC $-25°C \le T_A \le +85°C$ ICL7109MDL $-55°C \le T_A \le +125°C$		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		$V_{IN} = 0V$		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV = > 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	$V_{IN} = 0$, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29, open		700	1500	μA
Supply Current V^+ to V^-	I_{SUPP}			700	1500	μA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	−2.4	−2.8	−3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C
Input Common Mode Range	V_{CM}	IN HI, IN LO, COMMON	$V^- + 1.5$	$V^+ - 0.5$ to $V^- + 1.0$	$V^+ - 1.0$	V

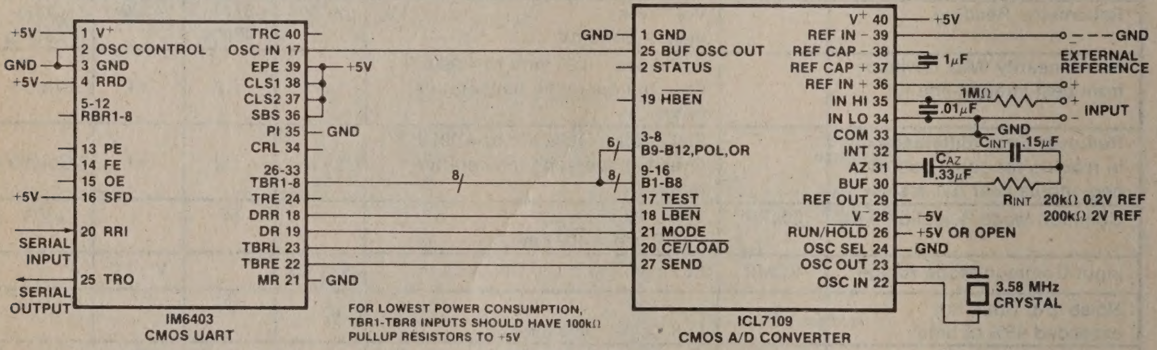
DIGITAL SECTION

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage		V_{OH}	I_{OUT} = 100μA Pins 2-16, 18, 19, 20	3.5	4.3		V
Output Low Voltage		V_{OL}	I_{OUT} = 1.6mA		0.2	0.4	V
Output Leakage Current			Pins 3-16 high impedance		±.01	±1	μA
Control I/O Pullup Current			Pins 18, 19, 20 $V_{OUT} = V^+ -3V$ MODE input at GND		5		μA
Control I/O Loading			$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18			50	pF
Input High Voltage		V_{IH}	Pins 18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage		V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current			Pins 26, 27 $V_{OUT} = V^+ -3V$		5		μA
Input Pull-up Current			Pins 17, 24 $V_{OUT} = V^+ -3V$		25		μA
Input Pull-down Current			Pin 21 V_{OUT} = GND +3V		5		μA
Oscillator Output Current	High	O_{OH}	V_{OUT} = 2.5V		1		mA
	Low	O_{OL}	V_{OUT} = 2.5V		1.5		mA
Buffered Oscillator Output Current	High	BO_{OH}	V_{OUT} = 2.5V		2		mA
	Low	BO_{OL}	V_{OUT} = 2.5V		5		mA
MODE Input Pulse Width		t_W		50			ns

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA

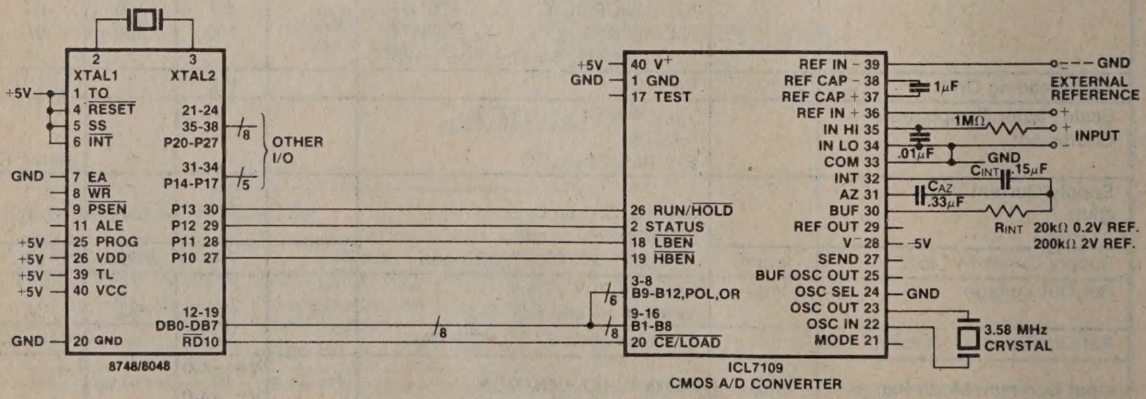
Note 2: Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V⁺ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.

Note 3: This limit refers to that of the package and will not be obtained during normal operation.



+5V
1 V+
2 OSC CONTROL
GND
3 GND
+5V
4 RRD
5-12 RBR1-8
13 PE
14 FE
15 OE
+5V
16 SFD
20 RRI
SERIAL INPUT
25 TRO
SERIAL OUTPUT
TRC 40
OSC IN 17
EPE 39
+5V
CLS1 38
CLS2 37
SBS 36
PI 35
GND
CRL 34
26-33 TBR1-8
TRE 24
DRR 18
DR 19
TBRL 23
TBRE 22
MR 21
GND
IM6403
CMOS UART
FOR LOWEST POWER CONSUMPTION, TBR1-TBR8 INPUTS SHOULD HAVE 100kΩ PULLUP RESISTORS TO +5V
8
6
8
GND
1 GND
25 BUF OSC OUT
2 STATUS
19 HBEN
3-8 B9-B12,POL,OR
9-16 B1-B8
17 TEST
18 LBEN
21 MODE
20 CE/LOAD
27 SEND
V+ 40
REF IN - 39
REF CAP - 38
REF CAP + 37
REF IN + 36
IN HI 35
IN LO 34
COM 33
INT 32
AZ 31
BUF 30
REF OUT 29
V- 28
RUN/HOLD 26
OSC SEL 24
OSC OUT 23
OSC IN 22
ICL7109
CMOS A/D CONVERTER
+5V
GND
1μF
EXTERNAL REFERENCE
1MΩ
.01μF
INPUT
GND
CINT .15μF
CAZ .33μF
RINT 20kΩ 0.2V REF
200kΩ 2V REF
-5V
+5V OR OPEN
GND
3.58 MHz CRYSTAL

Figure 1A. Typical Connection Diagram UART Interface - To transmit latest result, send any word to UART



2 XTAL1
3 XTAL2
+5V
1 TO
4 RESET
5 SS
6 INT
GND
7 EA
8 WR
9 PSEN
11 ALE
+5V
25 PROG
+5V
26 VDD
+5V
39 TL
+5V
40 VCC
GND
20 GND
21-24 35-38 P20-P27
8
OTHER I/O
31-34 P14-P17
5
P13 30
P12 29
P11 28
P10 27
12-19 DB0-DB7
RD10
8748/8048
8
6
8
+5V
40 V+
GND
1 GND
17 TEST
26 RUN/HOLD
2 STATUS
18 LBEN
19 HBEN
3-8 B9-B12,POL,OR
9-16 B1-B8
20 CE/LOAD
REF IN - 39
REF CAP - 38
REF CAP + 37
REF IN + 36
IN HI 35
IN LO 34
COM 33
INT 32
AZ 31
BUF 30
REF OUT 29
V- 28
SEND 27
BUF OSC OUT 25
OSC SEL 24
OSC OUT 23
OSC IN 22
MODE 21
ICL7109
CMOS A/D CONVERTER
GND
1μF
EXTERNAL REFERENCE
1MΩ
INPUT
.01μF
GND
CINT .15μF
CAZ .33μF
RINT 20kΩ 0.2V REF.
200kΩ 2V REF.
-5V
GND
3.58 MHz CRYSTAL

Figure 1B: Typical Connection Diagram Parallel Interface With MCS-48 Microcomputer

TABLE 2 - Pin Assignment and Function Description

PIN	SYMBOL	DESCRIPTION			
1	GND	Digital Ground, 0V, Ground return for all digital logic			
2	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.			
3	POL	Polarity - HI for Positive Input.			All three state output data bits
4	OR	Overrange - HI if Overranged.			
5	B12	Bit 12	(Most Significant Bit)		
6	B11	Bit 11	HI = true		
7	B10	Bit 10			
8	B9	Bit 9			
9	B8	Bit 8			
10	B7	Bit 7			
11	B6	Bit 6			
12	B5	Bit 5			
13	B4	Bit 4			
14	B3	Bit 3			
15	B2	Bit 2			
16	B1	Bit 1	(Least Significant Bit)		
17	TEST	Input High - Normal Operation. Input Low - Forces all bit outputs high. Note: This input is used for test purposes only.			
18	$\overline{\text{LBEN}}$	Low Byte Enable - With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8. - With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 7, 8, 9.			
19	$\overline{\text{HBEN}}$	High Byte Enable - With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, POL, OR. - With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 7, 8, 9.			
20	$\overline{\text{CE/LOAD}}$	Chip Enable Load - With Mode (Pin 21) low, $\overline{\text{CE/LOAD}}$ serves as a master output enable. When high, B1-B12, POL, OR outputs are disabled. - With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 7, 8, 9.			
21	MODE	Input Low - Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High - Causes immediate entry into handshake mode and output of data as in Figure 9. Input High - Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversion completion.			
22	OSC IN	Oscillator Input			
23	OSC OUT	Oscillator Output			
24	OSC SEL	Oscillator Select - Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator - clock will be same phase and duty cycle as BUF OSC OUT. - Input low configures OSC IN, OSC OUT for crystal oscillator - clock frequency will be 1/58 of frequency at BUF OSC OUT.			
25	BUF OSC OUT	Buffered Oscillator Output			
26	RUN/$\overline{\text{HOLD}}$	Input High - Conversions continuously performed every 8192 clock pulses. Input Low - Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.			
27	SEND	Input - Used in handshake mode to indicate ability of an external device to accept data.			
28	V^-	Analog Negative Supply - Nominally –5V with respect to GND (Pin 1).			
29	REF OUT	Reference Voltage Output - Nominally 2.8V down from V^+ (Pin 40).			
30	BUFFER	Buffer Amplifier Output			
31	AUTO-ZERO	Auto-Zero Node - Inside foil of C_{AZ}			
32	INTEGRATOR	Integrator Output - Outside foil of C_{INT}			
33	COMMON	Analog Common - System is Auto-Zeroed to COMMON			
34	INPUT LO	Differential Input Low Side			
35	INPUT HI	Differential Input High Side			
36	REF IN +	Differential Reference Input Positive			
37	REF CAP +	Reference Capacitor Positive			
38	REF CAP –	Reference Capacitor Negative			
39	REF IN –	Differential Reference Input Negative			
40	V^+	Positive Supply Voltage - Nominally +5V with respect to GND (Pin 1).			

Note: All digital levels are positive true.

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent circuit of the Analog Section of the ICL7109. When the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V^+, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 3. They are (1) Auto-Zero (AZ), (2) Signal Integrate (INT) and (3) Deintegrate (DE).

1. **Auto-Zero Phase**

During auto-zero three things happen. First, input high and low are disconnected from their pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. **Signal Integrate Phase**

During signal integrate the auto-zero loop is opened, the internal short is removed and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time of 2048 clock periods. Note that this differential voltage can be within the common mode range of the inputs. At the end of this phase, the polarity of the integrated signal is determined.

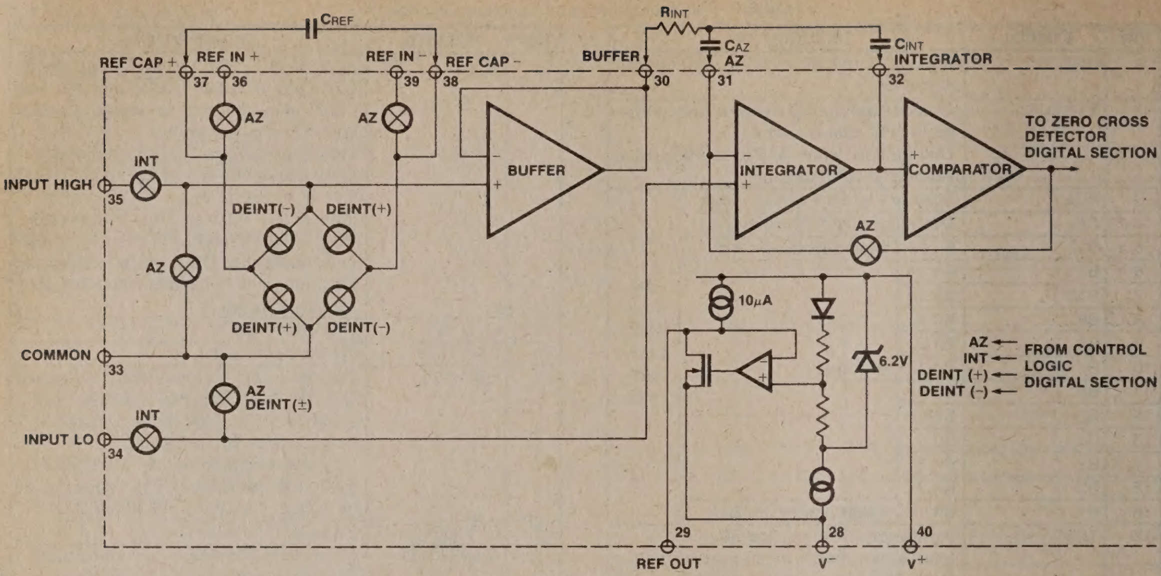

CREF
RINT
CAZ
CINT
REF CAP +
REF IN +
REF IN −
REF CAP −
BUFFER
AZ
INTEGRATOR
37
36
39
38
30
31
32
AZ
AZ
BUFFER
INTEGRATOR
COMPARATOR
TO ZERO CROSS DETECTOR DIGITAL SECTION
INT
INPUT HIGH
35
DEINT(−)
DEINT(+)
AZ
DEINT(+)
DEINT(−)
COMMON
33
AZ DEINT(±)
INT
INPUT LO
34
AZ
10μA
6.2V
AZ
INT
DEINT (+)
DEINT (−)
FROM CONTROL LOGIC DIGITAL SECTION
29
28
40
REF OUT
V−
V+

Figure 2: Analog Section

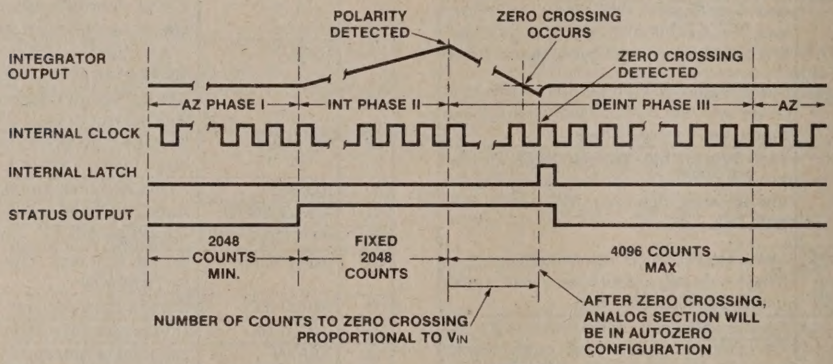

POLARITY DETECTED
ZERO CROSSING OCCURS
INTEGRATOR OUTPUT
ZERO CROSSING DETECTED
AZ PHASE I
INT PHASE II
DEINT PHASE III
AZ
INTERNAL CLOCK
INTERNAL LATCH
STATUS OUTPUT
2048 COUNTS MIN.
FIXED 2048 COUNTS
4096 COUNTS MAX
NUMBER OF COUNTS TO ZERO CROSSING PROPORTIONAL TO VIN
AFTER ZERO CROSSING, ANALOG SECTION WILL BE IN AUTOZERO CONFIGURATION

Figure 3: Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

3. **De-integrate Phase**

   The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero crossing (established in Auto Zero) with a fixed slope. Thus the time for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.5 volts above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

The ICL7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and −5V, this allows a 4V full scale integrator swing positive or negative maximizing the performance of the analog section.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection below).

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog COMMON.

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, supplies of ±6V may be used.

1. **Integrating Resistor**

   Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.096 volt full scale, 200kΩ is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, R_{INT} should be chosen by the relation

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

2. **Integrating Capacitor**

   The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3 volt from either supply). For the ICL7109 with ±5 volt supplies and analog common connected to GND, a ±3.5 to ±4 volt integrator output swing is nominal. For 7-1/2 conversions per second (61.72KHz clock frequency) as provided by the crystal oscillator, nominal values for C_{INT} and C_{AZ} are 0.15μF and 0.33μF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output voltage swing. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{(2048 \times \text{clock period})\ (20\mu A)}{\text{integrator output voltage swing}}$$

   An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. For the military temperature range, Teflon® capacitors are recommended. While their dielectric absorption characteristics vary somewhat from unit to unit, selected devices should give less than 0.5 count of error due to dielectric absorption.

3. **Auto-Zero Capacitor**

   The size of the auto-zero capacitor has some influence on the noise of the system; a big capacitor, giving less noise. However, it cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and more important the error that exists at the end of an auto-zero cycle. For 409.6mv full scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended.

   For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction. Teflon®, or equivalent, capacitors are recommended above 85°C for their low leakage characteristics.

4. **Reference Capacitor**

   A 1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the reference low is not at analog common) and a 409.6mV scale is used, a larger value is required to prevent roll-over error. Generally 10μF will hold the roll-over error to 0.5 count in this instance. Again, Teflon®, or equivalent capacitors should be used for temperatures above 85°C for their low leakage characteristics.

5. **Reference Voltage**

   The analog input required to generate a full scale output of 4096 counts is $V_{IN} = 2V_{REF}$. Thus for a normalized scale, a reference of 2.048V should be used for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are 34k and 0.15μF. This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

6. **Reference Sources**

   The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error.

For this reason, it is recommended that an external high-quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10μA. The output voltage is nominally 2.8V below V+, and has a temperature coefficient of ±80ppm/°C typ. When using the onboard reference, REF OUT (Pin 29) should be connected to REF− (pin 39), and REF+ should be connected to the wiper of a precision potentiometer between REF OUT and V+. The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048mV reference, the fixed resistor should be removed, and a 25kΩ precision potentiometer between REF OUT and V+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink enough current to destroy the device. This can be avoided by placing a 1kΩ resistor in series with pin 39.

DETAILED DESCRIPTION

Digital Selection

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic, and UART handshake logic, as shown in the Block Diagram, Figure 4.

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in Table 1 "Operating Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V+ (high). Inputs driven from TTL gates should have 3-5kΩ pull-up resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is low or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/$\overline{\text{HOLD}}$ Input

When the RUN/$\overline{\text{HOLD}}$ input is high, or left open, the circuit will continuously perform conversion cycles, updating the output latches after zero crossing during the Deintegrate (Phase III) portion of the conversion cycle (See Figure 3). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

If RUN/$\overline{\text{HOLD}}$ goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If RUN/$\overline{\text{HOLD}}$ stays or goes low, the converter will ensure minimum Auto-Zero time, and then wait in Auto-Zero until the RUN/$\overline{\text{HOLD}}$ input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at RUN/$\overline{\text{HOLD}}$. See Figure 5 for details.

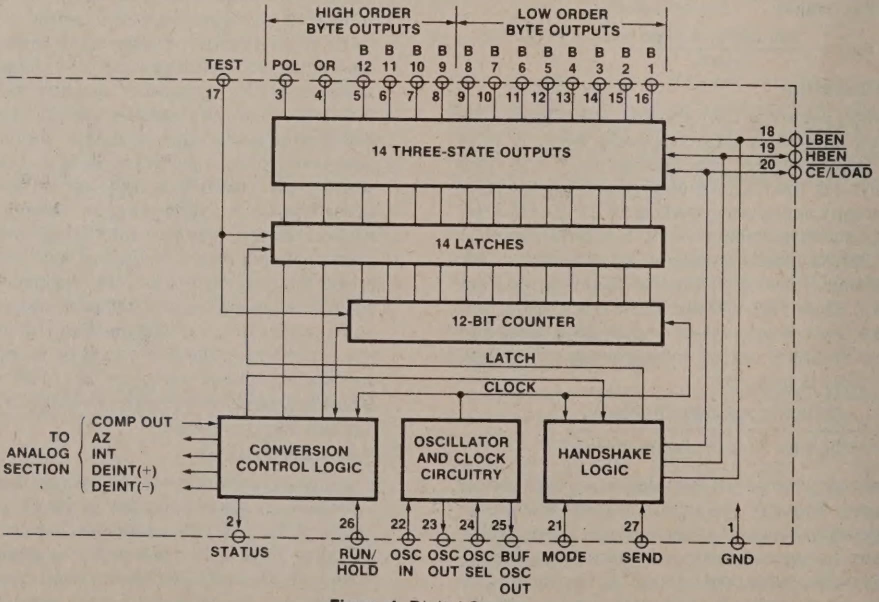

HIGH ORDER BYTE OUTPUTS
LOW ORDER BYTE OUTPUTS
TEST
POL
OR
B 12
B 11
B 10
B 9
B 8
B 7
B 6
B 5
B 4
B 3
B 2
B 1
17
3
4
5
6
7
8
9
10
11
12
13
14
15
16
14 THREE-STATE OUTPUTS
18
19
20
$\overline{\text{LBEN}}$
$\overline{\text{HBEN}}$
$\overline{\text{CE}}$/LOAD
14 LATCHES
12-BIT COUNTER
LATCH
CLOCK
TO ANALOG SECTION
COMP OUT
AZ
INT
DEINT(+)
DEINT(−)
CONVERSION CONTROL LOGIC
OSCILLATOR AND CLOCK CIRCUITRY
HANDSHAKE LOGIC
2
26
22
23
24
25
21
27
1
STATUS
RUN/$\overline{\text{HOLD}}$
OSC IN
OSC OUT
OSC SEL
BUF OSC OUT
MODE
SEND
GND

Figure 4: Digital Section

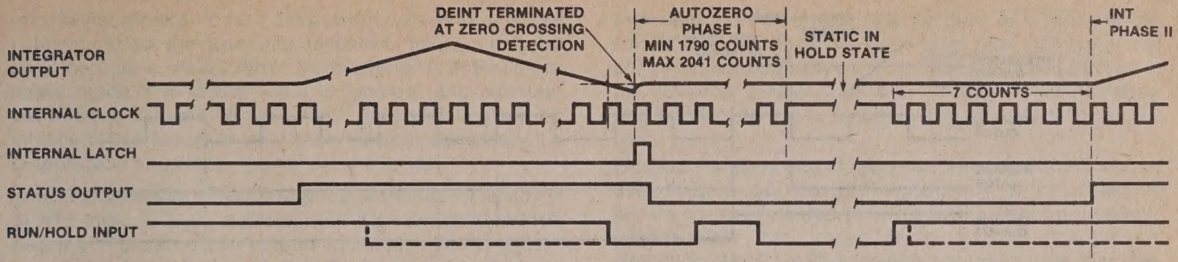


Figure 5: Run/$\overline{\text{Hold}}$ Operation

Using the RUN/$\overline{\text{HOLD}}$ input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in auto-zero with RUN/$\overline{\text{HOLD}}$ low. When RUN/$\overline{\text{HOLD}}$ goes high the conversion is started, and when the STATUS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). RUN/$\overline{\text{HOLD}}$ may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion.

Alternately, RUN/$\overline{\text{HOLD}}$ can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the Buffered Oscillator Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A032 for a discussion of the effects this will have on Auto-Zero performance.

If the RUN/$\overline{\text{HOLD}}$ input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for RUN/$\overline{\text{HOLD}}$ to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and over-range high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in the section entitled "Interfacing." The timing requirements for these outputs are shown in Figure 6 and Table 3.

Table 3 - Direct Mode Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{BEA}	Byte Enable Width	350	220		ns
t_{DAB}	Data Access Time from Byte Enable		210	350	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	400	260		ns
t_{DAC}	Data Access Time from Chip Enable		260	400	ns
t_{DHC}	Data Hold Time from Chip Enable		240	400	ns

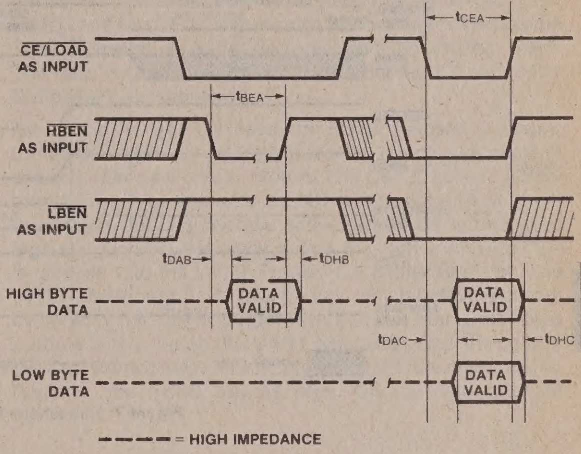


Figure 6: Direct Mode Output Timing

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7109 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is specifically designed to allow a direct interface between the ICL7109 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7109 provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, the ICL7109 will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed (See Figures 7 and 8). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry

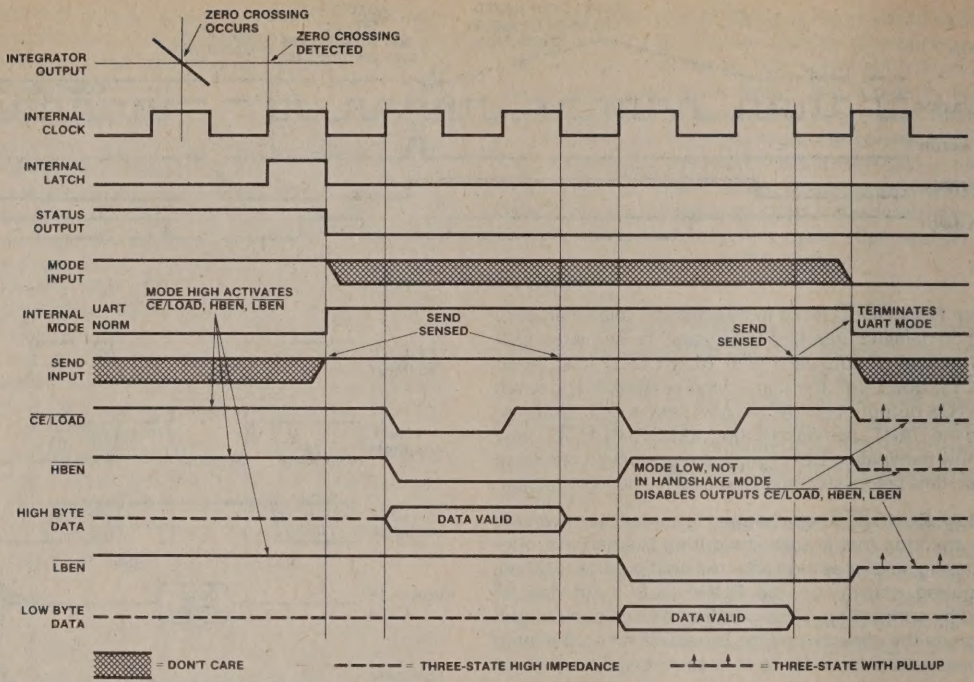

ZERO CROSSING OCCURS
ZERO CROSSING DETECTED
INTEGRATOR OUTPUT
INTERNAL CLOCK
INTERNAL LATCH
STATUS OUTPUT
MODE INPUT
MODE HIGH ACTIVATES CE/LOAD, HBEN, LBEN
INTERNAL MODE
UART
NORM
SEND SENSED
SEND SENSED
TERMINATES UART MODE
SEND INPUT
CE/LOAD
HBEN
MODE LOW, NOT IN HANDSHAKE MODE DISABLES OUTPUTS CE/LOAD, HBEN, LBEN
HIGH BYTE DATA
DATA VALID
LBEN
LOW BYTE DATA
DATA VALID
= DON'T CARE
= THREE-STATE HIGH IMPEDANCE
= THREE-STATE WITH PULLUP

Figure 7: Handshake With Send Held Positive

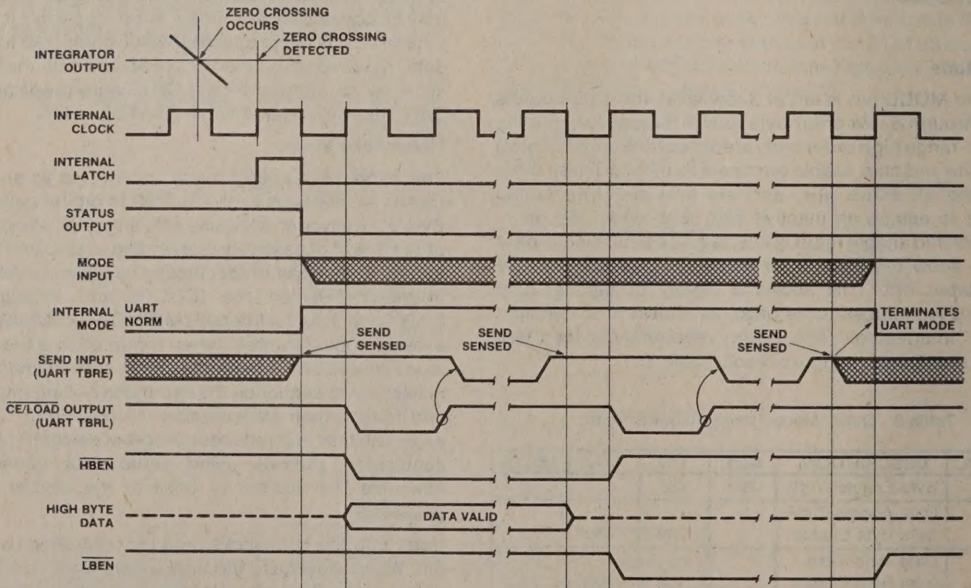

ZERO CROSSING OCCURS
ZERO CROSSING DETECTED
INTEGRATOR OUTPUT
INTERNAL CLOCK
INTERNAL LATCH
STATUS OUTPUT
MODE INPUT
INTERNAL MODE
UART
NORM
SEND SENSED
SEND SENSED
SEND SENSED
TERMINATES UART MODE
SEND INPUT (UART TBRE)
CE/LOAD OUTPUT (UART TBRL)
HBEN
HIGH BYTE DATA
DATA VALID
LBEN
LOW BYTE DATA
DATA VALID
= DON'T CARE
= THREE-STATE HIGH IMPEDANCE

Figure 8: Handshake - Typical UART Interface Timing

into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (See Figure 9) until the converter completes the output cycle and clears the handshake mode.

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte enable terminals become TTL-compatible outputs which provide the control signals for the output cycle (See Figures 7, 8, and 9).

In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

Figure 7 shows the sequence of the output cycle with SEND held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the CE/LOAD, LBEN and HBEN terminals are active as outputs). The high level at the SEND input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the CE/LOAD and the HBEN outputs assume a low level, and the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled. The CE/LOAD output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte enable remains low for two clock periods. Thus the CE/LOAD output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using CE/LOAD and LBEN while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

Figure 8 shows an output sequence where the SEND input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ICL7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the CE/LOAD terminal of the ICL7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The CE/LOAD and HBEN terminals will go low after SEND is sensed, and the high order byte outputs become active. When CE/LOAD goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the HBEN output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7109

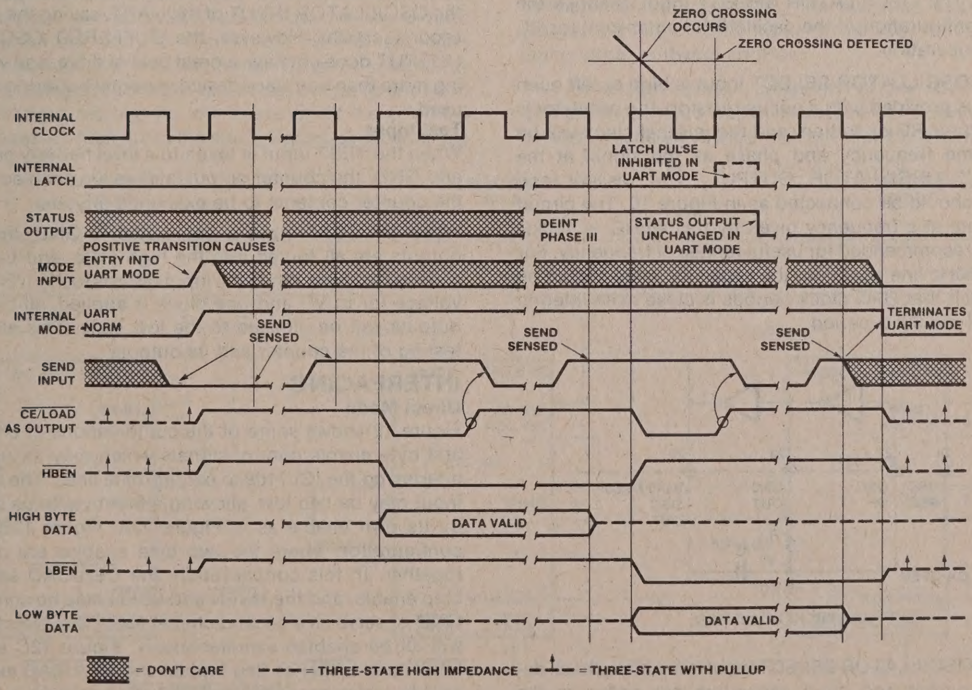

ZERO CROSSING OCCURS
ZERO CROSSING DETECTED
INTERNAL CLOCK
INTERNAL LATCH
LATCH PULSE INHIBITED IN UART MODE
STATUS OUTPUT
DEINT PHASE III
STATUS OUTPUT UNCHANGED IN UART MODE
POSITIVE TRANSITION CAUSES ENTRY INTO UART MODE
MODE INPUT
INTERNAL MODE
UART
NORM
SEND SENSED
SEND SENSED
SEND SENSED
TERMINATES UART MODE
SEND INPUT
CE/LOAD AS OUTPUT
HBEN
HIGH BYTE DATA
DATA VALID
LBEN
LOW BYTE DATA
DATA VALID
▨ = DON'T CARE
— — — = THREE-STATE HIGH IMPEDANCE
—⊥— = THREE-STATE WITH PULLUP

Figure 9: Handshake Triggered By Mode

internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{\text{HBEN}}$ output returns high. At the same time, the $\overline{\text{CE/LOAD}}$ and $\overline{\text{LBEN}}$ outputs go low, and the low order byte outputs become active. Similarly, when the $\overline{\text{CE/LOAD}}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the $\overline{\text{CE/LOAD}}$, $\overline{\text{HBEN}}$, and $\overline{\text{LBEN}}$ terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 9 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/$\overline{\text{HOLD}}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Oscillator

The ICL7109 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

When the OSCILLATOR SELECT input is high or left open (the input is provided with a pullup resistor), the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Figure 10. The circuit will oscillate at a frequency given by f = .45/RC. A 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 2048 clock periods is close to an integral multiple of the 60Hz period.

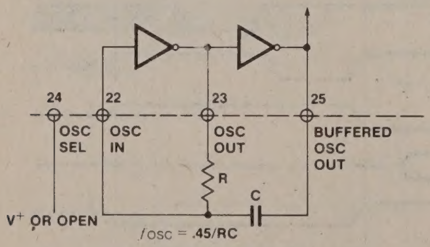


Figure 10: RC Oscillator

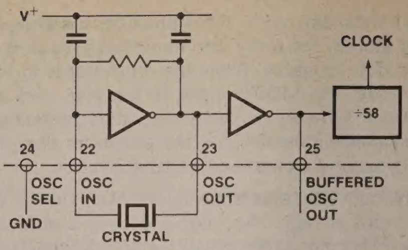


Figure 11: Crystal Oscillator

When the OSCILLATOR SELECT input is low a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Figure 11, the oscillator will operate with most crystals in the 1 to 5MHz range with no external components. Taking the OSCILLATOR SELECT input low also inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. Using an inexpensive 3.58MHz TV crystal, this division ratio provides an integration time given by:

$$T = (2048 \text{ clock periods}) \times \left(\frac{58}{3.58\text{MHz}}\right) = 33.18\text{ms}$$

This time is very close to two 60Hz periods or 33.33ms. The error is less than one percent, which will give better than 40dB 60Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8kHz.

If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle, and phase as the input signal when OSCILLATOR SELECT is left open. When OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ICL7109 with the IM6403 UART, it is possible to use one 3.58MHz crystal for both devices. The BUFFERED OSCILLATOR OUTPUT of the ICL7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive, and when driving more than one slave device, external buffering should be used.

Test Input

When the TEST input is taken to a level halfway between V^+ and GND, the counter output latches are enabled, allowing the counter contents to be examined anytime.

When the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the input returns to the 1/2 $(V^+ - \text{GND})$ voltage (or to V^+) and one clock is applied, all the counter outputs will be clocked to the low state. This allows easy testing of the counter and its outputs.

INTERFACING

Direct Mode

Figure 12 shows some of the combinations of chip enable and byte enable control signals which may be used when interfacing the ICL7109 to parallel data lines. The $\overline{\text{CE/LOAD}}$ input may be tied low, allowing either byte to be controlled by its own enable as in Figure 12A. Figure 12B shows a configuration where the two byte enables are connected together. In this configuration, the $\overline{\text{CE/LOAD}}$ serves as a chip enable, and the $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ may be connected to GND or serve as a second chip enable. The 14 data outputs will all be enabled simultaneously. Figure 12C shows the $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ as flag inputs, and $\overline{\text{CE/LOAD}}$ as a master enable, which could be the READ strobe available from most microprocessors.

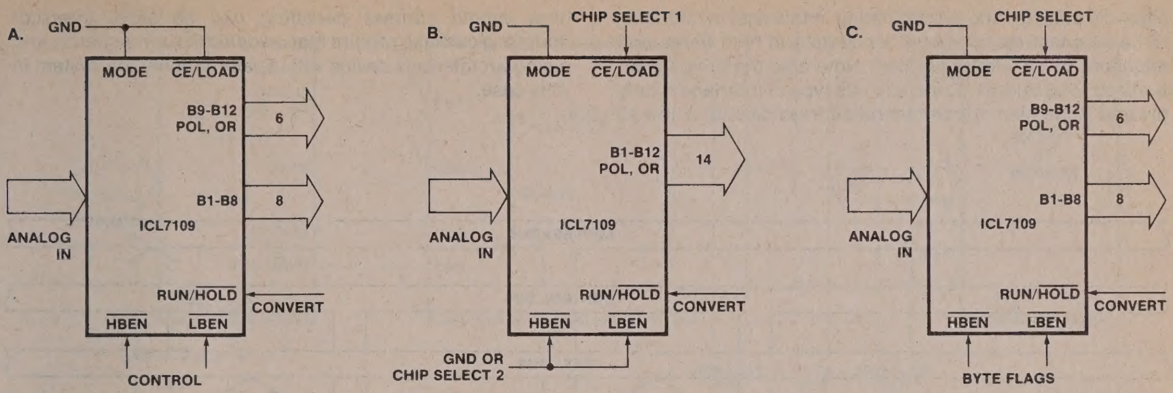

A.
GND
MODE
$\overline{\text{CE}}$/LOAD
B9-B12
POL, OR
6
B1-B8
8
ICL7109
ANALOG IN
RUN/$\overline{\text{HOLD}}$
CONVERT
$\overline{\text{HBEN}}$
$\overline{\text{LBEN}}$
CONTROL
B.
GND
CHIP SELECT 1
MODE
$\overline{\text{CE}}$/LOAD
B1-B12
POL, OR
14
ICL7109
ANALOG IN
RUN/$\overline{\text{HOLD}}$
CONVERT
$\overline{\text{HBEN}}$
$\overline{\text{LBEN}}$
GND OR
CHIP SELECT 2
C.
GND
CHIP SELECT
MODE
$\overline{\text{CE}}$/LOAD
B9-B12
POL, OR
6
B1-B8
8
ICL7109
ANALOG IN
RUN/$\overline{\text{HOLD}}$
CONVERT
$\overline{\text{HBEN}}$
$\overline{\text{LBEN}}$
BYTE FLAGS

Figure 12: Direct Mode Chip and Byte Enable Combinations

Figure 13 shows an approach to interfacing several ICL7109s to a bus, ganging the $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ signals to several converters together, and using the $\overline{\text{CE}}$/LOAD inputs (perhaps decoded from an address) to select the desired converter.

Some practical circuits utilizing the parallel three-state output capabilities of the ICL7109 are shown in Figures 14 through 19. Figure 14 shows a straightforward application to the Intel MCS-48, -80 and -85 systems via an 8255PPI, where the ICL7109 data outputs are active at all times. The I/O ports of an 8155 may be used in the same way. This interface can be used in a read-anytime mode, although a read performed while the data latches are being updated will lead to scrambled data. This will occur very rarely, in the proportion of setup-skew times to conversion time. One way to overcome this is to read the STATUS output as well, and if it is high, read the data again after a delay of more than 1/2 converter clock period. If STATUS is now low, the second reading is correct, and if it is still high, the first reading is correct. Alternatively, this timing problem is completely avoided by using a read-after-update sequence, as shown in Figure 15. Here the high to low transition of the STATUS output drives an interrupt to the microprocessor causing it to access the data. This application also shows the RUN/$\overline{\text{HOLD}}$ input being used to initiate conversions under software control.

A similar interface to Motorola MC6800 or MOS Technology MCS650X systems is shown in Figure 16. The high to low transition of the STATUS output generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the RUN/$\overline{\text{HOLD}}$ pin through Control Register B, allowing software-controlled initiation of conversions in this system also.

Figure 17 shows an interface to the Intersil IM6100 CMOS microprocessor family using the IM6101 PIE to control the data transfers. Here the data is read by the microprocessor in an 8-bit and a 6-bit word, directly from the ICL7109 to the microprocessor data bus. Again, the high to low transition of the STATUS output generates an interrupt leading to a software routine controlling the two read operations. As before, the RUN/$\overline{\text{HOLD}}$ input to the ICL7109 is shown as being under software control.

The three-state output capability of the ICL7109 allows direct interfacing to most microprocessor busses. Examples of this are shown in Figures 1, 18 and 19. It is necessary to

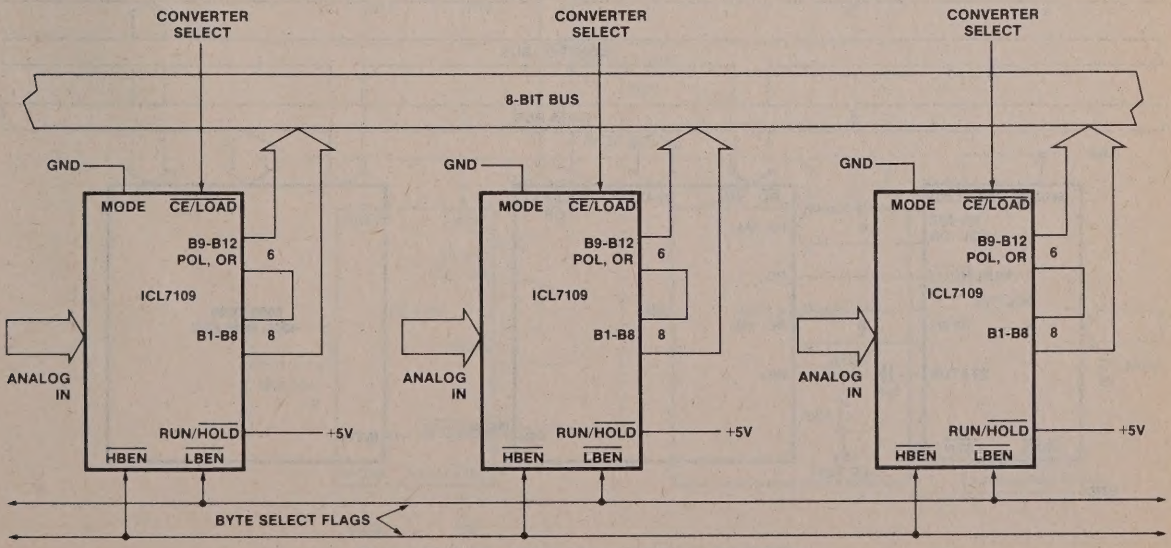

CONVERTER SELECT
CONVERTER SELECT
CONVERTER SELECT
8-BIT BUS
GND
MODE
$\overline{\text{CE}}$/LOAD
B9-B12
POL, OR
6
ICL7109
B1-B8
8
ANALOG IN
RUN/$\overline{\text{HOLD}}$
+5V
$\overline{\text{HBEN}}$
$\overline{\text{LBEN}}$
GND
MODE
$\overline{\text{CE}}$/LOAD
B9-B12
POL, OR
6
ICL7109
B1-B8
8
ANALOG IN
RUN/$\overline{\text{HOLD}}$
+5V
$\overline{\text{HBEN}}$
$\overline{\text{LBEN}}$
GND
MODE
$\overline{\text{CE}}$/LOAD
B9-B12
POL, OR
6
ICL7109
B1-B8
8
ANALOG IN
RUN/$\overline{\text{HOLD}}$
+5V
$\overline{\text{HBEN}}$
$\overline{\text{LBEN}}$
BYTE SELECT FLAGS

Figure 13: Three-stating Several 7109's to a Small Bus

carefully consider the system timing in this type of interface, to be sure that requirements for setup and hold times, and minimum pulse widths are met. Note also the drive limitations on long busses. Generally this type of interface is only favored if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can also require many additional components, and using an interface device will usually simplify the system in this case.

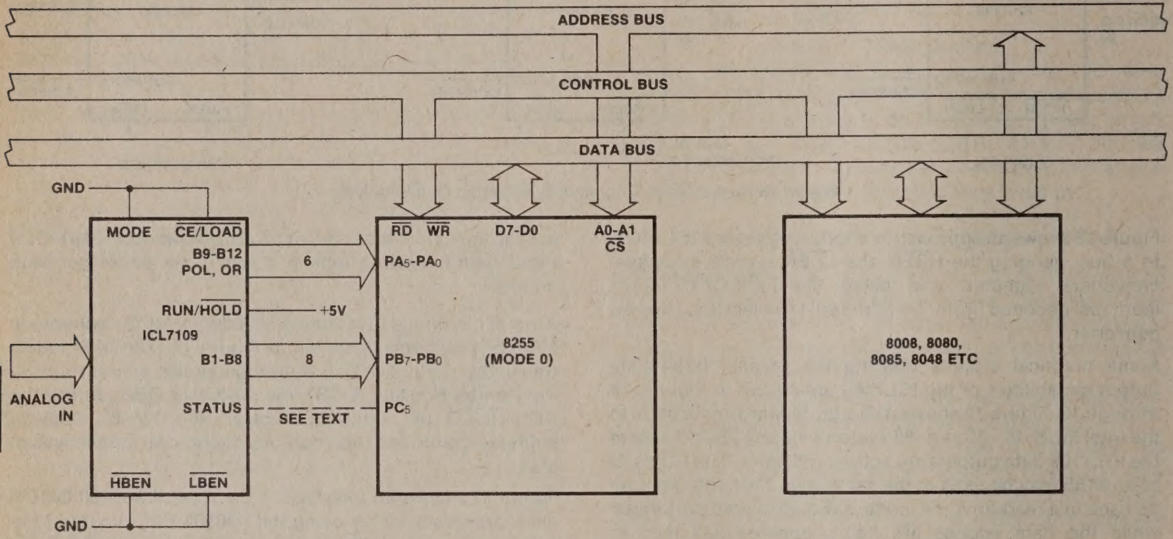

ADDRESS BUS
CONTROL BUS
DATA BUS
GND
MODE
CE/LOAD
B9-B12
POL, OR
6
RUN/HOLD
+5V
ICL7109
B1-B8
8
ANALOG IN
STATUS
SEE TEXT
HBEN
LBEN
GND
RD
WR
D7-D0
A0-A1
CS
PA5-PA0
8255 (MODE 0)
PB7-PB0
PC5
8008, 8080, 8085, 8048 ETC

Figure 14: Full-time Parallel Interface to MCS-48, -80, -85 Microcomputer Systems

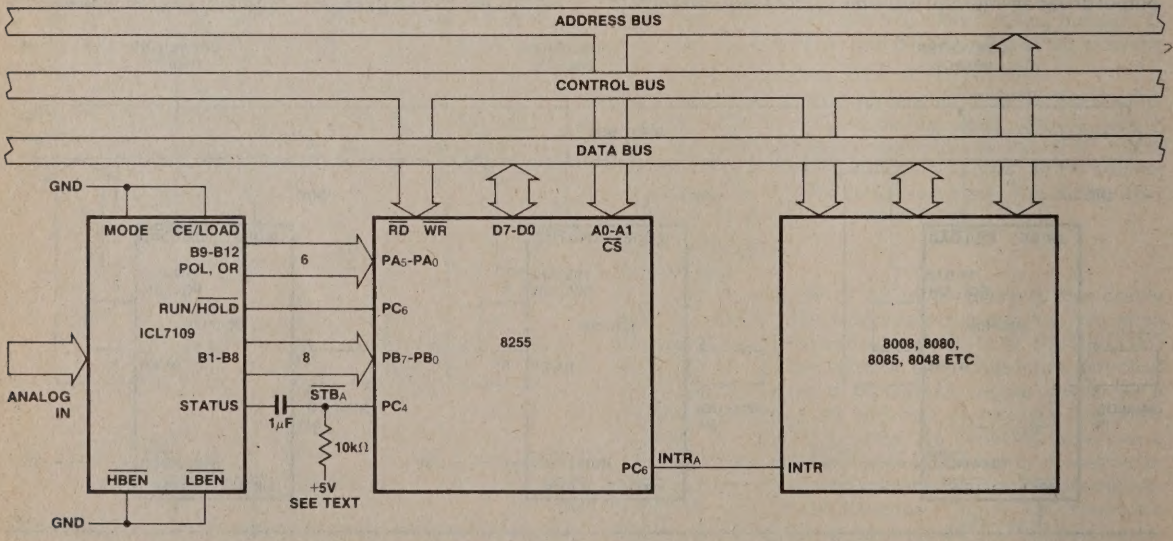

ADDRESS BUS
CONTROL BUS
DATA BUS
GND
MODE
CE/LOAD
B9-B12
POL, OR
6
RUN/HOLD
ICL7109
B1-B8
8
ANALOG IN
STATUS
1μF
STBA
10kΩ
+5V
SEE TEXT
HBEN
LBEN
GND
RD
WR
D7-D0
A0-A1
CS
PA5-PA0
PC6
8255
PB7-PB0
PC4
PC6
INTRA
INTR
8008, 8080, 8085, 8048 ETC

Figure 15: Full-time Parallel Interface to MCS-48, -80, -85 Microcomputers With Interrupt

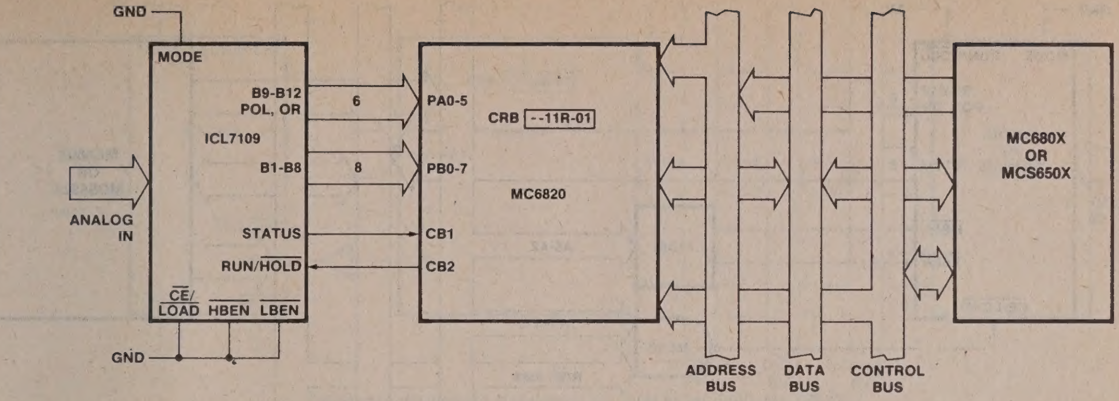

GND
MODE
B9-B12
POL, OR
6
PA0-5
CRB --11R-01
ICL7109
B1-B8
8
PB0-7
MC6820
ANALOG IN
STATUS
CB1
RUN/$\overline{\text{HOLD}}$
CB2
$\overline{\text{CE}}$/$\overline{\text{LOAD}}$
$\overline{\text{HBEN}}$
$\overline{\text{LBEN}}$
GND
MC680X OR MCS650X
ADDRESS BUS
DATA BUS
CONTROL BUS

Figure 16: Full-time Parallel Interface to MC680X or MCS650X Microprocessors

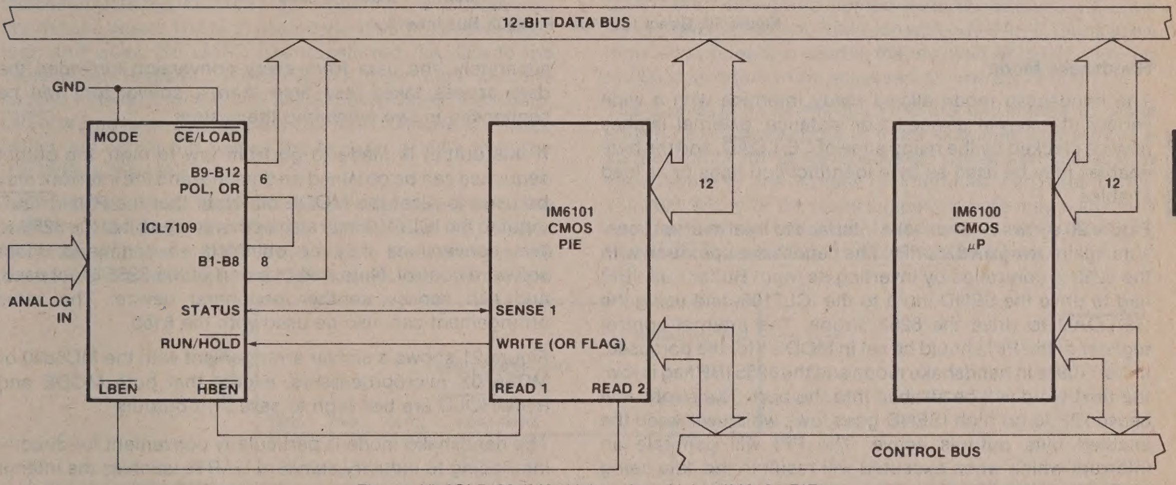

12-BIT DATA BUS
GND
MODE
$\overline{\text{CE}}$/LOAD
B9-B12
POL, OR
6
ICL7109
B1-B8
8
ANALOG IN
STATUS
RUN/$\overline{\text{HOLD}}$
$\overline{\text{LBEN}}$
$\overline{\text{HBEN}}$
IM6101 CMOS PIE
SENSE 1
WRITE (OR FLAG)
READ 1
READ 2
12
IM6100 CMOS μP
12
CONTROL BUS

Figure 17: ICL7109-IM6100 Interface Using IM6101 PIE

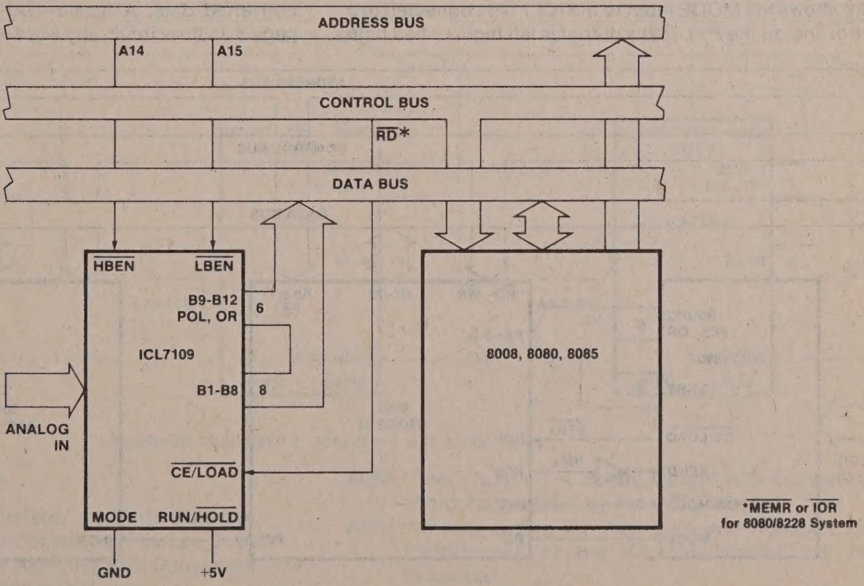

ADDRESS BUS
A14
A15
CONTROL BUS
$\overline{\text{RD}}$*
DATA BUS
$\overline{\text{HBEN}}$
$\overline{\text{LBEN}}$
B9-B12
POL, OR
6
ICL7109
B1-B8
8
ANALOG IN
$\overline{\text{CE}}$/$\overline{\text{LOAD}}$
MODE
RUN/$\overline{\text{HOLD}}$
GND
+5V
8008, 8080, 8085
*$\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ for 8080/8228 System

Figure 18: Direct Interface - ICL7109 to 8080/8085

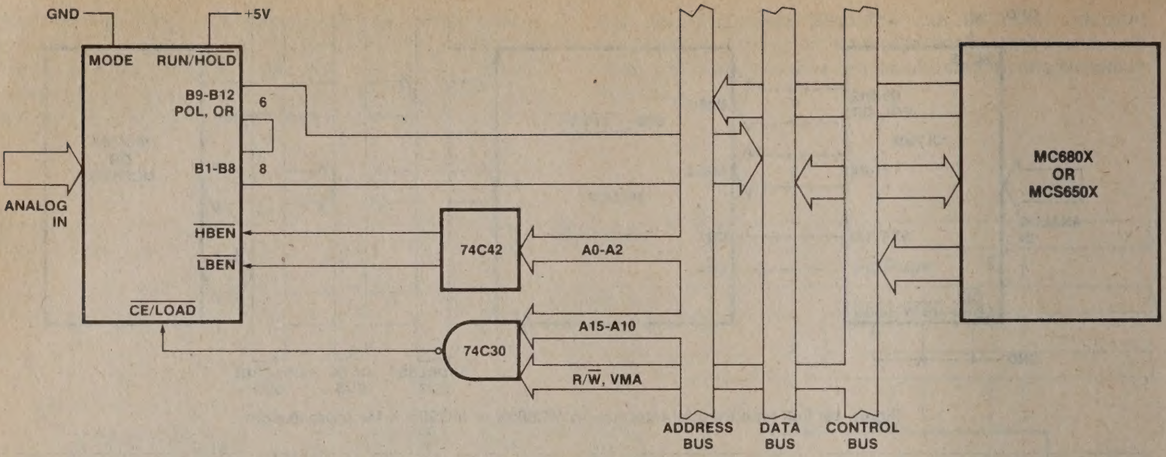

GND
+5V
MODE
RUN/$\overline{HOLD}$
B9-B12
POL, OR
6
B1-B8
8
ANALOG IN
$\overline{HBEN}$
$\overline{LBEN}$
$\overline{CE}$/LOAD
74C42
A0-A2
74C30
A15-A10
R/$\overline{W}$, VMA
ADDRESS BUS
DATA BUS
CONTROL BUS
MC680X OR MCS650X

Figure 19: Direct ICL7109 - MC680X Bus Interface

Handshake Mode

The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by the rising edge of $\overline{CE}/\overline{LOAD}$, and the byte enables may be used as byte identification flags or as load enables.

Figure 20 shows a handshake interface to Intel microprocessors again using an 8255PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ICL7109, and using the $\overline{CE}/\overline{LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. When the byte is read, the IBF will be reset low, which causes the ICL7109 to sequence into the next byte. This figure shows the MODE input to the ICL7109 connected to a control line on the PPI. If this output is left high, or tied high separately, the data from every conversion (provided the data access takes less time than a conversion) will be sequenced in two bytes into the system.

If this output is made to go from low to high, the output sequence can be obtained on demand, and the interrupt may be used to reset the MODE bit. Note that the RUN/$\overline{HOLD}$ input to the ICL7109 may also be driven by a bit of the 8255 so that conversions may be obtained on command under software control. Note that one port of the 8255 is not used, and can service another peripheral device. The same arrangement can also be used with the 8155.

Figure 21 shows a similar arrangement with the MC6800 or MCS650X microprocessors, except that both MODE and RUN/$\overline{HOLD}$ are tied high to save port outputs.

The handshake mode is particularly convenient for directly interfacing to industry standard UARTs (such as the Intersil IM6402/6403 or Western Digital TR1602) providing a minimum component count means of serially transmitting converted data. A typical UART connection is shown on page 3. In this circuit, any word received by the UART causes

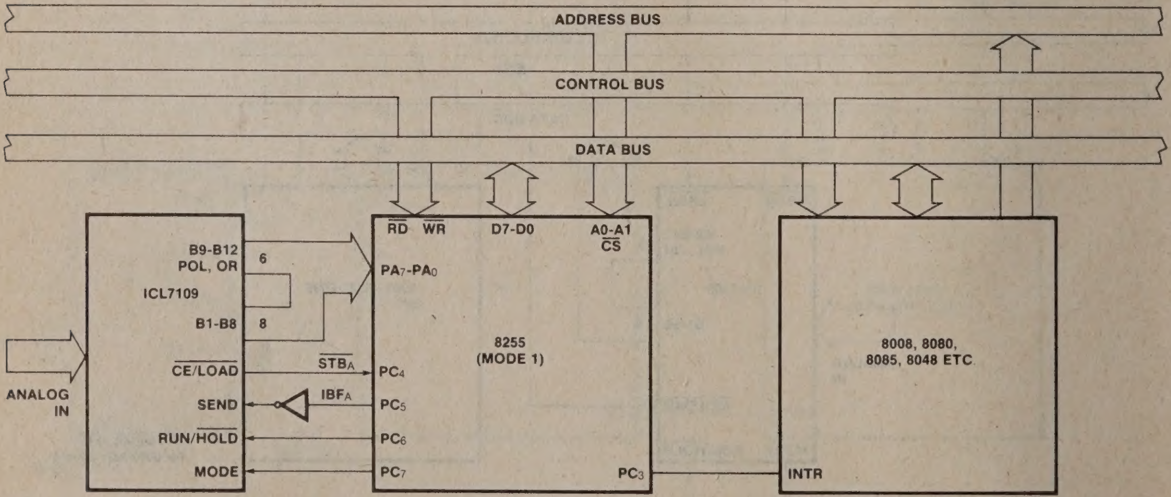

ADDRESS BUS
CONTROL BUS
DATA BUS
B9-B12
POL, OR
6
ICL7109
B1-B8
8
ANALOG IN
$\overline{CE}$/LOAD
SEND
RUN/$\overline{HOLD}$
MODE
$\overline{STB_A}$
IBF_A
$\overline{RD}$
$\overline{WR}$
D7-D0
A0-A1
$\overline{CS}$
PA_7-PA_0
8255 (MODE 1)
PC_4
PC_5
PC_6
PC_7
PC_3
INTR
8008, 8080, 8085, 8048 ETC.

Figure 20: Handshake Interface - ICL7109 to MCS-48, -80, 85

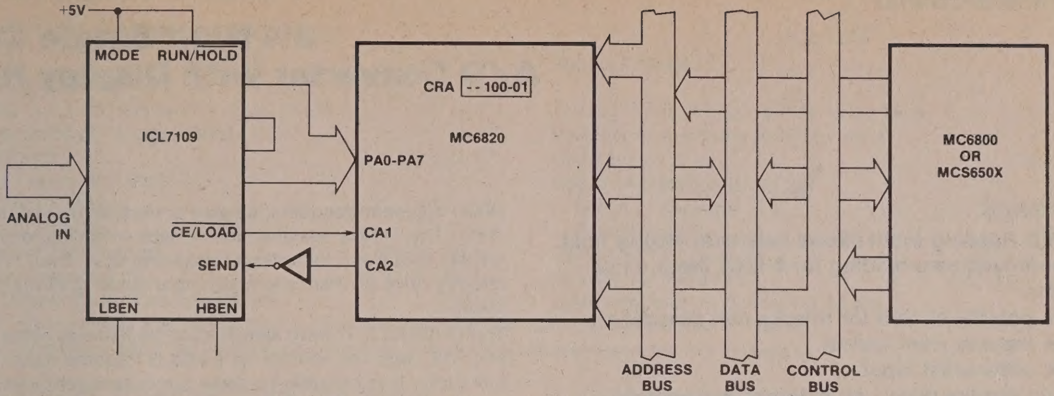

+5V
MODE
RUN/HOLD
ICL7109
ANALOG IN
CE/LOAD
SEND
LBEN
HBEN
CRA
-- 100-01
MC6820
PA0-PA7
CA1
CA2
ADDRESS BUS
DATA BUS
CONTROL BUS
MC6800 OR MCS650X

Figure 21: Handshake Interface - ICL7109 to MC6800, MCS650X

the UART DR (Data Ready) output to go high. This drives the MODE input to the ICL7109 high, triggering the ICL7109 into handshake mode. The high order byte is output to the UART first, and when the UART has transferred the data to the Transmitter Register, TBRE (SEND) goes high and the second byte is output. When TBRE (SEND) goes high again, $\overline{\text{LBEN}}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the ICL7109 to the UART.

Figure 22 shows an extension of the one converter - one UART scheme of the Typical Connection to several ICL7109s with one UART. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. With no external components, this scheme will allow up to eight ICL7109s to interface with one UART. Using a few more components to decode the received word will allow up to 256 converters to be accessed on one serial line.

The applications of the ICL7109 are not limited to those shown here. The purpose of these examples is to provide a starting point for users to develop useful systems, and to show some of the variety of interfaces and uses of the ICL7109. Many of the ideas suggested here may be used in combination; in particular the uses of the STATUS, RUN/$\overline{\text{HOLD}}$, and MODE signals may be mixed.

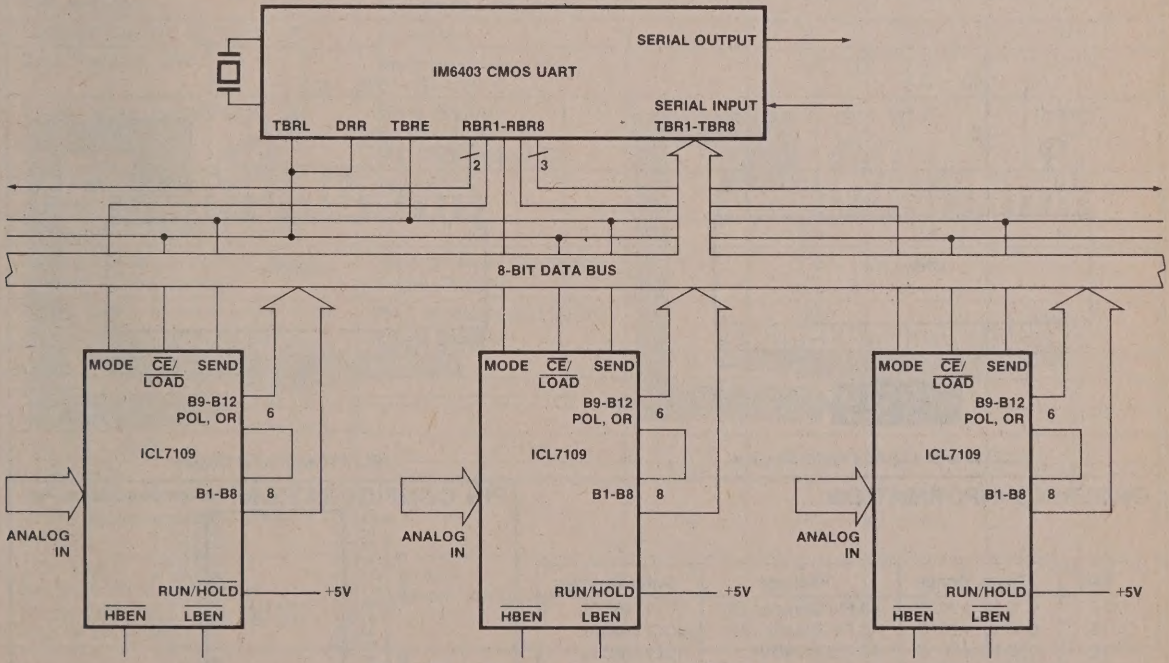

IM6403 CMOS UART
SERIAL OUTPUT
SERIAL INPUT
TBRL
DRR
TBRE
RBR1-RBR8
TBR1-TBR8
2
3
8-BIT DATA BUS
MODE
CE/LOAD
SEND
B9-B12
POL, OR
6
ICL7109
B1-B8
8
ANALOG IN
RUN/HOLD
+5V
HBEN
LBEN

Figure 22: Multiplexing Converters with Mode Input

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar

A017 "The Integrating A/D Converters," by Lee Evans

A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood

A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw

A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family," by Peter Bradshaw

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

ICL7116, 7117

3½ Digit Single Chip A/D Converter with Display Hold

FEATURES

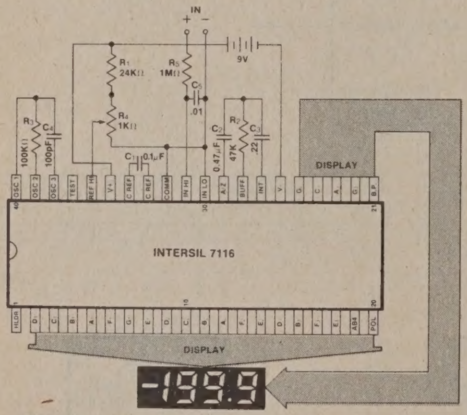
- **HOLD Reading Input allows indefinite display hold**
- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA input current typical.**
- **True differential input**
- **Direct display drive - no external components required. — LCD ICL7116
— LED ICL7117**
- **Low noise - less than 15 μV pk-pk typical.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**

GENERAL DESCRIPTION

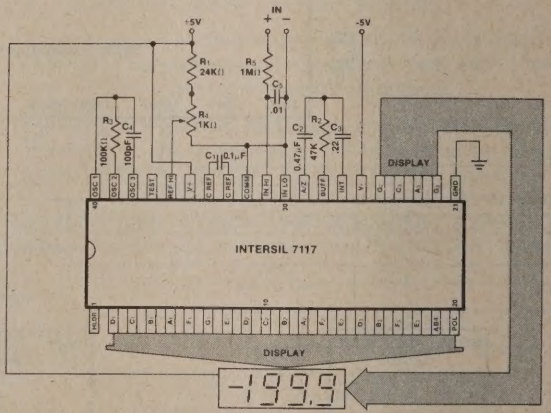
The Intersil ICL7116 and 7117 are high performance, low power 3-1/2 digit A/D converters. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7116 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7117 will directly drive an instrument-size light emitting diode (LED) display.

The 7116 and 7117 have almost all of the features of the 7106 and 7107 with the addition of a HOLD Reading input. With this input, it is possible to make a measurement and then retain the value on the display indefinitely. To make room for this feature the reference input has been referenced to Common rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the 7106 and 7107. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7116), enabling a high performance panel meter to be built with the addition of only seven passive components and a display.

TYPICAL CONNECTION DIAGRAMS


IN
+ −
9V
R1 24KΩ
R5 1MΩ
C5 .01
R4 1KΩ
R3 100KΩ
C4 100pF
C1 0.1μF
C2 0.47μF
R2 47K
C3 .22
OSC 1
OSC 2
OSC 3
TEST
REF HI
V+
C REF
C REF
COMM
IN HI
IN LO
A/Z
BUFF
INT
V-
DISPLAY
B.P.
40
30
21
INTERSIL 7116
1
10
20
HLDR
AB4
POL
DISPLAY
-199.9

ICL7116 with Liquid Crystal Display

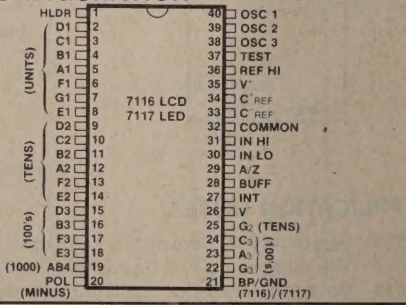

+5V
IN
+ −
-5V
R1 24KΩ
R5 1MΩ
C5 .01
R4 1KΩ
R3 100KΩ
C4 100pF
C1 0.1μF
C2 0.47μF
R2 47K
C3 .22
OSC 1
OSC 2
OSC 3
TEST
REF HI
V+
C REF
C REF
COMM
IN HI
IN LO
A/Z
BUFF
INT
V-
DISPLAY
GND
40
30
21
INTERSIL 7117
1
10
20
HLDR
AB4
POL
DISPLAY
-199.9

ICL7117 with LED Display

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
7116	0°C to +70°C	40-Pin Ceramic DIP	ICL7116CDL
7116	0°C to +70°C	40-Pin Plastic DIP	ICL7116CPL
7116	0°C to +70°C	40 Pin CERDIP	ICL7116CJL
7117	0°C to +70°C	40-Pin Ceramic DIP	ICL7117CDL
7117	0°C to +70°C	40-Pin Plastic DIP	ICL7117CPL
7117	0°C to +70°C	40-Pin CERDIP	ICL7117CJL

PIN CONFIGURATION (Outline dwgs DL,JL,PL)


HLDR 1
D1 2
C1 3
B1 4
A1 5
F1 6
G1 7
E1 8
(UNITS)
D2 9
C2 10
B2 11
A2 12
F2 13
E2 14
(TENS)
D3 15
B3 16
F3 17
E3 18
(100's)
(1000) AB4 19
POL 20
(MINUS)
7116 LCD
7117 LED
40 OSC 1
39 OSC 2
38 OSC 3
37 TEST
36 REF HI
35 V+
34 C+REF
33 C-REF
32 COMMON
31 IN HI
30 IN LO
29 A/Z
28 BUFF
27 INT
26 V-
25 G2 (TENS)
24 C3
23 A3
22 G3
(100's)
21 BP/GND
(7116)/(7117)

ABSOLUTE MAXIMUM RATINGS

ICL7116

Supply Voltage (V^+ to V^-)	15V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	Test to V^+
Power Dissipation (Note 2)	
Ceramic Package	1000 mW
Plastic Package	800 mW
Operating Temperature	0° C to +70° C
Storage Temperature	−65° C to +160° C
Lead Temperature (Soldering, 60 sec)	300° C

ICL7117

Supply Voltage V^+	+6V
V^-	−9V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	Gnd to V^+
Power Dissipation (Note 2)	
Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0° C to +70° C
Storage Temperature	−65° C to +160° C
Lead Temperature (Soldering, 60 sec)	300° C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to $\pm 100\mu A$.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	$V_{IN} = 0.0V$ Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ $V_{REF} = 100mV$	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \cong 200.0mV$	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or Full Scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	$V_{CM} = \pm 1V$, $V_{IN} = 0V$, Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	$V_{IN} = 0V$ Full Scale = 200.0mV		15		μV
Leakage Current @ Input	$V_{IN} = 0V$		1	10	pA
Zero Reading Drift	$V_{IN} = 0$ $0° < T_A < 70°C$		0.2	1	μV/°C
Scale Factor Temperature Coefficient	$V_{IN} = 199.0mV$ $0 < T_A < 70°C$ (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7117)	$V_{IN} = 0$		0.8	1.8	mA
V^- Supply Current (7117 only)			0.6	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25kΩ between COMMON & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25kΩ between COMMON & pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				TEST +1.5	V
V_{IL}, Pin 1 (7117 only)				GND +1.5	V
V_{IH}, Pin 1 (Both)		$V^+ -1.5$			V
7116 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	$V^+ - V^- = 9V$	4 4	5 5	6 6	V
7117 ONLY Segment Sinking Current (Except Pin 19) (Pin 19 only)	$V^+ = 5.0V$ Segment Voltage = 3V	5 10	8.0 16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7116 and 7117 at $T_A = 25°C$, $f_{clock} = 48kHz$. 7116 is tested in the circuit of Figure 1. 7117 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion below.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.

TEST CIRCUITS

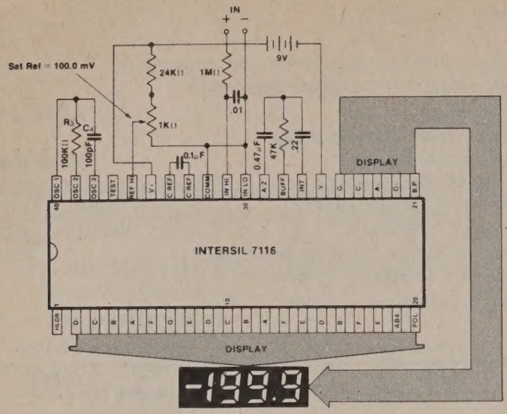

IN
+ −
9V
Set Ref = 100.0 mV
24KΩ
1MΩ
.01
1KΩ
R1
C1
100KΩ
100pF
0.1μF
0.47μF
47K
.22
DISPLAY
OSC 1
OSC 2
OSC 3
TEST
REF HI
V+
C REF
C REF
COMM
IN HI
IN LO
A-Z
BUFF
INT
V-
BP
INTERSIL 7116
HLDR
AB4
POL
DISPLAY
-199.9

Figure 1: 7116

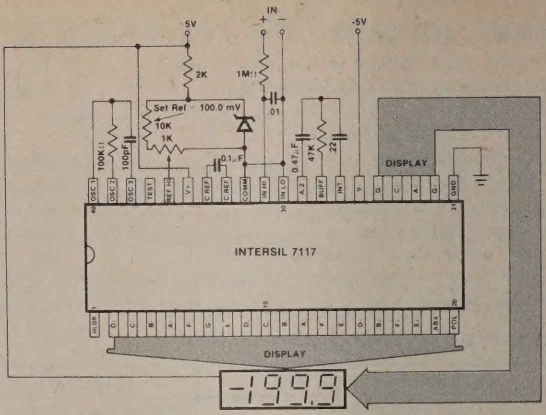

IN
+ −
-5V
-5V
2K
1MΩ
Set Ref = 100.0 mV
10K
1K
.01
100KΩ
100pF
0.1μF
0.47μF
47K
.22
DISPLAY
OSC 1
OSC 2
OSC 3
TEST
REF HI
V+
C REF
C REF
COMM
IN HI
IN LO
A-Z
BUFF
INT
V-
GND
INTERSIL 7117
HLDR
AB4
POL
DISPLAY
-199.9

Figure 2: 7117

DETAILED DESCRIPTION

ANALOG SECTION

4

Figure 3 shows the Block Diagram of the Analog Section for the ICL7116 and 7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) deintegrate (DE).

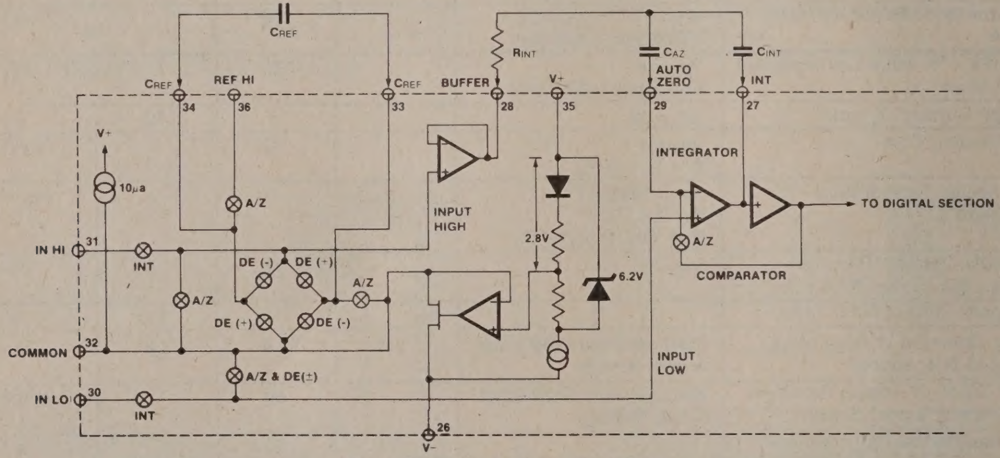

CREF
CREF
REF HI
CREF
BUFFER
RINT
V+
CAZ
AUTO ZERO
CINT
INT
34
36
33
28
35
29
27
INTEGRATOR
V+
10μa
A/Z
INPUT HIGH
TO DIGITAL SECTION
IN HI
31
INT
DE (-)
DE (+)
A/Z
2.8V
A/Z
6.2V
A/Z
COMPARATOR
DE (+)
DE (-)
COMMON
32
INPUT LOW
A/Z & DE(±)
IN LO
30
INT
26
V-

Figure 3: Analog Section of 7116/7117

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $\left(\frac{V_{in}}{V_{ref}}\right)$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

Reference

The reference input must be generated as a positive voltage with respect to COMMON. Note that current flowing in the COMMON pins' internal resistance causes a slight shift in the effective reference voltage, disturbing ratiometric readings at low reference inputs. If possible, do not let this current vary.

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7116) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (.001%/%), low output impedance (≃15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80 μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

Analog COMMON is also the voltage that input low returns to during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter.

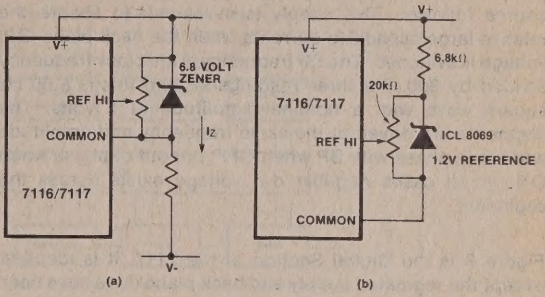


Figure 4: Using an External Reference

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

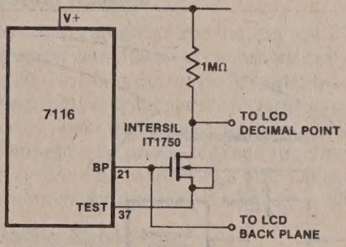


Figure 5: Simple Inverter for Fixed Decimal Point

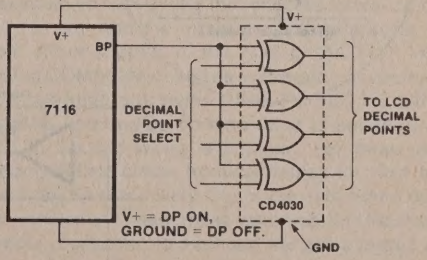


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled to high (to V$^+$) all segments will be turned on and the display should read - 1888. **[Caution: on the 7116, in the lamp test mode, the segments have a constant d-c voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.]**

DIGITAL SECTION

Figures 7 and 8 show the digital section for the 7116 and 7117, respectively. In the 7116, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases neglible d-c voltage exists across the segments.

Figure 8 is the Digital Section of the 7117. It is identical except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16 mA.

In both devices the polarity indicator is ON for negative analog inputs. This can be reversed by simply reversing IN LO and IN HI.

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at a logic "HI". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (7116) or GROUND (7117) to continuously update the display. This input is CMOS compatible, and has a 70k typical resistance to either TEST (7116) or GROUND (7117).

SEGMENT ASSIGNMENT

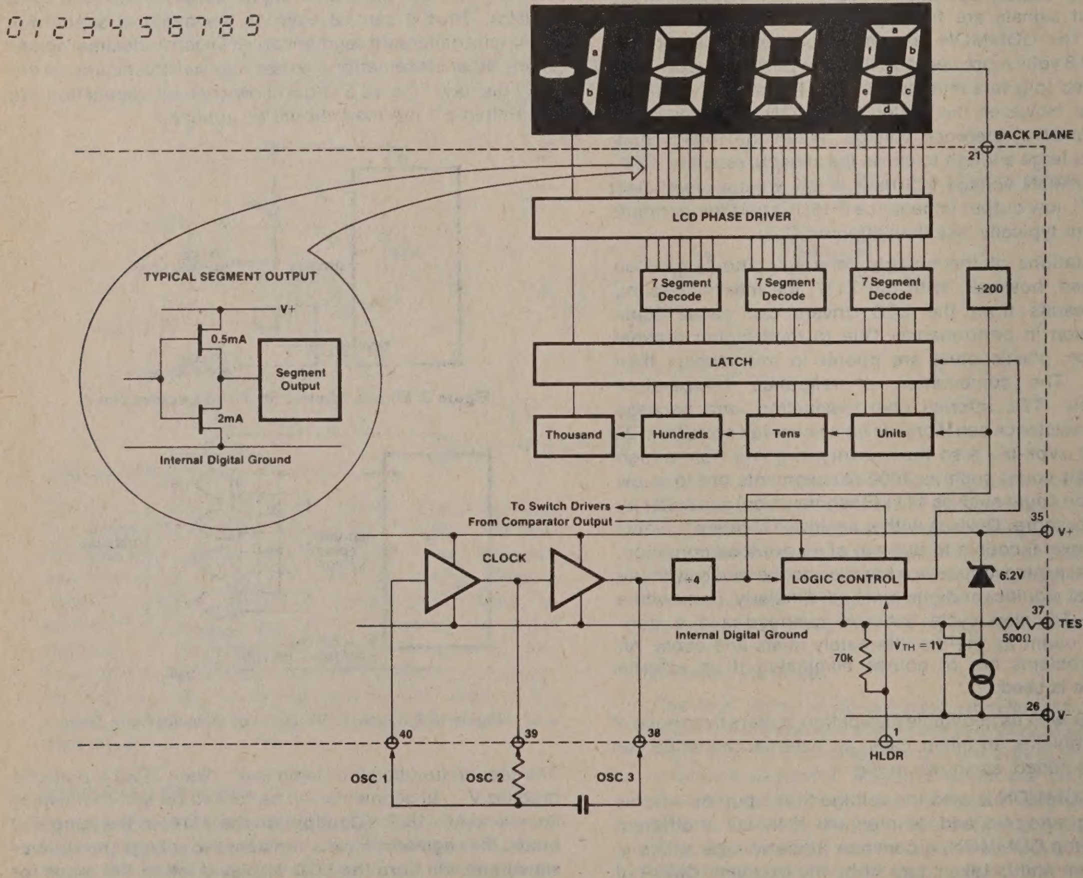

0 1 2 3 4 5 6 7 8 9
a
b
f
g
e
c
d
BACK PLANE
21
LCD PHASE DRIVER
TYPICAL SEGMENT OUTPUT
V+
0.5mA
Segment Output
2mA
Internal Digital Ground
7 Segment Decode
7 Segment Decode
7 Segment Decode
÷200
LATCH
Thousand
Hundreds
Tens
Units
To Switch Drivers
From Comparator Output
35
V+
CLOCK
÷4
LOGIC CONTROL
6.2V
37
TEST
500Ω
Internal Digital Ground
70k
V_TH = 1V
26
V-
40
39
38
1
HLDR
OSC 1
OSC 2
OSC 3

Figure 7: Digital Section 7116

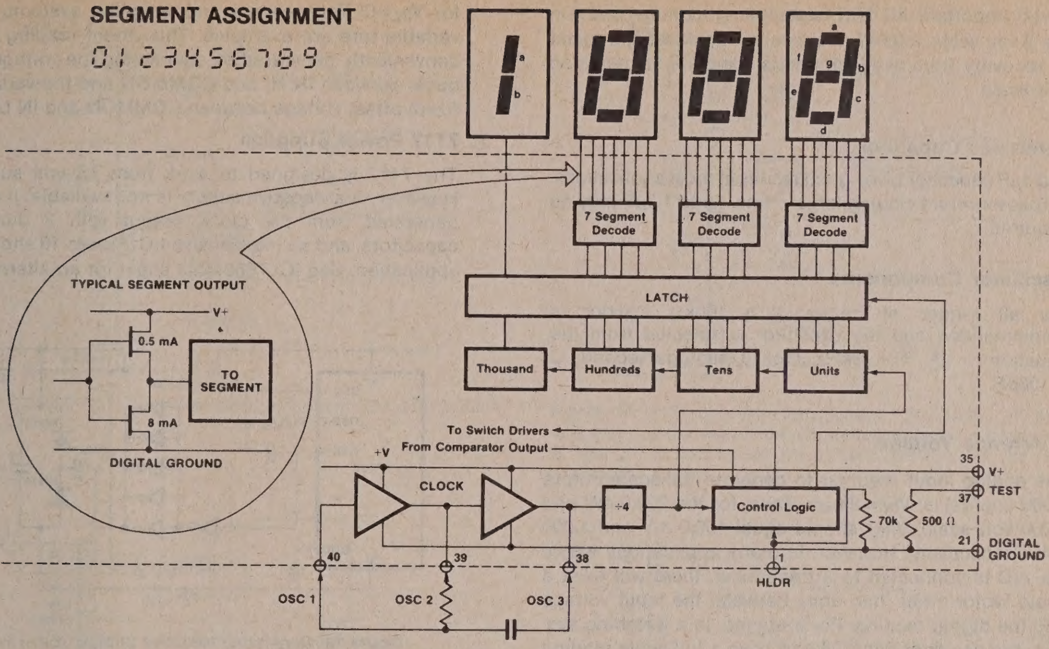

SEGMENT ASSIGNMENT
0 1 2 3 4 5 6 7 8 9
a
b
f
g
e
c
d
7 Segment Decode
7 Segment Decode
7 Segment Decode
LATCH
Thousand
Hundreds
Tens
Units
TYPICAL SEGMENT OUTPUT
V+
0.5 mA
TO SEGMENT
8 mA
DIGITAL GROUND
To Switch Drivers
From Comparator Output
+V
CLOCK
÷4
Control Logic
70k
500 Ω
35
V+
37
TEST
21
DIGITAL GROUND
1
HLDR
40
39
38
OSC 1
OSC 2
OSC 3

Figure 8: Digital Section 7117

System Timing

Figure 9 shows the clocking arrangement used in the 7116 and 7117. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

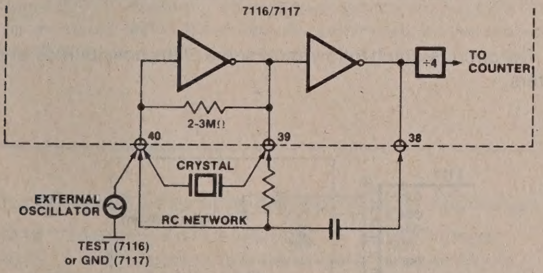

7116/7117
÷4
TO COUNTER
2-3MΩ
40
39
38
CRYSTAL
EXTERNAL OSCILLATOR
RC NETWORK
TEST (7116) or GND (7117)

Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33⅓ kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66⅔ kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200.0 mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7116 or the 7117, when the analog COMMON is used as a reference, a nominal ±2volt full scale integrator swing is fine. For the 7117 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock), nominal values for C_{INT} are 0.22 and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. If rollover errors occur a larger value, up to 1.0μF may be required.

5. Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7117 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7. 7117 Power Supplies

The 7117 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

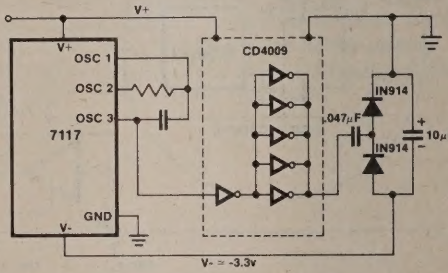

V+
V+
OSC 1
OSC 2
OSC 3
7117
GND
V-
CD4009
IN914
.047μF
IN914
+
10μF
-
V- = -3.3v

Figure 10: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7116 and 7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

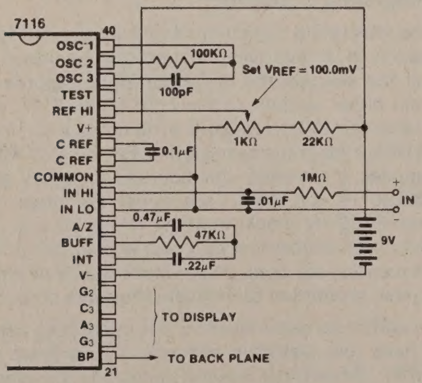

7116
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
V+
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V-
G2
C3
A3
G3
BP
21
100KΩ
100pF
Set VREF = 100.0mV
1KΩ
22KΩ
0.1μF
1MΩ
.01μF
+
IN
-
0.47μF
47KΩ
.22μF
9V
TO DISPLAY
TO BACK PLANE

Figure 11: 7116 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

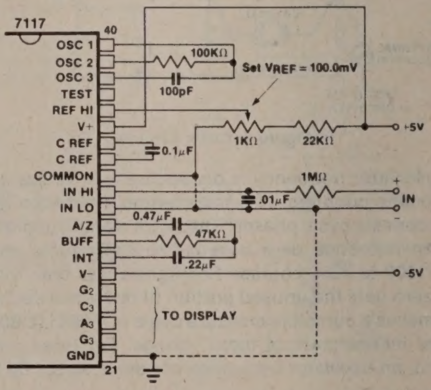

7117
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
V+
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V-
G2
C3
A3
G3
GND
21
100KΩ
100pF
Set VREF = 100.0mV
1KΩ
22KΩ
+5V
0.1μF
1MΩ
.01μF
+
IN
-
0.47μF
47KΩ
.22μF
-5V
TO DISPLAY

Figure 12: 7117 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common.)

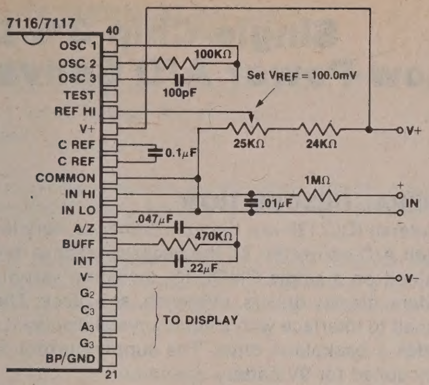

7116/7117
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
V+
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V-
G2
C3
A3
G3
BP/GND
21
100KΩ
100pF
Set VREF = 100.0mV
25KΩ
24KΩ
V+
0.1μF
1MΩ
.01μF
+
IN
-
.047μF
470KΩ
.22μF
V-
TO DISPLAY

Figure 13: 7116/7117: Recommended component values for 2.000V full scale.

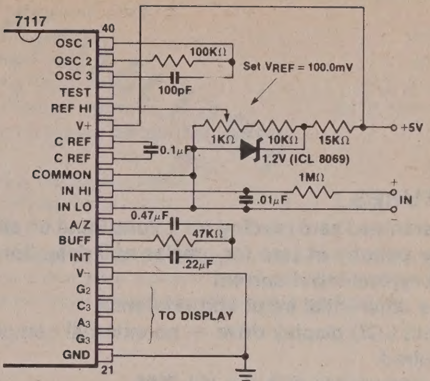

7117
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
V+
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V-
G2
C3
A3
G3
GND
21
100KΩ
100pF
Set VREF = 100.0mV
+5V
1KΩ
10KΩ
15KΩ
0.1μF
1.2V (ICL 8069)
1MΩ
.01μF
+
IN
-
0.47μF
47KΩ
.22μF
TO DISPLAY

Figure 14: 7117 operated from single +5V supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

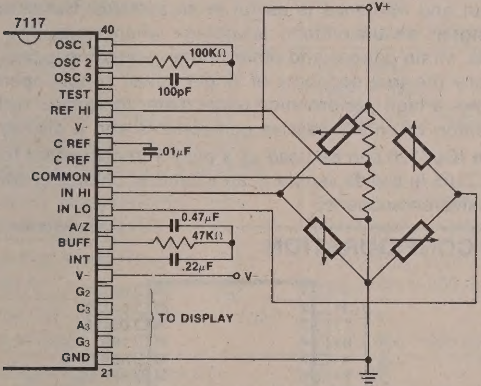

7117
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
V-
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V-
G2
C3
A3
G3
GND
21
V+
100KΩ
100pF
.01μF
0.47μF
47KΩ
.22μF
V-
TO DISPLAY

Figure 15: 7117 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

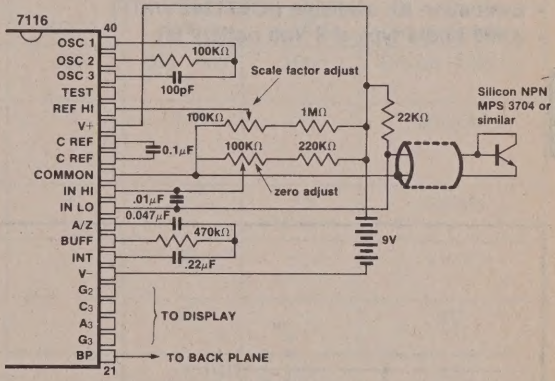

7116
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
V+
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V-
G2
C3
A3
G3
BP
21
100KΩ
100pF
Scale factor adjust
100KΩ
1MΩ
22KΩ
Silicon NPN MPS 3704 or similar
0.1μF
100KΩ
220KΩ
zero adjust
.01μF
0.047μF
470kΩ
9V
.22μF
TO DISPLAY
TO BACK PLANE

Figure 16: 7116 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

For additional information see the following Application Bulletins:

A016 "Selecting A/D Converters," by David Fullagar
A017 "The Integrating A/D Converters," by Lee Evans
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family," by Peter Bradshaw
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff

INTERSIL

ICL7126

Single-Chip 3½-Digit Low-Power A/D Converter

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

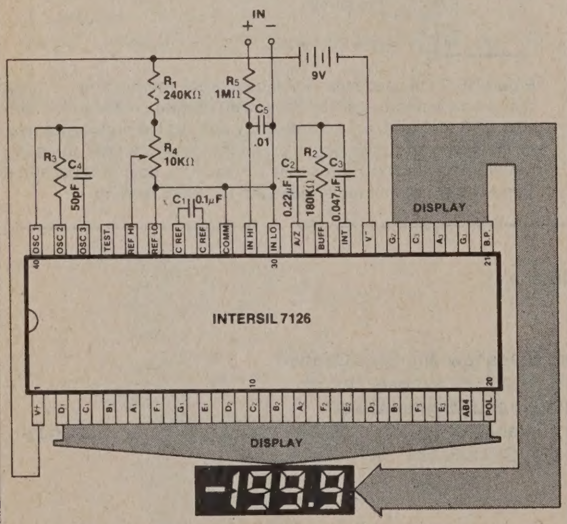
- Guaranteed zero reading for 0 Volts input on all scales
- True polarity at zero for precise null detection
- 1pA typical input current
- True differential input and reference
- Direct LCD display drive — no external components required
- Pin compatible with the ICL7106
- Low noise — less than 15μV p-p
- On-chip clock and reference
- Low power dissipation guaranteed less than 1mW
- No additional active circuits required
- Evaluation Kit available (ICL7126EV/KIT)
- 8,000 hours typical 9 Volt battery life

GENERAL DESCRIPTION

The Intersil ICL7126 is a high performance, very low power 3½ digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven segment decoders, display drivers, reference, and clock. The 7126 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is 100μA, ideally suited for 9V battery operation.

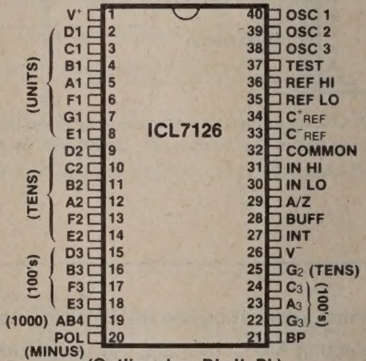
The 7126 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

The ICL7126 can be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.


IN
+
−
R1 240KΩ
R5 1MΩ
C5 .01
9V
R3
C4
50pF
R4 10KΩ
C1 0.1μF
C2 0.22μF
R2 180KΩ
C3 0.047μF
DISPLAY
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMM
IN HI
IN LO
A/Z
BUFF
INT
V−
G2
C3
A3
G3
B.P.
40
30
21
1
10
20
INTERSIL 7126
V+
D1
C1
B1
A1
F1
G1
E1
D2
C2
B2
A2
F2
E2
D3
B3
F3
E3
AB4
POL
DISPLAY
-199.9

ICL7126 with Liquid Crystal Display

PIN CONFIGURATION


V+ 1
D1 2
C1 3
B1 4
A1 5
F1 6
G1 7
E1 8
D2 9
C2 10
B2 11
A2 12
F2 13
E2 14
D3 15
B3 16
F3 17
E3 18
(1000) AB4 19
POL 20
(MINUS)
(UNITS)
(TENS)
(100's)
ICL7126
40 OSC 1
39 OSC 2
38 OSC 3
37 TEST
36 REF HI
35 REF LO
34 C+REF
33 C−REF
32 COMMON
31 IN HI
30 IN LO
29 A/Z
28 BUFF
27 INT
26 V−
25 G2 (TENS)
24 C3
23 A3
22 G3
21 BP
(100's)

(Outline dwg DL,JL,PL)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
7126	0°C to +70°C	40-Pin Ceramic DIP	ICL7126CDL
7126	0°C to +70°C	40-Pin Plastic DIP	ICL7126CPL
7126	0°C to +70°C	40-Pin CERDIP	ICL7126CJL
7126 Kit		Evaluation Kits See page 8.	ICL7126EV/KIT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) .... V^+ to V^-
Clock Input .... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature .... 0°C to +70°C
Storage Temperature.................. −65°C to +160°C
Lead Temperature (Soldering, 60 sec).............. 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	$V_{IN} = 0.0V$ Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ $V_{REF} = 100mV$	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \simeq 200.0mV$	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	$V_{CM} = \pm 1V$, $V_{IN} = 0V$. Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	$V_{IN} = 0V$ Full Scale = 200.0mV		15		μV
Leakage Current @ Input	$V_{IN} = 0V$		1	10	pA
Zero Reading Drift	$V_{IN} = 0$ $0° < T_A < 70°C$		0.2	1	μV/°C
Scale Factor Temperature Coefficient	$V_{IN} = 199.0mV$ $0 < T_A < 70°C$ (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	$V_{IN} = 0$ (Note 6)		50	100	μA
Analog COMMON Voltage (With respect to pos. supply)	250KΩ between Common & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (with respect to pos. Supply)	250KΩ between Common & pos. Supply		80		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to $V^- = 9V$	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to $V^- = 9V$	4	5	6	V
Power Dissipation Capacitance	vs. Clock Freq.		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHZ and are tested in the circuit of Figure 1.
Note 4: Refer to "Differential Input" discussion on page 4.
Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less then 50mV.
Note 6: During auto zero phase, current is 10-20μA higher. 48kHz oscillator, Figure 2, increases current by 8μA (typ)..

TEST CIRCUITS

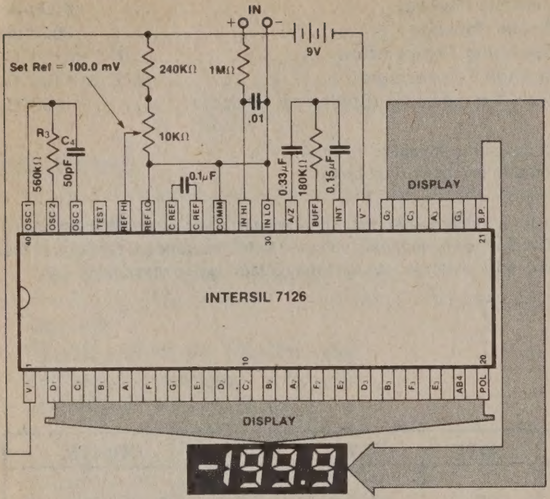

IN
+
-
9V
Set Ref = 100.0 mV
240KΩ
1MΩ
.01
10KΩ
R3
C4
560KΩ
50pF
0.1μF
0.33μF
180KΩ
0.15μF
DISPLAY
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMM
IN HI
IN LO
A/Z
BUFF
INT
V-
G2
C3
A3
G3
B.P.
40
30
21
INTERSIL 7126
1
10
20
V+
D1
C1
B1
A1
F1
G1
E1
D2
C2
B2
A2
F2
E2
D3
B3
F3
E3
AB4
POL
DISPLAY
-199.9

Figure 1: 7126 Clock Frequency 16kHz. (1 reading/sec)

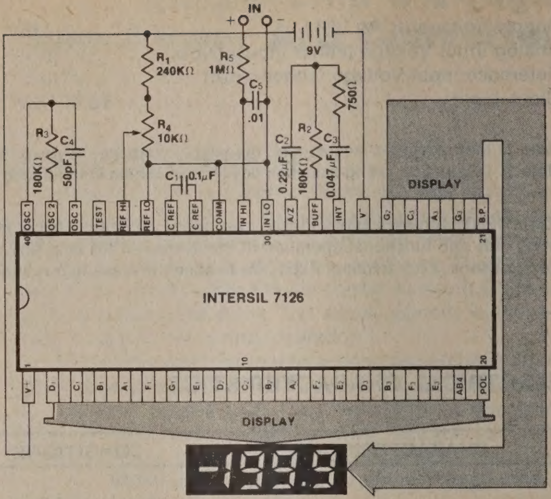

IN
+
-
9V
R1
240KΩ
R5
1MΩ
C5
.01
R4
10KΩ
R3
C4
180KΩ
50pF
C1
0.1μF
C2
R2
C3
0.22μF
180KΩ
0.047μF
750Ω
DISPLAY
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMM
IN HI
IN LO
A/Z
BUFF
INT
V-
G2
C3
A3
G3
B.P.
40
30
21
INTERSIL 7126
1
10
20
V+
D1
C1
B1
A1
F1
G1
E1
D2
C2
B2
A2
F2
E2
D3
B3
F3
E3
AB4
POL
DISPLAY
-199.9

Figure 2: Clock Frequency 48kHZ. (3 readings/sec)

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) deintegrate (DE).

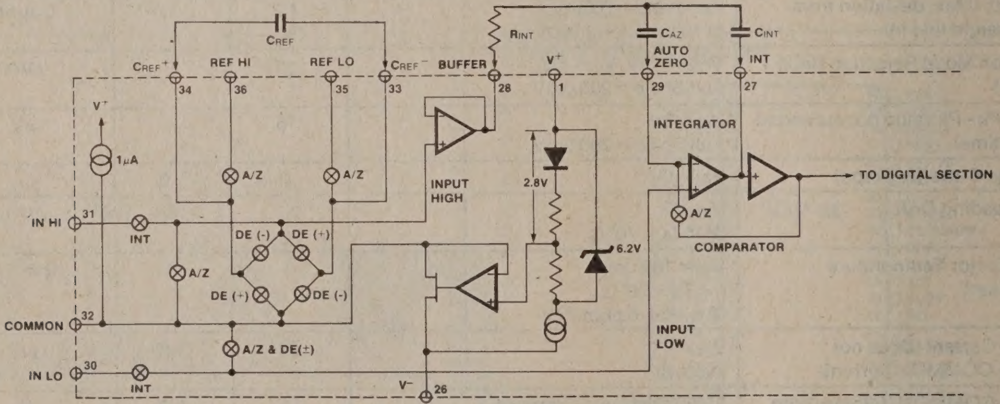

CREF
CREF+
REF HI
REF LO
CREF-
BUFFER
RINT
V+
CAZ
AUTO ZERO
CINT
INT
34
36
35
33
28
1
29
27
V+
1μA
A/Z
A/Z
INPUT HIGH
2.8V
INTEGRATOR
TO DIGITAL SECTION
A/Z
COMPARATOR
IN HI
31
INT
DE (-)
DE (+)
A/Z
DE (+)
DE (-)
6.2V
COMMON
32
A/Z & DE(±)
INPUT LOW
IN LO
30
INT
V-
26

Figure 3: Analog Section of 7126

1. **Auto-zero phase**

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less then $10\mu V$.

2. **Signal Integrate phase**

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one Volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. **De-integrate phase**

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000\left(\frac{V_{IN}}{V_{REF}}\right)$.

Differential Input

The input can accept differential voltages anywhere within the common mode rante of the input amplifier; or specifically from 0.5 Volts below the positive supply to 1.0 Volt above the negative supply. In this range the system has a CMRR of 86 db typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Values Selection below.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 Volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (<7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

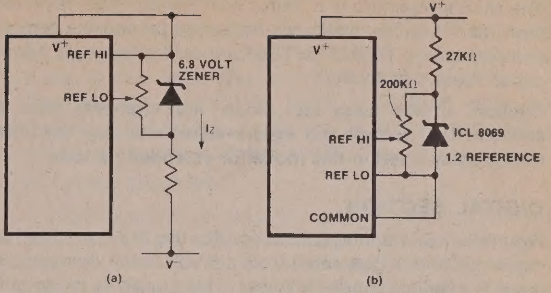


Figure 4: Using an External Reference

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2 to 8°C, typical for instruments, can give a scale factor error of a count or more. Also the common voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 100µA or more of current to hold the voltage 2.8 Volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1µA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

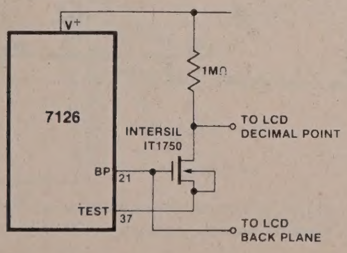


Figure 5: Simple Inverter for Fixed Decimal Point

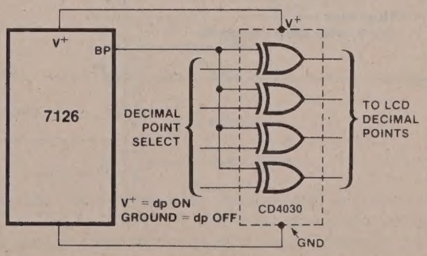


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test." When TEST is pulled high (to V$^+$) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant D-C voltage (no square-wave) and may burn the LCD display if left in this mode for extended periods.

DIGITAL SECTION

Figure 7 shows the digital section for the 7126. An internal digital ground is generated from a 6 Volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 Volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases neglible d-c voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

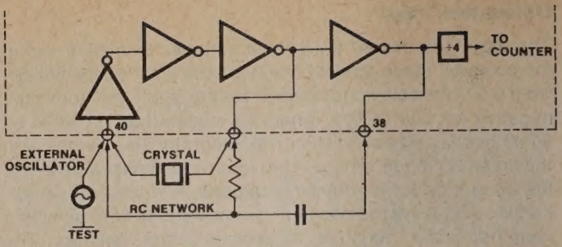

÷4
TO COUNTER
40
38
EXTERNAL OSCILLATOR
CRYSTAL
RC NETWORK
TEST

Figure 8: Clock Circuits

System Timing

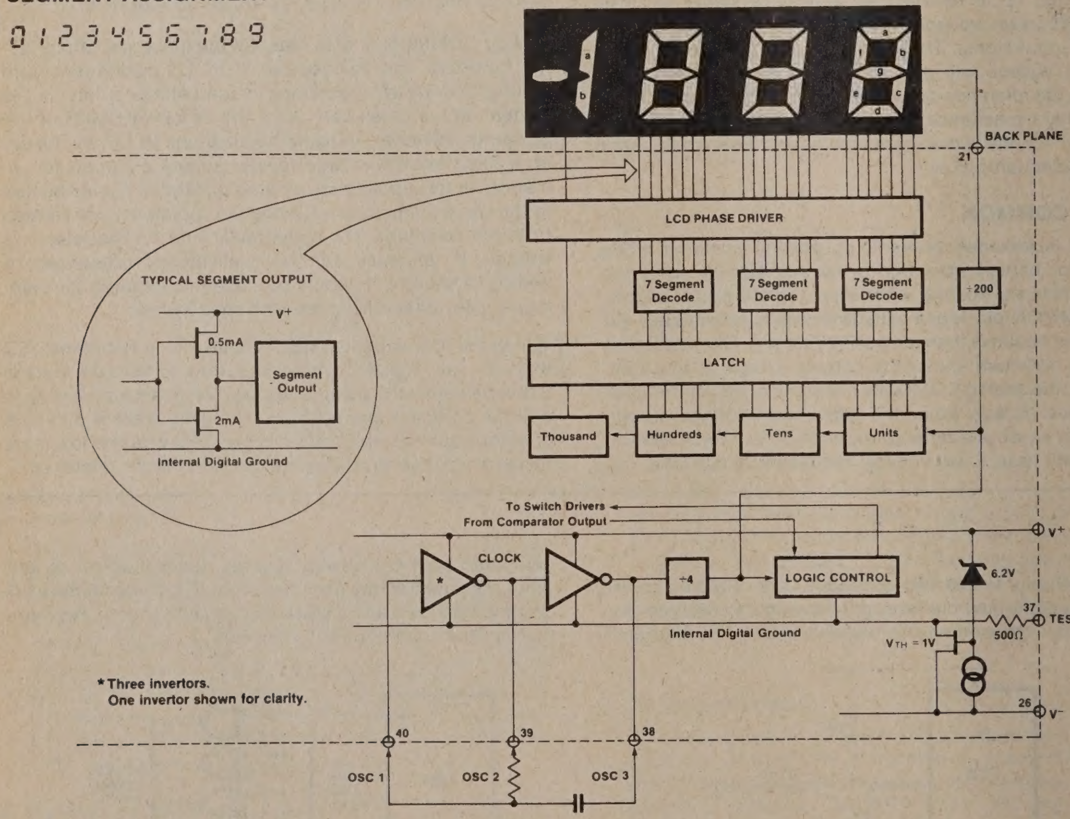
Figure 8 shows the clocking arrangement used in the 7126. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000

SEGMENT ASSIGNMENT

0 1 2 3 4 5 6 7 8 9


a
b
f
g
e
c
d
BACK PLANE
21
LCD PHASE DRIVER
7 Segment Decode
7 Segment Decode
7 Segment Decode
÷200
LATCH
Thousand
Hundreds
Tens
Units
TYPICAL SEGMENT OUTPUT
V+
0.5mA
Segment Output
2mA
Internal Digital Ground
To Switch Drivers
From Comparator Output
CLOCK
÷4
LOGIC CONTROL
6.2V
V+
37
TEST
500Ω
V_{TH} = 1V
26
V-
Internal Digital Ground
40
39
38
OSC 1
OSC 2
OSC 3

*Three invertors.
One invertor shown for clarity.

Figure 7: Digital Section

counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHZ would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33-1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66-2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 Volt full scale, 1.8MΩ is near optimum and similarly 180kΩ for a 200.0mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 Volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 Volt full scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1/sec (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay. See App. Note A017 for a description of the need and effects of this resistor.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.32μF capacitor is recommended. On the 2 Volt scale, a 0.033μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e., the REF LO pin is not analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the foll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{45}{RC}$. For 48kHz clock (3 readings/second), R = 180kΩ.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 Volt scale, V_{REF} should equal 100.0mV and 1.000 Volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. A suitable value for integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighting systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7126 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

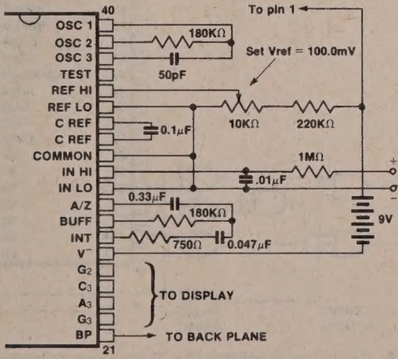


Figure 9: 7126 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).

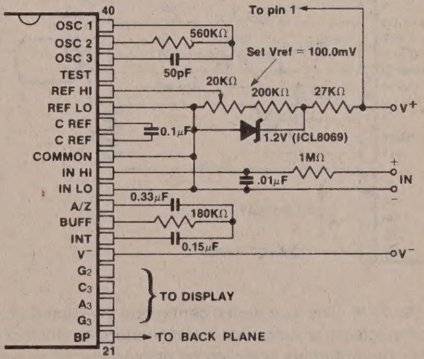


Figure 10: 7126 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading per second.

TYPICAL APPLICATIONS (Contd.)

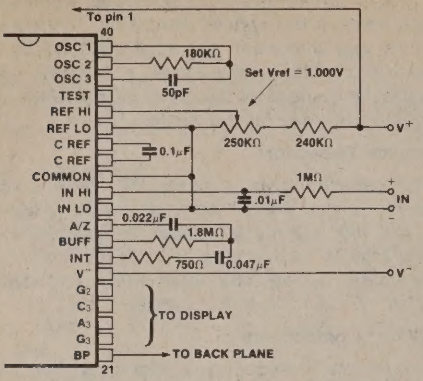

To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
BP
21
180KΩ
50pF
Set Vref = 1.000V
250KΩ
240KΩ
V⁺
0.1μF
1MΩ
.01μF
IN
0.022μF
1.8MΩ
750Ω
0.047μF
V⁻
TO DISPLAY
TO BACK PLANE

Figure 11: Recommended component values for 2.000V full scale, 3 readings per second. For 1 reading per second, delete 750Ω resistor, change C_{INT}, R_{OSC} to values of Fig. 10.

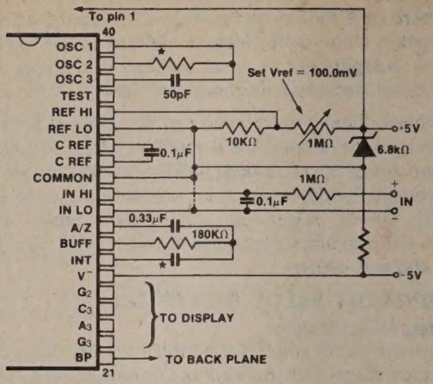

To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
BP
21
*
50pF
Set Vref = 100.0mV
10KΩ
1MΩ
+5V
6.8kΩ
0.1μF
1MΩ
0.1μF
IN
0.33μF
180KΩ
*
-5V
TO DISPLAY
TO BACK PLANE

Figure 12: 7126 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

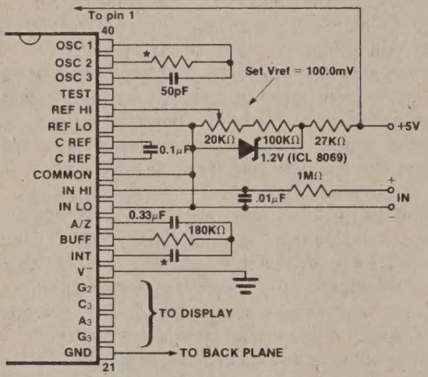

To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
GND
21
*
50pF
Set Vref = 100.0mV
+5V
20KΩ
100KΩ
27KΩ
0.1μF
1.2V (ICL 8069)
1MΩ
.01μF
IN
0.33μF
180KΩ
*
TO DISPLAY
TO BACK PLANE

Figure 13: 7126 operated from single +5V supply. An external reference must be used in this application, since the voltage between V⁺and V⁻ is insufficient for correct operation of the internal reference.

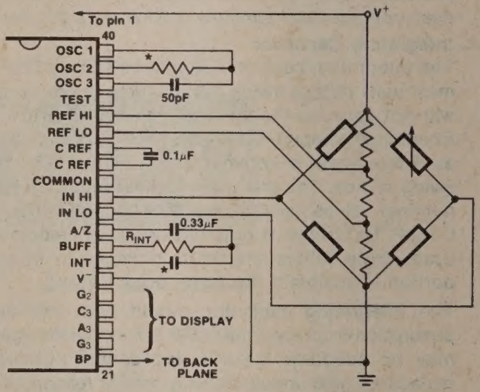

V⁺
To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
BP
21
*
50pF
0.1μF
0.33μF
RINT
*
TO DISPLAY
TO BACK PLANE

Figure 14: 7126 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

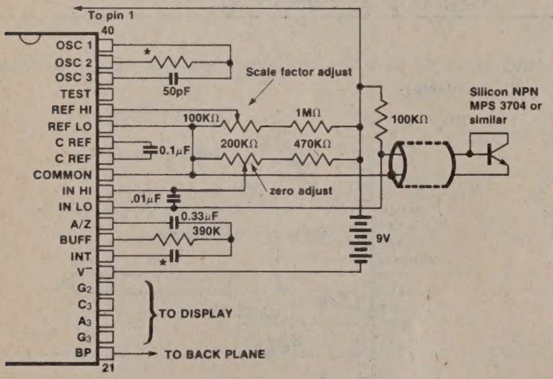

To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
BP
21
*
50pF
Scale factor adjust
100KΩ
1MΩ
100KΩ
Silicon NPN MPS 3704 or similar
200KΩ
470KΩ
0.1μF
zero adjust
.01μF
0.33μF
390K
9V
*
TO DISPLAY
TO BACK PLANE

Figure 15: 7126 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

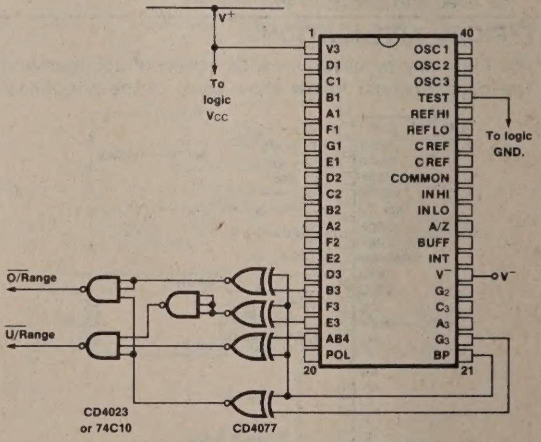

V⁺
To logic Vcc
1
40
V3
D1
C1
B1
A1
F1
G1
E1
D2
C2
B2
A2
F2
E2
D3
B3
F3
E3
AB4
POL
20
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G2
C3
A3
G3
BP
21
To logic GND.
V⁻
O/Range
U/Range
CD4023 or 74C10
CD4077

Figure 16: Circuit for developing Underrange and Overrange signals from 7126 outputs.

*Values depend on clock frequency. See Figure 9, 10, 11.

TYPICAL APPLICATIONS (Contd.)

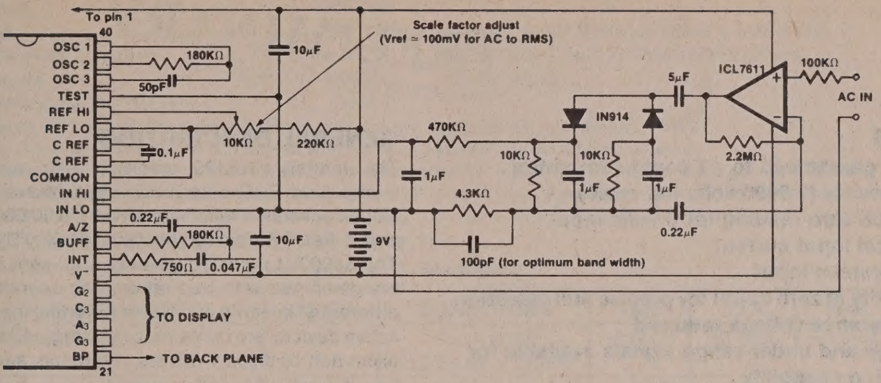

To pin 1
40
OSC 1
OSC 2
OSC 3
TEST
REF HI
REF LO
C REF
C REF
COMMON
IN HI
IN LO
A/Z
BUFF
INT
V⁻
G₂
C₃
A₃
G₃
BP
21
180KΩ
50pF
0.1μF
10μF
Scale factor adjust
(Vref = 100mV for AC to RMS)
10KΩ
220KΩ
0.22μF
180KΩ
750Ω
0.047μF
10μF
9V
TO DISPLAY
TO BACK PLANE
470KΩ
1μF
4.3KΩ
10KΩ
10KΩ
1μF
1μF
IN914
5μF
ICL7611
100KΩ
AC IN
2.2MΩ
0.22μF
100pF (for optimum band width)

Figure 17: AC to DC Converter with 7126. Test is used as a common mode reference level to ensure compatibility with most op-amps.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar
A017 "The Integrating A/D Converter," by Lee Evans
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family," by Peter Bradshaw
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff

7126 EVALUATION KITS

After purchasing a sample of the 7126, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½ digit panel meter. With the ICL7126EV/KIT and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

INTERSIL

ICL7135

Precision 4½ Digit Single Chip A/D Converter

PRELIMINARY
Specifications Subject To Change Without Notice

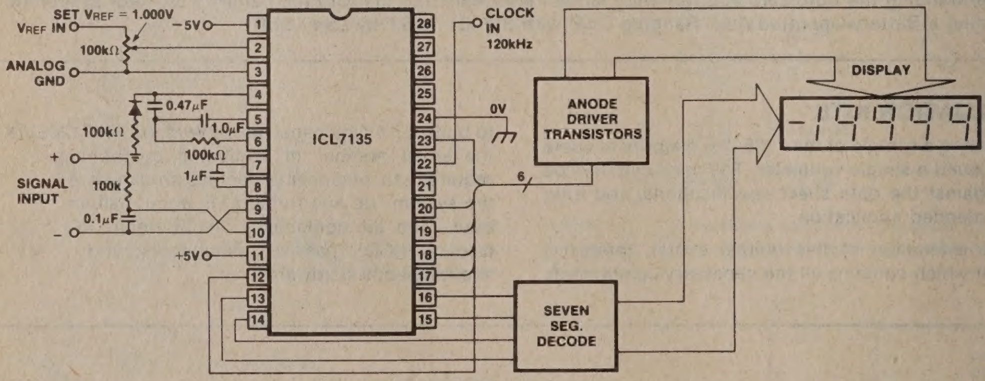
FEATURES

- **Accuracy guaranteed to ±1 count over entire ±20,000 counts (2.0000 volts full scale)**
- **Guaranteed zero reading for 0 volts input**
- **1 pA typical input current**
- **True differential input**
- **True polarity at zero count for precise null detection**
- **Single reference voltage required**
- **Over-range and under-range signals available for auto-ranging capability**
- **All outputs TTL compatible**
- **Blinking display gives visual indication of over-range**
- **Six auxillary inputs/outputs are available for interfacing to UARTs, microprocessors or other complex circuitry**
- **Multiplexed BCD output versatility**

GENERAL DESCRIPTION

The Intersil ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ±1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS I.C., with the exception of display drivers, reference, and a clock.

The Intersil ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include STROBE, OVERRANGE, UNDERRANGE, RUN/$\overline{\text{HOLD}}$ and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

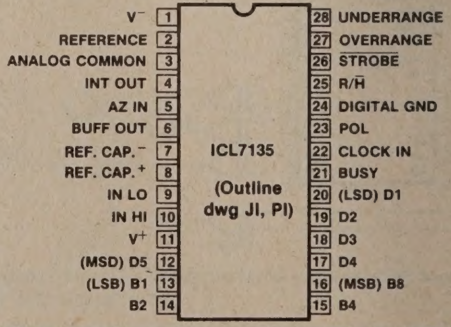

SET VREF = 1.000V
VREF IN
−5V
100kΩ
ANALOG GND
0.47μF
1.0μF
100kΩ
100kΩ
100kΩ
+
SIGNAL INPUT
100k
1μF
0.1μF
−
+5V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
ICL7135
CLOCK IN 120kHz
0V
6
ANODE DRIVER TRANSISTORS
DISPLAY
-19999
SEVEN SEG. DECODE

ICL7135 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7135	28-Pin CERDIP	0°C to +70°C	ICL7135CJI
7135	28-Pin Plastic DIP	0°C to +70°C	ICL7135CPI

PIN CONFIGURATION


V⁻ 1
REFERENCE 2
ANALOG COMMON 3
INT OUT 4
AZ IN 5
BUFF OUT 6
REF. CAP.⁻ 7
REF. CAP.⁺ 8
IN LO 9
IN HI 10
V⁺ 11
(MSD) D5 12
(LSB) B1 13
B2 14
28 UNDERRANGE
27 OVERRANGE
26 STROBE
25 R/H̄
24 DIGITAL GND
23 POL
22 CLOCK IN
21 BUSY
20 (LSD) D1
19 D2
18 D3
17 D4
16 (MSB) B8
15 B4
ICL7135
(Outline dwg JI, PI)

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 2)
Ceramic Package .... 1000 mW
Plastic Package .... 800 mW
Operating Temperature .... 0°C to +70°C
Storage Temperature .... −65°C to +160°C
Lead Temperature (Soldering, 10 sec) .... 300°C

Supply Voltage V^+ .... +6V
V^- .... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) .... V^+ to V^-
Clock Input .... Gnd to V^+

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7135 ELECTRICAL CHARACTERISTICS (Note 1)

$V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

		CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG		Zero Input Reading		$V_{IN} = 0.0V$ Full Scale = 2.000V	−0.0000	±0.0000	+0.0000	Digital Reading
		Ratiometric Reading (2)		$V_{IN} \equiv V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
		Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
		Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
		Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error
(Note 1) (Note 2)		Noise (P-P value not exceeded 95% of time)	e_n	$V_{IN} = 0V$ Full scale = 2.000V		15		μV
		Leakage Current at Input	I_{ILK}	$V_{IN} = 0V$		1	10	pA
		Zero Reading Drift		$V_{IN} = 0V$ $0° \le T_A \le 70°C$		0.5	2	μV/°C
		Scale Factor Temperature Coefficient (3)	TC	$V_{IN} = +2V$ $0 \le T_A \le 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
DIGITAL	INPUTS	Clock In, Run/$\overline{\text{Hold}}$, See Fig. 2	I_{INL} I_{INH}	$V_{IN} = 0$ $V_{IN} = +5V$		0.02 0.1	0.1 10	mA μA
	OUTPUTS	All Outputs	V_{OL}	$I_{OL} = 1.6ma$		0.25	0.40	V
		B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OH}	$I_{OH} = -1mA$	2.4	4.2		V
		BUSY, $\overline{\text{STROBE}}$, OVER-RANGE, UNDER-RANGE POLARITY	V_{OH}	$I_{OH} = -10\mu A$	4.9	4.99		V
	SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
		−5V Supply Range	V^-		−3	−5	−8	V
		+5V Supply Current	I^+	$f_C = 0$		1.1	3.0	mA
		−5V Supply Current	I^-	$f_C = 0$		0.8	3.0	
		Power Dissipation Capacitance	C_{PD}	vs. Clock Freq		40		pF
	Clock	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4-1/2 digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.

Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

Note 3: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

TEST CIRCUIT

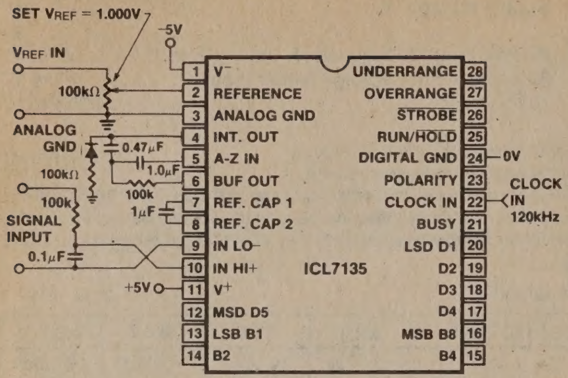

SET VREF = 1.000V
-5V
VREF IN
100kΩ
ANALOG GND
0.47μF
1.0μF
100kΩ
100k
100k
1μF
SIGNAL INPUT
0.1μF
+5V
1 V⁻
2 REFERENCE
3 ANALOG GND
4 INT. OUT
5 A-Z IN
6 BUF OUT
7 REF. CAP 1
8 REF. CAP 2
9 IN LO
10 IN HI
11 V⁺
12 MSD D5
13 LSB B1
14 B2
ICL7135
28 UNDERRANGE
27 OVERRANGE
26 STROBE
25 RUN/HOLD
24 DIGITAL GND
23 POLARITY
22 CLOCK IN
21 BUSY
20 LSD D1
19 D2
18 D3
17 D4
16 MSB B8
15 B4
0V
CLOCK IN 120kHz

Figure 1: 7135 Test Circuit

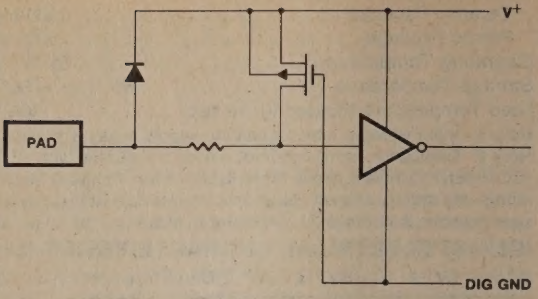

V⁺
PAD
DIG GND

Figure 2: 7135 Digital Logic Input

DETAILED DESCRIPTION

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7135. Each measurement cycle is divided into four phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT), (3) deintegrate (DE) and (4) zero integrator (ZI).

1. **Auto-zero phase**

   During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. **Signal Integrate phase**

   During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the polarity F/F.

3. **De-Integrate phase**

   The Third phase is de-integrate, or reference integrate. Input Low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 10,000 ($\frac{V_{IN}}{V_{REF}}$).

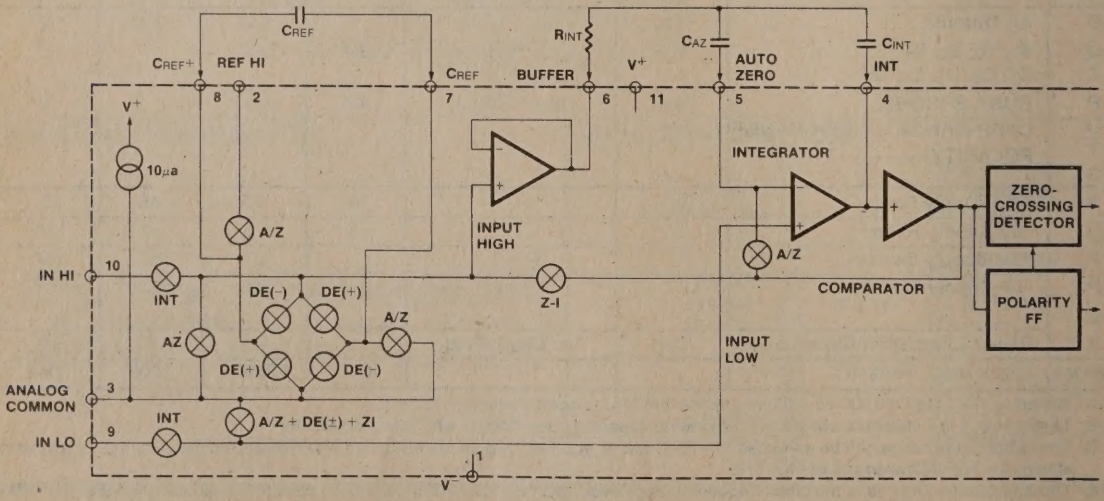

CREF
CREF+
REF HI
CREF-
BUFFER
RINT
V⁺
CAZ
AUTO ZERO
CINT
INT
8
2
7
6
11
5
4
V⁺
10μa
A/Z
INPUT HIGH
INTEGRATOR
ZERO-CROSSING DETECTOR
A/Z
IN HI
10
INT
Z-I
COMPARATOR
POLARITY FF
DE(-)
DE(+)
A/Z
AZ
DE(+)
DE(-)
INPUT LOW
ANALOG COMMON
3
INT
A/Z + DE(±) + ZI
IN LO
9
1
V⁻

Figure 3: Analog Section of ICL7135

4. Zero Integrator phase

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog COMMON

Analog COMMON is used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Fig. 4.

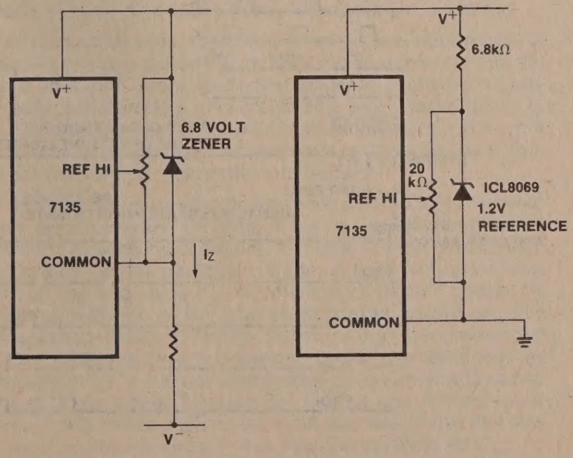
DETAILED DESCRIPTION

Digital Section

Figure 5 is the Digital Section of the 7135. It is identical to the 71C03 except that the 4-1/2/$\overline{3\text{-}1/2}$ digit pin has been eliminated (mask-option; consult factory). The 7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

1. RUN/$\overline{\text{HOLD}}$ (Pin 25). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002 clock pulses. If taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as R/$\overline{\text{H}}$ is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle, beginning with between 9,001 and 10,001 counts of auto zero. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 101 counts after the end of this cycle. Thus, if Run/$\overline{\text{Hold}}$ is low and has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

2. $\overline{\text{STROBE}}$ (Pin 26). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going $\overline{\text{STROBE}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 pules after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{STROBE}}$ pulse goes negative for 1/2 clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the $\overline{\text{STROBE}}$ goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last $\overline{\text{STROBE}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional $\overline{\text{STROBE}}$ pulses will be sent until a new measurement is available.



(a) (b)

Figure 4: Using an External Reference

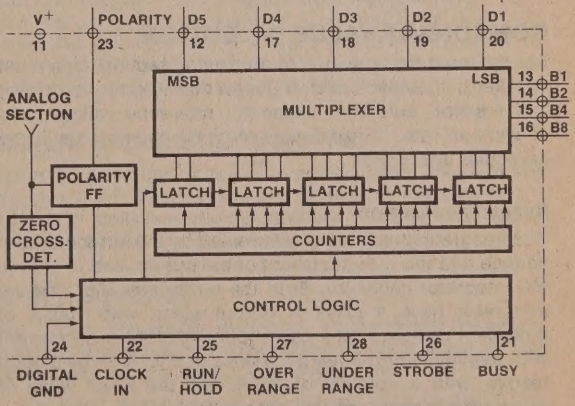


Figure 5: Digital Section 7135

3. BUSY (Pin 21). BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an over-range). The internal latches are enabled (i.e., loaded) during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY, so it may also be considered a (ZI + AZ) signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001 counts from the number of pulses received - as mentioned previously there is one "NO-count" pulse in each reference integrate cycle.

4. OVER-RANGE (Pin 27). This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output F-F is set at the end of BUSY and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

5. UNDER-RANGE (Pin 28). This pin goes positive when the reading is 9% of range or less. The output F-F is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of signal integrate of the next reading.

6. POLARITY (Pin 23). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (−) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

7. Digit Drives (Pins 12, 17, 18, 19 and 20). Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned and this scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D_5 will start the scan again. This can give a blinking display as a visual indication of over-range.

8. BCD (Pins 13, 14, 15 and 16). The Binary coded Decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the digit driver signal.

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. Values of 5 to 40μA give good results, with a nominal of 20μA, and the exact value of integrating resistor may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt full scale integrator swing is fine, and 0.10μF is nominal. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{integrator output voltage swing}} = \frac{(10{,}000)\ (\text{clock period})\ (20\mu A)}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

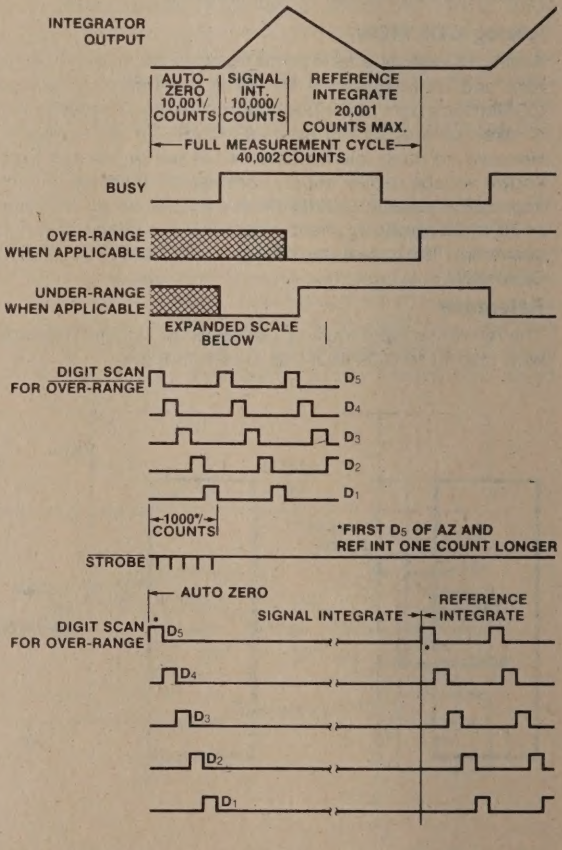

INTEGRATOR OUTPUT
AUTO-ZERO 10,001/ COUNTS
SIGNAL INT. 10,000/ COUNTS
REFERENCE INTEGRATE 20,001 COUNTS MAX.
FULL MEASUREMENT CYCLE 40,002 COUNTS
BUSY
OVER-RANGE WHEN APPLICABLE
UNDER-RANGE WHEN APPLICABLE
EXPANDED SCALE BELOW
DIGIT SCAN FOR OVER-RANGE
D5
D4
D3
D2
D1
1000*/ COUNTS
*FIRST D5 OF AZ AND REF INT ONE COUNT LONGER
STROBE
AUTO ZERO
SIGNAL INTEGRATE
REFERENCE INTEGRATE
DIGIT SCAN FOR OVER-RANGE
D5
D4
D3
D2
D1

Figure 6: Timing Diagram for Outputs

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

Rollover Resistor and Diode

A small rollover error occurs in the 7135, but this can be easily corrected by adding a diode and resistor in series between the INTegrator OUTput and analog COMMON or ground. The value shown in the schematics is optimum for the recommended conditions, but if integrator swing or clock frequency is modified adjustment may be needed. The diode can be any silicon diode, such as a 1N914. These components can be eliminated if rollover error is not important, and may be altered in value to correct other (small) sources of rollover as needed.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3μs delay, and at a clock frequency of 160kHz (6μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50μV input, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many-dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant nonlinearities in the first few counts of the instrument - see Application Note A017.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, 166⅔kHz, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50 and 60Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

EVALUATING THE ERROR SOURCES

Errors from the "ideal" cycle are caused by:

1. Capacitor droop due to leakage.
2. Capacitor voltage change due to charge "suck-out" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.
4. High-frequency limitations of buffer, integrator and comparator.
5. Integrating capacitor non-linearity (dielectric absorption.)
6. Charge lost by C_{REF} in charging C_{stray}.
7. Charge lost by C_{AZ} and C_{INT} to charge C_{stray}.

Each of these errors is analyzed for its error contribution to the converter in application notes listed on the back page, specifically A017 and A032.

NOISE

The peak-to-peak noise around zero is approximately 15μV (pk-to-pk value not exceeded 95% of the time). Near full scale, this value increases to approximately 30μV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

POWER SUPPLIES

The 7135 is designed to work from ±5V supplies. However, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.

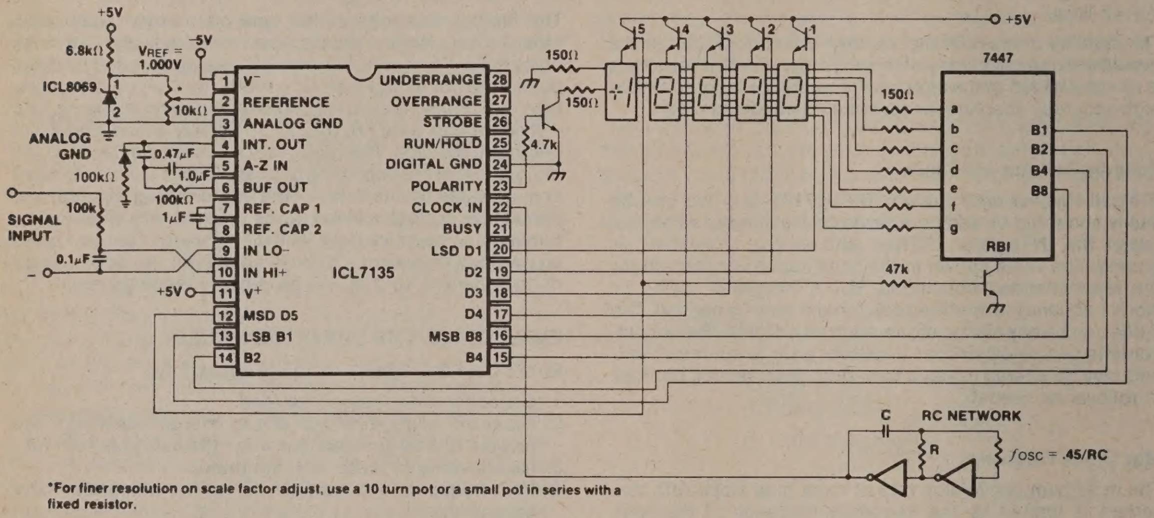
See "differential input" for a discussion of the effects this will have on the integrator swing without loss of linearity.

TYPICAL APPLICATIONS

The circuits which follow show some of the wide variety of possibilities, and serve to illustrate the exceptional versatility of this A/D converter.

Figure 7 shows the complete circuit for a 4-1/2 digit (±2.000V) full scale) A/D with LED readout using the ICL8069 as a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50μA. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The 1/2 digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder. The 2-gate clock circuit should use CMOS gates to maintain good power supply rejection.

Figure 8 is similar except the output drives a multiplexed common cathode LED Display with the 7-Common Emitter Transistor Array, for the digit driver transistors, making a lower component count possible. Both versions of the complete circuit will give a blinking display as a visual indication of overrange. A clock oscillator circuit using the ICM7555 CMOS timer is shown.


+5V
6.8kΩ
VREF = 1.000V
-5V
ICL8069
10kΩ
ANALOG GND
0.47μF
1.0μF
100kΩ
100kΩ
1μF
100k
SIGNAL INPUT
0.1μF
+5V
1 V⁻
2 REFERENCE
3 ANALOG GND
4 INT. OUT
5 A-Z IN
6 BUF OUT
7 REF. CAP 1
8 REF. CAP 2
9 IN LO⁻
10 IN HI+
11 V⁺
12 MSD D5
13 LSB B1
14 B2
ICL7135
28 UNDERRANGE
27 OVERRANGE
26 STROBE
25 RUN/HOLD
24 DIGITAL GND
23 POLARITY
22 CLOCK IN
21 BUSY
20 LSD D1
19 D2
18 D3
17 D4
16 MSB B8
15 B4
150Ω
150Ω
4.7k
5
4
3
2
1
+5V
7447
150Ω
a
b
c
d
e
f
g
B1
B2
B4
B8
RBI
47k
C
RC NETWORK
R
fosc = .45/RC

*For finer resolution on scale factor adjust, use a 10 turn pot or a small pot in series with a fixed resistor.

Figure 7: 4-1/2 Digit A-D Converter with a multiplexed common anode LED display

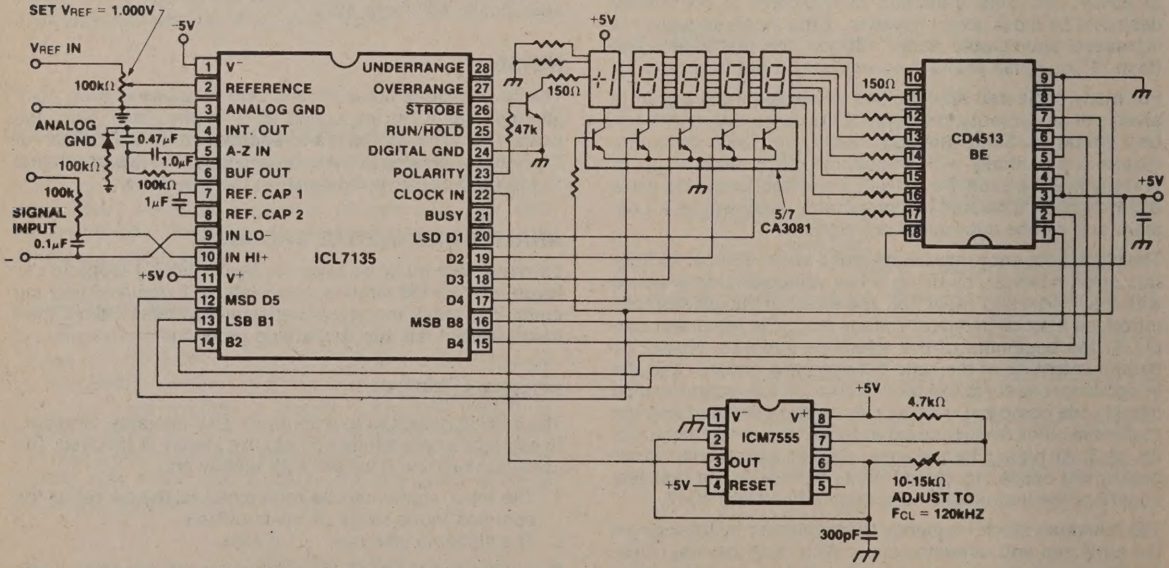

SET VREF = 1.000V
-5V
VREF IN
100kΩ
ANALOG GND
0.47μF
1.0μF
100kΩ
100kΩ
1μF
100k
SIGNAL INPUT
0.1μF
+5V
1 V⁻
2 REFERENCE
3 ANALOG GND
4 INT. OUT
5 A-Z IN
6 BUF OUT
7 REF. CAP 1
8 REF. CAP 2
9 IN LO⁻
10 IN HI+
11 V⁺
12 MSD D5
13 LSB B1
14 B2
ICL7135
28 UNDERRANGE
27 OVERRANGE
26 STROBE
25 RUN/HOLD
24 DIGITAL GND
23 POLARITY
22 CLOCK IN
21 BUSY
20 LSD D1
19 D2
18 D3
17 D4
16 MSB B8
15 B4
+5V
150Ω
47k
5/7 CA3081
150Ω
CD4513 BE
10 11 12 13 14 15 16 17 18
9 8 7 6 5 4 3 2 1
+5V
+5V
4.7kΩ
1 V⁻
2
3 OUT
4 RESET
ICM7555
8 V⁺
7
6
5
+5V
10-15kΩ ADJUST TO FCL = 120kHZ
300pF

Figure 8: Driving multiplexed common cathode LED displays

A suitable circuit for driving a plasma-type display is shown in Fig. 9. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving 'BI' are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The 2.5k & 3k resistors set the current levels in the display. A similar arrangement can be used with Nixie® tubes.

The popular LCD displays can be interfaced to the O/P of the ICL7135 with suitable display drivers, such as the ICM7211A as shown in Figure 11. A standard CMOS 4000 series LCD driver circuit is used for displaying the 1/2 digit, the polarity, and an 'overrange' flag. A similar circuit can be used with the ICL7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the 'extra' outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a 4-1/2 digit (±2.000V) A/D.

Figure 10 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the $\overline{\text{STROBE}}$ signal and 'Overrange' is indicated by blanking the 4 full digits.

® Nixie is a registered trademark of Burroughs Corporation.

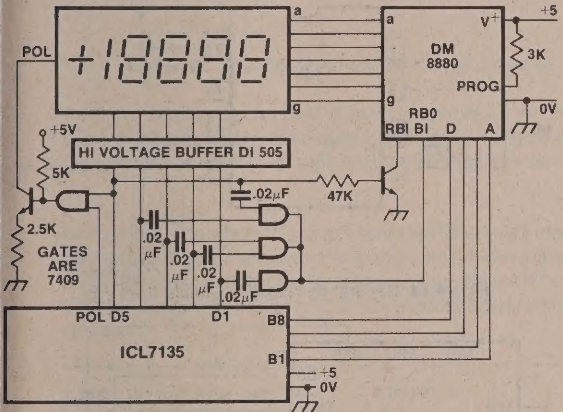

POL
a
g
a
V+
+5
DM
8880
3K
PROG
g
RBO
RBI BI
D
A
0V
+5V
HI VOLTAGE BUFFER DI 505
5K
.02μF
47K
2.5K
.02
μF
.02
μF
.02
μF
.02μF
GATES
ARE
7409
POL D5
D1
B8
ICL7135
B1
+5
0V

Figure 9: ICL7135 Plasma Display Circuit

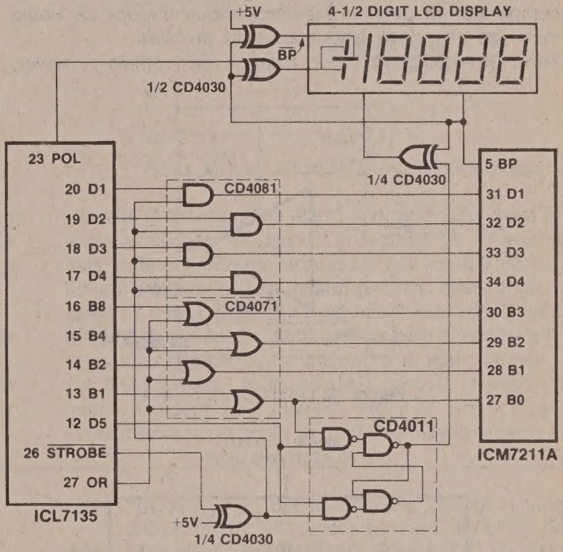

+5V
4-1/2 DIGIT LCD DISPLAY
BP
1/2 CD4030
23 POL
20 D1
19 D2
18 D3
17 D4
16 B8
15 B4
14 B2
13 B1
12 D5
26 STROBE
27 OR
ICL7135
CD4081
CD4071
CD4011
1/4 CD4030
5 BP
31 D1
32 D2
33 D3
34 D4
30 B3
29 B2
28 B1
27 B0
ICM7211A
+5V
1/4 CD4030

Figure 10: LCD Display with Digit Blanking on Overrange

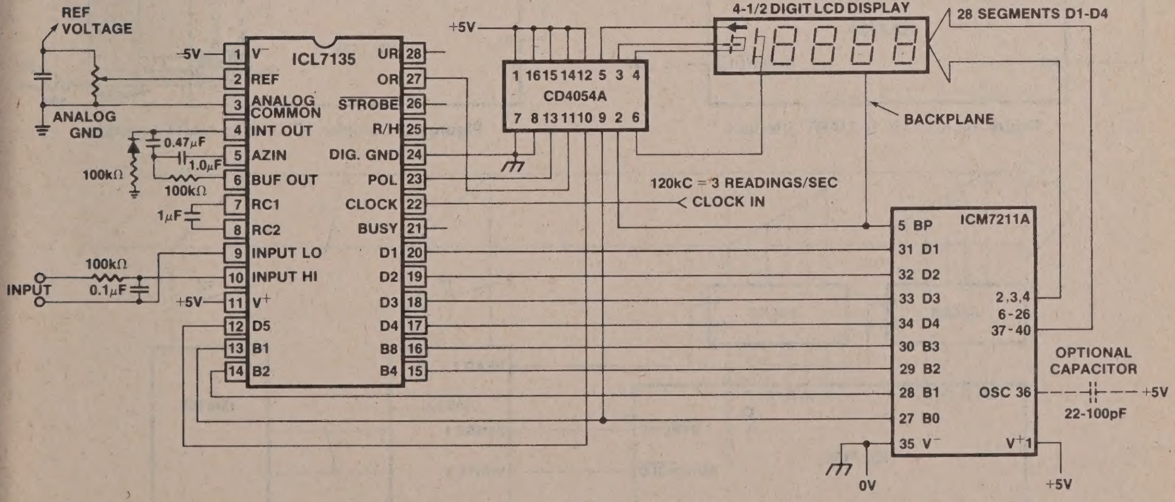

REF
VOLTAGE
ANALOG
GND
-5V
1 V−
2 REF
3 ANALOG COMMON
4 INT OUT
5 AZIN
6 BUF OUT
7 RC1
8 RC2
9 INPUT LO
10 INPUT HI
11 V+
12 D5
13 B1
14 B2
ICL7135
UR 28
OR 27
STROBE 26
R/H 25
DIG. GND 24
POL 23
CLOCK 22
BUSY 21
D1 20
D2 19
D3 18
D4 17
B8 16
B4 15
0.47μF
1.0μF
100kΩ
100kΩ
1μF
100kΩ
0.1μF
INPUT
+5V
+5V
1 16 15 14 12 5 3 4
CD4054A
7 8 13 11 10 9 2 6
4-1/2 DIGIT LCD DISPLAY
28 SEGMENTS D1-D4
BACKPLANE
120kC = 3 READINGS/SEC
CLOCK IN
ICM7211A
5 BP
31 D1
32 D2
33 D3
34 D4
30 B3
29 B2
28 B1
27 B0
35 V−
2,3,4
6-26
37-40
OSC 36
V+ 1
OPTIONAL
CAPACITOR
22-100pF
+5V
0V
+5V

Figure 11: Driving LCD Displays

TYPICAL APPLICATIONS (Contd.)

A problem sometimes encountered with both LED & plasma-type display driving is that of clock source supply line variations. Since the supply is shared with the display, any variation in voltage due to the display reading may cause clock supply voltage modulation. When in overrange the display alternates between a blank display and the 0000 overrange indication. This shift occurs during the reference integrate phase of conversion causing a low display reading just after overrange recovery. Both of the above circuits have considerable current flowing in the digital supply from drivers, etc. A clock source using Intersil's LM311 voltage comparator in positive feedback mode (Figure 12) could minimize any clock frequency shift problem.

The 7135 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated fro 2 capacitors, and an inexpensive I.C. (Figure 13).

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 14 shows a very simple interface between a free running ICL7135 and a UART. The five $\overline{\text{STROBE}}$ pulses sta the transmission of the five data words. The digit 5 word i 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Als the polarity is transmitted indirectly by using it to drive th Even Parity Enable Pin (EPE). If EPE of the receiver is hel low, a parity flag at the receiver can be decoded as a positiv signal, no flag as negative. A complex arrangement is show in Figure 15. Here the UART can instruct the A/D to begin measurement sequence by a word on RRI. The BUSY signa resets the Data Ready Reset (DRR). Again $\overline{\text{STROBE}}$ starts th

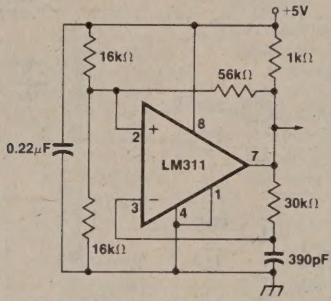

+5V
16kΩ
1kΩ
56kΩ
8
2
+
LM311
7
0.22μF
3
−
1
4
30kΩ
16kΩ
390pF

Figure 12: LM311 Clock Source

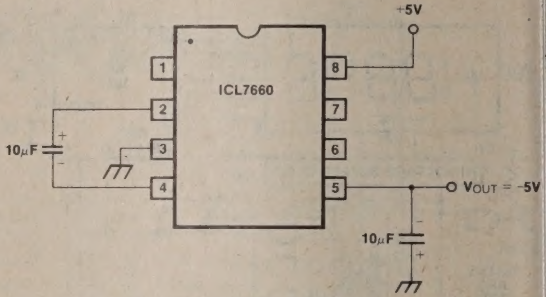

+5V
ICL7660
1
2
3
4
8
7
6
5
10μF
+
VOUT = −5V
10μF
+

Figure 13: Generating Negative Supply from +5V

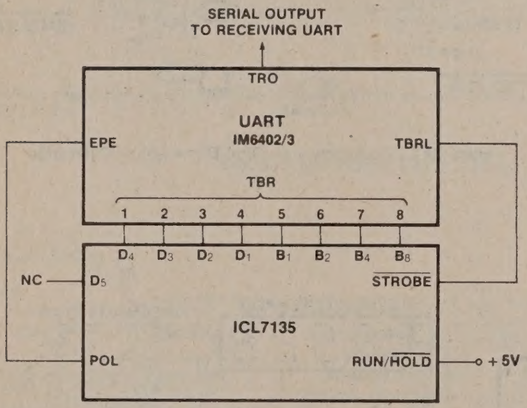

SERIAL OUTPUT
TO RECEIVING UART
TRO
UART
IM6402/3
EPE
TBRL
TBR
1 2 3 4 5 6 7 8
D4 D3 D2 D1 B1 B2 B4 B8
NC
D5
STROBE
ICL7135
POL
RUN/HOLD
+5V

Figure 14: ICL7135 to UART Interface

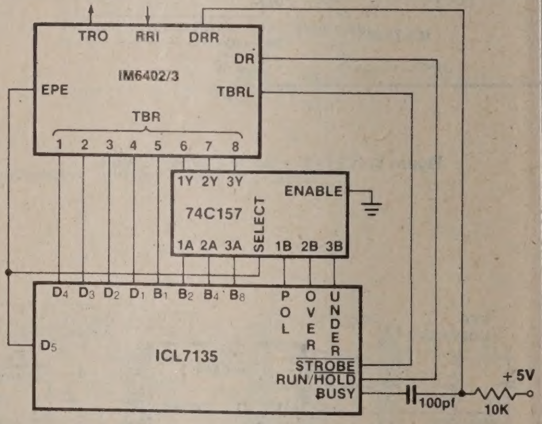

TRO
RRI
DRR
DR
IM6402/3
EPE
TBRL
TBR
1 2 3 4 5 6 7 8
1Y 2Y 3Y
ENABLE
74C157
SELECT
1A 2A 3A
1B 2B 3B
D4 D3 D2 D1 B1 B2 B4 B8
POL
OVER
UNDER
D5
ICL7135
STROBE
RUN/HOLD
BUSY
100pf
+5V
10K

Figure 15: Complex ICL7135 to UART Interface

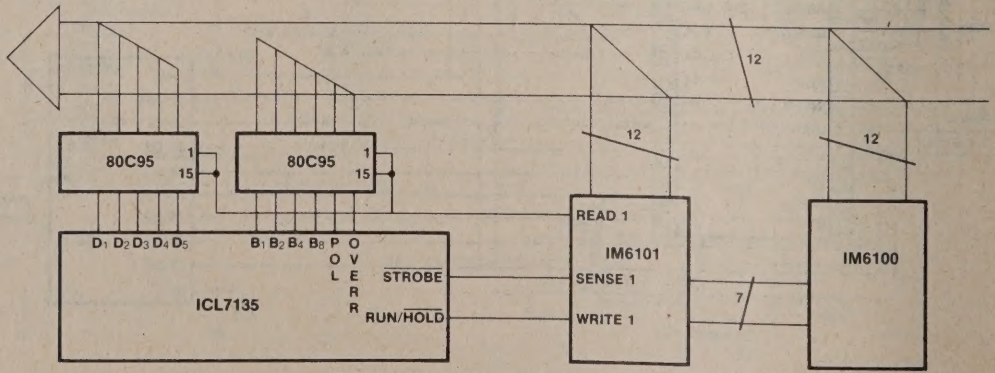

12
12
12
80C95
1
15
80C95
1
15
D1 D2 D3 D4 D5
B1 B2 B4 B8 P O
O V
L E
R
R
STROBE
ICL7135
RUN/HOLD
READ 1
IM6101
SENSE 1
7
WRITE 1
IM6100

Figure 16: IM6100 to ICL7135 Interface

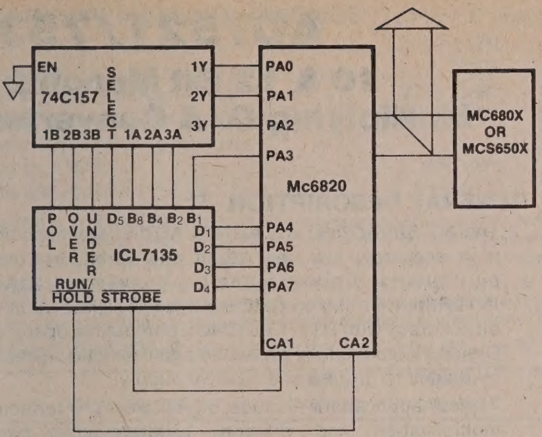

EN
74C157
SELECT
1Y
2Y
3Y
1B 2B 3B 1A 2A 3A
PA0
PA1
PA2
PA3
Mc6820
PA4
PA5
PA6
PA7
CA1
CA2
MC680X
OR
MCS650X
POL
OVER
UNDER
D5 B8 B4 B2 B1
D1
D2
D3
D4
ICL7135
RUN/HOLD
STROBE

Figure 17: ICL7135 to MC6800, MCS650X Interface

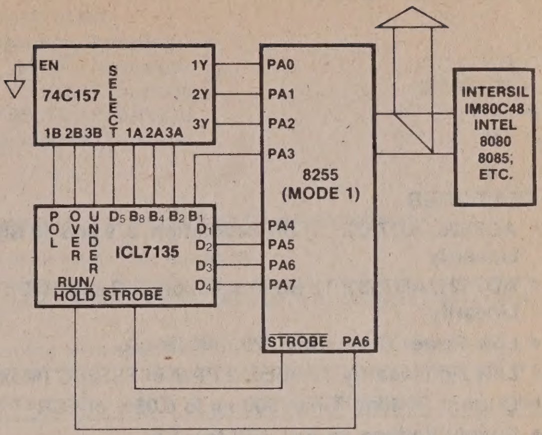

EN
74C157
SELECT
1Y
2Y
3Y
1B 2B 3B 1A 2A 3A
PA0
PA1
PA2
PA3
8255
(MODE 1)
PA4
PA5
PA6
PA7
STROBE
PA6
INTERSIL
IM80C48
INTEL
8080
8085,
ETC.
POL
OVER
UNDER
D5 B8 B4 B2 B1
D1
D2
D3
D4
ICL7135
RUN/HOLD
STROBE

Figure 18: ICL7135 to MCS-48, -80, 85 Interface

transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next $\overline{\text{STROBE}}$ pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the ICL7135 directly with three popular microprocessors are shown in Figures 16, 17 and 18. The main differences in the circuits are that the IM6100 with its 12 bit word capability can accept polarity, over-range, under-range, 4 bits of BCD and 5 digits simultaneously where the 8080/8048 and the MC6800 groups with 8 bit words need to have polarity, over-range and under-range multiplexed onto the Digit 5 word - as in the UART circuit. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar
A017 "The Integrating A/D Converters," by Lee Evans
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A019 "4-1/2 Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort
A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort
A028 "Building an Auto-Ranging DMM Using the 8052A/7103A A/D Converter Pair," by Larry Goff
A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family", by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

INTERSIL

AD7520/7530
AD7521/7531
10 & 12 Bit Monolithic Multiplying D/A Converters

FEATURES

- **AD7520/AD7530: 10 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **AD7521/AD7531: 12 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **Low Power Dissipation: 20 mW (Max)**
- **Low Nonlinearity Tempco: 2 PPM of FSR/° C (Max)**
- **Current Settling Time: 500 ns to 0.05% of FSR**
- **Supply Voltage Range: +5V to +15V**
- **DTL/TTL/CMOS Compatible**
- **Full Input Static Protection**
- **883B Processed Versions Available**

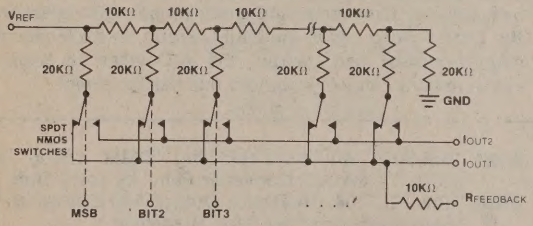
GENERAL DESCRIPTION

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). INTERSIL thin-film on CMOS processing gives up to 10-bit accuracy with DTL/TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

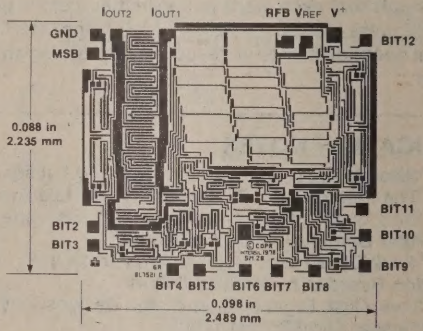
FUNCTIONAL DIAGRAM



VREF
10KΩ
10KΩ
10KΩ
10KΩ
20KΩ
20KΩ
20KΩ
20KΩ
20KΩ
20KΩ
GND
SPDT NMOS SWITCHES
IOUT2
IOUT1
10KΩ
RFEEDBACK
MSB
BIT2
BIT3

(Switches shown for Digital Inputs "High")
(Resistor values are nominal)

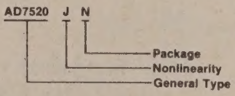
CHIP TOPOGRAPHY



IOUT2
IOUT1
RFB
VREF
V+
GND
MSB
BIT12
0.088 in
2.235 mm
BIT11
BIT10
BIT2
BIT3
BIT9
BIT4
BIT5
BIT6
BIT7
BIT8
0.098 in
2.489 mm

PACKAGE IDENTIFICATION

Suffix D: Cerdip package
Suffix N: Plastic DIP package

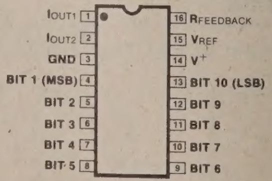


AD7520
J
N
Package
Nonlinearity
General Type

PIN CONFIGURATION (Outline dwgs DE, PE)

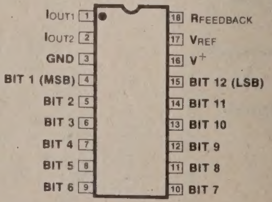
TOP VIEW

AD7520 (AD7530)



IOUT1 1
IOUT2 2
GND 3
BIT 1 (MSB) 4
BIT 2 5
BIT 3 6
BIT 4 7
BIT 5 8
16 RFEEDBACK
15 VREF
14 V+
13 BIT 10 (LSB)
12 BIT 9
11 BIT 8
10 BIT 7
9 BIT 6

AD7521 (AD7531)



IOUT1 1
IOUT2 2
GND 3
BIT 1 (MSB) 4
BIT 2 5
BIT 3 6
BIT 4 7
BIT 5 8
BIT 6 9
18 RFEEDBACK
17 VREF
16 V+
15 BIT 12 (LSB)
14 BIT 11
13 BIT 10
12 BIT 9
11 BIT 8
10 BIT 7

ORDERING INFORMATION

	Temperature Range		
Nonlinearity	0°C to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7530JN AD7521JN AD7531JN	AD7520JD AD7530JD AD7521JD AD7531JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7530KN AD7521KN AD7531KN	AD7520KD AD7530KD AD7521KD AD7531KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7530LN AD7521LN AD7531LN	AD7520LD AD7530LD AD7521LD AD7531LD	AD7520UD AD7521UD

ABSOLUTE MAXIMUM RATINGS (T_A = 25° C unless otherwise noted)

V+	+17V
V_{REF}	±25V
Digital Input Voltage Range	V^+ to GND
Output Voltage Compliance	−100mV to V^+
Power Dissipation (package)	
up to +75°C	450 mW
derate above +75°C @	6 mW/°C
Operating Temperatures	
JN, KN, LN Versions	0°C to +70°C
JD, KD, LD Versions	−25°C to 85°C
SD, TD, UD Versions	−55°C to +125°C
Storage Temperature	−65°C to +150°C

CAUTION: 1) The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{fb}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, TA = 25°C unless otherwise specified)

PARAMETER		AD7520 (AD7530)	AD7521 (AD7531)	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1) Resolution		10	12	Bits			
Nonlinearity	J S	0.2 (8-Bit)		% of FSR	Max	S, T, U: over −55°C to =125°C	1
	K T	0.1 (9-Bit)		% of FSR	Max		1
	L U	0.05 (10-Bit)		% of FSR	Max	$-10V \le V_{REF} \le = 10V$	1
Nonlinearity Tempco		2		PPM of FSR/°C	Max	$-10V \le V_{REF} \le +10V$	
Gain Error (Note 2)		0.3		% of FSR	Typ		
Gain Error Tempco (Note 2)		10		PPM of FSR/°C	Max		
Output Leakage Current (either output)		200 (300)		nA	Max	Over the specified temperature range	
Power Supply Rejection		±0.005		% of FSR/%	Typ		2
AC ACCURACY Output Current Settling Time		500		nS	Typ	To 0.05% of FSR (All digital inputs low to high and high to low)	6
Feedthrough Error		10		mV pp	Max	V_{REF} = 20V pp, 100kHz (50kHz) All digital inputs low	5
REFERENCE INPUT Input Resistance (Note 3)		5k 10k 20k		Ω	Min Typ Max	All digital inputs high. I_{OUT1} at ground.	
ANALOG OUTPUT Voltage Compliance (both outputs)		See absolute max. ratings					
Output Capacitance		I_{OUT1} 120 I_{OUT2} 37		pF pF	Typ Typ	All digital inputs high	4
		I_{OUT1} 37 I_{OUT2} 120		pF pF	Typ Typ	All digital inputs low	4
Output Noise (both outputs)		Equivalent to 10kΩ Johnson noise			Typ		3
DIGITAL INPUTS Low State Threshold		0.8		V	Max	Over the specified temp range	
High State Threshold		2.4		V	Min		
Input Current (low to high state)		1		μA	Typ		
Input Coding		Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5	
POWER REQUIREMENTS Power Supply Voltage Range		+5 to +15		V			
I^+		5		nA	Typ	All digital inputs at GND	
		2		mA	Max	All digital inputs high or low	
Total Power Dissipation (Including the ladder)		20		mW	Typ		

NOTES:

1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Ladder and feedback resistor Tempco is approximately −150ppm/°C.

TEST CIRCUITS

NOTE: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7530, AD7521 and AD7531.

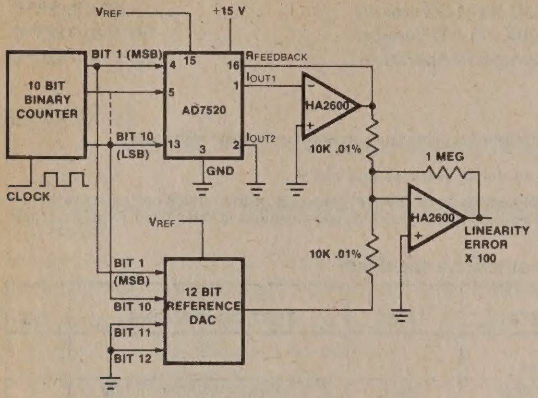

VREF
+15 V
BIT 1 (MSB)
10 BIT BINARY COUNTER
4
15
16
RFEEDBACK
5
1
IOUT1
AD7520
HA2600
BIT 10 (LSB)
13
3
2
IOUT2
10K .01%
GND
1 MEG
CLOCK
HA2600
LINEARITY ERROR X 100
VREF
10K .01%
BIT 1 (MSB)
12 BIT REFERENCE DAC
BIT 10
BIT 11
BIT 12

Figure 1. Nonlinearity

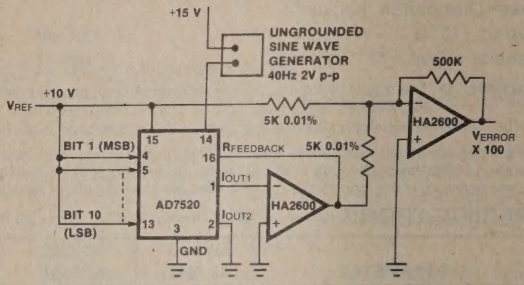

+15 V
UNGROUNDED SINE WAVE GENERATOR 40Hz 2V p-p
500K
+10 V
VREF
5K 0.01%
HA2600
VERROR X 100
BIT 1 (MSB)
15
14
4
16
RFEEDBACK
5K 0.01%
5
IOUT1
1
AD7520
HA2600
BIT 10 (LSB)
13
3
2
IOUT2
GND

Figure 2. Power Supply Rejection

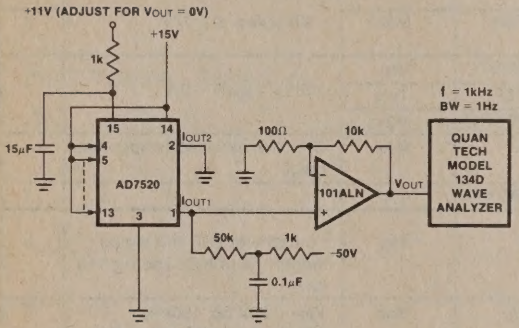

+11V (ADJUST FOR VOUT = 0V)
+15V
1k
f = 1kHz
BW = 1Hz
15
14
IOUT2
100Ω
10k
QUAN TECH MODEL 134D WAVE ANALYZER
15μF
4
2
5
AD7520
101ALN
VOUT
IOUT1
13
3
1
50k
1k
-50V
0.1μF

Figure 3. Noise

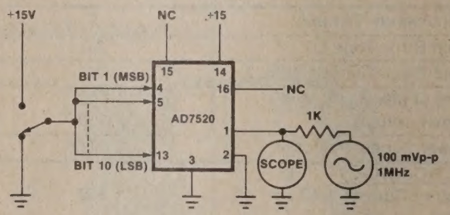

+15V
NC
+15
BIT 1 (MSB)
15
14
4
16
NC
5
AD7520
1K
1
BIT 10 (LSB)
13
3
2
SCOPE
100 mVp-p 1MHz

Figure 4. Output Capacitance

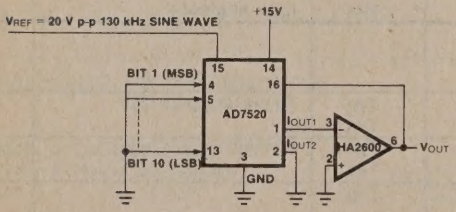

VREF = 20 V p-p 130 kHz SINE WAVE
+15V
BIT 1 (MSB)
15
14
4
16
5
AD7520
1
IOUT1
3
BIT 10 (LSB)
13
3
2
IOUT2
2
HA2600
6
VOUT
GND

Figure 5. Feedthrough Error

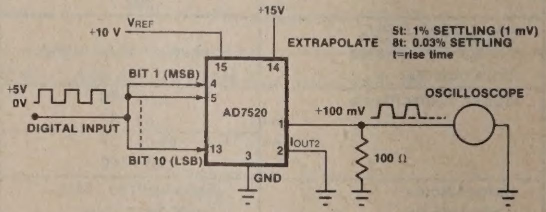

+15V
+10 V
VREF
EXTRAPOLATE
5t: 1% SETTLING (1 mV)
8t: 0.03% SETTLING
t=rise time
BIT 1 (MSB)
15
14
4
+5V
0V
5
OSCILLOSCOPE
AD7520
+100 mV
DIGITAL INPUT
1
13
3
2
IOUT2
100 Ω
BIT 10 (LSB)
GND

Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire VREF range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from VREF to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from IOUT1 and IOUT2 terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on IOUT1 terminal with all digital inputs LOW or on IOUT2 terminal when all inputs are HIGH.

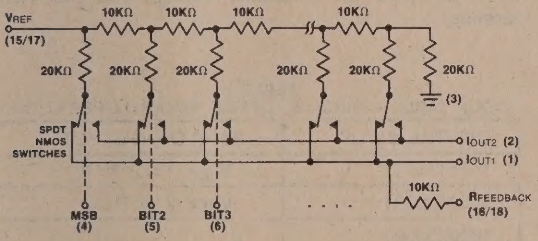
GENERAL CIRCUIT INFORMATION

The AD7520 (AD7530) and AD7521 (AD7531) are monolithic, multiplying D/A converters. Highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} busses which must be held either at ground or virtual ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.



(Switches shown for Digital Inputs "High")

Figure 7. 7520/7521 Functional Diagram

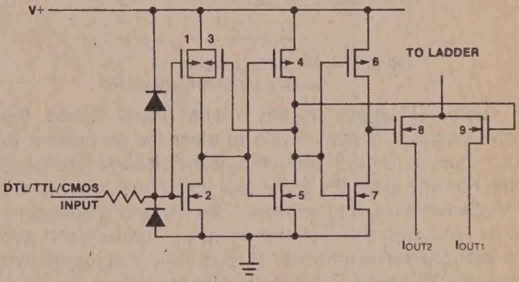


Figure 8. CMOS Switch

APPLICATIONS

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7520 (AD7530) and AD7521 (AD7531) in unipolar mode is shown in Figure 9. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

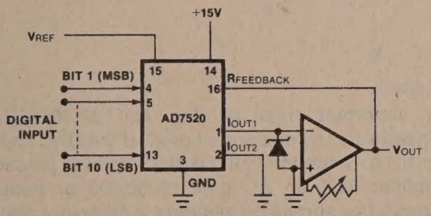


Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1 mV at V_{OUT}.

Gain Adjustment

1. Connect all AD7520 (AD7530) or AD7521 (AD7531) digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}\,(1\text{-}2^{-n})$ reading. ($n=10$ for AD7520 (AD7530) and $n=12$ for AD7521 (AD7531)).
3. To decrease V_{OUT}, connect a series resistor (0 to 500 ohms) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT}, connect a series resistor (0 to 500) ohms) in the I_{OUT_1} amplifier feedback loop.

TABLE 1

CODE TABLE — UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\,(1-2^{-n})$
1000000001	$-V_{REF}\,(1/2+2^{-n})$
1000000000	$-V_{REF}\,/\,2$
0111111111	$-V_{REF}\,(1/2-2^{-n})$
0000000001	$-V_{REF}\,(2^{-n})$
0000000000	0

NOTE: 1. LSB $=2^{-n}\,V_{REF}$

2. n = 10 for 7520, 7521
n = 12 for 7530, 7531

(APPLICATIONS, Cont'd.)

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7520 (AD7530) or AD7521 (AD7531) in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

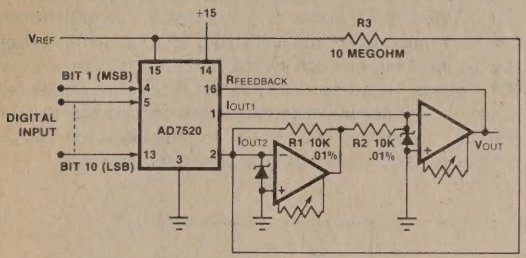


Figure 10. Bipolar Operation (4-Quadant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 Megohm), from V_{REF} to I_{OUT2}.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset zero adjust trimpot for 0V ±1 mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}(1-2^{-(n-1)})$ volts reading. (n = 10 for AD7520 and AD7530, and n = 12 for AD7521 and AD7531).
3. To increase V_{OUT}, connect a series resistor of up to 500Ω between V_{OUT} and R_{fb}.
4. To decrease V_{OUT}, connect a series resistor of up to 500Ω between the reference voltage and the V_{REF} terminal.

TABLE 2
CODE TABLE — BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-(n-1)})$
1000000001	$-V_{REF}(2^{-(n-1)})$
1000000000	0
0111111111	$V_{REF}(2^{-(n-1)})$
0000000001	$V_{REF}(1-2^{-(n-1)})$
0000000000	V_{REF}

NOTE: 1. LSB = $2^{-(n-1)} V_{REF}$

2. n = 10 for 7520 and 7521
n = 12 for 7530 and 7531

POWER DAC DESIGN USING AD7520

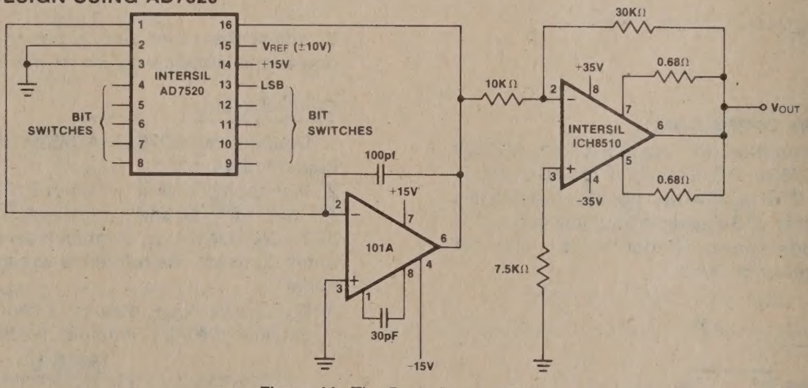


Figure 11. The Basic Power DAC

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 11. An INTERSIL IH8510 power amplifier (1 Amp continuous output at up to ±25 V) is driven by the AD7520.

A summing amplifier between the AD7520 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise the AD7520 can be directly connected to the IH8510, by using a 25 V reference for the DAC.

An important note on the AD7520/101A interface concerns the connection of pin 1 of the DAC and pin 2 of the 101A. Since this point is the summing junction of an amplifier with an AC gain of 50,000 or better, stray capacitance should be minimized; otherwise instabilities and poor noise performance will result. Note that the output of the 101A is fed into an inverting amplifier with a gain of -3, which can be easily changed to a non-inverting configuration. (For more information see: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

(APPLICATIONS, Cont'd.)

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 12, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (±1 LSB).

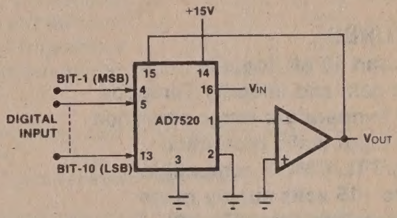


Figure 12. Analog/Digital Divider

INTERSIL

AD7523
8 Bit Monolithic Multiplying D/A Converters

FEATURES

- **8, 9 and 10 bit linearity**
- **Low gain and linearity Tempcos**
- **Full temperature range operation**
- **Full input static protection**
- **DTL/TTL/CMOS compatible**
- **+5 to +15 volts supply range**
- **Fast settling time: 100 nS**
- **Four quadrant multiplication**
- **883B Processed versions available**

GENERAL DESCRIPTION

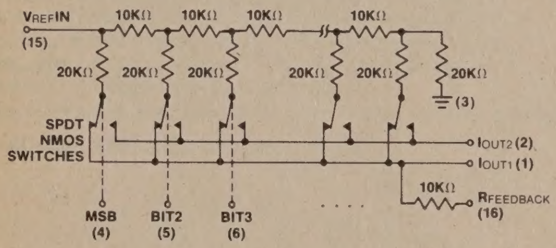
The Intersil AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Intersil's thin-film resistors on CMOS circuitry provide 8-bit resolution (8, 9 and 10-bit accuracy), with DTL/TTL/CMOS compatible operation.

Intersil AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND and very low power dissipation make it a very versatile converter.

Low noise audio gain control, motor speed control, digitally controlled gain and attenuators are a few of the wide number of applications of the 7523.

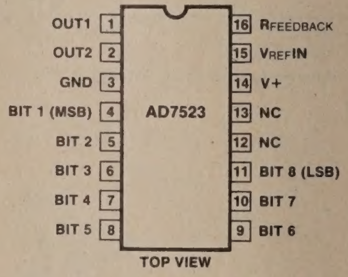
FUNCTIONAL DIAGRAM



VREFIN
(15)
10KΩ
10KΩ
10KΩ
10KΩ
20KΩ
20KΩ
20KΩ
20KΩ
20KΩ
20KΩ
(3)
SPDT
NMOS
SWITCHES
IOUT2 (2)
IOUT1 (1)
10KΩ
RFEEDBACK
(16)
MSB
(4)
BIT2
(5)
BIT3
(6)

(Switches shown for Digital Inputs "High")

PIN CONFIGURATION



OUT1 1
OUT2 2
GND 3
BIT 1 (MSB) 4
BIT 2 5
BIT 3 6
BIT 4 7
BIT 5 8
AD7523
16 RFEEDBACK
15 VREFIN
14 V+
13 NC
12 NC
11 BIT 8 (LSB)
10 BIT 7
9 BIT 6
TOP VIEW

OUTLINE DRAWINGS
DE,PE

ORDERING INFORMATION

Nonlinearity	Temperature Range 0°C to +70°C	 −20°C to +85°C	 −55°C to +125°C
0.2% (8 Bit)	AD7523JN	AD7523AD	AD7523SD
0.1% (9 Bit)	AD7523KN	AD7523BD	AD7523TD
0.05% (10 Bit)	AD7523LN	AD7523CD	AD7523UD

AD7523 T D

Package
D — 18-Pin Ceramic DIP
N — 18-Pin Plastic DIP

Nonlinearity and Temperature Range
J, K, L — Commercial
0°C to +70°C
A,B,C — Industrial
−20°C to +85°C
S,T,U — Military
−55°C to +125°C

Basic Part Number

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V^+	+17V
V_{REF}	±25V
Digital Input Voltage Range	–0.3 to VDD
Output Voltage Compliance	–0.3 to VDD
Power Dissipation (package)	
Plastic	
up to +70°C	670mW
derates above +70°C by	8.3mW/°C
Ceramic	
up to 75°C	450mW
derates above 75°C by	6mW/°C
Operating Temperatures	
JN, KN, LN Versions	0°C to +70°C
AD, BD, CD Versions	–25°C to +85°C
SD, TD, UD Versions	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2. Do not apply voltages higher than VDD and lower than GND to any terminal except V_{REF} + R_{FB}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

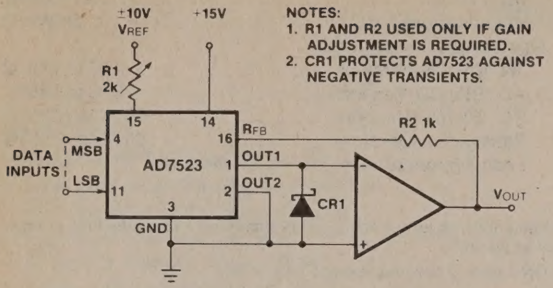
SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V unless otherwise specified)

PARAMETER		TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1) Resolution		8	8	Bits	Min	
Nonlinearity (Note 2)	(±1/2 LSB)	±0.2	±0.2	% of FSR	Max	$-10V \le V_{REF} \le +10V$ $V_{OUT1} = V_{OUT2} = 0V$
	(±1/4 LSB)	±0.1	±0.1	% of FSR	Max	
	(±1/8 LSB)	±0.05	±0.05	% of FSR	Max	
Monotonicity		Guaranteed				
Gain Error (Note 2)		±1.5	±1.8	% of FSR	Max	Digital inputs high.
Nonlinearity Tempco (Note 2 and 3)		2		PPM of FSR/°C	Max	$-10V$ V_{REF} $+10V$
Gain Error Tempco (Note 2 and 3)		10		PPM of FSR/°C	Max	
Output Leakage Current (either output)		±50	±200	nA	Max	$V_{OUT1} = V_{OUT2} = 0$
AC ACCURACY (Note 3) Power Supply Rejection (Note 2)		0.02	0.03	% of FSR/%	Max	V^+ = 14.0 to 15.0V
Output Current Settling Time		150	200	nS	Max	To 0.2% of FSR, R_L = 100Ω
Feedthrough Error		±1/2	±1	LSB	Max	V_{REF} = 20V pp, 200KHz sine wave. All digital inputs low.
REFERENCE INPUT		5K		Ω	Min	All digital inputs high. I_{OUT1} at ground.
Input Resistance (Pin 15)		20K			Max	
Temperature Coefficient (Note 3)		–500		ppm/°C	Max	
ANALOG OUTPUT (Note 3) Voltage Compliance (Note 4)		–100mV to V^+				Both outputs. See maximum ratings.
Output Capacitance	C_{OUT1}	100		pF	Max	All digital inputs high (VINH)
	C_{OUT2}	30		pF	Max	
	C_{OUT1}	30		pF	Max	All digital inputs low (VINL)
	C_{OUT2}	100		pF	Max	
DIGITAL INPUTS Low State Threshold (V_{INL})		0.8		V	Max	Guarantees DTL/TTL and CMOS (0.5 max, 14.5 min) levels
High State Threshold (V_{INH})		2.4		V	Min	
Input Current (per input)		±1		μA	Max	V_{IN} = 0V or +15V
Input Coding		Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)		4		pF	Max	
POWER REQUIREMENTS Power Supply Voltage Range		+5 to +16		V		Accuracy is tested and guaranteed at V^+ = +15V, only.
I^+		100		μA	Max	All digital inputs low or high.

NOTES:
1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

APPLICATIONS
UNIPOLAR OPERATION


±10V
VREF
+15V
R1
2k
15
14
RFB
16
4
MSB
DATA INPUTS
LSB
11
AD7523
1
OUT1
2
OUT2
3
GND
CR1
R2 1k
VOUT

NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. CR1 PROTECTS AD7523 AGAINST NEGATIVE TRANSIENTS.

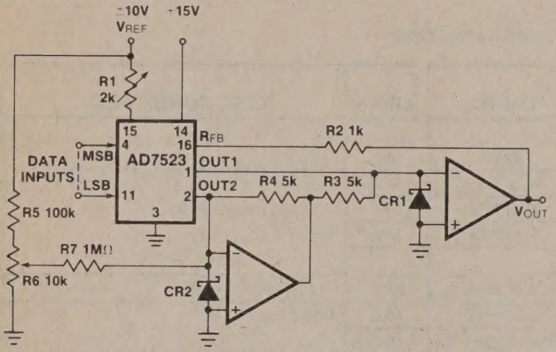
Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{255}{256}\right)$
10000001	$-V_{REF}\left(\frac{129}{256}\right)$
10000000	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$
00000001	$-V_{REF}\left(\frac{1}{256}\right)$
00000000	$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: 1 LSB = $(2^{-8})(V_{REF}) = \left(\frac{1}{256}\right)(V_{REF})$

Table 1. Unipolar Binary Code Table

BIPOLAR OPERATION


±10V
+15V
VREF
R1
2k
15
14
RFB
16
4
MSB
DATA INPUTS
LSB
11
AD7523
1
OUT1
2
OUT2
3
R5 100k
R2 1k
R4 5k
R3 5k
CR1
VOUT
R7 1MΩ
R6 10k
CR2

NOTES:
1. R3/R4 MATCH 0.1% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. R5-R7 USED TO ADJUST VOUT = 0V AT INPUT CODE 10000000.
4. CR1 & CR2 PROTECT AD7523 AGAINST NEGATIVE TRANSIENTS.

Figure 2. Bipolar (4-Quadrant) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{127}{128}\right)$
10000001	$-V_{REF}\left(\frac{1}{128}\right)$
10000000	0
01111111	$+V_{REF}\left(\frac{1}{128}\right)$
00000001	$+V_{REF}\left(\frac{127}{128}\right)$
00000000	$+V_{REF}\left(\frac{128}{128}\right)$

Note: 1LSB = $(2^{-7})(V_{REF}) = \left(\frac{1}{128}\right)(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

POWER DAC DESIGN USING AD7523

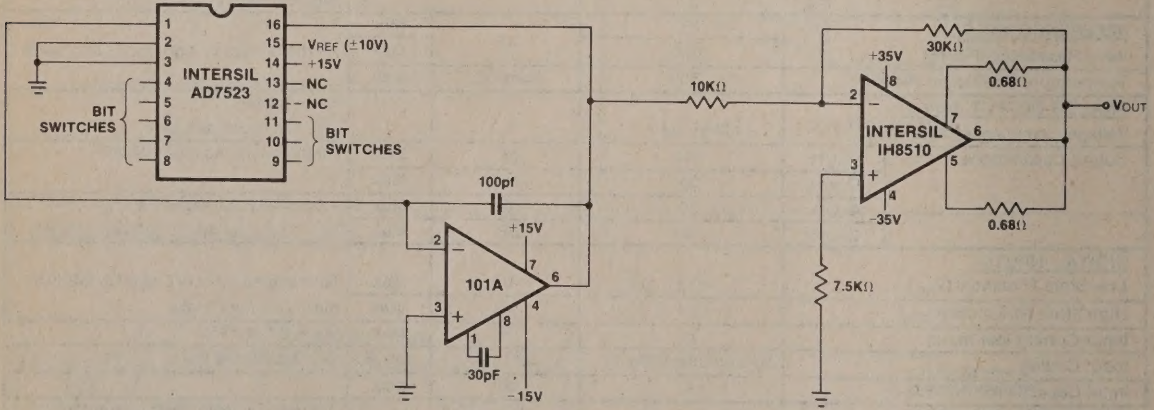

1
2
3
4
5
6
7
8
INTERSIL
AD7523
16
15
14
13
12
11
10
9
VREF (±10V)
+15V
NC
NC
BIT SWITCHES
BIT SWITCHES
100pf
+15V
2
3
101A
7
6
4
8
1
30pF
−15V
10KΩ
+35V
30KΩ
0.68Ω
2
8
INTERSIL
IH8510
7
6
5
3
4
−35V
0.68Ω
VOUT
7.5KΩ

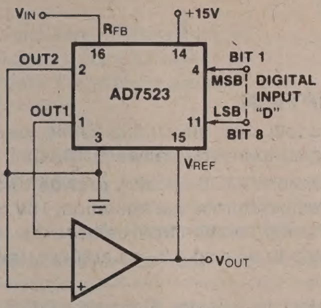
Figure 3. The Basic Power DAC

A typical power DAC designed for 10 bit accuracy and 8 bit resolution is shown in Figure 3. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the AD7523.

A summing amplifier between the AD7523 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7523 can be directly connected to the IH8510, by using a 25 volts reference for the DAC.

APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



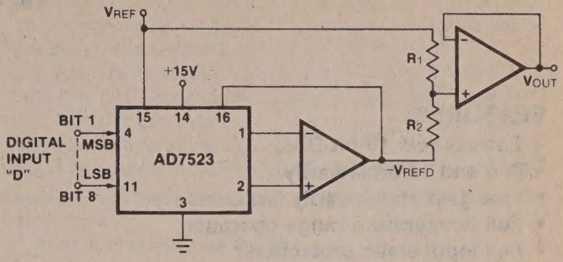
$V_{OUT} = -V_{IN}/D$

WHERE:

$$D = \frac{BIT1}{2^1} + \frac{BIT2}{2^2} + \dots \frac{BIT8}{2^8}$$

$$\left(0 \le D \le \frac{255}{256}\right)$$

MODIFIED SCALE FACTOR AND OFFSET



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1+R_2}\right) - \left(\frac{R_1 D}{R_1+R_2}\right)\right] \quad \text{WHERE: } D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \dots \frac{BIT\ 8}{2^8}$$

$$\left(0 \le D \le \frac{255}{256}\right)$$

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

For further information on the use of this device, see the following Application Bulletins:

A016 "Selecting A/D Converters," by David Fullagar
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A020 "A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger
A021 "Power D/A Converters Using the IH8510," by Dick Wilenken
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al., Electronics, Dec. 9, 1976

AD7533
10 Bit Monolithic Multiplying D/A Converters

FEATURES

- **Lowest cost 10-bit DAC**
- **8, 9 and 10 bit linearity**
- **Low gain and linearity Tempcos**
- **Full temperature range operation**
- **Full input static protection**
- **DTL/TTL/CMOS direct interface**
- **+5 to +15 volts supply range**
- **Low power dissipation**
- **Fast settling time**
- **Four quadrant multiplication**
- **Direct AD7520 equivalent**
- **883B Processed versions available**

GENERAL DESCRIPTION

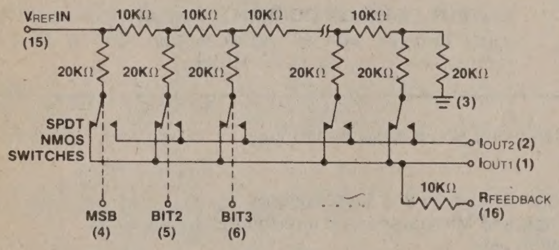
The Intersil AD7533 is a low cost, monolithic 10-bit, four-quadrant multiplying digital-to-analog converter (DAC).

Intersil's thin-film resistors on CMOS circuitry provide 10, 9 and 8 bit accuracy, full temperature range operation, +5V to +15V power range, full input protection from damage due to static discharge by clamps to V+ and ground and very low power dissipation.

Pin and function equivalent to Industry Standard AD7520, the AD7533 is recommended as a lower cost alternative for old or new 10-bit DAC designs.

Application of AD7533 includes programmable gain amplifiers, digitally controlled attenuators, function generators and control systems.

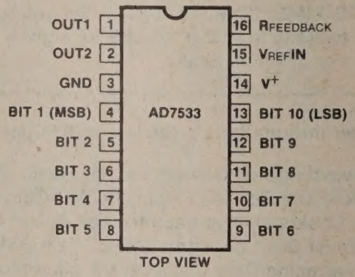
FUNCTIONAL DIAGRAM



VREFIN
(15)
10KΩ
10KΩ
10KΩ
10KΩ
20KΩ
20KΩ
20KΩ
20KΩ
20KΩ
20KΩ
(3)
SPDT
NMOS
SWITCHES
IOUT2 (2)
IOUT1 (1)
10KΩ
RFEEDBACK
(16)
MSB
(4)
BIT2
(5)
BIT3
(6)

(Switches shown for Digital Inputs "High")

PIN CONFIGURATION



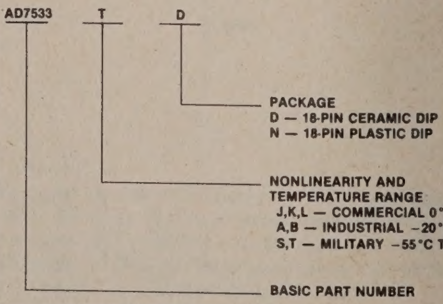
OUT1 1
OUT2 2
GND 3
BIT 1 (MSB) 4
BIT 2 5
BIT 3 6
BIT 4 7
BIT 5 8
AD7533
16 RFEEDBACK
15 VREFIN
14 V+
13 BIT 10 (LSB)
12 BIT 9
11 BIT 8
10 BIT 7
9 BIT 6
TOP VIEW

(Outline dwg DE, PE)

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	−20°C to +85°C	−55°C to +125°C
±0.2% (8-bit)	AD7533JN	AD7533AD	AD7533SD
±0.1% (9-bit)	AD7533KN	AD7533BD	AD7533TD
±0.05% (10-bit)	AD7533LN	AD7533CD	AD7533UD

PACKAGE IDENTIFICATION



AD7533
T
D
PACKAGE
D — 18-PIN CERAMIC DIP
N — 18-PIN PLASTIC DIP
NONLINEARITY AND
TEMPERATURE RANGE
J,K,L — COMMERCIAL 0°C TO +70°C
A,B — INDUSTRIAL −20°C TO +85°C
S,T — MILITARY −55°C TO +125°C
BASIC PART NUMBER

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V^+	−0.3V, +17V
V_{REF}	±25V
Digital Input Voltage Range	−0.3V to V^+
Output Voltage Compliance	−0.3 to V^+
Power Dissipation (package)	
Ceramic	
up to +75°C	450mW
derates above +75°C by	6mW/°C
Plastic	
up to 70°C	670mW
derates above 70°C by	8.3mW/°C
Operating Temperatures	
JN, KN, LN Versions	0°C to +70°C
AD, BD, CD Versions	−25°C to +85°C
SD, TD, UD Versions	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2. Do not apply voltages lower than ground or higher than V^+ to any pin except V_{REF} and R_{FB}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2} = 0$ unless otherwise specified.)

PARAMETER	T_A +25°C	T_A MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1) Resolution	10	10	Bits	Min	
Nonlinearity (Note 2)	±0.2	±0.2	% of FSR	Max	
	±0.1	±0.1	% of FSR	Max	$-10V \leq V_{REF} \leq +10V$
	±0.05	±0.05	% of FSR	Max	$V_{OUT1} = V_{OUT2} = 0V$
Gain Error (Note 2 and 5)	±1.4	±1.5	% of FS	Max	Digital Inputs = V_{INH}
Output Leakage Current (either output)	±50	±200	nA	Max	V_{REF} = ±10V
AC ACCURACY Power Supply Rejection (Note 2 and 3)	0.005	0.008	% of FSR/%	Max	V^+ = 14.0 to 17.0V
Output Current Settling Time	600 (Note 6)	800 (Note 3)	nS	Max	To 0.05% of FSR, R_L = 100Ω
Feedthrough Error (Note 3)	±0.05	±0.1	% FSR	Max	V_{REF} = ±10V, 100kHz sine wave. Digital inputs low.
REFERENCE INPUT	5K			Min	All digital inputs high.
Input Resistance (Pin 15)	20K		Ω	Max	
Temperature Coefficient	−300		ppm/°C	Typ	
ANALOG OUTPUT Voltage Compliance (Note 4)	−100mV to V^+				Both outputs. See maximum ratings.
Output Capacitance (Note 3) C_{OUT1}	100		pF	Max	All digital inputs high (V_{INH})
C_{OUT2}	35		pF	Max	
C_{OUT1}	35		pF	Max	All digital inputs low (V_{INL})
C_{OUT2}	100		pF	Max	
DIGITAL INPUTS Low State Threshold (VINL)	0.8		V	Max	
High State Threshold (VINH)	2.4		V	Min	
Input Current (I_{IN})	±1		μA	Max	V_{IN} = 0V and V^+
Input Coding	Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)	5		pF	Max	
POWER REQUIREMENTS V_{DD}	+15 ±10%		V		Rated Accuracy
Power Supply Voltage Range	+5 to +16		V		
I^+	2		mA	Max	Digital Inputs = V_{INL} to V_{INH}
	100	150	μA	Max	Digital Inputs = 0V or V^+

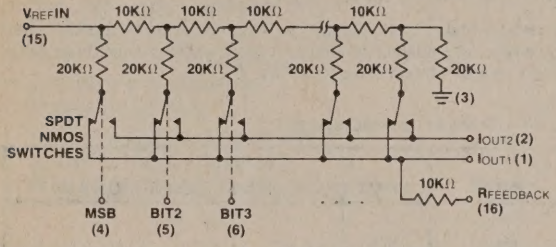
NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.
5. Full scale (FS) = − (V_{REF}) • (1023/1024)
6. Sample tested to ensure specification compliance.
7. 100% screened to MIL-STD-883, method 5004, para. 3.1.1. through 3.1.12 for class B device. Final electrical tests are: Nonlinearity, Gain Error, Output Leakage Current, V_{INH}, V_{INL}, I_{IN} and I^+ @ +25°C and +125°C (SD, TD, UD) or +25°C and +85°C (AD, BD, CD).

Specifications subject to change without notice.

GENERAL CIRCUIT INFORMATION

The Intersil AD7533 is a 10 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 1. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.


VREF IN
(15)
10KΩ
10KΩ
10KΩ
10KΩ
20KΩ
20KΩ
20KΩ
20KΩ
20KΩ
20KΩ
(3)
SPDT
NMOS
SWITCHES
IOUT2 (2)
IOUT1 (1)
10KΩ
RFEEDBACK
(16)
MSB
(4)
BIT2
(5)
BIT3
(6)
. . . .

(Switches shown for Digital Inputs "High")

Figure 1

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 2). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors resulting in accurate leg currents.

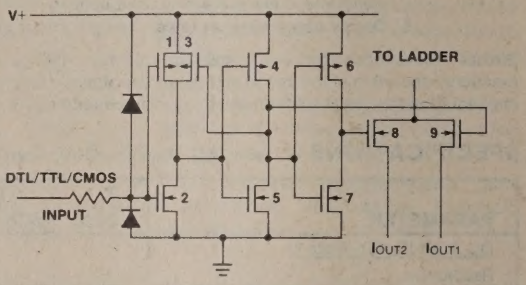
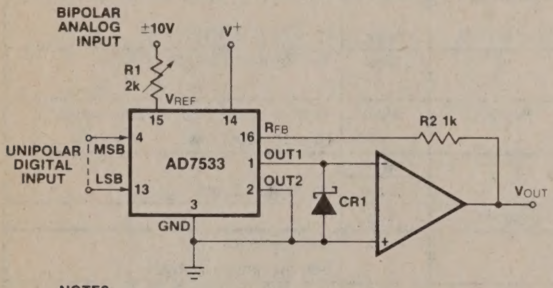

V+
1
3
4
6
TO LADDER
8
9
DTL/TTL/CMOS
INPUT
2
5
7
IOUT2
IOUT1

Figure 2

APPLICATIONS

UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)


BIPOLAR
ANALOG
INPUT
±10V
V+
R1
2k
VREF
15
14
RFB
R2 1k
4
16
UNIPOLAR
DIGITAL
INPUT
MSB
LSB
AD7533
OUT1
1
OUT2
2
13
3
CR1
VOUT
GND

NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. SCHOTTKY DIODE CR1 (HP5082-2811 OR EQUIV) PROTECTS OUT1 TERMINAL AGAINST NEGATIVE TRANSIENTS.

Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (VOUT as shown in Figure 3)
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:
1. Nominal Full Scale for the circuit of Figure 3 is given by

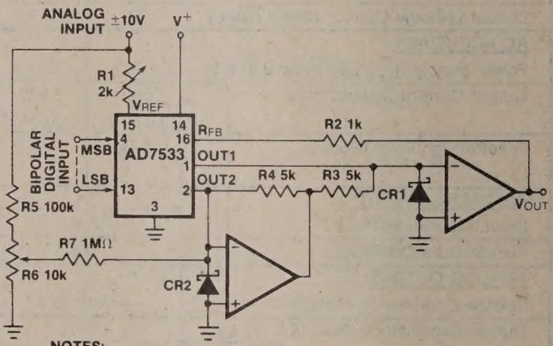
$$FS = -V_{REF}\left(\frac{1023}{1024}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 3 is given by

$$LSB = V_{REF}\left(\frac{1}{1024}\right)$$

Table 1. Unipolar Binary Code

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)


ANALOG
INPUT
±10V
V+
R1
2k
VREF
15
14
RFB
R2 1k
4
16
BIPOLAR
DIGITAL
INPUT
MSB
LSB
AD7533
OUT1
1
OUT2
2
13
3
R4 5k
R3 5k
CR1
VOUT
R5 100k
R7 1MΩ
R6 10k
CR2

NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. SCHOTTKY DIODES CR1 AND CR2 (HP5082-2811 OR EQUIV) PROTECT OUT1 AND OUT2 TERMINALS FROM NEGATIVE TRANSIENTS

Figure 4. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (VOUT as shown in Figure 4)
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

NOTES:
1. Nominal Full Scale Range for the circuit of Figure 4 is given by

$$FSR = V_{REF}\left(\frac{1023}{512}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 4 is given by

$$LSB = V_{REF}\left(\frac{1}{512}\right)$$

Table 2. Bipolar (Offset Binary) Code Table

POWER DAC DESIGN USING AD7533

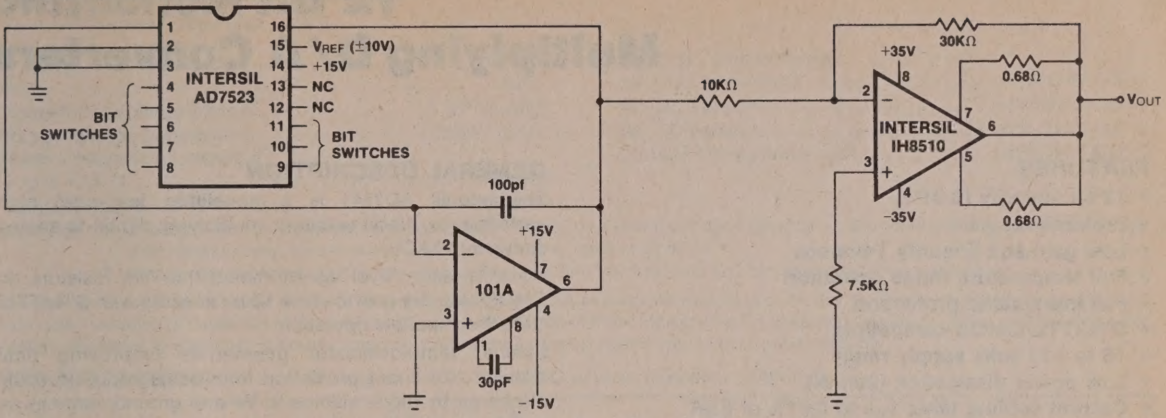
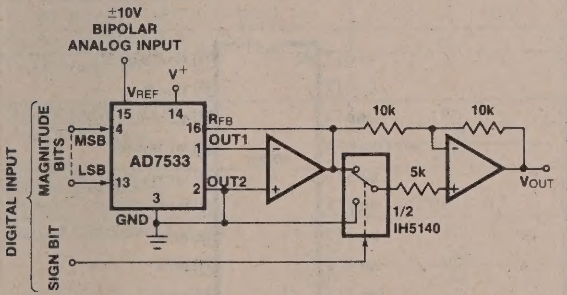

INTERSIL
AD7523
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VREF (±10V)
+15V
NC
NC
BIT SWITCHES
BIT SWITCHES
100pf
+15V
101A
30pF
-15V
10KΩ
30KΩ
+35V
0.68Ω
INTERSIL
IH8510
-35V
0.68Ω
VOUT
7.5KΩ

Figure 5. The Basic Power DAC

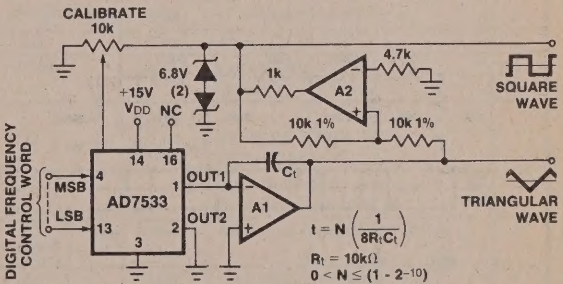
A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 5. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the AD7533.

A summing amplifier between the AD7533 and the IH8510 is used to separate the gain block containing the AD7533 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7533 can be directly connected to the IH8510, by using a 25 volts reference for the DAC. Notice that the output of the 101A is fed into an inverting amplifier with a gain of −3, which can be easily changed to a non-inverting configuration. (For more information write for: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

10-BIT AND SIGN MULTIPLYING DAC


±10V
BIPOLAR
ANALOG INPUT
V+
VREF
15
14
16
RFB
OUT1
MSB
LSB
AD7533
13
OUT2
GND
3
10k
10k
5k
VOUT
1/2
IH5140
DIGITAL INPUT
MAGNITUDE BITS
SIGN BIT

PROGRAMMABLE FUNCTION GENERATOR


CALIBRATE
10k
6.8V
(2)
+15V
VDD
NC
1k
4.7k
A2
SQUARE WAVE
10k 1%
10k 1%
14
16
OUT1
Ct
MSB
AD7533
OUT2
A1
LSB
13
3
TRIANGULAR WAVE
DIGITAL FREQUENCY CONTROL WORD
t = N (1 / 8RtCt)
Rt = 10kΩ
0 < N ≤ (1 - 2-10)

INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.

AD7541
12 Bit Monolithic Multiplying D/A Converters

FEATURES

- **12 bit linearity (0.01%)**
- **Pretrimmed gain**
- **Low gain and linearity Tempcos**
- **Full temperature range operation**
- **Full input static protection**
- **DTL/TTL/CMOS compatible**
- **+5 to +15 volts supply range**
- **Low power dissipation (20mW)**
- **Current settling time: 1μs to 0.01% of FSR**
- **Four quadrant multiplication**
- **883B Processed versions available**

GENERAL DESCRIPTION

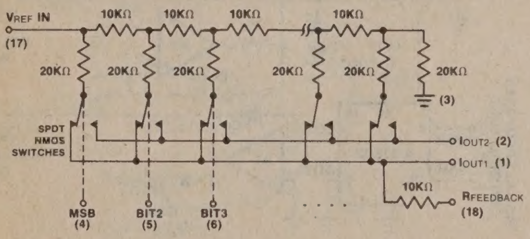
The Intersil AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Intersil's wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with DTL/TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Intersil AD7541.

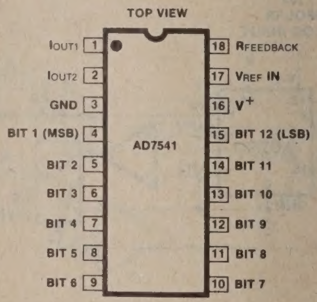
Pin compatible with AD7521, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

FUNCTIONAL DIAGRAM


VREF IN
(17)
10KΩ
10KΩ
10KΩ
10KΩ
20KΩ
20KΩ
20KΩ
20KΩ
20KΩ
20KΩ
(3)
SPDT
NMOS
SWITCHES
IOUT2 (2)
IOUT1 (1)
10KΩ
RFEEDBACK
(18)
MSB
(4)
BIT2
(5)
BIT3
(6)

(Switches shown for Digital Inputs "High")

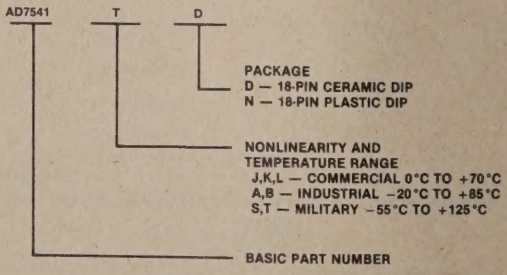
PIN CONFIGURATION


TOP VIEW
IOUT1 1
IOUT2 2
GND 3
BIT 1 (MSB) 4
BIT 2 5
BIT 3 6
BIT 4 7
BIT 5 8
BIT 6 9
AD7541
18 RFEEDBACK
17 VREF IN
16 V+
15 BIT 12 (LSB)
14 BIT 11
13 BIT 10
12 BIT 9
11 BIT 8
10 BIT 7

(Outline dwg DN, PN)

ORDERING INFORMATION

	Temperature Range		
Nonlinearity	**0°C to +70°C**	**-20°C to +85°C**	**-55°C to +125°C**
0.02% (11-bit)	AD7541JN	AD7541AD	AD7541SD
0.01% (12-bit)	AD7541KN	AD7541BD	AD7541TD
0.01% (12-bit) Guaranteed Monotonic	AD7541LN	—	—


AD7541
T
D
PACKAGE
D — 18-PIN CERAMIC DIP
N — 18-PIN PLASTIC DIP
NONLINEARITY AND
TEMPERATURE RANGE
J,K,L — COMMERCIAL 0°C TO +70°C
A,B — INDUSTRIAL -20°C TO +85°C
S,T — MILITARY -55°C TO +125°C
BASIC PART NUMBER

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V^+	+17V
V_{REF}	±25V
Digital Input Voltage Range	V^+ to GND
Output Voltage Compliance	−100mV to V^+
Power Dissipation (package)	
up to +75°C	450mW
derates above +75°C by	6mW/°C

Operating Temperatures	
JN, KN, LN Versions	0°C to +70°C
AD, BD Versions	−20°C to +85°C
SD, TD Versions	−55°C to +125°C
Storage Temperature	−65°C to +150°C

CAUTION 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{fb}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, T_A = 25°C unless otherwise specified)

PARAMETER			TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1) Resolution			12	12	Bits	Min		
Nonlinearity (Note 2)	S	J	±0.020	±0.024	% of FSR	Max	$-10V \le V_{REF} \le +10V$ $V_{OUT1} = V_{OUT2} = 0V$	1
	T	K	±0.010	±0.012	% of FSR	Max		
		L	±0.010	±0.012	% of FSR	Max		
			Guaranteed Monotonic					
Gain Error (Note 2)			±0.3	±0.4	% of FSR	Max	$-10V \le V_{REF} \le +10V$	
Output Leakage Current (either output)			±50	±200	nA	Max	$V_{OUT1} = V_{OUT2} = 0$	
AC ACCURACY (Note 3) Power Supply Rejection (Note 2)			±0.01	±0.02	% of FSR/%	Max	V^+ = 14.5 to 15.5V	2
Output Current Settling Time			1		µS	Max	To 0.01% of FSR	6
Feedthrough Error			1		mV pp	Max	V_{REF} = 20V pp, 10 kHz. All digital inputs low.	5
REFERENCE INPUT Input Resistance			5K		Ω	Min	All digital inputs high. I_{OUT1} at ground.	
			10K			Typ		
			20K			Max		
ANALOG OUTPUT Voltage Compliance (Note 4)			−100mV to V^+				Both outputs. See maximum ratings.	
Output Capacitance (Note 3)	C_{OUT1}		200		pF	Max	All digital inputs high (V_{INH})	4
	C_{OUT2}		60		pF	Max		
	C_{OUT1}		60		pF	Max	All digital inputs low (V_{INL})	4
	C_{OUT2}		200		pF	Max		
Output Noise (both outputs)			Equivalent to 10KΩ Johnson noise			Typ		3
DIGITAL INPUTS Low State Threshold (VINL)			0.8		V	Max		
High State Threshold (VINH)			2.4		V	Min		
Input Current			±1		µA	Max	V_{IN} = 0 or V^+	
Input Coding			Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5.	
Input Capacitance (Note 3)			8		pF	Max		
POWER REQUIREMENTS Power Supply Voltage Range			+5 to +16		V		Accuracy is not guaranteed over this range	
I^+			2		mA	Max	All digital inputs high or low	
Total Power Dissipation (including the ladder)			20		mW	Typ		

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

TEST CIRCUITS

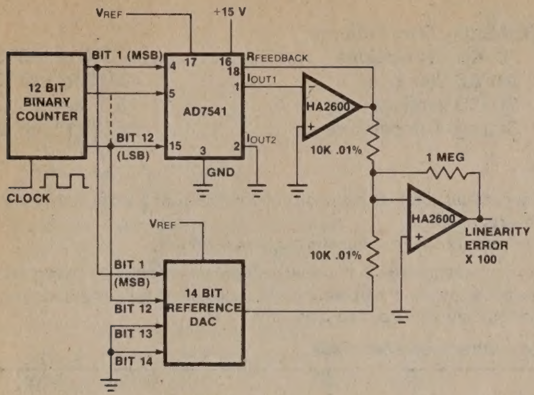

VREF
+15 V
BIT 1 (MSB)
12 BIT BINARY COUNTER
BIT 12 (LSB)
CLOCK
AD7541
RFEEDBACK
IOUT1
IOUT2
GND
HA2600
10K .01%
1 MEG
LINEARITY ERROR X 100
VREF
BIT 1 (MSB)
BIT 12
BIT 13
BIT 14
14 BIT REFERENCE DAC

Figure 1. Nonlinearity

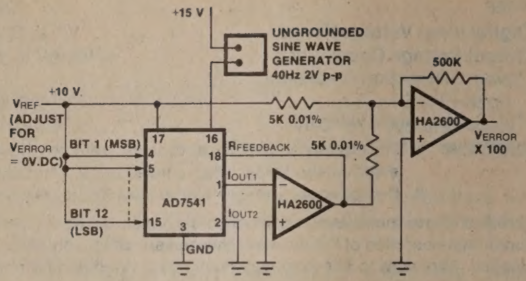

+15 V
UNGROUNDED SINE WAVE GENERATOR 40Hz 2V p-p
500K
+10 V
VREF (ADJUST FOR VERROR = 0V.DC)
5K 0.01%
BIT 1 (MSB)
BIT 12 (LSB)
AD7541
RFEEDBACK
IOUT1
IOUT2
GND
HA2600
VERROR X 100

Figure 2. Power Supply Rejection

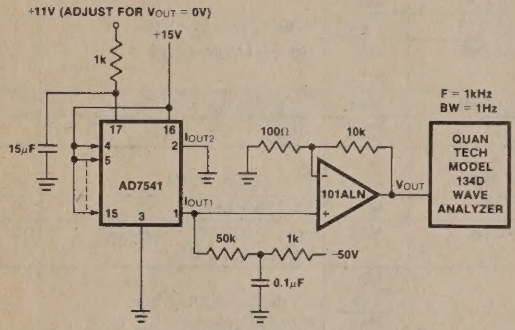

+11V (ADJUST FOR VOUT = 0V)
+15V
1k
15μF
AD7541
IOUT2
IOUT1
100Ω
10k
101ALN
VOUT
F = 1kHz BW = 1Hz
QUAN TECH MODEL 134D WAVE ANALYZER
50k
1k
-50V
0.1μF

Figure 3. Noise

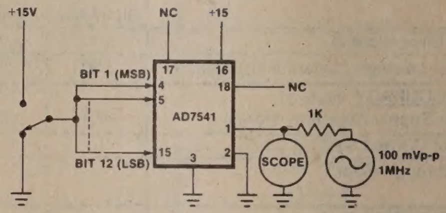

+15V
NC
+15
BIT 1 (MSB)
BIT 12 (LSB)
AD7541
NC
1K
SCOPE
100 mVp-p 1MHz

Figure 4. Output Capacitance

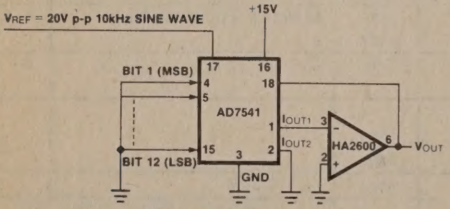

VREF = 20V p-p 10kHz SINE WAVE
+15V
BIT 1 (MSB)
BIT 12 (LSB)
AD7541
IOUT1
IOUT2
GND
HA2600
VOUT

Figure 5. Feedthrough Error

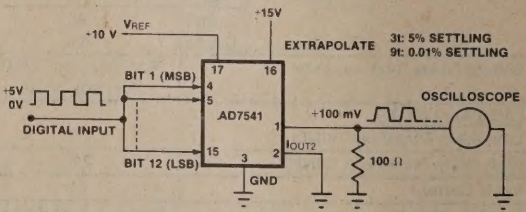

+15V
VREF
+10 V
EXTRAPOLATE
3t: 5% SETTLING
9t: 0.01% SETTLING
BIT 1 (MSB)
+5V
0V
DIGITAL INPUT
BIT 12 (LSB)
AD7541
OSCILLOSCOPE
+100 mV
IOUT2
100 Ω
GND

Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

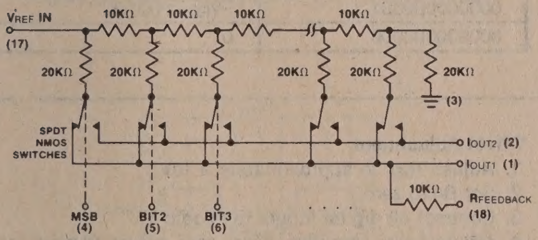
The Intersil AD7541 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.



(Switches shown for Digital Inputs "High")

Figure 7. AD7541 Functional Diagram

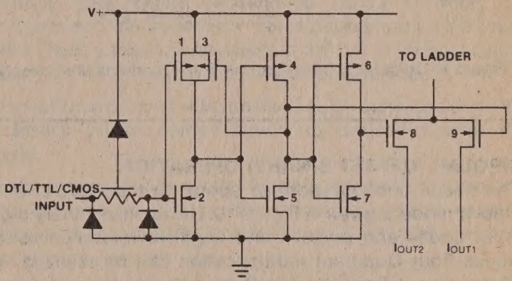


Figure 8. CMOS Switch

APPLICATIONS

General Recommendations

Static performance of the AD7541 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than ±200μV).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V^+ (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor (~1MΩ) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

APPLICATIONS, Continued

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 9. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. Schottky diode (HP 5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

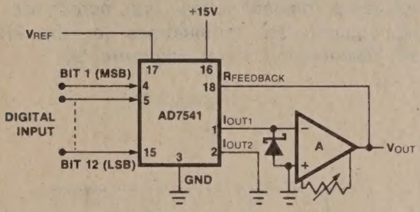


Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}\ (1 - 1/2^{12})$ reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

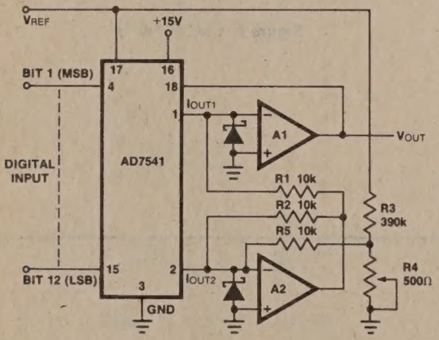
TABLE 1

Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}\ (1 - 1/2^{12})$
100000000001	$-V_{REF}\ (1/2 + 1/2^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF}\ (1/2 - 1/2^{12})$
000000000001	$-V_{REF}\ (1/2^{12})$
000000000000	0

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.



Note: R1 and R2 should be 0.01%, low-TCR resistors.

Figure 10. Bipolar Operation (4-Quadrant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from VREF to IOUT2.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Set R4 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT2} amplifier output.
5. Connect a short circuit across R2.
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT1} amplifier output.
8. Remove short circuit across R2.
9. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R4 for 0V ±0.2mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}\ (1 - 1/2^{11})$ volts reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 2

Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}\ (1 - 1/2^{11})$
100000000001	$-V_{REF}\ (1/2^{11})$
100000000000	0
011111111111	$V_{REF}\ (1/2^{11})$
000000000001	$V_{REF}\ (1 - 1/2^{11})$
000000000000	V_{REF}

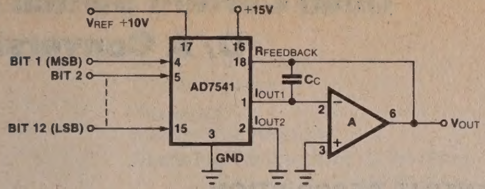


Figure 11. General DAC Circuit with Compensation Capacitor, C_C.

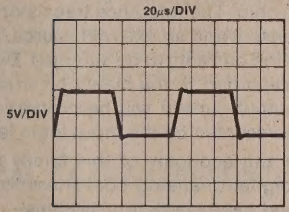


Figure 12. AD7541 Response with: A = Intersil 741HS

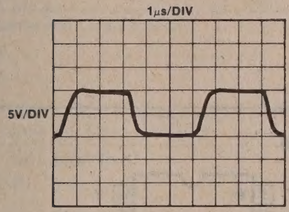


Figure 13. AD7541 Response with: A = Intersil 2515 C_C = 15pF

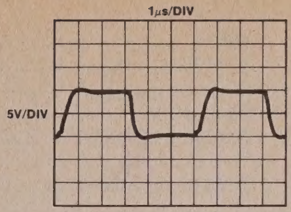


Figure 14. AD7541 Response with: A = Intersil 2520

DYNAMIC PERFORMANCE

The dynamic performance of the DAC, also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, open-loop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the AD7541 looking into I_{OUT1} varies between 10kΩ ($R_{Feedback}$ alone) and 5kΩ ($R_{Feedback}$ in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

Three typical circuits and the resultant waveforms are shown in Figures 11 to 14. A low-cost general purpose (Intersil 741HS), a low-cost high-speed (Intersil 2515) and a high-speed fast-settling (Intersil 2520) amplifier cover the principal application areas.

INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.

INTERSIL

ICL8018A/8019A/8020A
Quad Current Switch for D/A Conversion

FEATURES

- **TTL Compatible: LOW—0.8V**
  HIGH—2.0V
- **12 Bit Accuracy**
- **40 nsec, Switching Speed**
- **Wide Power Supply Range**
- **Low Temperature Coefficient**

APPLICATIONS:

- D/A-A/D Converters
- Digital Threshold Control
- Programmable Voltage Source
- Meter Drive
- X-Y Plotters

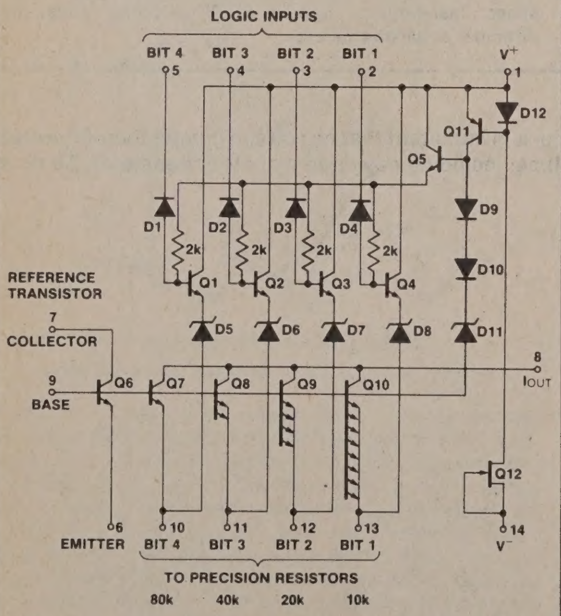
GENERAL DESCRIPTION

The Intersil ICL8018A family are high speed precision current switches for use in current summing digital-to-analog converters. They consist of four logically controlled current switches and a reference device on a single monolithic silicon chip. The reference transistor, combined with precision resistors and an external source, determines the magnitude of the currents to be summed. By weighting the currents in proportion to the binary bit which controls them, the total output current will be proportional to the binary number represented by the input logic levels.

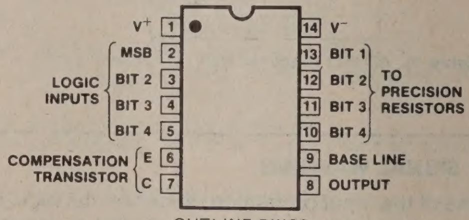
The performance and economy of this family make them ideal for use in digital-to-analog converters for industrial process control and instrumentation systems.

SCHEMATIC DIAGRAM

EQUIVALENT CIRCUIT


LOGIC INPUTS
BIT 4
BIT 3
BIT 2
BIT 1
5
4
3
2
V+
1
D12
Q11
Q5
D9
D1
D2
D3
D4
2k
2k
2k
2k
Q1
Q2
Q3
Q4
D10
REFERENCE TRANSISTOR
7
COLLECTOR
D5
D6
D7
D8
D11
8
IOUT
9
BASE
Q6
Q7
Q8
Q9
Q10
Q12
6
EMITTER
10
BIT 4
11
BIT 3
12
BIT 2
13
BIT 1
14
V−
TO PRECISION RESISTORS
80k
40k
20k
10k

PIN DIAGRAM


V+ 1
MSB 2
LOGIC INPUTS
BIT 2 3
BIT 3 4
BIT 4 5
COMPENSATION TRANSISTOR
E 6
C 7
14 V−
13 BIT 1
12 BIT 2
11 BIT 3
10 BIT 4
TO PRECISION RESISTORS
9 BASE LINE
8 OUTPUT

OUTLINE DWGS
JD, PD

ORDERING INFORMATION

ACCURACY	MILITARY TEMP RANGE CERDIP	COMMERCIAL TEMP RANGE PLASTIC DIP
Individual Devices		
.01%	ICL8018AMJD	ICL8018ACPD
0.1%	ICL8019AMJD	ICL8019ACPD
1.0%	ICL8020AMJD	ICL8020ACPD
Matched Sets*		
.01%	ICL8018AMXJD	ICL8018ACXPD
0.1%	ICL8019AMXJD	ICL8019ACXPD
1.0%	ICL8020AMXJD	ICL8020ACXPD

***NOTE:** Units ordered in equal quantities will be matched such that the V_{be}'s of the 8019 will be within ±10mV of the 8018 compensating transistor, and the V_{be}'s of the 8020 will be within ±50mV. The ICL8018 - X matched sets consist of one 8018, one 8019, and one 8020. The 8019 - X contains one 8019 and one 8020, while the 8020 - X contains two 8020's. Units shipped as matched sets will be marked with a unique set number.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±20V
Logic Input Voltage		−2V to V^+
Output Voltage		$V_{BASELINE}$ to +20V
$V_{BASELINE}$		V^- to +5V
Storage Temperature		−65°C to +150°C
Operating Temperature	ICL8018AM ICL8019AM ICL8020AM	−55°C to +125°C
	ICL8018AC ICL8019AC ICL8010AC	0°C to +70°C
Lead Temperature (soldering 10sec)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($4.5V \le V^+ \le 20V$, $V^- = -15V$, $T_A = 25°C$, V @ pin 6 = −5V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Error					
ICL8018A	$V_{INHI} = 5.0V$			±.01	
ICL8019A	$V_{INLO} = 0.0V$			±0.1	%
ICL8020A				±1	
Error Temperature Coefficient					
ICL8018A			±2	±5	ppm/°C
ICL8019A			±2	±25	
ICL8020A			±2	±50	
Switching Time To Turn On LSB			40		ns
Output Current (Nominal)					
BIT 1 (MSB)			1.0		mA
BIT 2			0.5		
BIT 3			0.25		
BIT 4 (LSB)			0.125		
Zero Output Current	$V_{IN} = 5.0V$		10	50	nA
Output Voltage Range		$V_{BASELINE}$ +1V		+10	V
Input Coding-Complimentary Binary (See Truth Table)					
Logic Input Voltage	ΔI_{OUT} <400nA				
"0" (Switch ON)				0.8	V
"1" (Switch OFF)		2.0			
Logic Input Current					
"0"	$V_{IN} = 0V$		−1.0	−2	mA
"1" (into device)	$V_{IN} = 5V$		0.01	0.1	μA
Power Supply Rejection					
V^+			.005		%/V
V^-			.0005		
Supply Voltage Range					
V^+		4.5	5	20	V
V^-		−10	−15	−20	
Supply Current ($V_{SUPP} = \pm 20V$)					
I^+			7	10	mA
I^-			1	3	

BASIC D/A THEORY

The majority of digital to analog converters contain the elements shown in Figure 1. The heart of the D/A converter is the logic controlled switching network, whose output is an analog current or voltage proportional to the digital number on the logic inputs. The magnitude of the analog output is determined by the reference supply and the array of precision resistors, see fig. 2. If the switching network has a current output, often a transconductance amplifier is used to provide a voltage output.

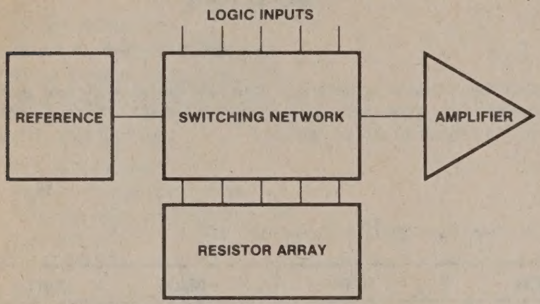


Figure 1: Elements of a D/A Converter

Logic Input	Nominal Output Current (mA)
0 0 0 0	1.875
0 0 0 1	1.750
0 0 1 0	1.625
0 0 1 1	1.500
0 1 0 0	1.375
0 1 0 1	1.250
0 1 1 0	1.125
0 1 1 1	1.000
1 0 0 0	0.825
1 0 0 1	0.750
1 0 1 0	0.625
1 0 1 1	0.500
1 1 0 0	0.375
1 1 0 1	0.250
1 1 1 0	0.125
1 1 1 1	0.000

Figure 2: Truth Table

DEFINITION OF TERMS

The **resolution** of a D/A converter refers to the number of logic inputs used to control the analog output. For example, a D/A converter using two quad current sources would be an 8 bit converter. If three quads were used, a 12 bit converter would be formed. Resolution is often stated in terms of one part in, e.g., 256 since the number of controlling bits is related to total number of identifiable levels by the power of 2. The four bit quad has sixteen different levels (see Truth Table) each output corresponding to a particular logic input word.

Note that **maximum output** of the quad switch is $1 + 1/2 + 1/4 + 1/8 = 1\text{-}7/8 = 1.875$ mA. If this series of bits were continued as $1/16 + 1/32 + 1/64 \ldots\ldots 1/2^{(n-1)}$, the maximum output limit would approach 2.0 mA. This limiting value is called **full scale output**. The maximum output is always less than the full scale output by one least significant bit, LSB. For a twelve bit system (resolution 1 part in 4096) with a full scale output of 10.0 volts the maximum output would be $\frac{4095}{4096}$ X 10V. Since the numbers are extremely close for high resolution systems, the terms are often used interchangeably.

The **accuracy** of a D/A converter is generally taken to mean the largest error of any output level from its nominal value. The accuracy or **absolute error** is often expressed as a **percentage of the full scale output**.

Linearity relates the maximum error in terms of the deviation from the best straight line drawn through all the possible output levels. Linearity is related to accuracy by the scale factor and output offset. If the scale factor is exactly the nominal value and offset is adjusted to zero, then accuracy and linearity are identical. Linearity is usually specified as being within ±1/2 LSB of the best straight line.

Another desirable property of D/A converter is that it be **monotonic**. This simply implies that each successive output level is greater than the preceding one. A possible worst case condition would be when the output changes from most significant bit (MSB) OFF, all other bits ON to the next level which has the MSB ON and all other bits OFF, e.g., 10000 . . . to 01111.

In applications where a quad current switch drives a transconductance amplifier (current to voltage converter), transient response is almost exclusively determined by the output amplifier itself. Where the quad output current drives a resistor to ground, switching time and settling time are useful parameters.

Switching time is the familiar 10% to 90% rise time type of measurement. Low capacitance scope probes must be used to avoid masking the high speeds that current source switching affords. The **settling time** is the elapsed time between the application of a fast input pulse and the time at which the output voltage has settled to or approached its final value within a specified limit of accuracy. This limit of accuracy should be commensurate with the resolution of the DAC to be used.

Typically, the settling time specification describes how soon after an input pulse the output can be relied upon as accurate to within ±1/2 LSB of an N bit converter. Since the 8018A family has been desiged with all the collectors of the current switching transistors tied together, the output capacitance is constant. The transient response is, therefore, a simple exponential relationship, and from this the settling time can be calculated and related to the measured rise time as shown in Figure 3.

Bits of Resolution	±1/2 LSB Error % Full Scale	Number of Time Constants	Number of Rise Times
8	.2 %	6.2	2.8
10	.05%	7.6	3.4
12	.01%	9.2	4.2
Rise Time (10%-90%) = 2.2 R_L C_{eff}			

Figure 3: Settling Time vs. Rise Time Resistor Load

CIRCUIT OPERATION

An example of a practical circuit for the ICL8018A quad current switch is shown in Figure 4. The circuit can be analyzed in two sections; the first generates very accurate currents and the second causes these currents to be switched according to input logic signals. A reference current of 125μA is generated by a stable reference supply and a precision resistor. An op-amp with low offset voltage

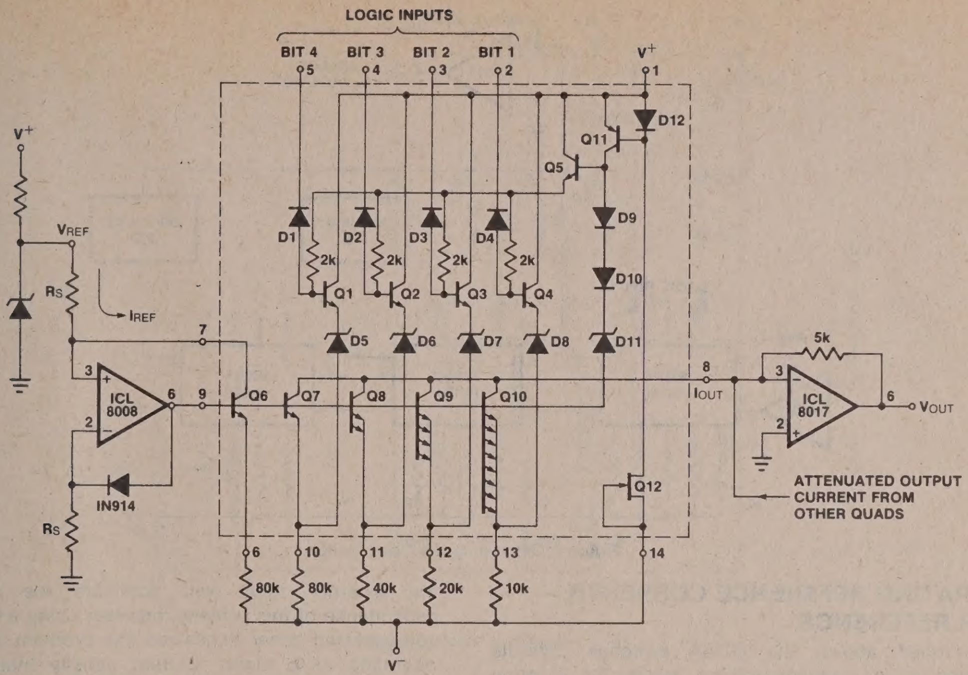


Figure 4: Typical Circuit

and low input bias current, such as the ICL8008, is used in conjunction with the internal reference transistor, Q_6, to force the voltage on the common base line, so that the collector current of Q_6 is equal to the reference current. The emitter current of Q_6 will be the sum of the reference current and a small base current causing a drop of slightly greater than 10 volts across the 80k resistor in the emitter of Q_6. Since this resistor is connected to −15V, this puts the emitter of Q_6 at nearly −5V and the common base line at one V_{BE} more positive at −4.35V typically.

Also connected to the common base line are the switched current source transistors Q_7 through Q_{10}. The emitters of these transistors are also connected through weighted precision resistors to −15V and their collector currents summed at pin 8. Since all these transistors, Q_6 through Q_{10}, are designed to have equal emitter-base voltages, it follows that all the emitter resistors will have equal voltage drops across them. It is this constant voltage and the precision resistors at the emitter that determine the exact value of switched output current. The emitter resistor of Q_7 is equal to that of Q_6, therefore, Q_7's collector current will be I_{REF} or $125\mu A$. Q_8 has 40k in the emitter so that its collector current will be twice I_{REF} or $250\mu A$. In the same way, the 20k and 10k in the emitters of Q_9 and Q_{10} contribute .5 mA and 1 mA to the total collector current.

The reference transistor and four current switching transistors are designed for equal emitter current density by making the number of emitters proportional to the current switched.

The remaining circuitry provides switching signals from the logic inputs. In the switch ON mode, zener diodes D_5 through D_8, connected to the emitter of each current switch transistor Q_7 thru Q_{10}, are reverse biased allowing the transistors to operate, producing precision currents summed in the collectors. The transistors are turned off by raising the voltage on the zeners high enough to turn on the zeners and raise the emitters of the switching transistor. This reverse biases the emitter base diode thereby shutting off that transistor's collector current.

The analog output current can be used to drive one load directly, (1kΩ to ground for FS = 1.875V for example) or can be used to drive a transconductance amplifier to give larger output voltages.

EXPANDING THE QUAD SWITCH

While there are few requirements for only 4 bit D to A converters, the 8018A is readily expanded to 8 and 12 bits with the addition of other quads and resistor dividers as shown in Figure 5.

To maintain the progression of binary weighted bit currents, the current output of the first quad drives the input of the transconductance amplifier directly, while a resistor divider network divides the output current of the second quad by 16 and the output current of the third by 256.

e.g., $I_{Total} = 1 \times (1 + 1/2 + 1/4 + 1/8) + 1/16\,(1 + 1/2 + 1/4 + 1/8) + 1/256\,(1 + 1/2 + 1/4 + 1/8) = 1 + 1/2 + 1/4 + 1/8 + 1/16 + 1/32 + 1/64 + 1/128 + 1/256 + 1/512 + 1/1024 + 1/2048.$

Note that each current switch is operating at the same high speed current levels so that standard 10k, 20k, 40k and 80k resistor networks can be used. Another advantage of this technique is that since the current outputs of the second and third quad are attenuated, so are the errors they contribute. This allows the use of less accurate switches and resistor networks in these positions; hence, the three accuracy grades of .01%, 0.1%, and 1% for the 8018A, 8019A and 8020A, respectively. It should be noted that only the reference transistor on the most significant quad is required to set up the voltage on the common base line joining the three sets of switching transistors (Pin 9).

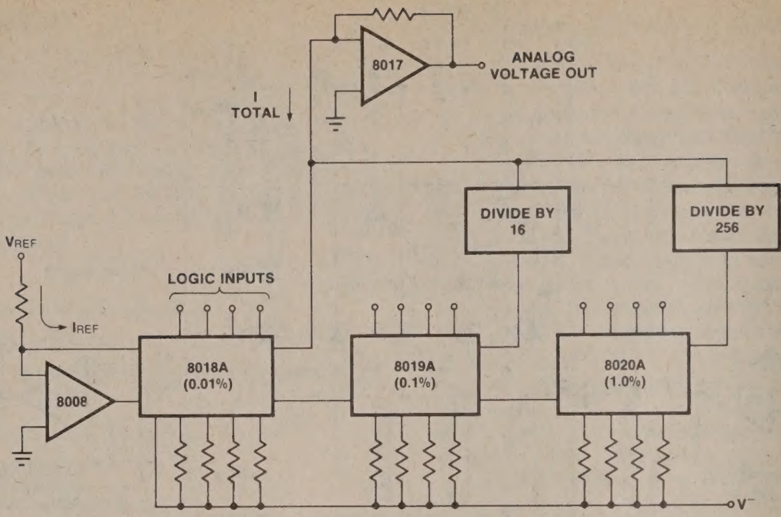


Figure 5: Expanding the Quad Switch

GENERATING REFERENCE CURRENTS — ZENER REFERENCE

As mentioned above, the 8018A switches currents determined by a constant voltage across the external precision resistors in the emitter of each switch. There are several ways of generating this constant voltage. One of the simplest is shown in Figure 6. Here an external zener diode is driven by the same current source line used to bias internal Zener D_{11}.

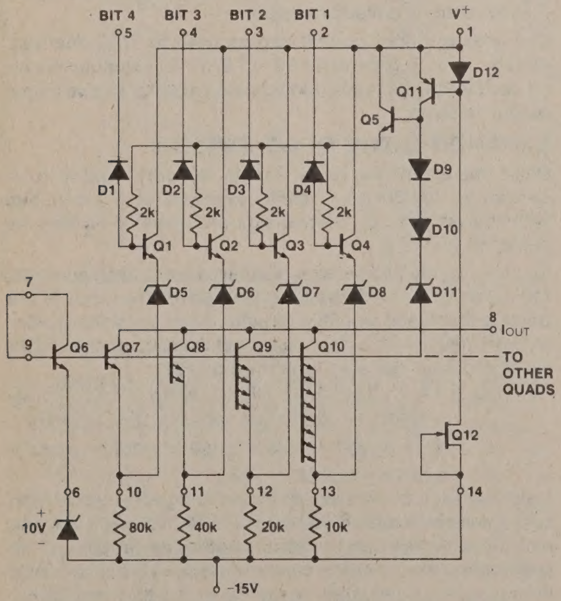


Figure 6: Simple Zener Reference

The zener current will be typically 1 mA per quad. The compensation transistor Q_6 is connected as a diode in series with the external zener. The V_{BE} of this transistor will approximately match the V_{BE}'s of the current switching transistors, thereby forcing the external zener voltage across each of the external resistors. The temperature coefficient of the external zener will dominate the temperature dependence of this scheme, however using a temperature compensated zener minimizes this problem. Since Q_6 is operating at a higher current density than the other switching transistors, the temperature matching of V_{BE}'s is not optimum, but should be adequate for a simple 8 or 10 bit converter.

The 8018A series is tested for accuracy with 10V reference voltage across the precision resistors, implying use of a 10 volt zener. Using a different external zener voltage will only slightly degrade accuracy if the zener voltage is above 5 or 6 volts.

When using other than 10 volt reference, the effects on logic thresholds should also be noted (see logic levels below). Full scale adjustment can be made at the output amplifier.

PNP REFERENCE

Another simple reference scheme is shown in Figure 7. Here an external PNP transistor is used to buffer a resistor divider. In this case, the −15 volt supply is used as a reference. Holding the V^- supply constant is not too difficult since the 8018A is essentially a constant current load. In this scheme, the internal compensation transistor is not necessary, since the V_{BE} matching is provided by the emitter-base junction of the external transistor. A small pot in series with the divider facilitates full scale output adjustment. A capacitor from base to collector of the external PNP will lower output impedance and minimize transient effects.

FULL COMPENSATION REFERENCE

For high accuracy, low drift applications, the reference scheme of Figure 4, offers excellent performance. In this circuit, a high gain op-amp compares two currents. The first is a reference current generated in R_S by the temperature compensated zener and the virtual ground at the non-inverting op-amp input. The second is the collector current of the reference transistor Q_6, provided on the quad switch. The output of the op-amp drives the base of Q_6 keeping its collector current exactly equal to the reference current. Since the switching transistor's emitter current densities are equal and since the precision resistors are proportional, all of the switched collector currents will have the proper value.

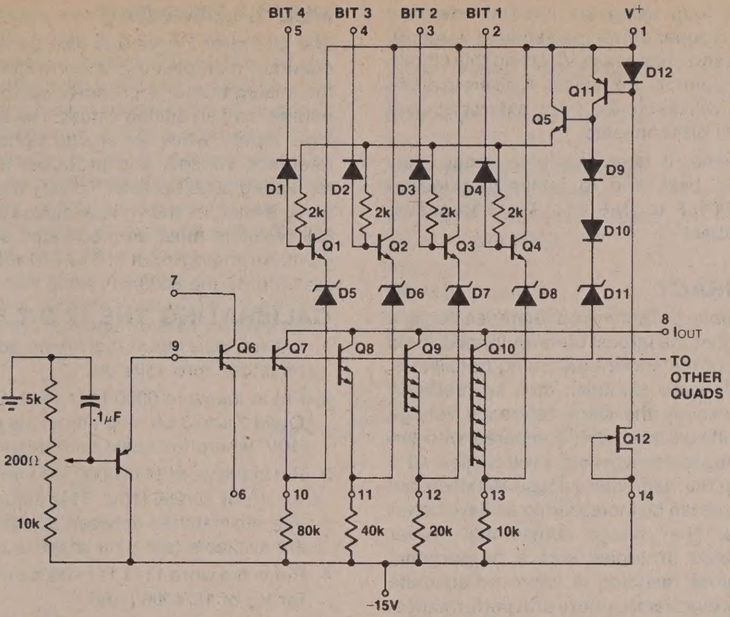
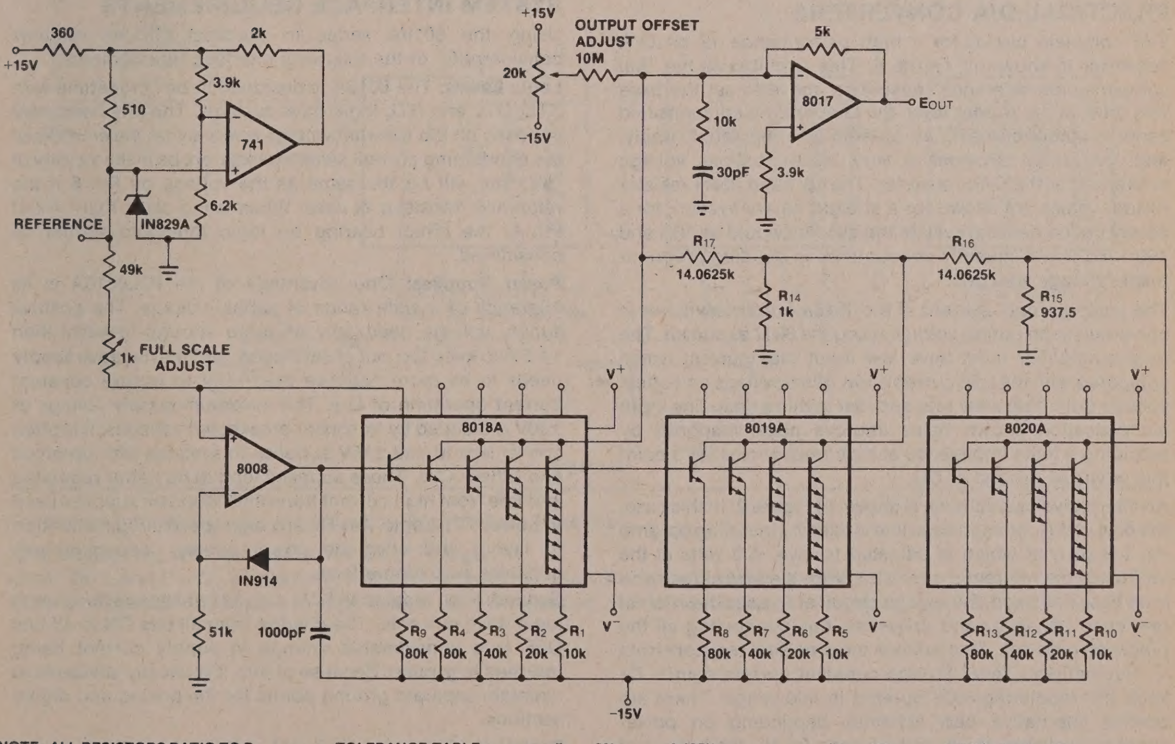

BIT 4
5
BIT 3
4
BIT 2
3
BIT 1
2
V+
1
D12
Q11
Q5
D9
D10
D11
D1
D2
D3
D4
2k
2k
2k
2k
Q1
Q2
Q3
Q4
D5
D6
D7
D8
7
8
IOUT
9
Q6
Q7
Q8
Q9
Q10
TO OTHER QUADS
5k
.1µF
Q12
200Ω
6
10
11
12
13
14
10k
80k
40k
20k
10k
−15V

Figure 7: PNP Reference


360
2k
+15V
3.9k
510
741
IN829A
6.2k
REFERENCE
49k
1k
FULL SCALE ADJUST
8008
IN914
51k
1000pF
+15V
OUTPUT OFFSET ADJUST
10M
20k
−15V
5k
10k
30pF
3.9k
8017
EOUT
R17
14.0625k
R14
1k
R16
14.0625k
R15
937.5
V+
8018A
V−
R9
80k
R4
80k
R3
40k
R2
20k
R1
10k
V+
8019A
V−
R8
80k
R7
40k
R6
20k
R5
10k
V+
8020A
V−
R13
80k
R12
40k
R11
20k
R10
10k
−15V

NOTE: ALL RESISTORS RATIO TO R_1
UNLESS OTHERWISE NOTED.

TOLERANCE TABLE

R_1	10k	0.1% ABS	R_6	20k	0.195%	R_{12}	40k	RATIO TO R_{10} 1%
R_2	20k	0.0122%	R_7	40k	0.391%	R_{13}	80k	RATIO TO R_{10} 1%
R_3	40k	0.0244%	R_8	80k	0.781%	R_{14}	1k	1% ABS
R_4	80k	0.0488%	R_9	80k	0.1%	R_{15}	937.5Ω	1% ABS
R_5	10k	0.096%	R_{10}	10k	0.5% ABS	R_{16}	14.0625k	RATIO TO R_{15} 1%
			R_{11}	20k	RATIO TO R_{10} 1%	R_{17}	14.0625k	RATIO TO R_{14} 0.1%

Figure 8

The op-amp feedback loop using the internal reference transistor will maintain proper currents in spite of V_{BE} drift, beta drift, resistor drift and changes in V^-. Using this circuit, temperature drifts of 2 ppm/°C are typical. A discrete diode connected as shown will keep Q_6 from saturating and prevent latch up if V^- is disconnected.

In any reference scheme, it is advisable to capacitively decouple the common base line to minimize transient effects. A capacitor, .001μF to .1μF from Pin 9 to analog ground is usually sufficient.

IMPROVED ACCURACY

As a final note on the subject of setting up reference levels, it should be pointed out that the largest contributor of error is the mismatch of V_{BE}'s of the current switching transistors. That is, if all the V_{BE}'s were identical, then all precision resistors would have exactly the same reference voltage across them. A one millivolt mismatch compared with ten volt reference across the precision resistors will cause a .01% error. While decreasing the reference voltage will decrease the accuracy, the voltage can be increased to achieve better than .01% accuracies. The voltage across the emitter resistors can be doubled or tripled with a proportional increase in resistor values resulting in improved absolute accuracy as well as improved temperature drift performance. This technique has been used successfully to implement up to 16 bit D/A converters.

PRACTICAL D/A CONVERTERS

The complete circuit for a high performance 12 bit D/A converter is shown in Figure 8. This circuit uses the "full compensation reference" described above to set the base line drive at the proper level, the temperature compensated zener is stabilized using an op-amp as a regulated supply, and the circuit provides a very stable, precise voltage reference for the D/A converter. The 16:1 and 256:1 resistor divider values are shown for a straight binary system; for a binary coded decimal system the dividers would be 10:1 and 100:1 (BCD is frequently encountered in building programmable voltage sources).

The analog output current of the 8018A current switches is converted to an output voltage using the 8017 as shown. The output amplifier must have low input bias current (small compared with the LSB current), low offset voltage and offset voltage drift, high slew rate and fast settling time. The input compensation shown helps improve pulse response by providing a finite impedance at high frequencies for a point that is virtual ground at DC.

An alternative bias scheme is shown in Figure 9. In this case, the bias at the common base line is fixed by inverting op-amp A_4, the gain of which is adjusted to give −5.0 volts at the emitter of the reference transistor. With the bias at the common base line fixed, the regular circuit of A_1 uses the internal reference transistor and drives the bus connecting all the precision resistors. This isolates the precision resistors from V^- fluctuations. Zener D_3 and constant current source Q_1 keep the regulating 8008 op-amp in mid-range. There are several alternative bias schemes depending on power supplies available. If −20 volts is used for V^-, the bottom of the precision resistor will be at −15 and operation will be the same as the standard circuit. If only −15V is available for V^- the gain of the output transconductance amplifier can be increased by 30% to allow use of a smaller switching currents with 7 volts across the precision resistors.

MULTIPLYING DAC

The circuit of Figure 9 is also convenient to use as a one quadrant multiplying D/A converter. In a multiplying DAC, the analog output is proportional to the product of a digital number and an analog signal. The digital number drives the logic inputs, while the analog signal replaces the constant reference voltage, and produces a current to set up the regulating 8008 op-amp. To vary the magnitude of currents being switched, the voltage across all the 10k, 20k, 40k and 80k resistors must be modulated according to the analog input. An analog input of 0 to +10 volts and an 80k resistor at the input to the 8008 will fulfill this requirement.

CALIBRATING THE 12 BIT D/A CONVERTER

1. With all logic inputs high (ones) adjust the output amplifier offset for zero volts out.
2. Put in the word 0000 1111 1111 (Quad 1 maximum output Quad 2 and 3 off) and adjust full scale pot for V_O of 15/16 (10V) where full scale output is to be 10 volts.
3. Put in the word 1111 0000 1111 and trim the Quad 2 divider for V_O of 15/256 (10V). This adjustment compensates for V_{BE} mismatches between quads although matched sets are available (see data sheet).
4. Put in the word 1111 1111 0000 and trim the Quad 3 divider for V_O of 15/4096 (10V).
5. Finally, with all bits ON (all 0's) readjust the full scale factor pot for

$$V_O = 4095/4096\ (10V)$$

SYSTEM INTERFACE REQUIREMENTS

Using the 8018A series in practical circuits requires consideration of the following interface requirements.

Logic Levels: The 8018A is designed to be compatible with TTL, DTL and RTL logic drive systems. The one constraint imposed on the external voltage levels is that the emitters of the conducting current switch transistors be in the vicinity of −5V; this will be the same as the voltage on Pin 6 if the reference transistor is used. When using other than −5V at Pin 6, the direct bearing on logic threshold should be considered.

Power Supplies: One advantage of the ICL8018A is its tolerance of a wide range of supply voltage. The positive supply voltage need only be large enough (greater than +4.5V) to keep Q_{11} out of saturation, and the negative supply needs to be more negative than −10V to ensure constant current operation of Q_{12}. The maximum supply voltage of ±20V is dictated by transistor breakdown voltages. It is often convenient to use ±15V supplies in systems with op-amps and other I.C.'s. These supplies tend to be better regulated and free from high current transients found on supplies used to power TTL Logic. As with any high speed circuit, attention to layout and adequate power supply decoupling will minimize switching effects.

Ground: High resolution D/A, e.g., 12 bits require fairly large logic drive currents. The change from all bits ON to all bits OFF is a considerable change in supply current being returned to ground. Because of this, it is usually advisable to maintain separate ground points for the analog and digital sections.

Resistors: Each quad current switch requires a set of matched resistors scaled proportional to their binary currents as R, 2R, 4R and 8R. For a 10V resistor voltage drop and "2 mA" full scale output current, resistor values of 10k, 20k, 40k and 80k are convenient. Other resistor values can be used, for example, to increase total output current. The individual switched currents can be increased up to 100% of their nominal values. The overall accuracy of the complete D/A converter depends on the accuracy of the reference, the accuracy of the quad current switch and tolerance of resistor matching. Because of the binary progression of switched currents, the tolerance of 80k/10k match can be twice that of the 40k/10k which, in turn, can be twice the tolerance of the 20k/10k ratio and still have equal output current errors. The current dividers between quads allows use of less well matched sets of resistors further along in the D/A just as it allows use of .01%, 0.1%, and 1% accurate quad current switches. There are several manufacturers producing the complete precision resistor networks required to implement up to 12 bit D/A converters. Contact Intersil for additional information.*

*Resistor Ladder Networks are manufactured by the following companies:

Micro Networks Corporation
5 Barbara Lane
Worcester, Massachusetts 01604
Tel. (617) 756-4635

Allen-Bradley Company
1201 S. Second Street
Milwaukee, Wisconsin 53204
Tel. (414) 671-2000

Hycomp, Inc.
146 Main Street
Maynard, Massachusetts 01754
Tel. (617) 897-4578

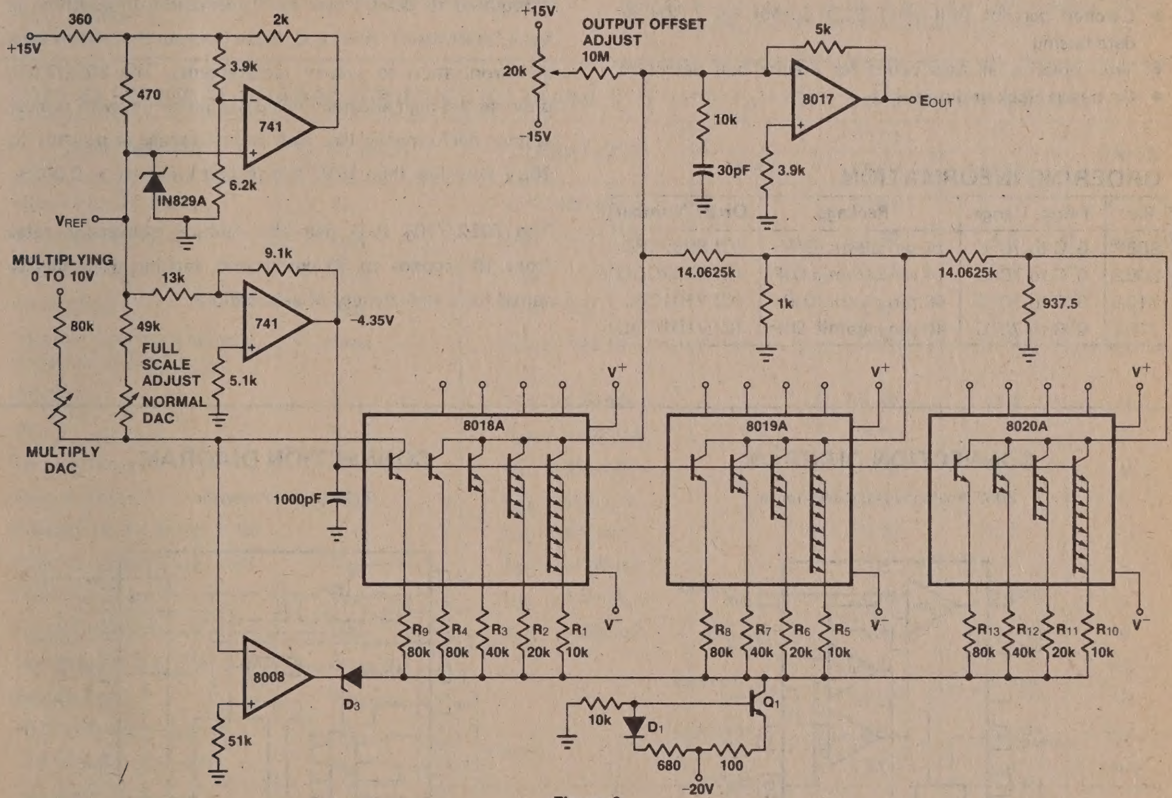

360
2k
+15V
3.9k
470
741
IN829A
6.2k
VREF
MULTIPLYING
0 TO 10V
9.1k
13k
80k
49k
741
-4.35V
FULL
SCALE
ADJUST
5.1k
NORMAL
DAC
MULTIPLY
DAC
1000pF
+15V
OUTPUT OFFSET
ADJUST
10M
20k
-15V
5k
8017
EOUT
10k
30pF
3.9k
14.0625k
1k
14.0625k
937.5
V+
V+
V+
8018A
8019A
8020A
V-
V-
V-
R9
80k
R4
80k
R3
40k
R2
20k
R1
10k
R8
80k
R7
40k
R6
20k
R5
10k
R13
80k
R12
40k
R11
20k
R10
10k
8008
D3
51k
Q1
10k
D1
680
100
-20V

Figure 9

For further information see the following Applications Bulletins.

A016 "Selecting A/D Converters" by Dave Fullagar.
A018 "Do's and Don'ts of Applying A/D Converters" by Peter Bradshaw and Skip Osgood.
A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger.

ICL8052/ICL7101
3½ Digit A/D Pair

FEATURES

- Guaranteed zero reading for 0 volts input
- Auto-zero; auto polarity
- 5pA input current typical
- Single reference voltage
- Latched parallel (full-time) BCD output for LCDs or data busing
- True polarity at zero count for precise null detection
- On-board clock and reference

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
7101	0°C to 70°C	40 pin plastic DIP	ICL7101CPL
7101	0°C to 70°C	40 pin ceramic DIP	ICL7101CDL

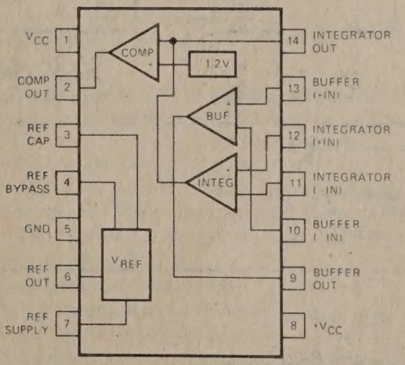
GENERAL DESCRIPTION

The 8052/7101 A/D Pair, with its parallel BCD outputs, is ideally suited for data processing applications or interfacing with 3½-digit Liquid Crystal Displays. No external circuitry is required to demultiplex the information. In addition, it has a "start/reset" input and "busy" output that allows easy synchronization to system requirements. The 8052/7101 provides 4½-digit accuracy in a 3½-digit format with typical system performance like 5pA input leakage, auto-zero to 10μV with less than 1μV/°C drift and Linearity to 0.002%.

The 8052/7101 A/D pair also features conversion rates from 10 seconds to 30 per second, making them ideally suited for a wide variety of applications.

CONNECTION DIAGRAM

8052 Analog Signal Conditioner

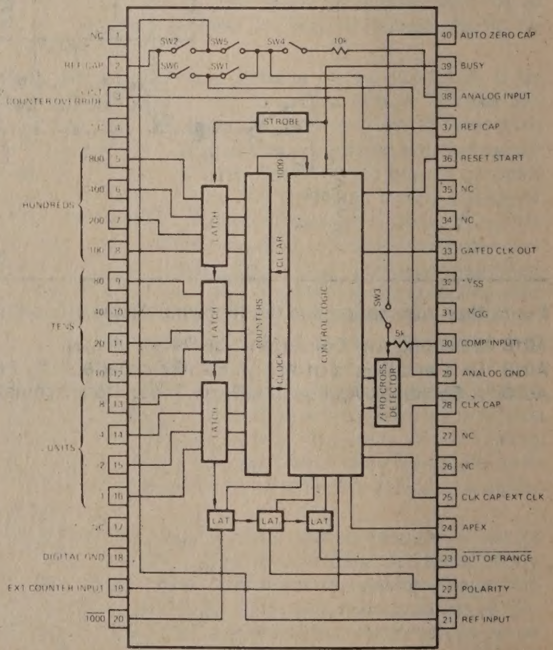


V_{CC} 1
COMP OUT 2
REF CAP 3
REF BYPASS 4
GND 5
REF OUT 6
REF SUPPLY 7
+V_{CC} 8
BUFFER OUT 9
BUFFER (-IN) 10
INTEGRATOR (-IN) 11
INTEGRATOR (+IN) 12
BUFFER (+IN) 13
INTEGRATOR OUT 14
COMP
1.2V
BUF
INTEG
V_{REF}

OUTLINE DRAWINGS
DD, PD

CONNECTION DIAGRAM

7101 Digital Processor



NC 1
REF CAP 2
COUNTER OVERRIDE 3
4
800 5
400 6
200 7
100 8
HUNDREDS
80 9
40 10
20 11
10 12
TENS
8 13
4 14
2 15
1 16
UNITS
NC 17
DIGITAL GND 18
EXT COUNTER INPUT 19
$\overline{1000}$ 20
REF INPUT 21
POLARITY 22
$\overline{\text{OUT OF RANGE}}$ 23
APEX 24
CLK CAP EXT CLK 25
NC 26
NC 27
CLK CAP 28
ANALOG GND 29
COMP INPUT 30
V_{GG} 31
+V_{SS} 32
GATED CLK OUT 33
NC 34
NC 35
RESET START 36
REF CAP 37
ANALOG INPUT 38
BUSY 39
AUTO ZERO CAP 40
SW2
SW5
SW4
SW6
SW1
SW3
10k
5k
STROBE
LATCH
CLEAR
COUNTERS
CLOCK
CONTROL LOGIC
ZERO CROSS DETECTOR
1000
LAT

OUTLINE DRAWING
DL, PL

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	500mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	300°C

8052 ONLY

Supply Voltage	±18V
Differential Input Voltage	±6V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite

7101 ONLY

Source Current (I_S)	100mA
Drain Current (I_D)	100mA
Digital Inputs	5mA
V^+ to V^-	25V
Digital Input	V^- to V^+

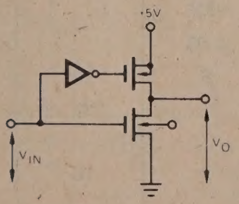
Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

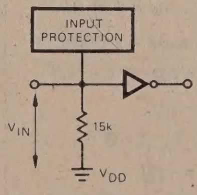
Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

7101 ELECTRICAL CHARACTERISTICS ($V^+ = +5.0V$, $V^- = -15V$, $T_A = +25°C$ unless otherwise specified)

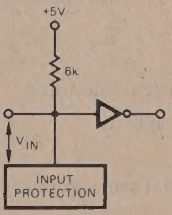
PARAMETER	SYMBOL	CONDITIONS	7101			UNITS
			MIN	TYP	MAX	
Clock Frequency	f_{IN}	C = 1500 pF		20		kHz
External Clock In	I_{INL}	$V_{IN} = 0$ V		0.35	1.0	mA
External Clock In	I_{INH}	$V_{IN} = +5.0$ V		0.35	1.0	mA
Reset/Start	I_{INL}	$V_{IN} = 0$ V		0.8	2.0	mA
Internal Counter Override External Counter Input	I_{INH}	$V_{IN} = +5.0$ V		0.35	1.0	mA
BCD	V_{OL}	$I_{OL} = 1.6$ mA		0.25	0.4	V
BCD	V_{OH}	$I_{OH} = -200\ \mu A$	2.4	4.5		V
Out-of-Range	V_{OL}	$I_{OL} = 3.2$ mA		0.25	0.4	V
Out-of-Range	V_{OH}	$I_{OH} = 400\ \mu A$	2.4	4.5		V
Polarity, Apex, Busy, $\overline{1000}$	V_{OL}	$I_{OL} = 0.8$ mA		0.25	0.4	
Polarity, Apex, Busy, $\overline{1000}$	V_{OH}	$I_{OH} = -200\ \mu A$	2.4	4.5		V
Gated Clockout	V_{OL}	$I_{OL} = 0.3$ mA		0.25	0.4	V
Gated Clockout	V_{OH}	$I_{OH} = -200\ \mu A$	2.4	4.5		V
Switches 1, 3, 4, 5, 6	$R_{DS(ON)}$			400		Ω
Switch 2	$R_{DS(ON)}$			2500		Ω
+5.0 V Supply Current	I_{CC}^+			15	25	mA
−15 V Supply Current	I_{CC}^-			3.0	5.0	mA



Output



External Counter Input
Internal Counter Override



Start/Reset

TYPICAL INPUT/OUTPUT SCHEMATICS

8052 ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = +25°C$ unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052			UNITS
		MIN	TYP	MAX	
OPERATIONAL AMPLIFIER					
Input Offset Voltage	$V_{CM} = 0V$		20	50	mV
Input Current (either input)	$V_{CM} = 0V$		5	50	pA
Common-Mode Rejection Ratio	$V_{CM} = \pm 10V$	70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio*	$V_{CM} = \pm 2V$		110		dB
Large Signal Voltage Gain	$R_L = 10k\Omega$ $V_{OUT} = \pm 10V$	20,000			V/V
Slew Rate			6		V/µs
Unity Gain Bandwidth			1		MHz
Output Short-Circuit Current			20	50	mA
COMPARATOR AMPLIFIER					
Small-Signal Voltage Gain	$R_L = 30k\Omega$		4000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		V
VOLTAGE REFERENCE					
Output Voltage		1.5	1.75	2.0	V
Output Resistance			5		ohms
Temperature Coefficient			50		ppm
Supply Current Total			6	12	mA

*This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS

($V_{++} = +15V$, $V_+ = +5.0V$, $V_- = -15V$, $T_A = +25°C$, Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/7101 (1)			UNITS
		MIN	TYP	MAX	
Zero Input Reading	$V_{in} = 0.0V$	−0.000	±0.000	+0.000	Digital Reading
Ratiometric Reading	$V_{in} \equiv V_{Ref.}$	+0.998	+1.000	+1.001	Digital Reading
Linearity over ± Full Scale (error off reading from best straight line)	$-2V \leqslant V_{in} \leqslant +2V$		0.1	1	Digital Count Error
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 2V$		0.1	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	$V_{in} = 0V$ Full scale = 200.0mV		0.2		Digital
	Full scale = 2.000V		0.05		Count
Leakage Current into Input	$V_{in} = 0V$		5	30	pA
Zero Reading Drift	$V_{in} = 0V$ $0° \leqslant T_A \leqslant 70°C$		1	5	µV/°C
Scale Factor Temperature Coefficient	$V_{in} = +2V$ $0° \leqslant T_A \leqslant 70°C$ (ext. ref. 0 ppm/°C)		3	15	ppm/°C

(1) Tested in 3½ digit (2,000 count) circuit shown in Fig. 1 clock frequency 20kHz.

CIRCUIT DESCRIPTION

Figure 1 shows a typical circuit for a DVM. A minimum of external components is required since the chips have an on-board clock and a medium-quality (40ppm/°C) internal reference. The circuit also shows the switching required for two scale factors: 2.000V and 200.0mV full scale.

The system uses the time-proven dual-slope integration with all of its advantages; non-critical components, high rejection of noise and AC signals, non-critical clock frequency and true ratiometric readings. At the same time, it eliminates one of the basic disadvantages of dual-slope conversion: separate positive and negative reference sources. In this system, the negative reference is generated by charging the reference capacitor to the positive reference potential and then switching it into the circuit inverted when a negative reference is required. Due to the very low leakage and charge injection of the FET switches, the positive and negative references track each other to 10μV over a wide temperature range. This assures a very small error between positive and negative scale factor and, thus, excellent linearity from (+) full-scale to (-) full-scale (.002% typical).

The measurement cycle for the 8052/7101 has three phases. These are auto-zero, integrate input, and integrate reference. At the end of a measurement the system automatically reverts to the auto-zero mode until a new measurement is initiated. If an over-load has not occurred in the previous measurement, 10 milliseconds of auto-zero is sufficient to null any offsets to 10μV. At power on, or after an overload, 100 milliseconds is required to assure the auto-zero capacitor has charged to the correct value.

Start Conversion

Prior to conversion, the reset-start input must be held low to inhibit conversion (during auto-zero). Conversion is initiated by a positive transition on the start-reset line. (It must therefore return to the low state prior to completion of conversion in order to allow proper auto-zero function.) The positive transition generates a clear pulse which resets all internal logic (counters, etc.) and sets the clock enable, thus initiating the conversion sequence.

Integrate Input

During the first period, switch #4 is closed, (all others open), applying the input potential to the buffer. Since the amplifier offsets are stored on the auto-zero capacitor, the integrator's slope is determined solely by the input voltage. The input voltage is integrated for exactly 1000 counts, thus reaching an integrator output proportional to the integral of the input for a fixed time.

Integrate Reference

At the end of 1000 counts, switch #4 is opened, the polarity flip-flop is set, and the integrate reference period begins. Depending on the polarity, switch #5 or #6 is closed, connecting the buffer input to ground or $2V_{ref}$. This causes the integrator to ramp towards its quiescent (auto-zero) point with a slope proportional to $+V_{ref}$ or $-V_{ref}$. When the integrator crosses its quiescent auto-zero point, the comparator changes state, causing the zero crossing detector to generate a conversion complete signal which inhibits the clock and loads the logic information into the output latches. Switch #5 (or #6) is opened, switches #1, #2, and #3 are closed, and the system returns to a quiescent auto-zero mode, awaiting the next initiate conversion signal. If 2000 counts are received prior to zero crossing, an out-of-range signal is generated which sets the "out-of-range" output and resets the system.

Note 1: Internal reference out ≃ 1.8V, reference input = 1,000 volts for 1.999 volt scale and 100mV for 199.9mV scale.
Note 2: External components shown are suggested for 3 readings/sec.
Note 3: Parallel BCD outputs and other latched outputs are strobed at end of conversion and retain data until completion of next conversion.
Note 4: Start/Reset should remain Low during Auto-Zero. Conversion is initiated by a positive pulse on start pin. (minimum width 100nsec).
Note 5: Component values ±20% typ.

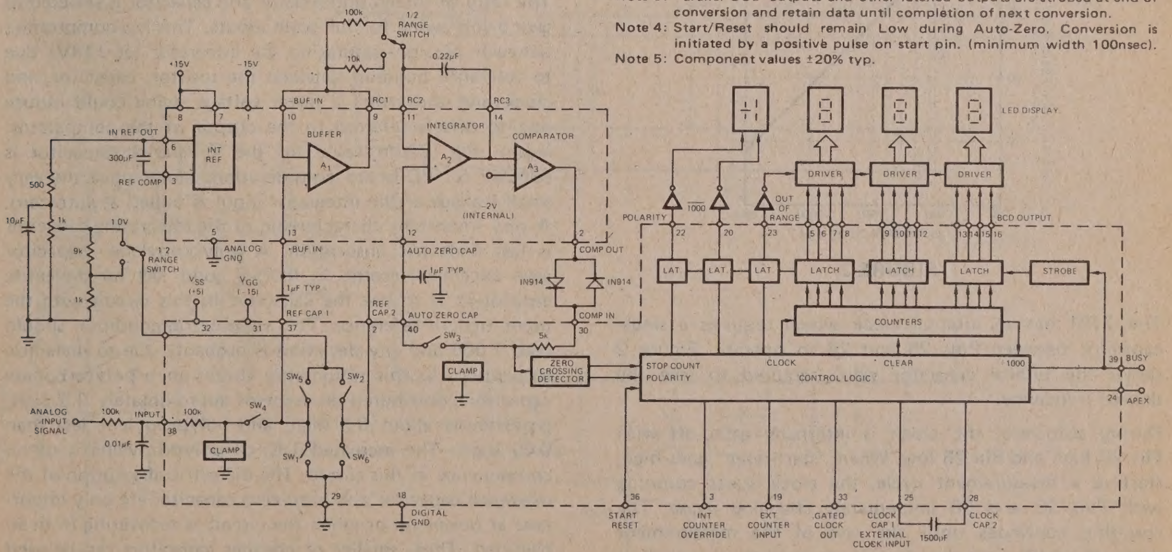

100k
1/2 RANGE SWITCH
10k
0.22µF
+15V
-15V
-BUF IN
RC1
RC2
RC3
8
7
1
10
9
11
14
IN REF OUT
INT REF
BUFFER
INTEGRATOR
COMPARATOR
A1
A2
A3
300µF
6
REF COMP
3
500
10µF
1k
1.0V
-2V (INTERNAL)
5
13
12
2
ANALOG GND
+BUF IN
AUTO ZERO CAP
COMP OUT
9k
1/2 RANGE SWITCH
1k
VSS (+5)
VGG (-15)
1µF TYP
IN914
IN914
REF CAP 1
REF CAP 2
AUTO ZERO CAP
COMP IN
32
31
37
2
40
30
SW3
5k
CLAMP
ZERO CROSSING DETECTOR
SW5
SW2
SW4
SW1
SW6
ANALOG INPUT SIGNAL
100k
INPUT
100k
38
0.01µF
CLAMP
29
18
DIGITAL GND
LED DISPLAY
DRIVER
DRIVER
DRIVER
POLARITY
1000
OUT OF RANGE
BCD OUTPUT
22
20
23
5
6
7
8
9
10
11
12
13
14
15
16
LAT
LAT
LAT
LATCH
LATCH
LATCH
STROBE
COUNTERS
STOP COUNT
POLARITY
CLOCK
CLEAR
1000
CONTROL LOGIC
39
BUSY
24
APEX
36
3
19
33
25
28
START RESET
INT COUNTER OVERRIDE
EXT COUNTER INPUT
GATED CLOCK OUT
CLOCK CAP 1 EXTERNAL CLOCK INPUT
1500pF
CLOCK CAP 2

FIGURE 1. 3½ DIGIT A/D CONVERTER FUNCTIONAL DIAGRAM

7101 Digital Processor Controls

Two pins are included on the 7101 that allow the user to externally control the gain of the converter. The first pin, "Internal Counter Override", if held high, will inhibit the carry pulse from the internal counter that switches the converter from signal integrate to reference integrate. As long as this input is high, the converter will remain in the signal integrate mode. At the same time, it enables the other pin, External Counter Input, to supply this transition pulse from external sources. One technique for changing the gain of the system would be to hold "Internal Counter Override" high through the first N carry pulses. This would increase the signal integrate time by a factor of N+1 and, thus, the sensitivity of the system by N+1. Since the number of suppressed pulses could be controlled digitally, the system could accomodate signals from ±2.000V to ±200.0mV (or lower, if time permits) without changing the external analog scale factor components. By using more complex external logic and both inputs, the user could digitally set offset (tare) and scale factor to convert voltages to physical units such as "degrees centigrade", "pounds", or "feet".

A "BUSY" pin is provided which permits interrogating the 8052/7101 to determine the status of the conversion. During the signal integrate and reference integrate periods, the "busy" line is high until the conversion is complete, at which time "busy" line goes low. This transition can be used to signal "new data available".

The "Apex" pin provides a digital signal which goes high during the reference integrate period.

"OUT-OF-RANGE" is indicated by a latched "low" on pin 23 for counts over 2000. The BCD digital values are "high" (true), except $\overline{1000}$ which is "low".

A positive polarity of the analog input signal is indicated by a "high" state at the output of the "polarity" latch on pin 22.

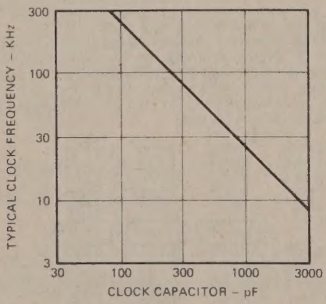


FIGURE 2.

The 7101 has an internal clock which requires a single capacitor between Pins 25 and 28 to operate. Figure 2 shows the typical capacitor value required to give the desired frequency.

During auto-zero, the clock is internally gated-off with Pin 28 high and Pin 25 low. When "start-reset" goes high, starting a measurement cycle, the clock starts counting with Pins 25 and 28 immediately changing phase. The counting continues until the end of the measurement cycle, at which time the clock is returned to its auto-zero condition.

In a typical application where visual readings are required, three readings per second is near the optimum speed. Faster readings make it difficult to resolve individual readings, while at slower rates the reader has to wait too long between measurements. In this application, 40% of the time (133mS) could be allocated to auto-zero and 60% (200mS) to signal and reference integrate. Since a measurement cycle consists of 3,000 clock pulses maximum, this dictates a clock frequency of 15kHz. Also, since the dual-slope technique of A/D conversion is not first-order dependent on clock frequency, the ±20% variation of clock frequency from unit-to-unit would result in no measurable error. However, in some applications, a more precise clock frequency would be desired. For instance, if precise rejection of 60Hz is required, the signal integrate phase (1,000 counts) would have to contain an integral number of 60Hz periods. For these applications, an external clock can be used by deleting the capacitor and connecting the external clock to Pin 25. However, if the clock is run asynchronously with start/reset, there will be one clock pulse of uncertainty in the integrate signal time, depending on where in the clock pulse period the start/reset went high. This will show up as one count of noise for signal near full-scale. This noise or jitter can be avoided by synchronizing the start/reset pulse to the negative-going edge of the external clock. Pin 33, Gated Clock Out, is a buffered output of the clock (internal or external) that is off (low) during auto-zero and in phase with Pin 25 during measurement.

Component Selection

Except for the reference voltage, none of the component values are first order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance, the reference capacitor and auto-zero capacitor are each shown as 1.0μfd. These relatively large values are selected to give greater immunity to PC board leakage since much smaller capacitors are adequate for charge injection errors or leakage errors from the 8052/7101.

The ratio of integrating resistor and capacitor is selected to give 9-volt swing for full-scale inputs. This is a compromise between possibly saturating the integrator (at ±14V) due to tolerance build-up between the resistor, capacitor, and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again, the .22μfd value for the integrating capacitor is selected for PC board considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating capacitor is low dielectric absorption. A polypropylene capacitor gave excellent results. In fact, a good test for dielectric absorption is to use the capacitor in this circuit with the input tied to reference. This ratiometric condition should read 1.000 and any deviation is probably due to dielectric absorption. In this ratiometric condition, a polycarbonate capacitor contributed an error of approximately 0.8 digit, polystyrene about 0.3 digit, and polypropylene less than 0.05 digit. The increased T.C. of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference capacitor and auto-zero capacitor are only important at power on or when the circuit is recovering from an overload. Thus, smaller or cheaper capacitors can be used here if accurate readings are not required for the first few seconds of recovery.

The back-to-back diodes on the comparator output are recommended in the 200.0mV range to reduce the noise effects. In the normal operating mode, they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero capacitor. At start-up or recovery from an overload, their impedance is low to large signals so the capacitor can be charged in one auto-zero cycle. If only the 2.000V range is used, a 100k resistor in place of the back-to-back diodes is adequate for noise effects.

Maximum Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μS delay. At a clock frequency of 160kHz (6μS period), half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash 1 on noise peaks even when the input is shorted.

Some circuits use positive feedback or a latch to solve the delay problem. However, unless the comparator voltage swing, the comparator gain, and the integrator gain are carefully controlled, this circuit can generate **anticipation** errors that greatly exceed the 3μS **delay** error. Also, it is very susceptible to noise spikes. A more controlled approach for extending the conversion rate is the use of a small resistor in the integrator feedback loop. This feeds a small pulse to the comparator to get it moving quickly and partially compensate for its delay.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitor. With most devices, measurement cycles as long as 10 seconds gave no measurable leakage error.

APPLICATIONS

8052/7101 3½ Digit LCD DPM/DVM

Figure 3 illustrates an application where the 8052/7101 interfaces with a Liquid Crystal Display. The CD4054 and CD4055s are Liquid Crystal Display Drivers (4-segment and 7-segment, respectively) which provide the level shifting (up to 30$V_{p\text{-}p}$ at $V_{DD}-V_{EE}$ = 15V) necessary to drive the LCD. Overrange is indicated by a special character. If blanking of any part of the display is required on overload, Pin 23 (7101) can be used to drive Pin 7 on those display drivers via an inverter and level shift such as CD4009 or 74C903 or another CD4054. Display applications requiring a plus sign rather than a blank indication for positive analog input levels (i.e., +1.999 versus 1.999) need to invert the "polarity" logic output level which is normally high for positive analog input signals.

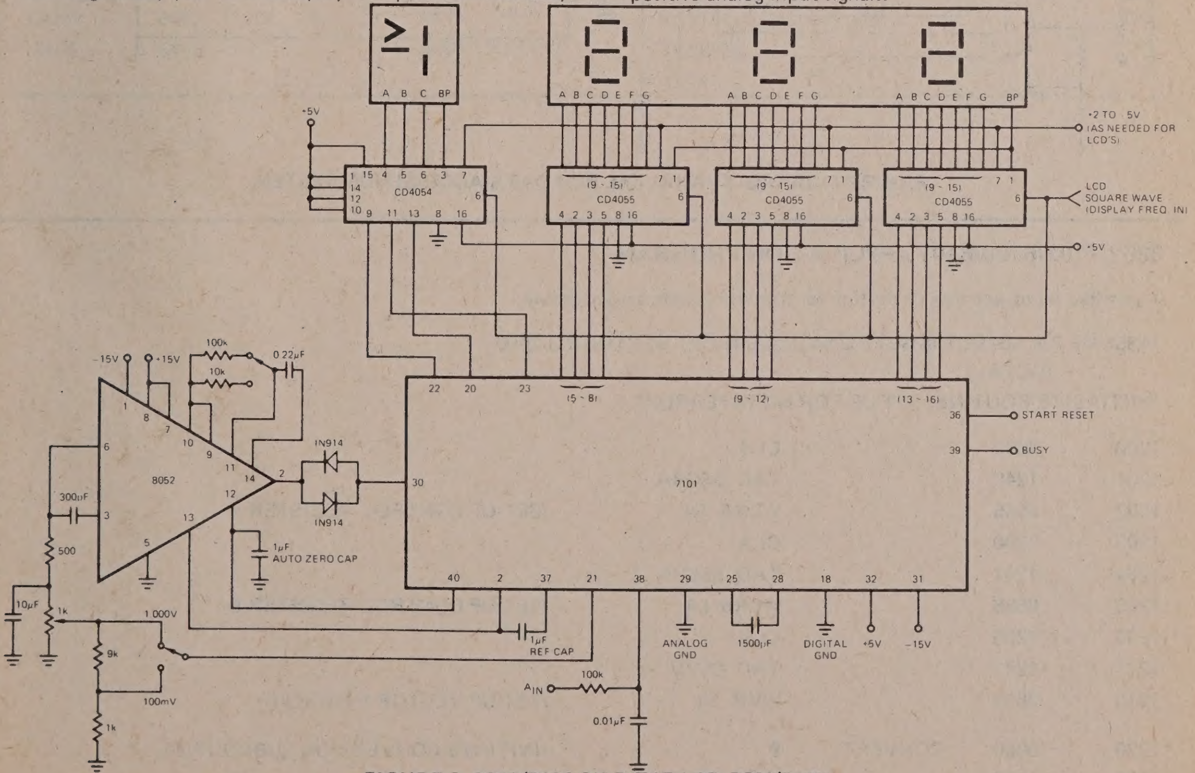

A B C BP
A B C D E F G
A B C D E F G
A B C D E F G BP
+5V
+2 TO +5V (AS NEEDED FOR LCD'S)
CD4054
1 15 4 5 6 3 7
14
12
10 9 11 13 8 16
CD4055
(9 - 15)
7 1
6
4 2 3 5 8 16
LCD SQUARE WAVE (DISPLAY FREQ IN)
+5V
-15V
+15V
100k
10k
0.22μF
8052
1
8
7
6
10
9
11
14
2
12
3
13
5
300pF
500
IN914
IN914
1μF AUTO ZERO CAP
22 20 23
(5 - 8)
(9 - 12)
(13 - 16)
36
39
START RESET
BUSY
30
7101
40 2 37 21 38 29 25 28 18 32 31
10μF
1k
1.000V
9k
100mV
1k
1μF REF CAP
100k
A_{IN}
0.01μF
ANALOG GND
1500pF
DIGITAL GND
+5V
-15V

FIGURE 3. 8052/7101 3½ DIGIT LCD DPM/DVM

8052/7101/6100/6101 Set

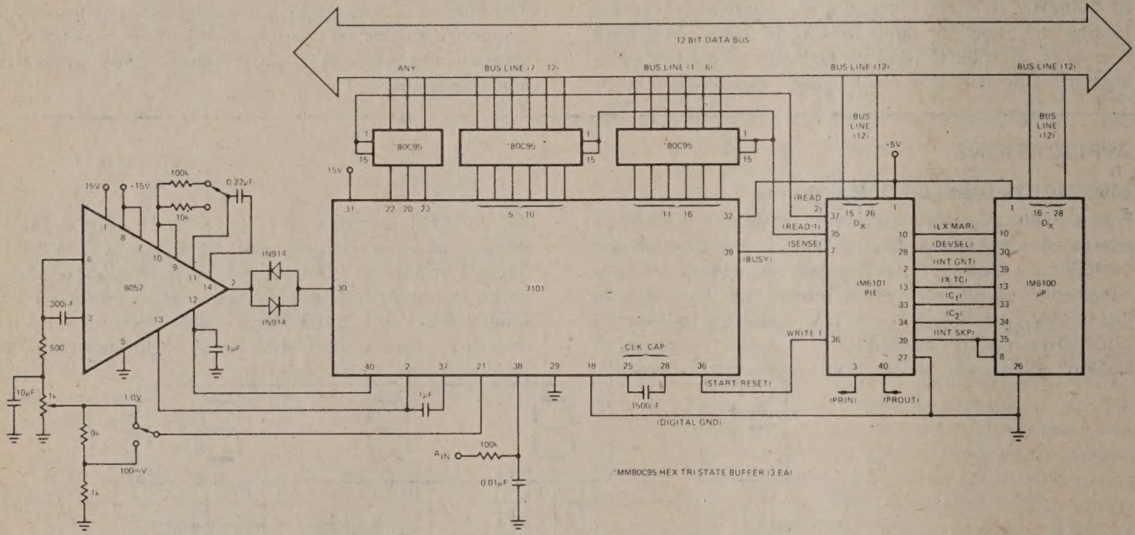
The circuit in Figure 4 interfaces the 8052/7101 A-to-D converter chip set to an IM6100* microprocessor, using the 6101* Parallel Interface Element. Hex Tri-state Buffers (e.g., MM80C95*) are used to control bus access from the 7101 during read operations.

Conversion is initiated by activating the WRITE 1 line (positive going). The converter pair will then convert the analog input to digital form, and latch the data in the 7101. The busy line will go low as the conversion ends, and this transition is sensed by the SENSE 1 line, triggering an interrupt. The interrupt routine should read the 12-line data word, and then the polarity, $\overline{1000}$ and out-of-range lines.

Sufficient time must be allowed for the auto-zero loop to settle before retriggering a conversion. Ten milliseconds of auto-zero is sufficient to null any offsets to 10 microvolts. At power-on or after an overload, 100 milliseconds is required to assure the auto-zero capacitor has charged to the correct value. This time delay may be implemented conveniently using the IM6102 (Memory Extender/Time Delay Device).

Some skeletal service routines for this connection are given on page 7 and 8.

*References:
Intersil IM6100 CMOS 12-bit Microprocessor
Intersil IM6101 Parallel Interface Element
National MM80C95 Hex CMOS Tri-State Buffers


12 BIT DATA BUS
ANY
BUS LINE (7 - 12)
BUS LINE (1 - 6)
BUS LINE (12)
BUS LINE (12)
BUS LINE (12)
BUS LINE (12)
80C95
80C95
80C95
+5V
15V
-15V
100k
10k
0.22µF
8052
IN914
IN914
300pF
500
10µF
1k
1.0V
9k
100mV
1k
1µF
1µF
7101
CLK CAP
1500pF
DIGITAL GND
START RESET
READ 1
READ 2
SENSE 1
BUSY
WRITE 1
IM6101 PIE
IM6100 µP
LX MAR
DEVSEL
INT GNT
X TC
C1
C2
INT SKP
PRIN
PROUT
D_X
D_X
A_{IN}
100k
0.01µF

*MM80C95 HEX TRI STATE BUFFER (3 EA)

FIGURE 4. 3½ DIGIT PARALLEL BCD DATA ACQUISITION SYSTEM

8052/7101/6100/6101 APPLICATION PROGRAM

A possible set-up and service routine for the connection is given below.

```
/ASSUME PIE SELECT IS SET TO 54, INTERRUPT VECTOR TO 2000
            (OCTAL)
/INITIALIZE ROUTINE: SET-UP FOR NO INTERRUPT

1200    7200                 CLA
1201    1240                 TAD  SSCRA
1202    6545                 WCRA  54          /SET-UP CONTROL REGISTER A
1203    7200                 CLA
1204    1241                 TAD  SSCRB
1205    6555                 WCRB  54          /SET-UP CONTROL REGISTER B
1206    7200                 CLA
1207    1242                 TAD  SSVV
1210    6556                 WVR  54           /SET-UP VECTOR REGISTER

1220    0000    CONVERT,     0                 /INITIATE CONVERSION SUBROUTINE
1221    1243                 TAD  SSCRAI
```

8052/7101/6100/6101 APPLICATION PROGRAM (CON'T)

```
1222    6545              WCRA  54          /SET-UP CONTROL REGISTER A
1223    6541              WRITE1  54        /THE WRITE PULSE STARTS CONVERSION

1224    5620              JMP  I  CONVERT   /RETURN

1240    0040    SSCRA,    0040              /WP 1 SET HI, IE1 SET LO
1241    0000    SCRRB,    0000              /SL1, SP1 SET LP, NEGATIVE EDGE SENSE
1242    2000    SSVV,     2000              /VECTOR ADDRESS
1243    0041    SSCRAI,   0041              /WPI SET HI, IE1 SET HI

0000    0000    INTRPT,   0                 /ENTRY POINT FOR INTERRUPT
0001    6002              IOF               /DISABLE INTERRUPT, JUMP TO VECTOR ADDRESS

0140    0000    AD1,      0                 /FIRST WORD OF DATA
0141    0000    AD2,      0                 /SECOND WORD OF DATA
0160    0000    TEMP1,    0                 /TEMPORARY STORAGE

2000    5210    VV,       JMP ATOD          /JUMP TO SERVICE POINT

2010    3160    ATOD,     DCA  TEMP1        /SAVE AC
2011    6540              READ1  54         /READ BCD LINES
2012    3140              DCA  AD1          /AND STORE
2013    6550              READ2  54         /READ POLARITY, 1000, AND OVERRANGE
2014    7040              CMA               /COMPLEMENT TO THE TRUE
2015    3141              DCA  AD2          /AND STORE
/       --      ---       ----              /ANY OTHER WORK
2020    1160              TAD  TEMP1        /RESTORE AC
2021    6001              ION               /RESTORE INTERRUPT
2022    5400              JMP  I  INTRPT    /RETURN
```

ICL8052/ICL71C03 Pair and ICL8068/ICL71C03 Pair

Precision 4½ Digit A/D Converter

FEATURES

- **Typically less than 2μV p-p noise (200.00mv full scale, ICL8068)**
- **Accuracy guaranteed to ±1 count over entire ±20,000 counts (2.0000 volts full scale)**
- **Guaranteed zero reading for 0 volts input**
- **True polarity at zero count for precise null detection**
- **Single reference voltage required**
- **Over-range and under-range signals available for auto-ranging capability**
- **All outputs TTL compatible**
- **Medium quality reference (40ppm typical) on board**
- **Blinking display gives visual indication of over-range**
- **Six auxillary inputs/outputs are available for interfacing to UARTs, Microprocessors or other complex circuitry**
- **5pA input current typical (8052A)**
- **Pin compatible with the ICL7103**

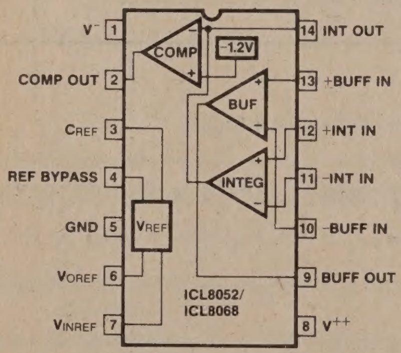
GENERAL DESCRIPTION

The ICL8052 or ICL8068/ICL71C03 chip pairs with their multiplexed BCD output and digit drivers are ideally suited for the visual display DVM/DPM market. The outstanding 4-1/2 digit accuracy, 200.00mV to 2.0000V full scale capability, auto-zero and auto-polarity combine with true ratiometric operation, almost ideal differential linearity and time-proven dual slope conversion. Use of these chip pairs eliminates clock feedthrough problems, and avoids the critical board layout usually required to minimize charge injection.

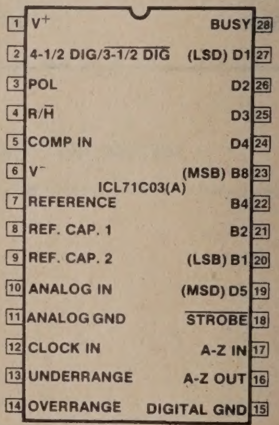
When only 2000 counts of resolution are required the 71C03 can be wired for 3-1/2 digits and give up to 30 readings/second making it ideally suited for a wide variety of applications.

The ICL71C03 is an improved CMOS plug-in replacement for the ICL7103 and should be used in all new designs.

PIN CONFIGURATION


V⁻ 1
COMP OUT 2
CREF 3
REF BYPASS 4
GND 5
VOREF 6
VINREF 7
14 INT OUT
13 +BUFF IN
12 +INT IN
11 –INT IN
10 –BUFF IN
9 BUFF OUT
8 V⁺⁺
COMP
-1.2V
BUF
INTEG
VREF
ICL8052/
ICL8068

(Outline dwg PD, DD)


1 V⁺
2 4-1/2 DIG/3-1/2 DIG
3 POL
4 R/H
5 COMP IN
6 V⁻
7 REFERENCE
8 REF. CAP. 1
9 REF. CAP. 2
10 ANALOG IN
11 ANALOG GND
12 CLOCK IN
13 UNDERRANGE
14 OVERRANGE
BUSY 28
(LSD) D1 27
D2 26
D3 25
D4 24
(MSB) B8 23
B4 22
B2 21
(LSB) B1 20
(MSD) D5 19
STROBE 18
A-Z IN 17
A-Z OUT 16
DIGITAL GND 15
ICL71C03(A)

(Outline dwg DI,JI,PI)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
8052A	0°C to 70°C	14 pin plastic DIP	ICL8052ACPD
8052A	0°C to 70°C	14 pin ceramic DIP	ICL8052ACDD
8068	0°C to 70°C	14 pin ceramic DIP	ICL8068CDD
8068A	0°C to 70°C	14 pin ceramic DIP	ICL8068ACDD

Part	Temp. Range	Package	Order Number
71C03	0°C to 70°C	28-Pin Plastic DIP	ICL71C03CPI
71C03	0°C to 70°C	28-Pin Ceramic DIP	ICL71C03CDI
71C03	0°C to 70°C	28-Pin CERDIP	ICL71C03CJI
71C03A	0°C to 70°C	28-Pin CERDIP	ICL71C03ACJI
71C03A	0°C to 70°C	28-Pin Plastic DIP	ICL71C03ACPI
71C03A	0°C to 70°C	28-Pin Ceramic DIP	ICL71A03ACDI

ABSOLUTE MAXIMUM RATINGS*

Power Dissipation (Note 1)	500mW
Storage Temperature	−65°C to +150°C

8052, 8068

Supply Voltage	±18V
Differential Input Voltage (8068)	±30V
(8052)	±6V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	

71C03

Positive Supply Voltage (GND to V^+)	6.5V
Negative Supply Voltage (GND to V^-)	−17V
Analog Input Voltage (Note 4)	V^+ to V^-
Digital Input Voltage (Note 5)	V^+ +0.3V GND −0.3V

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

Note 4: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 5: Connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that the power supply to the 71C03 be established before any inputs from sources not on that supply are applied.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

71C03 AND 71C03A ELECTRICAL CHARACTERISTICS ($V+ = +5.0$, $V- = -15V$, $T_A = 25°C$)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS	Clock In, Run/$\overline{\text{Hold}}$, 4-1/2/$\overline{\text{3-1/2}}$	I_{INL}	$V_{IN} = 0$		.2	.6	mA
		I_{INH}	$V_{IN} = +5V$		.1	10	μA
	Comp. In Current	I_{INL}	$V_{IN} = 0$		.1	10	μA
		I_{INH}	$V_{IN} = +5V$		.1	10	μA
	Threshold	V_{INTH}			2.5		V
OUTPUTS	All Outputs	V_{OL}	$I_{OL} = 1.6ma$		.25	.40	V
	B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OH}	$I_{OH} = -1mA$	2.4	4.2		V
	Busy, Strobe, Over-range, Under-range Polarity	V_{OH}	$I_{OH} = -10\mu A$	4.9	4.99		V
SWITCH	Switches 1, 3, 4, 5, 6	$r_{DS(on)}$			400		Ω
	Switch 2	$r_{DS(on)}$			1200		Ω
	Switch Leakage (All)	$I_{D\ OFF}$			2		pA
SUPPLY	+5V Supply Range			+4	+5	+6	V
	−15V Supply Range			−5	−15	−18	V
	+5V Supply Current	I^+	fclk = 0		1.1	3.0	mA
	−15V Supply Current	I^-	fclk = 0		0.8	3.0	
	Power Dissipation Capacitance	C_{PD}	vs. Clock Freq		40		pF
Clock	Clock Freq. (Note 1)			DC	2000	1200	kHz

Note 1: This specification relates to the clock frequency range over which the ICL71C03(A) will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

8068 ELECTRICAL CHARACTERISTICS (V^{++} = +15V, V^- = −15V, T_A = 25°C unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8068			8068A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	V_{CM} = 0V		20	65		20	65	mV
Input Current (either input) (Note 1)	V_{CM} = 0V		175	250		80	150	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
Large Signal Voltage Gain	R_L = 50kΩ	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			2			2		MHz
Output Short-Circuit Current			5	10		5	10	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		Ω
Temperature Coefficient			50			40		ppm/°C
Supply Voltage Range		±10		±18	±10		±18	V
Supply Current Total				14		8	14	mA

8052 ELECTRICAL CHARACTERISTICS (V^{++} = +15V, V^- = −15V, T_A = 25°C unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052			8052A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	V_{CM} = 0V		20	50		20	50	mV
Input Current (either input) (Note 1)	V_{CM} = 0V		5	50		2	10	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			1			1		MHz
Output Short-Circuit Current			20	100		20	100	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		Ω
Temperature Coefficient			50			40		ppm/°C
Supply Voltage Range		±10		±18	±10		±18	V
Supply Current Total			6	12		6	12	mA

Note 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \Theta jA\ Pd$ where ΘjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 2: This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS: 8068/71C03

($V^{++} = +15V$, $V^{+} = +5V$, $V^{-} = -15V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8068/71C03(1)			8068A/71C03A(2)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	$V_{IN} = 0.0V$ Full Scale = 200.00mV	−00.00	±00.00	+00.00	−00.00	±00.00	+00.00	Digital Reading
Ratiometric Reading(3)	$V_{IN} = V_{REF}$ Full Scale = 2.000V	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-2V \leq V_{IN} \leq +2V$		0.2	1		0.5	1	Digital Count Error
Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-2V \leq V_{IN} \leq +2V$		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{IN} \equiv +V_{IN} \approx 2V$		0.2	1		0.5	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	$V_{IN} = 0V$ Full scale = 200.0mV		3			2		μV
Leakage Current at Input	$V_{IN} = 0V$		200	300		100	200	pA
Zero Reading Drift	$V_{IN} = 0V$ $0° \leq T_A \leq 50°C$ (4)		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	$V_{IN} = +2V$ $0 \leq T_A \leq 50°C$ (4) (ext. ref. 0 ppm/°C)		3	15		2	5	ppm/°C

SYSTEM ELECTRICAL CHARACTERISTICS: 8052/71C03

($V^{++} = +15V$, $V^{+} = +5V$, $V^{-} = -15V$ $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/71C03(1)			8052A/71C03A(2)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	$V_{IN} = 0.0V$ Full Scale = 2.000V	−0.000	±0.000	+0.000	−0.0000	±0.0000	+0.0000	Digital Reading
Ratiometric Reading (3)	$V_{IN} \equiv V_{REF}$ Full Scale = 2.000V	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-2V \leq V_{IN} \leq +2V$		0.2	1		0.5	1	Digital Count Error
Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-2V \leq V_{IN} \leq +2V$		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{IN} \equiv +V_{IN} \approx 2V$		0.2	1		0.5	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	$V_{IN} = 0V$ Full scale = 200.0mV Full scale = 2.000V		20 50			30		μV
Leakage Current at Input	$V_{IN} = 0V$		5	30		3	10	pA
Zero Reading Drift	$V_{IN} = 0V$ $0° \leq T_A \leq 70°C$		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	$V_{IN} = +2V$ $0 \leq T_A \leq 70°C$ (ext. ref. 0 ppm/°C)		3	15		2	5	ppm/°C

Note 1: Tested in 3-1/2 digit (2,000 count) circuit shown in Fig. 7, clock frequency 12kHz. Pin 2 71C03 connected to Gnd.

Note 2: Tested in 4-1/2 digit (20,000 count) circuit shown in Fig 7, clock frequency 120kHz. Pin 2 71C03A open.

Note 3: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

Note 4: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the 8068.

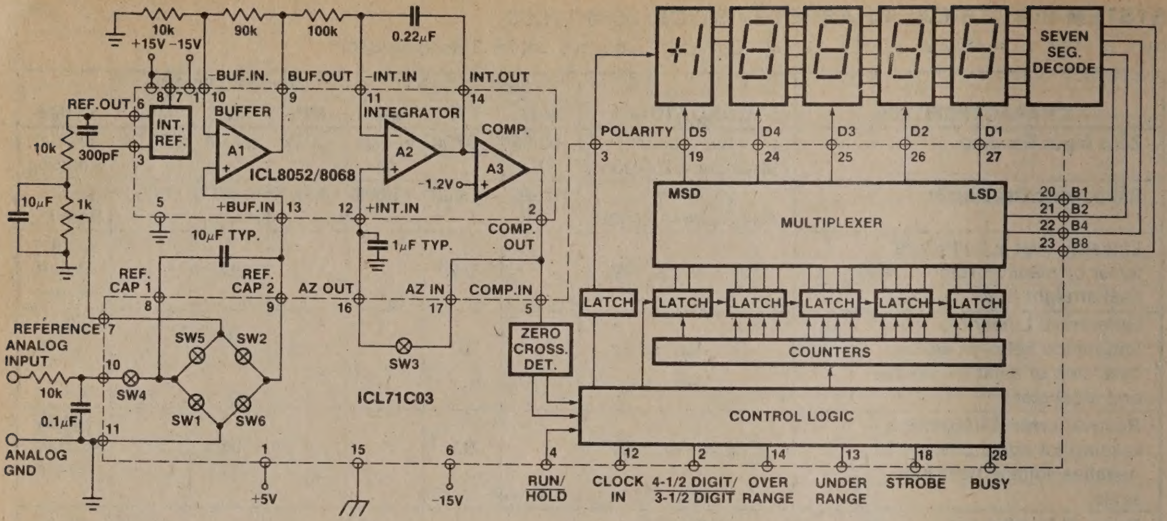

10k
+15V −15V
90k
100k
0.22μF
−BUF.IN.
BUF.OUT
−INT.IN
INT.OUT
REF.OUT 6
8 7 1
10
9
11
14
BUFFER
INTEGRATOR
INT. REF.
COMP.
10k
300pF
3
A1
A2
A3
ICL8052/8068
−1.2V
10μF
1k
5
+BUF.IN 13
12 +INT.IN
2
COMP. OUT
10μF TYP.
1μF TYP.
REF. CAP 1
REF. CAP 2
AZ OUT
AZ IN
COMP.IN
8
9
16
17
5
REFERENCE 7
ANALOG INPUT
10
10k
0.1μF
11
ANALOG GND
SW5
SW2
SW4
SW1
SW6
SW3
ICL71C03
ZERO CROSS. DET.
SEVEN SEG. DECODE
POLARITY
D5
D4
D3
D2
D1
3
19
24
25
26
27
MSD
LSD
MULTIPLEXER
20 B1
21 B2
22 B4
23 B8
LATCH
COUNTERS
CONTROL LOGIC
1
15
6
4
12
2
14
13
18
28
+5V
−15V
RUN/HOLD
CLOCK IN
4-1/2 DIGIT/3-1/2 DIGIT
OVER RANGE
UNDER RANGE
STROBE
BUSY

Figure 1. Functional Block Diagram

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent Circuit of the Analog Section o both the ICL71C03/8052 and the ICL71C03/8068 in the 3 different phases of operation. If the RUN/$\overline{\text{HOLD}}$ pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 40,002 at 4-1/2 digit and 4002 at 3-1/2 digit clock periods per cycle (see Figure 3 for details of conversion timing).

1. **Auto-Zero Phase I** Fig. 2A.
   During Auto-Zero, the input of the circuit is shorted to ANALOG GROUND through switch 1, and switch 3 closes a loop around the integrator and comparator, the purpose of which is to charge the auto-zero capacitor until the integrator output does not change with time. Also, switches 1 and 2 recharge the reference capacitor to V_{REF}.

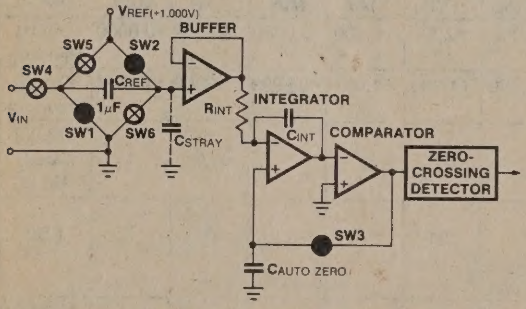

VREF(+1.000V)
BUFFER
SW5
SW2
SW4
CREF
1μF
VIN
SW1
SW6
RINT
CSTRAY
INTEGRATOR
CINT
COMPARATOR
ZERO-CROSSING DETECTOR
SW3
CAUTO ZERO

Figure 2A: Phase I Auto-Zero

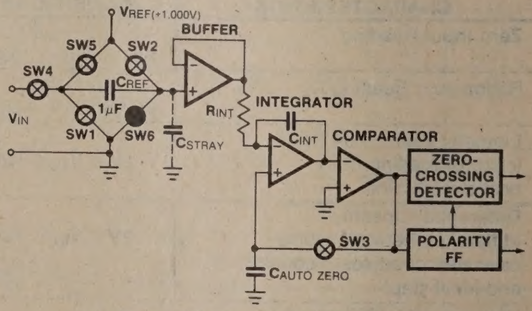

VREF(+1.000V)
BUFFER
SW5
SW2
SW4
CREF
1μF
VIN
SW1
SW6
RINT
CSTRAY
INTEGRATOR
CINT
COMPARATOR
ZERO-CROSSING DETECTOR
POLARITY FF
SW3
CAUTO ZERO

Figure 2C: Phase III + Deintegrate

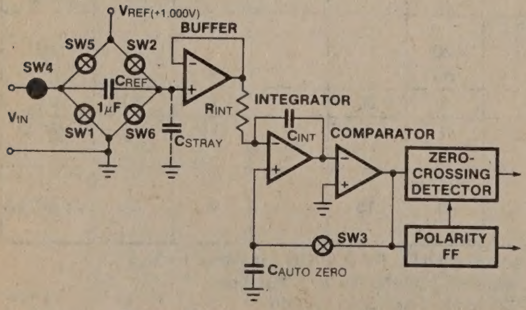

VREF(+1.000V)
BUFFER
SW5
SW2
SW4
CREF
1μF
VIN
SW1
SW6
RINT
CSTRAY
INTEGRATOR
CINT
COMPARATOR
ZERO-CROSSING DETECTOR
POLARITY FF
SW3
CAUTO ZERO

Figure 2B: Phase II Integrate Input

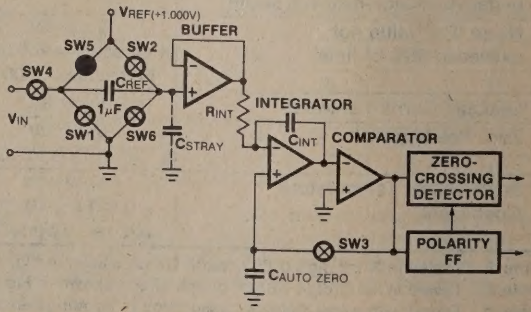

VREF(+1.000V)
BUFFER
SW5
SW2
SW4
CREF
1μF
VIN
SW1
SW6
RINT
CSTRAY
INTEGRATOR
CINT
COMPARATOR
ZERO-CROSSING DETECTOR
POLARITY FF
SW3
CAUTO ZERO

Figure 2D: Phase III - Deintegrate

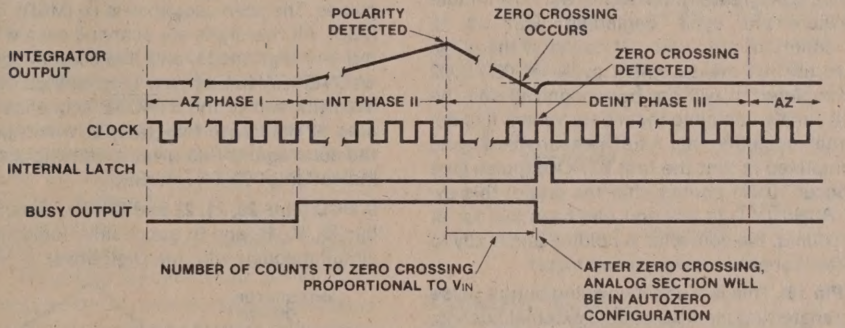
Figure 2: Analog Section of Either ICL8052 or ICL8068 with ICL71C03

2. **Input Integrate Phase II** Fig. 2B.

During Input Integrate the auto-zero loop is opened and the ANALOG INPUT is connected to the BUFFER INPUT through switch 4. If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus, the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

3. **Deintegrate Phase III** Fig. 2C&D.

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switch 6 or 5. If the input signal is positive, switch 6 is closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the BUFFER INPUT. Negative Inputs will cause $\pm V_{REF}$ to be applied to the BUFFER INPUT via switch 5. Thus, the reference capacitor generates the equivalent of a (+) or (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input Integrate phase, the input voltage required to give a full scale reading $= 2V_{REF}$.


POLARITY DETECTED
ZERO CROSSING OCCURS
INTEGRATOR OUTPUT
ZERO CROSSING DETECTED
AZ PHASE I
INT PHASE II
DEINT PHASE III
AZ
CLOCK
INTERNAL LATCH
BUSY OUTPUT
NUMBER OF COUNTS TO ZERO CROSSING PROPORTIONAL TO V_{IN}
AFTER ZERO CROSSING, ANALOG SECTION WILL BE IN AUTOZERO CONFIGURATION

COUNTS			
	Phase I	Phase II	Phase III
4-1/2 digit	10,001	10,000	20,001
3-1/2 digit	1,001	1,000	2,001

Figure 3: Conversion Timing

Zero-Crossing Flip Flop

Fig. 4 shows the problem that the zero-crossing F/F is designed to solve.

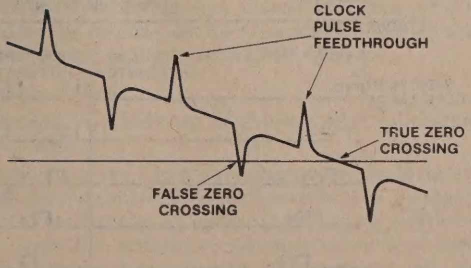

CLOCK PULSE FEEDTHROUGH
TRUE ZERO CROSSING
FALSE ZERO CROSSING

Figure 4: Integrator Output Near Zero-Crossing

The integrator output is approaching the zero-crossing point where the count will be latched and the reading displayed. For a 20,000 count instrument, the ramp is changing approximately 0.50mV per clock pulse (10 volt max integrator output divided by 20,000 counts). The clock pulse feedthrough superimposed upon this ramp would have to be less than 100μV peak to avoid causing significant errors.

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore the counter is disabled for one clock pulse at the beginning of phase 3. This one count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result

DETAILED DESCRIPTION

Digital Section

The 71C03 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

1. **4-1/2/$\overline{\text{3-1/2}}$ (Pin 2).** When high (or open) the internal counter operates as a full 4-1/2 decade counter, with a complete measurement cycle requiring 40,002 counts. When held low, the least significant decade is cleared and the clock is fed directly into the next decade. A measurement cycle now requires only 4,002 clock pulses. All 5 digit drivers are active in either case, with each digit lasting 200 counts with Pin 2 high (4-1/2 digit) and 20 counts for Pin 2 low (3-1/2 digit).

2. **RUN/$\overline{\text{HOLD}}$ (Pin 4).** When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002/4,002 clock pulses. If taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as Pin 4 is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle beginning with up to 10,001/1,001 counts of auto zero. Of course if the pulse occurs before the full measurement cycle (40,002/4,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first $\overline{\text{STROBE}}$ pulse (see below) will occur 101/11 counts after the end of this cycle. Thus, if RUN/$\overline{\text{HOLD}}$ is low and has been low for at least 101/11 counts, the converter is holding and ready to start a new measurement when pulsed high.

3. **$\overline{\text{STROBE}}$ (Pin 18).** This is a negative-going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative-going $\overline{\text{STROBE}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101/11 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201/21 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{STROBE}}$ pulse goes negative for 1/2 clock pulse width. Similarly, after Digit 5, Digit 4 goes high (for 200/20 clock pulses) and 100/10 pulses later the $\overline{\text{STROBE}}$ goes negative for the second time. This continues through Digit 1 (LSD) when the fifth and last $\overline{\text{STROBE}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was over-range) but no additional $\overline{\text{STROBE}}$ pulses will be sent until a new measurement is available.

4. **BUSY (Pin 28).** BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an OVER-RANGE). The internal latches are enabled (i.e., loaded) during the first clock pulse after BUSY and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY so it may also be considered an $\overline{\text{A-Z}}$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001/1,001 counts from the number of pulses received — as mentioned previously there is one "NO-count" pulse in each Reference Integrate cycle.

5. **OVER-RANGE (Pin 4).** This pin goes positive when the input signal exceeds the range (20,000/2,000) of the converter. The output F-F is set at the end of BUSY and is reset to zero at the beginning of Reference Integrate in the next measurement cycle.

6. **UNDER-RANGE (Pin 13).** This pin goes positive when the reading is 9% of range or less. The output F-F is set at the end of BUSY (if the new reading is 1800/180 or less) and is reset at the beginning of Signal Integrate of the next reading.

7. **POLARITY (Pin 3).** This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal (+) and (−) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of Reference Integrate and remains correct until it is revalidated for the next measurement.

8. **Digit Drives (Pins 19, 24, 25, 26 and 27).** Each digit drive is a positive-going signal which lasts for 200/20 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned even when operating in the 3-½ digit mode, and this scan is continuous unless an OVER-RANGE occurs. Then all Digit drives are blanked from the end of the STROBE sequence until the beginning of Reference Integrate, at which time D_5 will start the scan again. This gives a blinking display as a visual indication of OVER-RANGE.

9. **BCD (Pins 20, 21, 22 and 23).** The Binary coded decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the Digit driver.

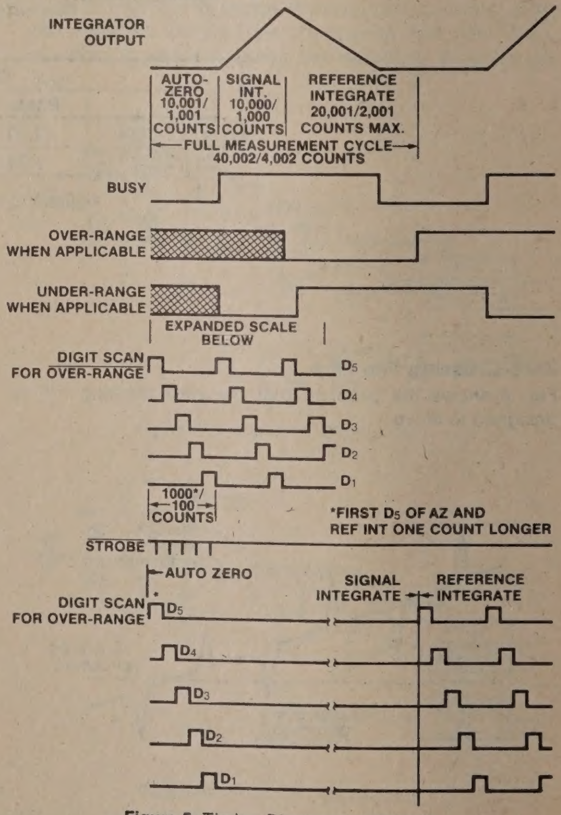

INTEGRATOR OUTPUT
AUTO-ZERO 10,001/1,001 COUNTS
SIGNAL INT. 10,000/1,000 COUNTS
REFERENCE INTEGRATE 20,001/2,001 COUNTS MAX.
FULL MEASUREMENT CYCLE 40,002/4,002 COUNTS
BUSY
OVER-RANGE WHEN APPLICABLE
UNDER-RANGE WHEN APPLICABLE
EXPANDED SCALE BELOW
DIGIT SCAN FOR OVER-RANGE
D5
D4
D3
D2
D1
1000*/100 COUNTS
*FIRST D5 OF AZ AND REF INT ONE COUNT LONGER
STROBE
AUTO ZERO
SIGNAL INTEGRATE
REFERENCE INTEGRATE
DIGIT SCAN FOR OVER-RANGE
D5
D4
D3
D2
D1

Figure 5: Timing Diagram for Outputs

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40μA give good results with a nominal of 20μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}^*}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then -

$$R_{INT} = \frac{(\text{Buffer gain})\ (\text{full scale voltage})}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{\begin{bmatrix}10{,}000\ (4\text{-}1/2\ \text{digit}) \\ 1000\ (3\text{-}1/2\ \text{digit})\end{bmatrix} \text{X clock period} \ \text{X}\ (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 1.0000, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracted from the input voltage while adding to the reference voltage during the next cycle. The result of this is that the noise voltage is effectively somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL71C03 is shown in Figure 6.

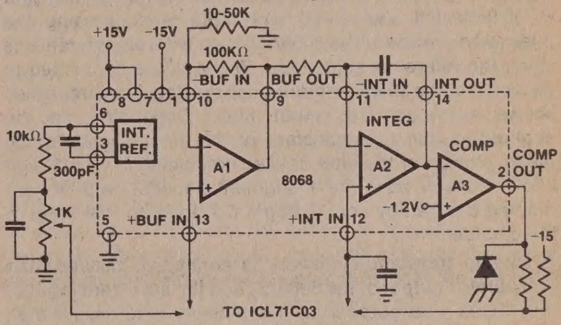


Figure 6: Adding Buffer Gain to ICL8068

ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and is the device of choice for systems where noise is a limiting factor, particularly in low signal level conditions.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit is no exception, even though it is entirely NPN, with an open-loop gain-bandwidth product of 300MHz. The comparator output follows the integrator ramp with a 3μs delay, and at a clock frequency of 160kHz (6μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50μV input, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users. However, if the clock frequency is increased appreciably above 160kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, 33-1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, 166-2/3kHz, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50 and 60Hz.

The clock used should be free from significant phase or frequency jitter. A simple two-gate oscillator and one based on a CMOS 7555 timer are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

APPLICATIONS

Specific Circuits Using the 8068/71C03 8052/71C03

Figure 7 shows the complete circuit for a ±4-1/2 digit (±200.0mV full scale) A/D with LED readout using the internal reference of the 8068/52. If an external reference is used, the reference supply (pin 7) should be connected to ground and the 300pF reference cap deleted. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The 1/2 digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder.

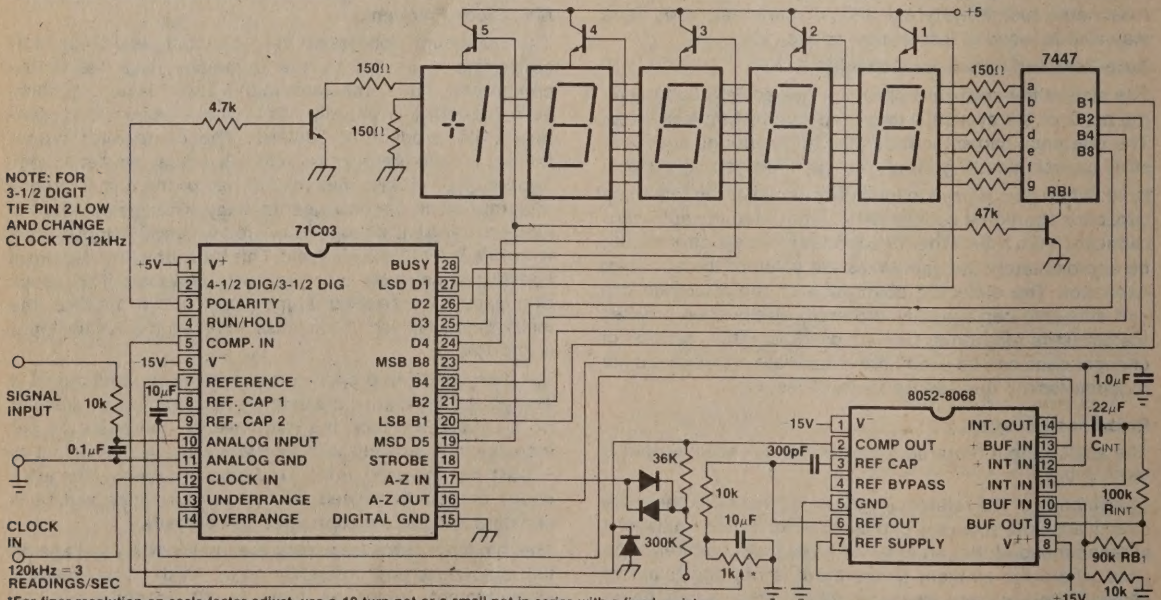
A voltage translation network is connected between the comparator output of the 8068/52 and the auto-zero input of the 71C03. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the 71C03 logic (+2.5V) while the auto-zero capacitor is being charged to V_{REF} (+100.0mV for a 200.0mV instrument). Otherwise, even with zero volts in, some reference integrate period would be required to drive the comparator output to the threshold level. This would show up as an equivalent offset error. Once the divider network has been selected, the unit-to-unit variation should contribute less than a tenth of a count error. A second feature is the back-to-back diodes, used to lower the noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At startup or recovery from an overload, their impedance is low to large signals so that the cap can be charged up in one auto-zero cycle. The buffer gain does not have to be set precisely at 10 since the gain is used in both the integrate and deintegrate phase. For scale factors other than 200.00mV the gain of the buffer should be changed to give a ±2V buffer output. For 2.0000V full scale this means unity gain and for 20,000mV (1μV resolution) a gain of 100 is necessary.* Not all 8068As can operate properly at a gain of 100 since their offset should be less than 10mV in order to accommodate the auto-zero circuitry. However, for devices selected with less than 10mV offset, the noise performance is reasonable with approximately 1.5μV near full scale. On all scales less than 200.00mV, the voltage translation network should be made adjustable as an offset trim.

The auto-zero cap should be 1μF for all scales and the reference capacitor should be 1μF times the gain of the buffer amplifier. At this value if the input leakages of the 8052/8068 are equal, the droop effects will cancel giving zero offset. This is especially important at high temperature. Some typical component values are shown in the table below. For 3-1/2 digit conversion use 12kHz clock.

$V^{++} = +15V$, $V^{+} = 5V$, $V^{-} = -15V$, Clock Freq = 120kHz (4-1/2 digit)

ICL8052/8068 with	ICL71C03A			UNITS
Full scale V_{IN}	20	200	2000	mV
Buffer Gain $\frac{(RB1 + RB2)}{RB2}$	100*	10	1	
R_{INT}	100	100	100	kΩ
C_{INT}	0.22	0.22	0.22	μF
C_{AZ}	1.0	1.0	1.0	μF
C_{REF}	10	10	1.0	μF
V_{REF}	10	100	1000	mV
Resolution (4-1/2 digit)	1	10	100	μV

*Note comment on offset limitations above. Buffer gain does not improve ICL8052 noise performance adequately.


+5
5
4
3
2
1
150Ω
4.7k
150Ω
150Ω
7447
a
b
c
d
e
f
g
B1
B2
B4
B8
RBI
47k
NOTE: FOR 3-1/2 DIGIT TIE PIN 2 LOW AND CHANGE CLOCK TO 12kHz
71C03
+5V
1 V+
2 4-1/2 DIG/3-1/2 DIG
3 POLARITY
4 RUN/HOLD
5 COMP. IN
-15V
6 V−
7 REFERENCE
10μF
8 REF. CAP 1
9 REF. CAP 2
10 ANALOG INPUT
11 ANALOG GND
12 CLOCK IN
13 UNDERRANGE
14 OVERRANGE
BUSY 28
LSD D1 27
D2 26
D3 25
D4 24
MSB B8 23
B4 22
B2 21
LSB B1 20
MSD D5 19
STROBE 18
A-Z IN 17
A-Z OUT 16
DIGITAL GND 15
SIGNAL INPUT
10k
0.1μF
CLOCK IN
120kHz = 3 READINGS/SEC
36K
300K
10k
10μF
1k *
300pF
8052-8068
15V
1 V−
2 COMP OUT
3 REF CAP
4 REF BYPASS
5 GND
6 REF OUT
7 REF SUPPLY
INT. OUT 14
+ BUF IN 13
+ INT IN 12
- INT IN 11
- BUF IN 10
BUF OUT 9
V++ 8
1.0μF
.22μF
CINT
100k RINT
90k RB1
10k RB2
+15V

*For finer resolution on scale factor adjust, use a 10 turn pot or a small pot in series with a fixed resistor.

Figure 7: 8052A (8068A)/71C03A 4-1/2 Digit A-D Converter

A suitable circuit for driving a plasma-type display is shown in Fig. 8. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving 'BI' are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The 2K & 3K resistors set the current levels in the display. A similar arrangement can be used with 'Nixie'® tubes.

® Nixie is a registered trademark of Burroughs Corporation.

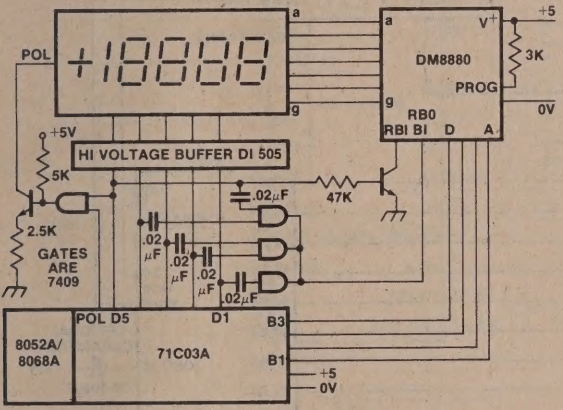

POL
+18888
a
g
a
V+
+5
DM8880
3K
PROG
g
RB0
0V
RBI BI D A
+5V
HI VOLTAGE BUFFER DI 505
5K
47K
.02µF
2.5K
GATES ARE 7409
.02 µF
.02 µF
.02 µF
.02µF
POL D5
D1
B3
8052A/ 8068A
71C03A
B1
+5
0V

Figure 8: ICL8052-8068/71C03A Plasma Display Circuit

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of 8068 or 8052/71C03A circuits, especially in high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. Both of the above circuits have considerable current flowing in the digital ground returns from drivers, etc. A recommended connection sequence for the ground lines is shown in Figure 9.

Other Circuits for Display Applications

The popular LCD displays can be interfaced to the O/P of the ICL71C03 with suitable display drivers, such as the ICM7211A as shown in Figure 10. A standard CMOS 4000 series LCD driver circuit is used for displaying the 1/2 digit, the polarity, and an 'overange' flag. A similar circuit can be used with the ICM7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the 'extra' outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed.

The Figure shows the complete circuit for a 4-1/2 digit (±2.000V) A/D again using the internal reference of the 8052A/8068A.

Figure 11 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the $\overline{\text{Strobe}}$ signal and 'Overange' is indicated by blanking the 4 digits. A clock oscillator circuit using the ICM7555 CMOS timer is shown. Some other suitable clock circuits are suggested in Figs. 12 & 13. The 2-gate circuit should use CMOS gates to maintain good power supply rejection.

A problem sometimes encountered with the 8052/68/71C03 A/D is that of gross over-voltage applied to the input. Voltage in excess of ±2.000 volts may cause the integrator output to saturate. When this occurs, the integrator can no longer source (or sink) the current required to hold the summing junction (Pin 11) at the voltage stored on the auto zero capacitor. As a result, the voltage across the integrator capacitor decreases sufficiently to give a false voltage reading. This problem can also show up as large-signal instability on overange conditions. A simple solution to this problem is to use junction FET transistors across the integrator capacitor to source (or sink) current into the summing junction and prevent the integrator amplifier from saturating, as shown in Figure 14.

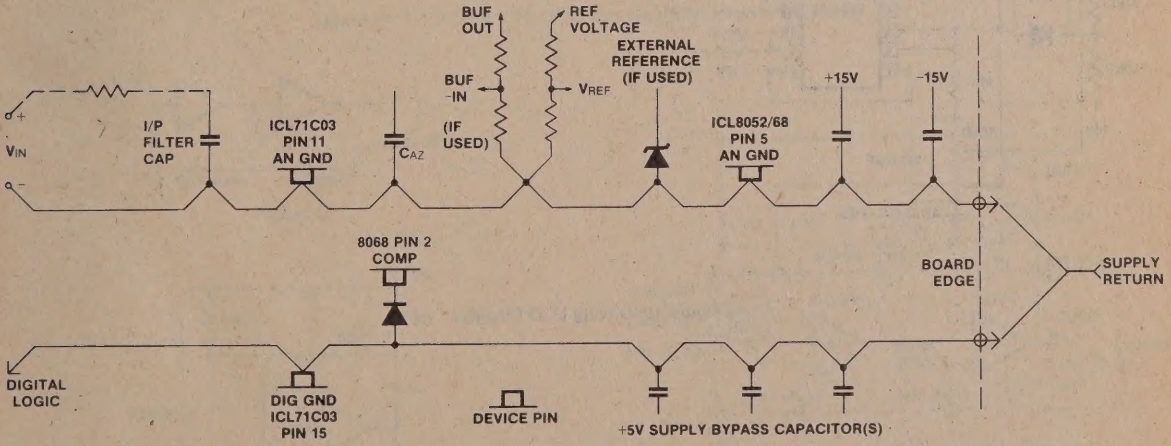

BUF OUT
REF VOLTAGE
EXTERNAL REFERENCE (IF USED)
BUF -IN
VREF
(IF USED)
+15V
-15V
+
VIN
-
I/P FILTER CAP
ICL71C03 PIN 11 AN GND
CAZ
ICL8052/68 PIN 5 AN GND
8068 PIN 2 COMP
BOARD EDGE
SUPPLY RETURN
DIGITAL LOGIC
DIG GND ICL71C03 PIN 15
DEVICE PIN
+5V SUPPLY BYPASS CAPACITOR(S)

Figure 9: Grounding Sequence

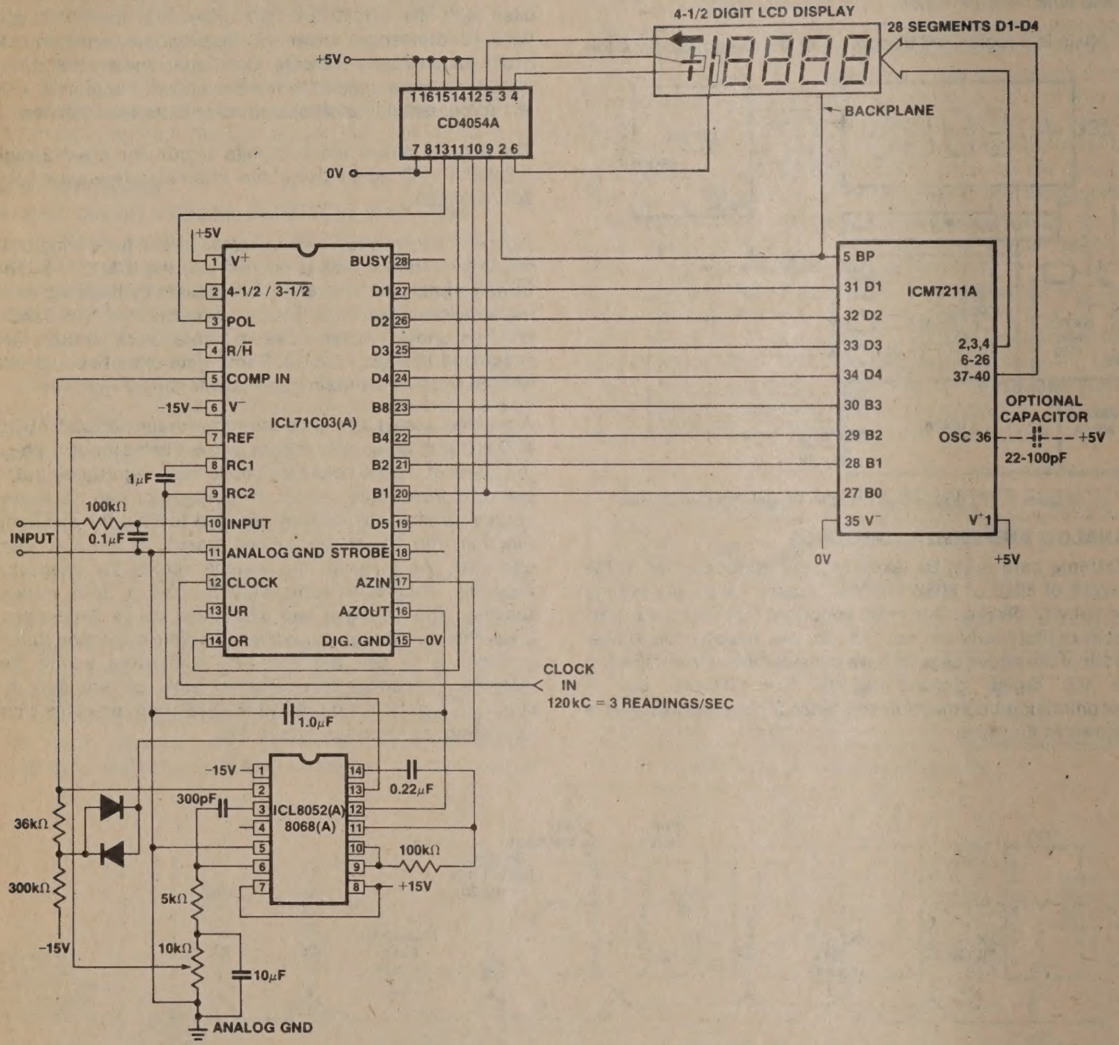

4-1/2 DIGIT LCD DISPLAY
28 SEGMENTS D1-D4
BACKPLANE
+5V
CD4054A
1 16 15 14 12 5 3 4
7 8 13 11 10 9 2 6
0V
+5V
ICL71C03(A)
1 V+
2 4-1/2 / 3-1/2
3 POL
4 R/H
5 COMP IN
6 V−
7 REF
8 RC1
9 RC2
10 INPUT
11 ANALOG GND
12 CLOCK
13 UR
14 OR
BUSY 28
D1 27
D2 26
D3 25
D4 24
B8 23
B4 22
B2 21
B1 20
D5 19
STROBE 18
AZIN 17
AZOUT 16
DIG. GND 15
−15V
1μF
100kΩ
INPUT
0.1μF
0V
CLOCK IN
120kC = 3 READINGS/SEC
1.0μF
ICM7211A
5 BP
31 D1
32 D2
33 D3
34 D4
30 B3
29 B2
28 B1
27 B0
35 V−
2,3,4
6-26
37-40
OSC 36
V+ 1
OPTIONAL CAPACITOR
22-100pF
+5V
0V
+5V
ICL8052(A)
8068(A)
−15V
300pF
0.22μF
100kΩ
+15V
36kΩ
300kΩ
−15V
5kΩ
10kΩ
10μF
ANALOG GND

Figure 10: Driving LCD Displays

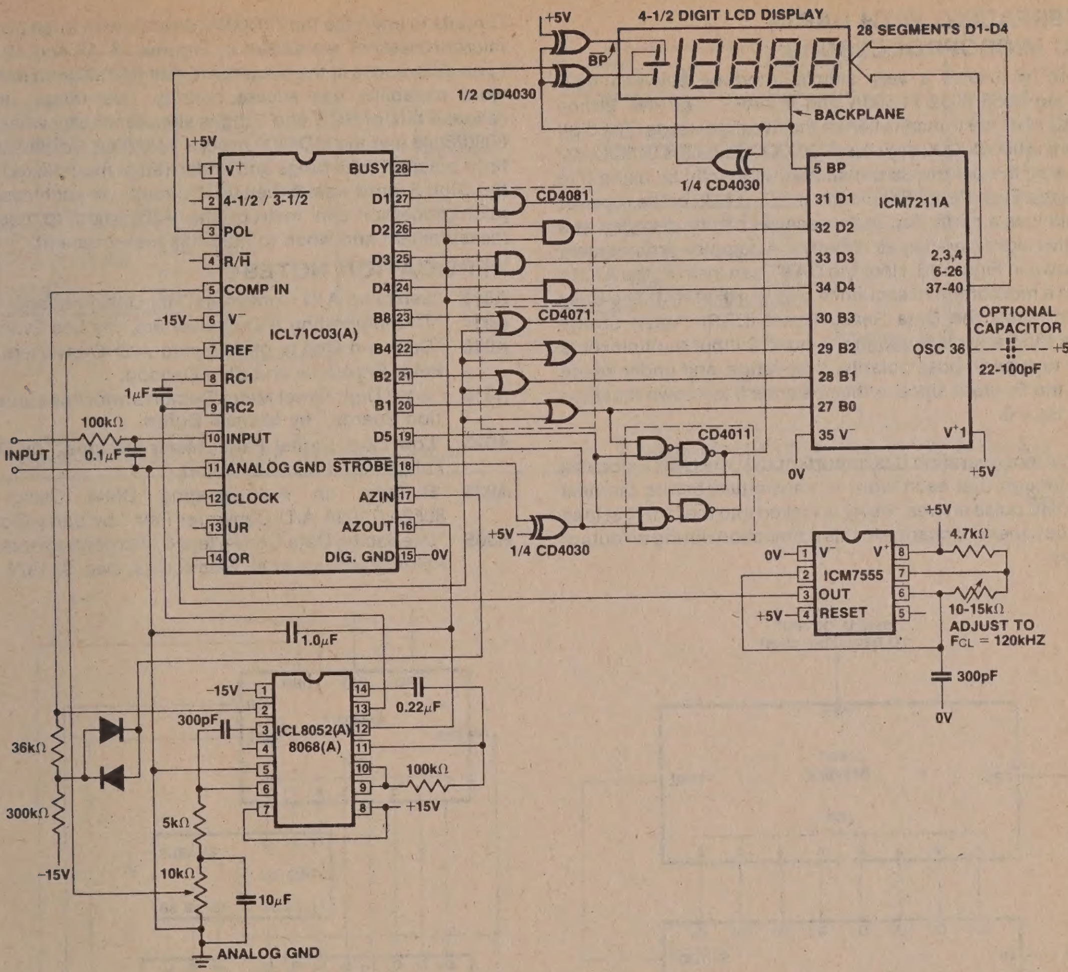

+5V
4-1/2 DIGIT LCD DISPLAY
28 SEGMENTS D1-D4
BP
1/2 CD4030
BACKPLANE
1/4 CD4030
+5V
1 V+
2 4-1/2 / 3-1/2
3 POL
4 R/H
5 COMP IN
-15V 6 V-
7 REF
8 RC1
9 RC2
10 INPUT
11 ANALOG GND
12 CLOCK
13 UR
14 OR
BUSY 28
D1 27
D2 26
D3 25
D4 24
B8 23
B4 22
B2 21
B1 20
D5 19
STROBE 18
AZIN 17
AZOUT 16
DIG. GND 15 0V
ICL71C03(A)
1µF
100kΩ
INPUT
0.1µF
CD4081
CD4071
CD4011
+5V
1/4 CD4030
5 BP
31 D1
32 D2
33 D3
34 D4
30 B3
29 B2
28 B1
27 B0
35 V-
ICM7211A
2,3,4
6-26
37-40
OSC 36
V+1
OPTIONAL CAPACITOR
22-100pF
+5V
0V
+5V
0V 1 V-
2
3 OUT
+5V 4 RESET
ICM7555
V+ 8
7
6
5
4.7kΩ
10-15kΩ
ADJUST TO
FCL = 120kHZ
300pF
0V
1.0µF
-15V 1
2
300pF 3
4
5
6
7
ICL8052(A)
8068(A)
14
13
12
11
10
9
8 +15V
0.22µF
100kΩ
36kΩ
300kΩ
-15V
5kΩ
10kΩ
10µF
ANALOG GND

Figure 11: 4-1/2 Digit LCD DPM with Digit Blanking on Overrange.

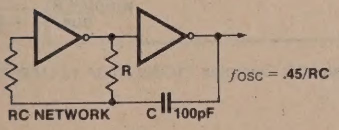

R
fosc = .45/RC
RC NETWORK
C
100pF

Figure 12

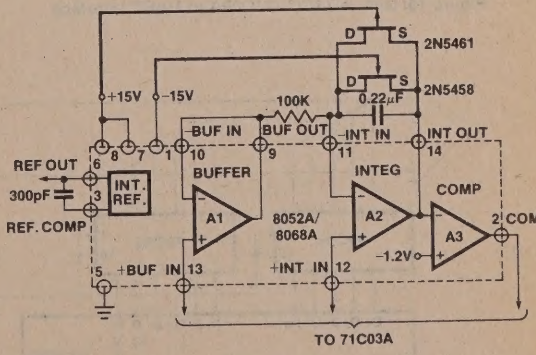

D
S
2N5461
D
S
2N5458
0.22µF
+15V
-15V
100K
-BUF IN
BUF OUT
-INT IN
INT OUT
6
8
7
1
10
9
11
14
REF OUT
300pF
REF. COMP
3
INT. REF.
BUFFER
A1
8052A/
8068A
INTEG
A2
COMP
A3
2 COMP
-1.2V
5 +BUF IN 13
+INT IN 12
TO 71C03A

Figure 14: Gross Overvoltage Protection Circuit

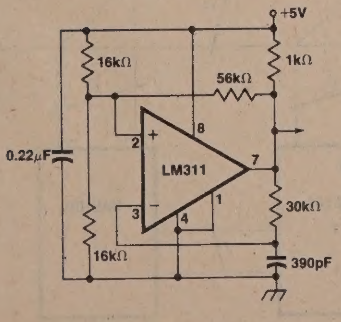

+5V
16kΩ
1kΩ
56kΩ
0.22µF
2
8
7
LM311
1
3
4
30kΩ
16kΩ
390pF

Figure 13: Clock Circuits

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 15 shows a very simple interface between free-running 8068/8052/71C03A and a UART. The five Strobe pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 16. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The Busy signal resets the Data Ready Reset (DRR). Again Strobe starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next STROBE pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the 71C03(A) directly with three popular microprocessors are shown in Figures 17, 18 and 19. The main differences in the circuits are that IM6100 with its 12 bit word capability can accept polarity, over-range, under-range, 4 bits of BCD and 5 digits simultaneously where the 8080/8048 and the MD6800 groups with 8 bit words need to have polarity, over-range and under-range multiplexed onto the Digit 5 word - as in the UART circuits. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

APPLICATION NOTES

A016	"Selecting A/D Converters," by David Fullagar
A017	"The Integrating A/D Converters," by Lee Evans
A018	"Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A019	"4-1/2 Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort
A023	"Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort
A028	"Building an Auto-Ranging DMM Using the 8052A/7103A A/D Converter Pair," by Larry Goff
R005	"Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

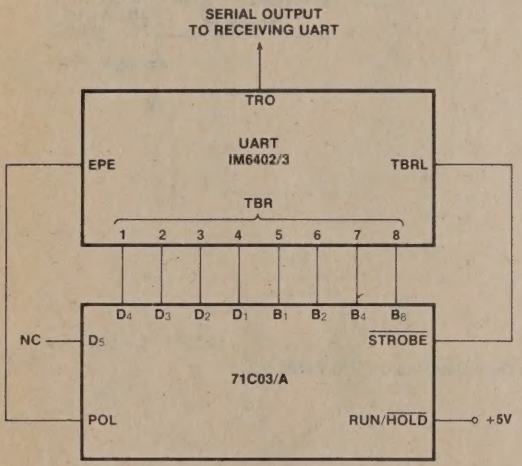

SERIAL OUTPUT
TO RECEIVING UART
TRO
UART
IM6402/3
EPE
TBRL
TBR
1 2 3 4 5 6 7 8
D4 D3 D2 D1 B1 B2 B4 B8
NC
D5
STROBE
71C03/A
POL
RUN/HOLD
+5V

Figure 15: Simple 71C03/71C03A to UART Interface

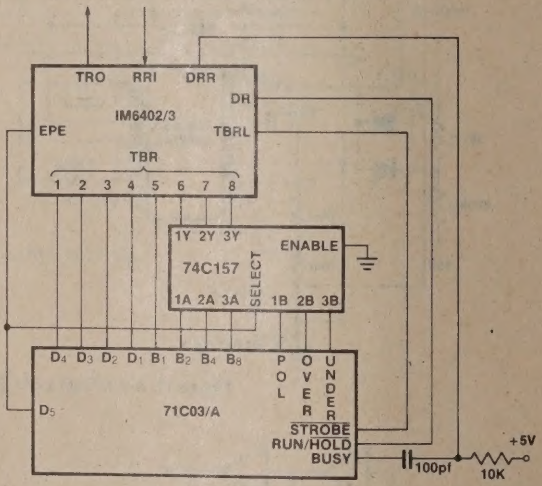

TRO
RRI
DRR
DR
IM6402/3
EPE
TBRL
TBR
1 2 3 4 5 6 7 8
1Y 2Y 3Y
ENABLE
74C157
SELECT
1A 2A 3A
1B 2B 3B
D4 D3 D2 D1 B1 B2 B4 B8
POL
OVER
UNDER
D5
71C03/A
STROBE
RUN/HOLD
BUSY
100pf
+5V
10K

Figure 16: Complex 71C03/7103A to UART Interface

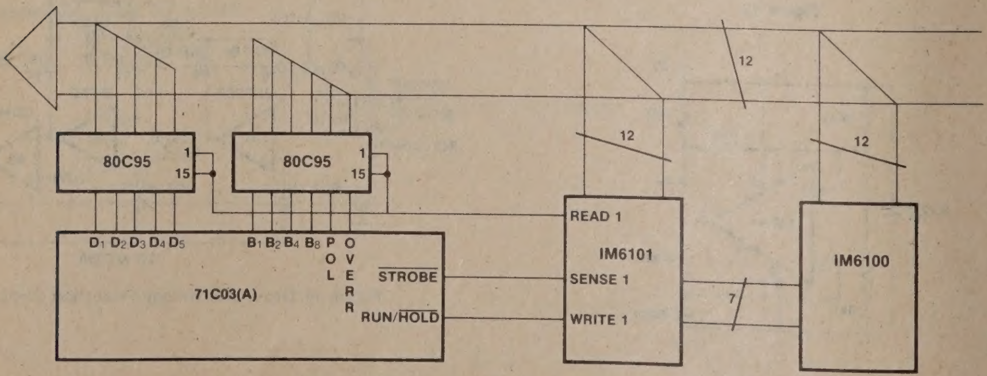

12
12
12
80C95
1
15
80C95
1
15
D1 D2 D3 D4 D5
B1 B2 B4 B8
POL
OVER
STROBE
71C03(A)
RUN/HOLD
READ 1
IM6101
SENSE 1
WRITE 1
7
IM6100

Figure 17: IM6100 to 71C03/71C03A Interface

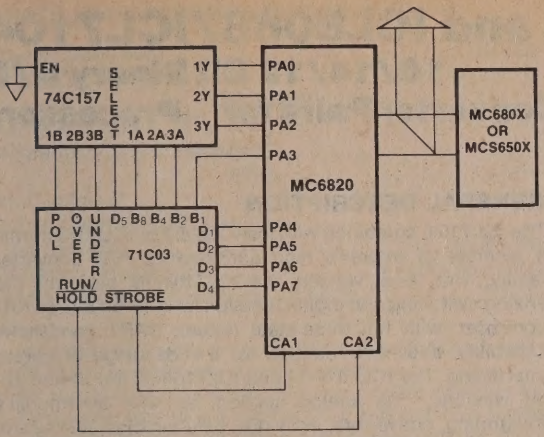

EN
74C157
SELECT
1Y
2Y
3Y
1B 2B 3B
1A 2A 3A
PA0
PA1
PA2
PA3
MC6820
MC680X OR MCS650X
POL
OVER
UNDER
D5 B8 B4 B2 B1
D1
D2
D3
D4
71C03
RUN/HOLD
STROBE
PA4
PA5
PA6
PA7
CA1
CA2

Figure 18: ICL71C03 to MC6800, MCS650X Interface

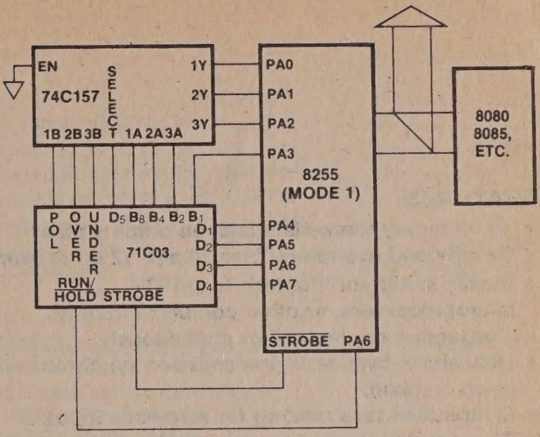

EN
74C157
SELECT
1Y
2Y
3Y
1B 2B 3B
1A 2A 3A
PA0
PA1
PA2
PA3
8255 (MODE 1)
8080 8085, ETC.
POL
OVER
UNDER
D5 B8 B4 B2 B1
D1
D2
D3
D4
71C03
RUN/HOLD
STROBE
PA4
PA5
PA6
PA7
STROBE
PA6

Figure 19: ICL71C03 to MCS-48, -80, 85 Interface

ICL8052/ICL7104
and ICL8068/ICL7104
16/14/12 Bit Binary A/D Converter Pairs for µProcessors

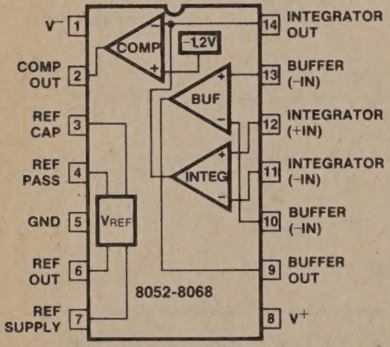
FEATURES

- **16 bit binary three-state latched outputs plus polarity and overrange. Also 14 and 12 bit versions.**
- **Ideally suited for interface to UARTs, microprocessors, or other complex circuitry.**
- **Conversion on demand or continuously.**
- **Handshake byte-serial transmission synchronously or on demand.**
- **Guaranteed zero reading for zero volts input.**
- **True polarity at zero count for precise null detection.**
- **Single reference voltage for true ratiometric operation.**
- **Onboard clock and reference.**
- **Auto-Zero; Auto-Polarity**
- **Accuracy guaranteed to 1 count.**
- **All outputs TTL compatible.**
- **±10V analog input range**
- **Status signal available for external sync, A/Z in preamp, etc.**

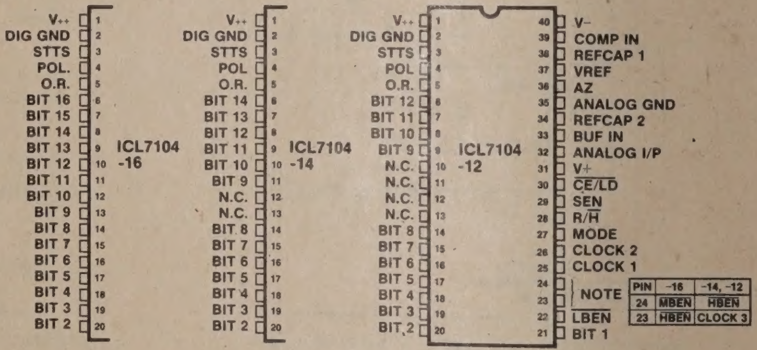
GENERAL DESCRIPTION

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Intersil's high performance A/D converter family. The 16-bit version, the ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output, UART handshake capability, and other outputs for a wide range of output interfacing. The ICL7014-14 and ICL7104-12 are 14 and 12-bit versions. The analog section, as with all Intersil's integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc.

PIN CONFIGURATIONS


V⁻ 1
COMP OUT 2
REF CAP 3
REF PASS 4
GND 5
REF OUT 6
REF SUPPLY 7
8 V⁺
9 BUFFER OUT
10 BUFFER (−IN)
11 INTEGRATOR (−IN)
12 INTEGRATOR (+IN)
13 BUFFER (−IN)
14 INTEGRATOR OUT
COMP
−1.2V
BUF
INTEG
VREF
8052-8068

(OUTLINE DWGS DD,JD,PD)


ICL7104 -16
V++ 1
DIG GND 2
STTS 3
POL. 4
O.R. 5
BIT 16 6
BIT 15 7
BIT 14 8
BIT 13 9
BIT 12 10
BIT 11 11
BIT 10 12
BIT 9 13
BIT 8 14
BIT 7 15
BIT 6 16
BIT 5 17
BIT 4 18
BIT 3 19
BIT 2 20
ICL7104 -14
V++ 1
DIG GND 2
STTS 3
POL 4
O.R. 5
BIT 14 6
BIT 13 7
BIT 12 8
BIT 11 9
BIT 10 10
BIT 9 11
N.C. 12
N.C. 13
BIT 8 14
BIT 7 15
BIT 6 16
BIT 5 17
BIT 4 18
BIT 3 19
BIT 2 20
ICL7104 -12
V++ 1
DIG GND 2
STTS 3
POL 4
O.R. 5
BIT 12 6
BIT 11 7
BIT 10 8
BIT 9 9
N.C. 10
N.C. 11
N.C. 12
N.C. 13
BIT 8 14
BIT 7 15
BIT 6 16
BIT 5 17
BIT 4 18
BIT 3 19
BIT 2 20
21 BIT 1
22 LBEN
23
24 NOTE
25 CLOCK 1
26 CLOCK 2
27 MODE
28 R/H
29 SEN
30 CE/LD
31 V+
32 ANALOG I/P
33 BUF IN
34 REFCAP 2
35 ANALOG GND
36 AZ
37 VREF
38 REFCAP 1
39 COMP IN
40 V−
PIN | −16 | −14, −12
24 | MBEN | HBEN
23 | HBEN | CLOCK 3

(OUTLINE DWGS DL,JL,PL)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14-Pin Plastic DIP	ICL8052CPD
8052	0°C to 70°C	14-Pin Ceramic DIP	ICL8052CDD
8052A	0°C to 70°C	14-Pin Plastic DIP	ICL8052ACPD
8052A	0°C to 70°C	14-Pin Ceramic DIP	ICL8052ACDD
8068	0°C to 70°C	14-Pin CERDIP	ICL8068CJD
8068A	0°C to 70°C	14-Pin CERDIP	ICL8068ACJD

Part	Temp. Range	Package	Order Number
7104 12-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-12CJL
7104 12-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-12CPL
7104 12-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-12CDL
7104 14-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-14CJL
7104 14-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-14CPL
7104 14-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-14CDL
7104 16-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-16CJL
7104 16-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-16CPL
7104 16-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-16CDL

ABSOLUTE MAXIMUM RATINGS

Power Dissipation[1] 500mW
Storage Temperature .... −65° C to +150° C

8052, 8068

Supply Voltage .... ±18V
Differential Input Voltage (8068) .... ±30V
(8052) .... ±6V
Input Voltage[2] .... ±15V
Output Short Circuit Duration,
All Outputs[3] .... Indefinite
Operating Temperature .... 0° C to +70° C
Lead Temperature (Soldering, 10 Sec.) .... 300° C

7104

V+ Supply (GND to V+) 12V
V++ to V− 32V
Positive Supply Voltage (GND to V++) 17V
Negative Supply Voltage (GND to V−) 17V
Analog Input Voltage (Pin 32-39)[4] .... V+ to V−
Digital Input Voltage .... V++0.3V
(Pins 2-30)[5] .... GND −0.3V

Notes:

1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70° C. For higher temperatures, derate 10mW/° C.

2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

3: Short circuit may be to ground or either supply. Rating applies to +70° C ambient temperature.

4: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

5: Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ICL7104 before its power supply is established.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7104 ELECTRICAL CHARACTERISTICS (V+ = +5V, V++ = +15V, V− = −15V, Ta = 25° C)

CHARACTERISTICS		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Input	CLOCK 1	I_{IN}	Vin = +5V to 0V	±2	±7	±30	μA
Comparator I/P	COMP IN (Note 1)	I_{IN}	Vin = 0V to +5V	−10	±0.001	+10	μA
Inputs with Pulldown	MODE	I_{IH}	Vin = +5V	+1	+5	+30	μA
		I_{IL}	Vin = 0V	−10	±0.01	+10	μA
Inputs with Pullups	SEN, R/$\overline{\text{H}}$ $\overline{\text{LBEN}}$, $\overline{\text{MBEN}}$, HBEN, CE/LD (Note 2)	I_{IH}	Vin = +5V	−10	±0.01	+10	μA
		I_{IL}	Vin = 0V	−30	−5	−1	μA
Input High Voltage	All Digital Inputs	V_{IH}		2.5	2.0	—	V
Input Low Voltage	All Digital Inputs	V_{IL}			1.5	1.0	V
Digital Outputs Three-Stated On	$\overline{\text{LB EN}}$ $\overline{\text{MB EN}}$ (16 only) $\overline{\text{HB EN}}$ $\overline{\text{CE/LD}}$ (Note 3) BIT n, POL, OR	V_{OL}	I_{OL} = 1.6 mA	—	.27	.4	V
		V_{OH}	I_{OH} = −10μA		4.5	—	V
		V_{OH}	I_{OH} = −240μA	2.4	3.5	—	V
Digital Outputs Three-Stated Off	BIT n, POL, OR	I_{OL}	0 ≤ Vout ≤ V+	−10	±.001	+10	μA
Non-Three-State Digital Output	STTS	V_{OL}	I_{OL} = 3.2 mA	—	.3	.4	V
		V_{OH}	I_{OH} = −400μA	2.4	3.3	—	V
	CLOCK 2	V_{OL}	I_{OL} = 320μA		0.5		V
		V_{OH}	I_{OH} = −320μA		4.5		V
	CLOCK 3 (-12, -14 ONLY)	V_{OL}	I_{OL} = 1.6 mA		.27	.4	V
		V_{OH}	I_{OH} = −320μA	2.4	3.5		V
Switch	Switch 1	$r_{DS(on)}$		—	25k		Ω
	Switches 2,3	$r_{DS(on)}$		—	4k	20k	Ω
	Switches 4,5,6,7,8,9	$r_{DS(on)}$		—	2k	10k	Ω
	Switch Leakage	$I_{D(off)}$		—	15		pA
Clock	Clock Freq. (Note 4)			DC	200	400	kHz
Supply Currents	+5V Supply Current All outputs high impedance	I+	Freq. = 200 kHz		200	600	μA
	+15V Supply Current	I++	Freq. = 200 kHz		.3	1.0	mA
	−15V Supply Current	I−	Freq. = 200 kHz		25	200	μA
Supply Voltage Range	Logic Supply	V+	Note 5	4.0		+11.0	V
	Positive Supply	V++		+10.0		+16.0	V
	Negative Supply	V−		−16.0		−10.0	V

Note 1: This spec applies when not in Auto-Zero phase.
Note 2: Apply only when these pins are inputs, i.e., the mode pin is low, and the 7104 is not in handshake mode.
Note 3: Apply only when these pins are outputs, i.e., the mode pin is high or the 7104 is in handshake mode.
Note 4: Clock circuit shown in Figs. 10 and 11.
Note 5: V+ must not be more positive than V++.

8068 ELECTRICAL CHARACTERISTICS (V_{SUPP} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTICS	CONDITIONS	8068 MIN	8068 TYP	8068 MAX	8068A MIN	8068A TYP	8068A MAX	UNITS
EACH OPERATIONAL AMPLIFIER									
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	65		20	65	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		175	250		80	150	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
A_V	Large Signal Voltage Gain	R_L = 50kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			2			2		MHz
I_{SC}	Output Short-Circuit Current			5	10		5	10	mA
COMPARATOR AMPLIFIER									
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE									
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		ohms
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPP}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPP}	Supply Current Total				14		8	14	mA

8052 ELECTRICAL CHARACTERISTICS (V_{SUPP} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTICS	CONDITIONS	8052 MIN	8052 TYP	8052 MAX	8052A MIN	8052A TYP	8052A MAX	UNITS
EACH OPERATIONAL AMPLIFIER									
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	50		20	50	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		5	50		2	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
A_V	Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			1			1		MHz
I_{SC}	Output Short-Circuit Current			20	100		20	100	mA
COMPARATOR AMPLIFIER									
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE									
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		ohms
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPP}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPP}	Supply Current Total			6	12		6	12	mA

Note 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA\,Pd$ where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 2: This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS: 8068/7104

(V_{++} = +15V, V_{+} = +5V, V_{-} = −15V Clock Frequency = 200KHz

		8068A/7104-12			8068A/7104-14			8068A/7104-16			
CHARACTERISTICS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	−.000	±.000	+.000	−0.0000	±0.0000	+0.0000	−0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (1)	V_{in} = $V_{Ref.}$ Full Scale = 4.000V	7FF	800	801	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	−4V ≤ V_{in} ≤ +4V		0.2	1		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step	−4V ≤ V_{in} ≤ +4V		.01			.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 4V$		0.2	1		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		3			2			2		μV
Leakage Current at Input (2)	V_{in} = 0V		200	265		100	165		100	165	pA
Zero Reading Drift	V_{in} = 0V 0°C ≤ T_A ≤ 70°C		1	5		0.5	2		0.5	2	μV/°C
Scale Factor Temperature (3) Coefficient	V_{in} = +4V 0 ≤ T_A ≤ 50°C (ext. ref. 0 ppm/°C)		2	5		2	5		2	5	ppm/°C

SYSTEM ELECTRICAL CHARACTERISTICS: 8052/7104

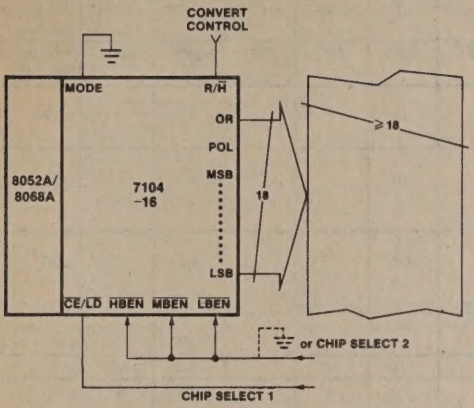
(V_{++} = +15V, V_{+} = +5V, V_{-} = −15V Clock Frequency = 200KHz

		8052/7104-12			8052A/7104-14			8052A/7104-16			
CHARACTERISTICS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	−.000	±.000	+.000	−0.0000	±0.0000	+0.0000	−0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (3)	V_{in} = $V_{Ref.}$ Full Scale = 4.000V	7FF	800	801	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	−4V ≤ V_{in} ≤ +4V		0.2	1		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step)	−4V ≤ V_{in} ≤ +4V		.01			.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 4V$		0.2	1		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		20 50			30			30		μV
Leakage Current at Input (2)	V_{in} = 0V		30	80		20	30		20	30	pA
Zero Reading Drift	V_{in} = 0V 0° ≤ T_A ≤ 70°C		1	5		0.5	2		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +4V 0 ≤ T_A ≤ 70°C (ext. ref. 0 ppm/°C)		3	15		2	5		2	5	ppm/°C

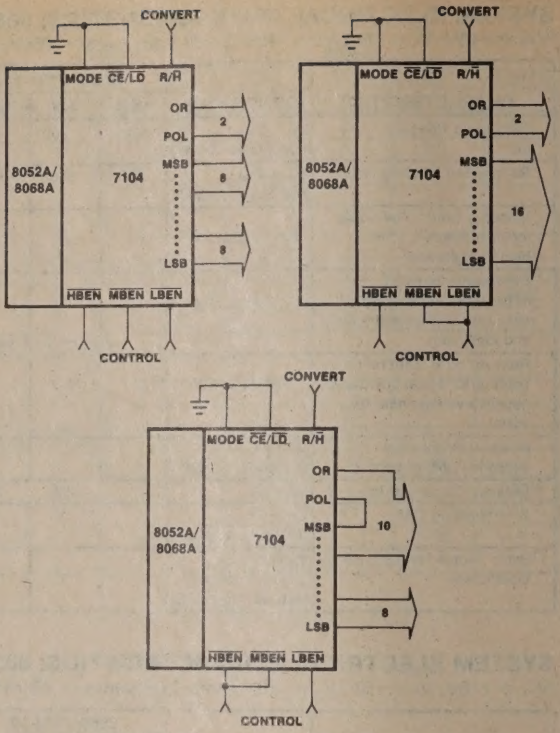
Note 1: Tested with low dielectric absorption integrating capacitor.

Note 2: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA\,Pd$ where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 3: The temperature range can be extended to 70°C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068. See note 2 above.


CONVERT
CONTROL
MODE
R/$\overline{H}$
OR
POL
MSB
LSB
8052A/
8068A
7104
−16
18
≥18
$\overline{CE}$/LD
$\overline{HBEN}$
$\overline{MBEN}$
$\overline{LBEN}$
or CHIP SELECT 2
CHIP SELECT 1

Full 18 Bit Three State Output


CONVERT
MODE
$\overline{CE}$/$\overline{LD}$
R/$\overline{H}$
OR
POL
MSB
LSB
8052A/
8068A
7104
2
8
8
16
10
$\overline{HBEN}$
$\overline{MBEN}$
$\overline{LBEN}$
CONTROL

Various Combinations of Byte Disables

AC CHARACTERISTICS (V++ = +15V, V+ = +5V, V− = −15V)

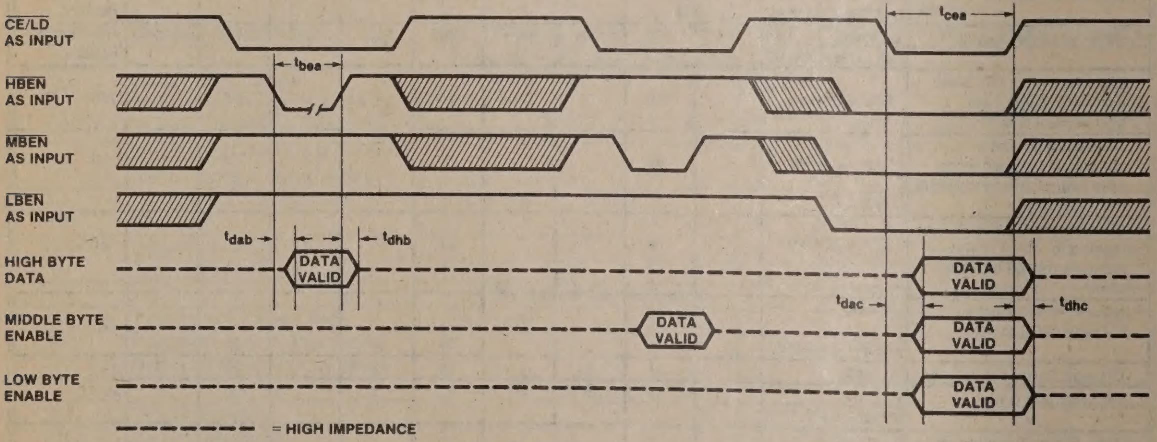

$\overline{CE}$/$\overline{LD}$
AS INPUT
$\overline{HBEN}$
AS INPUT
$\overline{MBEN}$
AS INPUT
$\overline{LBEN}$
AS INPUT
HIGH BYTE
DATA
MIDDLE BYTE
ENABLE
LOW BYTE
ENABLE
t_{bea}
t_{cea}
t_{dab}
t_{dhb}
t_{dac}
t_{dhc}
DATA
VALID
= HIGH IMPEDANCE

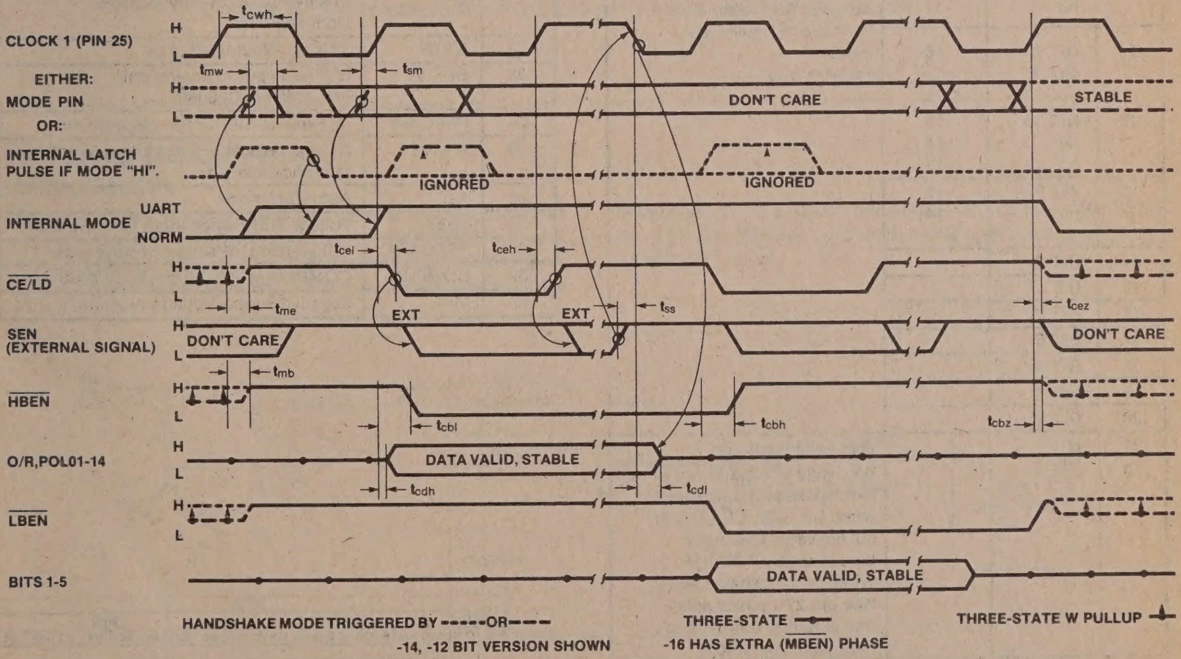
TABLE 1: Direct Mode Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{bea}	$\overline{XBEN}$ Min. Pulse Width		500		ns
t_{dab}	Data Access Time from $\overline{XBEN}$		200		
t_{dhb}	Data Hold Time from $\overline{XBEN}$		200		
t_{cea}	$\overline{CE}$/$\overline{LD}$ Min. Pulse Width		500		
t_{dac}	Data Access Time from $\overline{CE}$/$\overline{LD}$		200		
t_{dhc}	Data Hold Time from $\overline{CE}$/$\overline{LD}$		200		
t_{cwh}	CLOCK 1 High Time	1250	1000		

TABLE 2: Handshake Timing Requirements

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{mw}	MODE Pulse (minimum)		20		ns
t_{sm}	MODE pin set-up time		−150		
t_{me}	MODE pin high to low Z $\overline{\text{CE/LD}}$ high delay		200		
t_{mb}	MODE pin high to $\overline{\text{XBEN}}$ low Z (high) delay		200		
t_{cel}	CLOCK 1 high to $\overline{\text{CE/LD}}$ low delay		700		
t_{ceh}	CLOCK 1 high to $\overline{\text{CE/LD}}$ high delay		600		
t_{cbl}	CLOCK 1 high to $\overline{\text{XBEN}}$ low delay		900		
t_{cbh}	CLOCK 1 high to $\overline{\text{XBEN}}$ high delay		700		
t_{cdh}	CLOCK 1 high to data enabled delay		1100		
t_{cdl}	CLOCK 1 low to data disabled delay		1100		
t_{ss}	Send ENable set-up time		−350		
t_{cbz}	CLOCK 1 high to $\overline{\text{XBEN}}$ disabled delay		2000		
t_{cez}	CLOCK 1 high to $\overline{\text{CE/LD}}$ disabled delay		2000		
t_{cwh}	CLOCK 1 High Time	1250	1000		

4



CLOCK 1 (PIN 25)
H
L
tcwh
EITHER:
MODE PIN
OR:
tmw
tsm
DON'T CARE
STABLE
INTERNAL LATCH PULSE IF MODE "HI".
IGNORED
IGNORED
INTERNAL MODE
UART
NORM
CE/LD
tcel
tceh
tme
EXT
EXT
tss
tcez
SEN (EXTERNAL SIGNAL)
DON'T CARE
DON'T CARE
HBEN
tmb
tcbl
tcbh
tcbz
O/R,POL01-14
DATA VALID, STABLE
tcdh
tcdl
LBEN
BITS 1-5
DATA VALID, STABLE
HANDSHAKE MODE TRIGGERED BY -----OR---
-14, -12 BIT VERSION SHOWN
THREE-STATE
-16 HAS EXTRA (MBEN) PHASE
THREE-STATE W PULLUP

Timing Relationships In Handshake Mode

TABLE 3: Pin Assignment and Function Description

PIN	SYMBOL	OPTION	DESCRIPTION
1	V(++)		Positive Supply Voltage Nominally +15V
2	GND		Digital Ground .0V, ground return
3	STTS		STaTuS output .HI during Integrate and Deintegrate until data is latched .LO when analog section is in Auto-Zero configuration.
4	POL		POLarity. Three-state output. HI for positive input.
5	OR		OverRange. Three-state output.
6	BIT 16 BIT 14 BIT 12	−16 −14 −12	(Most significant bit)
7	BIT 15 BIT 13 BIT 11	−16 −14 −12	Data Bits, Three-state outputs. See Table 4 for format of $\overline{\text{EN}}$ables and bytes. HIGH = true
8	BIT 14 BIT 12 BIT 10	−16 −14 −12	
9	BIT 13 BIT 11 BIT 9	−16 −14 −12	
10	BIT 12 BIT 10 nc	−16 −14 −12	
11	BIT 11 BIT 9 nc	−16 −14 −12	
12	BIT 10 nc nc	−16 −14 −12	
13	BIT 9 nc nc	−16 −14 −12	
14	BIT 8		
15	BIT 7		
16	BIT 6		
17	BIT 5		
18	BIT 4		
19	BIT 3		
20	BIT 2		
21	BIT 1		Least significant bit
22	$\overline{\text{LBEN}}$		$\overline{\text{L}}$ow $\overline{\text{B}}$yte $\overline{\text{EN}}$able. If not in handshake mode (see pin 27) when LO (with $\overline{\text{CE}}/\overline{\text{LD}}$, pin 30) activates low-order byte outputs, BITS 1-8 When in handshake mode (see pin 27), serves as a low-byte flag output. See Figures 8, 9 and 10.
	$\overline{\text{MBEN}}$	−16	$\overline{\text{M}}$id $\overline{\text{B}}$yte $\overline{\text{EN}}$able. Activates BITS 9-16, see $\overline{\text{LBEN}}$ (pin 22)
23	$\overline{\text{HBEN}}$	−14 −12	$\overline{\text{H}}$igh $\overline{\text{B}}$yte $\overline{\text{EN}}$able. Activates BITS 9-14, POL, OR, see $\overline{\text{LBEN}}$ (pin 22)
	$\overline{\text{HBEN}}$	−16	$\overline{\text{H}}$igh $\overline{\text{B}}$yte $\overline{\text{EN}}$able. Activates POL, OR, see $\overline{\text{LBEN}}$ (pin 22).
24	CLOCK3	−14 −12	RC oscillator pin. Can be used as clock output.

PIN	SYMBOL	DESCRIPTION
25	CLOCK1	Clock input. External clock or oscillator.
26	CLOCK2	Clock output. Crystal or RC oscillator.
27	MODE	Input LO;Direct output mode where $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ act as inputs directly controlling byte outputs. If pulsed HI causes immediate entry into handshake mode (see Figure 9). If HI, enables $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ as outputs. Handshake mode will be entered and data output as in Figures 7 & 8 at conversion completion.
28	R/$\overline{\text{H}}$	Run/$\overline{\text{Hold}}$; Input HI-conversions continuously performed every 2^{17} (−16) 2^{15} (−14) or 2^{13} (−12) clock pulses. Input LO-conversion in progress completed, converter will stop in Auto-Zero 7 counts before input integrate.
29	SEN	Send-ENable: Input controls timing of byte transmission in handshake mode. HI indicates 'send'.
30	$\overline{\text{CE}}/\overline{\text{LD}}$	$\overline{\text{C}}$hip-$\overline{\text{E}}$nable/$\overline{\text{L}}$oa$\overline{\text{D}}$. With MODE (pin 27) LO, $\overline{\text{CE}}/\overline{\text{LD}}$ serves as a master output enable; when HI, the bit outputs and POL, OR are disabled. With MODE HI, pin serves as a $\overline{\text{L}}$oa$\overline{\text{D}}$ strobe (-ve going) used in handshake mode. See Figures 7 & 8.
31	V(+)	Positive Logic Supply Voltage. Nominally +5V.
32	AN.IN	ANalog INput. High side.
33	BUF IN	BUFfer INput to analog chip (ICL8052 or ICL8068)
34	REFCAP2	REFerence CAPacitor (negative side)
35	AN.GND.	ANalog GrouND. Input low side and reference low side.
36	A-Z	Auto-Zero node.
37	VREF	Voltage REFerence input (positive side)
38	REFCAP1	REFerence CAPacitor (positive side)
39	COMP-IN	COMParator INput from 8052/8068
40	V(−)	Negative Supply Voltage. Nominally −15V.

<table>
<tr><td></td><td colspan="18">$\overline{\text{CE}}/\overline{\text{LD}}$</td></tr>
<tr><td></td><td colspan="2">$\overline{\text{HBEN}}$</td><td colspan="8">$\overline{\text{MBEN}}$</td><td colspan="8">$\overline{\text{LBEN}}$</td></tr>
<tr><td>7104-16</td><td>POL</td><td>O/R</td><td>B16</td><td>B15</td><td>B14</td><td>B13</td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td></tr>
<tr><td></td><td></td><td></td><td colspan="8">$\overline{\text{HBEN}}$</td><td colspan="8">$\overline{\text{LBEN}}$</td></tr>
<tr><td>7104-14</td><td></td><td></td><td>POL</td><td>O/R</td><td>B14</td><td>B13</td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td></tr>
<tr><td>7104-12</td><td></td><td></td><td>POL</td><td>O/R</td><td></td><td></td><td>B12</td><td>B11</td><td>B10</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td></tr>
</table>

TABLE 4: Three-State Byte Formats and $\overline{\text{EN}}$able Pins.

Fig. 1 shows the functional block diagram of the operating system. For a detailed explanation, refer to fig. 2 below.

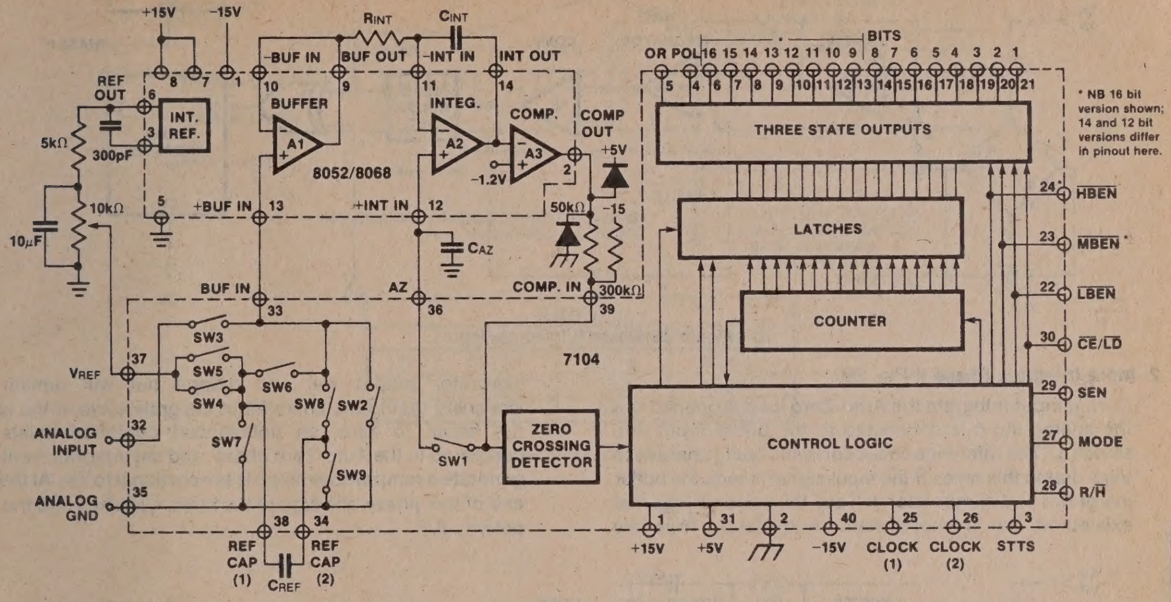

+15V
−15V
RINT
CINT
REF OUT
INT. REF.
5kΩ
300pF
10kΩ
10µF
−BUF IN
BUF OUT
−INT IN
INT OUT
BUFFER
A1
INTEG.
A2
COMP.
A3
COMP OUT
+5V
−1.2V
8052/8068
+BUF IN
+INT IN
CAZ
50kΩ
−15
300kΩ
BUF IN
AZ
COMP. IN
7104
VREF
SW3
SW5
SW4
SW6
SW8
SW2
SW7
SW9
SW1
ANALOG INPUT
ANALOG GND
REF CAP (1)
REF CAP (2)
CREF
ZERO CROSSING DETECTOR
OR POL
BITS
16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
THREE STATE OUTPUTS
LATCHES
COUNTER
CONTROL LOGIC
* NB 16 bit version shown; 14 and 12 bit versions differ in pinout here.
HBEN
MBEN *
LBEN
CE/LD
SEN
MODE
R/H
+15V
+5V
−15V
CLOCK (1)
CLOCK (2)
STTS

Figure 1: 8052A (8068A)/7104 16/14/12 Bit A/D Converter Functional Block Diagram

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DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent Circuit of the Analog Section of both the ICL7104/8052 and the ICL7104/8068 in the 3 different phases of operation. If the Run/Hold pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 131,072 for −16; 32,368 for −14; and 8092 for −12 clock periods per cycle (see Figure conversion timing).

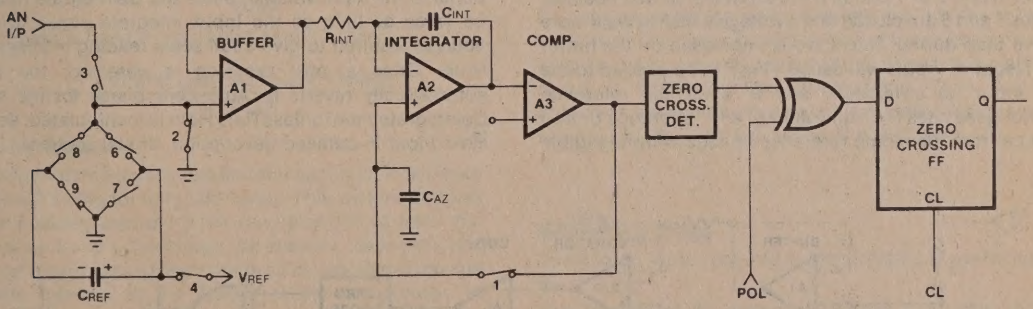

AN I/P
3
2
8
6
9
7
4
CREF
VREF
BUFFER
A1
RINT
CINT
INTEGRATOR
A2
CAZ
1
COMP.
A3
ZERO CROSS. DET.
POL
D
Q
ZERO CROSSING FF
CL
CL

Figure 2A: Phase I Auto-Zero

1. **Auto-Zero Phase I** Fig. 2A

   During Auto-Zero, the input of the buffer is shorted to analog ground thru switch 2, and switch 1 closes a loop around the integrator and comparator. The purpose of the loop is to charge the Auto-Zero capacitor until the integrator output no longer changes with time. Also, switches 4 and 9 recharge the reference capacitor to VREF.

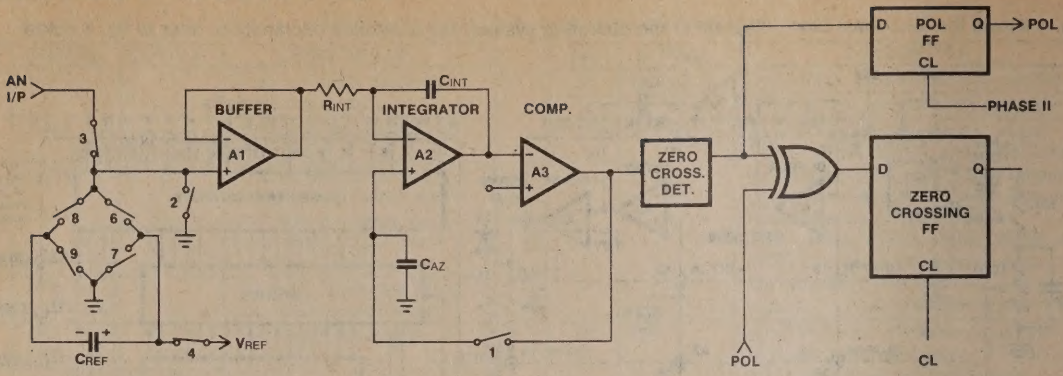

AN I/P
3
2
8
6
9
7
CREF
4
VREF
BUFFER
A1
RINT
CINT
INTEGRATOR
A2
CAZ
1
COMP.
A3
ZERO CROSS. DET.
D
POL FF
Q
POL
CL
PHASE II
ZERO CROSSING FF
POL
CL

Figure 2B: Phase II Integrate Input

2. Input Integrate Phase II Fig. 2B

During input integrate the Auto-Zero loop is opened and the analog input is connected to the buffer input thru switch 3. (The reference capacitor is still being charged to V_{REF} during this time.) If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

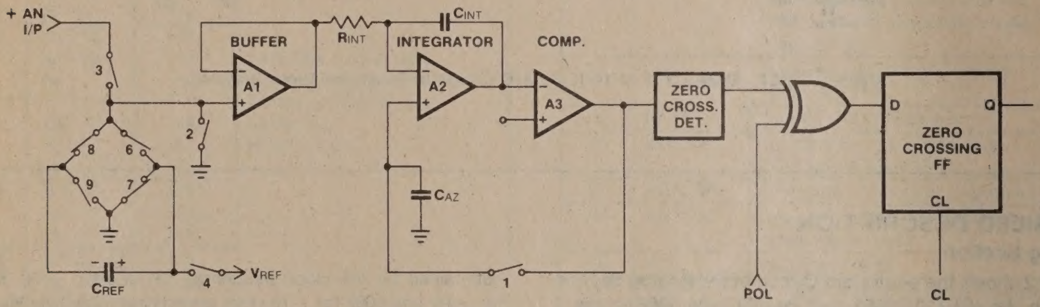

+ AN I/P
3
2
8
6
9
7
CREF
4
VREF
BUFFER
A1
RINT
CINT
INTEGRATOR
A2
CAZ
1
COMP.
A3
ZERO CROSS. DET.
D
Q
ZERO CROSSING FF
CL
POL
CL

Figure 2C: Phase III + Deintegrate

Deintegrate Phase III Fig. 2C & D

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switches 6 and 9 or 7 and 8. If the input signal was positive, switches 7 and 8 are closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the buffer input. Negative inputs will cause $+V_{REF}$ to be applied to the buffer input via switches 6 and 9. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input integrate phase, the input voltage required to give a full scale reading = $2V_{REF}$.

Note: Once a zero crossing is detected, the system automatically reverts to Auto-Zero phase for the leftover Deintegrate time (unless Run/$\overline{\text{H}}$old is manipulated, see Run/$\overline{\text{H}}$old Input in detailed description, digital section).

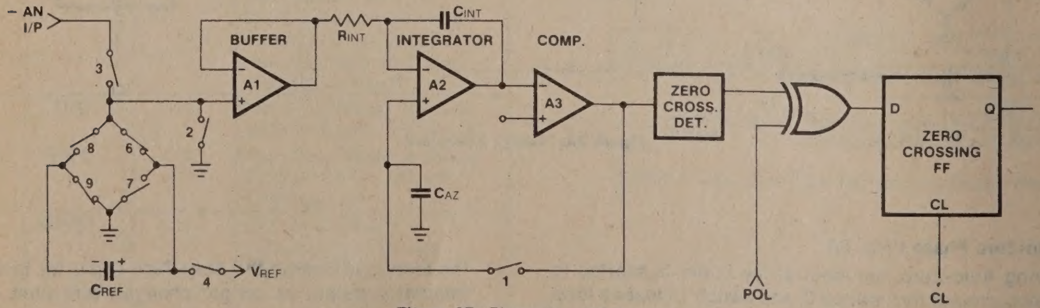
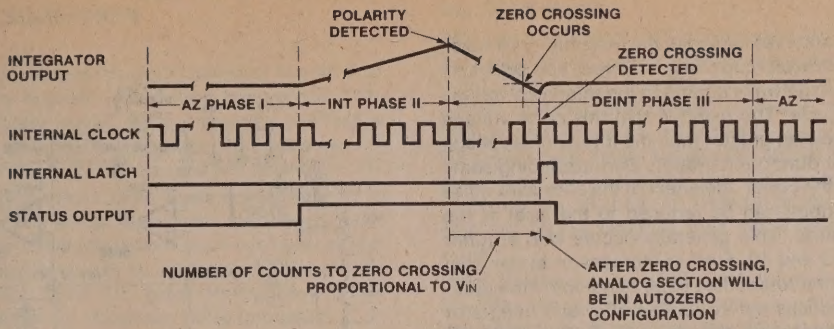

− AN I/P
3
2
8
6
9
7
CREF
4
VREF
BUFFER
A1
RINT
CINT
INTEGRATOR
A2
CAZ
1
COMP.
A3
ZERO CROSS. DET.
D
Q
ZERO CROSSING FF
CL
POL
CL

Figure 2D: Phase III - Deintegrate



COUNTS			
	Phase I	Phase II	Phase III
-16	32768	32768	65536
-14	8192	8192	16384
-12	2048	2048	4096

Figure 3: Conversion Timing

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40 μA give good results with a nominal of 20 μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}^*}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then -

$$R_{INT} = \frac{\text{(Buffer gain) (full scale voltage)}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is give by

$$C_{INT} = \frac{\left[\begin{array}{l}(32768 \text{ for } -16\\ (8192 \text{ for } -14 \text{ X clock period})\\ (2048 \text{ for } -12\end{array}\right] \text{X } (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it have low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half scale (100 . . . 000) and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7104 at 16 bits is one part in 65536, or 15.26ppm. Thus, if the reference has a temperature coefficient of 50ppm/°C (on board reference) a temperature change of 1/3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 4. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1-2μV, allowing full 16-bit use with full scale inputs of as low as 150mV. Note that at this level, thermoelectric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome. For further discussion, see App. Note A030.

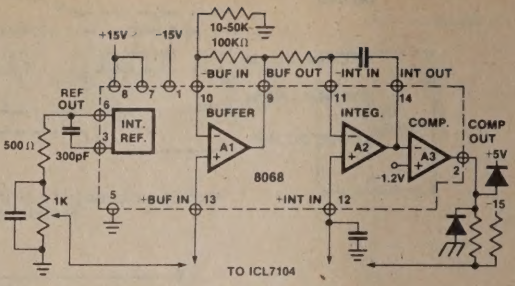


Figure 4: Adding Buffer Gain to ICL8068

Table 5: Typical Component Values

V++ = +15V, V+ = 5V, V- = -15V, Clock Freq = 200 kHz

ICL8052/8068 with	ICL7104-16			ICL7104-14		ICL7104-12		UNITS
Full scale V_{IN}	200	800	4000	100	4000	50	4000	mV
Buffer Gain	10	1	1	10	1	10	1	
R_{INT}	100	43	200	47	180	27	200	kΩ
C_{INT}	.33	.33	.33	0.1	0.1	.022	.022	μF
C_{AZ}	1.0	1.0	1.0	1.0	1.0	.47	.47	μF
C_{ref}	10	1.0	1.0	10	1.0	4.7	4.7	μF
V_{REF}	100	400	2000	50	2000	25	200	mV
Resolution	3.1	12	61	6.1	244	12	980	μV

ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and for systems where system noise is a limiting factor, particularly in low signal level conditions, will give better performance.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator circuit, a 16, 14 or 12 bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic and UART handshake logic, as shown in the Block Diagram Figure 5 (16 bit version shown).

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined under "ICL7104 Electrical Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in three bytes for the 7104-16 or two bytes for the 7104-14 and 7104-12, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STaTuS Output

During a conversion cycle, the STaTuS output goes high at the beginning of Input Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STaTuS is low) to drive interrupts, or for monitoring the status of the converter.

Run/$\overline{\text{H}}$old Input

When the Run/$\overline{\text{H}}$old input is connected to V+ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 3). (See under "Handshake Mode" for exception.) In this mode of operation, the conversion cycle will be performed in 131,072 for 7104-16, 32768 for 7104-14 and 8192 for 7104-2 clock periods, regardless of the resulting value.

If Run/$\overline{\text{H}}$old goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If Run/$\overline{\text{H}}$old stays or goes low, the converter will ensure a minimum Auto-Zero time, and then wait in Auto-Zero until the Run/$\overline{\text{H}}$old input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at Run/$\overline{\text{H}}$old. See Figure 6 for details.

Using the Run/$\overline{\text{H}}$old input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in Auto-Zero with Run/$\overline{\text{H}}$old low. When Run/$\overline{\text{H}}$old goes high the conversion is started, and when the STaTuS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). Run/$\overline{\text{H}}$old may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion. Alternately, Run/$\overline{\text{H}}$old can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the Run/$\overline{\text{H}}$old input can be provided by connecting it to the CLOCK3 (-12, -14), CLOCK2 (-16) Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

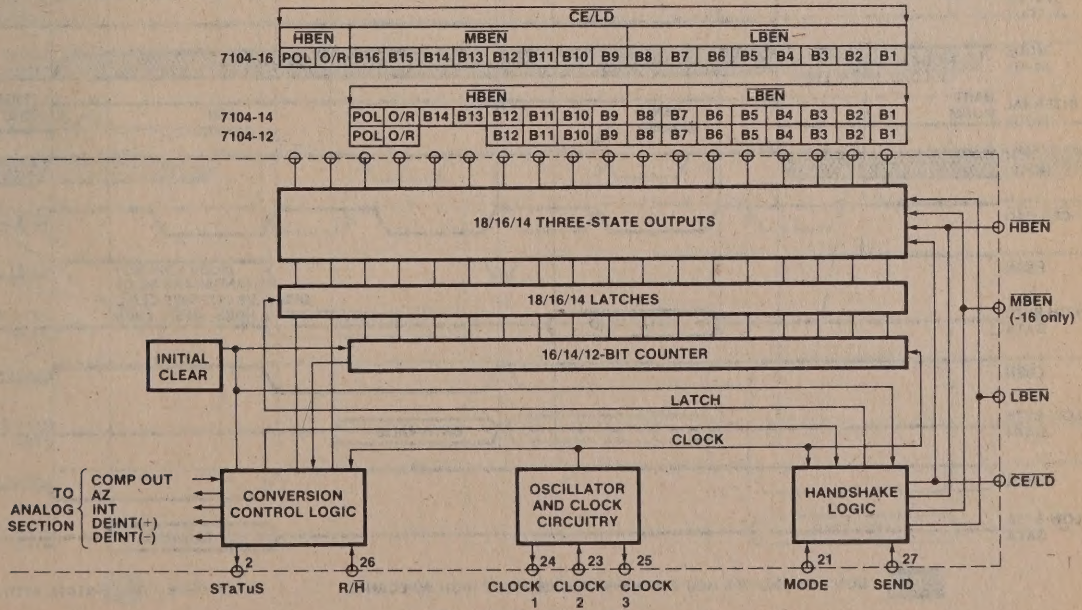

CE/LD
HBEN
MBEN
LBEN
7104-16
POL O/R B16 B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1
HBEN
LBEN
7104-14
POL O/R B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1
7104-12
POL O/R B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1
18/16/14 THREE-STATE OUTPUTS
HBEN
18/16/14 LATCHES
MBEN (-16 only)
INITIAL CLEAR
16/14/12-BIT COUNTER
LATCH
LBEN
CLOCK
CE/LD
TO ANALOG SECTION
COMP OUT
AZ
INT
DEINT(+)
DEINT(-)
CONVERSION CONTROL LOGIC
OSCILLATOR AND CLOCK CIRCUITRY
HANDSHAKE LOGIC
2
STaTuS
26
R/H
24
CLOCK 1
23
CLOCK 2
25
CLOCK 3
21
MODE
27
SEND

Figure 5: Digital Section

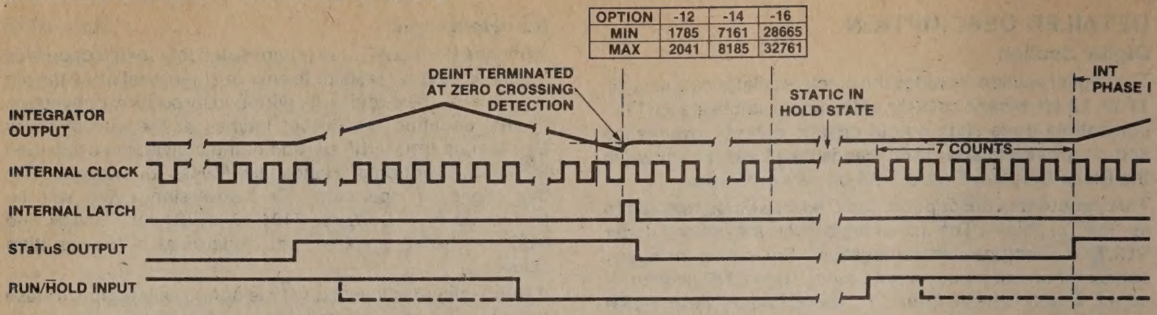

OPTION | -12 | -14 | -16
MIN | 1785 | 7161 | 28665
MAX | 2041 | 8185 | 32761
DEINT TERMINATED AT ZERO CROSSING DETECTION
STATIC IN HOLD STATE
INT PHASE I
7 COUNTS
INTEGRATOR OUTPUT
INTERNAL CLOCK
INTERNAL LATCH
STaTuS OUTPUT
RUN/HOLD INPUT

Figure 6: Run/Hold Operation

If the Run/$\overline{\text{H}}$old input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for Run/$\overline{\text{H}}$old to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs[bits 1 through 8 low order byte, see Table 4 for format of middle (-16) and high order bytes]are accessible under control of the byte and chip $\overline{\text{EN}}$able terminals as inputs. These $\overline{\text{EN}}$able inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip $\overline{\text{EN}}$able input is low, taking a byte $\overline{\text{EN}}$able input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used. The timing requirements for these outputs are shown under AC Characteristics and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STaTuS output will prevent this. Data is never updated while STaTuS is low. Also note the potential bus conflict described under "Initial Clear Circuitry".

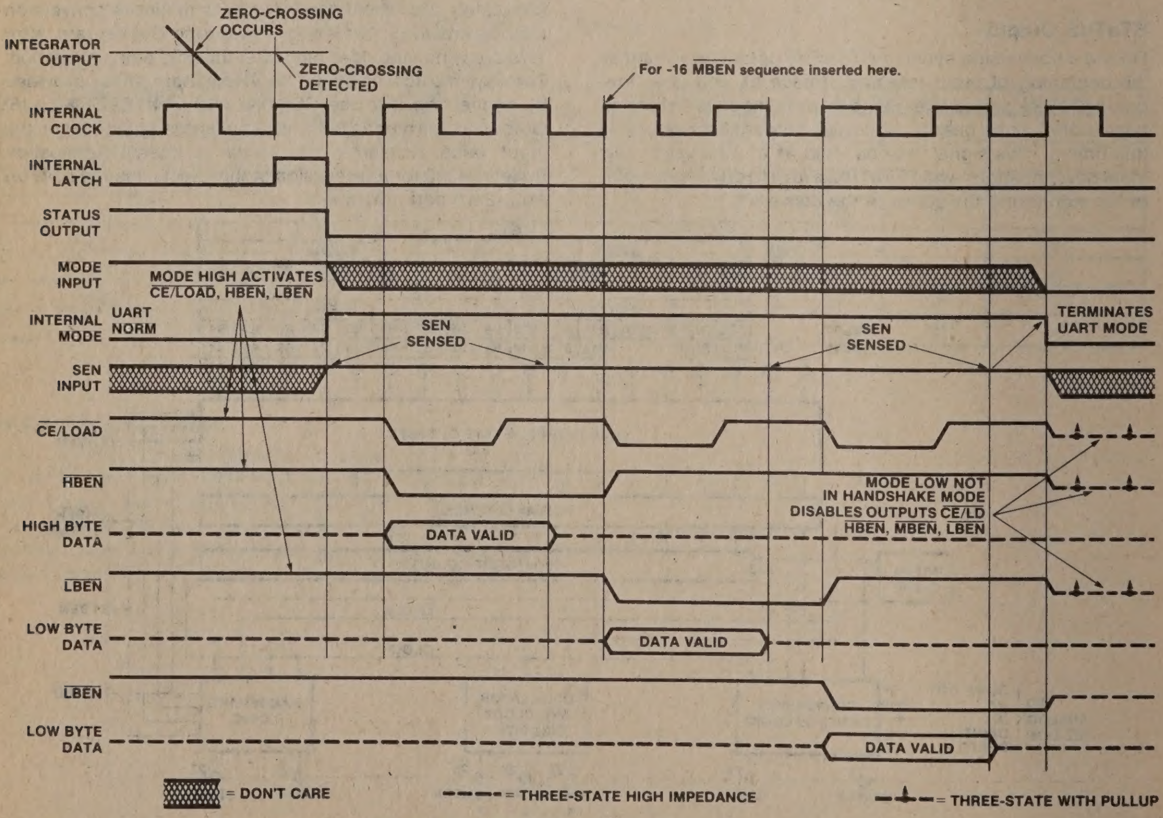

ZERO-CROSSING OCCURS
ZERO-CROSSING DETECTED
For -16 MBEN sequence inserted here.
INTEGRATOR OUTPUT
INTERNAL CLOCK
INTERNAL LATCH
STATUS OUTPUT
MODE INPUT
MODE HIGH ACTIVATES CE/LOAD, HBEN, LBEN
INTERNAL MODE
UART NORM
SEN SENSED
SEN SENSED
TERMINATES UART MODE
SEN INPUT
CE/LOAD
HBEN
MODE LOW NOT IN HANDSHAKE MODE DISABLES OUTPUTS CE/LD HBEN, MBEN, LBEN
HIGH BYTE DATA
DATA VALID
LBEN
LOW BYTE DATA
DATA VALID
LBEN
LOW BYTE DATA
DATA VALID
= DON'T CARE
= THREE-STATE HIGH IMPEDANCE
= THREE-STATE WITH PULLUP

Figure 7: Handshake With SEN Held Positive

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7104 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte ENable inputs. This mode is specifically designed to allow a direct interface between the ICL7104 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7104 provides all the control and flag signals necessary to sequence the three (ICL7106-16) or two (ICL7104-14, -12) bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (pin 27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte ENable terminals become TTL-compatible outputs which provide the control signals for the output cycle. The Send ENable pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CLOCK 1 (pin 25) clock edge, the corresponding byte ENable line goes low, and the Chip ENable/LoaD line (pin 30) (CE/LD) goes low for one full clock pulse only, returning high.

On the next falling CLOCK 1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte ENable pin will be cleared high, and (unless finished) the CE/LD and the next byte ENable pin will go low. This will continue until all three (2 in the case of 12 and 14 bit devices) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte ENable pin is (active) low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip ENable will be three-stated off, if MODE is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 7, 8, and 9, and Table 2.

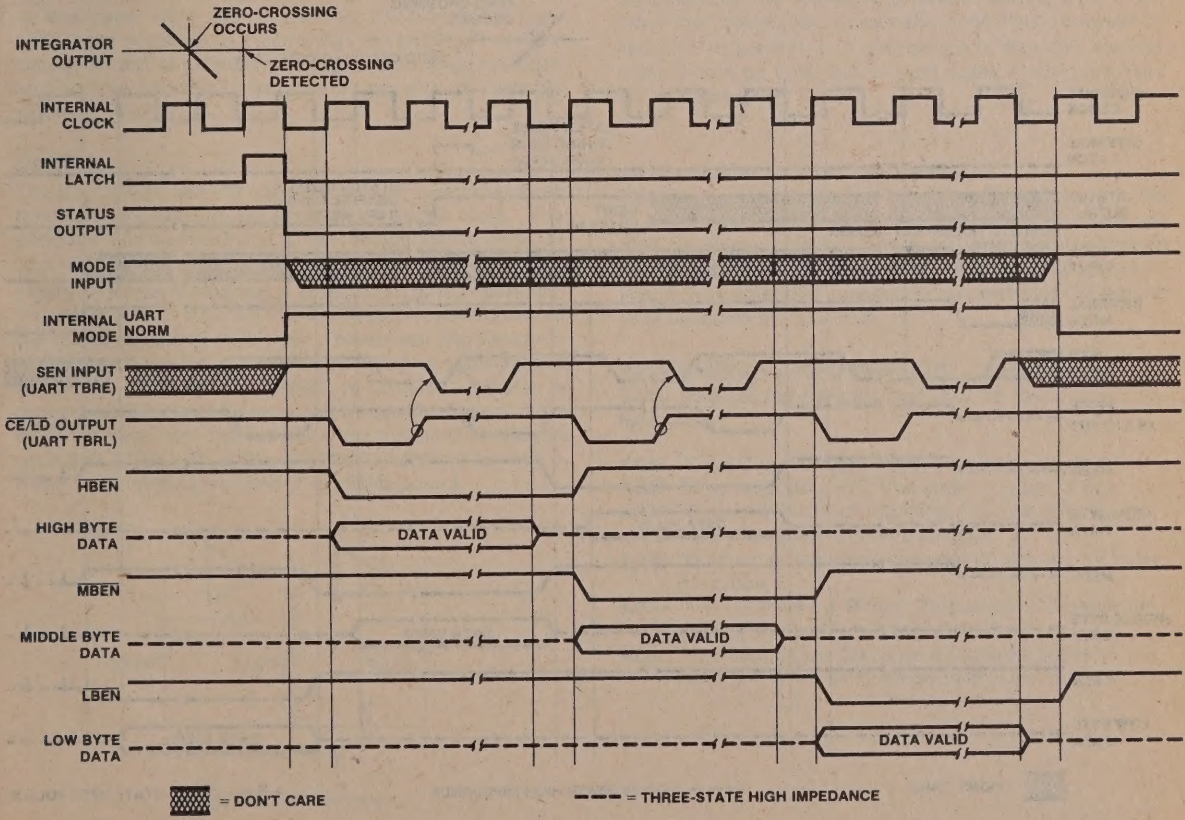


Figure 8: Handshake - Typical UART Interface Timing

Figure 7 shows the sequence of the output cycle with SEN held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{LBEN}}$, $\overline{\text{MBEN}}$ and $\overline{\text{HBEN}}$ terminals are active as outputs). The high level at the SEN input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the $\overline{\text{CE}}/\overline{\text{LD}}$ and the $\overline{\text{HBEN}}$ outputs assume a low level and the high-order byte (POL and OR, and except for -16, Bis 9-14) outputs are enabled. The $\overline{\text{CE}}/\overline{\text{LD}}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte $\overline{\text{EN}}$able remains low for two clock periods. Thus the $\overline{\text{CE}}/\overline{\text{LD}}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte $\overline{\text{EN}}$able as an output may be used as a byte identification flag. With SEN remaining high the converter completes the output cycle using $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{MBEN}}$ and $\overline{\text{LBEN}}$ while the remaining byte outputs (see Table 4) are activated. The handshake mode is terminated when all bytes are sent (3 for -16, 2 for -14, -12).

Figure 8 shows an output sequence where the SENinput is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEN input to the ICL7104 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{\text{CE}}/\overline{\text{LD}}$ terminal of the ICL7104 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEN input will be high when the handshake mode is entered after new data is stored. The $\overline{\text{CE}}/\overline{\text{LD}}$ and $\overline{\text{HBEN}}$ terminals will go low after SEN is sensed, and the high order byte outputs become active. When $\overline{\text{CE}}/\overline{\text{LD}}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{\text{HBEN}}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7104 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{\text{HBEN}}$ output returns high. At the same time, the $\overline{\text{CE}}/\overline{\text{LD}}$ and $\overline{\text{MBEN}}$ (-16) or $\overline{\text{LBEN}}$ outputs go low, and the corresponding byte outputs become active. Similarly, when the $\overline{\text{CE}}/\overline{\text{LD}}$ returns high at the end of one clock period, the enabled data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7104 internal clock high to low edge, disabling the data outputs. For the 16 bit device, the sequence is repeated for $\overline{\text{LBEN}}$. One-half internal clock later, the handshake mode will be cleared, and the chip and byte $\overline{\text{EN}}$able terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion

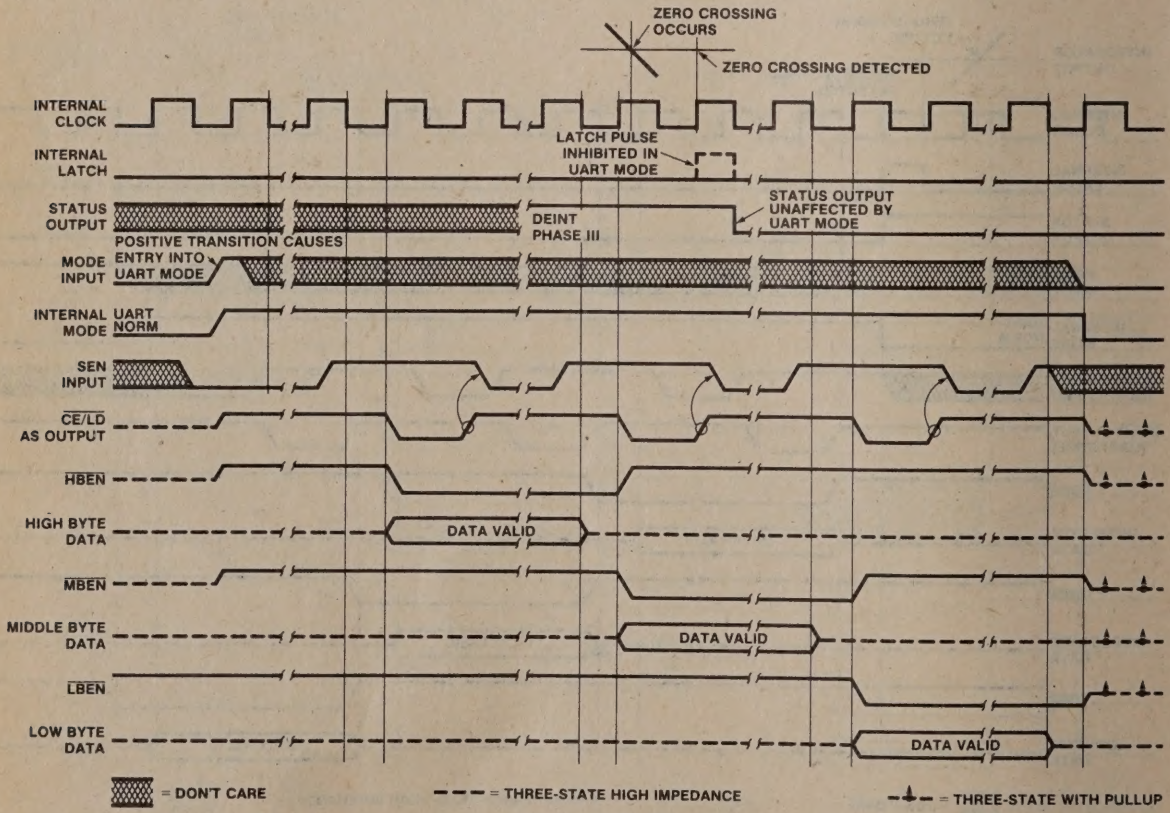

ZERO CROSSING OCCURS
ZERO CROSSING DETECTED
INTERNAL CLOCK
INTERNAL LATCH
LATCH PULSE INHIBITED IN UART MODE
STATUS OUTPUT
DEINT PHASE III
STATUS OUTPUT UNAFFECTED BY UART MODE
POSITIVE TRANSITION CAUSES ENTRY INTO UART MODE
MODE INPUT
INTERNAL MODE
UART
NORM
SEN INPUT
$\overline{\text{CE}}/\overline{\text{LD}}$ AS OUTPUT
$\overline{\text{HBEN}}$
HIGH BYTE DATA
DATA VALID
$\overline{\text{MBEN}}$
MIDDLE BYTE DATA
DATA VALID
$\overline{\text{LBEN}}$
LOW BYTE DATA
DATA VALID
= DON'T CARE
= THREE-STATE HIGH IMPEDANCE
= THREE-STATE WITH PULLUP

Figure 9: Handshake Triggered By Mode

except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 11 shows a handshake output sequence triggered by such an edge. In addition, the SEN input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEN input, and the sequence for the first (high order) byte is similar to the sequence for the other bytes. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STaTuS output and Run/$\overline{\text{Hold}}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

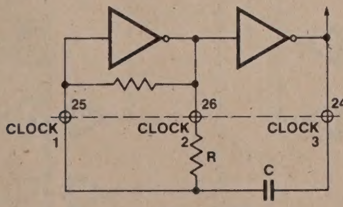
Initial Clear Circuitry

The internal logic of the 7104 is supplied by an internal regulator between V++ and Digital Ground. The regulator includes a low-voltage detector that will clear various registers. This is intended to ensure that on initial power-up, the control logic comes up in Auto-Zero, with the 2nd, 3rd, and 4th MSB bits cleared, and the "mode" FF cleared (i.e. in "direct" mode). This, however, will also clear these registers if the supply voltage "glitches" to a low enough value. Additionally, if the supply voltage comes up too fast, this clear pulse may be too narrow for reliable clearing. In general, this is not a problem, but if the UART internal "MODE" FF should come up set, the byte and chip ENable lines will become active outputs. In many systems this could lead to buss conflicts, especially in non-handshake systems. In any case, SEN should be high (held high for non-handshake systems) to ensure that the MODE FF will be cleared as fast as possible (see Fig. 7 for timing). For these and other reasons, adequate supply bypass is recommended.

Oscillator

The ICL7104-14 and -12 are provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator.

Figure 10 shows the oscillator configured for RC operation. The internal clock will be of the same frequency and phase as the voltage on the CLOCK 3 pin. The resistor and capacitor should be connected as shown. The circuit will oscillate at a frequency given by $f = .45/RC$. A 50-100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 32768 (-16), 8192 (-14), 2048 (-12) clock periods is close to an integral multiple of the 60Hz period.



$f_{osc} = .45/RC$

Figure 10: RC Oscillator

Note that CLOCK 3 has the same output drive as the bit outputs.

As a result of pin count limitations, the ICL7104-16 has only CLOCK 1 and CLOCK 2 available, and cannot be used as an RC oscillator. The internal clock will correspond to the inverse of the signal on CLOCK 2. Figure 11 shows a crystal oscillator circuit, which can be used with all 7104 versions. If an external clock is to be used, it should be applied to CLOCK 1. The internal clock will correspond to the signal applied to this pin.

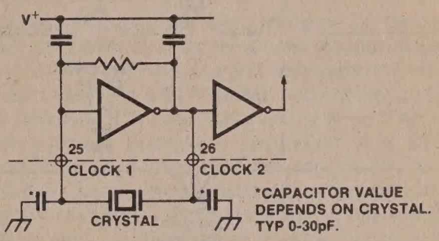


Figure 11: Crystal Oscillator

POWER SUPPLY SEQUENCING

Because of the nature of the CMOS process used to fabricate the ICL7104, and the multiple power supplies used, there are certain conditions of these supplies under which a disabling and potentially damaging SCR action can occur. All of these conditions involve the V+ supply (nom. +5V) being more positive than the V++ supply. If there is any possibility of this occuring during start-up, shut down, under transient conditions during operation, or when inserting a PC board into a "hot" socket, etc., a diode should be placed between V$^+$ and V++ to prevent it. A germanium or Schottky rectifier diode would be best, but in most cases a silicon rectifier diode is adequate.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of 8068 or 8052/7104 circuits, especially in 16-bit and high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. A recommended connection sequence for the ground lines is shown in Figure 12.

APPLICATIONS INFORMATION

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters", by Dave Fullagar
A017 "The Integrating A/D Converter", by Lee Evans
A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood
A025 "Building a Remote Data Logging Station", by Peter Bradshaw
A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

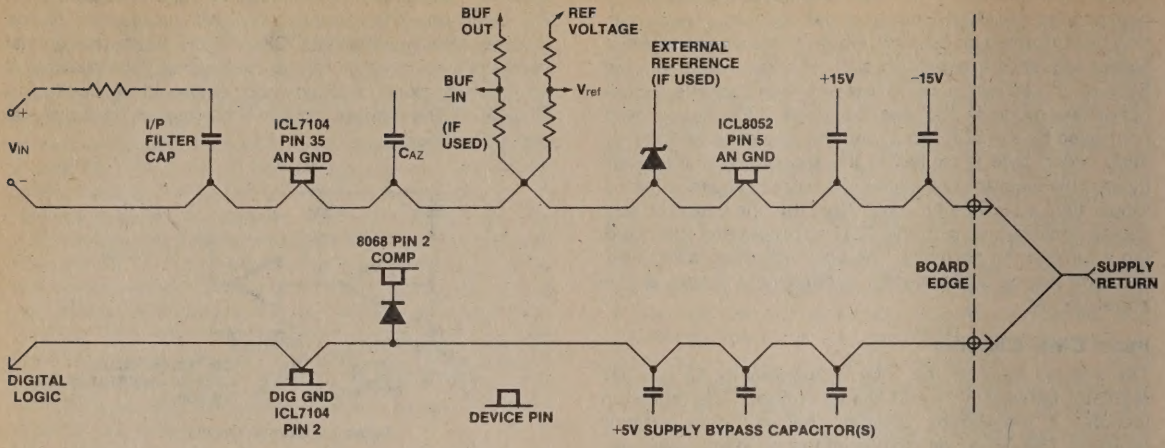

BUF OUT
REF VOLTAGE
EXTERNAL REFERENCE (IF USED)
+15V
−15V
BUF −IN
(IF USED)
V_{ref}
V_{IN}
I/P FILTER CAP
ICL7104 PIN 35 AN GND
C_{AZ}
ICL8052 PIN 5 AN GND
8068 PIN 2 COMP
BOARD EDGE
SUPPLY RETURN
DIGITAL LOGIC
DIG GND ICL7104 PIN 2
DEVICE PIN
+5V SUPPLY BYPASS CAPACITOR(S)

Figure 12: Grounding Sequence

INTERSIL

ICL8052/8053 (3½ Digit) ICL8052A/8053A (4½ Digit)

Precision Chip Pairs for A/D Conversion

FEATURES

- **Accuracy high enough for ±40,000 count instruments**
- **Priced low enough to compete with 3-1/2 digit DPM/DVM pairs**
- **One basic circuit for an entire family of DVMs**
- **Auto-Zero; Auto-Polarity**
- **5pA typical input current**
- **Single reference voltage**
- **True ratiometric (scale factor of 1)**

ORDERING INFORMATION

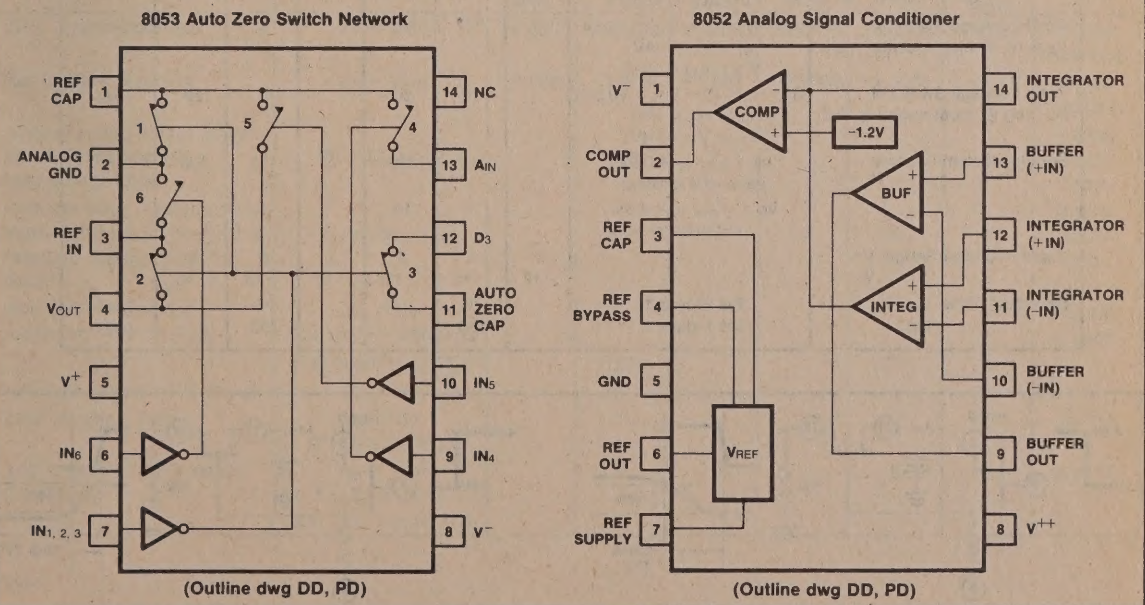
Part	Temp. Range	Package	Order Number
8052	0°C to +70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to +70°C	14 pin ceramic DIP	ICL8052CDD
8052A	0°C to +70°C	14 pin plastic DIP	ICL8052ACPD
8052A	0°C to +70°C	14 pin ceramic DIP	ICL8052ACDD
8053	0°C to +70°C	14 pin plastic DIP	ICL8053CPD
8053	0°C to +70°C	14 pin ceramic DIP	ICL8053CDD
8053A	0°C to +70°C	14 pin plastic DIP	ICL8053ACPD
8053A	0°C to +70°C	14 pin ceramic DIP	ICL8053ACDD

GENERAL DESCRIPTION

The ICL8052/8053 pair has been designed to "lock-in" the accuracy of a DVM and at the same time give the designer the freedom of using any output format his system requires. With reasonable care, the 0.001% linearity capability of the pair can be maintained in production instruments. The system uses time-proven dual-slope integration with all of its advantages: i.e., non-critical components, high rejection of noise and a-c signals, non-critical clock frequency and true ratiometric readings. At the same time it has reduced or eliminated many of the sources of error that have limited dual-slope accuracy. With the ICL8052/8053 pairs, critical board layout is no longer required to give low charge injection by the switches, and elaborate ground planes are not necessary to keep clock pulse transients out of the comparator circuitry. A further feature of these devices is that the DVM/DPM manufacturer can generate an entire family of instruments using only one basic p-c board with 2 or 3 jumper points. The family could include:

±200.0 mV Full Scale
±2.000 Volts
±400.0 mV
±4.000 Volts
±800.0 mV
±2.0000 Volts
±4.0000 Volts
±3.2768 Volts (16 bits in 0.1 mV increments)

CONNECTION DIAGRAM



8053 Auto Zero Switch Network
REF CAP 1
ANALOG GND 2
REF IN 3
VOUT 4
V+ 5
IN6 6
IN1, 2, 3 7
14 NC
13 AIN
12 D3
11 AUTO ZERO CAP
10 IN5
9 IN4
8 V−
1
2
3
4
5
6
(Outline dwg DD, PD)
8052 Analog Signal Conditioner
V− 1
COMP OUT 2
REF CAP 3
REF BYPASS 4
GND 5
REF OUT 6
REF SUPPLY 7
14 INTEGRATOR OUT
13 BUFFER (+IN)
12 INTEGRATOR (+IN)
11 INTEGRATOR (−IN)
10 BUFFER (−IN)
9 BUFFER OUT
8 V++
COMP
BUF
INTEG
−1.2V
VREF
(Outline dwg DD, PD)

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) .... 500 mW
Storage Temperature .... −65°C to +150°C
Operating Temperature .... 0°C to +70°C
Lead Temperature (Soldering, 60 sec.) .... 300°C

ICL8052 ONLY

Supply Voltage .... ±18V
Differential Input Voltage .... ±30V
Input Voltage (Note 2) .... ±15V
Output Short Circuit Duration,
All Outputs (Note 3) .... Indefinite

ICL8053 ONLY

Source Current (I_S) .... 100 mA
Drain Current (I_D) .... 100 mA
Digital Inputs .... 5 mA
V^+ to V^- 25V
Digital Input .... V^- to V^+

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL8053 ELECTRICAL CHARACTERISTICS ($V^+ = +5V$, $V^- = -15V$ unless otherwise specified)

CHARACTERISTICS	CONDITIONS	ICL8053			ICL8053A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
R_{on} Switch 1, 3 (each Switch)	$V_7 = +4.5V$ $V_6 = V_9 = V_{10} = +0.5V$		1000	2500		1000	2500	Ω
R_{on} Switch 2	Same as Switch 1, 2		2000	5000		2000	5000	Ω
R_{on} Switch 4	$V_9 = +4.5V$ $V_6 = V_7 = V_{10} = +0.5V$		1000	2500		1000	2500	Ω
R_{on} Switch 5	$V_{10} = +4.5V$ $V_6 = V_7 = V_9 = +0.5V$		1000	2500		1000	2500	Ω
R_{on} Switch 6	$V_6 = +4.5V$ $V_7 = V_9 = V_{10} = +0.5V$		1000	2500		1000	2500	Ω
Total Leakage Sw 1, 2, 5 & 6 $I_1 + I_3$ @ most positive Voltage	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_4 = -4V$, $V_2 = 0V$ $V_1 = V_3 = +4V$		10	50		5	20	pA
Total Leakage Sw 1, 2, 5 & 6 $I_1 + I_3$ @ most negative Voltage	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_4 = +4V$, $V_2 = 0V$ $V_1 = V_3 = -4V$		10	50		5	20	pA
Total Leakage Sw 3 & 4 $I_{12} + I_{13}$ @ most positive Volt.	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_1 = V_{11} = -4V$ $V_{12} = V_{13} = +4V$		10	50		5	20	pA
Total Leakage Sw 3 & 4 $I_{12} + I_{13}$ @ most negative Volt.	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_1 = V_{11} = +4V$ $V_{12} = V_{13} = -4V$		10	50		5	20	pA
Supply Current (V^+ or V^-)	$V_{6,\ 7,\ 9 \text{ or } 10} = 0.5V$ (each of 4 drivers)		150	300		150	300	μA
	$V_{6,\ 7,\ 9 \text{ and } 10} = 4.5V$ (all drivers)		1	10		1	10	μA
Supply Voltage Range V^+		4	5	8	4	5	8	V
V^-		−12	−15	−16	−12	−15	−16	V
Switching Time t_{on}	See Figure 1		75			75		nsec
t_{off}	See Figure 1		150			150		nsec

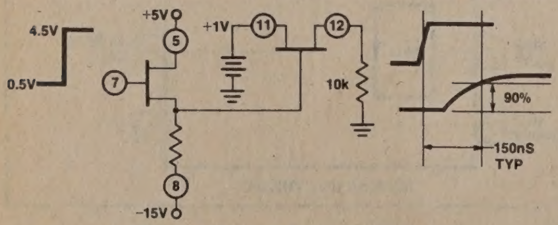
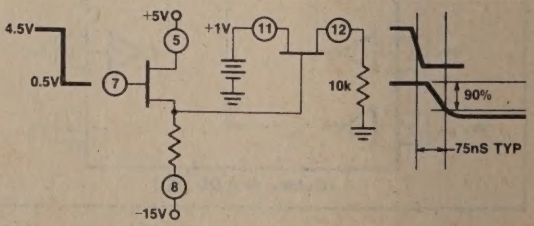


Figure 1: Turn-on Switching Time



Turn-off Switching Time

8052 ELECTRICAL CHARACTERISTICS (V_{SUPP} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTICS	CONDITIONS	8052 MIN	8052 TYP	8052 MAX	8052A MIN	8052A TYP	8052A MAX	UNITS
	EACH OPERATIONAL AMPLIFIER								
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	50		20	50	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		5	50		2	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
A_V	Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			1			1		MHz
I_{SC}	Output Short-Circuit Current			20	100		20	100	mA
	COMPARATOR AMPLIFIER								
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
	VOLTAGE REFERENCE								
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		ohms
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPP}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPP}	Supply Current Total			6	12		6	12	mA

Note 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA\,Pd$ where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 2: This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS (V^{++} = +15V, V^+ +5V, V^- = −15V; Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	ICL8052/8053(3) MIN	ICL8052/8053(3) TYP	ICL8052/8053(3) MAX	ICL8052A/8053A(4) MIN	ICL8052A/8053A(4) TYP	ICL8052A/8053A(4) MAX	UNITS
Zero Input Reading	V_{in} = 0.0V	−0.000	±0.000	+0.000	−0.0000	±0.0000	+0.0000	Digital Reading
Ratiometric Reading	$V_{in} = V_{Ref.}$	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-2V \le V_{in} \le +2V$		0.2	1		0.5	1	Digital Count Error
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 2V$		0.2	1		0.5	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV		0.2					Digital Count
	Full scale = 2.000V		0.05			0.3		
Leakage Current into Input	V_{in} = 0V		5	30		3	10	pA
Zero Reading Drift	V_{in} = 0V $0° \le T_A \le 70°C$		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +2V $0 \le T_A \le 70°C$ (ext. ref. 0 ppm/°C)		3	15		2	5	ppm/°C

Notes:

(3) Tested in 3-1/2 digit (2,000 count) circuit shown in Fig. 5 clock frequency 12 kHz.

(4) Tested in 4-1/2 digit (20,000 count) circuit shown in Fig. 5 clock frequency 120 kHz.

THEORY OF OPERATION

Figure 4 shows a function diagram for an A-D converter using the ICL8052/8053 pair. In this circuit, each measurement cycle is divided into four equal parts by the state F/F. The first part, state 00, is the auto-zero cycle. The switch driver decoder recognizes this state and turns on hex switches number 1, 2, and 3. Switches 1 and 2 impress a voltage equal to V_{REF} across the reference capacitor. Switch 3 closes a loop around the integrator and comparator. The purpose of this loop is to charge up the auto-zero capacitor until the integrator output no longer changes with time. During the second state, 01, switches 1, 2 and 3 are opened and switch 4 is closed. If the input voltage is zero, the buffer, integrator and comparator will see the same voltages that existed in the previous state. Thus, the integrator output will not change but will remain stationary during the entire signal-integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the auto-zero cycle and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this cycle, the sign of the ramp is latched into the polarity F/F. The final cycle, reference integrate, includes states 10 and 11. The switch driver decoder uses the output of the polarity F/F in deciding whether to close switch 5 or 6. If the input signal was positive, switch 6 is closed and a voltage which is V_{REF} more negative than during auto-zero is impressed on the buffer input. If the input signal was negative switch 5 is closed and a voltage which is V_{REF} more positive than during auto-zero is impressed on the buffer input. Thus, the reference capacitor generates the equivalent of a (+) reference of a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to zero. The time, or number of counts, required to do this is proportional to the input voltage. Since the reference cycle can be twice as long as the signal integrate cycle, the input voltage required to give a full scale reading $\equiv 2 V_{REF}$. The circuit, as described to this point, is not new to this application. It has been used successfully for several years. However, this system makes three major contributions to the accuracy of this circuit. These are: (1) low charge injection, (2) junction FET op amp, and (3) zero-crossing flip-flop.

1. **Low Charge Injection.**

   During auto-zero, there is no problem in charging the capacitors to the correct voltage. The problem is getting the switches off without changing this voltage. As the gate is driven off, the gate-to-drain capacitance of the switch injects a charge on the reference or auto-zero capacitor, changing its voltage. The designer, using discrete components, is forced into critical board layouts where charges of opposite polarity are injected to compensate or neutralize the driver injection. This balance will be upset by any unit-to-unit variation of switch capacitance so at best the final design is a compromise. In the ICL8052/8053 the critical layout has been done on the semiconductor chip and need not concern the user. Also, since a silicon-gate process is used for the switches, the unit-to-unit variation is extremely low. The net result is to give an error due to charge injection that is so low it is difficult to measure; but certainly less than 5μV referred to the input.

2. **Junction FET Op Amps.**

   Both the buffer and integrator use junction FET inputs in a guarded circuit that reduces the voltage across the FET to 3 or 4 volts. At this voltage level, input leakage currents of 2 pA are typical. For typical component values 2 pA leakage contributes less than 2μV of error to the circuit. In theory, MOS FET's would contribute less leakage but their increased noise would swamp out any improvement by orders of magnitude.

3. **Zero-Crossing Flip Flop.**

   The problem that the zero-crossing flip-flop is designed to solve is shown in figure 2.

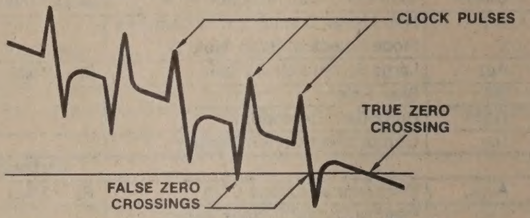


Figure 2: Integrator Output Near Zero-Crossing

The integrator output is approaching the zero-crossing point where the clock will be stopped and the reading displayed. The clock pulse feedthrough superimposed upon this ramp will cause a false reading by stopping the count prematurely. For a 40,000 count instrument, the ramp is changing approximately 0.25mV per clock pulse (10 volt max integrator output divided by 40,000 counts). The clock pulses have to be less than 100μV peak to avoid causing significant errors. The circuit layout to achieve this can be time consuming at best and impossible at worst. The suggested circuit gets around this problem by feeding the zero-crossing information into a J-K flip-flop instead of using it directly. The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. Any false zero-crossing caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance. If a correction was not made, the display would always be one count too high. The correction is to change the four states of the converter one count early. In other words, instead of changing states at the beginning of count 0000, the states are changed at the beginning of count 9999. Since this pulse is always available as "carry" from a synchronous counter, no extra decoding is required. A bonus feature of this circuit is that latching the counter output becomes very simple with no potential race condition existing. The designer has one complete clock pulse to transfer the counter data to the latches and decouple them before a false reading will occur. The timing diagram for a signal ≈ 0 is shown in figure 3.

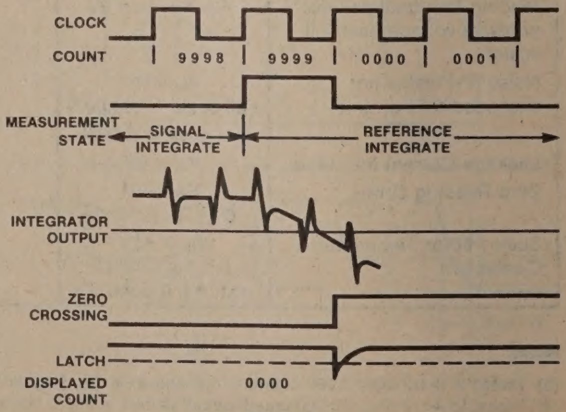


Figure 3

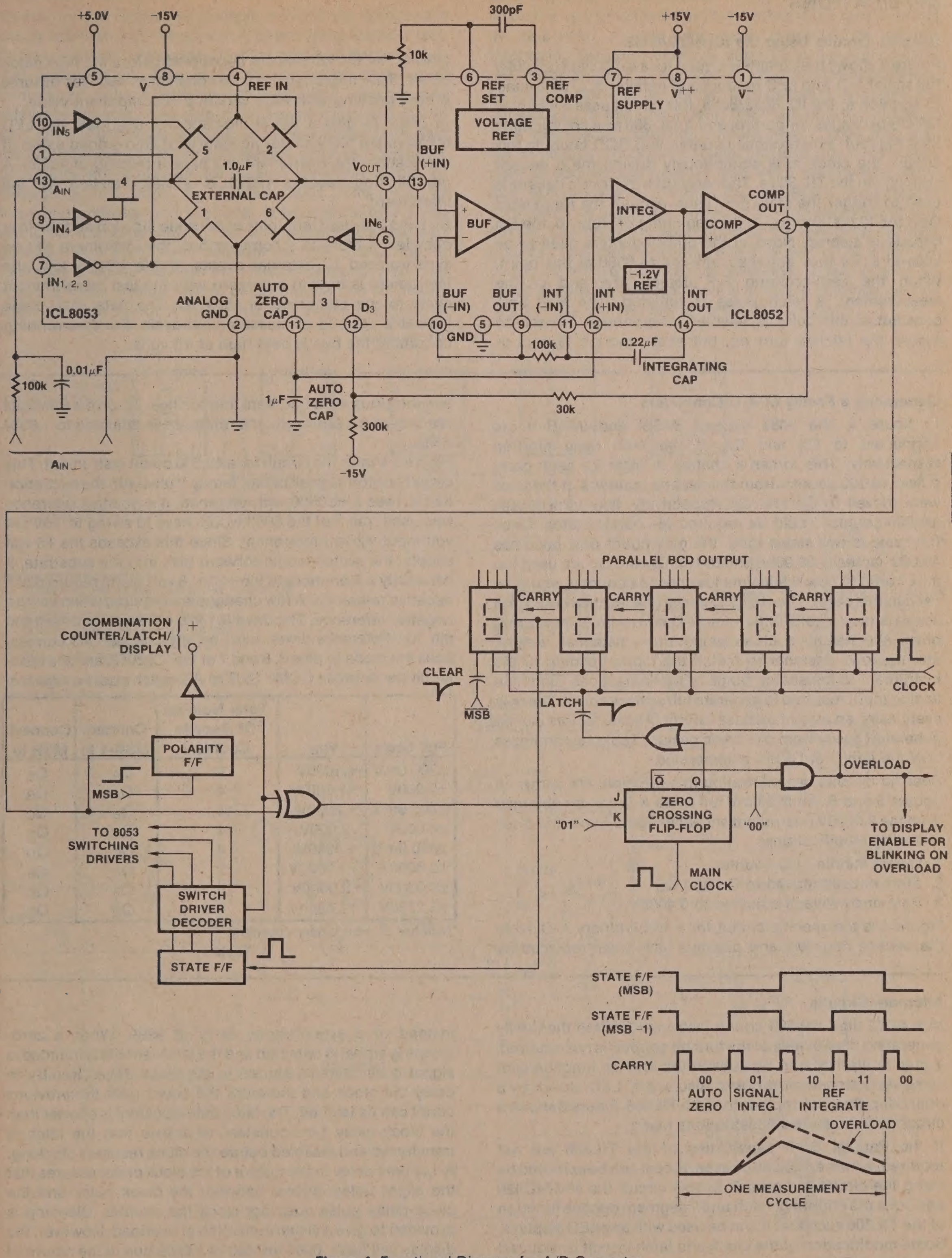

+5.0V
−15V
300pF
10k
+15V
−15V
V+
V−
REF IN
REF SET
REF COMP
REF SUPPLY
V++
V−
VOLTAGE REF
IN5
A_{IN}
IN4
$IN_{1,2,3}$
5
2
1.0µF
EXTERNAL CAP
1
6
4
3
V_{OUT}
BUF (+IN)
IN6
BUF
INTEG
COMP
COMP OUT
−1.2V REF
ICL8053
ANALOG GND
AUTO ZERO CAP
D_3
BUF (−IN)
BUF OUT
INT (−IN)
INT (+IN)
INT OUT
ICL8052
GND
100k
0.22µF
INTEGRATING CAP
0.01µF
100k
1µF
AUTO ZERO CAP
300k
30k
−15V
A_{IN}
PARALLEL BCD OUTPUT
CARRY
CARRY
CARRY
CARRY
CLEAR
MSB
CLOCK
LATCH
COMBINATION COUNTER/LATCH/ DISPLAY
+
POLARITY F/F
MSB
OVERLOAD
Q̄
Q
J
K
ZERO CROSSING FLIP-FLOP
"01"
"00"
TO DISPLAY ENABLE FOR BLINKING ON OVERLOAD
TO 8053 SWITCHING DRIVERS
SWITCH DRIVER DECODER
MAIN CLOCK
STATE F/F
STATE F/F (MSB)
STATE F/F (MSB −1)
CARRY
00 AUTO ZERO
01 SIGNAL INTEG
10
11 REF INTEGRATE
00
OVERLOAD
ONE MEASUREMENT CYCLE

Figure 4: Functional Diagram for A/D Converter

APPLICATIONS

Specific Circuits Using the ICL8052/8053

Figure 5 shows the complete circuit for a 4-1/2 digit (±2.000V full scale) A-D with LED readout and parallel BCD data lines. In addition to the ICL8052/8053, this circuit uses 6 low-cost CMOS packages for control and 5 TIL 306 as a combination LED readout, synchronous counter, and BCD latch. In this circuit, the clock runs continuously driving the 5 decade counters in the TIL 306's. The carry from the fourth decade is used to trigger the state F-F. Thus, each of the four states lasts for 10,000 counts. At the beginning of state 10, the 5th decade is cleared. None of the other counters need to be cleared since they automatically roll to 0000 at this point. When the zero-crossing F-F detects the end of the measurement, a latch pulse is initiated. The R-C time constant of this pulse is selected long enough (50nsec) to assure the latches turn on, but short enough (3μsec) to assure that the latches are decoupled before the next clock pulse. Selecting a typical time constant of 400nsec assures proper latching with wide variance in component value.

In order to give a visual indication of overload, the LED displays are blanked during state 00 if an overload exists. If overloaded, the instrument will blink a reading of 19999. A non-blinking reading 19999 is a valid reading for the instrument.

By tying the clear terminals of the state flip-flop and the four decade counters to a common bus, the instrument can be synchronized to external events. If the bus is low, the instrument is held in auto-zero with the last measurement cycle at the beginning of state 00. The data valid pulse indicates the end of measurement cycle. For free-running condition, the bus is held high at +5 volts.

Generating a Family of A-D Converters

In figure 5, the lines marked (MSB) and (MSB-1) are connected to Q_B and Q_A of the 4-bit state flip-flop respectively. This forces a change in state for each carry pulse (10,000 counts) from the decade counters. If the lines were moved to Q_C and Q_B respectively, two carry pulses (20,000 counts) would be required to change states. Since full-scale is two states long, the max count now becomes 40,000; (actually 39,999). Similarly if Q_D and Q_C are used the max count is now 7,999 (one less decade counter would be used in this case). The ability to easily change max count (full scale) is most useful where the A-D converter is measuring physical constants such as temperature, distances, weight, etc. It allows designer to match the digital reading of the instrument to the analog range of the transducer. Since the analog input required to generate full scale output is $2V_{REF}$ in every case, an almost endless variety of scale factors can be generated easily from one basic design. Table I summarizes how the family of DVM's is generated.

Specific circuits demonstrating this principle are shown in figures 5 and 6. An 800.0mV full scale A-D can be obtained from the 2.0000V instrument shown in figure 5 with the three following modifications:

1. Delete middle LED counter.
2. State decode moved to Q_D and Q_C.
3. Reference voltage adjusted to 0.4000V.

Figure 6 is the specific circuit for a 16-bit binary A-D. Here the decade counters and displays have been replaced by synchronous 4-bit counters and latches. To give a full scale reading of ±3.2768 volts the reference is adjusted to 1.6384 volts.

Figure 7 shows the circuit for a 40,000 count instrument. This circuit conforms to all of the "family" rules with the exception that it uses a −2.0000 volt reference. If a positive reference was used, pin 3 of the 8053 would have to swing to +6V (+4 volt input +2 volt reference). Since this exceeds the +5 volt supply, the switch would forward bias into the substrate. It can easily accommodate the +2 to −6 volt swing required of a negative reference. A few changes are required when using a negative reference. The drive to pin 6 (+Reference driver) and pin 10 (−Reference driver) must be interchanged, no connections are made to pins 3, 6 and 7 of the ICL8052, and the resistor divider between COMP OUT to AZ switch must be adjusted.

Full Scale	V_{REF}	Total Number Of Decade Counters	Connect MSB-1 to	Connect MSB to
±200.0mV	+.1000V	4	Q_A	Q_B
±2.000V	+1.000V	4	Q_A	Q_B
±400.0mV	+.2000V	4	Q_B	Q_C
±4.000V	−2.000V	4	Q_B	Q_C
±800.0mV	+.4000V	4	Q_C	Q_D
±2.0000V	+1.0000V	5	Q_A	Q_B
±4.0000V	−2.0000V	5	Q_B	Q_C
±3.2768V	+1.6384V	4*	Q_C	Q_D

*Number of 4-bit binary counters

Table I

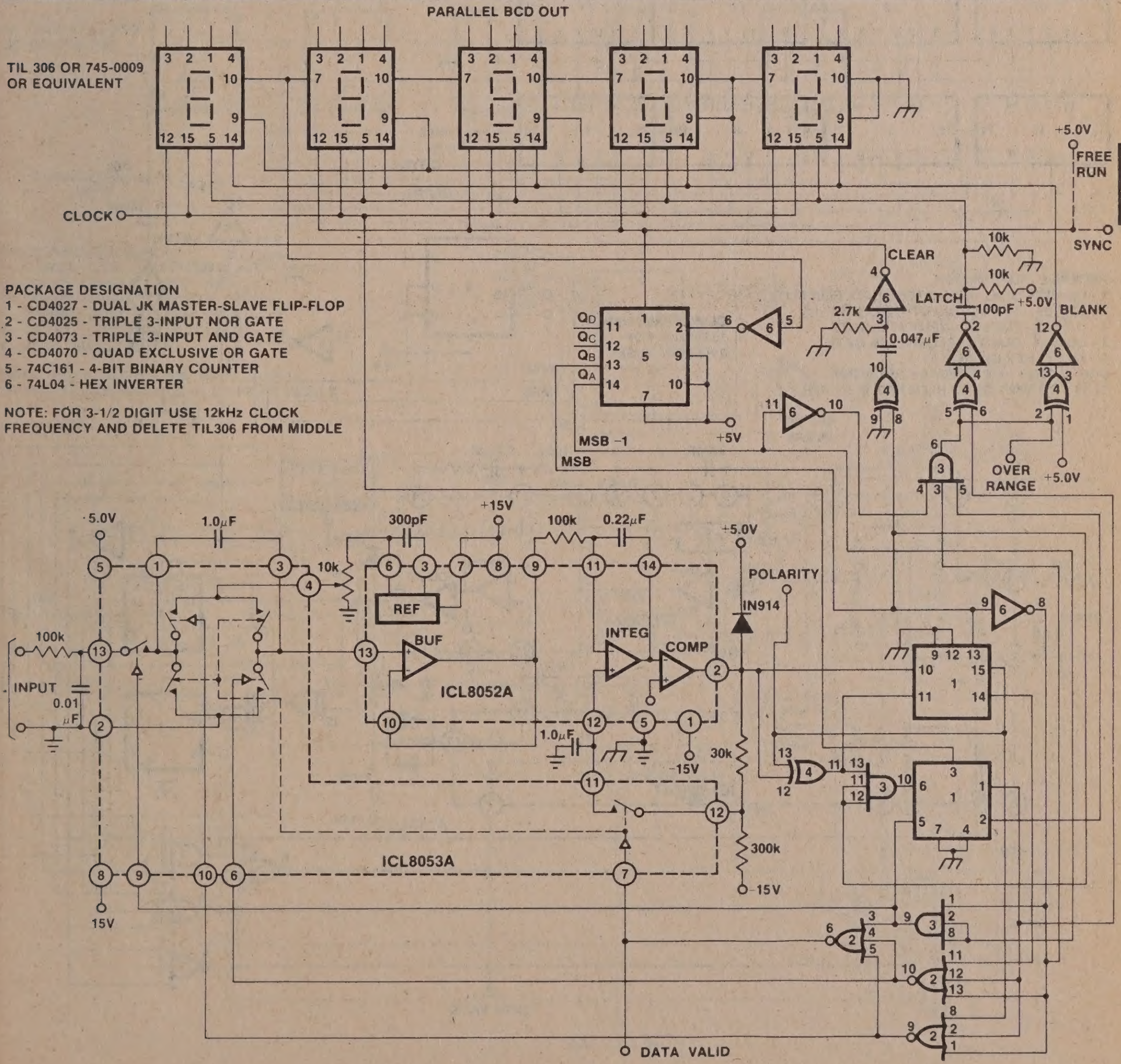
Alternate Circuits

In a 4-1/2 digit (20,000 count) instrument where the family generating capabilities of the four bit counter is not required, a dual D flip-flop can be substituted for this function with some reduction in parts costs. Also a "±1" LED, driven by a dual D flip-flop, can replace the fifth TIL306. Figure 8 shows a circuit with these two substitutions made.

If the Parallel BCD capabilities of the TIL306 are not required, a further reduction in parts cost can be achieved by using the circuit of figure 9. In this circuit the MM74C926 performs the counting, latch and 7 segment decode function of the TIL306 such that it can be used with any LED displays. Some modification of the clock and latch circuit is required since the 74C926 uses a ripple counter with a carry at 0000 instead of a synchronous carry at 9999. When a zero-crossing signal is detected and the latch-enable is initiated, a signal is simultaneously fed to the clock drive circuitry to delay the clock and therefore the count until the previous count can be latched. The latch time-constant is shorter than the clock-delay time-constant to assure that the latch is transferred and disabled before the clock resumes clocking. A 1μs time delay in the output of the clock driver assures that the slight delay (100ns) between the clock pulse and the clock-delay pulse does not clock the counter. Blanking is provided to give a visual indication of overload. However, the display will flash .0000 instead of 1.9999 due to the nature of the ripple counter.

Component Selection

Except for the Reference Voltage, none of the component values are first-order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance the reference capacitor and auto-zero capacitor are each shown as 1.0μF. These relative large values are selected to give greater immunity to PC board leakage since much smaller capacitors are adequate for charge injection errors or leakage errors from the ICL8052/8053. The ratio of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at ±14 volts) due to tolerance build-up between the resistor, capacitor a and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again the .22 value for integrating cap is selected for PC considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating cap is low dielectric absorption. A polypropylene cap (made by TRW) gave excellent results in the application. In fact a good test for dielectric absorption is to test the subject cap in this circuit with the input tied to reference. This ratiometric condition should read 1.0000 and any deviation is probably due to dielectric absorption. In this test poly-carbonate caps typically read .9992, polystyrene, .9997 and polypropylene, 1.0000. The increased temperature coefficient of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.


PARALLEL BCD OUT
TIL 306 OR 745-0009
OR EQUIVALENT
CLOCK
+5.0V
FREE RUN
SYNC
10k
CLEAR
LATCH
100pF
BLANK
2.7k
0.047μF
MSB −1
MSB
+5V
OVER RANGE
+5.0V
Q_D
Q_C
Q_B
Q_A
5.0V
1.0μF
300pF
+15V
100k
0.22μF
10k
REF
BUF
INTEG
COMP
ICL8052A
POLARITY
IN914
100k
INPUT
0.01 μF
1.0μF
-15V
30k
300k
-15V
ICL8053A
15V
DATA VALID

PACKAGE DESIGNATION
1 - CD4027 - DUAL JK MASTER-SLAVE FLIP-FLOP
2 - CD4025 - TRIPLE 3-INPUT NOR GATE
3 - CD4073 - TRIPLE 3-INPUT AND GATE
4 - CD4070 - QUAD EXCLUSIVE OR GATE
5 - 74C161 - 4-BIT BINARY COUNTER
6 - 74L04 - HEX INVERTER

NOTE: FOR 3-1/2 DIGIT USE 12kHz CLOCK FREQUENCY AND DELETE TIL306 FROM MIDDLE

Figure 5: General Circuit for a Family of DVM's.

The output of the comparator is clamped to the +5 volts supply to prevent the positive swing of the comparator from forward biasing the auto-zero switch to its substrate and injecting minority carriers that would be collected as leakage currents. In addition, a voltage translation network connects the output of the comparator to the auto-zero switch. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the CMOS logic (+2.5V) while the auto-zero cap is being charged to V_{REF} (+1V in the case of 2.0000 instrument). Otherwise even with zero signal in, some reference integrate period would be required to drive the comparator output to the threshold region. This would show up as an equivalent offset error. Once the divider chain has been selected, the unit-to-unit variation should contribute less than a few tenths-of-a-count error in the worse case (40,000 count instrument) and proportionately less in other instruments. For a 3-1/2 digit instrument, the error is unmeasurable.

Finally, the back-to-back diodes are used to lower noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At start-up or recovery from an overload, their impedance is low to large signals so the cap can be charged in one auto-zero cycle.

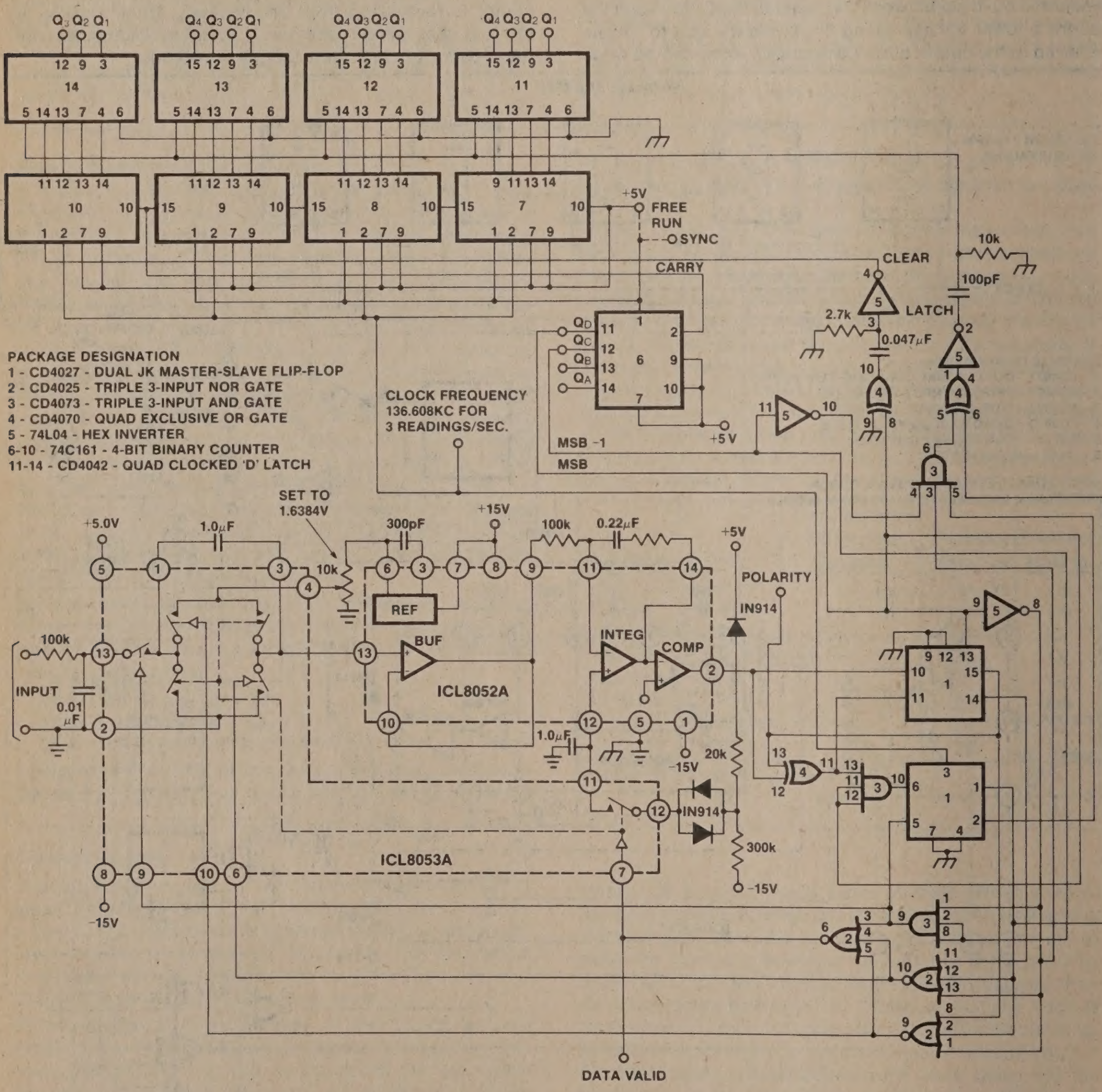

Q3 Q2 Q1
Q4 Q3 Q2 Q1
12 9 3
14
13
12
11
15 12 9 3
5 14 13 7 4 6
11 12 13 14
9 11 13 14
10
9
8
7
15
1 2 7 9
+5V
FREE RUN
SYNC
CARRY
CLEAR
LATCH
10k
100pF
2.7k
0.047μF
QD
QC
QB
QA
MSB -1
MSB
+5V
PACKAGE DESIGNATION
1 - CD4027 - DUAL JK MASTER-SLAVE FLIP-FLOP
2 - CD4025 - TRIPLE 3-INPUT NOR GATE
3 - CD4073 - TRIPLE 3-INPUT AND GATE
4 - CD4070 - QUAD EXCLUSIVE OR GATE
5 - 74L04 - HEX INVERTER
6-10 - 74C161 - 4-BIT BINARY COUNTER
11-14 - CD4042 - QUAD CLOCKED 'D' LATCH
CLOCK FREQUENCY
136.608KC FOR
3 READINGS/SEC.
SET TO
1.6384V
+5.0V
1.0μF
300pF
+15V
100k
0.22μF
10k
REF
BUF
INTEG
COMP
ICL8052A
POLARITY
IN914
INPUT
0.01μF
1.0μF
-15V
20k
300k
IN914
ICL8053A
-15V
DATA VALID

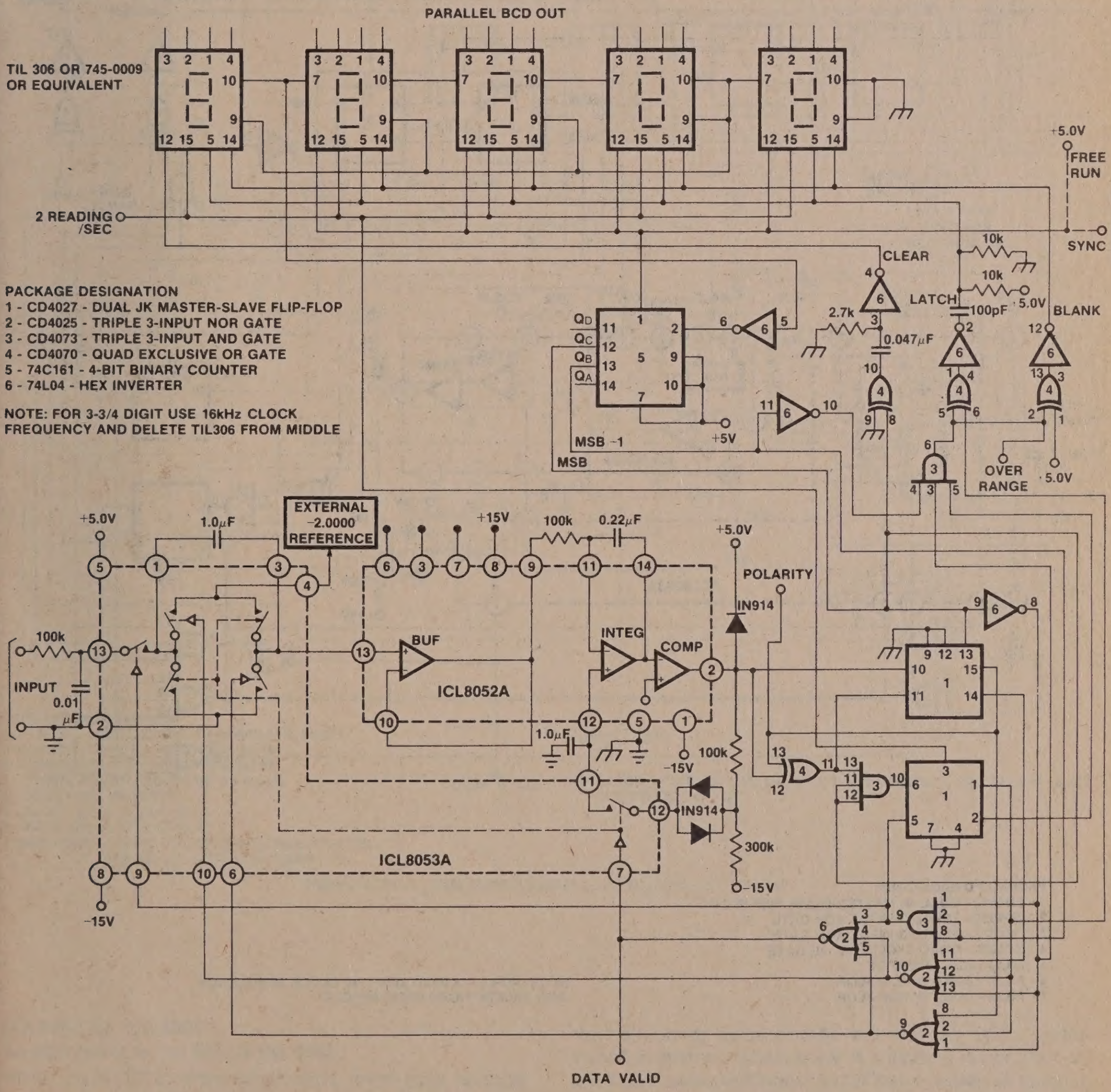
Figure 6: 16-Bit Binary Converter

Max Clock Frequency

The maximum conversion rate of most dual-slope A-D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open-loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μs delay. At a clock frequency of 160kHz (6μs period) half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash "1" on noise peaks even when the input is shorted.

Some circuits use positive feedback or a latch to solve the delay problem. However, unless the comparator voltage swing, the comparator gain, and the integrator gain are carefully controlled, this circuit can generate *anticipation* errors that greatly exceed the 3μs *delay* error. Also it is very susceptible to noise spikes. A more controlled approach for extending the conversion rate is the use of a small resistor in the integrator feedback loop. This feeds a small pulse to the comparator to get it moving quickly, and partially compensate for its delay.

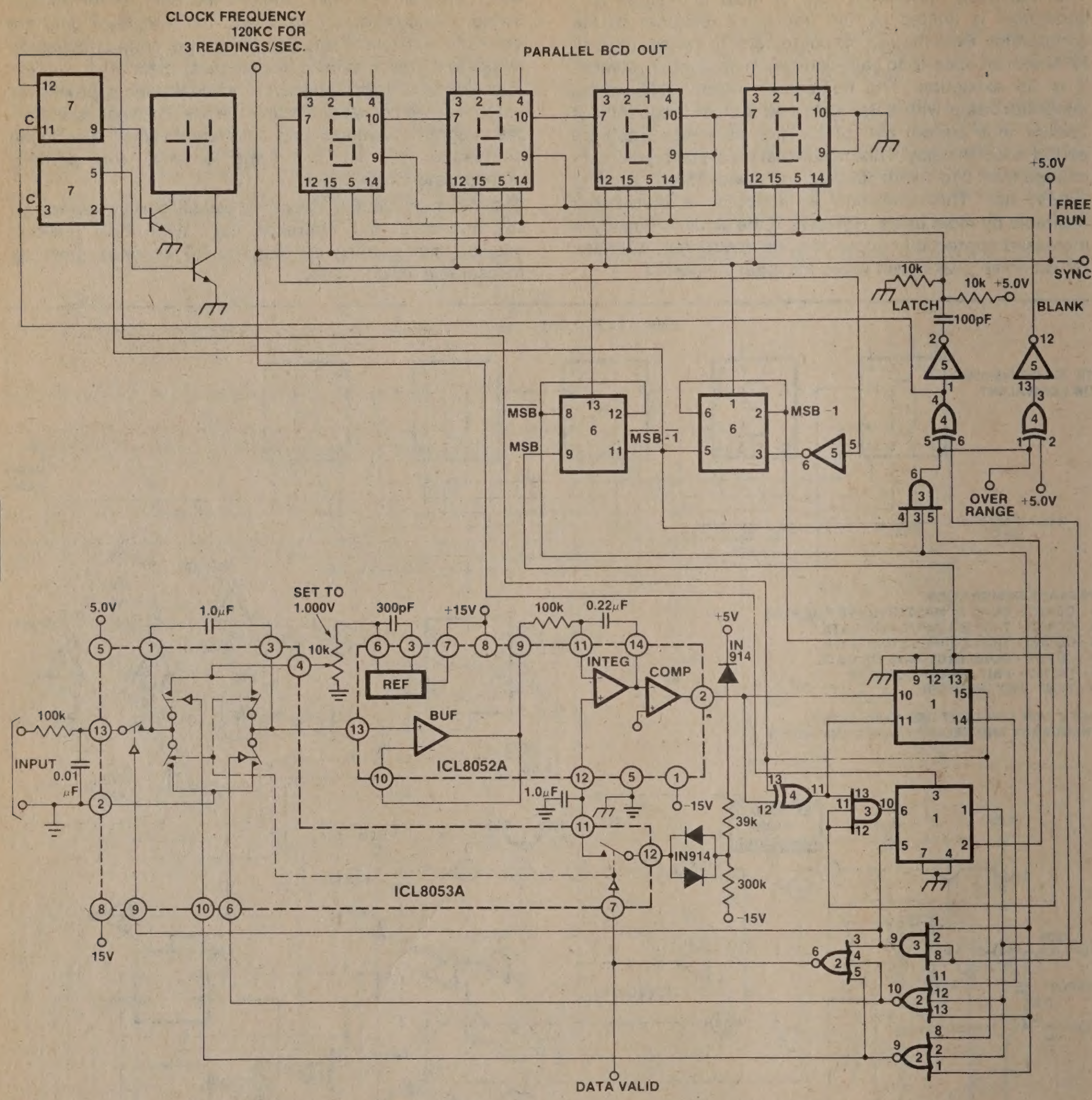
The minimum clock frequency is established by leakage on the auto-zero and reference cap. With most devices, measurement cycles as long as 10 seconds gave no measurable leakage error.


PARALLEL BCD OUT
TIL 306 OR 745-0009 OR EQUIVALENT
3 2 1 4
7
10
9
12 15 5 14
2 READING /SEC
+5.0V
FREE RUN
SYNC
10k
CLEAR
LATCH
100pF
5.0V
BLANK
2.7k
0.047μF
Q_D
Q_C
Q_B
Q_A
MSB -1
MSB
+5V
OVER RANGE
5.0V
EXTERNAL -2.0000 REFERENCE
+5.0V
1.0μF
+15V
100k
0.22μF
POLARITY
IN914
BUF
INTEG
COMP
ICL8052A
100k
INPUT
0.01 μF
1.0μF
-15V
100k
300k
IN914
ICL8053A
-15V
DATA VALID

PACKAGE DESIGNATION
1 - CD4027 - DUAL JK MASTER-SLAVE FLIP-FLOP
2 - CD4025 - TRIPLE 3-INPUT NOR GATE
3 - CD4073 - TRIPLE 3-INPUT AND GATE
4 - CD4070 - QUAD EXCLUSIVE OR GATE
5 - 74C161 - 4-BIT BINARY COUNTER
6 - 74L04 - HEX INVERTER

NOTE: FOR 3-3/4 DIGIT USE 16kHz CLOCK FREQUENCY AND DELETE TIL306 FROM MIDDLE

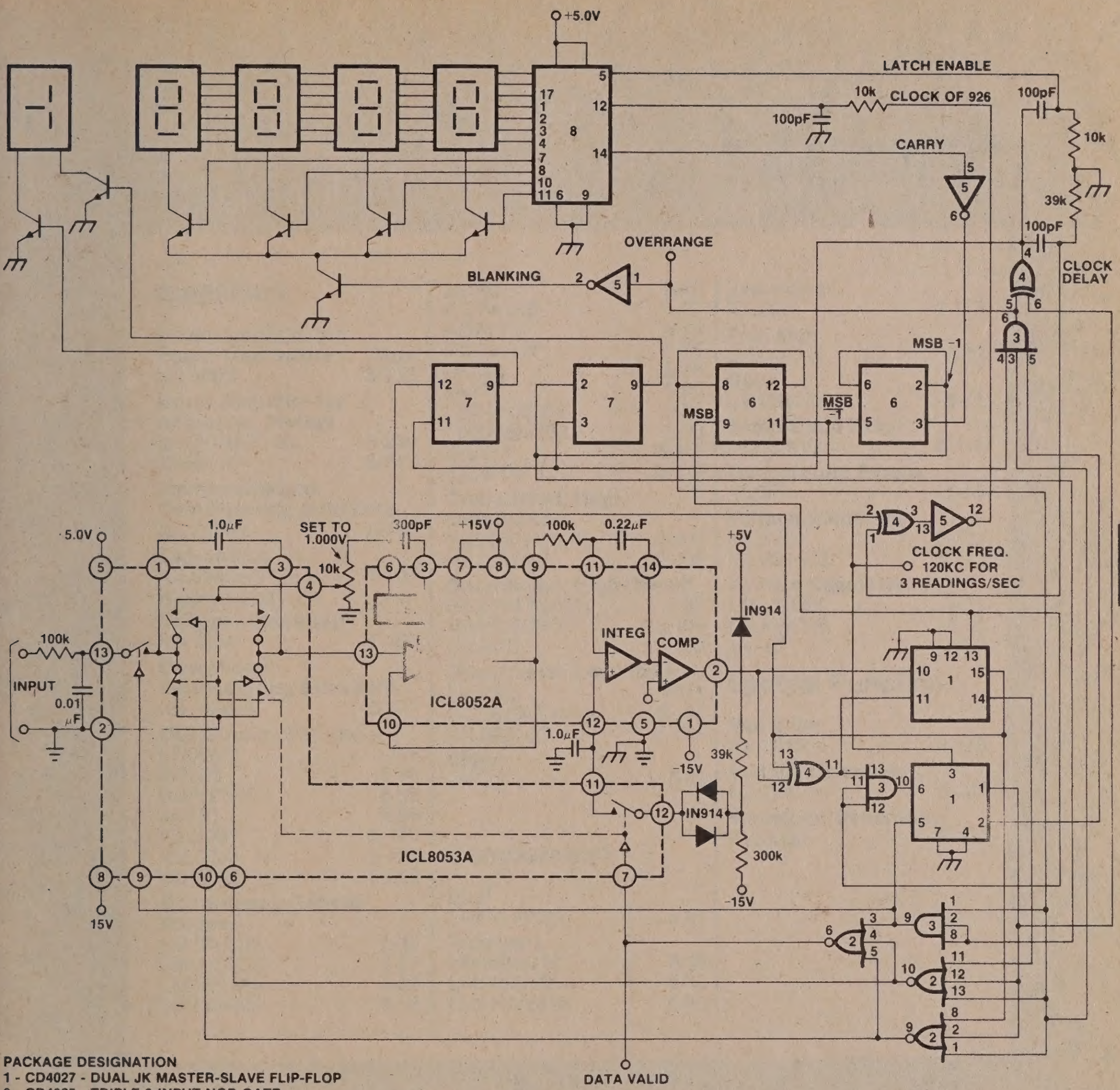
Figure 7: 4-3/4 Digit DVM


CLOCK FREQUENCY
120KC FOR
3 READINGS/SEC.
PARALLEL BCD OUT
+5.0V
FREE RUN
SYNC
10k
10k +5.0V
LATCH
100pF
BLANK
MSB
MSB
MSB -1
MSB -1
OVER RANGE
+5.0V
SET TO
1.000V
5.0V
1.0μF
300pF
+15V
100k
0.22μF
+5V
IN 914
10k
REF
INTEG
COMP
BUF
100k
INPUT
0.01 μF
ICL8052A
1.0μF
-15V
39k
IN914
300k
-15V
ICL8053A
15V
DATA VALID

PACKAGE DESIGNATION
1 - CD4027 - DUAL JK MASTER-SLAVE FLIP-FLOP
2 - CD4025 - TRIPLE 3-INPUT NOR GATE
3 - CD4073 - TRIPLE 3-INPUT AND GATE
4 - CD4070 - QUAD EXCLUSIVE OR GATE
5 - 74L04 - HEX INVERTER
6 - 74L74 - DUAL 'D' FLIP-FLOP
7 - 74L74 - DUAL 'D' FLIP-FLOP

NOTE: FOR 3-1/2 DIGIT USE 1/10 CLOCK FREQUENCY AND DELETE TIL306 FROM MIDDLE.

Figure 8: 4-1/2 Digit DVM (Parallel BCD)


+5.0V
LATCH ENABLE
10k
CLOCK OF 926
100pF
100pF
10k
CARRY
39k
100pF
CLOCK DELAY
OVERRANGE
BLANKING
MSB -1
MSB
MSB -1
CLOCK FREQ.
120KC FOR
3 READINGS/SEC
5.0V
1.0μF
SET TO 1.000V
300pF
+15V
100k
0.22μF
+5V
10k
100k
INPUT
0.01 μF
INTEG
COMP
IN914
ICL8052A
1.0μF
-15V
39k
IN914
300k
-15V
ICL8053A
15V
DATA VALID

PACKAGE DESIGNATION
1 - CD4027 - DUAL JK MASTER-SLAVE FLIP-FLOP
2 - CD4025 - TRIPLE 3-INPUT NOR GATE
3 - CD4073 - TRIPLE 3-INPUT AND GATE
4 - CD4070 - QUAD EXCLUSIVE OR GATE
5 - 74L04 - HEX INVERTER
6 - 74L74 - DUAL 'D' FLIP-FLOP
7 - 74L74 - DUAL 'D' FLIP-FLOP
8 - MM74C926 - 4 DIGIT COUNTER WITH MULTIPLEXED 7-SEGMENT OUTPUT DRIVERS

NOTE: FOR 3-1/2 DIGIT USE SAME CLOCK FREQUENCY AND DELETE LEAST SIGNIFICANT LED.

Figure 9: 4-1/2 Digit DVM (20,000 Count Multiplexed Display)

ICL8052 vs. ICL8068

An alternative to the 8052 is the 8068.

While the ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances, the ICL8068 has substantially lower noise voltage and will give better performance in systems where noise is a limiting factor, such as low signal level conditions. Specifications may be found in the ICL8068/ICL8052/ICL71C03 and ICL8068/ICL8052/ICL7104 data sheets.

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Operational Amplifiers—General Purpose

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	GBW (typ) (MHz)	I_{SUPP} (mA)	T_A (°C)	Packages*	Remarks
101A	General Purpose, Uncompensated	2.0	75	50,000	0.8	3.0	-55, + 125	J,F,T	
101ALN	Guaranteed Noise 101A	2.0	75	50,000	0.8	3.0	-55, + 125	J,F,T	50 nV/ √Hz @ 10 Hz
107	Gen Purpose, Compensated	2.0	75	50,000	—	3.0	-55, + 125	T	
108	Low Level, Uncompensated	2.0	2.0	50,000	1.0	0.6	-55, + 125	J,F,T	
108A	Low Offset 108	0.5	2.0	80,000	1.0	0.6	-55, + 125	J,F,T	
108LN	Guaranteed Noise 108	2.0	2.0	50,000	1.0	0.6	-55, + 125	T	70 nV/ √Hz @ 10 Hz
124	Quad, Compensated	5.0	300	100,000	1.0	2.0	-55, + 125	J	
301A	Gen Purpose, Uncompensated	7.5	250	25,000	0.8	3.0	0, + 70	P,T	50 nV/ √Hz @ 10 Hz
301ALN	Guaranteed Noise 301A	7.5	250	25,000	0.8	3.0	0, + 70	P,T	
307	Low Bias, Compensated	7.5	250	25,000	—	3.0	0, + 70	P,T	
308	Low Level, Uncompensated	7.5	7.0	25,000	1.0	0.8	0, + 70	F,J,P,T	
308A	Low Offset 308	0.5	7.0	80,000	1.0	0.8	0, + 70	J,T	
308LN	Guaranteed noise 308	7.5	7.0	25,000	1.0	0.8	0, + 70	T	70 nV/ √Hz @ 10 Hz
324	Quad, Compensated	7.0	500	100,000	1.0	2.0	0, + 70	J,P	
741	Gen Purpose Compensated	5.0	500	50,000	1.0	2.8	-55, + 125	T	
741C	Gen Purpose Compensated	6.0	500	25,000	1.0	2.8	0, + 70	P,T	
741HS	Guaranteed Slew Rate 741	5.0	500	50,000	1.0	2.8	-55, + 125	J,T	Slew Rate 0.7V/µS
741CHS	Guaranteed Slew Rate 741C	6.0	500	25,000	1.0	2.8	0, + 70	P,T	Slew Rate 0.7V/µS
741LN	Guaranteed Noise 741	5.0	500	50,000	1.0	2.8	-55, + 125	J,F,T	50 nV/ √Hz @ 10 Hz
741CLN	Guaranteed Noise 741C	6.0	500	25,000	1.0	2.8	0, + 70	P,T	50 nV/ √Hz @ 10 Hz
741K	High Accuracy 741	0.5	50	50,000	1.0	2.8	0 to 70	T	
748	General Purpose	1.0	80	25,000	0.8	2.0	-55 to 125	P,T	
748C	General Purpose, Compensated	1.0	80	25,000	0.8	2.0	0 to 70	P,T	
777	General Purpose Comparator	0.7	25	150,000	0.8	2.5	-55, + 125	P,T	
777C	General Purpose Comparator	0.7	25	150,000	0.8	2.5	0, + 70	P,T	
8008M	Low bias Current, Compensated	5.0	10	20,000	1.0	2.8	-55, + 125	J,T	
8008C	Low bias current, Compensated	6.0	25	20,000	1.0	2.8	-0, + 70	J,P,T	
IH5101	Ultra low noise		1,000	100,000	10.0	15.0	-55 to +125	I	
LH2101A	Dual high performance	2.0	100	25,000	0.8	2.5	-55 to 125	D	
LH2108	Dual super beta	2.0	3.0	25,000	1.0	0.4	-55 to 125	D	
LH2108A	Dual super beta	0.5	3.0	40,000	1.0	0.4	-55 to 125	D	
LH2301A	Dual high performance	7.5	300	15,000	0.8	2.5	0 to 70	D	
LH2308	Dual super beta	7.5	10	15,000	1.0	0.4	0 to 70	D	
LH2308A	Dual super beta	0.5	10	60,000	1.0	0.4	0 to 70	D	

Operational Amplifiers—Low Power Programmable

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	GBW (MHz)	I_{SUPP} (µA)	at I_{set} (µA)	at V_s (V)	T_A (°C)	Packages*
4250	Programmable, Uncompensated	5.0	10	25,000	—	8.0	1	±1.5	-55 to 125	T
4250C	Programmable, Compensated	5.0	10	25,000	—	8.0	1	±1.5	0, to 70	T
		6.0	75	25,000	—	90	10	±1.5		
8021M	Programmable, Compensated	3.0	20	50,000	0.27	40	30	±6.0	-55, - 125	J,T
8021C	Programmable, Compensated	6.0	30	50,000	0.27	50	30	±6.0	0, - 70	T
8022M	Dual 8021M	3.0	20	50,000	0.27	40	30	±6.0	-55, - 125	J,F
8022C	Dual 8021C	6.0	30	50,000	0.27	50	30	±6.0	0, - 70	J,P
8023M	Triple 8021M	3.0	20	50,000	0.27	40	30	±6.0	-55, to 125	J
8023C	Triple 8021C	6.0	30	50,000	0.27	50	30	±6.0	0, to 70	J,P

Video Amplifiers

Type	Description	Gains (typ) (V/V)	Bandwidths (typ) (MHz)	e_n µV (rms)	Output Offset (V)	I_{SUPP} (mA)	T_A (°C)	Packages*
733M	Gain selectable video amp.	400, 100, 10	40, 90, 120	12	1.5	24	-55, + 125	T
733C	Gain selectable video amp.	400, 100, 10	40, 90, 120	12	1.5	24	0, + 70	T

*See package key, page 5-5.

Operational Amplifiers— FET Input

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	GBW (typ) (MHz)	Slew Rate (V/μS)	I_{SUPP} (mA)	T_A (°C)	Packages*	Remarks
LH0042	General Purpose	5.0	10	50,000		6	2.3	-55 to 125	T	
AD503	High accuracy, low offset	20	10	50,000		3	7 max	0, +70	T	
SU536	General Purpose	30	30	50,000		6	6	-55, to125	T	
740M	General Purpose	20	200	50,000	3	6	5.2	-55, +125	T	
740C	General Purpose	110	2000	20,000	1	6	8.0	0, +70	T	
8007M	General Purpose, Compensated	20	20	50,000	1.0	6	5.2	-55, +125	T	All BIFET amplifiers offer low noise — see data sheets.
8007AM	8007M, Low I_b	30	1.0	20,000	1.0	2.5	6	-55, +125	T	
8007C	General Purpose, Compensated	50	50	20,000	1.0	6	6	0, +70	T	
8007AC	8007C, Low I_b	30	1.0	20,000	1.0	2.5	6	0, +70	T	
8043M	Dual 8007M	20	20	50,000	1.0	6.0	6	-55, +125	J	
8043C	Dual 8007C	50	50	20,000	1.0	6.0	6.8	-55, +125	J,P	
8500	MOSFET Input, Compensated	50	0.1	20,000	0.7	0.5	2.7	-25, +85	T	
8500A	MOSFET Input, Super Low I_b	50	0.01	20,000	0.7	0.5	2.7	-25, +85	T	

Operational Amplifiers—High Speed

Type	Description	V_{OS} (mV)	I_b (pA)	A_{VOL} (V/V)	GBW (MHz)	Slew Rate (V/μS)	I_{SUPP} (mA)	T_A (°C)	Packages*
HA2500	High slew rate, Compensated	5.0	200	20,000	12	25	6.0	-55, + 125	F,T,J
HA2502	High slew rate, Compensated	8.0	250	15,000	12	20	6.0	-55, + 125	F,T,J
HA2505	High slew rate, Compensated	8.0	250	15,000	12	20	6.0	0, + 75	F,T
HA2507	High slew rate, Compensated	5.0	125	15,000	12	30	4.0	0 to 75	F,T
HA2510	High slew rate, Compensated	8.0	200	10,000	12	50	6.0	-55, + 125	F,T
HA2512	High slew rate, Compensated	10.0	250	7,500	12	40	6.0	-55, + 125	F,T
HA2515	High slew rate, Compensated	10.0	250	7,500	12	40	6.0	0, + 75	F,T
HA2517	High slew rate, Compensated	5.0	125	7,500	12	60	4.0	0 to 75	F,T
HA2520	Compensated for $A_v \geq 3$	8.0	200	10,000	30	100	6.0	-55, + 125	F,T,J
HA2522	Compensated for $A_v \geq 3$	10.0	250	7,500	30	80	6.0	-55, + 125	F,T,J
HA2525	Compensated for $A_v \geq 3$	10.0	250	7,500	30	80	6.0	0, + 75	F,T,J
HA2527	High slew rate, Compensated for $A_v \geq 3$	5.0	125	7,500	20	120	4.0	-65 to 150	F,T
8017M	High speed, inverting	5.0	200	25,000	10	130*	7.0	-55 + 125	T,F
8017C	High speed, inverting	7.0	200	25,000	10	130*	8.0	0 + 70	T,F

Operational Amplifiers—High Impedance

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	Slew Rate (V/μS)	I_{SUPP} (mA)	T_A (°C)	Packages*
HA2600	High impedance, Compensated	4.0	10	100,000	4	3.7	-55, + 125	F,J,T
HA2602	High impedance, Compensated	5.0	25	80,000	4	4.0	-55, + 125	F,J,T
HA2605	High impedance, Compensated	5.0	25	80,000	4	4.0	0, + 75	F,J,T
HA2607	High impedance, Compensated	4.0	5	70,000	7	3.0	0 to 75	P
HA2620	2600 Compensated for $A_v \geq 5$	4.0	15	100,000	25	3.7	-55, + 125	F,J,T
HA2622	2602 Compensated for $A_v \geq 5$	5.0	25	80,000	20	4.0	-55, + 125	F,J,T
HA2625	2605 Compensated for $A_v \geq 5$	5.0	25	80,000	20	4.0	0, + 75	F,J,T
HA2627	2607 Compensated for $A_v \geq 5$	4.0	5	70,000	35	3.0	0 to 75	P

See package key, page 5-5.

Voltage Followers

Type	Description	V_{OS} (mV)	I_{IN} (nA)	A_V(MIN) (V/V)	3 db B/W (MHz)	Slew Rate (V/µS)	Output Swing (V)	I_{SUPP} (mA)	T_A (°C)	Packages*
102	Voltage Follower	5	10	0.999	—	—	±10	4.0	-55, + 125	F,T
110	Voltage Follower	4	3	0.999	—	—	±10	—	-55, + 125	J,F,T
302	Voltage Follower	15	30	0.9985	15	30	±10	4.0	0, + 70	T
310	Voltage Follower	7.5	7	0.999	15	30	±10	—	0, + 70	J,P,T
LH2110	Dual Voltage Follower	4.0	3	0.999	—	—	±10	4.0	-55, + 125	D
LH2310	Dual Voltage Follower	7.5	7	0.999	—	—	±10	4.0	0 to 70	D

Comparators

Type	Description	V_{OS} (mV)	I_b (nA)	A_v (V/mV)	t_{pd} (ns)(typ)	I_{SUPP} (mA)	V_{OL} (V)	I_{OL} (mA)	T_A (°C)	Packages*
111	Precision Comparator	3	100	200	200	6	0.4	8	-55, + 125	J,F,T
311	Precision Comparator	7.5	250	200	200	7.5	0.4	8	0, + 70	J,F,P,T
8001M	Low Power Comparator	3	100	15	250	2	0.5	2	-55, + 125	T
8001C	Low Power Comparator	5	250	15	250	2	0.4	2	0, + 70	T
LM139	Quad. Comparator	5	100	200	1300	2	0.7	4	-55, + 125	J
LM239	Quad. Comparator	5	250	200	1300	2	0.7	4	-25, + 85	J
LM339	Quad. Comparator	5	250	200	1300	2	0.7	4	0, + 70	J,P
LH2111	Dual Precision Comparator	3	100	200	200	6	0.4	8	-55, + 125	J
LH2311	Dual Precision Comparator	7.5	250	200	200	7.5	0.4	8	0, to 70	J

Notes: t_{pd} measured for 100 mV step with 5 mV overdrive
I_{SUPP} measured for V_{SUPP} + ±15V

Power Amplifiers

Type	Description	Use	Output Current (A)	Output Swing (V)	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	Slew Rate (V/µS)	Quiescent I_{SUPP} (mA)	T_A (°C)
ICH8510M	Hybrid Power Amp.	Servo	1.0	±26	3.0	250	100,000	0.5	40	-55, + 125
ICH8510C	Hybrid Power Amp.	and	1.0	±26	6.0	500	100,000	0.5	50	-25, + 85
ICH8520M	Hybrid Power Amp.	Actuator	2.0	±26	3.0	250	100,000	0.5	40	-55, + 125
ICH8520C	Hybrid Power Amp.		2.0	±26	6.0	500	100,000	0.5	50	-25, + 85
ICH8530M	Hybrid Power Amp.		2.7	±25	3.0	250	100,000	0.5	40	-55, + 125
ICH8530C	Hybrid Power Amp.		2.7	±25	6.0	500	100,000	0.5	50	-25, + 85
ICL8063C	Monolithic Power Amp.	Power	2.0	±27	50		6		250	0, + 70
ICL8063M	Monolithic Power Amp.	Transistors	2.0	±27	75		6		300	-55, + 125

Note 1. Specifications apply at ±30V supplies.
2. All units packaged in 8 lead TO3 can.
3. Fully protected against inductive current flow.
4. Externally settable output current limiting.

Voltage Regulators

Type	Input Voltage (V) min	Input Voltage (V) max	Output Voltage (V) min	Output Voltage (V) max	Input/Output Differential (V) min	Input/Output Differential (V) max	Load Current (mA) min	Load Current (mA) max	Load Regulation (%)	Line Regulation (%/V)	Avg. Temp. Coeff. (%/°C)	Pd at 25°C (mW)	T_j (°C)	Packages*
100	8.5	40	2.0	30	2.0	30	3.0	12	0.5	0.2	0.005	500	- 55, + 150	F,T
105	8.5	50	4.5	40	3.0	30	0	12	0.05	0.06	0.005	500	- 55, + 150	F,T
300	8.0	30	2.0	20	3.0	20	3.0	12	0.5	0.2	0.03	300	0, + 70	T
305	8.0	40	4.5	30	3.0	30	0	12	0.05	0.06	0.03	500	0, + 70	T
723	9.5	40	2.0	37	3.0	38	0	50	0.15	0.03	0.015	800	- 55, + 125	T,J
723C	9.5	40	2.0	37	3.0	38	0	50	000.2	0.03	0.015	660	0, + 70	P,T

*See package key, page 5-5.

Monolithic Voltage Converter—The ICL7660

Converts positive voltage into negative voltages over a range of +1.5V through +10V. May be cascaded for higher negative output voltages, paralleled for greater output current, used as a positive voltage multiplier, or any combination of the above. Typical supply current is 170µA, and output source resistance is 55Ω at T_A = 25°C and I_o = 20mA.

Special Function Circuits

Type		Accuracy	V_{SUPP} (V)	T_A (°C)	Packages*
AD590	Temperature transducer—output linear at 1 μA/°K	±1°C	4 to 30	-55 to 150	F,H
8013AM	Four quadrant multiplier. Output proportional to algebraic products of two input signals. Features ±0.5% accuracy; internal op-amp for level shift, division and square root functions; full ±10V input/output range; 1 MHz bandwidth.	±0.5%	±15	-55, + 125	T
8013BM		±1.0%	±15	-55, + 125	T
8013CM		±2.0%	±15	-55, + 125	T
8013AC		±0.5%	±15	0, + 70	T
8013BC		±1.0%	±15	0, + 70	T
8013CC		±2.0%	±15	0, + 70	T
8038AM	Simultaneous Sine, Square, and Triangle wave outputs T^2L compatible to 28V over frequency range from 0.01 Hx to 1.0 MHz. Low distortion (<1%); high linearity (0.1%); low frequency drift with temperature (50ppm/°C max.), variable duty cycle (2%-98%).	1.5%	±5 to ±15	-55, + 125	J
8038AC		1.5%	±5 to ±15	0, + 70	J
8038BM		3.0%	±5 to ±15	-55, + 125	J
8038BC		3.0%	±5 to ±15	0, + 70	P
8038CC	External frequency modulation.	5.0%	±5 to ±15	0, + 70	P
8048BC	Log amp. 1V/decade (Adjustable). 120 db range with current input. Error referred to output.	±30 mV	±15	0, + 70	J,P
8048CC		±60 mV	±15	0, + 70	J,P
8049BC	Antilog amp. adjustable scale factor.	±10 mV	±15	0, + 70	J,P
8049CC	Error referred to input	±30 mV	±15	0, + 70	J,P
8069	1.2V temperature compensated voltage reference		5 to 15	-55, + 125	TO-52, TO-92
8211M	Micropower voltage detector/indicator/voltage regulator/ programmable zener. Contains 1.15V micropower reference plus comparator and hysteresis output. Main output inverting (8212) or non-inverting (8211).	2 to 30	-55, + 125	T	
8211C		2 to 30	0, + 70	P,T	
8212M		2 to 30	-55, + 125	T	
8212C		2 to 30	0, + 70	P,T	

Note: All parameters are specified at V_{SUPP} = ± 15V and T_A = + 25°C unless otherwise noted.
Package Key: D—Solder lid side brazed ceramic dual in line. F—Ceramic flat pack. J—Glass frit seal ceramic dual in line. P—Plastic dual in line. T—Metal can.

Operational Amplifiers—CMOS

Type	Description	Compensation	Offset Null	V_{OS} Selection	I_{OS}	I_B	Output Swing	Input CMR	Packages*
7611	Single, Selectable I_Q	Internal	Yes	2, 5, 15 mV	0.5 pA	1 pA	V_{SUPP} - 100 mV	V_{SUPP} - 100 mV	P,T
7612	Single, Selectable I_Q, Extended CMVR	Internal	Yes	2, 5, 15 mV	0.5 pA	1 pA	V_{SUPP} + 300 mV	V_{SUPP} - 100 mV	P,T
7613	Single, Selectable I_Q, Input Protected	Internal	Yes	2, 5, 15 mV	0.5 pA	1 pA	V_{SUPP} - 100 mV	V_{SUPP} - 100 mV	P,T
7614	Single, Fixed I_Q	External	Yes	2, 5, 15 mV	0.5 pA	1 pA	V_{SUPP} - 100 mV	V_{SUPP} - 100 mV	P,T
7615	Single, Fixed I_Q Input Protected	External	Yes	2, 5, 15 mV	0.5 pA	1 pA	V_{SUPP} - 100 mV	V_{SUPP} - 100 mV	P,T
7621	Dual, Fixed I_Q	Internal	No	2, 5, 15 mV	0.5 pA	1 pA	V_{SUPP} - 100 mV	V_{SUPP} - 100 mV	P,T
7622	Dual, Fixed I_Q	Internal	Yes	2, 5, 15 mV	0.5 pA	1 pA	V_{SUPP} - 100 mV	V_{SUPP} - 100 mV	P,J
7631	Triple, Selectable I_Q	Internal	No	5, 10, 20 mV	0.5 pA	1 pA	V_{SUPP} - 100 mV	V_{SUPP} - 100 mV	P,J
7632	Triple, Selectable I_Q	None	No	5, 10, 20 mV	0.5 pA	1 pA	V_{SUPP} - 100 mV	V_{SUPP} - 100 mV	P,J
7641	Quad, Fixed I_Q	Internal	No	5, 10, 20 mV	0.5 pA	1 pA	V_{SUPP} - 100 mV	V_{SUPP} - 100 mV	P,J
7642	Quad, Fixed I_Q	Internal	No	5, 10, 20 mV	0.5 pA	1 pA	V_{SUPP} - 100 mV	V_{SUPP} - 100 mV	P,J

Precision Operational Amplifiers, V_{SUPP} = ±2V to ±8V

Type	Description	V_{OS} (μV)	ΔV_{OS} (μV/°C)	ΔV_{OS} (μV/year)	I_{SUPP} (mA)	A_V (dB, min)	Packages*	T_A°C
ICL 7600C	Compensated	±2	±0.01	0.2	1.7	90	J,P	0 to 70
ICL 7600I	Compensated	±2	±0.01	0.2	1.7	90	J,P	-25 to 85
ICL 7600M	Compensated	±2	±0.05	0.2	1.7	90	J,P	-55 to 125
ICL 7601C	Uncompensated	±2	±0.01	0.2	1.7	90	J,P	0 to 70
ICL 7601I	Uncompensated	±2	±0.01	0.2	1.7	90	J,P	-25 to 85
ICL 7601M	Uncompensated	±2	±0.05	0.2	1.7	90	J,P	-55 to 125

Precision Instrumentation Amplifiers, V_{SUPP} = ±2V to ±5V, I_{SUPP} = 1.7mA

Type	Description	V_{OS} (μV)	ΔV_{OS} (μV/°C)	ΔV_{OS} (μV/year)	A_V (dB, min)	Slew Rate (V/μs)	I_{BIAS} (pA)	Packages*	T_A°C
ICL 7605C	Compensated	±2	±0.01	0.5	90	0.5	±300	J,P	0 to 70
ICL 7605I	Compensated	±2	±0.01	0.5	90	0.5	±300	J,P	-25 to 85
ICL 7605M	Compensated	±2	±0.05	0.5	90	0.5	±300	J,P	-55 to 125
ICL 7606C	Uncompensated	±2	±0.01	0.5	90	0.5	±300	J,P	0 to 70
ICL 7606I	Uncompensated	±2	±0.01	0.5	90	0.5	±300	J,P	-25 to 85
ICL 7606M	Uncompensated	±2	±0.05	0.5	90	0.5	±300	J,P	-55 to 125
ICL 7650C	V_{SUPP} = ±3V to ±8V	±1	±0.01	100 nV/$\sqrt{\text{month}}$	126	2.5	±1.5	J,P,T	0 to 70
ICL 7650I	V_{SUPP} = ±3V to ±8V	±1	±0.01	100 nV/$\sqrt{\text{month}}$	126	2.5	±1.5	J,P,T	-25 to 85

* See package key above.

LH0042
Operational Amplifier/Buffer

FEATURES

- **Low input offset voltage—5mV-typ.**
- **High open loop gain—100 dB typ.**
- **Excellent slew rate—3.0 V/μs typ.**
- **Internal 6 dB/octave frequency compensation**
- **Pin compatible with standard IC op amps (TO-5 package)**

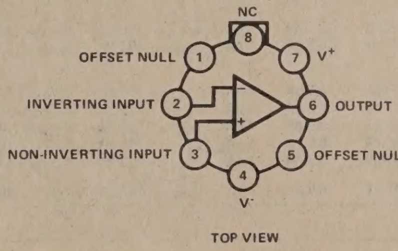
GENERAL DESCRIPTION

The LH0042 is a FET input operational amplifier with very closely matched input characteristics, very high input impedance, and ultra-low input current, with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. Devices are internally compensated and free of latch-up and unusual oscillation problems, and may be offset nulled with a single 10K trimpot with negligible effect in CMRR.

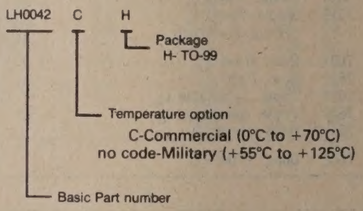
The LH0042 is specified for operation over the −55°C to +125°C military temperature range. The LH0042C is specified for operation over the −25°C to +85°C temperature range.

The LH0042 IC op amp is intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0042 provides low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

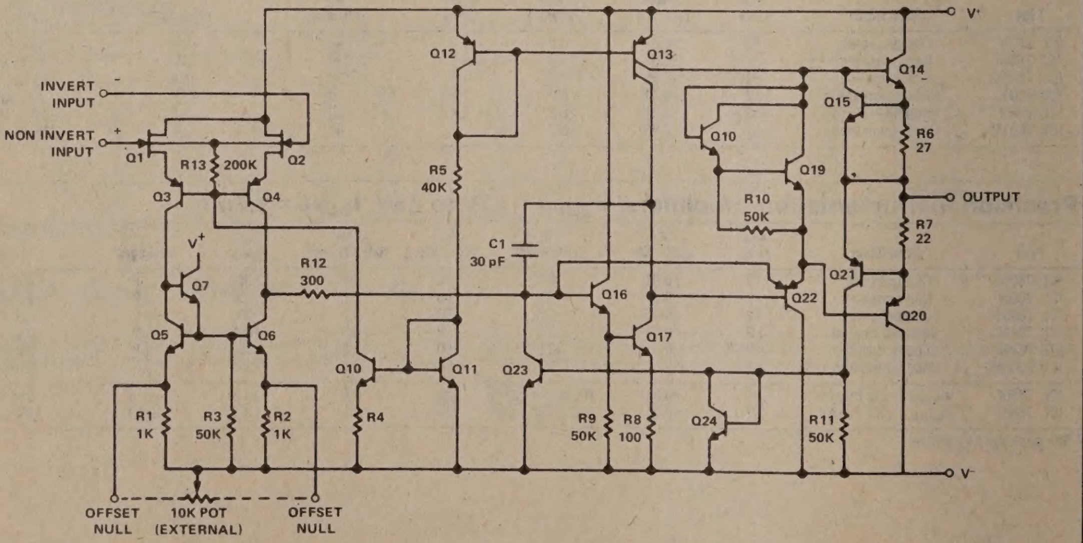
PIN CONFIGURATION (outline dwg TO-99)


NC
8
OFFSET NULL 1
7 V+
INVERTING INPUT 2
6 OUTPUT
NON-INVERTING INPUT 3
5 OFFSET NULL
4
V-
TOP VIEW

ORDERING INFORMATION


LH0042 C H
Package
H- TO-99
Temperature option
C-Commercial (0°C to +70°C)
no code-Military (+55°C to +125°C)
Basic Part number

EQUIVALENT CIRCUIT


V+
INVERT INPUT −
NON INVERT INPUT +
Q1
Q2
R13 200K
Q3
Q4
V+
Q7
R12 300
Q5
Q6
R1 1K
R3 50K
R2 1K
R4
OFFSET NULL
10K POT (EXTERNAL)
OFFSET NULL
Q12
R5 40K
C1 30 pF
Q10
Q11
Q23
Q13
Q14
Q15
Q10
Q19
R10 50K
R6 27
OUTPUT
R7 22
Q21
Q22
Q16
Q17
Q20
R9 50K
R8 100
Q24
R11 50K
V-

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Power Dissipation (see graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V⁻	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0042	−55°C to +125°C
LH0042C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS for LH0042/LH0042C

(T_A = 25°C, V_S = ±15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0042			LH0042C			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$R_S \leq 100\ k\Omega$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5			10		µV/°C
Offset Voltage Drift with Time			7			10		µV/week
Input Offset Current			1	5		2	10	pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current			10	25		15	50	pA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	70	86		70	80		dB
Large Signal Voltage Gain	$R_L = 1\ k\Omega$, $V_{OUT} = \pm 10V$	50	150		25	100		V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$	±10	±12.5		±10	±12		V
Output Current Swing	$V_{OUT} = \pm 10V$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current			2.5	3.5		2.8	4.0	mA
Power Consumption				105			120	mW

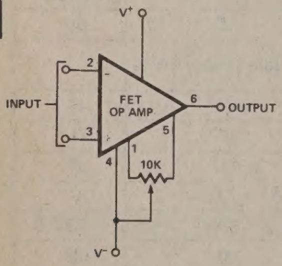
AC ELECTRICAL CHARACTERISTICS For all amplifiers (T_A = 25°C, V_S = ±15V)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0042			LH0042C			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/µs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	µs
Overshoot			10	30		15	40	%
Settling Time (0.1 %)	ΔV_{IN} = 10V		4.5			4.5		µs
Overload Recovery			4.0			4.0		µs
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 100 Hz		55			55		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 1 kHz		35			35		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 kHz		30			30		nV/√Hz
Input Noise Voltage	BW = 10 Hz to 10 kHz, R_S = 10 kΩ		12			12		µVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

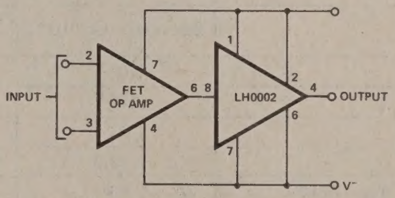
Notes:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.
3. Unless otherwise specified, these specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq \pm 125°C$ for the LH0042 and $-25°C \leq T_A + 85°C$ for the LH0042C. Typical values are given for T_A = 25°C.

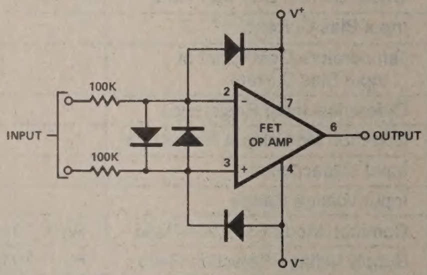
AUXILIARY CIRCUITS (shown for TO-5 pin out)


V+
2
INPUT
FET OP AMP
6
OUTPUT
3
5
4
1
10K
V-

OFFSET NULL


2
7
1
INPUT
FET OP AMP
6 8
LH0002
2
4
OUTPUT
3
4
6
7
V-

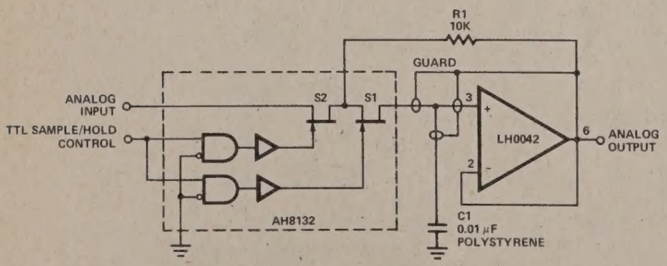
BOOSTING OUTPUT DRIVE TO ±100 mA


V+
100K
2
7
INPUT
FET OP AMP
6
OUTPUT
100K
3
4
V-

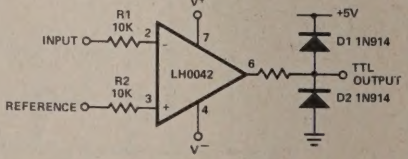
NOTE: ALL DIODES ARE ULTRA LOW LEAKAGE

PROTECTING INPUTS FROM ±150V TRANSIENTS

TYPICAL APPLICATIONS


R1
10K
GUARD
ANALOG INPUT
S2
S1
3
TTL SAMPLE/HOLD CONTROL
LH0042
6
ANALOG OUTPUT
2
AH8132
C1
0.01 µF
POLYSTYRENE

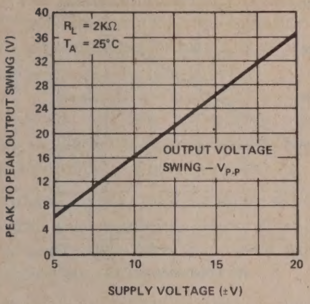
ALTERNATE LOW DRIFT SAMPLE


V+
R1
10K
INPUT
2
7
+5V
D1 1N914
LH0042
6
TTL OUTPUT
R2
10K
REFERENCE
3
4
D2 1N914
V-

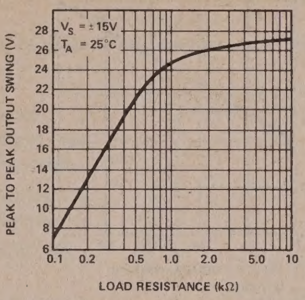
PRECISION VOLTAGE COMPARATOR

TYPICAL PERFORMANCE CHARACTERISTICS (CON'T.)

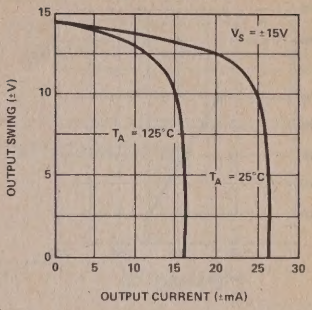
OUTPUT SWING VS SUPPLY VOLTAGE



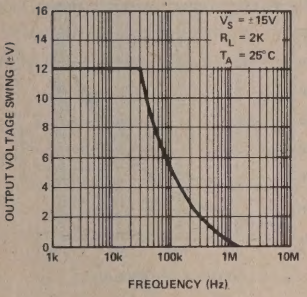
OUTPUT VOLTAGE SWING VS LOAD RESISTANCE



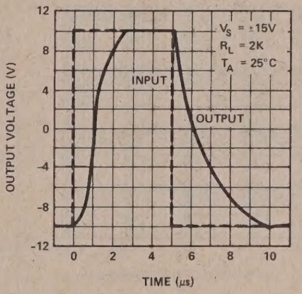
CURRENT LIMITING



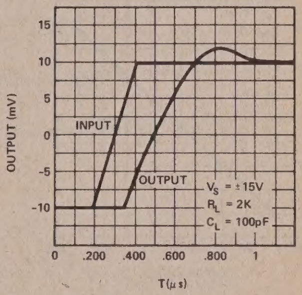
OUTPUT VOLTAGE SWING VS FREQUENCY



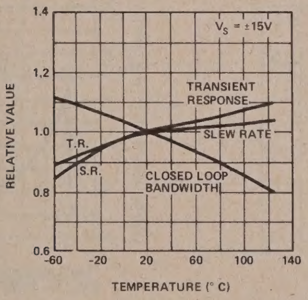
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



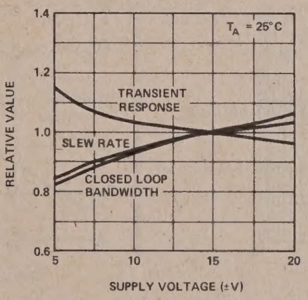
TRANSIENT RESPONSE



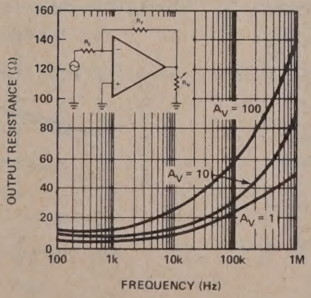
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



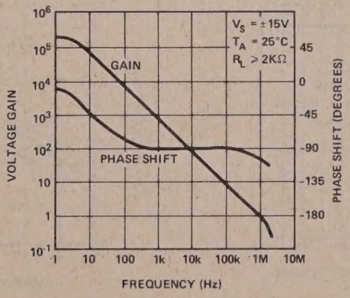
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



OUTPUT RESISTANCE VS FREQUENCY

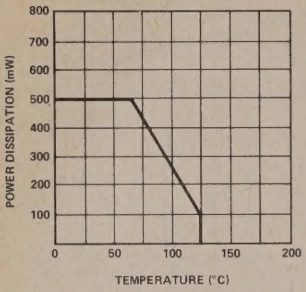


OPEN LOOP TRANSFER CHARACTERISTICS VS FREQUENCY

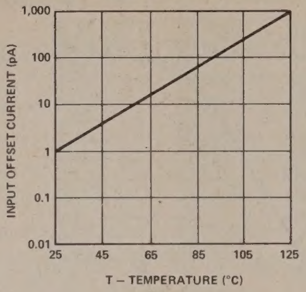


TYPICAL PERFORMANCE CHARACTERISTICS

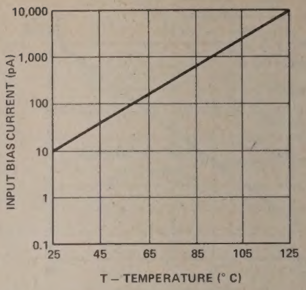
MAXIMUM POWER DISSIPATION



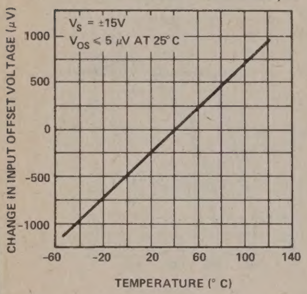
INPUT OFFSET CURRENT VS TEMPERATURE



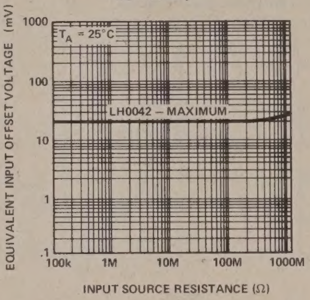
INPUT BIAS CURRENT VS TEMPERATURE



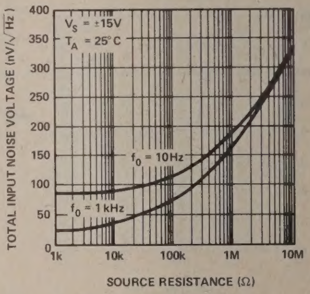
INPUT OFFSET VOLTAGE VS TEMPERATURE



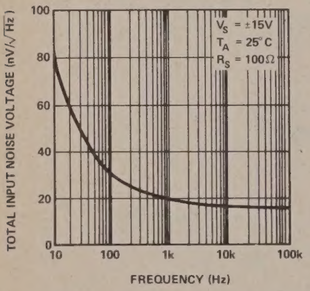
OFFSET ERROR (WITHOUT VOS NULL)



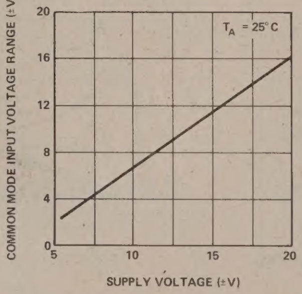
TOTAL INPUT NOISE VOLTAGE* VS SOURCE RESISTANCE



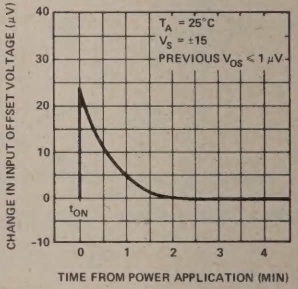
TOTAL INPUT NOISE VOLTAGE* VS FREQUENCY



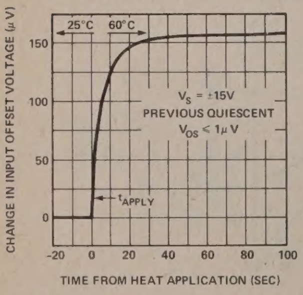
COMMON MODE INPUT VOLTAGE VS SUPPLY VOLTAGE



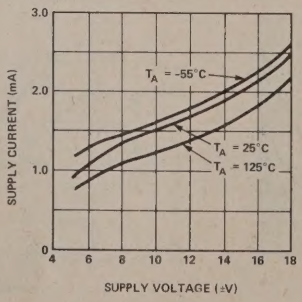
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



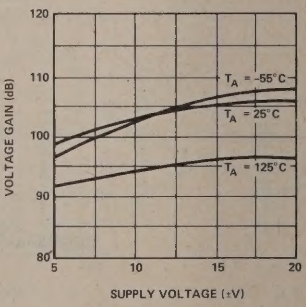
CHANGE IN INPUT OFFSET VOLTAGE DUE TO THERMAL SHOCK VS TIME



SUPPLY VOLTAGE VS SUPPLY CURRENT



VOLTAGE GAIN



*NOISE VOLTAGE INCLUDES CONTRIBUTION FROM SOURCE RESISTANCE.

INTERSIL

LM100, LM300
Voltage Regulator

FEATURES

- Output voltage adjustable from 2V to 30V
- One percent load and line regulation
- One percent stability over full military temperature range
- Adjustable short circuit current limiting
- Output currents in excess of 5A possible by adding external transistors
- Can be used as either a linear or high-efficiency switching regulator

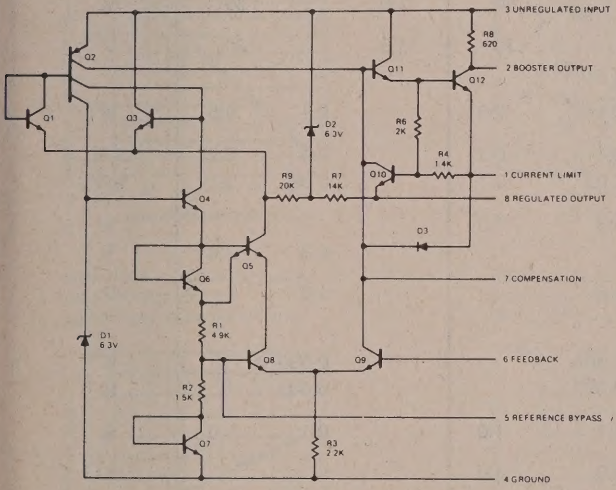
GENERAL DESCRIPTION

The Intersil 100/300 monolithic integrated circuit is a voltage regulator. It is designed for use in applications that range from digital power supplies to precision regulators.

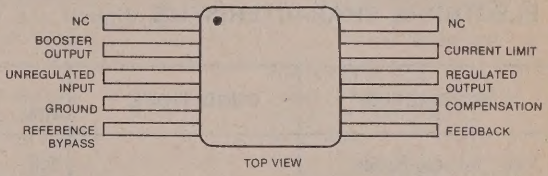
The output voltage is adjustable from 2V to 30V with a 1% load and line regulation. Short circuit current limiting is also adjustable. By adding external transistors, output currents in excess of 5A are possible.

The device can be used as either a linear or high-efficiency switching regulator, and will start on any load within rating. It responds quickly to both load and line transients and features small standby power dissipation, and freedom from oscillations with varying resistive and reactive loads.

SCHEMATIC DIAGRAM

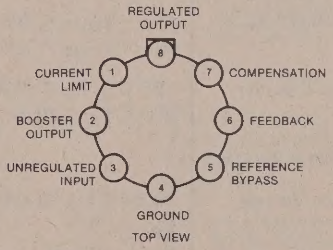

3 UNREGULATED INPUT
R8
620
Q2
Q11
2 BOOSTER OUTPUT
Q12
Q1
Q3
D2
6.3V
R6
2K
R4
1.4K
R9
20K
R7
14K
Q10
1 CURRENT LIMIT
8 REGULATED OUTPUT
Q4
D3
Q6
Q5
7 COMPENSATION
D1
6.3V
R1
4.9K
Q8
Q9
6 FEEDBACK
R2
1.5K
5 REFERENCE BYPASS
Q7
R3
2.2K
4 GROUND

PIN CONFIGURATIONS


NC
BOOSTER OUTPUT
UNREGULATED INPUT
GROUND
REFERENCE BYPASS
NC
CURRENT LIMIT
REGULATED OUTPUT
COMPENSATION
FEEDBACK
TOP VIEW

(outline dwg FB)

NOTE: Pin 4 connected to bottom of package.


REGULATED OUTPUT
8
CURRENT LIMIT
1
COMPENSATION
7
BOOSTER OUTPUT
2
FEEDBACK
6
UNREGULATED INPUT
3
REFERENCE BYPASS
5
4
GROUND
TOP VIEW

(outline dwg TO-99)

NOTE: Pin 4 connected to case.

ORDERING INFORMATION

Part number	To 99 Can	10-Pin Flatpak	Dice
LM100	LM100H*	LM100F	LM100/D
LM300	LM300H		LM300/D

* Add /883B to order if 883B processing is desired.

ABSOLUTE MAXIMUM RATINGS

	LM100	LM300
Input Voltage	40V	35V
Input-Output Voltage Differential	40V	30V
Power Dissipation (Note 1)	500 mW	300 mW
Operating Junction Temperature Range	-55°C to +150°C	0°C to 70°C
Storage Temperature Range	-65°C to +150°C	-55°C to 125°C
Lead Temperature (Soldering, 60 sec)	300°C	260°C

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	LM100			LM300			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range		8.5		40	8.0		30	V
Output Voltage Range		2.0		30	2.0		20	V
Output-Input Voltage Differential		3.0		30	3.0		20	V
Load Regulation (Note 3)	$R_{SC} = 0$, $I_O < 12$ mA		0.1	0.5		0.1	0.5	%
Line Regulation	$V_{IN} - V_{OUT} \leq 5V$		0.1	0.2		0.1	0.2	%/V
	$V_{IN} - V_{OUT} > 5V$		0.05	0.1		0.05	0.1	%/V
Temperature Stability	$-55°C \leq T_A \leq +125°C$		0.3	1.0				%
	$0°C \leq T_A \leq 70°C$					0.3	2.0	%
Feedback Sense Voltage			1.8			1.8		V
Output Noise Voltage	$10\text{ Hz} \leq f \leq 10\text{ kHz}$							
	$C_{REF} = 0$		0.005			0.005		%
	$C_{REF} = 0.1\ \mu F$		0.002			0.002		%
Long Term Stability			0.1	1.0		0.1	1.0	%
Standby Current Drain	$V_{IN} = 40V$		1.0	3.0				mA
	$V_{IN} = 30V$					1.0	3.0	mA
Minimum Load Current	$V_{IN} - V_{OUT} = 30V$		1.5	3.0				mA
	$V_{IN} - V_{OUT} = 20V$					1.5	3.0	mA

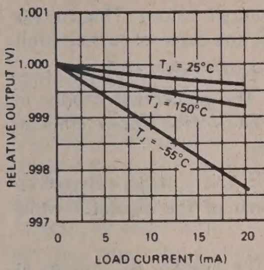
NOTE 1: The maximum junction temperature of the 100 is 150°C, while that of the 300 is 100°C. For operating at elevated temperatures devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the flat package, the derating is based on thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power averaged over a five second interval.

NOTE 2: These specifications apply for a junction temperature between -55°C and +150°C, (100) 0°C and 70°C, (300) for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

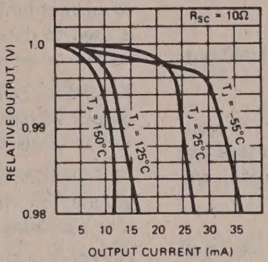
NOTE 3: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

TYPICAL PERFORMANCE CHARACTERISTICS FOR 100, 300*

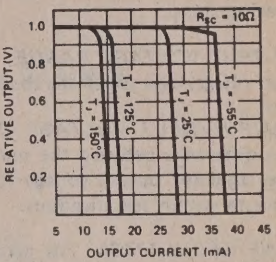
REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



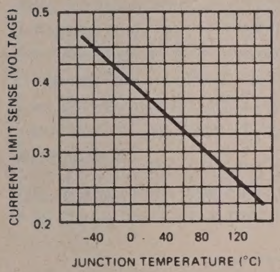
REGULATION CHARACTERISTICS WITH CURRENT LIMITING



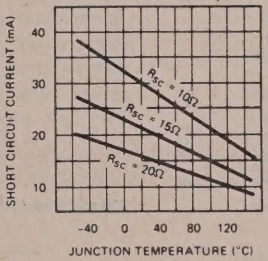
CURRENT LIMITING CHARACTERISTICS



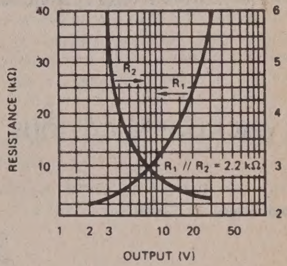
CURRENT LIMIT SENSE VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



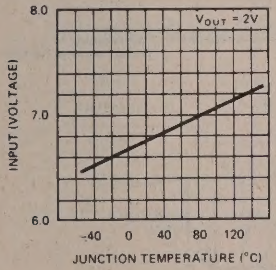
SHORT CIRCUIT CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



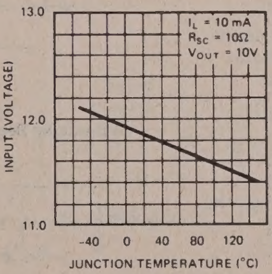
OPTIMUM DIVIDER RESISTANCE VALUES AS A FUNCTION OF OUTPUT VOLTAGE



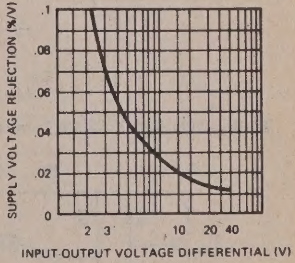
MINIMUM INPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



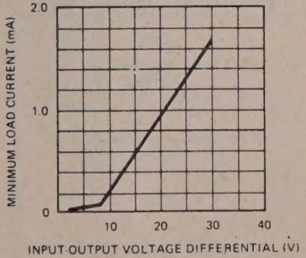
REGULATOR DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



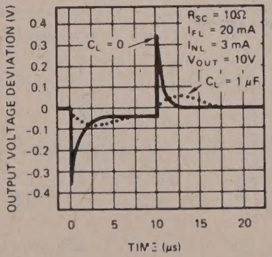
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



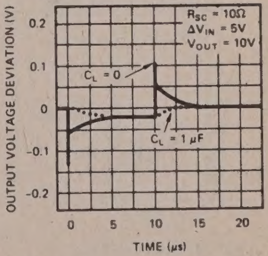
MINIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



*300 Only Guaranteed $0°C \leq T_A \leq 70°C$

DEFINITION OF TERMS

INPUT VOLTAGE RANGE: The range of DC input voltages over which the regulator will operate within specifications.

OUTPUT VOLTAGE RANGE: The range of regulated output voltages over which the specifications apply.

OUTPUT-INPUT VOLTAGE DIFFERENTIAL: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

LINE REGULATION: The percentage change in regulated output voltage for a change in input voltage.

LOAD REGULATION: The percentage change in regulated output voltage for a change in load from the minimum load to the maximum load current specified.

CURRENT-LIMIT SENSE VOLTAGE: The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

TEMPERATURE STABILITY: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

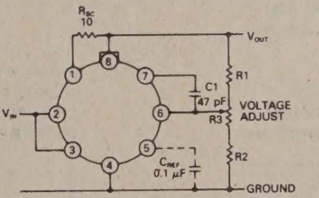
FEEDBACK SENSE VOLTAGE: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

OUTPUT NOISE VOLTAGE: The average AC voltage at the output with constant load and no input ripple.

STANDBY CURRENT DRAIN: That part of the operating current of the regulator which does not contribute to the load current.

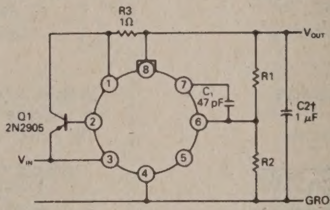
TYPICAL APPLICATIONS

Basic Regulator Circuit


R_{SC}
10
V_{OUT}
R1
C1
47 pF
VOLTAGE ADJUST
R3
V_{IN}
R2
C_{REF}
0.1 μF
GROUND
1
2
3
4
5
6
7
8

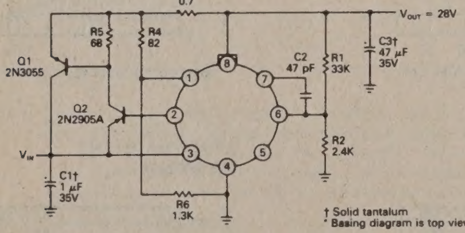
* Basing diagram is Top View

200 mA Regulator


R3
1Ω
V_{OUT}
R1
C2†
1 μF
C_1
47 pF
Q1
2N2905
V_{IN}
R2
GROUND
1
2
3
4
5
6
7
8

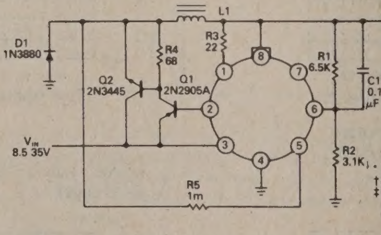
† Solid Tantalum
* Basing diagram is Top View

2A Regulator With Foldback Current Limiting


R3
0.7
V_{OUT} = 28V
R5
68
R4
82
Q1
2N3055
C2
47 pF
R1
33K
C3†
47 μF
35V
Q2
2N2905A
V_{IN}
R2
2.4K
C1†
1 μF
35V
R6
1.3K
1
2
3
4
5
6
7
8

† Solid tantalum
* Basing diagram is top view

4A Switching Regulator


L1
V_{OUT} = 5V
D1
1N3880
R4
68
R3
22
R1
6.5K
C2†
100 μF
35V
Q2
2N3445
Q1
2N2905A
C1
0.1 μF
V_{IN}
8.5 35V
R2
3.1K
R5
1m
1
2
3
4
5
6
7
8

* Basing diagram is top view
† Solid tantalum
‡ 60 turns = 20 on Arnold Engineering A930157.2 molybdenum permalloy core

INTERSIL

LM101A/301A
General Purpose Operational Amplifier

GENERAL DESCRIPTION

The Intersil 101A and 301A are general purpose operational amplifiers. These high performance op amps are improved versions of the standard 101/301.

This general purpose op amp has many outstanding features; overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations. The 101A also features better accuracy and lower noise in high impedance circuitry, and low input currents. Frequency compensation is achieved with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

The Intersil 101A operates over a temperature range from −55°C to +125°C while that of the 301A is 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	101A	±22V
	301A	±18V
Power Dissipation (Note 1)		500 mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short-Circuit Duration		Indefinite
Operating Temperature Range	101A	−55°C to 125°C
	301A	0°C to 70°C
Storage Temperature Range		-65°C to 150°C
Lead Temperature (Soldering, 60 sec)		300°C

NOTE 1: The maximum junction temperature of the 101A is 150°C, while that of the 301A is 100°C. For operating at elevated temperatures devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the flat package, the derating is based on thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

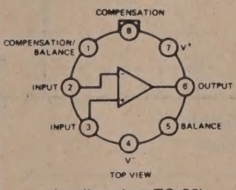
ORDERING INFORMATION

Part Number	8 lead TO-99	8 pin Plastic DIP	10 lead Flatpak	14 pin CER DIP	14 pin Plastic DIP	Dice
101A	LM101AH*		LM101AF*	LM101AJ-14		LM101A/D
301A	LM301AH	LM301AN	LM301AF	LM301AJ	LM301AN-14	LM301A/D

* Add/883B to ordering number if 883B processing is desired.

PIN CONFIGURATIONS

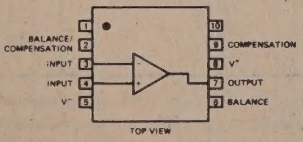
TO-5


COMPENSATION
COMPENSATION/ BALANCE
V+
INPUT
OUTPUT
INPUT
BALANCE
V−
1
2
3
4
5
6
7
8
TOP VIEW

(outline dwg TO-99)

NOTE: Pin 4 connected to case.

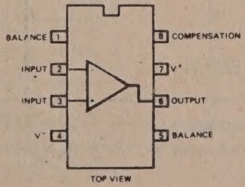
Flat Package


BALANCE/ COMPENSATION
INPUT
INPUT
V−
COMPENSATION
V+
OUTPUT
BALANCE
1
2
3
4
5
6
7
8
9
10
TOP VIEW

(outline dwg FB)

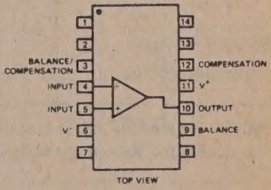
NOTE: Pin 5 connected to bottom of package.

8 Pin Plastic DIP


BALANCE
INPUT
INPUT
V−
COMPENSATION
V+
OUTPUT
BALANCE
1
2
3
4
5
6
7
8
TOP VIEW

(outline dwg PA)

14 Pin DIP


BALANCE/ COMPENSATION
INPUT
INPUT
V−
COMPENSATION
V+
OUTPUT
BALANCE
1
2
3
4
5
6
7
8
9
10
11
12
13
14
TOP VIEW

(outline dwgs JD, PD)

NOTE: Pin 6 connected to bottom of package.

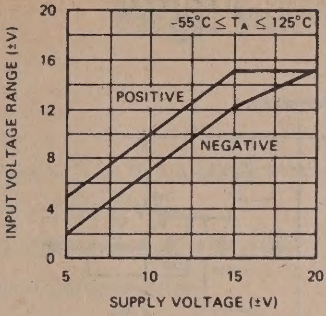
ELECTRICAL CHARACTERISTICS (Note)

PARAMETER	CONDITIONS	101A			301A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\ k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3	50	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4		0.5	2		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$		1.8	3.0				mA
	$T_A = 25°C$, $V_S = \pm 15V$					1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	µV/°C
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$		0.01	0.1				nA/°C
	$25°C \leq T_A \leq 70°C$					0.01	0.3	nA/°C
	$-55°C \leq T_A \leq 25°C$		0.02	0.2				nA/°C
	$0°C \leq T_A \leq 25°C$					0.02	0.6	nA/°C
Input Bias Current				100			300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 20V$	±15			±12			V
	$V_S = \pm 15V$							V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	96		dB

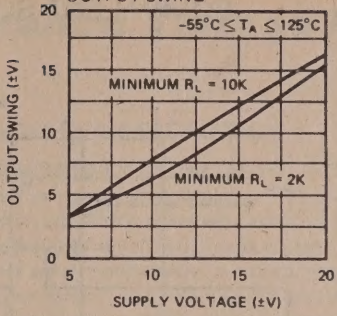
NOTE: For the 101A, these specifications apply for $\pm 5V < V_S < \pm 20V$ and $-55°C \leq T_A \leq 125°C$ unless otherwise specified.
For the 301A, these specifications apply for $\pm 5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified.

GUARANTEED PERFORMANCE *

INPUT VOLTAGE RANGE

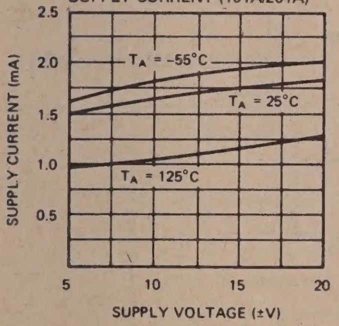


OUTPUT SWING

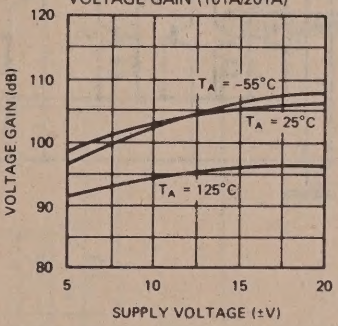


TYPICAL PERFORMANCE *

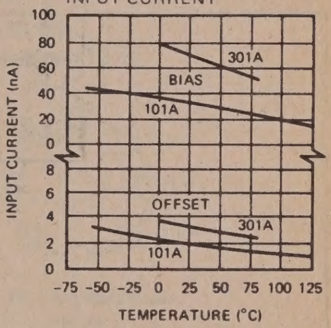
SUPPLY CURRENT (101A/201A)



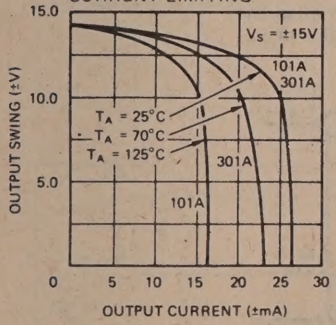
VOLTAGE GAIN (101A/201A)



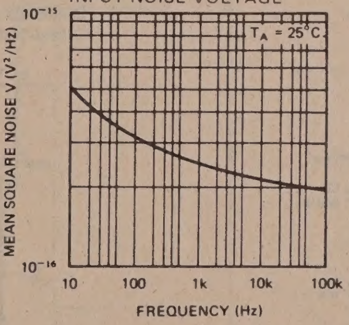
INPUT CURRENT



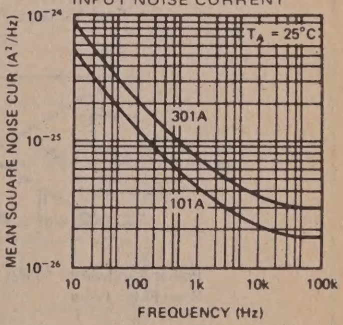
CURRENT LIMITING



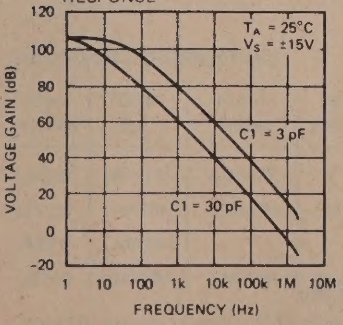
INPUT NOISE VOLTAGE



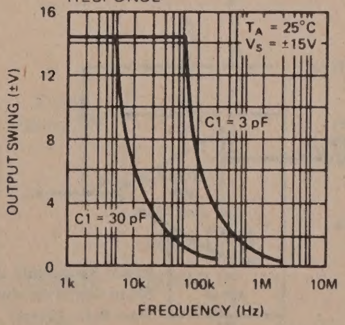
INPUT NOISE CURRENT



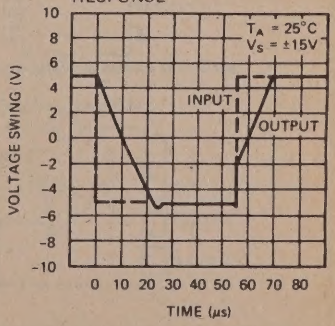
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

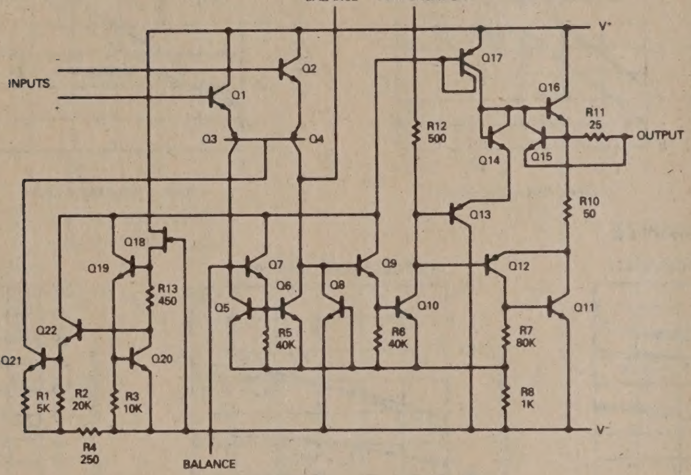


VOLTAGE FOLLOWER PULSE RESPONSE



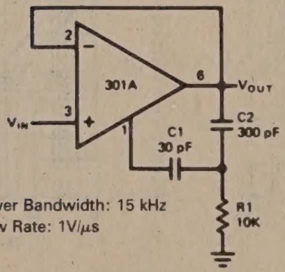
*301A only guaranteed to ±15V, 0°C ≤ T_A ≤ 70°C.

EQUIVALENT SCHEMATIC DIAGRAM


BALANCE
COMPENSATION
V+
INPUTS
Q1
Q2
Q3
Q4
Q17
Q16
R11
25
OUTPUT
R12
500
Q14
Q15
R10
50
Q13
Q18
Q19
R13
450
Q7
Q6
Q8
Q9
Q12
Q5
Q10
Q11
R5
40K
R6
40K
R7
80K
Q22
Q21
Q20
R1
5K
R2
20K
R3
10K
R8
1K
V−
R4
250
BALANCE

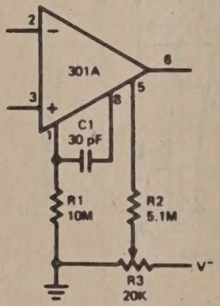
TYPICAL APPLICATIONS

Fast Voltage Follower

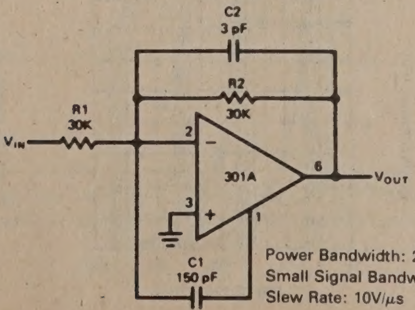

2
−
301A
6
VOUT
VIN
3
+
1
C1
30 pF
C2
300 pF
R1
10K

Power Bandwidth: 15 kHz
Slew Rate: 1V/μs

Standard Compensation and Offset Balancing Circuit


2
−
301A
6
3
+
5
8
1
C1
30 pF
R1
10M
R2
5.1M
R3
20K
V−

Fast Summing Amplifier


C2
3 pF
R2
30K
R1
30K
VIN
2
−
301A
6
VOUT
3
+
1
C1
150 pF

Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

LM102/302
LM110/310
High Performance Voltage Followers

FEATURES

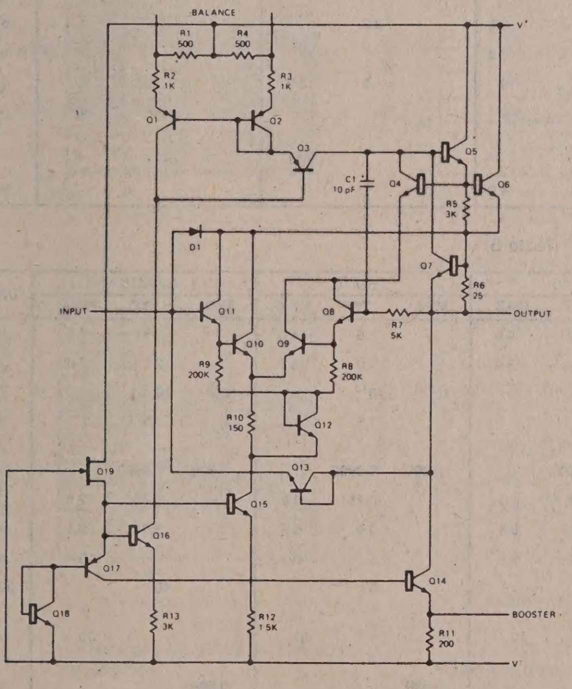
- Low Input Current — 7 to 30 nA Max
- High Slew Rate — 10 to 30 V/μs
- Wide Bandwidth — 20 MHz (LM110/LM310)
- Internal Frequency Compensation
- Interchangeable with 741 in Follower Applications

GENERAL DESCRIPTION

The LM102/LM302 and LM110/LM310 are monolithic high performance voltage followers. In buffer applications they offer substantial advantages compared with general purpose operational amplifiers: input current, bandwidth, and slew rate are all significantly improved. Applications include high speed sample and hold circuits, instrumentation amplifiers, active filters, as well as general purpose buffers.

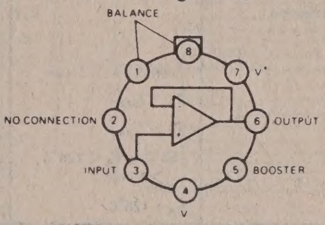
For new designs the LM110/LM310 is recommended.

EQUIVALENT CIRCUIT


BALANCE
R1 500
R4 500
V+
R2 1K
R3 1K
Q1
Q2
Q3
Q5
C1 10 pF
Q4
Q6
R5 3K
D1
Q7
R6 25
INPUT
Q11
Q8
R7 5K
OUTPUT
Q10
Q9
R9 200K
R8 200K
R10 150
Q12
Q19
Q13
Q15
Q16
Q17
Q14
Q18
R13 3K
R12 1.5K
R11 200
BOOSTER
V-

PIN CONFIGURATIONS

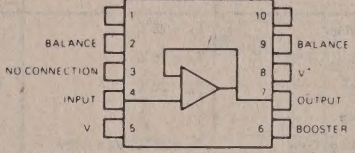
(outline dwg TO-99)


BALANCE
8
1
7
V+
NO CONNECTION
2
6
OUTPUT
INPUT
3
5
BOOSTER
4
V-

NOTE: Pin 4 connected to case

TOP VIEW

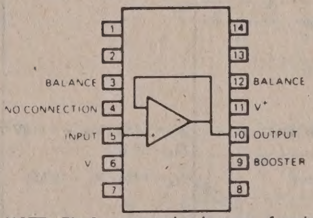
(outline dwg FB)


1
10
BALANCE
2
9
BALANCE
NO CONNECTION
3
8
V+
INPUT
4
7
OUTPUT
V-
5
6
BOOSTER

NOTE: Pin 5 connected to bottom of package

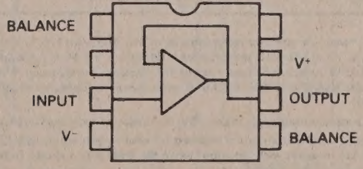
TOP VIEW

(outline dwg JD)


1
14
2
13
BALANCE
3
12
BALANCE
NO CONNECTION
4
11
V+
INPUT
5
10
OUTPUT
V-
6
9
BOOSTER
7
8

NOTE: Pin 6 connected to bottom of package

(outline dwg PA)


BALANCE
V+
INPUT
OUTPUT
V-
BALANCE

ORDERING INFORMATION

Part number	TO-99 Can	10 pin Flatpak	14 pin CER DIP	8 pin Plastic DIP	Dice
LM102	LM102H	LM102F			LM102/D
LM110	LM110H*	LM110F*	LM110J		LM110/D
LM302	LM302H				LM302/D
LM310	LM310H	LM310F	LM310J	LM310N	LM310/D

*Add/883B to order number if 883B processing is desired.

LM102, LM302, LM110, LM310

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite

Operating Temperature Range:	102, 110	−55°C to +125°C
	202, 210	−25°C to +85°C
	302, 310	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

ELECTRICAL CHARACTERISTICS 102/202/302 (Note 4)

PARAMETER	CONDITIONS	LM102			LM202			LM302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage			2	5		3	10		5	15	mV
Average Temperature Coefficient of Offset Voltage			6			15			20		μV/°C
Input Current			3	10		7	15		10	30	nA
Input Resistance		10^{10}	10^{12}		10^{10}	10^{12}		10^{9}	10^{12}		Ω
Voltage Gain	$R_L \geq 10$ kΩ	0.999	0.9996		0.999	0.9995	1.000	0.9985	0.9995	1.000	
Output Resistance			0.8	2.5		0.8	2.5		0.8	2.5	Ω
Output Voltage Swing (Note 6)	$R_L \geq 8$ kΩ	±10	±13		±10			±10			V
Supply Current			3.5	5.5		3.5	5.5		3.5	5.5	mA
Positive Supply Rejection		60			60			60			dB
Negative Supply Rejection		70			70			70			dB
Input Capacitance				3.0		3.0			3.0		pF
Offset Voltage	$T_{MIN} \leq T_A \leq T_{MAX}$			7.5			15			20	mV
Input Current	$T_A = T_{MAX}$		3	10		1.5	5.0		3.0	15	nA
	$T_A = T_{MIN}$		30	100		30	50		20	50	nA
Voltage Gain	$-55°C \leq T_A \leq 125°C$ $R_L \geq 10$ kΩ	0.999									
Supply Current	$T_A = 125°C$		2.6	4.0							mA

ELECTRICAL CHARACTERISTICS 110/210/310 (Note 5)

PARAMETER	CONDITIONS	LM110			LM210			LM310			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$		1.5	4.0		1.5	4.0		2.5	7.5	mV
Input Bias Current	$T_A = 25°C$		1.0	3.0		1.0	3.0		2.0	7.0	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Capacitance			1.5			1.5			1.5		pF
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L = 8$ kΩ	0.999	0.9999		0.999	0.9999		0.999	0.9999		V/V
Output Resistance	$T_A = 25°C$		0.75	2.5		0.75	2.5		0.75	2.5	Ω
Supply Current	$T_A = 25°C$		3.9	5.5		3.9	5.5		3.9	5.5	mA
Input Offset Voltage				6.0			6.0			10	mV
Offset Voltage Temperature Drift			10			10			10		μV/°C
Input Bias Current				10			10			10	nA
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L = 10$ kΩ	0.999			0.999			0.999			V/V
Output Voltage Swing (Note 6)	$V_S = \pm15V$, $R_L = 10$ kΩ	±10			±10			±10			V
Supply Current	$T_A = T_{MAX}$		2.0	4.0		2.0	4.0				mA
Supply Voltage Rejection Ratio	$\pm5V \leq V_S \leq \pm18V$	70	80		70	80		70	80		dB

NOTE 1: The maximum junction temperature of the 102 and 110 is 150°C, that of the 202 and 210 is 100°C, while that of the 302 and 310 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 3: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.

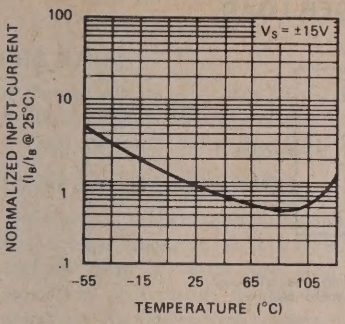
NOTE 4: These specifications apply for $T_A = 25°C$, $V_S = \pm15V$ and $C_L \leq 100$ pF unless otherwise noted.

NOTE 5: These specifications apply for $\pm5V \leq V_S \leq \pm18V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the 210, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$, while for the 310 the limits are $0°C \leq T_A \leq 70°C$.

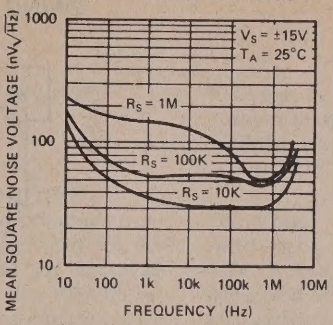
NOTE 6: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

TYPICAL PERFORMANCE

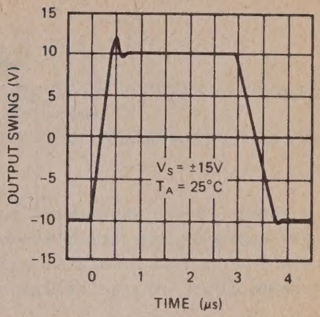
NORMALIZED INPUT CURRENT



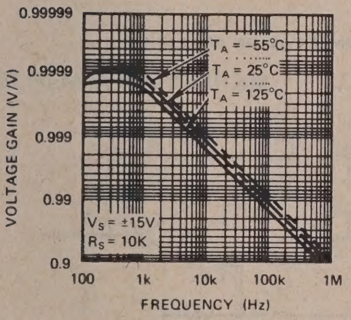
OUTPUT NOISE VOLTAGE



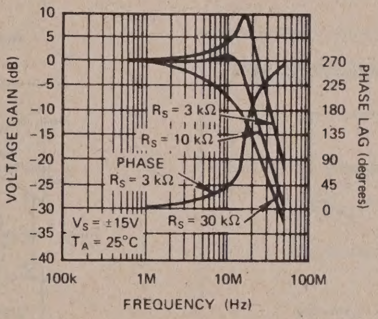
LARGE SIGNAL PULSE RESPONSE



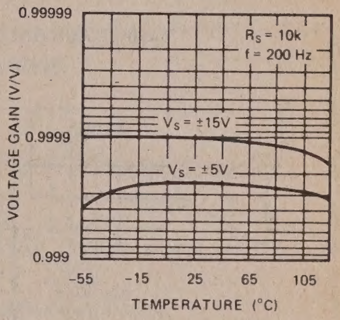
VOLTAGE GAIN



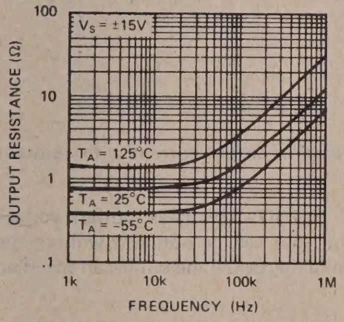
VOLTAGE GAIN*



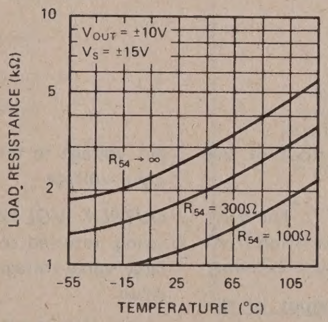
VOLTAGE GAIN



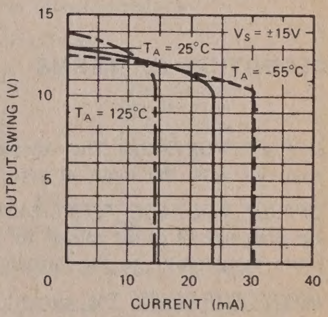
OUTPUT RESISTANCE



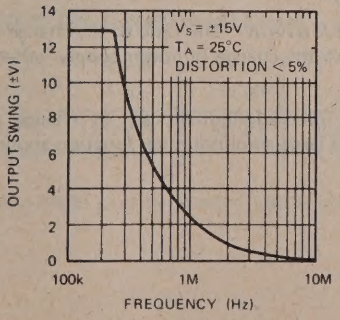
SYMMETRICAL OUTPUT SWING



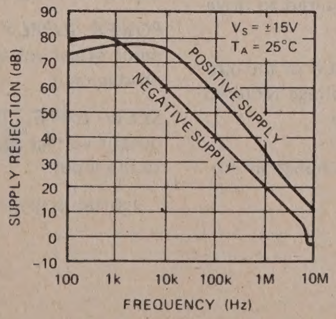
POSITIVE OUTPUT SWING



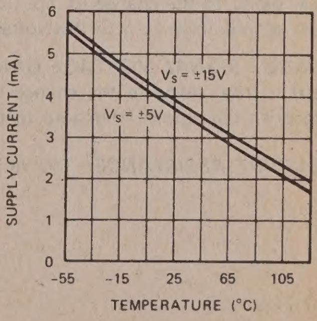
LARGE SIGNAL FREQUENCY RESPONSE



POWER SUPPLY REJECTION

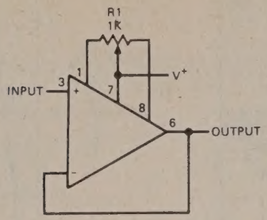


SUPPLY CURRENT

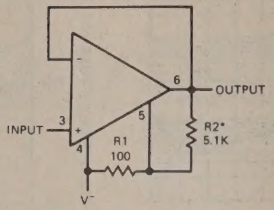


*Note that optimum stability is obtained for a source resistance of 10 kΩ. For source resistances lower than 10 kΩ, it is advisable to put additional resistance in series with the input to ensure adequate stability margin.

OFFSET BALANCING


R1
1K
V+
INPUT
3
1
7
8
6
OUTPUT

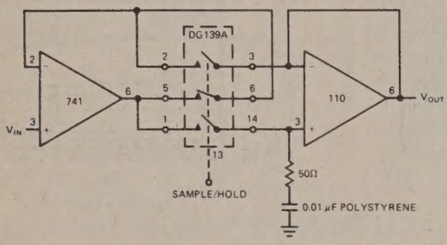
INCREASING NEGATIVE SWING UNDER LOAD


6
OUTPUT
5
INPUT
3
4
R1
100
R2*
5.1K
V−

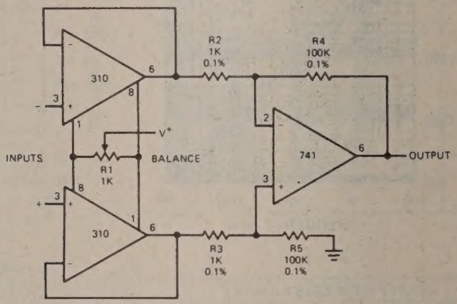
*May be added to reduce internal dissipation.

APPLICATIONS

SAMPLE AND HOLD


DG139A
2
3
5
6
1
14
13
741
110
VIN
VOUT
SAMPLE/HOLD
50Ω
0.01 μF POLYSTYRENE

INSTRUMENTATION AMPLIFIER


R2
1K
0.1%
R4
100K
0.1%
310
6
8
3
1
V+
INPUTS
BALANCE
R1
1K
741
OUTPUT
2
3
R3
1K
0.1%
R5
100K
0.1%

DEFINITION OF TERMS

OFFSET VOLTAGE: The voltage at the output of the amplifier with the input at zero.

OFFSET VOLTAGE TEMPERATURE DRIFT: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

INPUT CURRENT: The current into the input of the amplifier with the input at zero.

INPUT RESISTANCE: The ratio of the rated output voltage swing to the change in input current required to drive the output from zero to this voltage.

LARGE SIGNAL VOLTAGE GAIN: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE: The ratio of the change in output voltage to the change in output current with constant input voltage.

OUTPUT VOLTAGE SWING: The peak output voltage swing, referred to zero, that can be obtained without the large-signal voltage gain falling below the minimum specified value.

SUPPLY CURRENT: The current required from the power supply to operate the amplifier, with no load, anywhere within its linear range.

POWER SUPPLY REJECTION: The ratio of the change in input offset voltage to the change in power supply voltage producing it.

SLEW RATE: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

LM105, LM305
Voltage Regulator

FEATURES

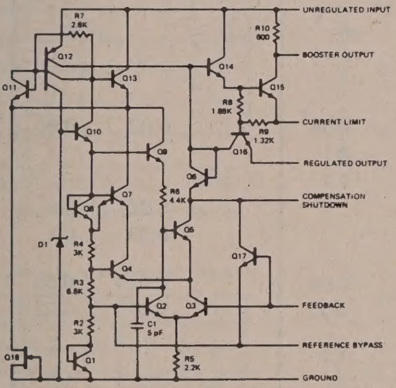
- Output voltage adjustable from 4.5V to 40V (105)
- DC line regulation guaranteed at 0.03%/V
- Load regulation better than 0.1%
- Output current in excess of 10A possible by adding external resistor
- Direct, plug-in replacement for 100/300 giving improved regulation

GENERAL DESCRIPTION

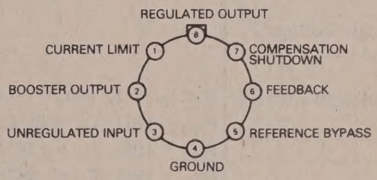
The Intersil 105/305 monolithic integrated circuit is a positive voltage regulator. It is a direct replacement for the 100/300 with an extra gain stage added for improved regulation. In contrast to the 100/300, the 105/305 requires no minimum load current while permitting higher voltage operation by reducing standby current drain.

The Intersil 105/305 can be used as either a linear or switching regulator circuit with output voltages greater than 4.5V. It features fast response to both load and line transients, and freedom from oscillations with varying resistive and reactive loads.

SCHEMATIC DIAGRAM


UNREGULATED INPUT
R7
2.8K
R10
600
BOOSTER OUTPUT
Q12
Q14
Q11
Q13
Q15
R8
1.86K
CURRENT LIMIT
Q10
R9
1.32K
Q9
Q16
REGULATED OUTPUT
Q6
Q7
R6
4.4K
COMPENSATION
SHUTDOWN
Q8
Q5
D1
R4
3K
Q17
Q4
R3
6.8K
Q2
Q3
FEEDBACK
C1
5 pF
R2
3K
REFERENCE BYPASS
Q18
Q1
R5
2.2K
GROUND

PIN CONFIGURATIONS

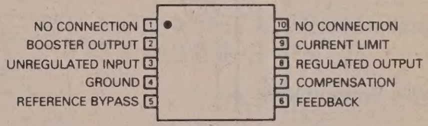

REGULATED OUTPUT
8
CURRENT LIMIT
1
7
COMPENSATION
SHUTDOWN
BOOSTER OUTPUT
2
6
FEEDBACK
UNREGULATED INPUT
3
5
REFERENCE BYPASS
4
GROUND

(outline dwg TO-99)

TOP VIEW

NOTE: Pin 4 connected to case

Flat Package


NO CONNECTION
1
BOOSTER OUTPUT
2
UNREGULATED INPUT
3
GROUND
4
REFERENCE BYPASS
5
10
NO CONNECTION
9
CURRENT LIMIT
8
REGULATED OUTPUT
7
COMPENSATION
6
FEEDBACK

TOP VIEW

(outline dwg FB)

NOTE: Pin 4 connected to bottom of package

ORDERING INFORMATION

Part number	TO-99 Can	10 pin Flatpak	Dice
LM105	LM105H*	LM105F	LM105/D
LM305	LM305H		LM305/D

* Add /883B to order number if 883B processing is desired.

ABSOLUTE MAXIMUM RATINGS

	105	305
Input Voltage	50V	40V
Input-Output Voltage Differential	40V	40V
Power Dissipation (Note 1)	500 mW	500 mW
Operating Junction Temperature Range	−55°C to +150°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−55°C to 125°C
Lead Temperature (Soldering, 60 sec)	300°C	300°C

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	105 MIN	105 TYP	105 MAX	305 MIN	305 TYP	305 MAX	UNITS
Input Voltage Range		8.5		50	8.0		40	V
Output Voltage Range		4.5		40	4.5		30	V
Output-Input Voltage Differential		3.0		30	3.0		30	V
Load Regulation (Note 3)	$0 \leq I_O < 12$ mA							
	$R_{SC} = 18\Omega$, $T_A = 25°C$		0.02	0.05		0.02	0.05	%
	$R_{SC} = 10\Omega$, $T_A = 125°C$		0.03	0.1				%
	$R_{SC} = 18\Omega$, $T_A = -55°C$		0.03	0.1				%
	$R_{SC} = 15\Omega$, $T_A = 70°C$					0.03	0.1	%
	$R_{SC} = 18\Omega$, $T_A = 0°C$					0.03	0.1	%
Line Regulation	$V_{IN} - V_{OUT} \leq 5V$		0.025	0.06		0.025	0.06	%/V
	$V_{IN} - V_{OUT} > 5V$		0.015	0.03		0.05	0.03	%/V
Temperature Stability	$-55°C \leq T_A \leq +125°C$		0.3	1.0				%
	$0°C \leq T_A \leq 70°C$					0.3	1.0	%
Feedback Sense Voltage			1.8			1.8		V
Output Noise Voltage	$10\text{ Hz} \leq f \leq 10\text{ kHz}$							
	$C_{REF} = 0$		0.005			0.005		%
	$C_{REF} = 0.1\ \mu F$		0.002			0.002		%
Long Term Stability			0.1	1.0		0.1	1.0	%
Standby Current Drain	$V_{IN} = 50V$		0.8	2.0				mA
	$V_{IN} = 40V$					0.8	2.0	mA
Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 120 Hz		0.003	0.01		0.003	0.01	%/V

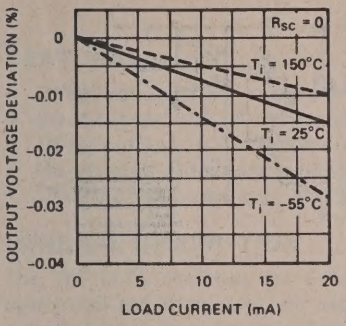
NOTE 1: The maximum junction temperature of the 105 is 150°C, while that of the 305 is 85°C. For operating at elevated temperatures devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the flat package, the derating is based on thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power averaged over a five second interval.

NOTE 2: These specifications apply for a junction temperature between −55°C and +150°C, (105) 0°C and 70°C, (305) for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

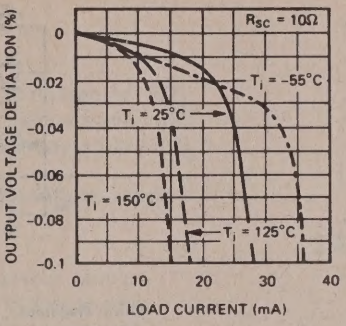
NOTE 3: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

TYPICAL PERFORMANCE CHARACTERISTICS FOR 105,305*

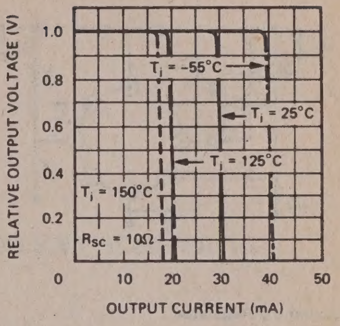
LOAD REGULATION



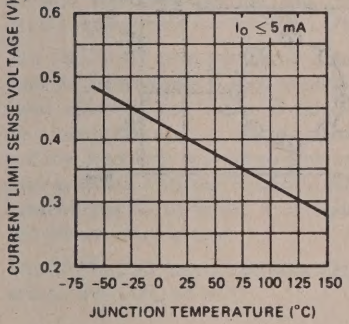
LOAD REGULATION



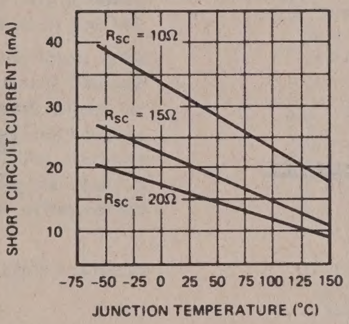
CURRENT LIMITING CHARACTERISTICS



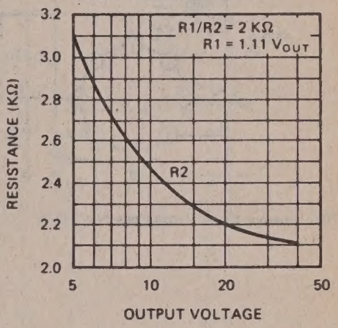
CURRENT LIMIT SENSE VOLTAGE



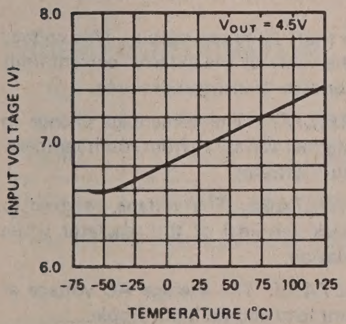
SHORT CIRCUIT CURRENT



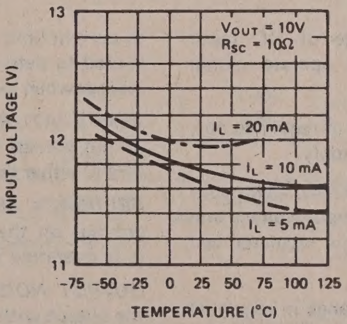
OPTIMUM DIVIDER RESISTANCE VALUES



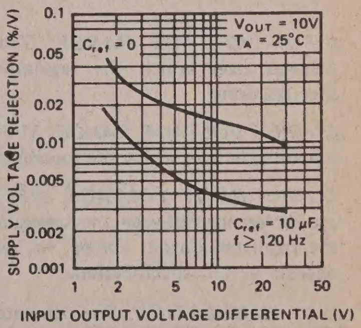
MINIMUM INPUT VOLTAGE



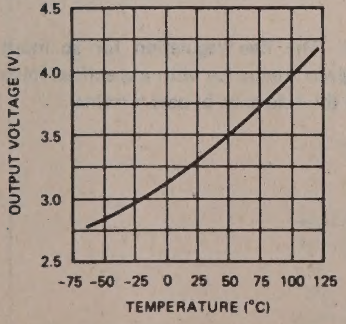
REGULATOR DROPOUT VOLTAGE



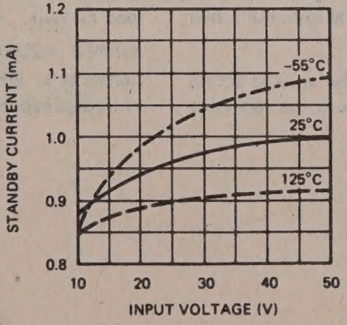
SUPPLY VOLTAGE REJECTION



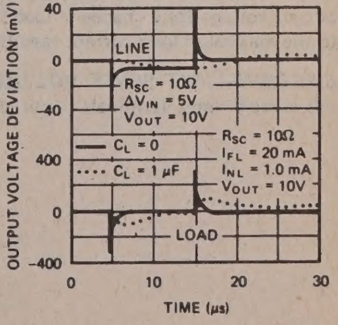
MINIMUM OUTPUT VOLTAGE



STANDBY CURRENT DRAIN



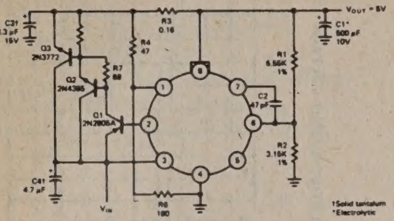
TRANSIENT RESPONSE



*305 only guaranteed 0°C ≤ T_A ≤ 70°C, V_{IN} = 40V max, V_{OUT} = 30V max.

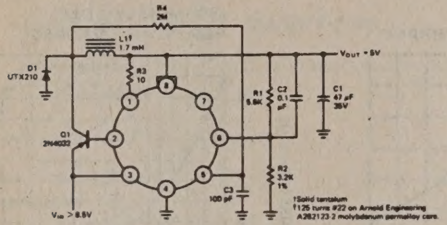
TYPICAL APPLICATIONS*

10A Regulator with Foldback Current Limiting


C3†
3.3 μF
15V
Q3
2N3772
Q2
2N4385
R7
68
Q1
2N2905A
C4†
4.7 μF
V_{in}
R4
47
R3
0.16
R6
180
V_{OUT} = 5V
C1*
500 μF
10V
R1
6.56K
1%
C2
47 pF
R2
3.16K
1%
1
2
3
4
5
6
7
8

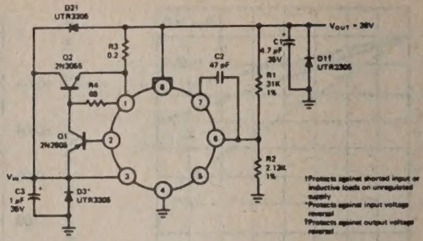
†Solid tantalum
*Electrolytic

Switching Regulator


R4
2M
L1†
1.7 mH
D1
UTX210
R3
10
Q1
2N4032
V_{in} > 8.5V
V_{OUT} = 5V
R1
5.6K
C2
0.1 μF
C1
47 μF
35V
C3
100 pF
R2
3.2K
1%
1
2
3
4
5
6
7
8

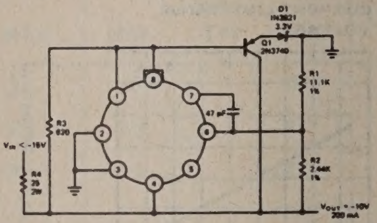
†Solid tantalum
†125 turns #22 on Arnold Engineering A262123-2 molybdenum permalloy core.

1.0A Regulator with Protective Diodes


D2†
UTR3305
R3
0.2
Q2
2N3055
R4
68
Q1
2N2905
V_{in}
C3
1 μF
35V
D3*
UTR3305
C2
47 pF
C1
4.7 μF
35V
D1†
UTR3305
V_{OUT} = 28V
R1
31K
1%
R2
2.13K
1%
1
2
3
4
5
6
7
8

†Protects against shorted input or inductive loads on unregulated supply
*Protects against input voltage reversal
†Protects against output voltage reversal

Shunt Regulator


D1
1N3821
3.3V
Q1
2N3740
R1
11.1K
1%
47 pF
R3
620
V_{in} < -15V
R4
25
2W
R2
2.44K
1%
V_{OUT} = -10V
200 mA
1
2
3
4
5
6
7
8

*Pin connections shown are for TO-5

DEFINITION OF TERMS

INPUT VOLTAGE RANGE: The range of DC input voltages over which the regulator will operate within specifications.

OUTPUT VOLTAGE RANGE: The range of regulated output voltages over which the specifications apply.

OUTPUT-INPUT VOLTAGE DIFFERENTIAL: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

LINE REGULATION: The percentage change in regulated output voltage for a change in input voltage.

LOAD REGULATION: The percentage change in regulated output voltage for a change in load from the minimum load to the maximum load current specified.

CURRENT-LIMIT SENSE VOLTAGE: The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

TEMPERATURE STABILITY: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

FEEDBACK SENSE VOLTAGE: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

OUTPUT NOISE VOLTAGE: The average AC voltage at the output with constant load and no input ripple.

STANDBY CURRENT DRAIN: That part of the operating current of the regulator which does not contribute to the load current.

RIPPLE REJECTION: The line regulation for ac input signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal.

INTERSIL

LM107, LM307
Operational Amplifiers

FEATURES

- Offset voltage 3 mV maximum over temperature (107)
- Input current 100 nA maximum over temperature (107)
- Offset current 20 nA maximum over temperature (107)
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode range

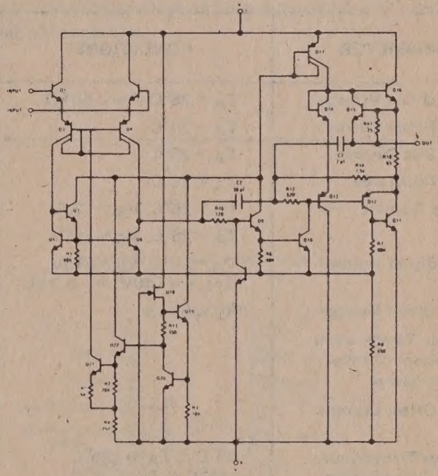
GENERAL DESCRIPTION

The 107 series amplifiers are complete, general purpose operational amplifiers, with the necessary frequency compensation built into the chip. Advanced processing techniques make the input currents a factor of ten lower than industry standards like the 709. Yet, they are a direct, plug-in replacement for the 709, LM101, LM101A and 741.

The 107 series provides better accuracy and lower noise than its predecessors in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators of timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at reduced cost.

The 307 has somewhat different specifications, and operates from 0°C to 70°C.

EQUIVALENT SCHEMATIC

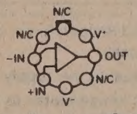


ORDERING INFORMATION

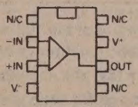
Part number	TO-99 Can	10 pin Flatpak	14 pin CERDIP	8 pin DIP	Dice
LM107	LM107H*	LM107F*	LM107J-14*		LM107/D
LM307	LM307H	LM307F	LM307J-14	LM307N	LM307/D

* Add /883B to ordering number if 883B processing desired.

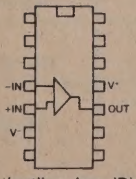
PIN CONFIGURATIONS



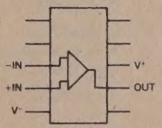
(outline dwg TO-99)



(outline dwg PA)



(outline dwg JD)



(outline dwg FB)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 107,	±22V
307	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite

Operating Temperature Range	107	−55°C to 125°C
	307	0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 60 sec)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	107 MIN	107 TYP	107 MAX	307 MIN	307 TYP	307 MAX	UNITS
Input Offset Voltage	T_A = 25°C, R_S ≤ 50 kΩ		0.7	2.0		2.0	7.5	mV
Input Offset Current	T_A = 25°C		1.5	10		3	50	nA
Input Bias Current	T_A = 25°C		30	75		70	250	nA
Input Resistance	T_A = 25°C	1.5	4		0.5	2		MΩ
Supply Current	T_A = 25°C, V_S = ±20V		1.8	3.0				mA
	T_A = 25°C, V_S = ±15V					1.8	3.0	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, R_L ≥ 2 kΩ	50	160		25	160		V/mV
Input Offset Voltage	R_S ≤ 50 kΩ			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	µV/°C
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	25°C ≤ T_A ≤ 125°C		0.01	0.1				nA/°C
	−55°C ≤ T_A ≤ 25°C		0.02	0.2				nA/°C
	25°C ≤ T_A ≤ 70°C					0.01	0.3	nA/°C
	0°C ≤ T_A ≤ 25°C					0.02	0.6	nA/°C
Input Bias Current				100			300	mA
Supply Current	T_A = +125°C, V_S = ±20V		1.2	2.5				mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L ≥ 2 kΩ	25			15			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±14		±12	±14		V
	R_L = 2 kΩ	±10	±13		±10	±13		V
Input Voltage Range	V_S = ±20V	±15						V
	V_S = ±15V				±12			V
Common Mode Rejection Ratio	R_S ≤ 50 kΩ	80	96		70	90		dB
Supply Voltage Rejection Ratio	R_S ≤ 50 kΩ	80	96		70	96		dB

Note 1: The maximum junction temperature of the 107 is 150°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to 70°C and ambient temperatures to 55°C.

Note 4: These specifications apply for $\pm 5V < V_s < \pm 20V$ and $-55°C \le T_A \le 125°C$ for the 107, unless otherwise specified. For the 307, the specifications apply for $0°C \le T_A \le 70°C$ and $\pm 5V \le V_s \le \pm 15V$, unless otherwise specified.

INTERSIL

LM108/A, LM308/A
Low Level Operational Amplifiers

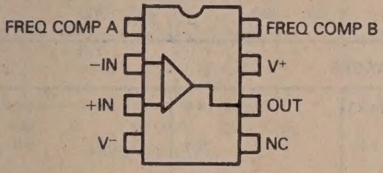
FEATURES

- Input Bias Current — 2 nA max to 7 nA max
- Input Offset Current — 0.2 nA max to 1 nA max
- Input Offset Voltage — 0.5 mV max to 7.5 mV max
- $\Delta V_{os}/\Delta T$ — 5 μV/°C to 30 μV/°C
- $\Delta I_{os}/\Delta T$ — 2.5 pA/°C to 10 pA/°C
- Pin for Pin Replacement for 101A/301A

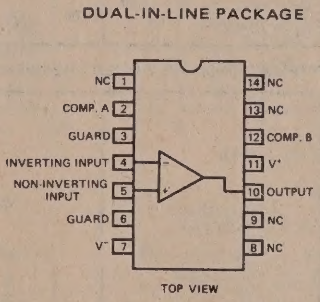
GENERAL DESCRIPTION

These differential input, precision amplifiers provide low input currents and offset voltages competitive with FET and chopper stabilized amplifiers. They feature low power consumption over a supply voltage range of >2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor. The LM108A and LM308A are high performance selections from the 108/308 amplifier family.

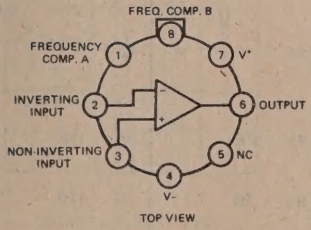
PIN CONFIGURATIONS


FREQ COMP A
−IN
+IN
V⁻
FREQ COMP B
V⁺
OUT
NC

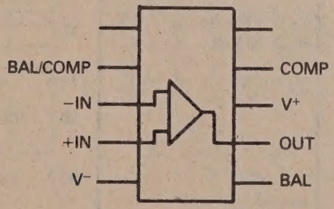
(outline dwg PA)


DUAL-IN-LINE PACKAGE
NC 1
COMP. A 2
GUARD 3
INVERTING INPUT 4
NON-INVERTING INPUT 5
GUARD 6
V⁻ 7
14 NC
13 NC
12 COMP. B
11 V⁺
10 OUTPUT
9 NC
8 NC
TOP VIEW

(outline dwg JD)


FREQ. COMP. B
8
FREQUENCY COMP. A
1
7
V⁺
INVERTING INPUT
2
6
OUTPUT
NON-INVERTING INPUT
3
5
NC
4
V⁻
TOP VIEW

(outline dwg TO-99)


BAL/COMP
−IN
+IN
V⁻
COMP
V⁺
OUT
BAL

(outline dwg FB-1)

ORDERING INFORMATION

Part number	TO-99 Can	8 pin MiniDIP	14 pin CERDIP	10 pin Flatpak	Dice
LM108A	LM108AH*		LM108AJ	LM108AF	LM108A/D
LM308A	LM308AH	LM308AN	LM308AJ	LM308AF	LM308A/D
LM108	LM108H*		LM108J	LM108F	LM108/D
LM308	LM308H	LM308N	LM308J	LM308F	LM308/D

*If 883B processing is desired add /883B to order number.

LM108/A, LM308/A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
108, 108A	±20V
308, 308A	±18V
Internal PowerDissipation (Note 1)	
Metal Can (TO-99	500 mW
DIP	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-CircuitDuration	Indefinite
Operating TemperatureRange	
108, 108A	−55°C to +125°C
308, 308A	0°C to +70°C
Storage TemperatureRange	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

PARAMETER	CONDITIONS	308			308A			108			108A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			2.0	7.5		0.3	0.5		0.7	2.0		0.3	0.5	mV
Input Offset Current			0.2	1.0		0.2	1.0		0.05	0.2		0.05	0.2	nA
Input Bias Current			1.5	7		1.5	7		0.8	2.0		0.8	2.0	nA
Input Resistance		10	40		10	40		30	70		30	70		MΩ
Supply Current	V_S = ±20V								0.3	0.6		0.3	0.6	mA
	V_S = ±15V		0.3	0.8		0.3	0.8							mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 10\ k\Omega$	25	300		80	300		50	300		80	300		V/mV
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES														
Input Offset Voltage				10			0.73			3.0			1.0	mV
Input Offset Current				1.5			1.5			0.4			0.4	nA
Average Temperature Coefficient of Input Offset Voltage			6.0	30		1.0	5.0		3.0	15		1.0	5.0	μV/°C
Average Temperature Coefficient of Input Offset Current			2	10		2.0	10		0.5	2.5		0.5	2.5	pA/°C
Input Bias Current				10			10			3.0			3.0	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 10\ k\Omega$	15			60			25			40			V/mV
Input Voltage Range	V_S = ±15V	±13.5			±13.5			±13.5			±13.5			V
Common Mode Rejection Ratio		80	100		96	110		85	100		96	110		dB
Supply Voltage Rejection Ratio		80	96		96	110		80	96		96	110		dB
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±13	±14		±13	±14		±13	±14		±13	±14		V
Supply Current	T_A = +125°C, V_S = ±20V								0.15	0.4		0.15	0.4	mA

NOTE 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C.

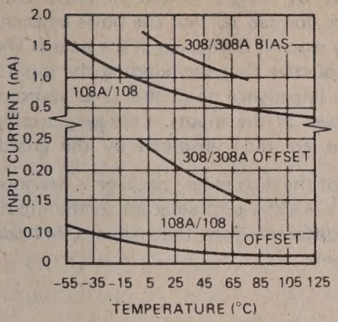
NOTE 2: The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

NOTE 3: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

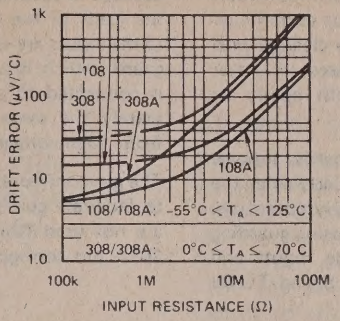
NOTE 4: Unless otherwise specified, these specifications apply for supply voltages from ±5V to ±20V for the 108, and 108A and ±5V to ±15V for the 308 and 308A.

TYPICAL PERFORMANCE CURVES

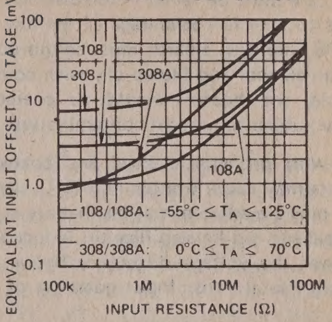
INPUT CURRENTS



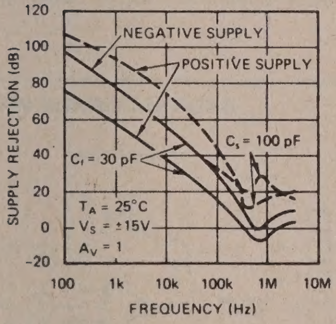
MAXIMUM DRIFT ERROR



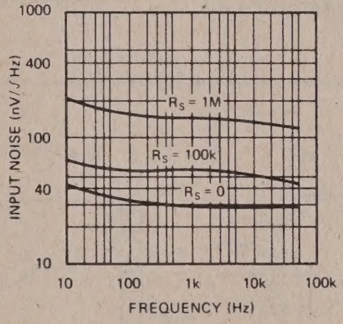
MAXIMUM OFFSET ERROR



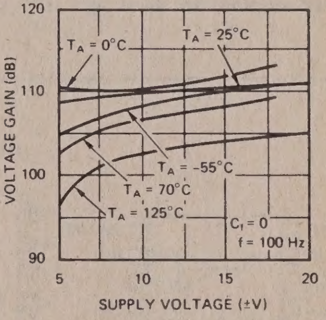
POWER SUPPLY REJECTION



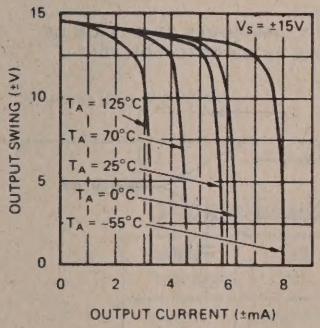
INPUT NOISE VOLTAGE



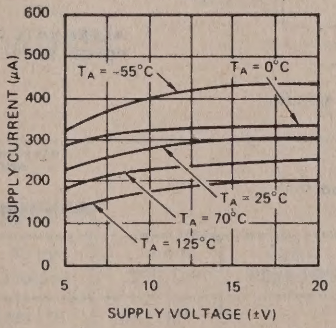
VOLTAGE GAIN



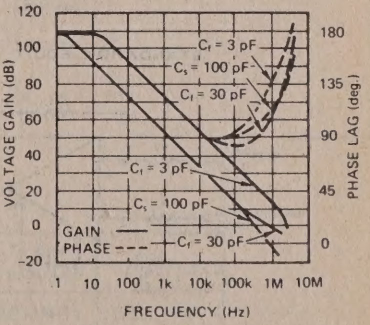
OUTPUT SWING



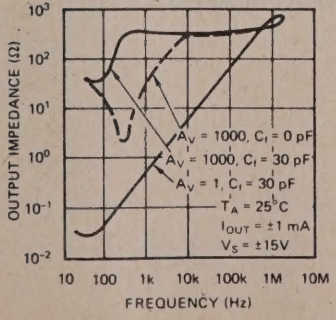
SUPPLY CURRENT



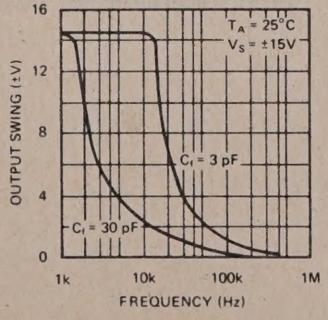
OPEN LOOP
FREQUENCY RESPONSE



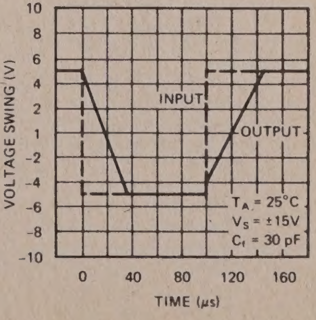
CLOSED LOOP
OUTPUT IMPEDENCE



LARGE SIGNAL
FREQUENCY RESPONSE



VOLTAGE FOLLOWER
PULSE RESPONSE



GUARDING

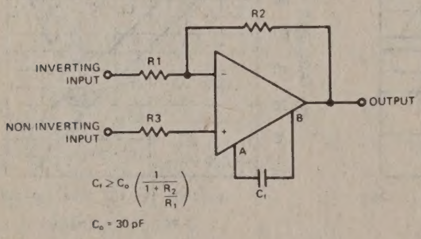
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage at the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration).

FREQUENCY COMPENSATION CIRCUITS

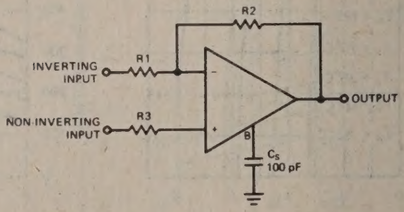
STANDARD CIRCUIT



$$C_f \geq C_o \left(\frac{1}{1 + \frac{R_2}{R_1}}\right)$$

C_o = 30 pF

ALTERNATE CIRCUIT: IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TEN.



LM111, LM311
Precision Voltage Comparators

FEATURES

- Differential Input Voltage Range — ±30V
- Input Common Mode Voltage Range — ±14V
- Operating Power Supplies +5V to ±18V
- Input Offset Current — 20 nA max
- Input Offset Voltage — 3 mV max
- Output Flexibility — 35V; 50 mA; T^2L Compatible
- Strobed Output & Input Offset Adjustable

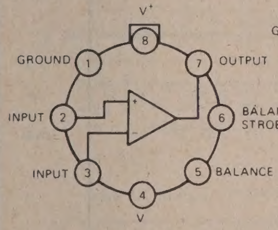
GENERAL DESCRIPTION

The LM111 Series comparators are designed for precision applications where the input and output characteristics of 710 and 106 high speed comparators are not adequate for low level signal detection and high level output drive capability. They are designed to operate from supplies up to ±18V and single supplies down to +5V. The output is capable of driving TTL, RTL, DTL as well as MOS and lamps or relays. Input offset voltage balancing and TTL strobe capability are provided. Outputs can be wire OR'ed.

Switching speeds to TTL logic levels are typically 250 ns.

PIN CONFIGURATIONS

METAL CAN

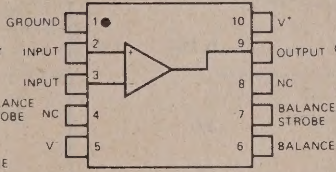

V+
8
GROUND 1
7 OUTPUT
INPUT 2
6 BALANCE STROBE
INPUT 3
5 BALANCE
4
V-

NOTE Pin 4 connected to case

TOP VIEW

(outline dwg TO-99)

FLAT PACKAGE

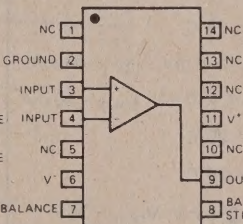

GROUND 1
INPUT 2
INPUT 3
NC 4
V- 5
10 V+
9 OUTPUT
8 NC
7 BALANCE STROBE
6 BALANCE

NOTE Pin 5 connected to bottom of package

TOP VIEW

(outline dwg FB)

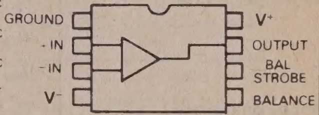
DUAL-IN-LINE


NC 1
GROUND 2
INPUT 3
INPUT 4
NC 5
V- 6
BALANCE 7
14 NC
13 NC
12 NC
11 V+
10 NC
9 OUTPUT
8 BALANCE/STROBE

NOTE Pin 6 connected to bottom of package

TOP VIEW

(outline dwg JD)


GROUND
+IN
-IN
V-
V+
OUTPUT
BAL STROBE
BALANCE

(outline dwg PA)

ORDERING INFORMATION

Part number	TO-99 Can	10 pin Flatpak	14 pin CER DIP	8 pin Plastic DIP	14 pin Plastic DIP	Dice
LM111	LM111H*	LM111F	LM111J*		LM311N-14	LM111/D
LM311	LM311H	LM311F	LM311J	LM311N		LM311/D

* Add /883B to order number if 883B processing is desired.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage		36V
Output to Negative Supply Voltage	LM111,	50V
	LM311	40V
Ground to Negative Supply Voltage		30V
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Power Dissipation (Note 2)		500 mW
Output Short Circuit Duration		10 sec
Operating Temperature Range	LM111	-55°C to +125°C
	LM311	0°C to +70°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LM111			LM311			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 4)	$T_A = 25^\circ C$, $R_S \leq 50k$		0.7	3.0		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25^\circ C$		4.0	10		6.0	50	nA
Input Bias Current	$T_A = 25^\circ C$		60	100		100	250	nA
Voltage Gain	$T_A = 25^\circ C$		200			200		V/mV
Response Time (Note 5)	$T_A = 25^\circ C$		200			200		ns
Saturation Voltage	$T_A = 25^\circ C$							
	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA		0.75	1.5				
	$V_{IN} < -10$ mV, $I_{OUT} = 50$ mA					0.75	1.5	V
Strobe on Current	$T_A = 25^\circ C$		3.0			3.0		mA
Output Leakage Current	$T_A = 25^\circ C$							
	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.2	10				
	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$					0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			4.0			10	mV
Input Offset Current (Note 4)				20			70	nA
Input Bias Current				150			300	nA
Input Voltage Range			±14			±14		V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$							
	$V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4				
	$V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA					0.23	0.4	V
Output Leakage Current (Note 6)	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5				µA
Positive Supply Current	$T_A = 25^\circ C$		5.1	6.0		5.1	7.5	mA
Negative Supply Current	$T_A = 25^\circ C$		4.1	5.0		4.1	5.0	mA

NOTE 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

NOTE 2: The maximum junction temperature of the 111 is 150°C, while that of the 311 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W, when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

NOTE 3: These specifications apply for $V_s = \pm 15V$ and over the operating temperature range, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15 supplies.

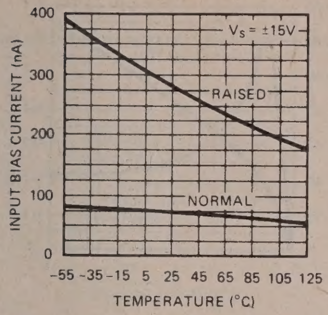
NOTE 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

NOTE 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

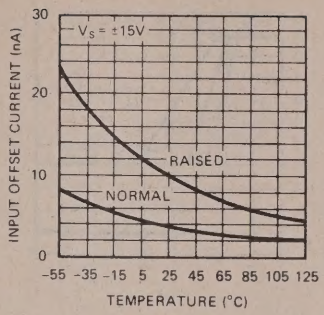
NOTE 6: This specification applies for Pin 1 −15V, Pin 7 +20V.

TYPICAL PERFORMANCE

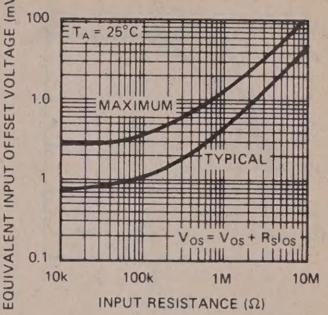
INPUT BIAS CURRENT 111



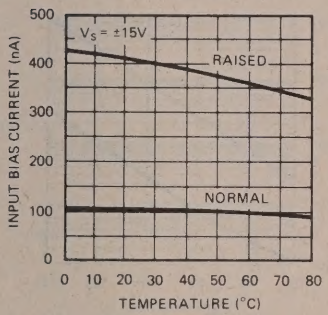
INPUT OFFSET CURRENT 111



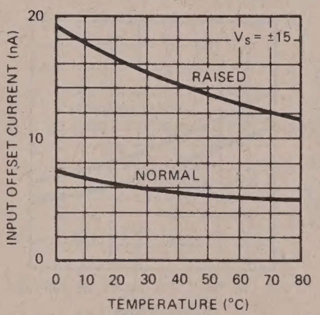
OFFSET ERROR 111



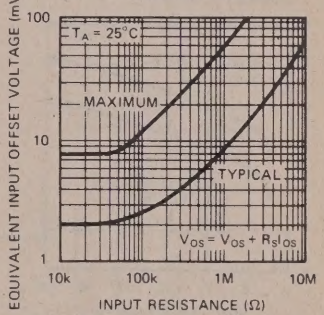
INPUT BIAS CURRENT 311



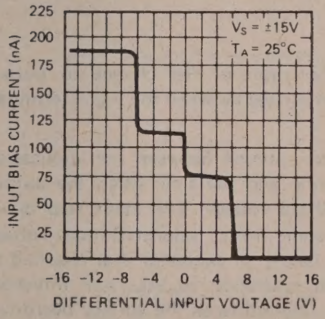
INPUT OFFSET CURRENT 311



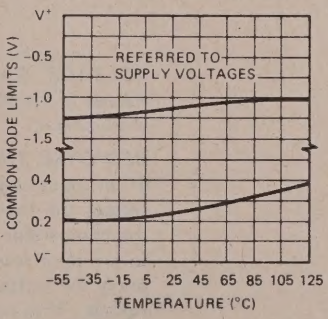
OFFSET ERROR 311



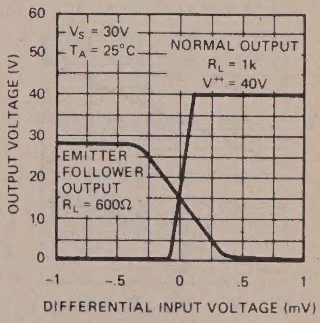
INPUT CHARACTERISTICS



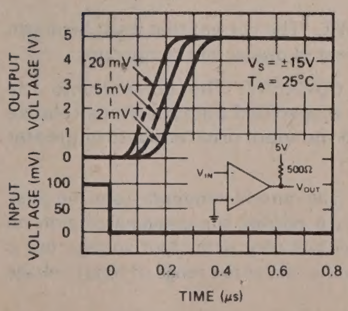
COMMON MODE LIMITS



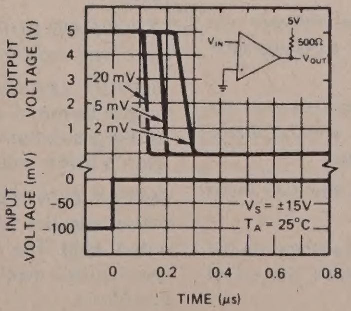
TRANSFER FUNCTION



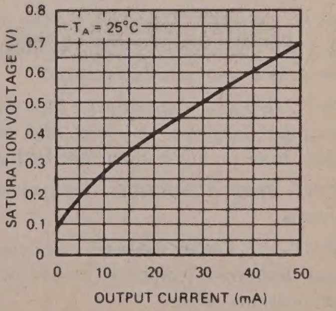
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

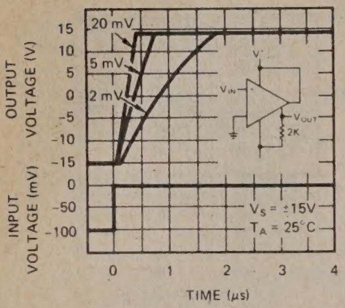


OUTPUT SATURATION VOLTAGE

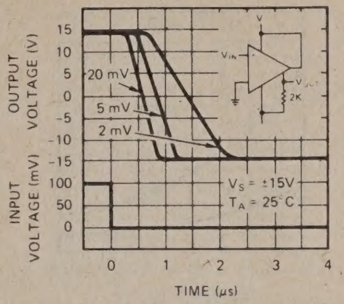


TYPICAL PERFORMANCE (Cont)

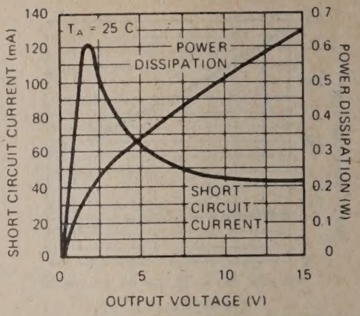
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



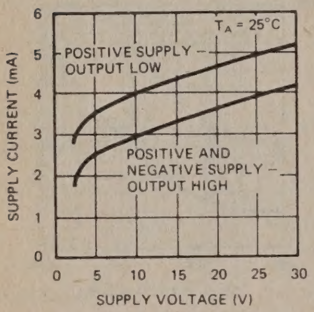
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



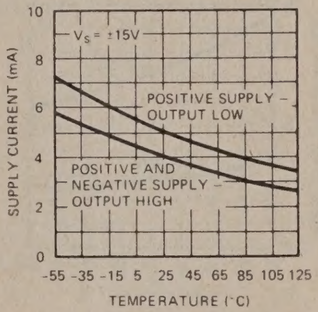
OUTPUT LIMITING CHARACTERISTICS



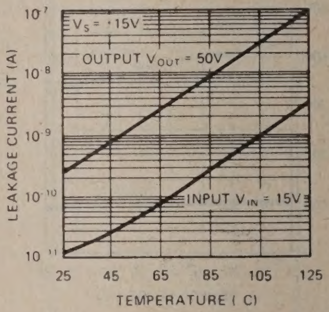
SUPPLY CURRENT



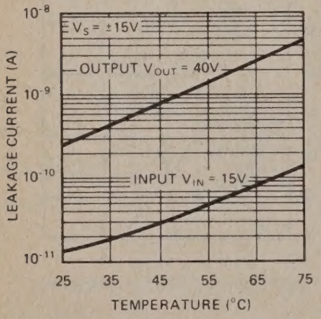
SUPPLY CURRENT



LEAKAGE CURRENTS 111/211



LEAKAGE CURRENTS 311



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE: The voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

INPUT OFFSET CURRENT: The difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

INPUT BIAS CURRENT: The average of the two input currents.

INPUT VOLTAGE RANGE: The range of voltage on the input terminals (common mode) over which the offset specifications apply.

VOLTAGE GAIN: The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

RESPONSE TIME: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

SATURATION VOLTAGE: The low output voltage level with the input drive equal to or greater than a specified value.

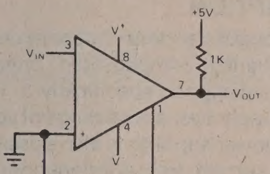
STROBE ON CURRENT: The current that must be drawn out of the strobe terminal to disable the comparator.

OUTPUT LEAKAGE CURRENT: The current into the output terminal with a specified output voltage relative to the ground pin and the input drive equal to or greater than a given value.

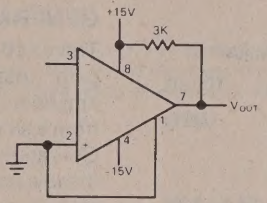
SUPPLY CURRENT: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

TYPICAL APPLICATIONS

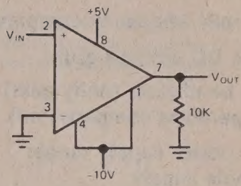
TTL COMPATIBLE OUTPUT SWING


+5V
V+
VIN
3
8
1K
7
VOUT
1
2
4
V-

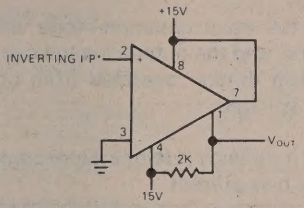
HIGH LEVEL TTL COMPATIBLE OUTPUT SWING


+15V
3K
3
8
7
VOUT
1
2
4
-15V

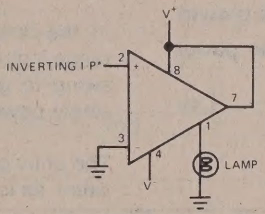
MOS LOGIC COMPATIBLE OUTPUT SWING


+5V
VIN
2
8
7
VOUT
1
3
4
10K
-10V

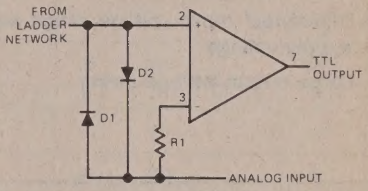
OBTAINING ±15 VOLT OUTPUT SWING


+15V
INVERTING I/P*
2
8
7
1
3
4
VOUT
2K
15V

DRIVING GROUND-REFERRED LOAD

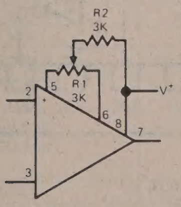

V+
INVERTING I/P*
2
8
7
1
3
4
V-
LAMP

USING CLAMP DIODES TO IMPROVE RESPONSE

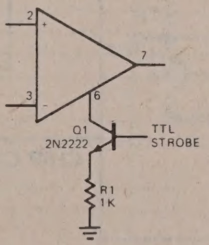

FROM
LADDER
NETWORK
2
D2
7
TTL
OUTPUT
3
D1
R1
ANALOG INPUT

*INPUT POLARITY REVERSED WHEN USING PIN 1 AS OUTPUT

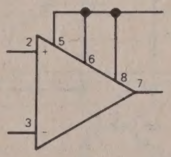
OFFSET BALANCING


R2
3K
5
R1
3K
V+
2
6
8
7
3

STROBING


2
7
3
6
Q1
2N2222
TTL
STROBE
R1
1K

INCREASING INPUT STAGE SLEW RATE*



*INCREASES TYPICAL COMMON MODE SLEW FROM 7.0V/µs TO 18V/µs

INTERSIL

LM124/324
Low Power Quad Operational Amplifiers

FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain 100dB
- Wide bandwidth (unity gain) 1MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3V to 30V
  - or dual supplies ±1.5V to ±15V
- Very low supply current drain (800μA) — essentially independent of supply voltage (1mW/op amp at +5V)
- Low input biasing current 45nA (temperature compensated)
- Low input offset 2mV and offset current 5nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V$^+$ — 1.5V

GENERAL DESCRIPTION

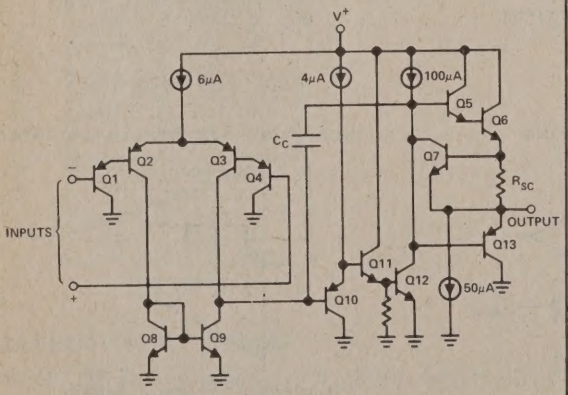
The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

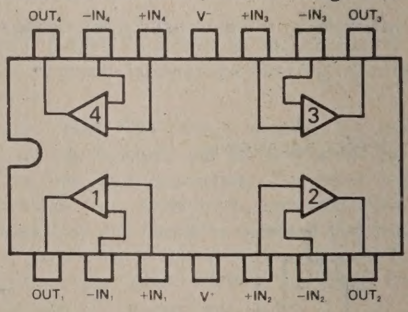
In the linear mode the input common-mode voltage range includes ground, and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain cross frequency is temperature compensated, as is the input bias current.

SCHEMATIC DIAGRAM (Each Amplifier)



PIN CONFIGURATION (outline dwgs JD, PD)

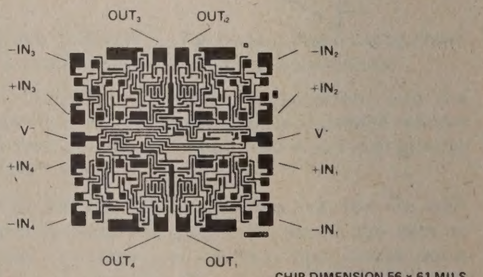


ORDERING INFORMATION

Part Number	Temperature Range	Dice	14 Pin CERDIP	14 Pin Plastic Dip
LM124	–55°C to +125°C	LM124/D	LM124J*	
LM324	0°C to +70°C	LM324/D	LM324J	LM324 N–14

* Add /883B to order number if 883B processing is desired.

CHIP CONFIGURATION



CHIP DIMENSION 56 x 61 MILS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V^+	32V or ±16V
Differential Input Voltage	32V
Input Voltage	−0.3V to +32V
Power Dissipation (Note 1)	
Plastic	570 mW
CERDIP	900 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \le 15$ and $T_A = 25°C$	Continuous

Input Current ($V_{IN} < -0.3\ V_{OL}$), (Note 3)	50 mA
Operating Temperature Range	
LM324	0°C to +70°C
LM124	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = +5.0V$, Note 4)

PARAMETER	CONDITIONS	LM124			LM324			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		±2	±5		±2	±7	mV
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$ $T_A = 25°C$		45	150		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		±3	±30		±5	±50	nA
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30V$, $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	$R_L = \infty$ $V_{CC} = 30V$, (LM2902 $V_{CC} = 26C$) $R_L = \infty$ On All Op Amps Over Full Temperature Range $T_A = 25°C$		1.5 0.7	3 1.2		1.5 0.7	3 1.2	mA mA mA
Large Signal Voltage Gain	$V^+ = 15V$ (For Large V_O Swing) $R_L \ge 2k\Omega$, $T_A = 25°C$	50	100		25	100		V/mV
Output Voltage Swing	$R_L = 2k\Omega$, $T_A = 25°C$ (LM2902 $R_L \ge 10k\Omega$)	0		$V^+-1.5$	0		$V^+-1.5$	V
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		65	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		dB
Amplifier-to-Amplifier Coupling (Note 8)	f = 1kHz to 20kHz, $T_A = 25°C$ (Input Referred)		−120			−120		dB
Output Current Source	$V_{IN^+} = 1V$, $V_{IN-} = 0V$, $V^+ = 15V$, $T_A = 25°C$	20	40		20	40		mA
Sink	$V_{IN-} = 1V$, $V_{IN} = 0V$, $V^+ = 15V$, $T_A = 25°C$	10	20		10	20		mA
	$V_{IN-} = 1V$, $V_{IN+} = 0V$, $T_A = 25°C$, $V_O = 200mV$	12	50		12	50		μA
Short Circuit to Ground	$T_A = 25°C$, (Note 2)		40	60		40	60	mA
Short Circuit to V^+			20	40		20	40	
Input Offset Voltage	(Note 5)			±7			±9	mV
Input Offset Voltage Drift	$R_S = 0\Omega$		7			7		μV/°C
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150	nA
Input Offset Current Drift			10			10		pA/°C
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	500		40	500	nA
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30V$	0		V^+-2	0		V^+-2	V
Large Signal Voltage Gain	$V^+ = +15V$ (For Large V_O Swing) $R_L \ge 2k\Omega$	25			15			V/mV
Output Voltage Swing V_{OH}	$V^+ = 30V$, $R_L = 2k\Omega$ $R_L \ge 10k\Omega$	26 27	 28		26 27	 28		V V
V_{OL}	$V^+ = 5V$, $R_L \le 10k\Omega$		5	20		5	20	mV
Output Current Source	$V_{IN} = +1V$, $V_{IN-} = 0V$, $V^+ = 15V$	10	20		10	20		mA
Sink	$V_{IN-} = +1V$, $V_{IN^+} = 0V$, $V^+ = 15V$	5	8		5	8		mA
Differential Input Voltage	(Note 7)			V^+			V^+	V

5

Note 1: For operating at high temperatures, the LM324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM124 can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Intersil's LM124 series is protected against shorts to either V⁺ or V⁻. No more than one output at a time should be shorted. At $V_{SUPP} > 15V$, continuous shorts can exceed the power dissipation ratings and cause eventual destruction.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parsitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V⁺ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative again returns to a value greater than −0.3V.

Note 4: These specifications apply for $V^+ = +5V$ and $-55°C \le T_A \le +125°C$ for the LM124, and $0°C \le T_A \le +70°C$ for the LM324.

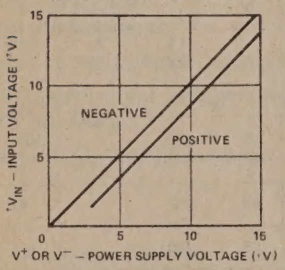
Note 5: $V_O \cong 1.4V$, $R_S = 0\Omega$ with V⁺ from 5V to 30V, and over the full input common-mode range (0V to $V^+ = 1.5V$).

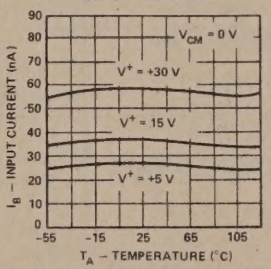
Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

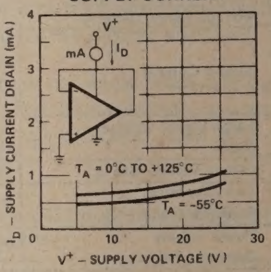
Note 7: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +32V without damage.

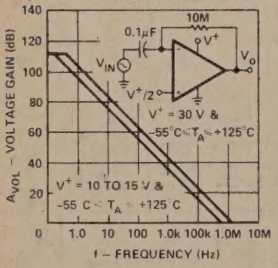
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.

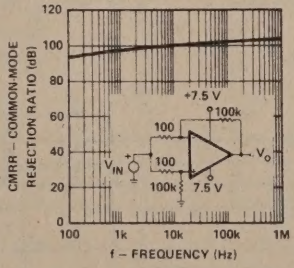
TYPICAL PERFORMANCE CHARACTERISTICS

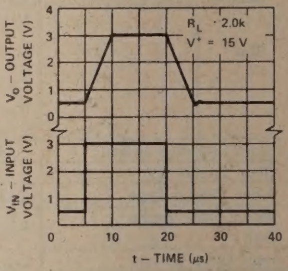

INPUT VOLTAGE RANGE

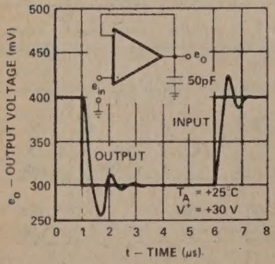

INPUT CURRENT

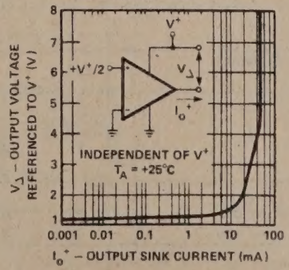

SUPPLY CURRENT

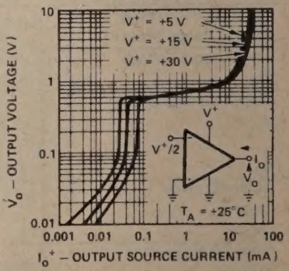

OPEN LOOP FREQUENCY RESPONSE


COMMON MODE REJECTION RATIO


VOLTAGE FOLLOWER PULSE RESPONSE


VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)


OUTPUT CHARACTERISTICS CURRENT SOURCING


OUTPUT CHARACTERISTICS CURRENT SINKING

INTERSIL

LM139/339
Voltage Comparators

FEATURES

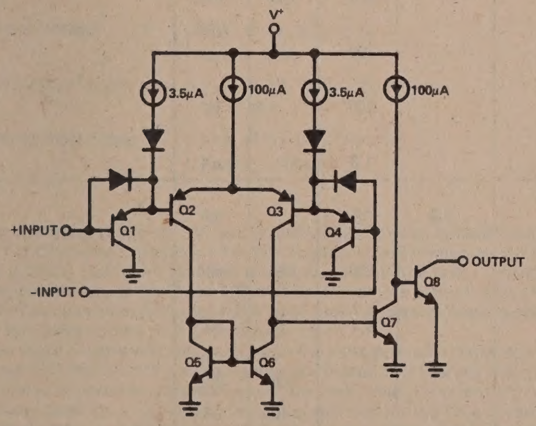
- **Wide single supply voltage range or dual supplies**
- **Very low supply current drain (0.8 mA)—independent of supply voltage (2 mW/comparator at +5 V)**
- **Low input biasing current 25 nA**
- **Low input offset current ±5 nA and offset voltage ±3 mV**
- **Input common-mode voltage range includes gnd**
- **Differential input voltage range equal to the power supply voltage**
- **Low output saturation voltage 250 mV at 4 mA**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

GENERAL DESCRIPTION

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic —where the low power drain of the LM339 is a distinct advantage over standard comparators.

SCHEMATIC DIAGRAM

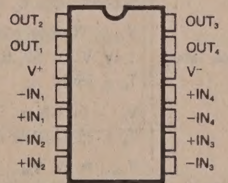


ORDERING INFORMATION

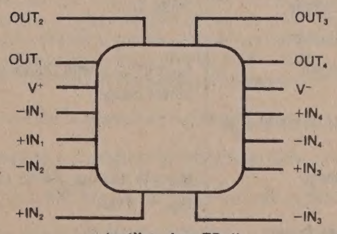
Part Number	Temperature Range	Dice	14 pin CCR DIP	14 pin Plastic	14 pin Flatpak
LM139	−55°C to +125°C	LM139/D	LM139J*		LM139F
LM339	0°C to +70°C	LM339/D	LM339J	LM339N	LM339F

* Add /883B to order number if 883B processing is desired.

PIN CONFIGURATION



(outline dwgs JD, PD)



(outline dwg FD-1)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V^+	36 V or ±18 V
Differential Input Voltage	36 V
Input Voltage	−0.3 V to +36 V
Power Dissipation (Note 1)	
Molded DIP	570 mW
Cavity DIP	900 mW
Flat Pack	800 mW
Output Short-Circuit to GND, (Note 2)	Continuous
Input Current ($V_{IN} < -0.3$ V), (Note 3)	50 mA
Operating Temperature Range	
LM339	0°C to +70°C
LM139	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

NOTE:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS ($V^+ = 5$ V, Note 4)

PARAMETER	CONDITIONS	LM139			UNITS
		MIN.	TYP.	MAX.	
Input Offset Voltage	$T_A = 25°C$, (Note 9)		±2.0	±5.0	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $T_A = 25°C$, (Note 5)		25	100	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		±3.0	±25	nA
Input Common-Mode Voltage Range	$T_A = 25°C$, (Note 6)	0		$V^+ - 1.5$	V
Supply Current	$R_L = \infty$ on all Comparators, $T_A = 25°C$				mA
	$R_L = \infty$, $V^+ = 30V$, $T_A = 25°C$		0.8	2.0	mA
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15V$ (To Support Large V_O Swing), $T_A = 25°C$		200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		300		ns
Response Time	$V_{RL} = 5$ V, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 7)		1.3		μs
Output Sink Current	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $V_O \leq 1.5$ V, $T_A = 25°C$	6.0	16		mA
Saturation Voltage	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA, $T_A = 25°C$		250	500	mV
Output Leakage Current	$V_{IN(+)} \geq 1V$, $V_{IN(-)} = 0$, $V_O = 5$ V, $T_A = 25°C$		0.1		nA
Input Offset Voltage	(Note 9)			9.0	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100	nA
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300	nA
Input Common-Mode Voltage Range		0		$V^+ - 2.0$	V
Saturation Voltage	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA			700	mV
Output Leakage Current	$V_{IN(+)} \geq 1V$, $V_{IN(-)} = 0$, $V_O = 30$ V			1.0	μA
Differential Input Voltage	Keep all V_{IN}'s ≥ 0 V (or V^-, if used), (Note 8)			36	V

ELECTRICAL CHARACTERISTICS (CON'T) ($V^+ = 5$ V

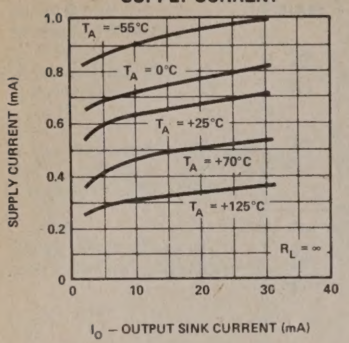
PARAMETER	CONDITIONS	LM339			UNITS
		MIN.	TYP.	MAX.	
Input Offset Voltage	T_A = 25°C, (Note 9)		±2.0	±5.0	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = 25°C, (Note 5)		25	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C		±5.0	±50	nA
Input Common-Mode Voltage Range	T_A = 25°C, (Note 6)	0		$V^+ - 1.5$	V
Supply Current	$R_L = \infty$ on all Comparators, T_A = 25°C		0.8	2.0	mA
	$R_L = \infty$, V^+ = 30V, T_A = 25°C				mA
Voltage Gain	$R_L \geq 15\ k\Omega$, V^+ = 15V (To Support Large V_O Swing), T_A = 25°C		200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, $R_L = 5.1\ k\Omega$, T_A = 25°C		300		ns
Response Time	V_{RL} = 5 V, $R_L = 5.1\ k\Omega$, T_A = 25°C, (Note 7)		1.3		μs
Output Sink Current	$V_{IN(-)} \geq$ 1V, $V_{IN(+)}$ = 0, $V_O \leq$ 1.5 V, T_A = 25°C	6.0	16		mA
Saturation Voltage	$V_{IN(-)} \geq$ 1V, $V_{IN(+)}$ = 0, $I_{SINK} \leq$ 4 mA, T_A = 25°C		250	500	mV
Output Leakage Current	$V_{IN(+)} \geq$ 1V, $V_{IN(-)}$ = 0, V_O = 5 V, T_A = 25°C		0.1		nA
Input Offset Voltage	(Note 9)			9.0	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150	nA
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			400	nA
Input Common-Mode Voltage Range		0		$V^+ - 2.0$	V
Saturation Voltage	$V_{IN(-)} \geq$ 1V, $V_{IN(+)}$ = 0, $I_{SINK} \leq$ 4 mA			700	mV
Output Leakage Current	$V_{IN(+)} \geq$ 1V, $V_{IN(-)}$ = 0, V_O = 30 V			1.0	μA
Differential Input Voltage	Keep all V_{IN}'s $\geq$ 0 V (or V^-, if used), (Note 8)			36	V

Note:

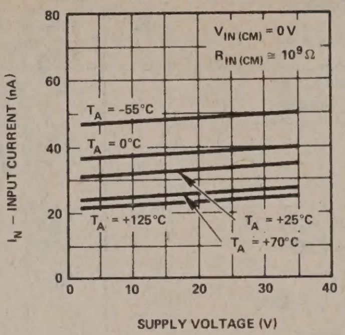
1. For operating at high temperatures, the LM339 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq$ 100 mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than −0.3V.
4. These specifications apply for V^+ = 5V and $-55°C \leq T_A \leq +125°C$, for the LM139. The LM339 temperature specifications are limited to $0°C \leq T_A \leq +70°C$.
5. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5$V, but either or both inputs can go to +30V without damage.
7. The response time specified is for a 100 mV input step with 5 mV overdrive signals 300 ns can be obtained, see typical performance characteristics section.
8. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).
9. At output switch point, V_O = 1.4V, R_S = 0Ω with V^+ from 5V; and over the full input common-mode range (0V to $V^+ - 1.5$V).
10. For input signals that exceed V^+, only the overdriven comparator is affected. With a 5V supply V_{IN} should be limited to 25V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

TYPICAL PERFORMANCE CHARACTERISTICS

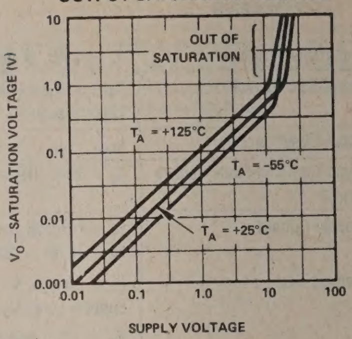
SUPPLY CURRENT



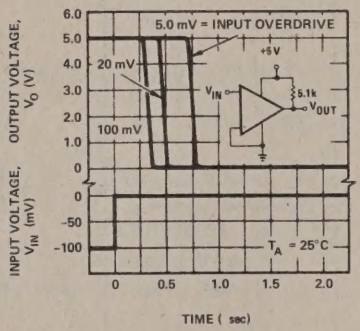
INPUT CURRENT



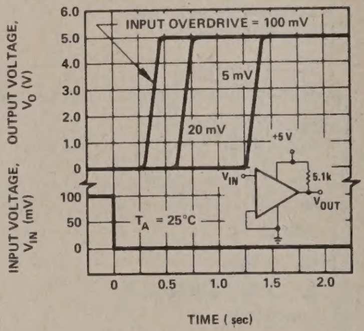
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES—NEGATIVE TRANSITION

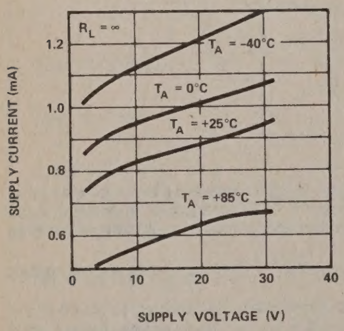


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES—POSITIVE TRANSITION

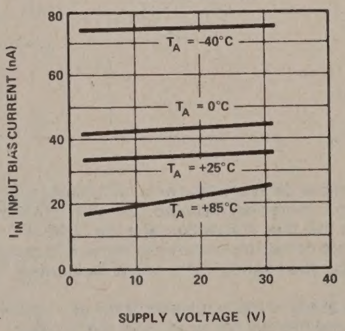


TYPICAL PERFORMANCE CHARACTERISTICS LM2901

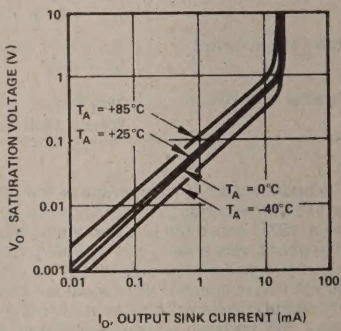
SUPPLY CURRENT



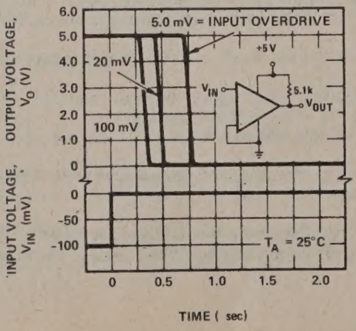
INPUT CURRENT



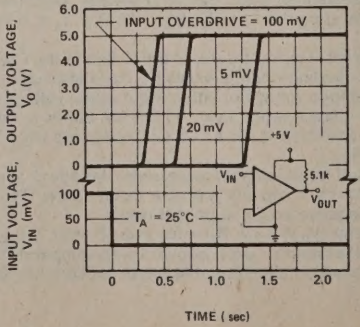
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES—NEGATIVE TRANSITION



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES—POSITIVE TRANSITION



APPLICATION HINTS

The LM139/339 are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

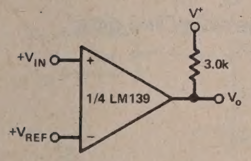
The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V to 30 V.

It is usually unnecessary to use a bypass capacitor across the power supply line.

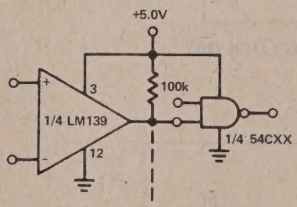
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60 Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

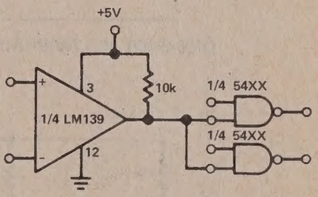
TYPICAL APPLICATIONS ($V^+ = 15\ V$)



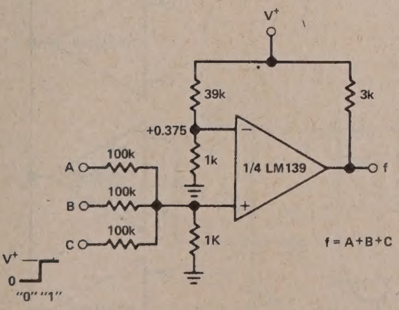
BASIC COMPARATOR



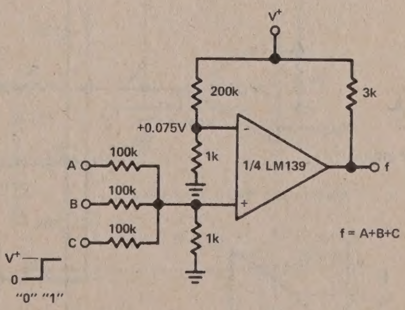
DRIVING CMOS



DRIVING TTL

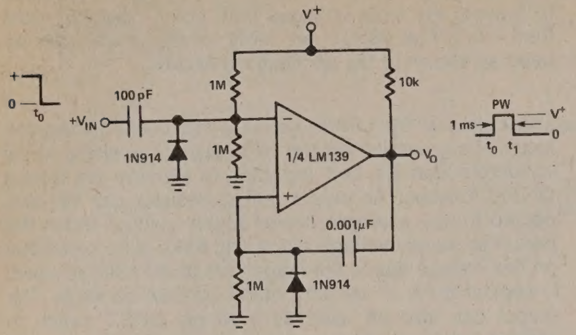


AND GATE

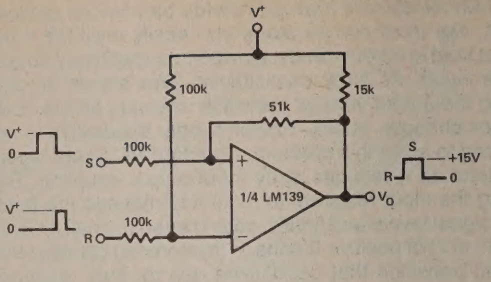


OR GATE

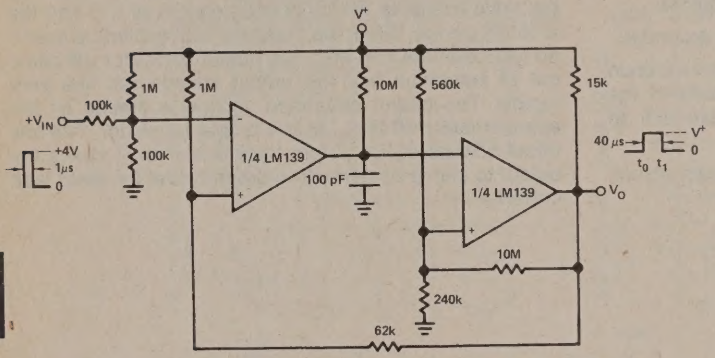
TYPICAL APPLICATIONS (CON'T) ($V^+ = 15$ V)


V+
+
0
t0
100 pF
+VIN
1N914
1M
1M
10k
1/4 LM139
VO
0.001μF
1M
1N914
PW
1 ms
V+
0
t0 t1

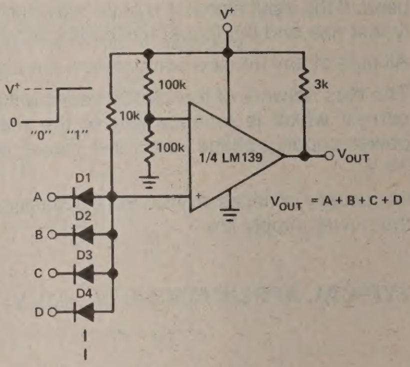
ONE-SHOT MULTIVIBRATOR


V+
100k
15k
51k
V+
0
100k
S
1/4 LM139
VO
S
+15V
R
0
V+
0
100k
R

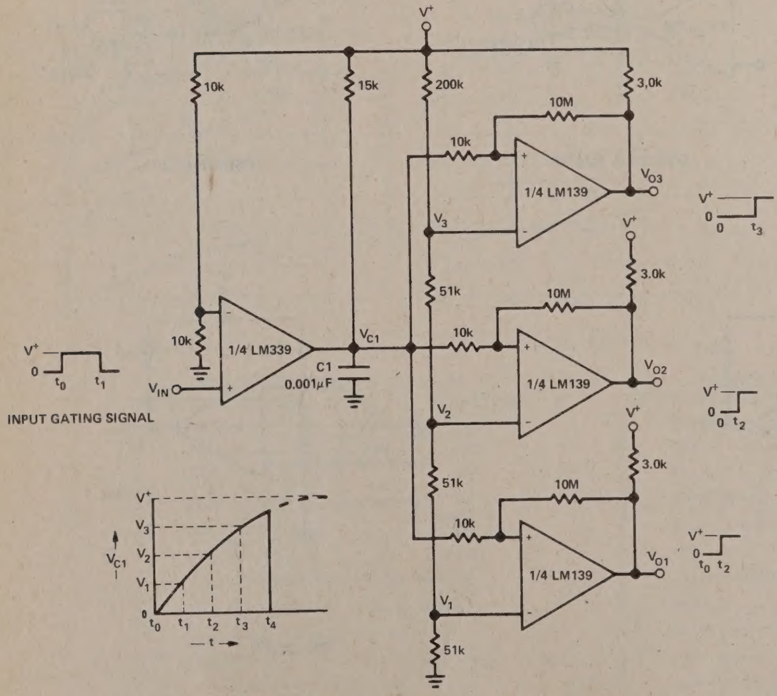
BI-STABLE MULTIVIBRATOR


V+
1M
1M
10M
560k
15k
100k
+VIN
+4V
1μs
0
100k
1/4 LM139
100 pF
1/4 LM139
VO
40 μs
V+
0
t0 t1
10M
240k
62k

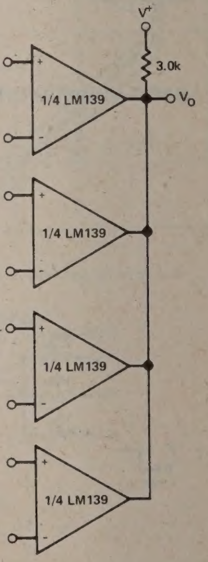
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT


V+
V+
0
"0" "1"
100k
3k
10k
100k
1/4 LM139
VOUT
D1
A
D2
B
D3
C
D4
D
VOUT = A + B + C + D

LARGE FAN-IN AND GATE

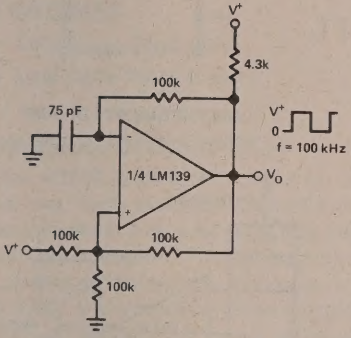

V+
10k
15k
200k
3,0k
10M
10k
1/4 LM139
VO3
V3
V+
0
0 t3
V+
3.0k
51k
10M
10k
10k
1/4 LM339
VC1
C1
0.001μF
1/4 LM139
VO2
V2
V+
0
0 t2
V+
0
t0 t1
VIN
INPUT GATING SIGNAL
V+
3.0k
51k
10M
10k
1/4 LM139
VO1
V1
V+
0
t0 t2
51k
V+
V3
V2
V1
VC1
0
t0 t1 t2 t3 t4
t

TIME DELAY GENERATOR

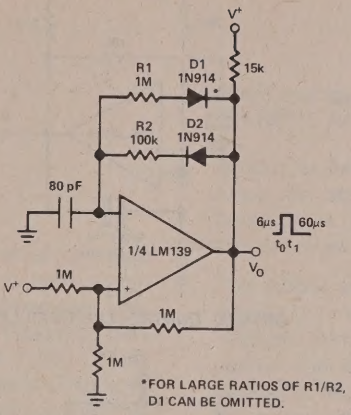

V+
3.0k
VO
1/4 LM139
1/4 LM139
1/4 LM139
1/4 LM139

'ANDing' THE OUTPUTS

TYPICAL APPLICATIONS (V+ = 5.0 V)

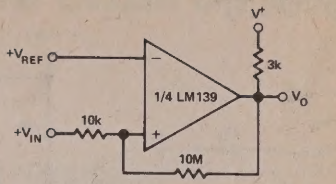

V+
4.3k
100k
75 pF
1/4 LM139
VO
V+
0
f = 100 kHz
100k
100k
V+
100k

SQUAREWAVE OSCILLATOR

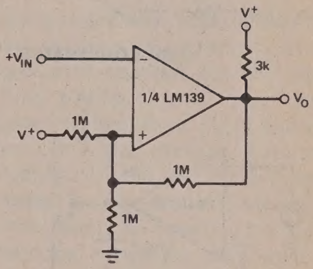

V+
15k
R1
1M
D1
1N914
R2
100k
D2
1N914
80 pF
1/4 LM139
6μs
60μs
t0
t1
VO
1M
V+
1M
1M

*FOR LARGE RATIOS OF R1/R2, D1 CAN BE OMITTED.

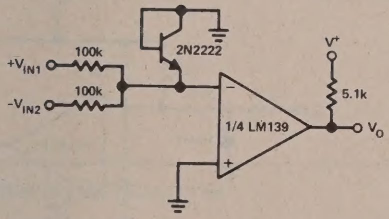
PULSE GENERATOR


V+
+VREF
3k
1/4 LM139
VO
+VIN
10k
10M

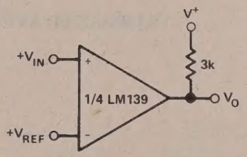
NON-INVERTING COMPARATOR WITH HYSTERESIS


V+
+VIN
3k
1/4 LM139
VO
V+
1M
1M
1M

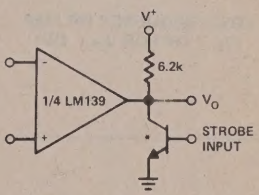
INVERTING COMPARATOR WITH HYSTERESIS


2N2222
100k
+VIN1
100k
-VIN2
V+
5.1k
1/4 LM139
VO

COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY

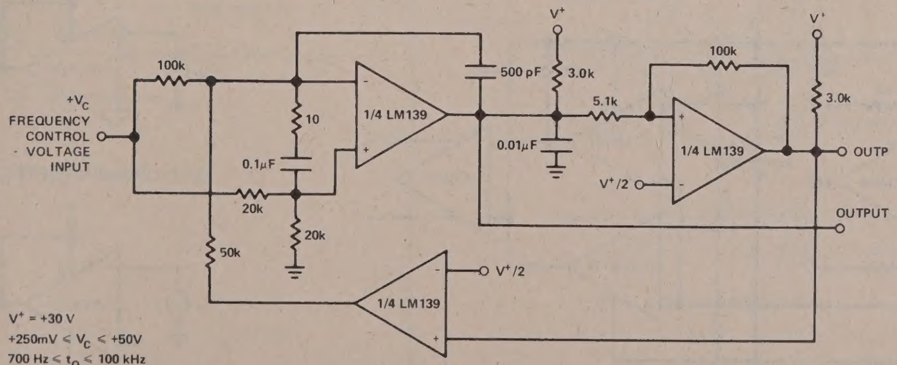

V+
+VIN
3k
1/4 LM139
VO
+VREF

BASIC COMPARATOR


V+
6.2k
1/4 LM139
VO
*
STROBE INPUT

*OR LOGIC GATE WITHOUT PULL-UP RESISTOR

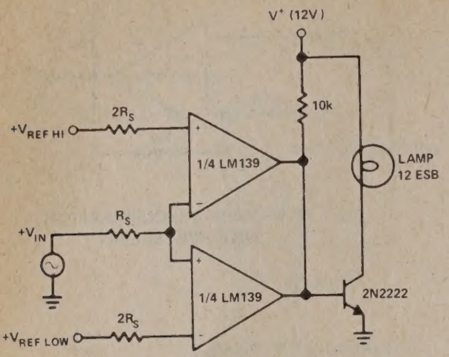
OUTPUT STROBING


100k
+VC
FREQUENCY CONTROL VOLTAGE INPUT
10
0.1μF
20k
20k
50k
1/4 LM139
500 pF
V+
3.0k
5.1k
0.01μF
100k
V+/2
1/4 LM139
V+
3.0k
OUTP
OUTPUT
V+/2
1/4 LM139

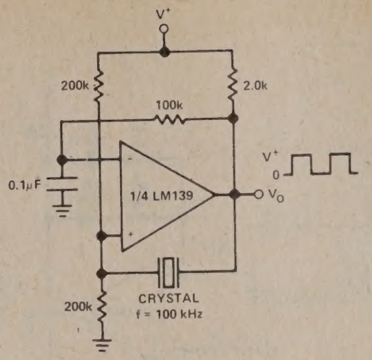
V+ = +30 V
+250mV ≤ VC ≤ +50V
700 Hz ≤ fO ≤ 100 kHz

TWO-DECADE HIGH-FREQUENCY VCO

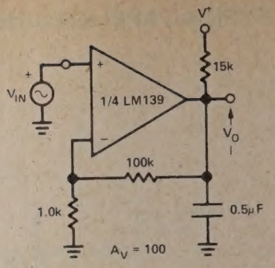
TYPICAL APPLICATIONS (CON'T) ($V^+ = 5$ V)


V⁺ (12V)
10k
2R_S
+V_{REF HI}
1/4 LM139
LAMP
12 ESB
R_S
+V_{IN}
1/4 LM139
2N2222
2R_S
+V_{REF LOW}

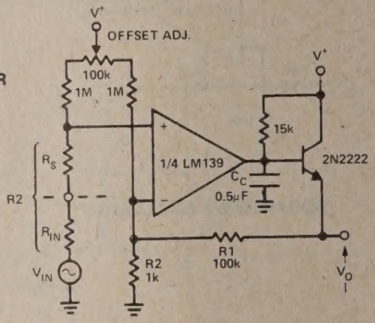
LIMIT COMPARATOR


V⁺
200k
2.0k
100k
V⁺
0
0.1μF
1/4 LM139
V_O
CRYSTAL
f = 100 kHz
200k

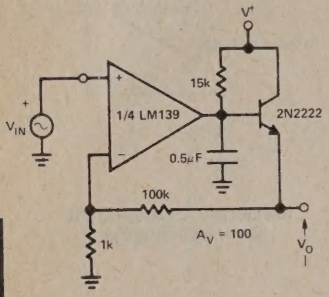
CRYSTAL CONTROLLED OSCILLATOR


V⁺
15k
V_{IN}
1/4 LM139
V_O
100k
1.0k
0.5μF
A_V = 100

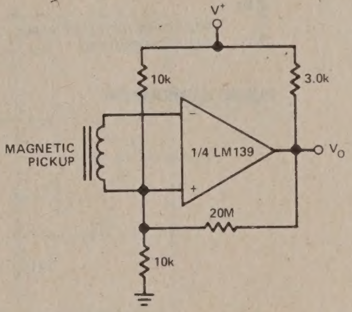
LOW FREQUENCY OP AMP


V⁺
OFFSET ADJ.
100k
1M
1M
V⁺
15k
R_S
1/4 LM139
2N2222
R2
C_C
0.5μF
R_{IN}
R1
100k
V_{IN}
R2
1k
V_O

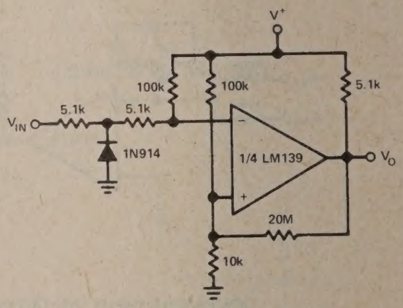
LOW FREQUENCY OP AMP WITH OFFSET ADJUST


V⁺
15k
1/4 LM139
2N2222
V_{IN}
0.5μF
100k
1k
A_V = 100
V_O

LOW FREQUENCY OP AMP
(V_O = 0V FOR V_{IN} = 0V)

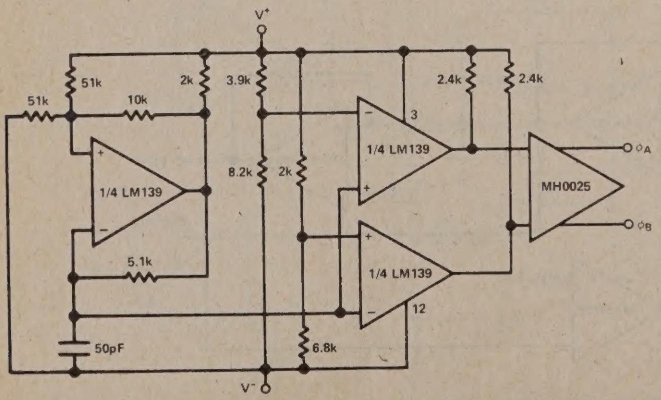

V⁺
10k
3.0k
MAGNETIC
PICKUP
1/4 LM139
V_O
20M
10k

TRANSDUCER AMPLIFIER

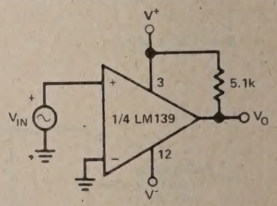

V⁺
100k
100k
5.1k
5.1k
5.1k
V_{IN}
1N914
1/4 LM139
V_O
20M
10k

ZERO CROSSING DETECTOR
(SINGLE POWER SUPPLY)

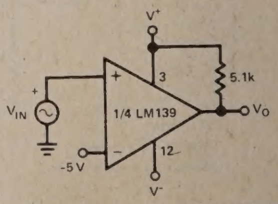
SPLIT-SUPPLY APPLICATIONS ($V^+ = +15$ V and $V^- = -15$ V)


V⁺
51k
2k
3.9k
2.4k
2.4k
51k
10k
3
1/4 LM139
φA
8.2k
2k
1/4 LM139
MH0025
φB
5.1k
1/4 LM139
12
50pF
6.8k
V⁻

MOS CLOCK DRIVER


V⁺
3
5.1k
V_{IN}
1/4 LM139
V_O
12
V⁻

ZERO CROSSING DETECTOR


V⁺
3
5.1k
V_{IN}
1/4 LM139
V_O
-5V
12
V⁻

COMPARATOR WITH A NEGATIVE REFERENCE

AD503
High Accuracy Low Offset Op Amp

FEATURES

- **Low I_{BIAS}: 15pA MAX**
- **Low Drift: 25μV°C MAX**

GENERAL DESCRIPTION

The AD503 is an IC FET input op amp which provides the user with input currents of a few pA, high overall performance, low cost, and accurately specified, predictable operation. The device achieves maximum bias currents as low as 5pA, minimum gain of 75,000, CMRR of 80dB, and a minimum slew rate of 3V/μs. It is free from latch-up and is short circuit protected, and no external compensation is required, as the internal 6dB/octave rolloff provides stability in closed loop applications.

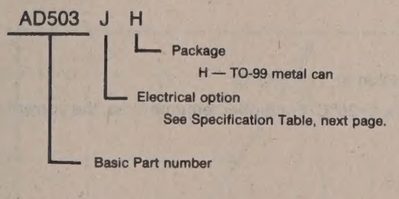
The AD503 is suggested for all general purpose FET input amplifier requirements where low cost is of prime importance.

The circuits are supplied in the TO-99 package; the AD503J, K are specified for 0 to +70°C temperature range operation; the AD503S for operation from −55°C to +125°C.

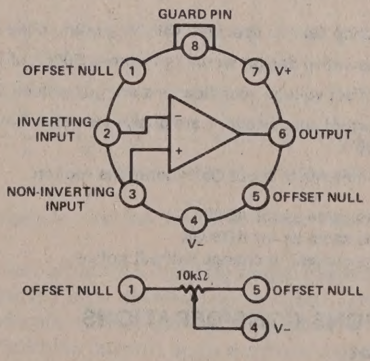
It provides performance comparable to modular FET op amps, but because of its monolithic construction, however, its cost is significantly below that of modules, and becomes even lower in large quantities.

The AD503 is especially designed for applications involving the measurement of low level currents or small voltages from high impedance sources, in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations, the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the noninverting "buffer" connection is used). The AD503, therefore, is of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

ORDERING INFORMATION


AD503 J H
Package
H — TO-99 metal can
Electrical option
See Specification Table, next page.
Basic Part number

PIN CONFIGURATION


GUARD PIN
8
OFFSET NULL 1
7 V+
INVERTING INPUT 2
−
+
6 OUTPUT
NON-INVERTING INPUT 3
5 OFFSET NULL
4
V−
OFFSET NULL 1
10kΩ
5 OFFSET NULL
4 V−

(outline dwg TO-99)

SPECIFICATIONS (Typical @ +25°C and ±15Vdc, unless otherwise noted)

PARAMETER	AD503J	AD503K	AD503S
OPEN LOOP GAIN[1]			
$V_{OUT} = \pm10V$, $R_L \geq 2k\Omega$	20,000 min (50,000 typ)	50,000 min (120,000 typ)	**
T_A = min to max	15,000 min	40,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±13V typ)	*	*
Voltage @ $R_L = 10k\Omega$, T_A = min to max	±12V min (±14V typ)	*	*
Load Capacitance[2]	750pF	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	3.0V/µs min (6.0V/µs typ)	*	*
Settling Time, Unity Gain (to 0.1%)	10µs	*	*
INPUT OFSET VOLTAGE[3]	50mV max (20mV typ)	20mV max (8mV typ)	**
vs Temperature, T_A = min to max	75µV/°C max (30µV/°C typ)	25µV/°C max (10µV/°C typ)	50µV°C max (20µV/°C typ)
vs Supply, T_A = min to max	400µV/V max (200µV/V typ)	200µV/V max (100µV/V typ)	**
INPUT BIAS CURRENT			
Either Input[4]	15pA max (5pA typ)	10pA max (2.5pA typ)	**
INPUT IMPEDANCE			
Differential	$10^{11}\ \Omega \parallel 2pF$	*	*
Common Mode	$10^{12}\ \Omega \parallel 2pF$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	15µV (p-p)	*	*
5Hz to 50kHz	5.0µV (rms)	*	*
f = 1kHz (spot noise)	30.0nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±3.0V	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, $V_{IN} = \pm10V$	70dB min (90dB typ)	80dB min (90dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	±(5 to 22)V
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

Note 1. Open Loop Gain is specified with V_{OS} both nulled and unnulled.

Note 2. A conservative design would not exceed 500pF of load capacitance.

Note 3. Input offset voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.

Note 4. Bias current specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$. For higher temperatures, the current doubles every 10°C.

Note 5. See comments in Input Considerations section.

*Specifications same as for AD503J.
**Specifications same as for AD503K.
Specifications subject to change without notice.

APPLICATIONS CONSIDERATIONS

Bias Current

Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the "maximum" bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed up operating unit.

The AD503 specifies maximum bias currents at either input after warmup, thus giving the user the values he expected.

Improving Bias Current Beyond Guaranteed Values

Bias currents can be substantially reduced by decreasing the junction temperature of the device. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

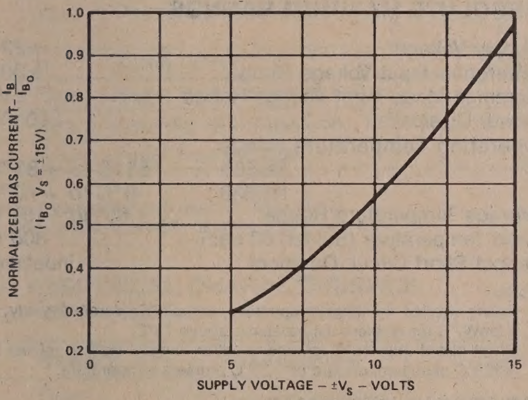


Figure 1. Normalized Bias Current vs Supply Voltage

Operation of the AD503K at ±5V reduces the warmed up bias current by 70% to a typical value of 0.75pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading.

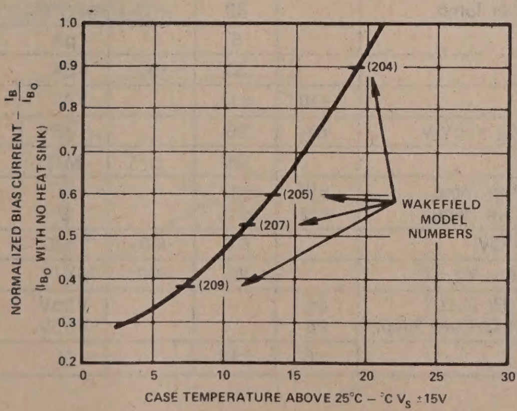


Figure 2. Normalized Bias Current vs Case Temperature

Note that the use of the model 209 heat sink reduces warmed up bias current by 60% to 1.0pA in the AD503K.

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

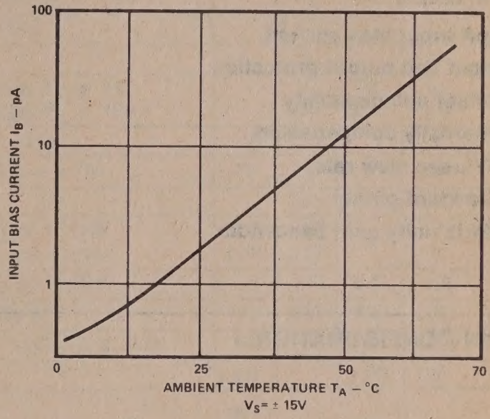


Figure 3. Input Bias Current vs Temperature

Input Considerations

The common mode input characteristic is shown in Figure 4. Note that positive common mode inputs up to +13.5 Volts and negative common mode inputs to –Vs are permissible, without incurring excessive bias currents. To prevent possible damage to the unit, do not exceed V_{CM} = Vs.

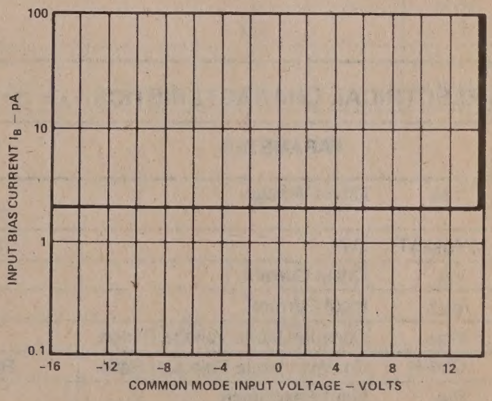


Figure 4. Input Bias Current vs Common Mode Voltage

Like most other FET input op amps, the AD503 displays a degraded bias current specification when operated at moderate differential input voltages. It maintains its specified bias current up to a differential input voltage of ±3V typically. Above ±3V, the bias current will increase to approximately 400μA. This is not a failure mode. Above ±10V differential input voltage, the bias current will increase 100μA/V_{diff} (in volts), and other parameters may suffer degradation.

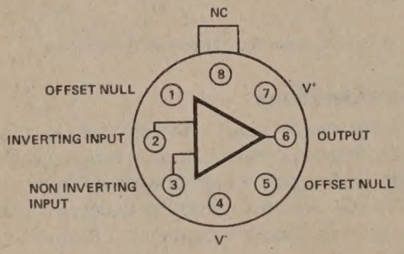
INTERSIL

536
FET Input Operational Amplifier

FEATURES

- **5pA input bias current**
- **Input and output protection**
- **Offset null capability**
- **Internally compensated**
- **6V/μsec slew rate**
- **Standard pinout**
- **1MHz unity gain bandwidth**

PIN CONFIGURATION



(outline dwg TO-99)

DESCRIPTION

The 536 is a special purpose high performance operational amplifier utilizing a FET input stage for extremely high input impedance and low input current.

The device features internal compensation, standard pinout, wide differential and common mode input voltage ranges, high slew rate and high output drive capability.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Differential Input Voltage Range .... ±30V
Common Mode Input Voltage Range .... $\pm V_S$
Power Dissipation[1] 500mW
Operating Temperature Range
SU536 ... −55°C to +85°C
NE536 ..... 0°C to +70°C
Storage Temperature Range .... −65° to +150°C
Lead Temperature (Solder, 60 sec) .... 300°C
Output Short Circuit Duration[2] .... indefinite

Notes:
1. Rating applies for case temperature to +25°C; derate linearly at 6.5mW/°C for ambient temperatures above 75°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

ORDERING INFORMATION

TEMPERATURE RANGE	DICE	TO-99 CAN
0°C to +70°C	NE536/D	NE536T
−55°C to +85°C	SU536/D	SU536T

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, V_{SUPP} ±15V unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS	NE536			UNIT
			MIN.	TYP.	MAX.	
V_{OS}	Offset Voltage	$R_S \leq 10k\Omega$ Over Temp., $R_S \leq 10k\Omega$		30 30	90	mV mV
$\Delta V_{OS}/\Delta T$	Drift	$R_S = 0\Omega$, Over Temp.		30		μV/°C
I_{OS}	Offset Current			5		pA
I_{BIAS}	Input Current[2]			30	100	pA
V_{CM}	Common Mode Voltage Range		±10	±11		V
CMRR	Common Mode Rejection Ratio	$R_S \leq 10k\Omega$, $V_{IN} = \pm 10V$	64	80		dB
R_{IN}	Input Resistance			100		MΩ
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$, Over Temp. $R_L \geq 10k\Omega$, Over Temp.	±10 ±12	±11 ±13		V V
I_{CC}	Supply Current	$V_{OUT} = 0V$		6.0	8.0	mA
PSRR	Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$, $\pm 6 \leq V_S \pm 15$		100	300	μV/V
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, R_L 2kΩ $V_O = \pm 10V$, $R_L \geq 2k\Omega$, Over Temp.	50 25			V/mV V/mV
V_{SUPP}	Power Supply Range		±6	±18		V

Notes:
1. Input current typically doubles every 10°C.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $\pm 6V \leq V_S \leq \pm 20V$ unless otherwise specified.[2]

PARAMETER		TEST CONDITIONS	SU536			UNIT
			MIN.	TYP.	MAX.	
V_{OS}	Offset Voltage[2]	$R_S \leq 10k\Omega$ Over Temp. Range, $R_S \leq 10k\Omega$		7.5 7.5	20 30	mV mV
$\Delta V_{OS}/\Delta T$	Drift	$R_S \leq 10k\Omega$		20		μV/°C
I_{OS}	Offset Current			5		pA
I_{BIAS}	Input Current[1,2]	Over Temp. Range, $R_L \geq 2k$ Over Temp. Range, $R_L \geq 10k$		5 250	30 3000	pA pA
V_{CM}	Common Mode Voltage Range	$V_{SUPP} = \pm 15V$	±10	±11		V
CMRR	Common Mode Rejection Ratio	$R_S \leq 10k\Omega$, $V_{IN} = \pm 10V$	70	80		dB
R_{IN}	Input Resistance			100		MΩ
V_{OUT}	Output Voltage Swing[2]	$R_L \geq 2k\Omega$, $V_{SUPP} = \pm 15V$ $R_L \geq 10k\Omega$, $V_{SUPP} = \pm 15V$	±10 ±12	±12 ±13		V V
I+	Supply Current	$V_{OUT} = 0V$, $V_{SUPP} = \pm 20V$		4.5	5.5	mA
P_{SRR}	Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		50	150	μV/V
A_{VOL}	Large Signal Voltage Gain[2]	$V_{SUPP} = \pm 15V$, $V_O = \pm 10V$, $R_L \geq 2k\Omega$	50			V/mV
V_{SUPP}	Power Supply Range		±6		±20	V

Notes:
1. Input current typically doubles every 10°C.
2. Operating temperature range is −55°C to +85°C.

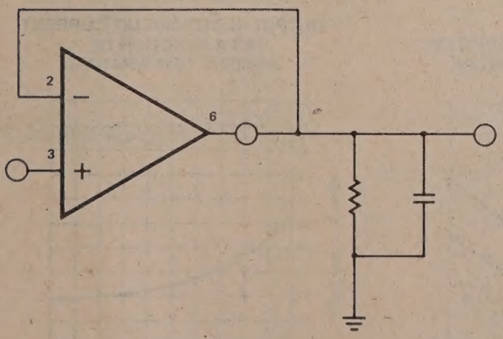
AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$ unless otherwise specified.[1,2]

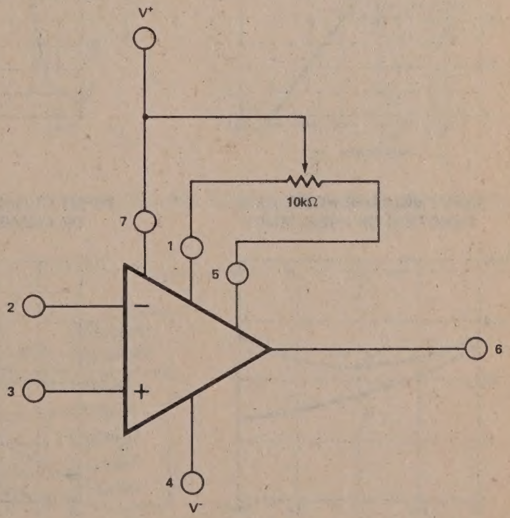
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{DIFF}	Differential Capacitance			6		pF
e_n	Input Noise Voltage	0.1Hz—100kHz		20		μVrms
Z_O	Output Impedance			100		Ω
G_{BW}	Unity Gain Frequency Full Power Bandwidth	$V_{SUPP} = \pm 15V$ $V_{SUPP} = \pm 15V$		1 100		MHz KHz
SR	Slew Rate, Inverter Slew Rate, Follower	$V_{SUPP} = \pm 15V$, $A = -1V$ $V_{SUPP} = \pm 15V$, $A = +1V$		6 6		V/μs V/μs

Notes:
1. Temperature range is $-55 \leq T_A \leq 85°C$
2. $\pm 6V \leq V_{SUPP} \pm 20V$

TEST CIRCUITS



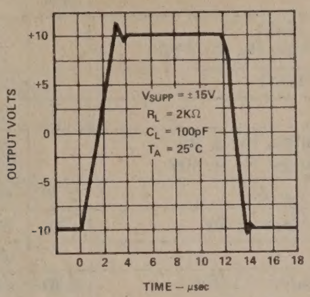
VOLTAGE FOLLOWER CIRCUIT



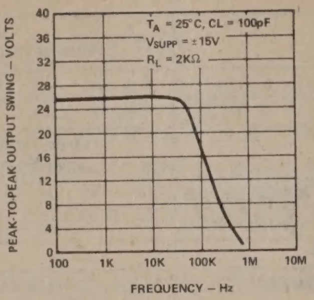
OFFSET NULL CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS

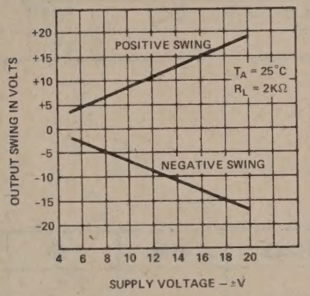
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



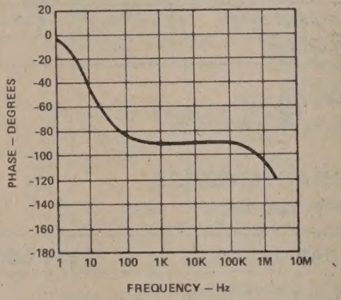
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



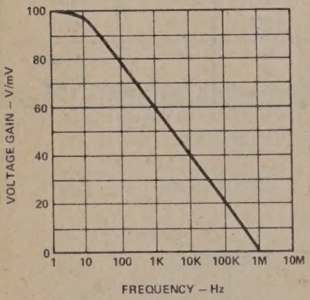
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



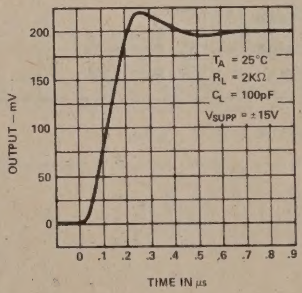
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



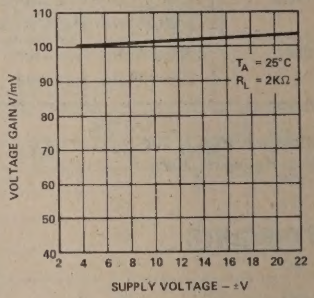
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



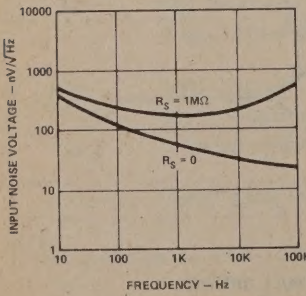
VOLTAGE FOLLOWER TRANSIENT RESPONSE



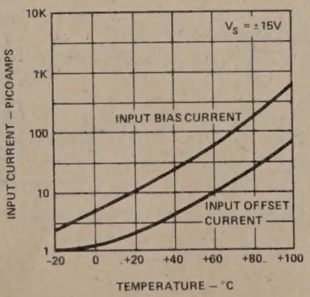
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



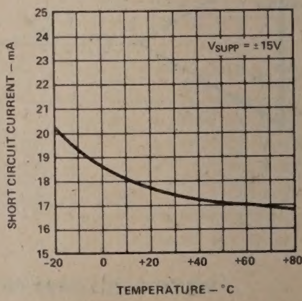
INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INTERSIL

AD590
Two-Terminal IC Temperature Transducer

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

- **Linear current output: 1 μA/°K**
- **Wide range: −55°C to +150°C**
- **Two-terminal device: Voltage in/current out**
- **Laser trimmed to ±0.5°C calibration accuracy (AD590M)**
- **Excellent linearity: ±0.5°C over full range (AD590M)**
- **Wide power supply range: +4V to +30V**
- **Sensor isolation from case**
- **Low cost**

GENERAL DESCRIPTION

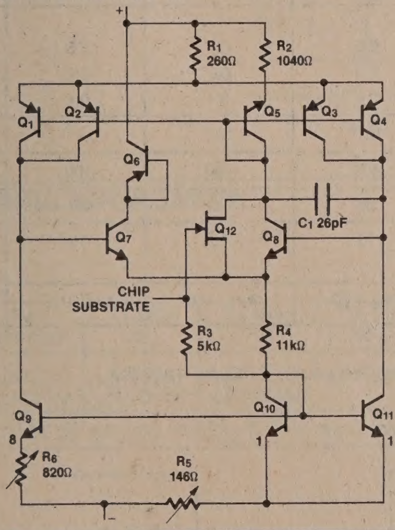
The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing 1 μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2 μA output at 298.2°K (+25°C).

The AD590 should be used in any temperature sensing application between −55°C and +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance-measuring circuitry and cold junction compensation are not needed in applying the AD590. In the simplest application, a resistor, a power source and any voltmeter can be used to measure temperature.

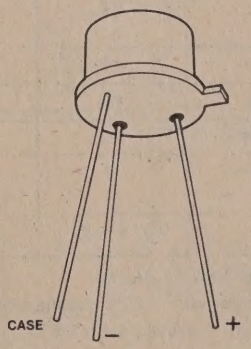
In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

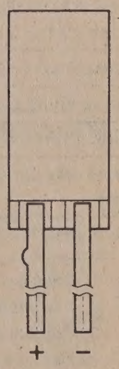
SCHEMATIC DIAGRAM



PIN CONFIGURATIONS



(Outline Drawing TO-52)



(Outline Drawing DH)

ORDERING INFORMATION

NON-LINEARITY (°C)	TO-52 PACKAGE	CERAMIC PACKAGE
±3.0	AD590IH	AD590IF
±1.5	AD590JH	AD590JF
±0.8	AD590KH	AD590KF
±0.4	AD590LH	AD590LF
±0.3	AD590MH	AD590MF

ABSOLUTE MAXIMUM RATINGS

($T_A = +25°C$ unless otherwise noted)

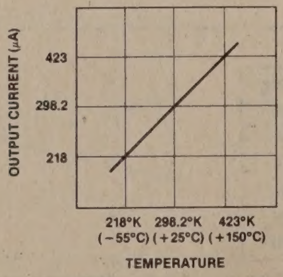
Forward Voltage (V^+ to V^-) . . . . +44V
Reverse Voltage (V^+ to V^-) . . . . −20V
Breakdown Voltage (Case to V^+ or V^-) . . . . ±200V
Rated Performance Temperature Range . . −55°C to +150°C
Storage Temperature Range . . . . −65°C to +175°C
Lead Temperature (Soldering, 10 sec) . . . . +300°C

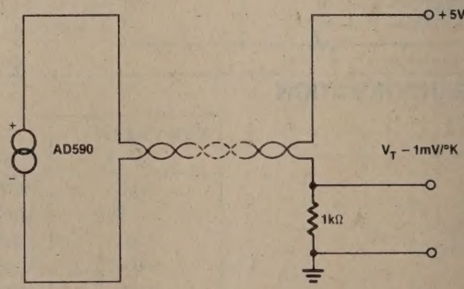
SPECIFICATIONS (Typical values at $T_A = +25°C$, $V^+ = 5V$ unless otherwise noted)

CHARACTERISTICS	AD590I	AD590J	AD590K	AD590L	AD590M	UNITS
Output Nominal Output Current @ +25°C (298.2°K)	298.2	298.2	298.2	298.2	298.2	μA
Nominal Temperature Coefficient	1.0	1.0	1.0	1.0	1.0	μA/°K
Calibration Error @ +25°C (Notes)	±10.0 max	±5.0 max	±2.5 max	±1.0 max	±0.5 max	°C
Absolute Error (−55°C to +150°C) Without External Calibration Adjustment	±20.0 max	±10.0 max	±5.5 max	±3.0 max	±1.7 max	°C
With External Calibration Adjustment	±5.8 max	±3.0 max	±2.0 max	±1.6 max	±1.0 max	°C
Non-Linearity	±3.0 max	±1.5 max	±0.8 max	±0.4 max	±0.3 max	°C
Repeatability (Note 2)	±0.1 max	±0.1 max	±0.1 max	±0.1 max	±0.1 max	°C
Long Term Drift (Note 3)	±0.1 max	±0.1 max	±0.1 max	±0.1 max	±0.1 max	°C/month
Current Noise	40	40	40	40	40	$pA/\sqrt{Hz}$
Power Supply Rejection						
$+4 < V^+ < +5V$	0.5	0.5	0.5	0.5	0.5	μA/V
$+5 < V^+ < +15V$	0.2	0.2	0.2	0.2	0.2	μA/V
$+15V < V^+ < +30V$	0.1	0.1	0.1	0.1	0.1	μA/V
Case Isolation to Either Lead	10^{10}	10^{10}	10^{10}	10^{10}	10^{10}	Ω
Effective Shunt Capacitance	100	100	100	100	100	pF
Electrical Turn-On Time (Note 1)	20	20	20	20	20	μs
Reverse Bias Leakage Current (Note 4)	10	10	10	10	10	pA
Power Supply Range	+4 to +30	+4 to +30	+4 to +30	+4 to +30	+4 to +30	V

Notes
1. Does not include self heating effects.
2. Maximum deviation between +25°C reading after temperature cycling between −55°C and +150°C.
3. Conditions: Constant +5V, constant +125°C.
4. Leakage current doubles every +10°C.

TYPICAL APPLICATIONS





Typical Connection

μA723
Voltage Regulator

FEATURES

- **150 mA output current without external pass transistor**
- **Output currents in excess of 10A possible by adding external transistors**
- **Input voltage 40V max**
- **Output voltage adjustable from 2V to 37V**
- **Can be used as either a linear or a switching regulator.**

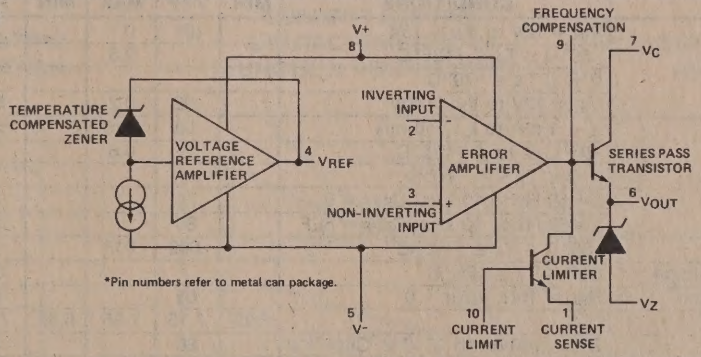
GENERAL DESCRIPTION

The 723 is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 120 mA, but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The 723 is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature-controller.

The 723C is identical to the 723M except that the 723C has its performance guaranteed over a 0°C to 70°C temperature range, instead of −55°C to +125°C.

BLOCK DIAGRAM



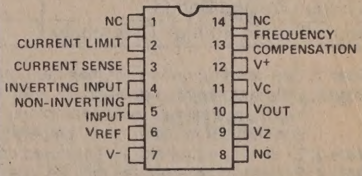
V+
8
FREQUENCY COMPENSATION
9
7
VC
TEMPERATURE COMPENSATED ZENER
VOLTAGE REFERENCE AMPLIFIER
4
VREF
INVERTING INPUT
2
−
ERROR AMPLIFIER
3
+
NON-INVERTING INPUT
SERIES PASS TRANSISTOR
6
VOUT
CURRENT LIMITER
VZ
5
V−
10
CURRENT LIMIT
1
CURRENT SENSE

*Pin numbers refer to metal can package.

ORDERING INFORMATION

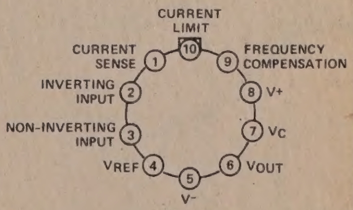
Part Number	TO-99 Can	14 Pin CERDIP	14 Pin Plastic DIP	Dice
μA723C μA723M	μA723HC μA723HM*	μA723DC μA723DM*	μA723PC	μA723C/D μA723M/D
* Add QB to order number if 883B processing is desired.				

PIN CONFIGURATIONS



NC 1
CURRENT LIMIT 2
CURRENT SENSE 3
INVERTING INPUT 4
NON-INVERTING INPUT 5
VREF 6
V− 7
14 NC
13 FREQUENCY COMPENSATION
12 V+
11 VC
10 VOUT
9 VZ
8 NC

(outline dwgs JD, PD)



CURRENT LIMIT 10
CURRENT SENSE 1
FREQUENCY COMPENSATION 9
INVERTING INPUT 2
8 V+
NON-INVERTING INPUT 3
7 VC
VREF 4
6 VOUT
5
V−

TOP VIEW

NOTE: Pin 5 connected to case.

(outline dwg TO-100)

ABSOLUTE MAXIMUM RATINGS

Pulse Voltage from V^+ to V^- (50 ms)	50V
Continuous Voltage from V^+ to V^-	40V
Input-Output Voltage Differential	40V
Maximum Amplifier Input Voltage (Either Input)	7.5V
Maximum Amplifier Input Voltage (Differential)	5V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation Metal Can (Note 1)	800 mW
Cavity DIP (Note 1)	900 mW
Molded DIP (Note 1)	660 mW
Operating Temperature Range µA723	−55°C to +125°C
µA723C	0°C to +70°C
Storage Temperature Range Metal Can	−65°C to +150°C
DIP	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	µA723 MIN	µA723 TYP	µA723 MAX	µA723C MIN	µA723C TYP	µA723C MAX	UNITS
Line Regulation	V_{IN} = 12V to V_{IN} = 15V		.01	0.1		.01	0.1	% V_{OUT}
	−55°C ≤ T_A ≤ +125°C			0.3				
	0°C ≤ T_A ≤ +70°C						0.3	
	V_{IN} = 12V to V_{IN} = 40V		.02	0.2		0.1	0.5	
Load Regulation	I_L = 1 mA to I_L = 50 mA		.03	0.15		.03	0.2	
	−55°C ≤ T_A ≤ +125°C			0.6				
	0°C ≤ T_A ≤ = +70°C						0.6	
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5µF		86			86		
Average Temperature Coefficient of Output Voltage	−55°C ≤ T_A ≤ +125°C		.002	.015				%/°C
	0°C ≤ T_A ≤ +70°C					.003	.015	
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20			20		µVrms
	BW = 100 Hz to 10 kHz, C_{REF} = 5µF		2.5			2.5		
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		1.3	3.5		1.3	4.0	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	
Input-Output Voltage Differential		3.0		38	3.0		38	

Note 1: See derating curves for maximum power rating above 25°C.

Note 2: Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 KΩ connected as shown in Figure 1. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

Note 3: L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

Note 4: Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.

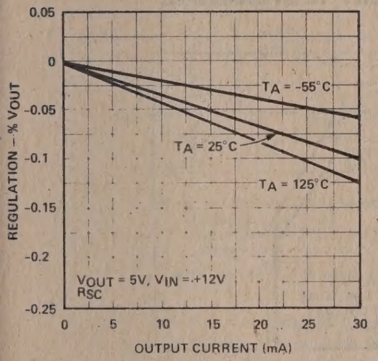
Note 5: Replace R1/R2 in figures with divider shown in Figure 13.

Note 6: V^+ must be connected to a +3V or greater supply.

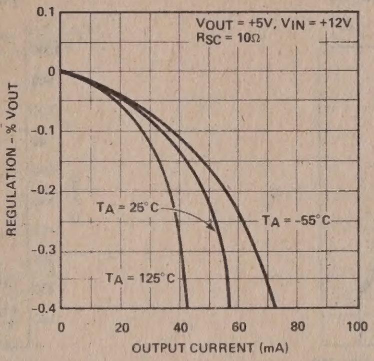
Note 7: For metal can applications where V_Z is required, an external 6.2 volt zener diode should be connected in series with V_{OUT}.

TYPICAL PERFORMANCE CHARACTERISTICS

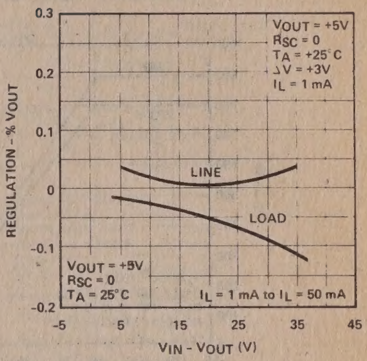
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



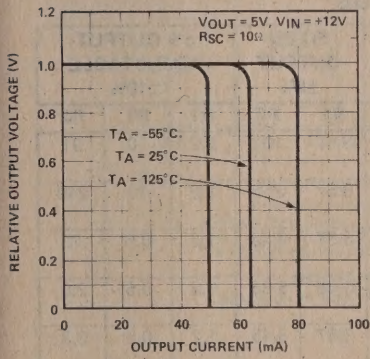
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



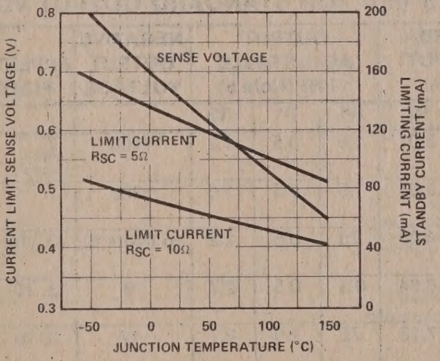
LOAD & LINE REGULATION VS INPUT-OUTPUT VOLTAGE DIFFERENTIAL



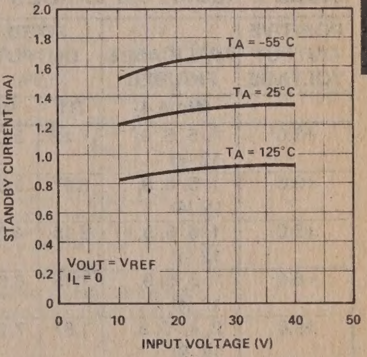
CURRENT LIMITING CHARACTERISTICS



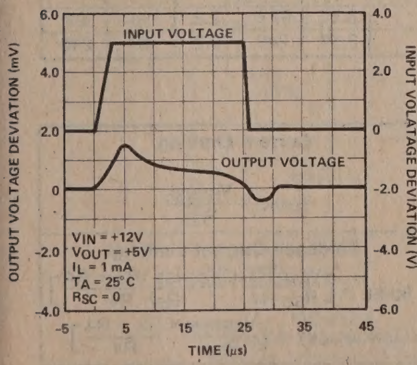
CURRENT LIMITING CHARACTERISTICS VS JUNCTION TEMPERATURE



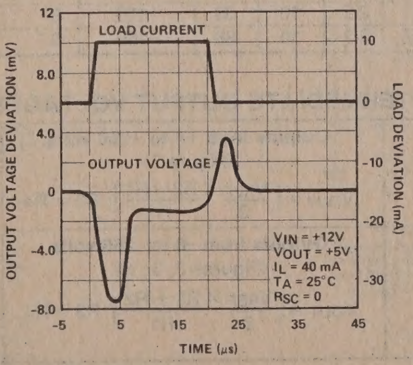
STANDBY CURRENT DRAIN VS INPUT VOLTAGE



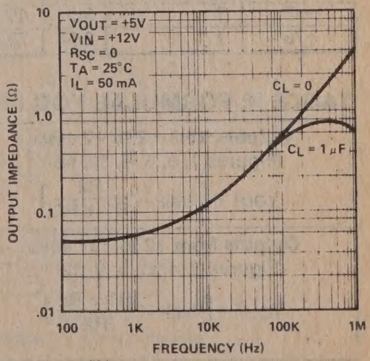
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE

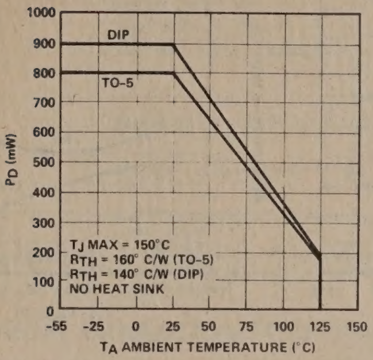


OUTPUT IMPEDANCE VS FREQUENCY



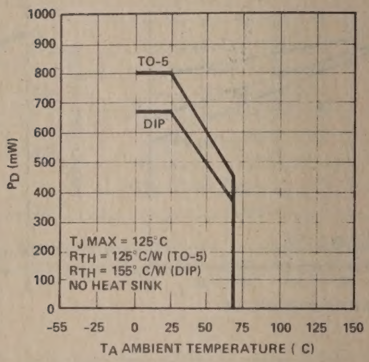
MAXIMUM POWER RATINGS

μA723
POWER DISSIPATION VS AMBIENT TEMPERATURE



TJ MAX = 150°C
RTH = 160° C/W (TO-5)
RTH = 140° C/W (DIP)
NO HEAT SINK

μA723C
POWER DISSIPATION VS AMBIENT TEMPERATURE



TJ MAX = 125°C
RTH = 125°C/W (TO-5)
RTH = 155° C/W (DIP)
NO HEAT SINK

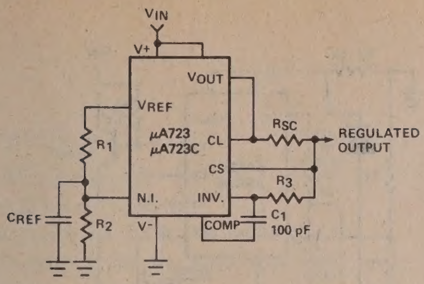
TABLE I: RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGE

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES (Note 4)	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
		R1	R2	R1	P1	R2			R1	R2	R1	P1	R2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (Note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II: FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts (Figures 1, 5, 6, 9, 12, (4)) $V_{OUT} = \left[V_{REF} \times \frac{R2}{R1 + R2}\right]$	**Outputs from +4 to +250 volts** (Figure 7) $V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R2 - R1}{R1}\right]$; $R3 = R4$	**Current Limiting** $I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$
Outputs from +7 to +37 volts (Figures 2, 4, (5, 6, 9, 12)) $V_{OUT} = \left[V_{REF} \times \frac{R1 + R2}{R2}\right]$	**Outputs from −6 to −250 volts** (Figures 3, 8, 10) $V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R1 + R2}{R1}\right]$; $R3 = R4$	**Foldback Current Limiting** $I_{KNEE} = \left[\frac{V_{OUT} R3}{R_{SC}\, R4} + \frac{V_{SENSE}\,(R3 + R4)}{R_{SC}\, R4}\right]$ $I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4}\right]$

TYPICAL APPLICATIONS

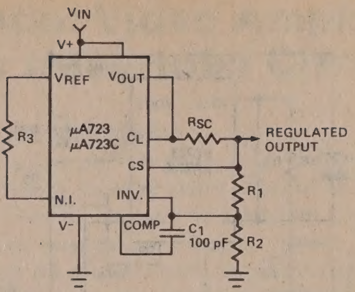

VIN
V+
VOUT
VREF
μA723
μA723C
CL
CS
N.I.
INV.
V−
COMP
R1
R2
R3
RSC
CREF
C1
100 pF
REGULATED OUTPUT

TYPICAL PERFORMANCE

Regulated Ouput Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

NOTE: $R_3 = \frac{R_1R_2}{R_1 + R_2}$ for minimum temperature drift.

FIGURE 1:
Basic Low Voltage Regulator
(V_{OUT} = 2 to 7 Volts)


VIN
V+
VREF
VOUT
μA723
μA723C
CL
CS
N.I.
INV.
V−
COMP
R3
RSC
R1
R2
C1
100 pF
REGULATED OUTPUT

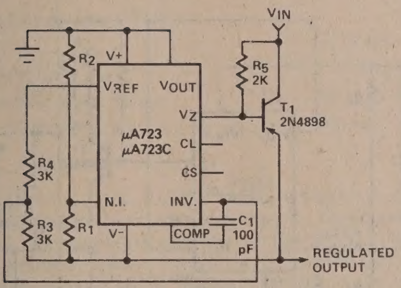
TYPICAL PERFORMANCE

Regulated Ouput Voltage	15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 50 mA)	4.5 mV

NOTE: $R_3 = \frac{R_1R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

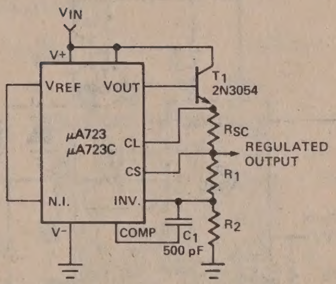
FIGURE 2:
Basic High Voltage Regulator
(V_{OUT} = 7 to 37 Volts)


VIN
R2
V+
VREF
VOUT
VZ
CL
CS
μA723
μA723C
N.I.
INV.
V−
COMP
R5
2K
T1
2N4898
R4
3K
R3
3K
R1
C1
100 pF
REGULATED OUTPUT

TYPICAL PERFORMANCE

Regulated Ouput Voltage	−15V
Line Regulation (ΔV_{IN} = 3V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

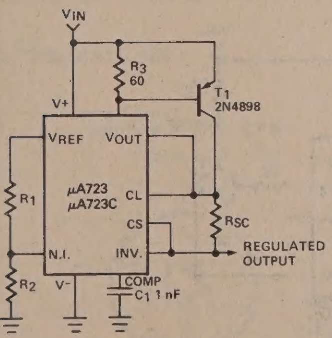
FIGURE 3:
Negative Voltage Regulator


VIN
V+
VREF
VOUT
T1
2N3054
μA723
μA723C
CL
CS
N.I.
INV.
V−
COMP
RSC
R1
R2
C1
500 pF
REGULATED OUTPUT

TYPICAL PERFORMANCE

Regulated Ouput Voltage	+15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 1A)	15 mV

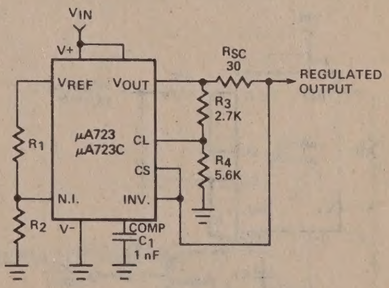
FIGURE 4:
Positive Voltage Regulator
(External NPN Pass Transistor)


VIN
R3
60
T1
2N4898
V+
VREF
VOUT
μA723
μA723C
CL
CS
N.I.
INV.
V−
COMP
R1
R2
RSC
C1 1 nF
REGULATED OUTPUT

TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 1A)	5 mV

FIGURE 5:
Positive Voltage Regulator
(External PNP Pass Transistor)

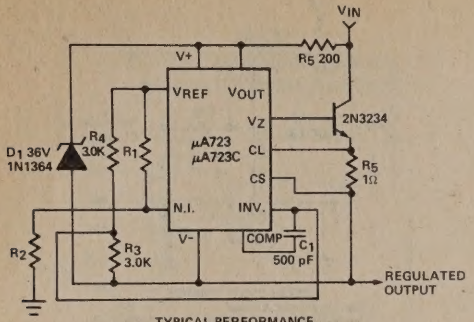

VIN
V+
RSC
30
VREF
VOUT
R3
2.7K
R4
5.6K
μA723
μA723C
CL
CS
N.I.
INV.
V−
COMP
R1
R2
C1
1 nF
REGULATED OUTPUT

TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Short Circuit Current	20 mA

FIGURE 6:
Foldback Current Limiting

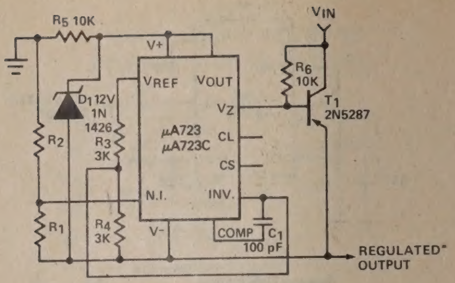
TYPICAL APPLICATIONS (CON'T.)


VIN
V+
R5 200
VREF
VOUT
VZ
2N3234
D1 36V
1N1364
R4
3.0K
R1
μA723
μA723C
CL
CS
R5
1Ω
N.I.
INV.
V-
COMP
C1
500 pF
R2
R3
3.0K
REGULATED
OUTPUT

TYPICAL PERFORMANCE

Regulated Output Voltage	+50V
Line Regulation (ΔV_{IN} = 20V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

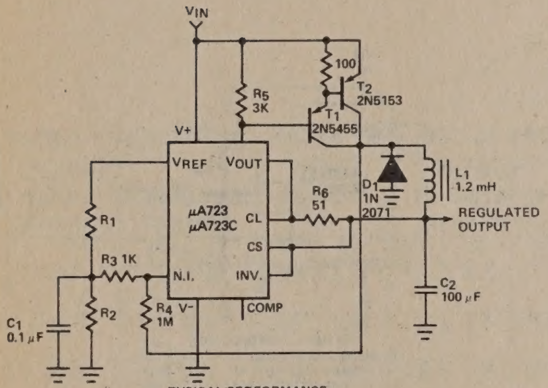
FIGURE 7:
Positive Floating Regulator


R5 10K
VIN
V+
R6
10K
VREF
VOUT
D1 12V
1N
1426
T1
2N5287
VZ
R2
R3
3K
μA723
μA723C
CL
CS
N.I.
INV.
R1
R4
3K
V-
COMP
C1
100 pF
REGULATED*
OUTPUT

TYPICAL PERFORMANCE

Regulated Output Voltage	-100V
Line Regulation (ΔV_{IN} = 20V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

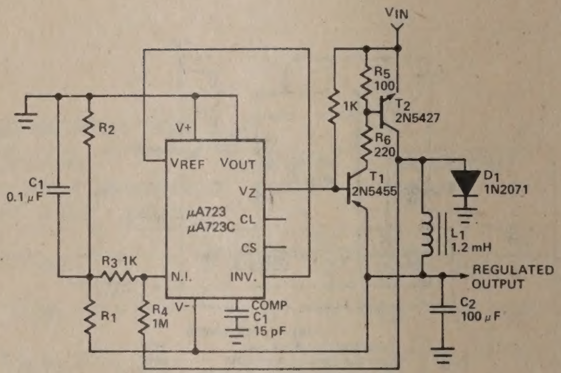
FIGURE 8:
Negative Floating Regulator


VIN
100
T2
2N5153
R5
3K
T1
2N5455
V+
VREF
VOUT
D1
1N
2071
L1
1.2 mH
R6
51
μA723
μA723C
CL
CS
REGULATED
OUTPUT
R1
R3 1K
N.I.
INV.
C2
100 μF
C1
0.1 μF
R2
R4
1M
V-
COMP

TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 30V)	10 mV
Load Regulation (ΔI_L = 2A)	80 mV

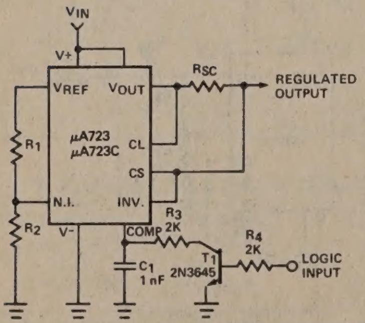
FIGURE 9:
Positive Switching Regulator


VIN
R5
100
1K
T2
2N5427
R2
V+
R6
220
VREF
VOUT
T1
2N5455
D1
1N2071
C1
0.1 μF
VZ
μA723
μA723C
CL
CS
L1
1.2 mH
R3 1K
N.I.
INV.
REGULATED
OUTPUT
R1
R4
1M
V-
COMP
C1
15 pF
C2
100 μF

TYPICAL PERFORMANCE

Regulated Output Voltage	-15V
Line Regulation (ΔV_{IN} = 20V)	8 mV
Load Regulation (ΔI_L = 2A)	6 mV

FIGURE 10:
Negative Switching Regulator

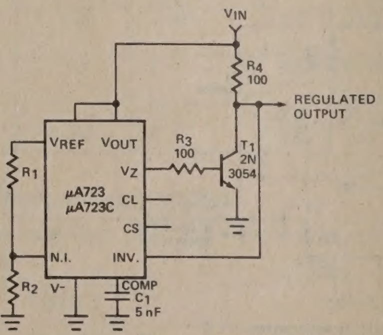

VIN
V+
RSC
VREF
VOUT
REGULATED
OUTPUT
R1
μA723
μA723C
CL
CS
N.I.
INV.
R3
2K
R2
V-
COMP
R4
2K
T1
2N3645
LOGIC
INPUT
C1
1 nF

NOTE: Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Ouput Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

FIGURE 11:
Remote Shutdown Regulator with Current Limiting


VIN
R4
100
REGULATED
OUTPUT
VREF
VOUT
R3
100
T1
2N
3054
R1
VZ
μA723
μA723C
CL
CS
N.I.
INV.
R2
V-
COMP
C1
5 nF

TYPICAL PERFORMANCE

Regulated Ouput Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

FIGURE 12:
Shunt Regulator

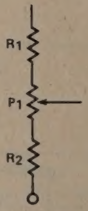


FIGURE 13:
Output Voltage Adjust (See Note 5)

INTERSIL

μA733

Differential Video Amplifier Linear Integrated Circuits

FEATURES

- 120 MHz Bandwidth
- 250 kΩ Input Resistance
- Selectable Gains of 10, 100, and 400
- No Frequency Compensation Required

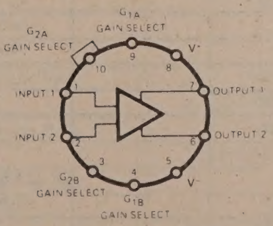
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation	
Metal Can	500 mW
Flatpak	570 mW
DIP	670 mW
Operating Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

10-LEAD METAL CAN
(TOP VIEW)



G_{1A} GAIN SELECT
G_{2A} GAIN SELECT
V+
INPUT 1
OUTPUT 1
INPUT 2
OUTPUT 2
G_{2B} GAIN SELECT
V−
G_{1B} GAIN SELECT
1
2
3
4
5
6
7
8
9
10

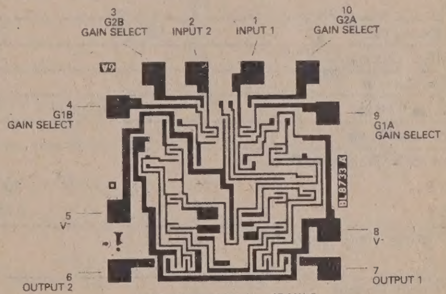
Note: Pin 5 connected to case.

(outline dwg TO-100)

GENERAL DESCRIPTION

The 733 is a monolithic two-stage Differential Input, Differential Output Video Amplifier. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories.

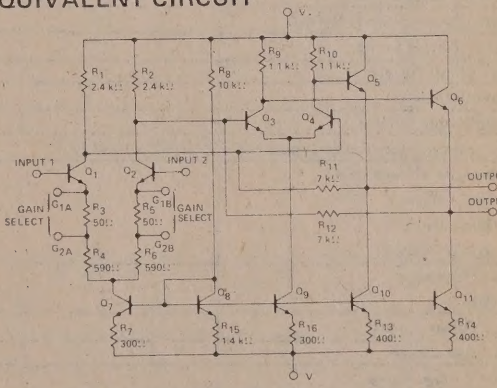
CHIP TOPOGRAPHY



3 G2B GAIN SELECT
2 INPUT 2
1 INPUT 1
10 G2A GAIN SELECT
4 G1B GAIN SELECT
9 G1A GAIN SELECT
5 V−
8 V+
6 OUTPUT 2
7 OUTPUT 1

CHIP DIMENSION 43 x 45 MILS

EQUIVALENT CIRCUIT



V+
R_1 2.4 kΩ
R_2 2.4 kΩ
R_8 10 kΩ
R_9 1.1 kΩ
R_{10} 1.1 kΩ
Q_5
Q_6
Q_3
Q_4
INPUT 1
Q_1
Q_2
INPUT 2
R_{11} 7 kΩ
OUTPUT 1
OUTPUT 2
R_{12} 7 kΩ
GAIN SELECT
G_{1A}
R_3 50Ω
R_5 50Ω
G_{1B}
GAIN SELECT
G_{2A}
R_4 590Ω
R_6 590Ω
G_{2B}
Q_7
Q_8
Q_9
Q_{10}
Q_{11}
R_7 300Ω
R_{15} 1.4 kΩ
R_{16} 300Ω
R_{13} 400Ω
R_{14} 400Ω
V−

ORDERING INFORMATION

Temp Range	Package	Order Number
Commercial	Dice TO-99	μA733C/D μA733HC
Military	Dice TO-99	μ733M/D μ733HM

733M ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±6.0 V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 1)		300	400	500	
Gain 2 (Note 2)		90	100	110	
Gain 3 (Note 3)		9.0	10	11	
Bandwidth	R_S = 50Ω				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		20	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	R_S = 50Ω, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f $\leqslant$ 100 kHz	60	86		dB
Gain 2	V_{CM} = ±1 V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV_S = ±0.5 V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$					
Differential Voltage Gain					
Gain 1 (Note 1)		200		600	
Gain 2 (Note 2)		80		120	
Gain 3 (Note 3)		8.0		12	
Input Resistance					
Gain 2		8.0			kΩ
Input Offset Current				5.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio		50			dB
Supply Voltage Rejection Ratio		50			dB
Output Offset Voltage					
Gain 1				1.5	V
Gain 2 and Gain 3				1.2	V
Output Swing		2.5			V_{p-p}
Output Sink Current		2.2			mA
Positive Supply Current				27	mA

Notes: 1. Pins G1A and G1B connected together.
2. Pins G2A and G2B connected together.
3. Gain select pins left open.

733C ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = ±6.0$ V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 1)		250	400	600	
Gain 2 (Note 2)		80	100	120	
Gain 3 (Note 3)		8.0	10	12	
Bandwidth	$R_S = 50\Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\Omega$, $V_{OUT} = 1\ V_{p-p}$				
Gain 1			10.5		ns
Gain 2			4.5	12	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\Omega$, $V_{OUT} = 1\ V_{p-p}$				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		10	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	5.0	μA
Input Bias Current			9.0	30	μA
Input Noise Voltage	$R_S = 50\Omega$, BW = 1 kHz to 10 MHz		12		μV_{rms}
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{CM} = ±1$ V, f ≤ 100 kHz	60	86		dB
Gain 2	$V_{CM} = ±1$ V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = ±0.5$ V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for $0°C \leq T_A \leq ±70°C$					
Differential Voltage Gain					
Gain 1 (Note 1)		250		600	
Gain 2 (Note 2)		80		120	
Gain 3 (Note 3)		8.0		12	
Input Resistance—Gain 2		8.0			kΩ
Input Offset Current				6.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{CM} = ±1$ V, f ≤ 100 kHz	50			dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = ±0.5$ V	50			dB
Output Offset Voltage (All Gain)				1.5	V
Output Voltage Swing		2.8			V_{p-p}
Output Sink Current		2.5			mA
Power Supply Current				27	mA

Notes:
1. Pins G1A and G1B connected together.
2. Pins G2A and G2B connected together.
3. Gain select pins left open.

INTERSIL

µA740
FET Input Operational Amplifier

FEATURES

- High input impedance. . . 1MΩ
- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- No latch up

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V+	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (740)	−55°C to +125°C
Commercial (740C)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

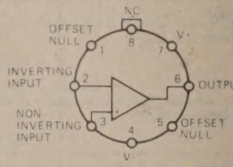
ORDERING INFORMATION

Temperature Range	Package	Order number
Commercial	Dice	µA740C/D
Military	Dice	µA740M/D
Commercial	TO-99 Can	µA740HC
Military	TO-99 Can	µ740HM

GENERAL DESCRIPTION

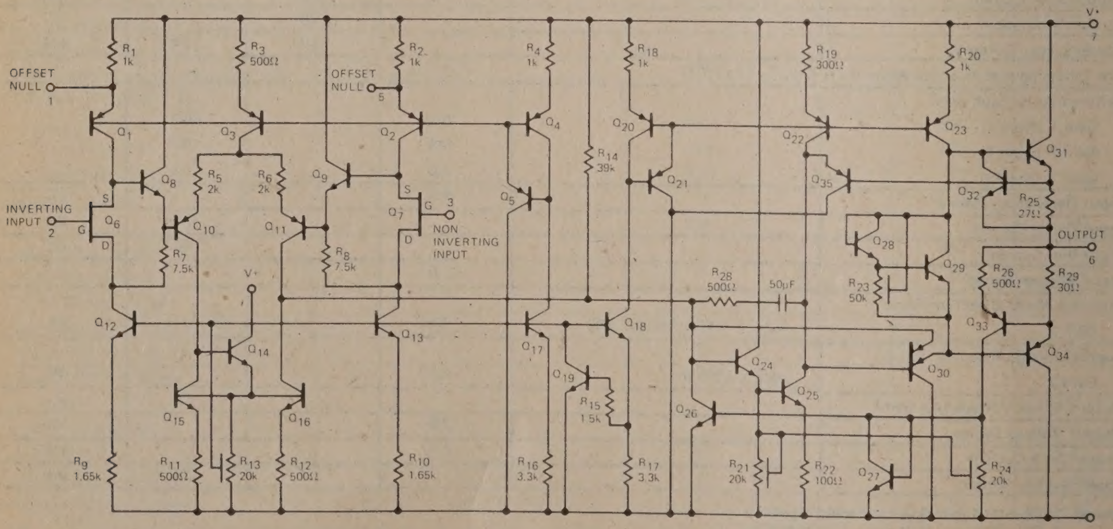
The 740 is a high performance. monolithic FET -Input Operational Amplifier epitaxial process. It is intended for a wide range of analog applications where very high input impedance is required and features very low input offset current and very low input bias current. High slew rate, high common mode voltage range and absence of "latch up" make the 740 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in active filters, integrators, summing amplifiers, sample and holds, transducer amplifiers, and other general feedback applications. The 740 is short circuit protected and has the same pin configuration as the 741 operational amplifier. No external components for frequency compensation are required as the internal 6 dB/octave roll-off insures stability in closed loop applications.

PIN CONFIGURATIONS
(outline dwg TO-99)


NC
8
OFFSET NULL
1
V+
7
INVERTING INPUT
2
6
OUTPUT
NON INVERTING INPUT
3
4
5
OFFSET NULL
V-

NOTE: Pin 4 Connected to Case.

EQUIVALENT CIRCUIT


V+
7
OFFSET NULL 1
OFFSET NULL 5
INVERTING INPUT 2
NON INVERTING INPUT
G 3
S
G
D
V+
OUTPUT
6
R1 1k
R3 500Ω
R2 1k
R4 1k
R18 1k
R19 300Ω
R20 1k
R14 39k
R5 2k
R6 2k
R7 7.5k
R8 7.5k
R25 27Ω
R28 500Ω
50pF
R23 50k
R26 500Ω
R29 30Ω
R15 1.5k
R9 1.65k
R11 500Ω
R13 20k
R12 500Ω
R10 1.65k
R16 3.3k
R17 3.3k
R21 20k
R22 100Ω
R24 20k
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35

740M

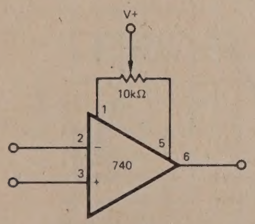
ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_C = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		$R_S \leq 100k\Omega$		10	20	mV
Input Offset Current (Note 4)				40	150	pA
Input Current (either input) (Note 4)				100	200	pA
Input Resistance				1		MΩ
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50,000	1		
Output Resistance				75		Ω
Output Short-Circuit Current				20		mA
Common Mode Rejection Ratio			64	80		dB
Supply Voltage Rejection Ratio				70	300	µV/V
Supply Current				4.2	5.2	mA
Power Consumption				126	156	mW
Slew Rate				6.0		V/µs
Unity Gain Bandwidth				3.0		MHz
Transient Response (Unity Gain)	Risetime	$C_L \leq 100pF$, $R_L = 2k\Omega$, V_{IN} = 100mV		110		ns
	Overshoot			10	20	%

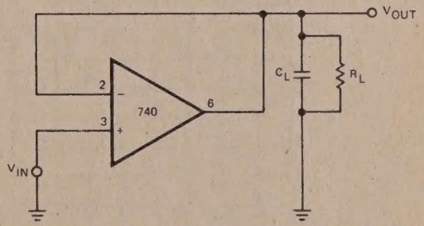
The following specifications apply for T_C = –55°C to +85°C:

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		±10		±12	V
Large Signal Voltage Gain		25,000			
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		V
Input Offset Voltage	$R_S \leq 100k\Omega$		15	30	mV
Input Offset Current	T_A = –55°C		30		pA
	T_A = +85°C		185		pA
Input Current (either input)	T_A = –55°C			200	pA
	T_A = +85°C		2.5	4.0	nA

VOLTAGE OFFSET
NULL CIRCUIT



TRANSIENT RESPONSE
TEST CIRCUIT



740C

ELECTRICAL CHARACTERISTICS ($V_S = \pm15V$, $T_C = 25°C$ unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 100k\Omega$		30	110	mV
Input Offset Current (Note 4)				60	300	pA
Input Current (either input) (Note 4)				0.1	2.0	nA
Input Resistance				1		MΩ
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	20,000	1		
Output Resistance				75		Ω
Output Short-Circuit Current				20		mA
Supply Current				4.2	8.0	mA
Power Consumption				126	240	mW
Slew Rate				6.0		V/μs
Unity Gain Bandwidth				1.0		MHz
Transient Response (Unity Gain)	Risetime	$C_L \leq 100pF$, $R_L = 2k\Omega$, $V_{IN} = 100mV$		300		ns
	Overshoot			10		%

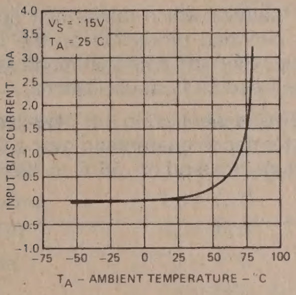
The following specifications apply for $0°C \leq T_A \leq +70°C$:

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		±10	±12		V
Common Mode Rejection Ratio		55	80		dB
Supply Voltage Rejection Ratio			70	500	μV/V
Large Signal Voltage Gain			500,000		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		V
Input Offset Voltage			30		mV
Input Offset Current			60		pA
Input Current (either input)			1.1	10	nA

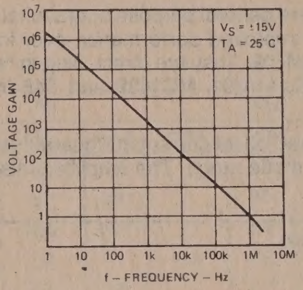
NOTE 1: Rating applies for ambient temperature to +70°C; derate linearly at 6.3mW/°C for ambient temperatures above +70°C.
NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 3: Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
NOTE 4: Typically doubles for every 10°C increase in ambient temperature.

TYPICAL PERFORMANCE CURVES FOR 740 AND 740C

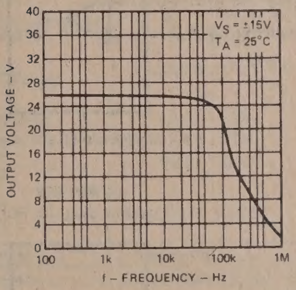
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



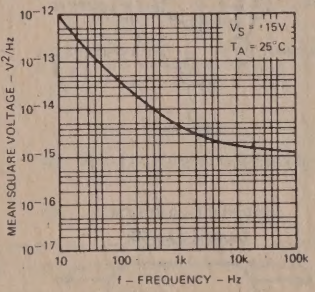
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



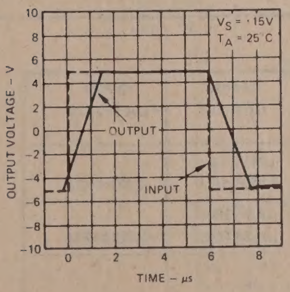
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



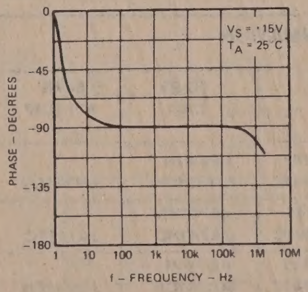
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



INTERSIL

741
Operational Amplifier

GENERAL DESCRIPTION

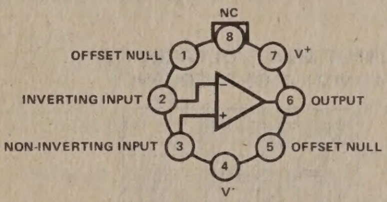
The 741 and 741C are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The offset voltage and offset current are guaranteed over the entire common mode range. The amplifiers also offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The 741C is identical to the 741 except that the 741C has its performance guaranteed over a 0°C to 70°C temperature range, instead of −55°C to 125°C.

PIN CONFIGURATIONS

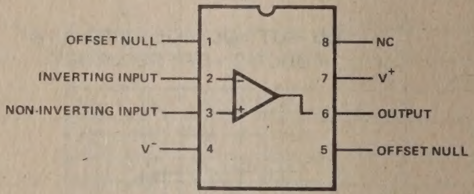
METAL CAN
(outline dwg TO-99)


NC
8
OFFSET NULL
1
7
V+
INVERTING INPUT
2
6
OUTPUT
NON-INVERTING INPUT
3
5
OFFSET NULL
4
V-

TOP VIEW

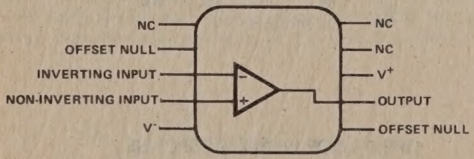
NOTE: PIN 4 CONNECTED TO CASE

8 PIN MINIDIP
(outline dwg PA)

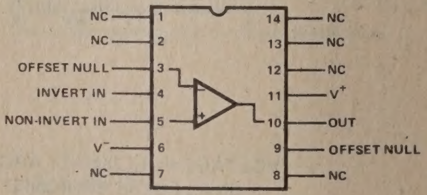

OFFSET NULL
1
8
NC
INVERTING INPUT
2
7
V+
NON-INVERTING INPUT
3
6
OUTPUT
V-
4
5
OFFSET NULL

NOTE: PIN 4 CONNECTED TO BOTTOM OF PACKAGE

10 PIN FLATPACK
(outline dwg FB)


NC
OFFSET NULL
INVERTING INPUT
NON-INVERTING INPUT
V-
NC
NC
V+
OUTPUT
OFFSET NULL

14 PIN DIP
(outline dwg, JD, PD)


NC
1
NC
2
OFFSET NULL
3
INVERT IN
4
NON-INVERT IN
5
V-
6
NC
7
14
NC
13
NC
12
NC
11
V+
10
OUT
9
OFFSET NULL
8
NC

ORDERING INFORMATION

	TO-99 CAN	8-PIN MINIDIP	14 PIN PLASTIC	14 PIN CERDIP	10 PIN FLATPACK
LM741	LM741H			LM741J	
LM741C	LM741CH	LM741CN	LM741CN-14	LM741CJ	LM741CJ
μA741	μA741HM			μA741DM	
μA741C	μA741HC	μA741TC	μA741PC	μA741DC	μA741FM
AD741	AD741H				
AD741C	AD741CH	AD741CN			
ICL741	ICL741MTY			ICL741MJD	ICL741MFB
ICL741C	ICL741CTY	ICL741CPA	ICL741CPD	ICL741CJD	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 741	±22V
741C	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration	Indefinite
Operating Temperature Range 741	—55°C to 125°C
741C	0°C to 70°C
Storage Temperature Range	—65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

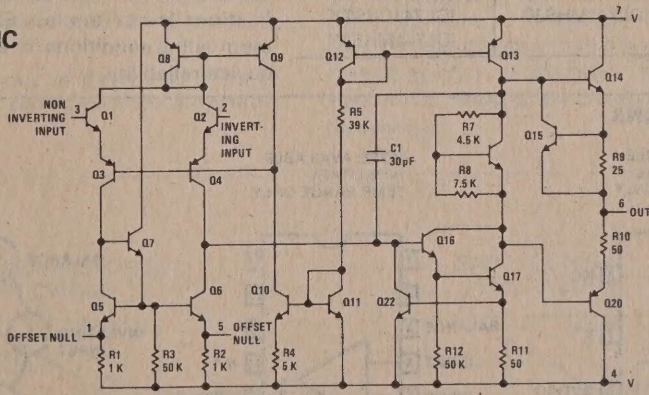
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	741			741C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$T_A = 25°C$, $R_S < 10\,k\Omega$		1.0	5.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		30	200		30	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		1.7	2.8		1.7	2.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L > 2\,k\Omega$	50	160		25	160		v/mV
Input Offset Voltage	$R_S < 10\,k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L > 2\,k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$ $R_L = 2\,k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S < 10\,k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S < 10\,k\Omega$	77	96		77	96		dB

Note 1: The maximum junction temperature of the 741 if 150°C, while that of the 741C is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to case.
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \le T_{AK} \le 125°C$, unless otherwise specified. With the 741C, however, all specifications are limited to $0°C \le T_A \le 70°C$ and $V_S = \pm 15V$.

EQUIVALENT SCHEMATIC



ICL741HS

High Speed 741 Operational Amplifier

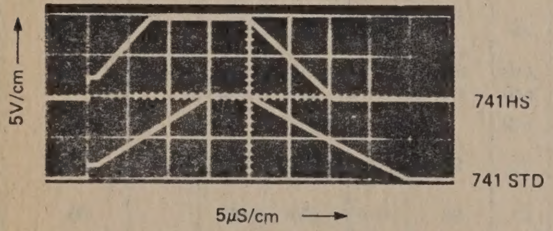
FEATURES

- Pin For Pin and Electrically Equivalent to μA741
- Guaranteed Slew Rate — 0.7V/μs Min.
- Low Cost
- Short Circuit Protection
- Large Common-Mode Input Range
- Guaranteed Drift Characteristics
- No Latch Up
- Internal Frequency Compensation

GENERAL DESCRIPTION

The 741HS high slew rate version of the 741 general purpose operational amplifier is intended for applications where slew rate performance greater than 0.3V/μsec is required. Typical applications are oscillators, active filters, sample and hold and other large signal applications. This device has a guaranteed minimum slew rate of 0.7V/μsec and is identical and equivalent to the standard 741 operational amplifier. It will fill the application void between the 741 and 101A type amplifiers (slew rate = 0.3V/μsec) and the more costly high-speed amplifiers (slew rate = 30V/μsec).

HIGH-SPEED 741 OPERATIONAL AMPLIFIER



ORDERING INFORMATION

8 Pin Plastic DIP	14 Pin CERDIP	TO-99 Can
ICL741CHSPA	ICL741MHSJD	ICL741CHSTY ICL741MHSTY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering at 60 sec.)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

NOTE 1: The maximum junction temperature of the 741HS is 150°C, while that of the 741CHS is 100°C. For operating at elevated temperatures devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the flat package, the derating is based on thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

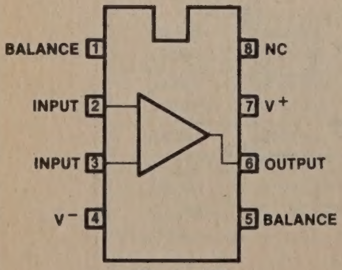
NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage. T_A = 25°C unless otherwise specified.

NOTE 3: Short circuit may be to ground or either supply.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

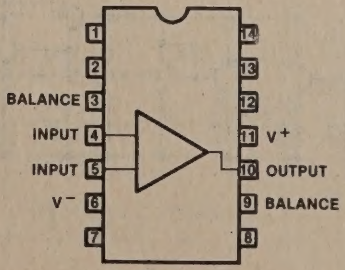
PIN CONFIGURATIONS

NOTE: AVAILABLE
IN COMMERCIAL
TEMP RANGE ONLY

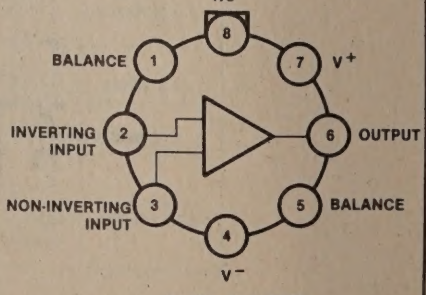


(outline dwg PA)

NOTE: AVAILABLE
IN MILITARY
TEMP RANGE ONLY



(outline dwg JD)



(outline dwg TO-99)

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	741CHS MIN	741CHS TYP	741CHS MAX	741MHS MIN	741MHS TYP	741MHS MAX	UNITS
Input Offset Voltage	$T_A = 25^\circ C$, $R_S \leq 50k\Omega$		2	6.0		1.0	5.0	mV
Input Offset Current	$T_A = 25^\circ C$		20	200		20	200	nA
Input Bias Current	$T_A = 25^\circ C$		200	500		200	500	nA
Input Resistance	$T_A = 25^\circ C$	0.3	2.0		0.3	1.0		MΩ
Supply Current	$T_A = 25^\circ C$, $V_S = \pm 15V$		1.7	2.8		1.7	2.8	mA
Large Signal Voltage Gain	$T_A = 25^\circ C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	25	160		50	160		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			7.5			6	mV
Slew Rate	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$ $C_L = 50pF$	0.7	1.0		0.7	1.0		V/μsec
Input Offset Current	$T_A = 25^\circ C$			300			500	nA
Input Bias Current				0.8			1.5	μA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	15			25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±14		±12	±14		V
	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	77	96		77	96		dB

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT OFFSET CURRENT: The difference in the currents into the two input terminals when the output is at zero.

INPUT VOLTAGE RANGE: The range of voltages on the input terminals for which the offset specifications apply.

INPUT BIAS CURRENT: The average of the two input currents.

COMMON MODE REJECTION RATIO: The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT RESISTANCE: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

SLEW RATE: A measure of the large signal capability of amplifier output to follow the amplifier input. Slew Rate = $2\pi \, BW_{\text{Large Signal}} \, V_{\text{O-Peak}}$.

SUPPLY CURRENT: The current required from the power supply to operate the amplifier with no load and the output at zero.

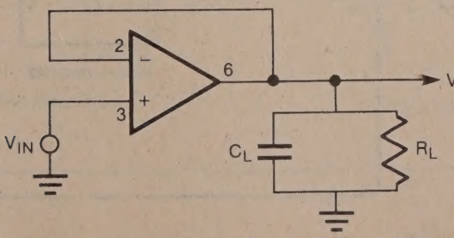
OUTPUT VOLTAGE SWING: The peak output voltage swing, referred to zero, that can be obtained without clipping.

LARGE-SIGNAL VOLTAGE GAIN: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

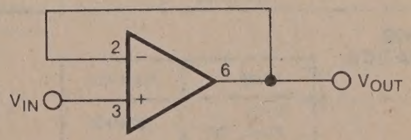
POWER SUPPLY REJECTION: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

TEST CIRCUITS

TRANSIENT RESPONSE
TEST CIRCUIT



FAST VOLTAGE
FOLLOWER



Power Bandwidth: 1.5kHz
Slew Rate: 1V/μs

AD741K
General Purpose Operational Amplifier High Accuracy

GENERAL DESCRIPTION

The AD741K is a high accuracy version of the popular 741 op amp. By setting maximum limits on voltage drift, and significantly reducing errors due to offset voltage, bias and offset currents, gain, PSRR, and CMRR, improvements in accuracy on the order of five times can be achieved over that delivered by a standard 741.

SPECIFICATIONS

(Typical @ +25°C and ±15VDC, unless otherwise specified)

Model	AD741K
Open Loop Gain	
R_L = 2k Ω, V_O = ±10V	
Over Temp Range, $T_{min/max}$,	50,000 min
same loads as above	
Output Characteristics	25,000 min
Voltage @ R_L = 2k Ω, $T_{min/max}$	±10V min
Short Circuit Current	25mA
Frequency Response	
Unity Gain, Small Signal	1MHz
Full Power Response	10kHz
Slew Rate, Unity Gain	0.5V/μsec
Input Offset Voltage	
Initial, R_S ≤ 10K Ω	2mV max
$T_{min/max}$	3mV max
Avg vs Temperature (untrim.)	15μV/°C max
vs Supply, $T_{min/max}$	15μV/V max
Input Offset Current	
Initial	10nA max
$T_{min/max}$	15nA max
Avg vs Temperature	0.2nA/°C max
Input Bias Current	
Initial	75nA max
$T_{min/max}$	120nA max
Avg vs Temperature	1.5nA/°C max
Input Impedance	
Differential	2M Ω
Input Voltage Range (Note 1)	
Differential, max safe	±30V
Common Mode, max safe	±15V
Common Mode Rejection	
$T_{min/max}$	90dB min
Power Supply	
Rated Performance	±15V
Operating	±(5 to 22)V
Current, Quiescent	2.8mA max
Temperature Range	
Operating, Rated Performance	0 to +70°C
Storage	−65°C to +150°C

ORDERING INFORMATION

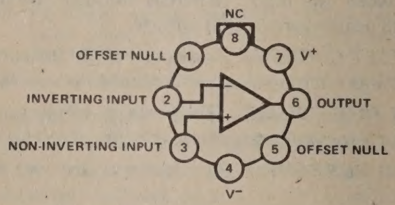
TO-99	AD741KH
8 Pin Plastic DIP	AD741KN

ABSOLUTE MAXIMUM RATINGS

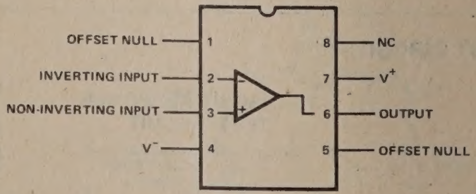
Supply Voltage	±22V
Power Dissipation	500mW
Differential Voltage	±30V
Input Voltage	±15V
Output Short Circuit Duration	indefinite
Operating Temp Range	0-70°C
Lead Temperature (soldering, 10 sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

PIN CONFIGURATIONS



NOTE: PIN 4 CONNECTED TO CASE
(outline dwg TO-99)



(outline dwg PA)

INTERSIL

ICL741LN, ICL741CLN, ICL101ALN ICL301ALN, ICL108LN, ICL308LN

Low Noise Operational Amplifiers

FEATURES

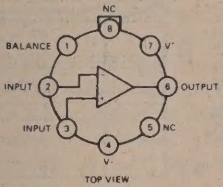
- Guaranteed Noise Specifications
- Complete Electrical Specifications

GENERAL DESCRIPTION

These low noise amplifiers are suitable for all applications where low level signals are encountered. The three important noise parameters, input referred voltage noise, input referred current noise, and popcorn noise, are all 100% screened and guaranteed.

PIN CONFIGURATIONS

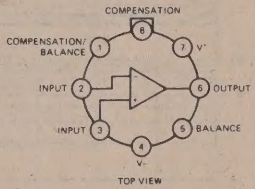
741/741C


NC
8
BALANCE
1
7
V+
INPUT
2
6
OUTPUT
INPUT
3
5
NC
4
V-
TOP VIEW

(outline dwg TO-99)

NOTE: PIN 4 CONNECTED TO CASE.

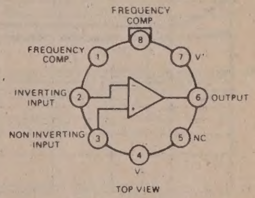
101A/301A


COMPENSATION
8
COMPENSATION/
BALANCE
1
7
V+
INPUT
2
6
OUTPUT
INPUT
3
5
BALANCE
4
V-
TOP VIEW

(outline dwg TO-99)

NOTE: PIN 4 CONNECTED TO CASE.

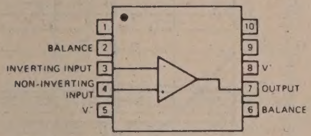
108/308


FREQUENCY
COMP.
8
FREQUENCY
COMP.
1
7
V+
INVERTING
INPUT
2
6
OUTPUT
NON INVERTING
INPUT
3
5
NC
4
V-
TOP VIEW

(outline dwg TO-99)

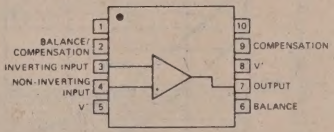
NOTE: PIN 4 CONNECTED TO CASE.

741


1
BALANCE
2
INVERTING INPUT
3
NON-INVERTING
INPUT
4
V-
5
10
9
8
V+
7
OUTPUT
6
BALANCE

(outline dwg FB-1)

101A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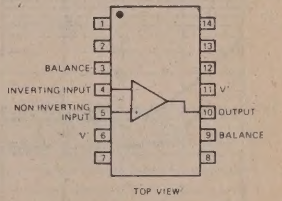
BALANCE/
COMPENSATION
2
INVERTING INPUT
3
NON-INVERTING
INPUT
4
V-
5
10
9
COMPENSATION
8
V+
7
OUTPUT
6
BALANCE

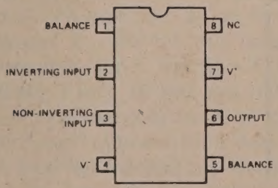
(outline dwg FB)

741


1
2
BALANCE
3
INVERTING INPUT
4
NON INVERTING
INPUT
5
V-
6
7
14
13
12
11
V+
10
OUTPUT
9
BALANCE
8
TOP VIEW

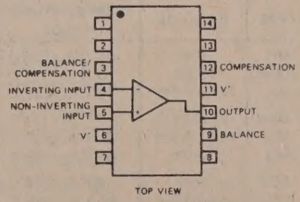
(outline dwg JD)

741C


BALANCE
1
INVERTING INPUT
2
NON-INVERTING
INPUT
3
V-
4
8
NC
7
V+
6
OUTPUT
5
BALANCE

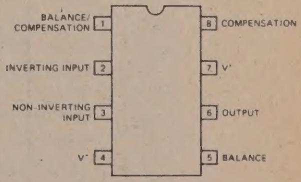
(outline dwg PA)

101A


1
2
BALANCE/
COMPENSATION
3
INVERTING INPUT
4
NON-INVERTING
INPUT
5
V-
6
7
14
13
12
COMPENSATION
11
V+
10
OUTPUT
9
BALANCE
8
TOP VIEW

(outline dwg JD)

301A


BALANCE/
COMPENSATION
1
INVERTING INPUT
2
NON-INVERTING
INPUT
3
V-
4
8
COMPENSATION
7
V+
6
OUTPUT
5
BALANCE

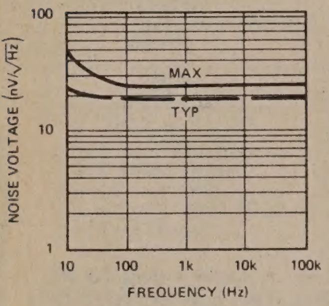
(outline dwg PA)

GUARANTEED NOISE SPECIFICATIONS ($T_A = 25^\circ C$)

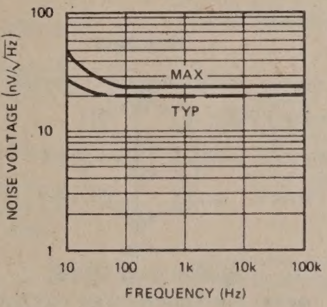
	741	741C	101A	301A	108	308	UNITS
Input Referred Voltage Noise @ 10 Hz (Max)	50	50	50	50	70	70	nV/√Hz
Input Referred Current Noise @ 10 Hz (Max)	0.4	0.4	0.7	0.7	0.2	0.2	pA/√Hz
Popcorn Noise Transition Amplitude for R_S = 100k (Max)	25	25	25	25	25	25	μV

For other electrical specifications see standard data sheets.

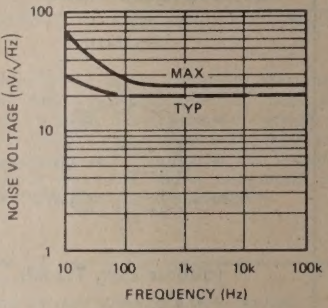
741 INPUT REFERRED VOLTAGE NOISE



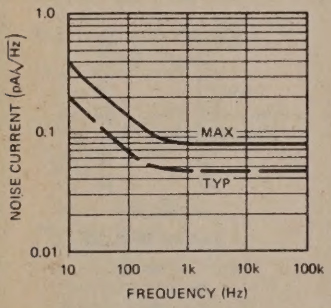
101A/301A INPUT REFERRED VOLTAGE NOISE



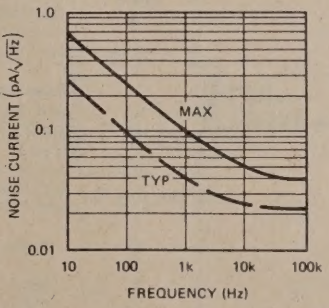
108/308 INPUT REFERRED VOLTAGE NOISE



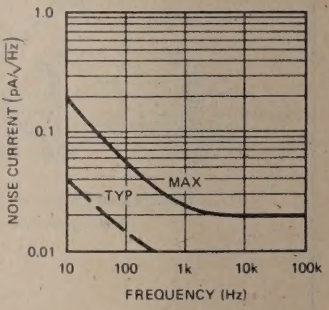
741 INPUT REFERRED CURRENT NOISE



101A/301A INPUT REFERRED CURRENT NOISE



108/308 INPUT REFERRED CURRENT NOISE



ORDERING INFORMATION

PART NUMBER	TYPE	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
741-LN	MIL	TO-99	-55°C to +125°C	ICL741LNTY
741C-LN	COM	TO-99	0°C to + 70°C	ICL741CLNTY
741-LN	MIL	14 Lead DIP	-55°C to +125°C	ICL741LNJD
741C-LN	COM	8 Lead DIP	0°C to + 70°C	ICL741CLNPA
741-LN	MIL	FLAT PACK	-55°C to +125°C	ICL741LNFB
101A-LN	MIL	TO-99	-55°C to +125°C	ICL101ALNTY
301A-LN	COM	TO-99	0°C to + 70°C	ICL301ALNTY
101A-LN	MIL	14 Lead DIP	-55°C to +125°C	ICL101ALNJD
301A-LN	COM	8 Lead DIP	0°C to + 70°C	ICL301ALNPA
101A-LN	MIL	FLAT PACK	-55°C to +125°C	ICL101ALNFB
108-LN	MIL	TO-99	-55°C to +125°C	ICL108LNTY
308-LN	COM	TO-99	0°C to + 70°C	ICL308LNTY

NOISE IN OPERATIONAL AMPLIFIERS

VOLTAGE NOISE: The noise due to the equivalent input voltage generator is measured using the circuit shown in Figure 1. It is expressed in nV/√Hz.

CURRENT NOISE: The noise due to the equivalent input current generator is measured using the circuit in Figure 2. It is expressed in pA/√Hz. Popcorn noise cannot be effectively screened using this test due to its erratic nature and very low frequency.

POPCORN NOISE: Popcorn noise, sometimes referred to as burst noise, is a low frequency noise phenomenon in which the output of the amplifier appears to jump erratically between two or more stable states. It is most noticeable when operating at high source impedances and is expressed as a transition amplitude, in µV, for a given source resistance. The test circuit of Figure 3 is used.

The noise of an amplifier may be expressed in terms of an input referred voltage generator (e_n) and an input referred current generator (i_n), see Figure 4. The total noise of an amplifier in a typical application contains contributions from both these generators, together with a contribution from the source resistance. The total mean square noise for a bandwidth of 1 Hz is given by:

$$e^2_T = e^2_n + i^2_n R^2_S + 4kTR_S \qquad (1)$$

Since both e_n and i_n are frequency dependent, the total mean square noise for a given bandwidth $\Delta f = f_2 - f_1$ is given by:

$$e^2_T = \int_{f_1}^{f_2} e^2_n \, df + R^2_S \int_{f_1}^{f_2} i^2_n \, df + 4kTR_S \, \Delta f \qquad (2)$$

With most amplifiers, the voltage noise term dominates for low source impedances. The current noise term is dominant at higher source impedances.

To specify operational amplifier noise performance one of two methods is used. One is to specify the total input referred noise for a given bandwidth and source impedance. This is defined as e_T from equation 1 above. The test circuit in Figure 5 is used. The typical broadband noise of the 741 and 101A type amplifier is shown in Figure 5.

The second method is to guarantee specific values of e_n and i_n (in equation 2) at various frequencies. A Noise Analyzer is used for this measurement (Figure 3). The values of e_n and i_n (for Δf = 1 Hz) are measured at 10 Hz, 100 Hz, 1 kHz, 10 kHz and 100 kHz. The recorded values may be plotted graphically, as shown on page 1. The noise information obtained from these measurements is considerably more general than that obtained from the first method, since the noise for any source impedance and bandwidth may be calculated from equation 2. (Graphical integration can determine the area under each curve.)

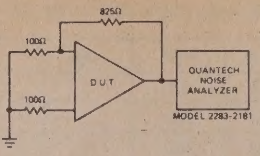


FIGURE 1.

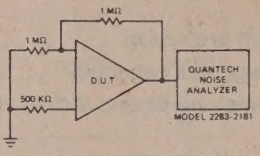


FIGURE 2.

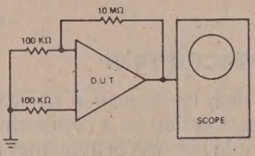


FIGURE 3.

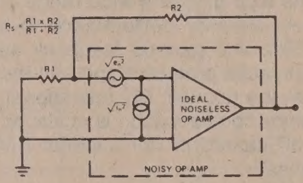


FIGURE 4.

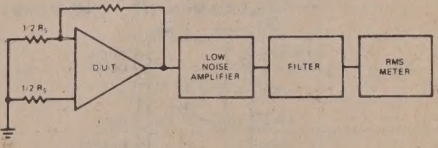


FIGURE 5.

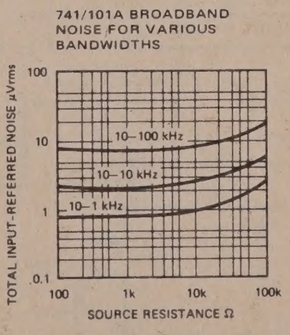

741/101A BROADBAND NOISE FOR VARIOUS BANDWIDTHS

FIGURE 6.

µA748
Operational Amplifier

FEATURES

- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch up

GENERAL DESCRIPTION

The 748 is a High Performance Monolithic Operational Amplifier and is intended for a high wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of latch-up make the 748 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The 748 is short-circuit protected and has the same pin configuration as the popular 741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. For superior performance, see 777 data sheet.

ABSOLUTE MAXIMUM RATINGS

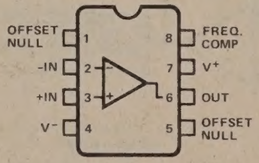
Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (748)	−55°C to +125°C
Commercial (748C)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can	300°C
Molded DIPs	260°C
Output Short Circuit Duration (Note 3)	Indefinite

NOTES:

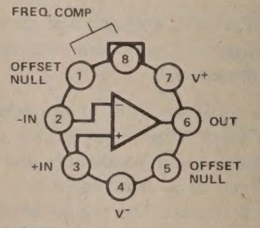
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can, 8.3 mW/°C for the DIP and 5.6 mW/°C for the mini DIP.
2. For supply voltages less than ±15V, absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PIN CONFIGURATIONS

8-LEAD MINI DIP (outline dwg PA)



8-LEAD METAL CAN (outline dwg TO-99)



NOTE: Pin 4 connected to case

ORDERING INFORMATION

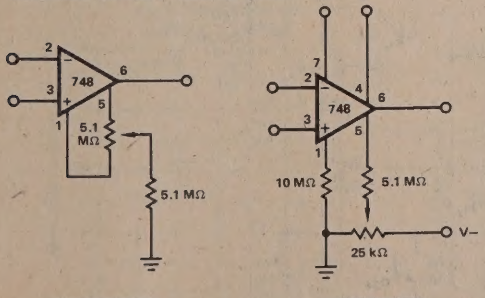
Part Number	Temperature Range	Package	Order Number
µA748C	0°C to +70°C	Dice	µA748C/D
		TO-99 can	µA748HC
		8 pin minidip	µA748TC
µA748M	−55°C to +125°C	Dice	µA748M/D
µA748HM		TO-99 can	µA748HM

(TOP VIEW)

748 ELECTRICAL CHARACTERISTICS ($V_S = \pm15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified)

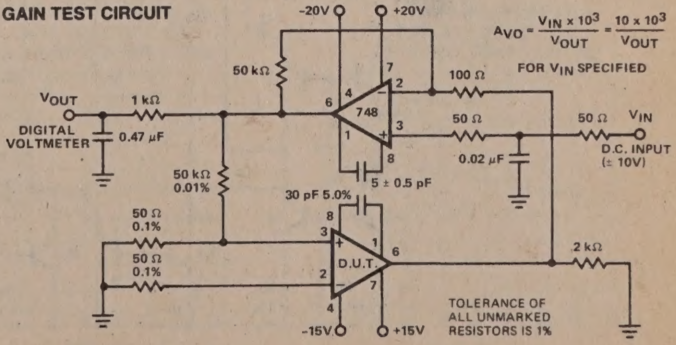
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			2.0		pF
Offset Voltage Adjustment Range			±15		mV
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm10$ V	50,000	150,000		V/V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response (Voltage Follower, Gain of 1) — Rise Time	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.3		μs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10) — Rise Time	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.2		μs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2$ kΩ, $C_C = 3.5$ pF		5.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		10	200	nA
	$T_A = -55°C$		50	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm10$ V	25,000			V/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5	mA
	$T_A = -55°C$		2.0	3.3	mA
Power Consumption	$T_A = +125°C$		45	75	mW
	$T_A = -55°C$		60	100	mW

VOLTAGE OFFSET NULL CIRCUIT


V+
V−
2
3
748
6
5
1
5.1 MΩ
5.1 MΩ
7
4
10 MΩ
25 kΩ
V−

SUGGESTED **ALTERNATE**

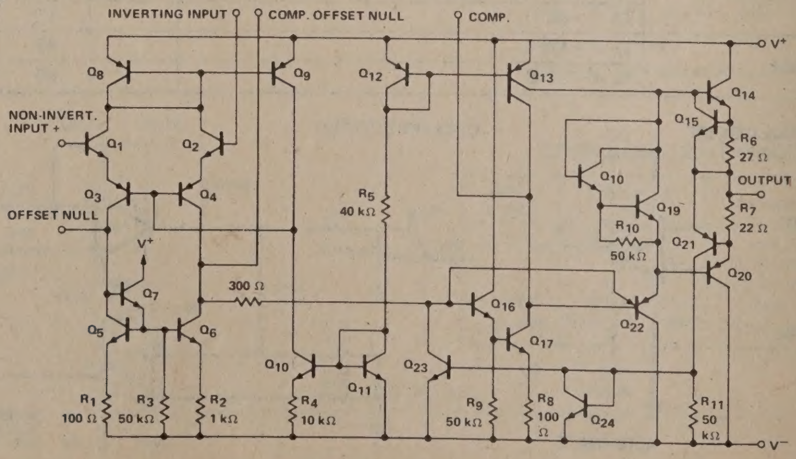
GAIN TEST CIRCUIT


−20V
+20V
AVO = VIN x 10³ / VOUT = 10 x 10³ / VOUT
FOR VIN SPECIFIED
50 kΩ
100 Ω
VOUT
1 kΩ
748
DIGITAL VOLTMETER
0.47 μF
50 Ω
VIN
D.C. INPUT (± 10V)
0.02 μF
5 ± 0.5 pF
50 kΩ 0.01%
30 pF 5.0%
50 Ω 0.1%
50 Ω 0.1%
D.U.T.
2 kΩ
−15V
+15V
TOLERANCE OF ALL UNMARKED RESISTORS IS 1%

748C ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified)

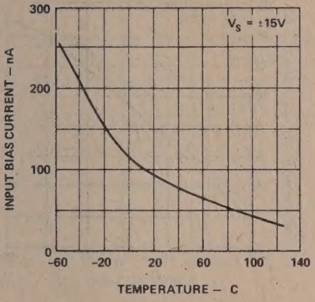
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			2.0		pF
Offset Voltage Adjustment Range			±15		mV
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10$ V	20,000	150,000		V/V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response (Voltage Follower, Gain of 1) Rise Time	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2\ k\Omega$, $C_L \leq 100$ pF		0.3		µs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2\ k\Omega$		0.5		V/µs
Transient Response (Voltage Follower, Gain of 10) Rise Time	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2\ k\Omega$, $C_L \leq 100$ pF		0.2		µs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2\ k\Omega$, $C_C = 3.5$ pF		5.5		V/µs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10\ k\Omega$			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150	µV/V
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10$ V	15,000			V/V
Output Voltage Swing	$R_L \leq 10\ k\Omega$	±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		V
Power Consumption			60	100	mW

EQUIVALENT CIRCUIT

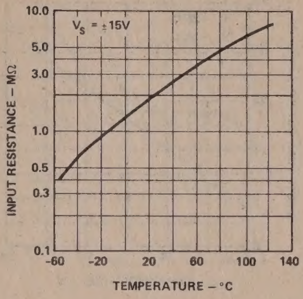

INVERTING INPUT
COMP. OFFSET NULL
COMP.
V+
Q8
Q9
Q12
Q13
Q14
NON-INVERT. INPUT +
Q1
Q2
Q15
R6 27 Ω
Q18
OUTPUT
Q3
Q4
R5 40 kΩ
Q19
R7 22 Ω
OFFSET NULL
R10 50 kΩ
Q21
V+
Q7
300 Ω
Q20
Q16
Q22
Q5
Q6
Q17
Q10
Q23
Q11
R1 100 Ω
R3 50 kΩ
R2 1 kΩ
R4 10 kΩ
R9 50 kΩ
R8 100 Ω
Q24
R11 50 kΩ
V−

TYPICAL PERFORMANCE CURVES FOR 748

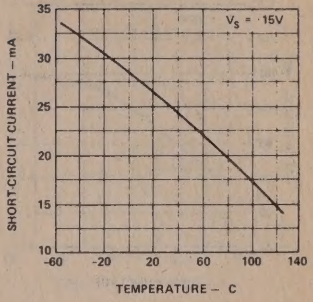
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



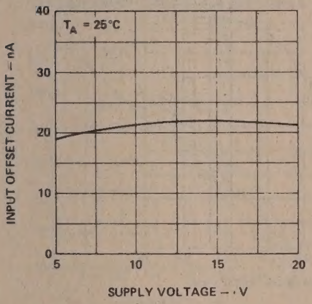
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



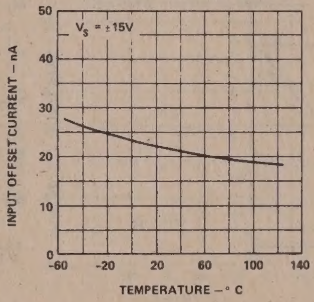
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



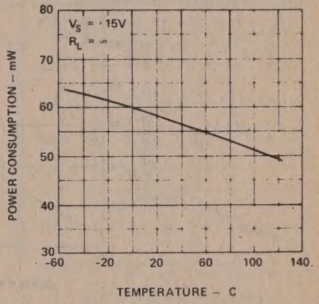
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

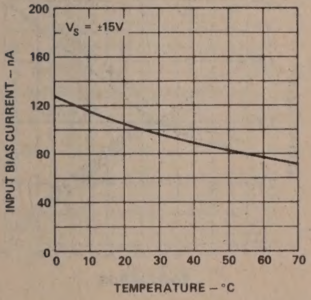


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

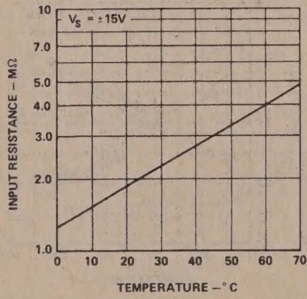


TYPICAL PERFORMANCE CURVES FOR 748C

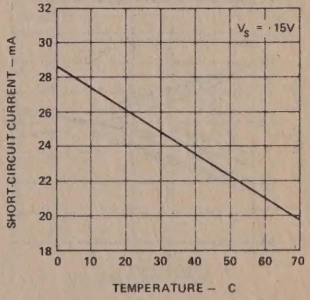
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



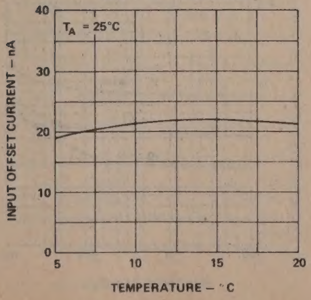
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



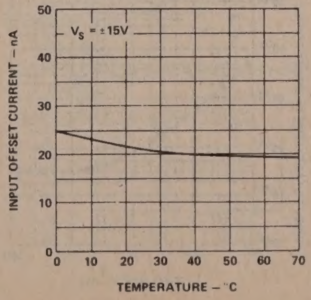
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



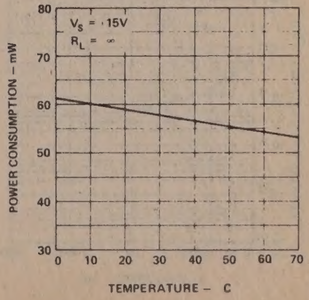
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

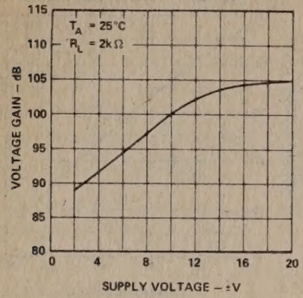


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

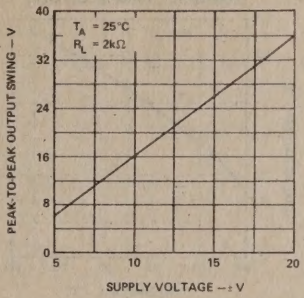


TYPICAL PERFORMANCE CURVES FOR 748 AND 748C

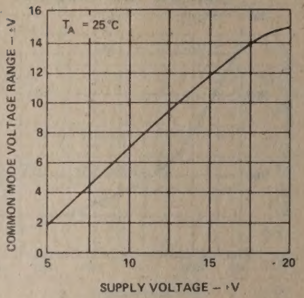
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



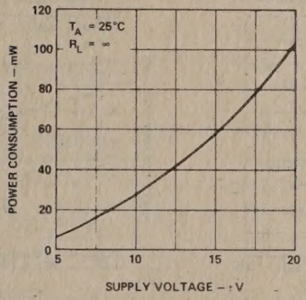
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



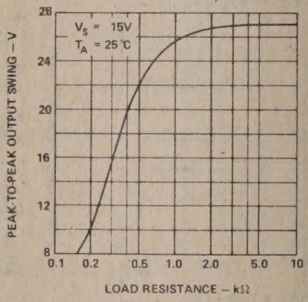
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



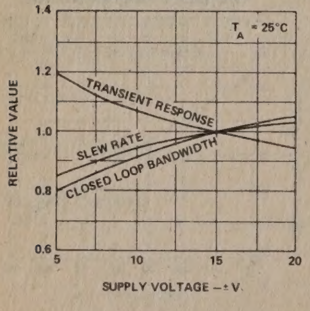
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



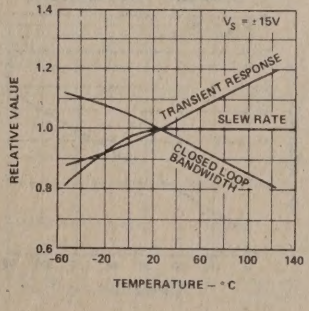
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



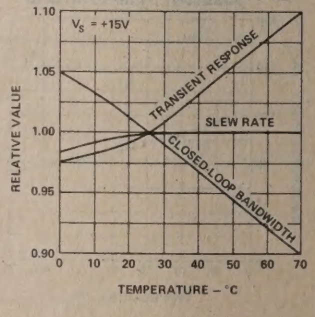
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



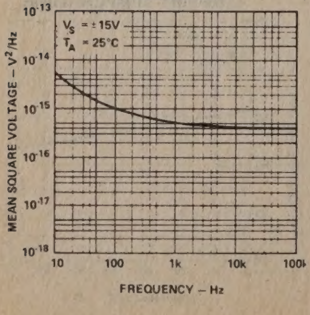
748 FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



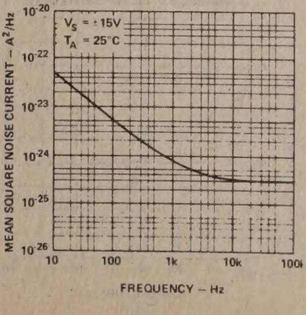
748C FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



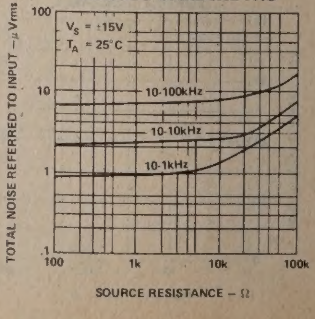
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

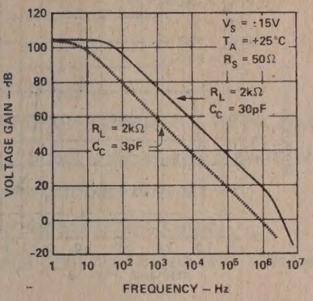


BROAD BAND NOISE FOR VARIOUS BANDWIDTHS

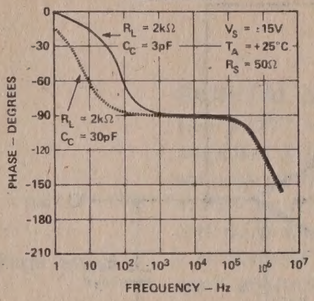


TYPICAL PERFORMANCE CURVES FOR 748 AND 748C

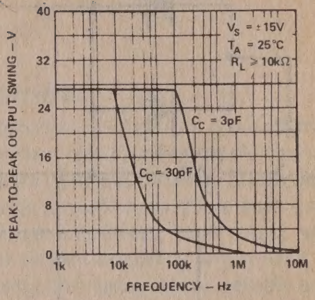
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



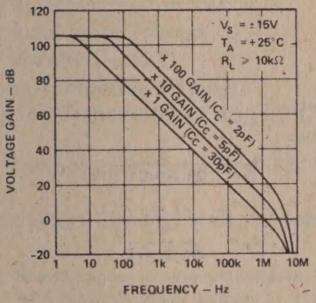
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



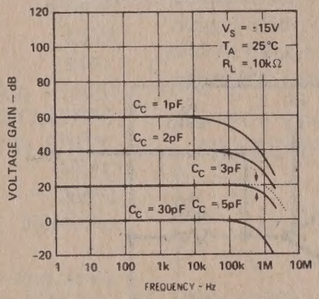
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



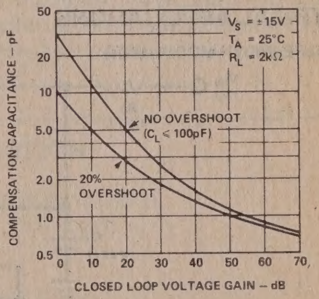
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



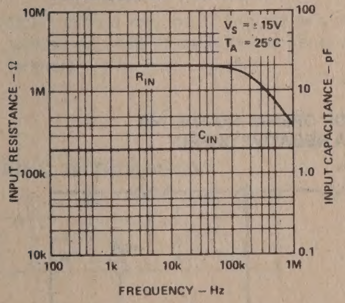
FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



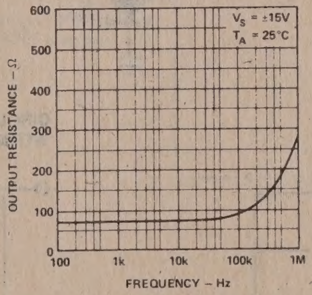
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



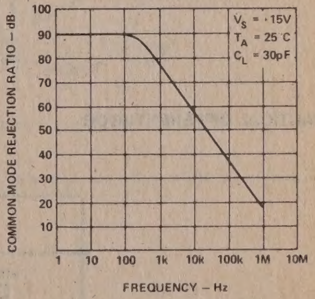
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



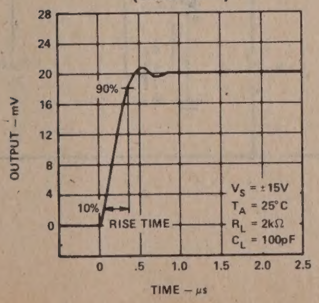
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



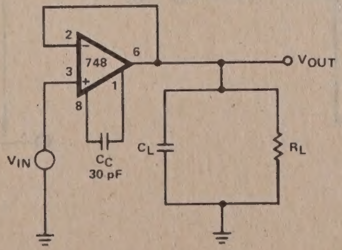
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



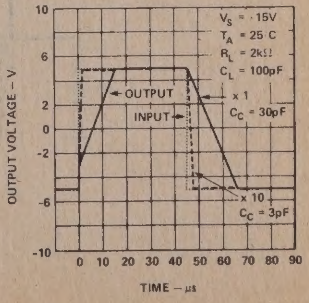
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

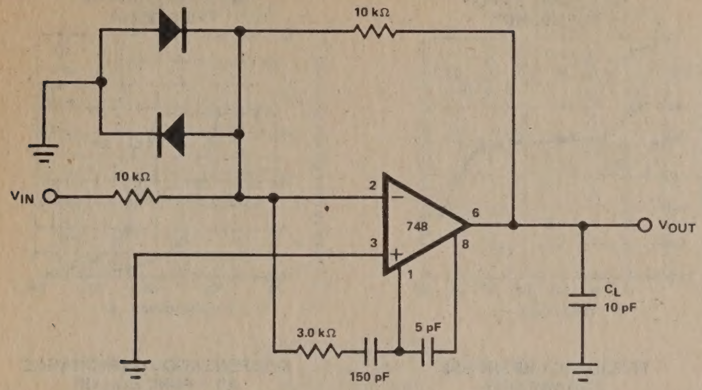


VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

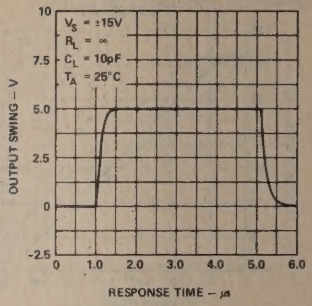


TYPICAL PERFORMANCE CURVES

FEED FORWARD COMPENSATION

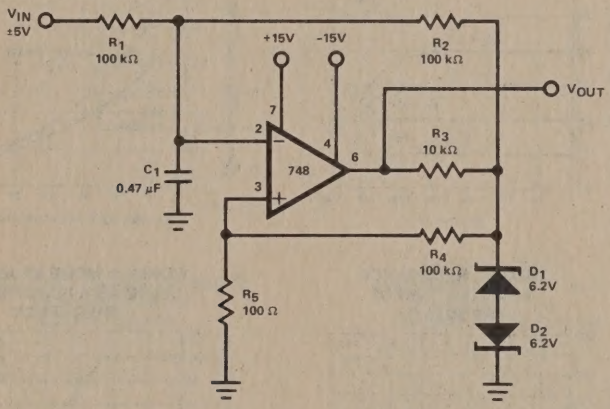

10 kΩ
10 kΩ
VIN
2
3
748
6
8
1
VOUT
CL
10 pF
3.0 kΩ
150 pF
5 pF

LARGE SIGNAL FEED FORWARD TRANSIENT RESPONSE



TYPICAL APPLICATIONS

PULSE WIDTH MODULATOR


VIN
±5V
R1
100 kΩ
+15V
-15V
R2
100 kΩ
VOUT
7
2
4
6
748
3
C1
0.47 µF
R3
10 kΩ
R4
100 kΩ
R5
100 Ω
D1
6.2V
D2
6.2V

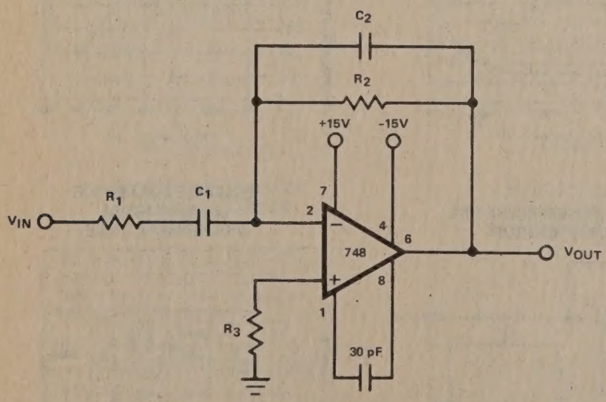
$$f_c = \frac{1}{2\pi\ R_2\ C1}$$

$$f_n = \frac{1}{2\pi\ R_1\ C1}$$

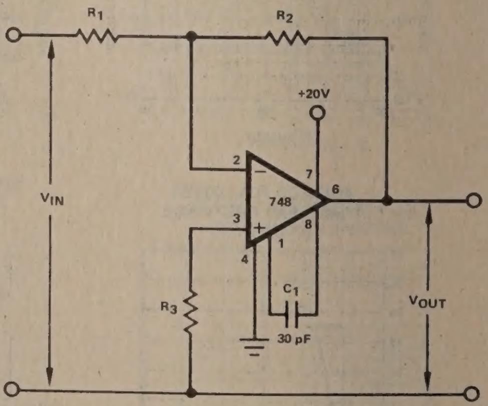
$$= \frac{1}{2\pi\ R_2\ C2}$$

$f_c < f_n < f_{\text{unity gain}}$

PRACTICAL DIFFERENTIATOR


C2
R2
+15V
-15V
R1
C1
VIN
7
2
4
6
748
8
1
R3
30 pF
VOUT

CIRCUIT FOR OPERATING THE 748 WITHOUT A NEGATIVE SUPPLY


R1
R2
+20V
2
7
6
748
3
8
1
4
VIN
R3
C1
30 pF
VOUT

INTERSIL

μA777
Precision Operational Amplifier

FEATURES

- **Low offset voltage and offset current**
- **Low offset voltage and current drift**
- **Low input bias current**
- **Low input noise voltage**
- **Large common mode and differential voltage ranges**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	
Metal Can	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range (HC)	0°C to 70°C
(HM)	−55°C to +125°C
Lead Temperature (Soldering, 10s)	300°C
	260°C
Output Short Circuit Duration (Note 3)	Indefinite

Note 1: Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for Metal Can, 8.3mW/°C for the DIP, and 5.6mW/°C for the Mini DIP.

Note 2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3. Short Circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for $I_{SET} \leq 30\mu A$.

ORDERING INFORMATION

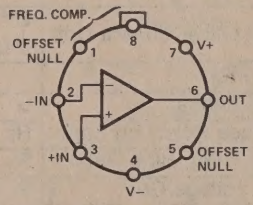
	Dice	TO-99 Can
μA777C	μA777C/D	μA777HC
μA777M	μA777M/D	μA777MC

GENERAL DESCRIPTION

The μA777 is a monolithic Precision Operational Amplifier. It is an excellent choice when performance versus cost trade-offs are possible between super beta or FET input operational amplifiers and low cost general purpose operational amplifiers. Low offset and bias currents improve system accuracy when used in applications such as long term integrators, sample and hold circuits and high source impedance summing amplifiers. Even though the input bias current is extremely low, the μA777 maintains full ±30V differential voltage range. High common mode input voltage range, latch-up protection, short circuit protection and simple frequency compensation make the device versatile and easily used.

PIN CONFIGURATION

8-LEAD METAL CAN
(TOP VIEW)

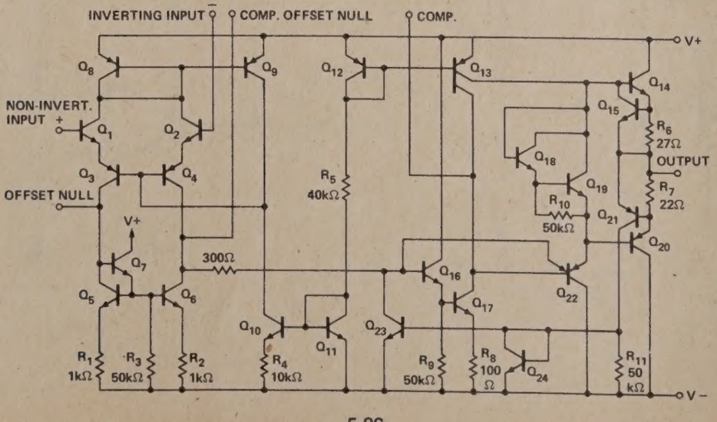


(outline dwg TO-99)

ELECTRICAL CHARACTERISTICS FOR μA777 ($V_S = \pm15V$, $T_A = 25°C$, $C_C = 30pF$ unless otherwise specified)

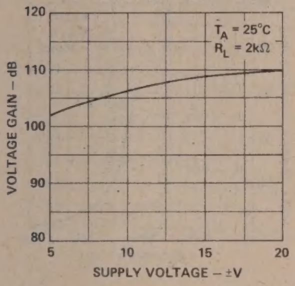
PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50k\Omega$		0.7	5.0	mV
Input Offset Current				0.7	20.0	nA
Input Bias Current				25	100	nA
Input Resistance			1.0	2.0		MΩ
Input Capacitance				3.0		pF
Offset Voltage Adjustment Range				±25		mV
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	25,000	250,000		V/V
Output Resistance				100		Ω
Output Short Circuit Current				±25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	$V_{IN} = 20mV$, $C_C = 30pF$ $R_L = 2k\Omega$, $C_L \leq 100pF$		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2k\Omega$		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	$V^{IN} = 20mV$, $C_C = 3.5pF$ $R_L = 2k\Omega$, $C_L \leq 100pF$		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \leq 2k\Omega$, $C_C = 3.5pF$		5.5		V/μs
The following specifications apply over operating temperature range.						
Input Offset Voltage		$R_S \leq 50k\Omega$		0.8	5.0	mV
Average Input Offset Voltage Drift		$R_S \leq 50k\Omega$		4.0	30	μV/°C
Input Offset Current					40	nA
Average Input Offset Current Drift		$25°C \leq T_A \leq +70°C$		0.01	10.3	nA/°C
		$0°C \leq T_A \leq +25°C$		0.02	0.6	nA/°C
Input Bias Current					200	nA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 50k\Omega$	70	95		dB
Supply Voltage Rejection Ratio		$R_S \leq 50k\Omega$		15	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	15,000			V/V
Output Voltage Swing		$R_L \geq 10k\Omega$	±12	±14		V
		$R_L \geq 2k\Omega$	±10	±13		V
Power Consumption				60	100	mW

EQUIVALENT CIRCUIT

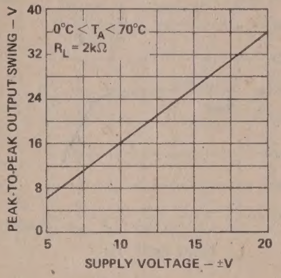

INVERTING INPUT
COMP. OFFSET NULL
COMP.
V+
Q8
Q9
Q12
Q13
Q14
NON-INVERT. INPUT +
Q1
Q2
Q15
R6 27Ω
OUTPUT
Q18
Q3
Q4
R5 40kΩ
Q19
R7 22Ω
OFFSET NULL
R10 50kΩ
Q21
V+
Q20
Q7
300Ω
Q16
Q22
Q5
Q6
Q17
Q10
Q11
Q23
R1 1kΩ
R3 50kΩ
R2 1kΩ
R4 10kΩ
R9 50kΩ
R8 100 Ω
Q24
R11 50 kΩ
V−

TYPICAL PERFORMANCE CURVES

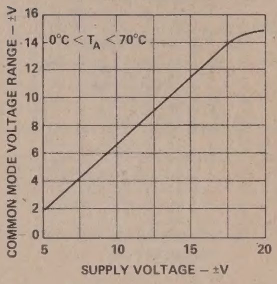
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



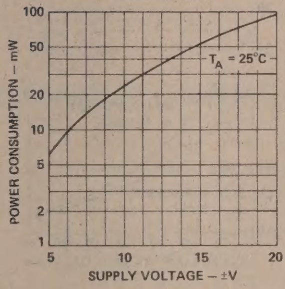
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



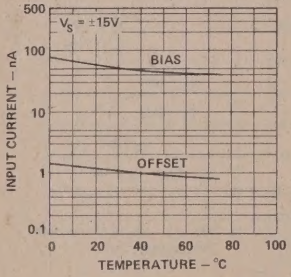
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



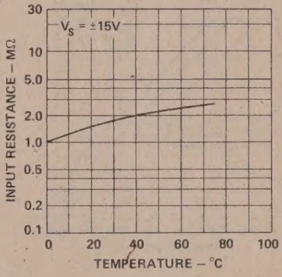
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



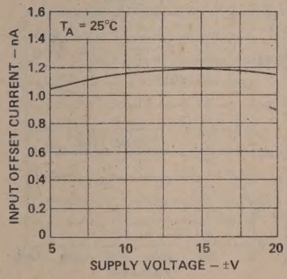
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



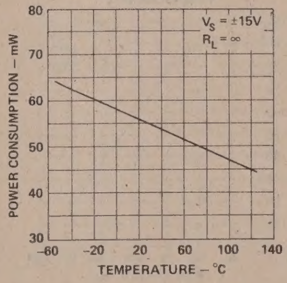
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



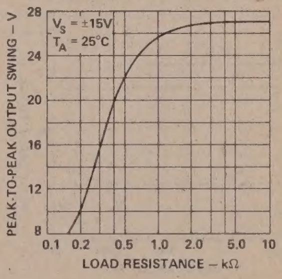
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



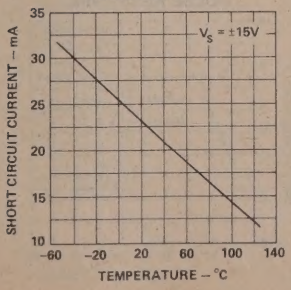
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



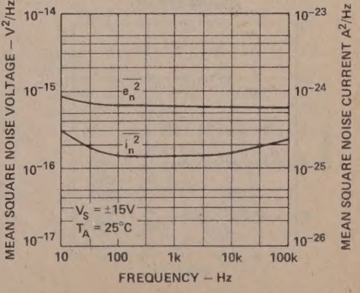
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

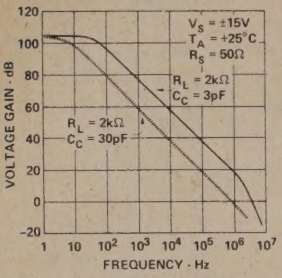


INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY

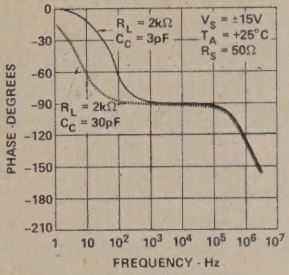


TYPICAL PERFORMANCE CURVES

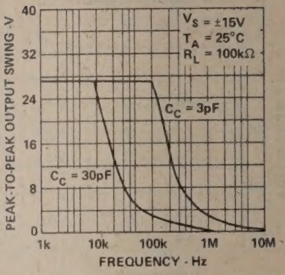
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



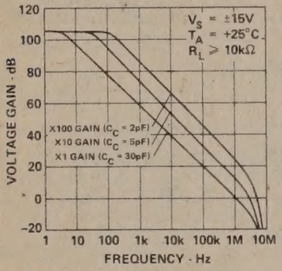
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



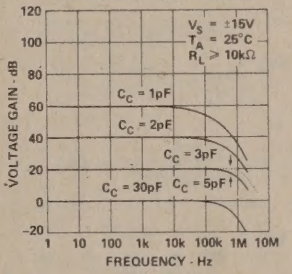
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



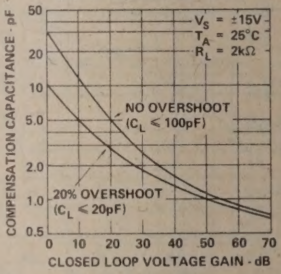
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



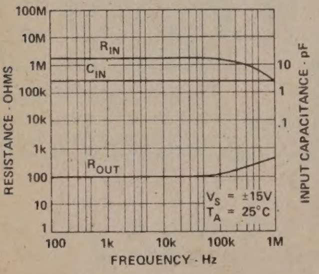
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



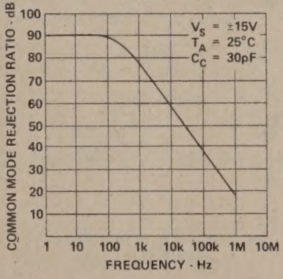
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



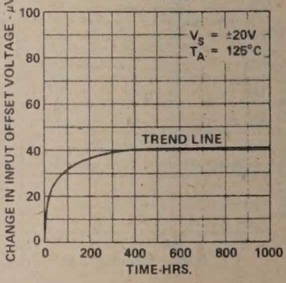
INPUT RESISTANCE, OUTPUT RESISTANCE, AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



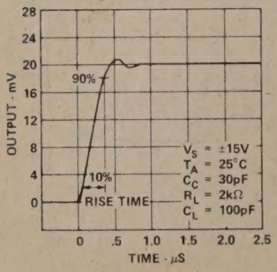
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



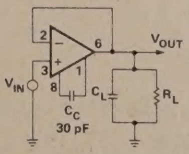
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



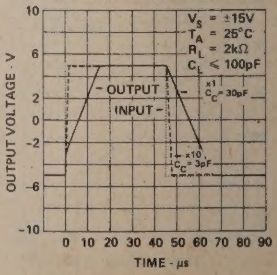
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

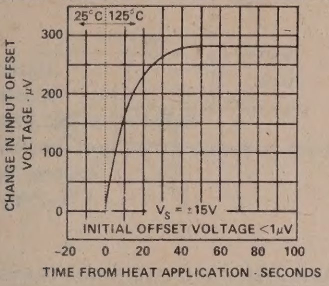


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

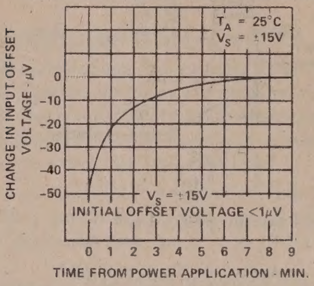


TYPICAL PERFORMANCE CURVES

THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE

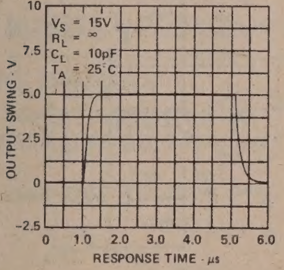


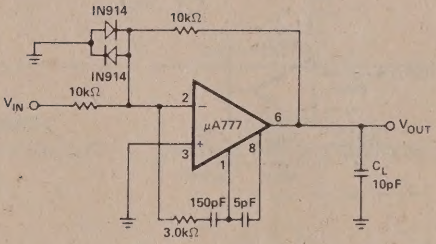
STABILIZATION TIME OF INPUT OFF—SET VOLTAGE FROM POWER TURN-ON



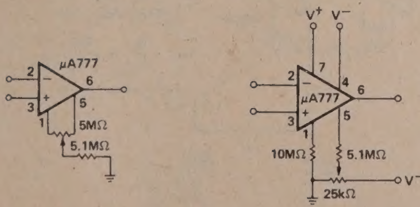
FEED FORWARD COMPENSATION

LARGE SIGNAL FEEDFORWARD TRANSIENT RESPONSE




IN914
10kΩ
IN914
10kΩ
V_{IN}
2
3
μA777
6
8
1
V_{OUT}
C_L
10pF
150pF
5pF
3.0kΩ

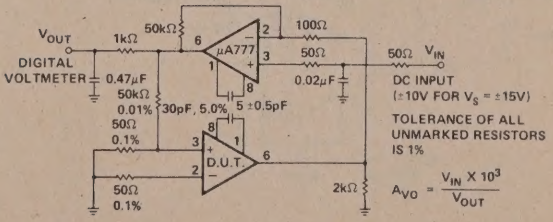
VOLTAGE OFFSET NULL CIRCUIT


μA777
2
3
6
1
5
5MΩ
5.1MΩ
V+
V−
7
4
μA777
6
5
1
10MΩ
5.1MΩ
25kΩ
V−

SUGGESTED

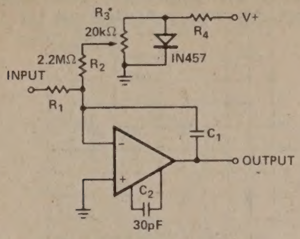
ALTERNATE

GAIN TEST CIRCUIT


V_{OUT}
DIGITAL VOLTMETER
1kΩ
50kΩ
0.47μF
50kΩ
0.01%
30pF, 5.0%
5 ±0.5pF
50Ω
0.1%
50Ω
0.1%
6
μA777
2
3
1
8
100Ω
50Ω
0.02μF
50Ω
V_{IN}
8
1
3
2
D.U.T.
6
2kΩ
DC INPUT
(±10V FOR V_S = ±15V)
TOLERANCE OF ALL UNMARKED RESISTORS IS 1%
$A_{VO} = \frac{V_{IN} \times 10^3}{V_{OUT}}$

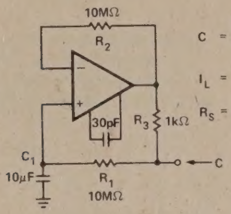
TYPICAL APPLICATIONS

BIAS COMPENSATED LONG TIME INTEGRATOR


R3*
20kΩ
V+
R4
IN457
2.2MΩ
R2
INPUT
R1
C1
OUTPUT
C2
30pF

*ADJUST R_3 FOR MINIMUM INTEGRATOR DRIFT

CAPACITANCE MULTIPLIER

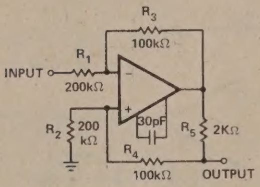

10MΩ
R2
30pF
R3
1kΩ
C1
10μF
R1
10MΩ
C

$$C = \frac{R_1}{R_3} C_1$$

$$I_L = \frac{V_{OS} + I_{OS} R_1}{R_3}$$

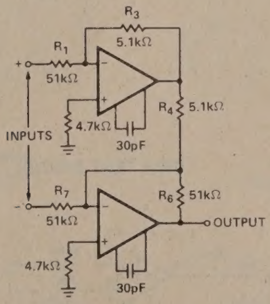
$$R_S = R_3$$

BILATERAL CURRENT SOURCE


R3
100kΩ
R1
INPUT
200kΩ
R2
200 kΩ
30pF
R5
2KΩ
R4
100kΩ
OUTPUT

$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5} \ ; R_1 = R_2; R_3 = R_4 + R_5$$

±100V COMMON MODE RANGE INSTRUMENTATION AMPLIFIER


R3
5.1kΩ
R1
+
51kΩ
INPUTS
4.7kΩ
30pF
R4
5.1kΩ
R7
−
51kΩ
R6
51kΩ
OUTPUT
4.7kΩ
30pF

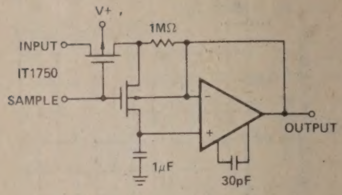
$\frac{R_1}{R_7} \equiv \frac{R_3}{R_4}$ for best CMRR

$R_3 = R_4$

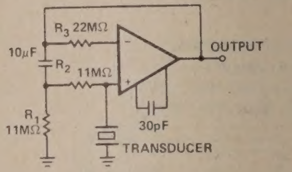
$R_1 = R_6 = 10R_3$

$\text{Gain} = \frac{R_7}{R_6}$

SAMPLE AND HOLD

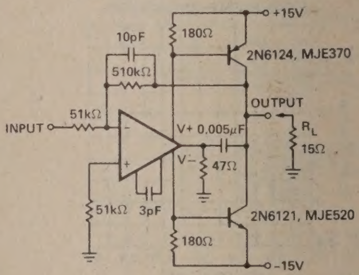

V+
1MΩ
INPUT
IT1750
SAMPLE
OUTPUT
1μF
30pF

AMPLIFIER FOR CAPACITANCE TRANSDUCERS

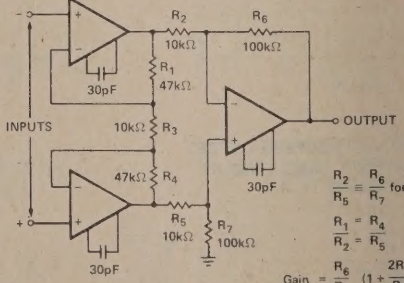

R3 22MΩ
10μF
R2
11MΩ
OUTPUT
R1
11MΩ
30pF
TRANSDUCER

LOW FREQUENCY CUTOFF $R_1 \times C_1$

HIGH SLEW RATE POWER AMPLIFIER


+15V
10pF
180Ω
2N6124, MJE370
510kΩ
OUTPUT
51kΩ
INPUT
V+ 0.005μF
RL
15Ω
V−
47Ω
51kΩ
3pF
2N6121, MJE520
180Ω
−15V

INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION


−
R2
10kΩ
R6
100kΩ
R1
47kΩ
30pF
INPUTS
10kΩ
R3
OUTPUT
47kΩ
R4
30pF
+
R5
10kΩ
R7
100kΩ
30pF

$\frac{R_2}{R_5} \equiv \frac{R_6}{R_7}$ for best CMRR

$R_1 = R_4$

$R_2 = R_5$

$\text{Gain} = \frac{R_6}{R_2} \left(1 + \frac{2R_1}{R_3}\right)$

LH2101A/LH2301A Dual High Performance Op Amp

FEATURES

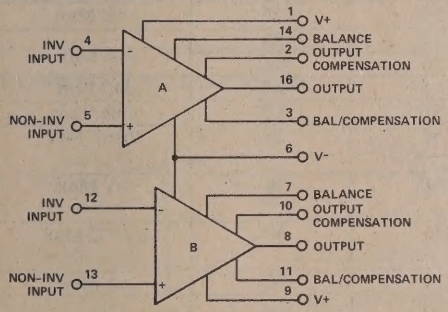
- **Low offset voltage**
- **Low offset current**
- **Guaranteed drift characteristics**
- **Offsets guaranteed over entire common mode and supply voltage ranges**
- **Slew rate of 10V/μs**

GENERAL DESCRIPTION

The LH2101A series of dual operational amplifiers consist of two LM101A type op amps in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, and reduced insertion cost.

The LH2101A is specified for operation over the −55°C to +125°C military temperature range, while the LH2301A is specified for operation over the 0°C to +70°C temperature range.

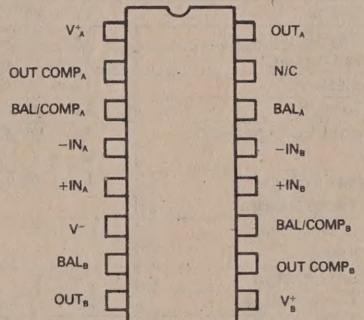
CONNECTION DIAGRAM



INV INPUT 4
NON-INV INPUT 5
A
1 V+
14 BALANCE
2 OUTPUT COMPENSATION
16 OUTPUT
3 BAL/COMPENSATION
6 V-
INV INPUT 12
NON-INV INPUT 13
B
7 BALANCE
10 OUTPUT COMPENSATION
8 OUTPUT
11 BAL/COMPENSATION
9 V+

ORDER NUMBER LH2101AD, LH2301AD

PIN CONFIGURATION

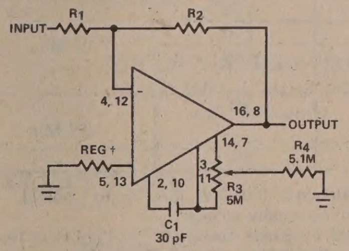


V⁺A
OUT COMPA
BAL/COMPA
−INA
+INA
V⁻
BALB
OUTB
OUTA
N/C
BALA
−INB
+INB
BAL/COMPB
OUT COMPB
V⁺B

(outline dwg DE)

AUXILIARY CIRCUITS

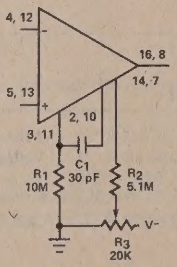
INVERTING AMPLIFIER WITH BALANCING CIRCUIT



R1
R2
INPUT
4, 12
16, 8
OUTPUT
14, 7
REG †
R4
5.1M
5, 13
2, 10
3, 11
R3
5M
C1
30 pF

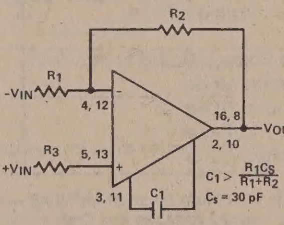
†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

ALTERNATE BALANCING CIRCUIT



4, 12
16, 8
14, 7
5, 13
2, 10
3, 11
C1
30 pF
R1
10M
R2
5.1M
V-
R3
20K

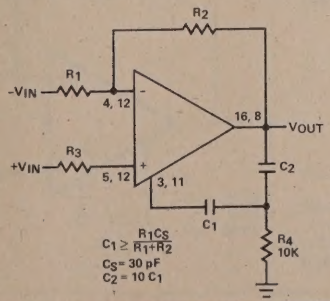
SINGLE POLE COMPENSATION



R2
R1
-VIN
4, 12
16, 8
VOUT
R3
5, 13
+VIN
2, 10
3, 11
C1

$C_1 > \frac{R_1 C_S}{R_1 + R_2}$
$C_S = 30\text{ pF}$

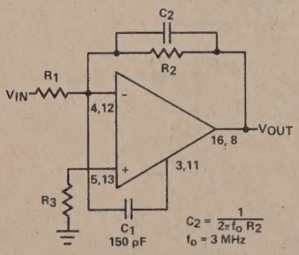
TWO POLE COMPENSATION



R2
R1
-VIN
4, 12
16, 8
VOUT
R3
+VIN
5, 12
3, 11
C2
C1
R4
10K

$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$
$C_S = 30\text{ pF}$
$C_2 = 10\,C_1$

FEEDFORWARD COMPENSATION



C2
R2
R1
VIN
4,12
VOUT
16, 8
3,11
5,13
R3
C1
150 pF

$C_2 = \frac{1}{2\pi f_o R_2}$
$f_o = 3\text{ MHz}$

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±22V
Power Dissipation (Note 1)		500 mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short-Circuit Duration		Continuous
Operating Temperature Range	LH2101A	−55°C to 125°C
	LH2301A	0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

ELECTRICAL CHARACTERISTICS Each side (Note 3)

PARAMETER	CONDITIONS	LIMITS		UNITS
		LH2101A	LH2301A	
Offset Voltage	$T_A = 25°C$, $R_S \le 50k\Omega$	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	10	50	nA Max
Input Bias Current	$T_A = 25°C$	75	250	
Input Resistance	$T_A = 25°C$	1.5	0.5	MΩ Min
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$	3.0	3.0	mA Max
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \ge 2k\Omega$	50	25	V/mV Min
Input Offset Voltage Average Temperature	$R_S \le 50\ k\Omega$	3.0	10	mV Max
Coefficient of Input Offset Voltage		15	30	μV/°C Max
Input Offset Current		20	70	nA Max
Average Temperature	$25°C \le T_A \le 125°C$	0.1	0.3	nA/°C Max
Coefficient of Input Offset Current	$-55°C \le T_A \le 25°C$	0.2	0.6	
Input Bias Current		100	300	nA Max
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$	2.5		mA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \ge 2\ k\Omega$	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±12	V Min
	$R_L = 2\ k\Omega$	±10	±10	
Input Voltage Range Common Mode	$V_S = \pm 20V$	±15	±12	
Rejection Ratio Supply Voltage	$R_S \le 50\ k\Omega$	80	70	dB Min
Rejection Ratio	$R_S \le 50\ k\Omega$	80	70	

Note 1: The maximum junction temperature of the LH2101A is 150°C, and the thermal resistance is 100°C/W, junction to ambient.
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 3: These specifications apply for $\pm 5V \le V_S \le \pm 20V$ and $-55°C \le T_A \le 125°C$, unless otherwise specified. For the LH2301A these specifications apply for $0°C \le T_A \le 70°C$, ±5V and $\le V_S \le \pm 15V$. Supply current and input voltage range are specified as $V_S = \pm 15V$ for the LH2301A. $C_1 = 30$ pF unless otherwise specified.

LH2108/2308
Dual Super Beta Op Amp

FEATURES

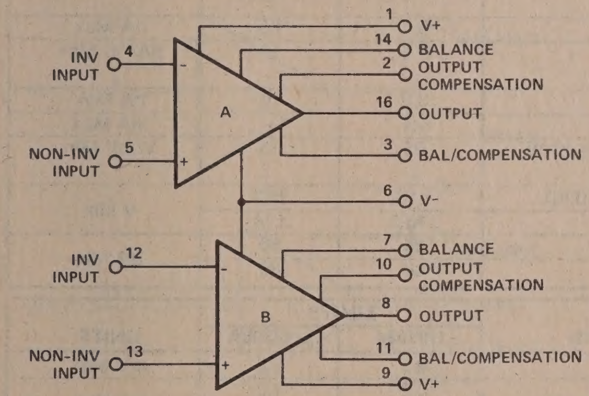
- **Low offset current - 50 pA**
- **Low offset voltage - 0.7 mV**
- **Low offset voltage - LH2108A: 0.3 mV**
  LH2108: 0.7 mV
- **Wide input voltage range - ±15V**
- **Wide operating supply range - ±3V to ±20V**

GENERAL DESCRIPTION

The LH2108A/LH2308A and LH2108/LH2308 series of dual operational amplifiers consist of two LM108A or LM108 type op amps in a single hermetic package. Featuring all the same performance characteristics of the single device, these duals also offer closer thermal tracking, lower weight, and reduced insertion cost.

The LH2108A/LH2108 is specified for operation over the −55°C to +125°C military temperature range, and the LH2308A/LH2308 is specified for operation from 0°C to +70°C.

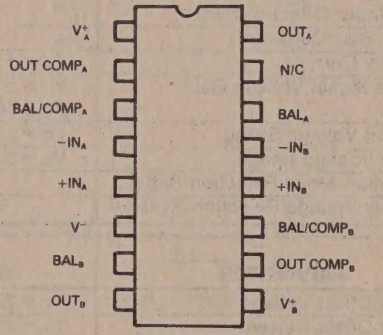
CONNECTION DIAGRAM



1 V+
14 BALANCE
2 OUTPUT COMPENSATION
16 OUTPUT
3 BAL/COMPENSATION
6 V−
7 BALANCE
10 OUTPUT COMPENSATION
8 OUTPUT
11 BAL/COMPENSATION
9 V+
INV INPUT 4
NON-INV INPUT 5
INV INPUT 12
NON-INV INPUT 13
A
B
−
+

ORDER NUMBER LH2108AD, LH2408AD, LH2108D, OR LH2408D

PIN CONFIGURATION

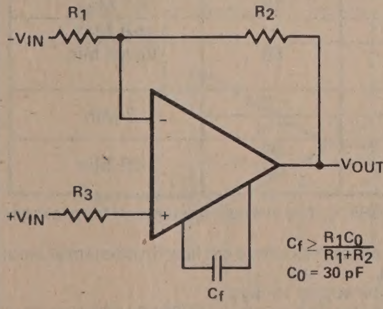


V^+_A
OUT COMP$_A$
BAL/COMP$_A$
−IN$_A$
+IN$_A$
V⁻
BAL$_B$
OUT$_B$
OUT$_A$
N/C
BAL$_A$
−IN$_B$
+IN$_B$
BAL/COMP$_B$
OUT COMP$_B$
V^+_B

(outline dwg DE)

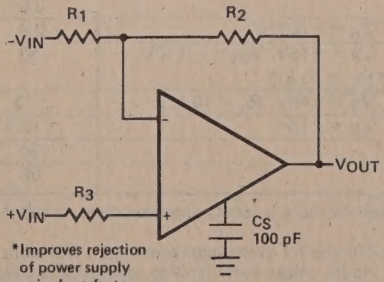
AUXILIARY CIRCUITS

STANDARD COMPENSATION CIRCUIT



R1
R2
−VIN
VOUT
R3
+VIN
−
+
Cf
$C_f \geq \frac{R_1 C_0}{R_1 + R_2}$
$C_0 = 30$ pF

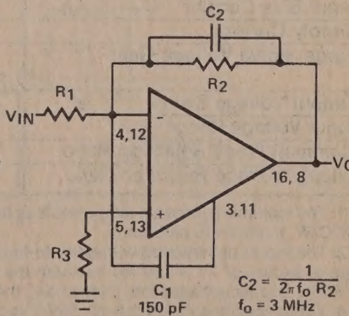
ALTERNATE* FREQUENCY COMPENSATION



R1
R2
−VIN
VOUT
R3
+VIN
−
+
CS
100 pF

*Improves rejection of power supply noise by a factor of ten.

FEEDFORWARD COMPENSATION



C2
R2
R1
VIN
4,12
−
+
VOUT
16, 8
3,11
5,13
R3
C1
150 pF
$C_2 = \frac{1}{2\pi f_0 R_2}$
$f_0 = 3$ MHz

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH2108A/LH2108	−55°C to +125°C
LH2308A/LH2408	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS Each side (Note 4)

PARAMETER	CONDITIONS	LIMITS		UNITS
		LH2108	LH2308	
Input Offset Voltage	$T_A = 25°C$	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	0.2	1.0	nA Max
Input Bias Current	$T_A = 25°C$	2.0	7.0	
Input Resistance	$T_A = 25°C$	30	10	MΩ Min
Supply Current	$T_A = 25°C$	0.6	0.8	mA Max
Large Signal Voltage Gain	$T_A = 25°C$ $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 10$ kΩ	50	25	V/mV Min
Input Offset Voltage		3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	30	μV/°C Max
Input Offset Current		0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	10	pA/°C Max
Input Bias Current		3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	—	mA Max
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 10$ kΩ	25	15	V/mV Min
Output Voltage Swing	$V_S = ±15V$, $R_L = 10$ kΩ	±13	±13	V Min
Input Voltage Range	$V_S = ±15V$	±13.5	±14	
Common Mode Rejection Ratio		85	80	dB Min
Supply Voltage Rejection Ratio		80	80	

PARAMETER	CONDITIONS	LIMITS		UNITS
		LH2108A	LH2308A	
Input Offset Voltage	$T_A = 25°C$	0.5	0.5	mV Max
Input Offset Current	$T_A = 25°C$	0.2	1.0	nA Max
Input Bias Current	$T_A = 25°C$	2.0	7.0	
Input Resistance	$T_A = 25°C$	30	10	MΩ Min
Supply Current	$T_A = 25°C$	0.6	0.8	mA Max
Large Signal Voltage Gain	$T_A = 25°C$ $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 10$ kΩ	80	80	V/mV Min
Input Offset Voltage		1.0	0.73	mV Max
Average Temperature Coefficient of Input Offset Voltage		5	5	μV/°C Max
Input Offset Current		0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	10	pA/°C Max
Input Bias Current		3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	-	mA Max
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 10$ kΩ	40	60	V/mV Min
Output Voltage Swing	$V_S = ±15V$, $R_L = 10$ kΩ	±13	±13	V Min
Input Voltage Range	$V_S = ±15V$	±13.5	±14	
Common Mode Rejection Ratio		96	96	dB Min
Supply Voltage Rejection Ratio		96	96	

Note 1: The maximum junction temperature of the LH2108/A is 150°C, and that of the LH2308/A is 85°C. The thermal resistance of the packages is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $±5V \leq V_S \leq ±20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified, and the LH2308A/LH2308 for $±5V \leq V_S \leq 15V$ and $0°C \leq T_A \leq 70°C$.

LH2110/LH2310
Dual Voltage Follower

FEATURES

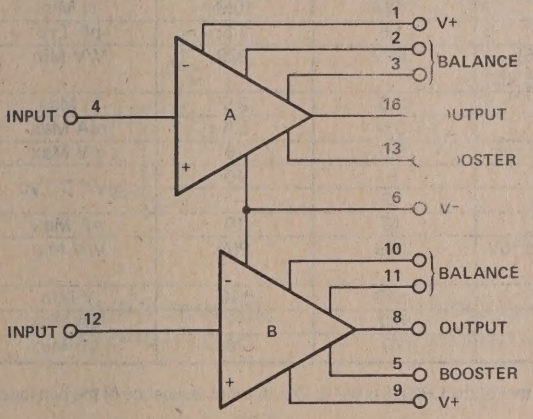
- **Low input current - 1 nA**
- **High input resistance - 10 MΩ**
- **High slew rate - 30V/μs**
- **Wide bandwidth - 20 MHz**
- **Wide operating supply range - ±5V to ±18V**
- **Output short circuit protected.**

GENERAL DESCRIPTION

The LH2110 series of dual voltage followers consist of two LM110 type followers in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, and reduced insertion cost.

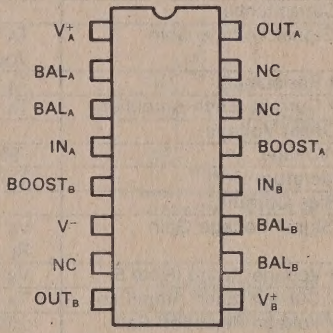
The LH2110 is specified for operation over the −55°C to +125°C military temperature range, and the LH2310 is specified for operation from 0°C to +70°C.

CONNECTION DIAGRAM


1
V+
2
3
BALANCE
INPUT
4
A
−
+
16
UTPUT
13
OOSTER
6
V−
10
11
BALANCE
INPUT
12
B
−
+
8
OUTPUT
5
BOOSTER
9
V+

ORDER NUMBER LH2110D or LH2310D

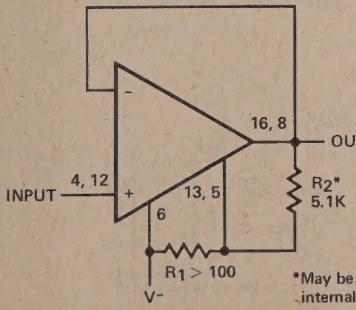
PIN CONFIGURATION


V_A^+
BAL_A
BAL_A
IN_A
$BOOST_B$
V^-
NC
OUT_B
OUT_A
NC
NC
$BOOST_A$
IN_B
BAL_B
BAL_B
V_B^+

(outline dwg DE)

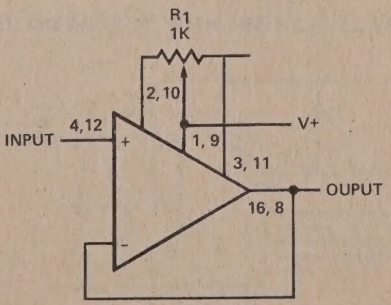
AUXILIARY CIRCUITS

INCREASING NEGATIVE SWING UNDER LOAD


−
+
16, 8
OUTPUT
INPUT
4, 12
13, 5
6
R2*
5.1K
R1 > 100
V−

*May be added to reduce internal dissipation

OFFSET BALANCING CIRCUIT


R1
1K
2, 10
4,12
INPUT
+
1, 9
V+
3, 11
OUPUT
16, 8
−

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range LH2110	−55°C to 125°C
LH2310	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS Each side (Note 4)

PARAMETER	CONDITIONS	LIMITS LH2110	LIMITS LH2310	UNITS
Input Offset Voltage	$T_A = 25°C$	4.0	7.5	mV Max
Input Bias Current	$T_A = 25°C$	3.0	7.0	nA Max
Input Resistance	$T_A = 25°C$	10M	10M	Ω Min
Input Capacitance		1.5	1.5	pF Typ
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L = 8\ k\Omega$	.999	.999	V/V Min
Output Resistance	$T_A = 25°C$	2.5	2.5	Ω Max
Supply Current (Each Amplifier)	$T_A = 25°C$	5.5	5.5	mA Max
Input Offset Voltage		6.0	10	mV Max
Offset Voltage Temperature Drift	$-55°C \leq T_A \leq 85°C$	6	10	μV/°C Typ
	$T_A = 125°C$	12	—	
Input Bias Current		10	10	nA Max
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L = 10\ k\Omega$	.999	.999	V/V Min
Output Voltage Swing (Note 5)	$V_S = ±15V$, R_L 10 kΩ	±10	±10	V Min
Supply Current (Each Amplifier)	$T_A = 125°C$	4.0	—	mA Max
Supply Voltage Rejection Ratio	$±5V \leq V_S \leq ±18V$	70	70	dB Min

Note 1: The maximum junction temperature of the LH2110 is 150°C, while that of the LH2310 is 85°C. The thermal resistance of the package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C. It is necessary to insert a resistor greater than 2 KΩ in series with the inut when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.

Note 4: These specifications apply for $±5V \leq V_S \leq ±18V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified, and for the LH2310, all temperature specifications are limited to $0°C \leq T_A \leq 70°C$.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V− terminals.

INTERSIL

LH2111, LH2311
Dual Voltage Comparator

FEATURES

- **Wide operating range - ±15V to a single +5V**
- **Low input currents - 6 nA**
- **High sensitivity - 10 μV**
- **Wide differential input range - ±30V**
- **High output drive - 50V, 50 mA**

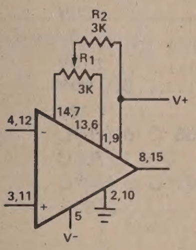
GENERAL DESCRIPTION

The LH2111 series of dual voltage comparators consist of two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, and reduced insertion cost.

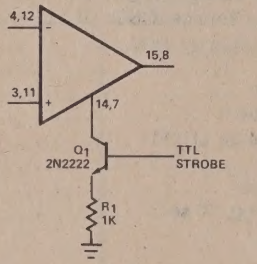
The LH2111 is specified for operation over the −55°C to +125°C military temperature range, and the LH2311 is specified for operation from 0°C to 70°C.

AUXILIARY CIRCUITS

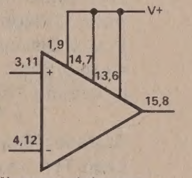
OFFSET BALANCING


R2
3K
R1
3K
V+
14,7
13,6
1,9
4,12
8,15
3,11
2,10
5
V-

STROBING

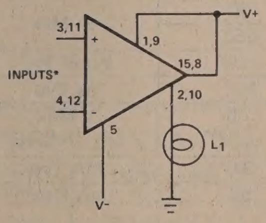

4,12
15,8
3,11
14,7
Q1
2N2222
TTL
STROBE
R1
1K

INCREASING INPUT STAGE CURRENT*

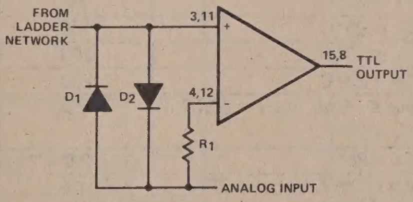

V+
1,9
14,7
13,6
3,11
15,8
4,12

*Increases typical common mode slew from 7.0/μs to 18V/μs.

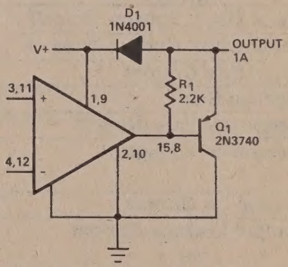
DRIVING GROUND-REFERRED LOAD


V+
3,11
1,9
15,8
INPUTS*
4,12
2,10
5
L1
V-

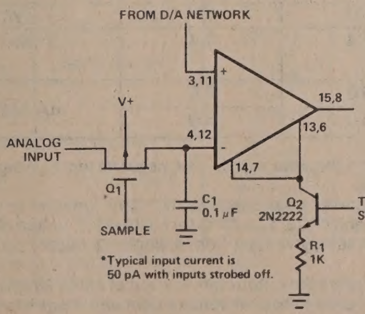
USING CLAMP DIODES TO IMPROVE RESPONSES


FROM
LADDER
NETWORK
3,11
15,8
TTL
OUTPUT
D1
D2
4,12
R1
ANALOG INPUT

COMPARATOR AND SOLENOID DRIVER

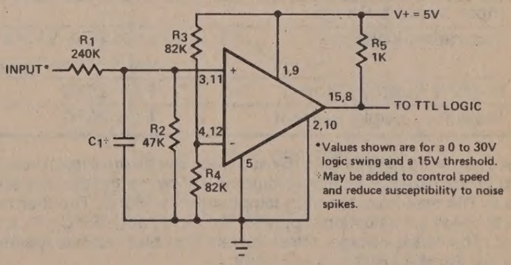

D1
1N4001
V+
OUTPUT
1A
R1
2.2K
3,11
1,9
Q1
2N3740
15,8
2,10
4,12

STROBING OFF BOTH INPUT* AND OUTPUT STAGES


FROM D/A NETWORK
3,11
15,8
V+
13,6
4,12
ANALOG
INPUT
14,7
Q1
C1
0.1μF
Q2
2N2222
TTL
STROBE
SAMPLE
R1
1K

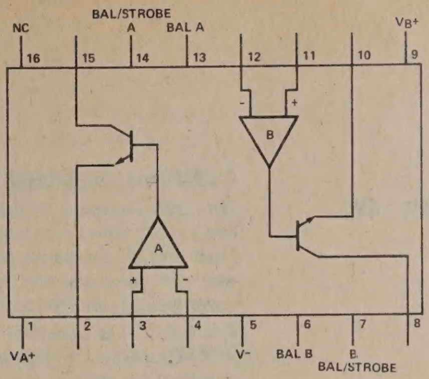
*Typical input current is 50 pA with inputs strobed off.

TTL INTERFACE WITH HIGH LEVEL LOGIC


V+ = 5V
R1
240K
R3
82K
R5
1K
INPUT*
3,11
1,9
15,8
TO TTL LOGIC
2,10
C1
R2
47K
4,12
5
R4
82K

*Values shown are for a 0 to 30V logic swing and a 15V threshold.
†May be added to control speed and reduce susceptibility to noise spikes.

CONNECTION DIAGRAM



ORDER NUMBER LH2111D OR LH2311D

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage	36V
Output to Negative Supply Voltage (V_{OUT} - V−)	50V
Ground to Negative Supply Voltage (GND - V−)	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LH2111	−55°C to 125°C
LH2311	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS Each side (Note 3)

PARAMETER	CONDITIONS	LIMITS		UNITS
		LH2111	LH2311	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$	3.0	7.5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	250	
Voltage Gain	$T_A = 25°C$	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	ns Typ
Saturation Voltage	$V_{IN} \leq -5mV$, $I_{OUT} = 50mA$ $T_A = 25°C$	1.5	1.5	V Max
Strobe On Current	$T_A = 25°C$	3.0	3.0	mA Typ
Output Leakage Current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$ $T_A = 25°C$	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \leq 50k$	4.0	10	mV Max
Input Offset Current (Note 4)		20	70	nA Max
Input Bias Current		150	300	
Input Voltage Range		±14	±14	V Typ
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -5mV$, $I_{SINK} \leq 8$ mA	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6.0	7.5	mA Max
Negative Supply Current	$T_A = 25°C$	5.0	5.0	

Note: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature is 150°C. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$ for the LH2111, and $0°C \leq T_A \leq 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm 10V$.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

INTERSIL

HA 2500/02/05/10/12/15/20/22/25
High Slew Rate Operational Amplifiers

FEATURES

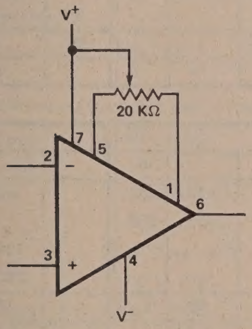
- Slew Rate — Up to 120 V/μs
- Settling Time — 200 ns to 0.1%
- Bias Current — 100 nA
- Gain Bandwidth Product — 30 MHz
- Internal Frequency Compensation
- Radiation Hardened
- Meets MIL-STD-883

GENERAL DESCRIPTION

The 2500 series of high slew rate operational amplifiers are monolithic integrated circuits fabricated using dielectric isolation and thin film resistors. These internally compensated amplifiers feature excellent input parameters, high gain and wide bandwidth. They are ideally suited for D/A and A/D converter circuits, pulse amplifiers and high frequency buffer amplifiers.

2500 through 2515 are compensated for unity gain. 2520 through 2525 are intended for closed loop gains of 3 or greater, and feature increased slew rates and gain-bandwidth products.

VOLTAGE OFFSET NULL CIRCUIT

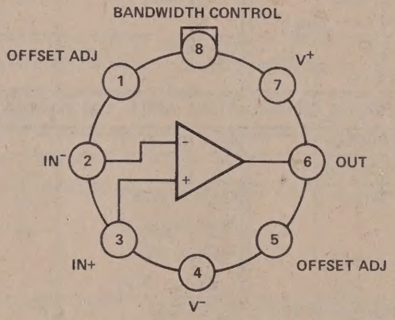


ORDERING INFORMATION

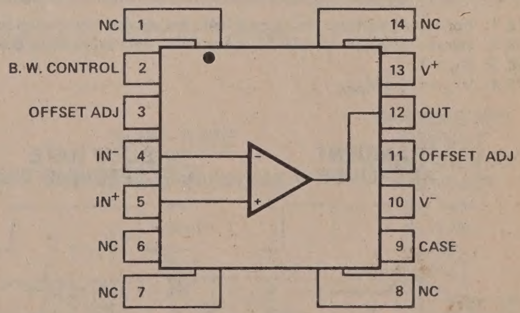
PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER
HA2500	-55°C to +125°C	TO-99 Flat Pack	HA2-2500-2 * HA9-2500-2 *
HA2502	-55°C to +125°C	TO-99 Flat Pack	HA2-2502-2 * HA9-2502-2 *
HA2505	0°C to +75°C	TO-99 Flat Pack	HA2-2505-5 HA9-2505-5
HA2510	-55°C to +125°C	TO-99 Flat Pack	HA2-2510-2 * HA9-2510-2 *
HA2512	-55°C to +125°C	TO-99 Flat Pack	HA2-2512-2 * HA9-2512-2 *
HA2515	0°C to +75°C	TO-99 Flat Pack	HA2-2515-5 HA9-2515-5
HA2520	-55°C to +125°C	TO-99 Flat Pack	HA2-2520-2 * HA9-2520-2 *
HA2522	-55°C to +125°C	TO-99 Flat Pack	HA2-2522-2 * HA9-2522-2 *
HA2525	0°C to +75°C	TO-99 Flat Pack	HA2-2525-5 HA9-2525-5

*883 processing is available for these devices.
Order -8 instead of -2.

PIN CONFIGURATIONS



(TOP VIEW)
(outline dwg TO-99)



(outline dwg FD)

ABSOLUTE MAXIMUM RATINGS

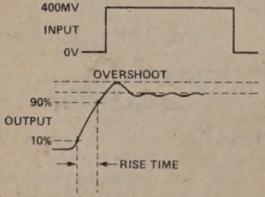
Supply Voltage	±20V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±15V
Peak Output Current	±50 mA
Internal Power Dissipation (Note 2)	300 mW
Lead Temperature (Soldering, 60 sec)	300°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C (2500, 2502) 0°C to +75°C (2505)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V unless otherwise specified)

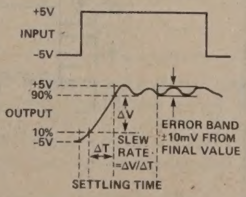
PARAMETER	CONDITIONS	2500			2502			2505			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leqslant 10\,k\Omega$		2	5		4	8		4	8	mV
Input Offset Current			10	25		20	50		20	50	nA
Input Resistance		25	50		20	50		20	50		MΩ
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = \pm10V$	20k	30k		15k	25k		15k	25k		V/V
Gain Bandwidth	$A_V > 10$		12			12			12		MHz
Full Power Bandwidth	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = 20Vp\text{-}p$	350	500		300	500		300	500		kHz
Rise Time (Notes 3,4)	$R_L = 2k\Omega$, $C_L = 50pF$		25	50		25	50		25	50	ns
Overshoot (Notes 3,4)	$R_L = 2k\Omega$, $C_L = 50pF$		25	40		25	50		25	50	%
Slew Rate (Note 3)	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = \pm5V$	±25	±30		±20	±30		±20	±30		V/µs
Settling Time (to 0.1% of Final Value) (Note 3)	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = \pm5V$		330			330			330		ns
Output Current	$V_O = \pm10V$	±10			±10			±10			mA
Supply Current			4	6		4	6		4	6	mA
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leqslant 10\,k\Omega$			8			10			10	mV
Input Offset Current				50			100			100	nA
Input Bias Current	+25°C to +125°C		100	200		125	250				nA
	-55°C to +25°C		200	400		250	500				nA
	+25°C to +75°C								125	250	nA
	0°C to +25°C								250	500	nA
Offset Voltage Average Drift	$R_S \leqslant 10\,k\Omega$		20			20			20		µV/°C
Offset Current Average Drift			0.1			0.1			0.1		nA/°C
Common Mode Rejection Ratio	$V_{CM} = \pm5V$	80	90		74	90		74	90		dB
Common Mode Range		±10			±10			±10			V
Supply Voltage Rejection Ratio	$\Delta V = \pm5V$	80	90		74	90		74	90		dB
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = \pm10V$	7.5k			5k			10k			V/V
Output Voltage Swing	$R_L = 2k\Omega$	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 2: Derate TO-86 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.
NOTE 3: $A_V = 1$.
NOTE 4: $V_O = 400\ mV_{p\text{-}p}$.

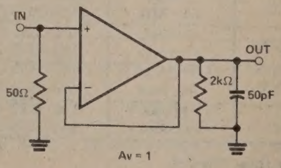
TRANSIENT RESPONSE



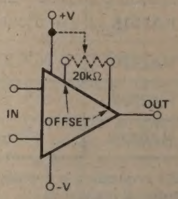
SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



NOTE: Measured on both positive and negative transitions.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±15V
Peak Output Current	±50 mA
Internal Power Dissipation (Note 2)	300 mW
Lead Temperature (Soldering, 60 sec)	300°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C (2510, 2512) 0°C to +75°C (2515)

ELECTRICAL CHARACTERISTICS (T$_A$ = 25°C, V$_S$ = ±15V unless otherwise specified)

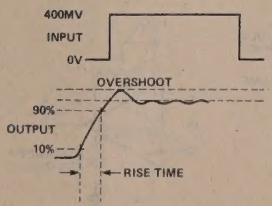
PARAMETER	CONDITIONS	2510			2512			2515			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\,k\Omega$		4	8		5	10		5	10	mV
Input Offset Current			10	25		20	50		20	50	nA
Input Resistance		50	100		40	100		40	100		MΩ
Large Signal Voltage Gain	$R_L = 2\,k\Omega$, $V_O = \pm 10V$	10k	15k		7.5k	15k		7.5k	15k		V/V
Gain Bandwidth	$A_V > 10$		12			12			12		MHz
Full Power Bandwidth	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = 20Vp\text{-}p$	750	1000		600	1000		600	1000		kHz
Rise Time (Notes 3,4)	$R_L = 2k\Omega$, $C_L = 50pF$		25	50		25	50		25	50	ns
Overshoot (Notes 3,4)	$R_L = 2k\Omega$, $C_L = 50pF$		25	40		25	50		25	50	%
Slew Rate (Note 3)	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = \pm 5V$	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (to 0.1% of Final Value) (Note 3)	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = \pm 5V$		250			250			250		ns
Output Current	$V_O = \pm 10V$	±10			±10			±10			mA
Supply Current			4	6		4	6		4	6	

THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE

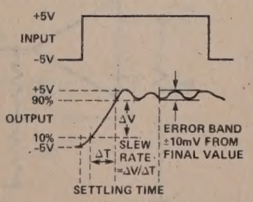
PARAMETER	CONDITIONS	2510 MIN	2510 TYP	2510 MAX	2512 MIN	2512 TYP	2512 MAX	2515 MIN	2515 TYP	2515 MAX	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$			11			14			14	mV
Input Offset Current				50			100			100	nA
Input Bias Current	+25°C to +125°C		100	200		125	250				nA
	-55°C to +25°C		200	400		250	500				nA
	+25°C to +75°C								125	250	nA
	0°C to +25°C								250	500	nA
Offset Voltage Average Drift	$R_S \leq 10\,k\Omega$		20			30			30		µV/°C
Offset Current Average Drift			0.1			0.1			0.1		nA/°C
Common Mode Rejection Ratio	$V_{CM} = \pm 5V$	80	90		74	90		74	90		dB
Common Mode Range		±10			±10			±10			V
Supply Voltage Rejection Ratio	$\Delta V = \pm 5V$	80	90		74	90		74	90		dB
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	7.5k			5k			5k			V/V
Output Voltage Swing	$R_L = 2k\Omega$	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 2: Derate TO-86 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.
NOTE 3: $A_V = 1$.
NOTE 4: $V_O = 400\ mV_{p=p}$.

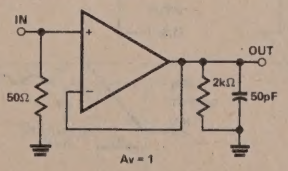
TRANSIENT RESPONSE



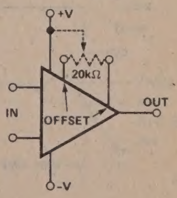
SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



NOTE: Measured on both positive and negative transitions.

ABSOLUTE MAXIMUM RATINGS

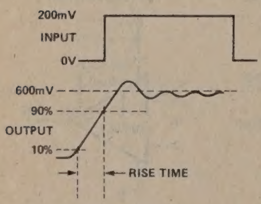
Supply Voltage	±20V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±15V
Peak Output Current	±50 mA
Internal Power Dissipation (Note 2)	300 mW
Lead Temperature (Soldering, 60 sec)	300°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C (2520, 2522) 0°C to +75°C (2525)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = ±15V$ unless otherwise specified)

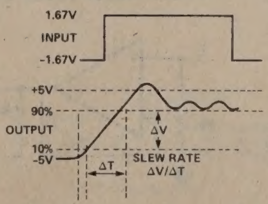
PARAMETER	CONDITIONS	2520			2522			2525			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\,k\Omega$		4	8		5	10		5	10	mV
Input Offset Current			10	25		20	50		20	50	nA
Input Resistance		50	100		40	100		40	100		MΩ
Large Signal Voltage Gain	$R_L = 2\,k\Omega$, $V_O = ±10V$	10k	15k		7.5k	15k		7.5k	15k		V/V
Gain Bandwidth	$A_V > 10$		30			30			30		MHz
Full Power Bandwidth	$R_L = 2\,k\Omega$, $C_L = 50pF$, $V_O = 20V_{p-p}$	1500	2000		1200	1600		1200	1600		kHz
Rise Time (Notes 3,4)	$R_L = 2k\Omega$, $C_L = 50pF$		15	50		15	50		15	50	ns
Overshoot (Notes 3,4)	$R_L = 2\,k\Omega$, $C_L = 50pF$		25	40		25	50		25	50	%
Slew Rate (Note 3)	$R_L = 2\,k\Omega$, $C_L = 50pF$, $V_O = ±5V$	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (to 0.1% of Final Value) (Note 3)	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = ±5V$		200			200			200		ns
Output Current	$V_O = ±10V$	±10			±10			±10			mA
Supply Current			4	6		4	6		4	6	mA
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leq 10\,k\Omega$			11			14			14	mV
Input Offset Current				50			100			100	nA
Input Bias Current	+25°C to +125°C		100	200		125	250				nA
	-55°C to +25°C		200	400		250	500				nA
	+25°C to +75°C								125	250	nA
	0°C to +25°C								250	500	nA
Offset Voltage Average Drift	$R_S \leq 10\,k\Omega$		20			30			30		µV/°C
Offset Current Average Drift			0.1			0.1			0.1		nA/°C
Common Mode Rejection Ratio	$V_{CM} = ±5V$	80	90		74	90		74	90		dB
Common Mode Range		±10			±10			±10			V
Supply Voltage Rejection Ratio	$\Delta V = ±5V$	80	90		74	90		74	90		dB
Large Signal Voltage Gain	$R_L = 2\,k\Omega$, $V_O = ±10V$	7.5k			5k			5k			V/V
Output Voltage Swing	$R_L = 2\,k\Omega$	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 2: Derate TO-86 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.
NOTE 3: $A_V = 3$.
NOTE 4: $V_O = 600\ mV_{p-p}$.

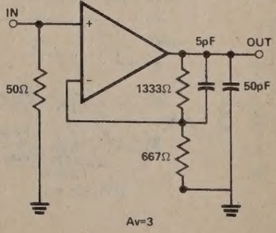
TRANSIENT RESPONSE



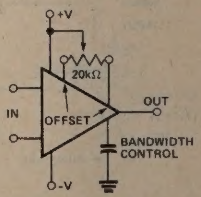
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE

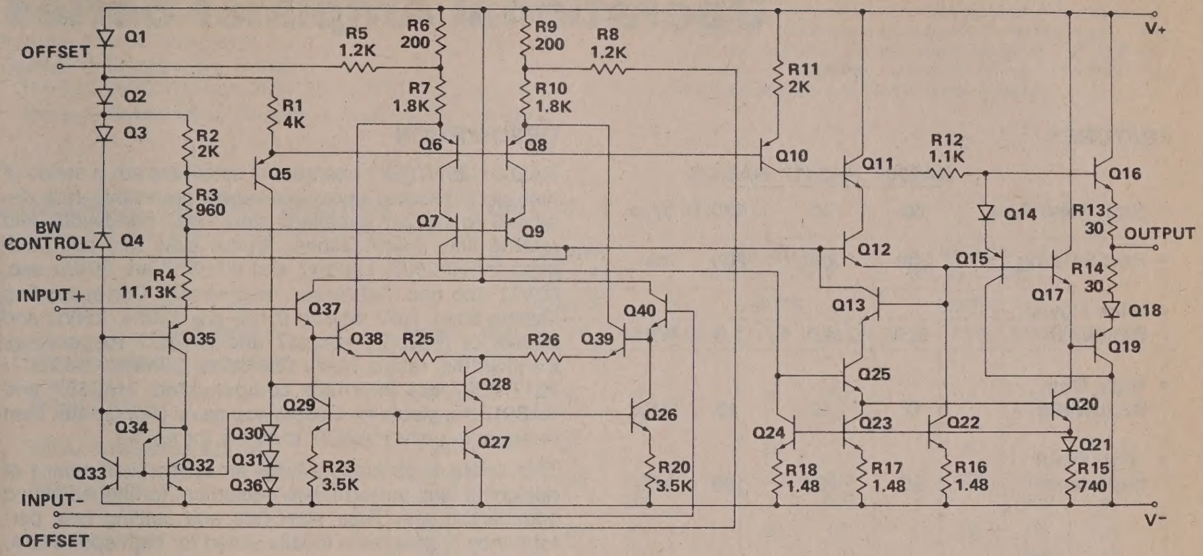


SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP



NOTE: Measured on both positive and negative transitions.

SCHEMATIC DIAGRAM


OFFSET
Q1
Q2
Q3
R5
1.2K
R6
200
R7
1.8K
R9
200
R8
1.2K
R10
1.8K
R11
2K
V+
R1
4K
R2
2K
Q5
R3
960
Q6
Q8
Q10
Q11
R12
1.1K
Q16
Q14
R13
30
OUTPUT
BW
CONTROL
Q4
Q7
Q9
Q12
Q15
R14
30
Q17
R4
11.13K
INPUT+
Q37
Q40
Q13
Q18
Q35
Q38
R25
R26
Q39
Q19
Q28
Q25
Q29
Q26
Q20
Q34
Q30
Q27
Q24
Q23
Q22
Q21
Q33
Q32
Q31
Q36
R23
3.5K
R20
3.5K
R18
1.48
R17
1.48
R16
1.48
R15
740
INPUT-
V-
OFFSET

HA2507/2517/2527
High Slew Rate Operational Amplifier Series

FEATURES

	HA2507	HA2517	HA2527	
• High Slew Rate	30	60	120	V/µs
• Fast Settling	330	250	200	ns
• Wide Power Bandwidth	0.5	1.0	1.6	MHz
• High Gain Bandwidth	12	12	20	MHz
• High Input Impedance	50	100	100	MΩ

ORDERING INFORMATION

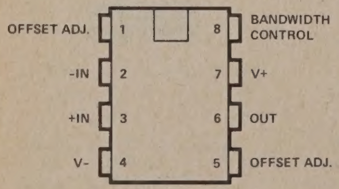
HA3-2507-5 HA3-2517-5 HA3-2527-5	8 pin minidip

DESCRIPTION

HA2507/2517/2527 operational amplifiers are a series of high-performance, epoxy-packaged monolithic IC's designed to deliver excellent slew rate, bandwidth and settling time specifications. Typical slew rate specifications for HA2507, HA2517 and HA2527 are 30V/µ sec, 60V/µ sec and 120V/µsec respectively. Corresponding settling times (10V step to 0.1%) are 330ns, 250ns and 200ns for HA2507, HA2517 and HA2527 respectively. Bandwidths range from 12MHz to 20MHz. HA2507/2517/2527 are internally compensated; HA2507 and HA2517 are stable for closed loop gains (A_V) greater than or equal to unity. HA2527 is stable for $A_V > 3$.

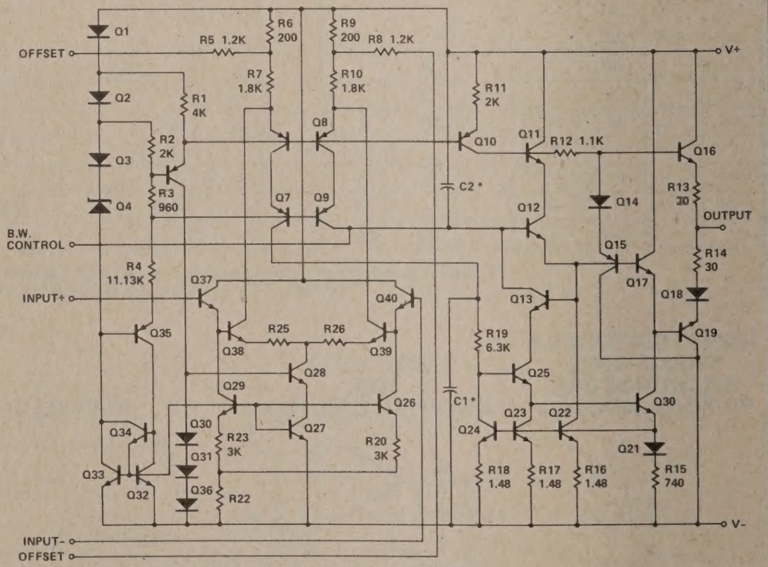
This series of op amps affords an economical means of designing high performance equipment for industrial and commercial use. Their slew rate and settling time performance makes them ideally suited for high speed D/A, A/D and pulse amplification designs. The wide bandwidth offered by these devices also makes them valuable components in RF and video applications. HA2507/2517/2527 also deliver offset current, bias current and offset voltage specifications compatible with the requirements of accurate signal conditioning systems.

PIN CONFIGURATION


OFFSET ADJ.
1
-IN
2
+IN
3
V-
4
8
BANDWIDTH CONTROL
7
V+
6
OUT
5
OFFSET ADJ.

(outline dwg PA)

SCHEMATIC


Q1
OFFSET
R5 1.2K
R6 200
R9 200
R8 1.2K
V+
Q2
R1 4K
R7 1.8K
R10 1.8K
R11 2K
Q3
R2 2K
Q8
Q10
Q11
R12 1.1K
Q16
Q4
R3 960
Q7
Q9
C2*
Q12
Q14
R13 30
OUTPUT
B.W. CONTROL
Q15
R14 30
R4 11.13K
Q37
Q17
INPUT+
Q40
Q13
Q18
Q35
R25
R26
Q38
Q39
R19 6.3K
Q19
Q28
Q29
Q25
Q26
C1*
Q30
Q34
Q30
Q27
Q24
Q23
Q22
R23 3K
R20 3K
Q21
Q31
Q33
Q32
Q36
R22
R18 1.48
R17 1.48
R16 1.48
R15 740
V-
INPUT-
OFFSET

*VALUES OF C1, C2, R25 AND R26 VARY DEPENDING ON DEVICE TYPE.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals 40.0V
Differential Input Voltage .... ±15.0V
Peak Output Current 50mA
Internal Power Dissipation 300mW
Operating Temperature Range—
  HA-2507/HA-2517/HA-2527 ..... $0°C \leq T_A \leq +75°C$
  Storage Temperature Range .. $-65° \leq T_A \leq +150°C$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS $V^+ = +15V$ D.C., $V^- = -15V$ D.C.

PARAMETER	TEMP.	HA-2507 0°C to +75°C			HA-2517 0°C to +75°C			HA-2527 0°C to +75°C			UNITS
		LIMITS			LIMITS			LIMITS			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		5	10		5	10		5	10	mV
	Full			14			14			14	mV
Offset Voltage Average Drift	Full		25			30			30		µV/°C
Bias Current	+25°C		125	250		125	250		125	250	nA
	Full			500			500			500	nA
Offset Current	+25°C		20	50		20	50		20	50	nA
	Full			100			100			100	nA
Input Resistance	+25°C	20	50		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	15K	25K		7.5K	15K		7.5K	15K		V/V
	Full	10K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	74	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	220	500		450	1000		750	1600		kHz
TRANSIENT RESPONSE											
Rise Times (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	50		25	50		25	50	%
Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±15	±30		±30	±60		±60	±120		V/µs
Settling Time to 0.1% (Notes 1, 4, 5 & 8)	+25°C		0.33			0.25			0.20		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	74	90		74	90		74	90		dB

Notes:
1. $R_L = 2K$
2. $V_{CM} = +5.0V$
3. $A_V > 10$
4. $V_O = +10.0V$
5. $C_L = 50pF$
6. $V_O = +400mV$ for HA-2507 and HA-2517; $V_O = +200mV$ for HA-2527
7. $V_O = +600mV$
8. For HA-2507 and HA-2517, $A_V = 1$; For HA-2527, $A_V = 3$
9. $\Delta V = +5.0V$

INTERSIL

HA2600, HA2605, HA2622, HA2602, HA2620, HA2625

High Impedance Operational Amplifiers

FEATURES

- Input Impedance – 500MΩ
- Offset Current – 1nA
- Bias Current – 1nA
- Gain Bandwidth Product – 100MHz
- High Gain – 150K
- Output Short Circuit Protection
- Meets MIL-STD-883

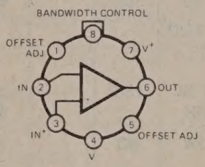
GENERAL DESCRIPTION

The 2600 series of high impedance operational amplifiers are monolithic integrated circuits fabricated using dielectric isolation. These internally compensated amplifiers feature excellent input parameters, low input bias and wide bandwidth. They are ideally suited for general purpose use in instrumentation and signal processing applications.

2600 through 2605 are compensated for unity gain. 2620 through 2625 are intended for closed loop gains of 5 or greater and feature increased slew rated and gain-bandwidth products.

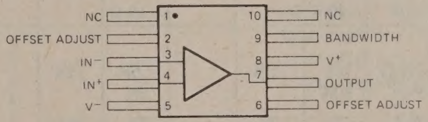
PIN CONFIGURATIONS, TOP VIEWS

(outline dwg TO-99)

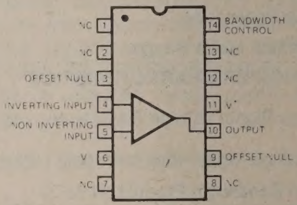

BANDWIDTH CONTROL
8
OFFSET ADJ
1
7
V+
IN–
2
6
OUT
3
5
IN+
OFFSET ADJ
4
V–

Pin 4 Connected to case

(outline dwg FB)


NC
OFFSET ADJUST
IN–
IN+
V–
1
2
3
4
5
10
9
8
7
6
NC
BANDWIDTH
V+
OUTPUT
OFFSET ADJUST

(outline dwg JD)


NC 1
NC 2
OFFSET NULL 3
INVERTING INPUT 4
NON INVERTING INPUT 5
V– 6
NC 7
14 BANDWIDTH CONTROL
13 NC
12 NC
11 V+
10 OUTPUT
9 OFFSET NULL
8 NC

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER
HA2600	–55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2600-2 * HA9-2600-2 * HA1-2600-2 *
HA2602	–55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2602-2 * HA9-2602-2 * HA1-2602-2 *
HA2605	0°C to +75°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2605-5 HA9-2605-5 HA1-2605-5
HA2620	–55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2620-2 * HA9-2620-2 * HA1-2620-2 *
HA2622	–55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2622-2 * HA9-2622-2 * HA1-2622-2 *
HA2625	0°C to +75°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2625-5 HA9-2625-5 HA1-2625-5

*883B processing is available for these devices. Order -8 instead of -2.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22.5V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±12V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	300mW
Lead Temperature (Soldering, 60 sec.)	+300°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	-55°C to +125°C (2600, 2602) 0°C to +75°C (2605)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V, unless otherwise specified)

PARAMETER	CONDITIONS	2600			2602			2605			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	4		3	5		3	5	mV
Input Offset Current			1	10		5	25		5	25	nA
Input Bias Current			1	10		5	25		5	25	nA
Input Resistance		100	500		40	300		40	300		MΩ
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = \pm10V$	100K	150K		80K	150K		80K	150K		V/V
Unity Gain Bandwidth	$V_O < 90mV$		12			12			12		MHz
Full Power Bandwidth	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = 20V_{p\text{-}p}$	50	75		50	75		50	75		KHz
Rise Time (Note 3)	$R_L = 2k\Omega$, $C_L = 100pF$		30	60		30	60		30	60	ns
Overshoot (Note 4)	$R_L = 2k\Omega$, $C_L = 100pF$		25	40		25	50		25	50	%
Slew Rate	$R_L = 2k\Omega$, $C_L = 100pF$, $V_O = \pm5V$	4	7		4	7		4	7		V/μs
Setting Time (to ±10mV of Final Value)	$R_L = 2k\Omega$, $C_L = 100pF$, $V_O = \pm5V$		1.5			1.5			1.5		ns
Output Current	$V_O = \pm10V$	±15	±22		±10	±18		±10	±18		mA
Supply Current			3	3.7		3	4		3	4	mA
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leq 10k\Omega$		2	6			7			7	mV
Input Offset Current			5	30			60			40	nA
Input Bias Current			10	30			60			40	nA
Offset Voltage Average Drift	$R_S \leq 10k\Omega$		5								μV/°C
Common Mode Rejection Ratio	$V_{CM} = \pm5V$	80	100		74	100		74	100		dB
Common Mode Range		±11			±11			±11			V
Supply Voltage Rejection Ratio	$V_S = \pm9V$ To $\pm15V$	80	90		74	90		74	90		dB
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = \pm10V$	70k			60k			70k			V/V
Output Voltage Swing	$R_L = 2k\Omega$	±10	±12		±10	±12		±10	±12		V

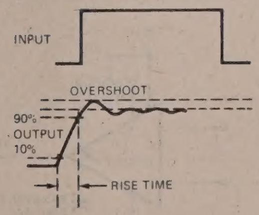
NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Derate TO-91 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.

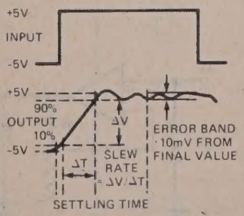
NOTE 3: $V_O = 400\ mV_{p\text{-}p}$

NOTE 4: $V_O = 800\ mV_{p\text{-}p}$

TRANSIENT RESPONSE

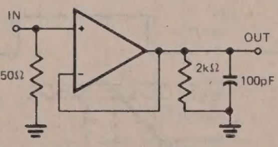


SLEW RATE AND SETTLING TIME

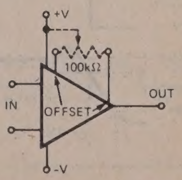


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22.5V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±12V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	300mW
Lead Temperature (Soldering, 60 sec.)	300°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C (2620, 2622) 0°C to +75°C (2625)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm15V$, unless otherwise specified)

PARAMETER	CONDITIONS	2620			2622			2625			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 3)	$R_S \leq 10k\Omega$		0.5	4		3	5		3	5	mV
Input Offset Current			1	15		5	25		5	25	nA
Input Bias Current			1	15		5	25		5	25	nA
Input Resistance		65	500		40	300		40	300		MΩ
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = \pm10V$, $C_L = 50pF$	100K	150K		80K	150K		80K	150K		V/V
Gain Bandwidth (Notes 4 and 5)	$R_L = 2k\Omega$, $C_L = 50pF$		100			100			100		MHz
Full Power Bandwidth	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = 20V_{p-p}$	400	600		320	600		320	600		KHz
Rise Time (Note 6)	$R_L = 2k\Omega$, $C_L = 50pF$		17	45		17	45		17	45	ns
Slew Rate (Note 6)	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = \pm5.0V$	±25	±35		±20	±35		±20	±35		V/μs
Output Current	$V_O = \pm10V$	±15	±22		±10	±18		±10	±18		mA
Supply Current			3	3.7		3	4		3	4	mA
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leq 10k\Omega$			6			7			7	mV
Input Offset Current			5	35			60			40	nA
Input Bias Current			10	35			60			40	nA
Common Mode Rejection Ratio	$V_{CM} = \pm5V$	80	100		74	100		74	100		dB
Common Mode Range		±11			±11			±11			V
Supply Voltage Rejection Ratio	$V_{Supply} = \pm9V$ To $\pm15V$	80	90		74	90		74	90		dB
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = \pm10V$, $C_L = 50pF$	70k			60k			70k			V/V
Output Voltage Swing	$R_L = 2k\Omega$, $C_L = 50pF$	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Derate TO-91 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.

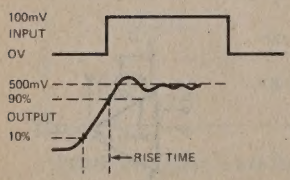
NOTE 3: May be externally adjusted to zero.

NOTE 4: $V_O < 90mV$.

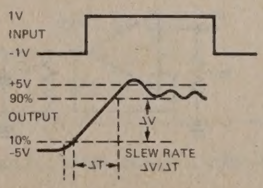
NOTE 5: 40dB gain.

NOTE 6: $A_V = 5.0V$.

TRANSIENT RESPONSE

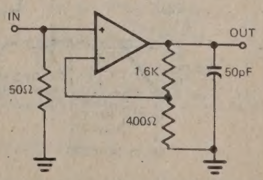


SLEW RATE

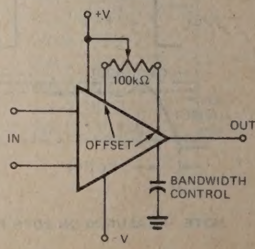


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP



INTERSIL

HA2607/2627
Wide Band Operational Amplifier Series

FEATURES

	HA-2607	HA-2627	
• **Wide gain-bandwidth**	**12**	**100**	**MHz**
• **High slew rate**	**7**	**35**	**V/μs**
• **Wide power bandwidth**	**75**	**600**	**KHz**
• **High gain**	**150KV/V**		
• **High input impedance**	**500M Ω**		
• **Output short circuit protection**			

ORDERING INFORMATION

HA3-2607-5	8 pin minidip
HA3-2627-5	8 pin minidip

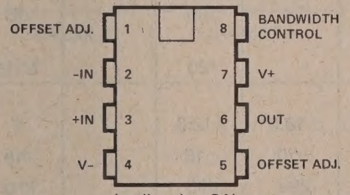
DESCRIPTION

HA-2607/2627 bipolar operational amplifiers are high performance, epoxy-packaged monolithic IC's designed to deliver outstanding wideband AC performance. HA-2607 has a specified bandwidth of 12MHz while HA-2627 has a typical gain-bandwidth of 100MHz!* HA-2607 and HA-2627 also offer correspondingly high slew rates of 7V/μ Sec and 35V/μ Sec respectively. These dynamic characteristics, coupled with 150,000V/V open-loop gain enables HA-2607/2627 to perform high-gain amplification of very fast, wideband signals.

The HA-2607 and HA-2627 op amps afford an economical means of designing high performance equipment for industrial and commercial use. These amplifiers are ideally suited to pulse amplification designs as well as high frequency (e.g. RF, video) applications. The frequency response of both amplifiers can be tailored to exact design requirements by means of an external bandwidth control capacitor.

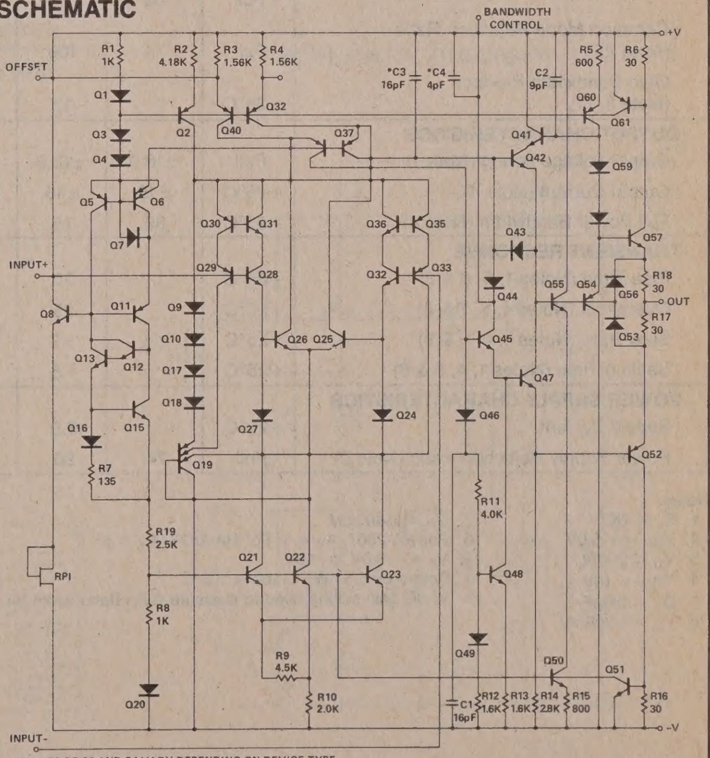
*HA-2607/2627 are internally compensated—HA-2607 is stable for $A_V \geq 1$,—HA-2627 is stable for $A_V \geq 5$.

PIN CONFIGURATION


OFFSET ADJ.
1
8
BANDWIDTH CONTROL
-IN
2
7
V+
+IN
3
6
OUT
V-
4
5
OFFSET ADJ.

(outline dwg PA)

SCHEMATIC


BANDWIDTH CONTROL
+V
OFFSET
R1 1K
R2 4.18K
R3 1.56K
R4 1.56K
*C3 16pF
*C4 4pF
C2 9pF
R5 600
R6 30
Q1
Q2
Q32
Q40
Q37
Q41
Q42
Q60
Q61
Q59
Q3
Q4
Q5
Q6
Q7
Q30
Q31
Q36
Q35
Q43
Q57
INPUT+
Q29
Q28
Q32
Q33
Q44
Q55
Q54
Q56
R18 30
OUT
R17 30
Q53
Q8
Q11
Q9
Q10
Q26
Q25
Q45
Q13
Q12
Q17
Q47
Q18
Q16
Q15
Q27
Q24
Q46
Q52
R7 135
Q19
R11 4.0K
R19 2.5K
RPI
Q21
Q22
Q23
Q48
R8 1K
R9 4.5K
Q49
Q50
Q51
R10 2.0K
C1 16pF
R12 1.6K
R13 1.6K
R14 2.8K
R15 800
R16 30
Q20
-V
INPUT-

*VALUES OF C3 AND C4 VARY DEPENDING ON DEVICE TYPE.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals 45.0V
Differential Input Voltage .... ±12.0V
Peak Output Current...... Full Short Circuit Protection
Internal Power Dissipation (Note 10) 300mW
Operating Temperature Range—
HA-2607/HA-2627 .... $0° \leq T_A \leq +75°C$
Storage Temperature Range ... $-65°C \leq T_A \leq +150°C$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS $V^+ = +15VDC$, $V^- = -15VDC$

		HA-2607 0°C to +75°C			HA-2627 0°C to +75°C			
		LIMITS						
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		4	6		4	6	mV
	Full			8			8	mV
Offset Voltage Average Drift	Full		5			5	30	nA
Bias Current	+25°C		5	30		5	30	nA
	Full			50			50	
Offset Current	+25°C		5	30		5	30	nA
	Full			50			50	nA
Input Resistance	+25°C	40	300		40	300		MΩ
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1)	+25°C	70	150K		70	150K		V/V
	Full	60			60			V/V
Common Mode Rejection Ratio (Note 2)	Full	74	100		74	100		dB
Gain Bandwidth Product (Note 3, 11)	+25°C		12			100		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4)	+25°C	50	75		290	600		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		17	45	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40	%
Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±4	±7		±17	±35		V/μs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		1.5			1.5		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	74	90		74	90		dB

Notes:

1. $R_L = 2K$
2. $V_{CM} = +5.0V$
3. $V_O < 90mV$
4. $V_O = +10V$
5. $C_L = 100pF$
6. $V_L = +200mV$
7. $V_O = +400mV$
8. For HA-2607, $A_V = 1$; For HA-2627, $A_V = 5$.
9. $V_S = +9.0V$ to $+15V$
10. Derate by 6.6mW/°C above 105°C
11. 40 dB gain setting used to measure Gain-Band width for HA-2627

LM4250C
Programmable Operational Amplifier

FEATURES

- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programable electrical characteristics
- Offset Voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

GENERAL DESCRIPTION

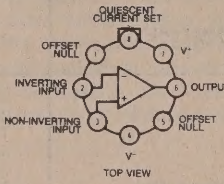
The 4250 is an extremely versatile programable monolithic operational amplifier. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product.

The 4250C is guaranteed over a 0°C to 70°C temperature range.

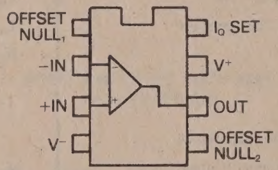
ORDERING INFORMATION

Dice	8 Pin Minidip	TO-99 Can
LM4250C/D	LM4250CN	LM4250CH

PIN CONFIGURATIONS

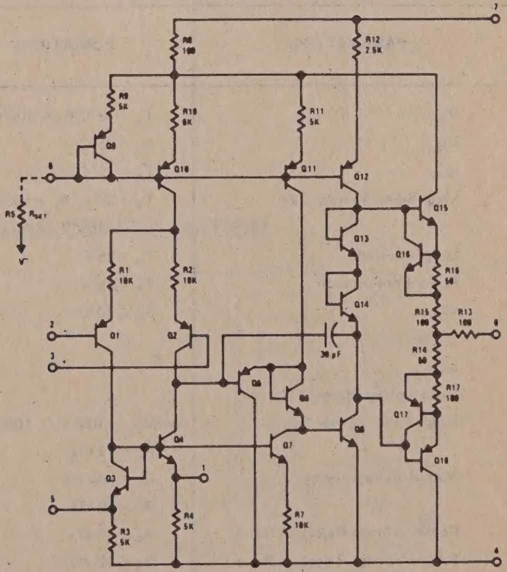

QUIESCENT CURRENT SET
8
OFFSET NULL
1
V+
7
INVERTING INPUT
2
OUTPUT
6
NON-INVERTING INPUT
3
OFFSET NULL
5
4
V−
TOP VIEW

(outline dwg TO-99)


OFFSET NULL$_1$
I$_Q$ SET
−IN
V+
+IN
OUT
V−
OFFSET NULL$_2$

(outline dwg PA)

SCHEMATIC DIAGRAM


7
R8 100
R12 2.5K
R9 5K
R10 5K
R11 5K
Q9
8
Q10
Q11
Q12
R5 R$_{SET}$
V−
Q15
Q13
Q16
R16 50
R1 10K
R2 10K
Q14
R15 100
R13 100
6
2
Q1
Q2
R14 50
3
30 pF
Q5
Q6
R17 100
Q8
Q17
Q4
Q7
Q18
1
Q3
5
R4 5K
R7 10K
R3 5K
4

RESISTOR BIASING

Set Current Setting Resistor to V$^-$

	I_{SET}				
V_S	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V	Output Short Circuit Duration	Indefinite
Power Dissipation (Note 1)	500 mW	Operating Temperature Range	0°C $\leq T_A \leq$ 70°C
Differential Input Voltage	±30V	Storage Temperature Range	−65°C to 150°C
Input Voltage (Note 2)	±15V	Lead Temperature (Soldering, 10 sec)	300°C
I_{SET} Current	150μA		

ELECTRICAL CHARACTERISTICS (0°C $\leq T_A \leq$ 70°C unless otherwise specified)

PARAMETERS	CONDITIONS	V_S = ±1.5V			
		I_{SET} = 1 μA		I_{SET} = 10 μA	
		MIN	MAX	MIN	MAX
V_{OS}	T_A = 25°C R_S < 100 kΩ		5 mV		6 mV
I_{OS}	T_A = 25°C		6 nA		20 nA
I_{bias}	T_A = 25°C		10 nA		75 nA
Large Signal Voltage Gain	T_A = 25°C R_L = 100 kΩ	25k			
	V_O = ±0.6V R_L = 10 kΩ			25k	
Supply Current	T_A = 25°C		8 μA		90 μA
Power Consumption	T_A = 25°C		24 μW		270 μW
V_{OS}	R_S < 10 kΩ		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	V_O = ±0.6V R_L = 100 kΩ	25k			
	R_L = 10 kΩ			25k	
Output Voltage Swing	R_L = 100 kΩ	±0.6V			
	R_L = 10 kΩ			±0.6V	
Common Mode Rejection Ratio	R_S < 10 kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	R_S < 10 kΩ	74 dB		74 dB	
Supply Current			8 μA		90 uA
Power Consumption			24 μW		270 uW

PARAMETERS	CONDITIONS	V_S = ±15V			
		I_{SET} = 1 μA		I_{SET} = 10 μA	
		MIN	MAX	MIN	MAX
V_{OS}	T_A = 25°C R_S < 100 kΩ		5 mV		6 mV
I_{OS}	T_A = 25°C		6 nA		20 nA
I_{bias}	T_A = 25°C		10 nA		75 nA
Large Signal Voltage Gain	T_A = 25°C R_L = 100 kΩ	60k			
	V_O = ±10V R_L = 10 kΩ			60k	
Supply Current	T_A = 25°C		11 μA		100 μA
Power Consumption	T_A = 25°C		330 μW		3 mW
V_{OS}	R_S < 10 kΩ		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	V_O = ±10V R_L = 100 kΩ	50k			
	R_L = 10 kΩ			50k	
Output Voltage Swing	R_L = 100 kΩ	±12V			
	R_L = 10 kΩ			±12V	
Common Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq$ 10 kΩ	74 dB		74 dB	
Supply Current			11 uA		100 uA
Power Consumption			300 uW		3 mW

INTERSIL

IH5101
Ultra Low Noise High Frequency Amplifier

FEATURES

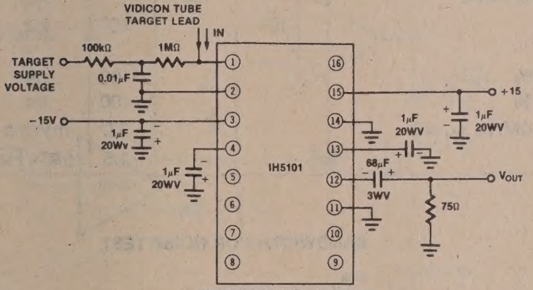
- **Input Noise Current ≤1.5pA/√Hz**
- **10MHz Bandwidth**
- **40dB Gain**
- **±15V Supply**

GENERAL DESCRIPTION

The IH5101 is specifically designed for transresistance amplifier applications. Its ultra low noise and high frequency capabilities make it ideal for vidicon head tube amplification; the low level current output of a vidicon head tube can be readily converted to a voltage level for system processing. For example, a 100nA tube output current will be transformed into 75mV of output voltage.

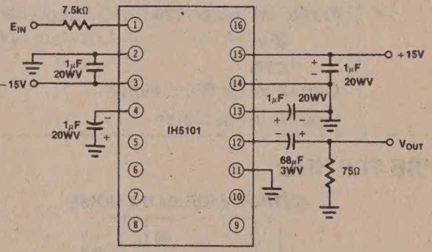
TYPICAL APPLICATIONS

VIDICON HEAD AMPLIFIER


VIDICON TUBE
TARGET LEAD
IN
100kΩ
1MΩ
TARGET
SUPPLY
VOLTAGE
0.01μF
−15V
1μF
20Wv
1μF
20WV
IH5101
+15
1μF
20WV
1μF
20WV
68μF
3WV
VOUT
75Ω
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

TRANSRESISTANCE = 0.75mV/nA

VIDEO AMPLIFIER WITH 40dB VOLTAGE GAIN


7.5kΩ
EIN
1μF
20WV
−15V
1μF
20WV
IH5101
+15V
1μF
20WV
1μF
20WV
68μF
3WV
VOUT
75Ω
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

ORDERING INFORMATION

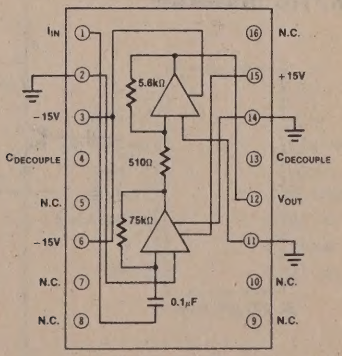
IH5101 M IE

Package
16-Pin DIP (.6 x .7 Lead Space)

Temperature Range
M — Military (−55°C to +125°C)
I — Industrial (−25°C to +85°C)

Device Type

PIN CONFIGURATION


IIN
−15V
CDECOUPLE
N.C.
−15V
N.C.
N.C.
N.C.
+15V
CDECOUPLE
VOUT
N.C.
N.C.
5.8kΩ
510Ω
75kΩ
0.1μF
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

(outline dwg IE)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Current	1mA
Peak Output Current	10mA
Power Dissipation (Note)	1W
Storage Temperature	−65°C to +150°C
Operating Temperature (M)	−55°C to +125°C
(I)	−25°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

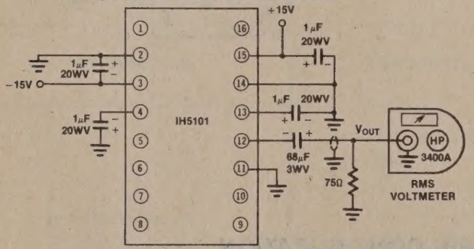
NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10mW/°C.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, (25°C unless otherwise noted)

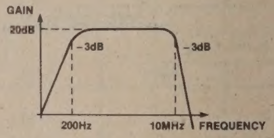
SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
$\Delta V_O / \Delta I_{IN}$	Transresistance (V_{OUT}/I_{IN})			0.75		mV/nA
I_Q	Power Supply Current (Quiescent) (Pins 3 and 15)	$I_{IN} = 0$			15	mA
Z_O	Output Impedance	f = 1MHz			10	Ω
ΔV_O	Output Swing	$R_L = 75\Omega$, f = 1MHz		1.0		V_{p-p}
BW	Bandwidth (3dB)	$R_L = 75\Omega$	10^2		10^7	Hz
	Transient Response (Step Response)	$R_L = 75\Omega$				
	$t_{(ON)}$	10% to 90%			100	ns
	$t_{(OFF)}$	90% to 10%			100	ns
	Output Wide Band Noise	100Hz to 10MHz, $I_{IN} = 0$			3.0	mVrms
i_n	Input Current Noise				1.5	pA/$\sqrt{Hz}$

NOISE TESTING

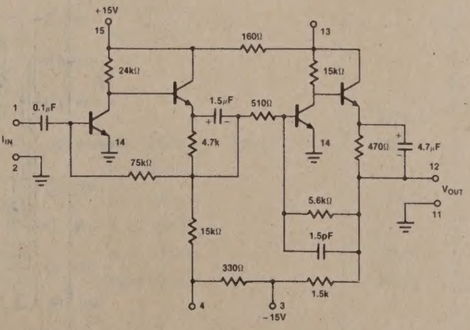
OUTPUT WIDE BAND NOISE


+15V
1μF 20WV
1μF 20WV
−15V
1μF 20WV
IH5101
1μF 20WV
VOUT
68μF 3WV
75Ω
HP 3400A
RMS VOLTMETER
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪ ⑫ ⑬ ⑭ ⑮ ⑯

BANDWIDTH FOR NOISE TEST



SCHEMATIC DIAGRAM


+15V
15
160Ω
13
24kΩ
15kΩ
1
0.1μF
1.5μF
510Ω
IIN
14
4.7k
14
470Ω
4.7μF
2
75kΩ
12
VOUT
5.6kΩ
11
15kΩ
1.5pF
330Ω
1.5k
4
3
−15V

IH5110 — IH5115
General Purpose Sample & Hold

FEATURES

- Low cost
- Military and industrial temperature ranges
- ±10V input voltage range
- 0.5mV/sec drift typical @ $C_S = 0.01\mu F$
- TTL, DTL and CMOS compatible
- Short circuit protected
- Input offset voltage adjustable to < 100μV using a 20k potentiometer
- 0.1% guaranteed sample accuracy with 10V signals and $C_S = 0.01\mu F$
- Sample to hold offset is 5mV max

SCHEMATIC DIAGRAM

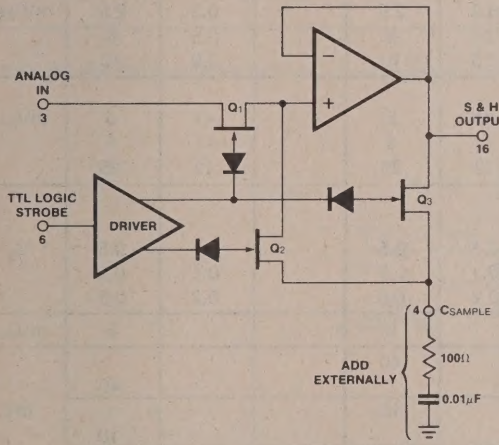

ANALOG IN
3
Q1
−
+
S & H OUTPUT
16
TTL LOGIC STROBE
6
DRIVER
Q3
Q2
4
CSAMPLE
ADD EXTERNALLY
100Ω
0.01μF

FIGURE 1

GENERAL DESCRIPTION

Each of the 5110 family is a complete Sample and Hold circuit, (except for sampling capacitor) including input buffer amplifier, output buffer amplifier and CMOS logic switching. The devices are designed to operate from ±15V and +5V supplies. The input logic is designed to "Sample" and "Hold" from standard TTL logic levels.

The design is such that the input and output buffering is performed by only one operational amplifier, by switching the sampling capacitor from the output back to input. Switches Q_1, Q_2, and Q_3 (see Fig. 1) accomplish this switching. In the sampling mode Q_1 and Q_3 are shorted and Q_2 is open; thus the op. amp. charges up the sampling capacitor. In the hold mode Q_1 and Q_3 are open and Q_2 is shorted; thus the sampling cap. is switched back to the non-inverting input of the op. amp.

This structure provides a very accurate d.c. gain of 1 with very fast settling times (i.e. 5μs); additionally the design has internal feedback to cancel charge injection effects (sample to hold offsets). Q_1 and Q_2 are driven 180 degrees out of phase to accomplish this charge nulling.

ORDERING INFORMATION

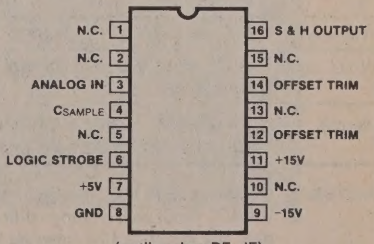
IH5110 M JE

Package
JE=16 pin CERDIP
DE=16 pin ceramic DIP (special order only)

Temperature Range
M=Military (−55°C to +125°C)
I =Industrial (−20°C to +85°C)

Device Chip Type

PIN CONFIGURATION


N.C. 1
N.C. 2
ANALOG IN 3
CSAMPLE 4
N.C. 5
LOGIC STROBE 6
+5V 7
GND 8
16 S & H OUTPUT
15 N.C.
14 OFFSET TRIM
13 N.C.
12 OFFSET TRIM
11 +15V
10 N.C.
9 −15V

(outline dwg DE, JE)

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±16V
Power Dissipation	500mW
Operating Temperature	−25° C to 85° C −55° C to 125° C
Storage Temperature Range	−65° C to 150° C
Lead Temperature (Soldering, 10 sec)	300 °C

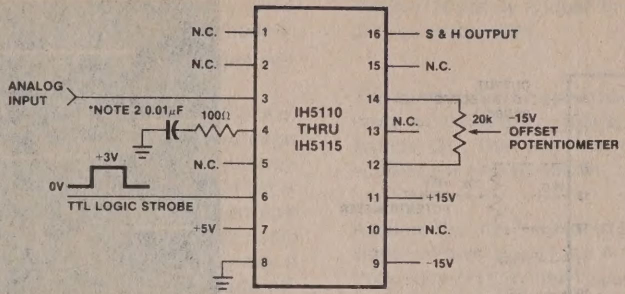
ELECTRICAL CHARACTERISTICS (Pin 7 = 5V, Pin 8 = GND, Pin 9 = −15V, Pin 11 = 15V, T_A = 25° C) Note 3

SYMBOL	CHARACTERISTIC	IH5110, 5112, 5114			IH5111, 5113, 5115			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Close	Aperature Time		120	200		120	200	ns
t_{acq}	Acquisition Time for Max Analog Voltage Step $C_S = 0.1\mu F$ (0.1% Accur.) $C_S = 0.01\mu F$ (0.1% Accur.) $C_S = 0.001\mu F$ (0.1% Accur.) See fig. 4		 25 4 4	 35 6 6		 25 4 4	 35 6 6	μs
V_{drift}	Drift Rate $C_S = 0.1\mu F$ $C_S = 0.01\mu F$ $C_S = 0.001\mu F$ See fig. 2		 0.3 0.5 2.0	 2.5 5 10		 0.3 0.5 2.0	 2.5 5 10	mV/sec
V_{inject}	Charge Injection or Sample to Hold Offsets $C_S = 0.1\mu F$ $C_S = 0.01\mu F$ $C_S = 0.001\mu F$ See Note 1 & fig. 3		 <1 <1 12	 5 5 25		 <1 <1 12	 5 5 25	mV_{p-p}
V_{switch}	Switching Transients or Spikes (Duration Less than 2μs) $C_S = 0.1\mu F$ $C_S = 0.01\mu F$ $C_S = 0.001\mu F$ See fig. 3		 0.1 0.1 0.2	 0.5 0.5 0.5		 0.1 0.1 0.2	 0.5 0.5 0.5	V_p
V_{couple}	A.C. Feedthrough Coupled to Output			5			5	mV_{p-p}
V_{offset}	D.C. Offset When in Sample Mode (Trimmable to 0m V With Ext. 20kΩ Potentiometer 5110			40				mV
	5111						40	
	5112			10				
	5113						10	
	5114			5				
	See fig. 2 5115						5	
R_{in}	Input Impedance in Hold or Sample Mode (f ≤ 10Hz)		100			100		MegΩ
$I_{\pm 15V}$	Plus or Minus 15V Supply Quiescent Current		3.4	6		3.4	6	mA
I_{5V}	5V Supply Quiescent Current		0.3	10		0.3	10	μA
V_{analog}	D.C. Input Voltage Range			±7.5			±10	
$V_{A.C.\ range}$	A.C. Input Voltage Range See Note 2 & fig. 5	15			20			V
I_{strobe}	TTL Logic Strobe Input Current in Either Hold or Sample Mode		0.1	10		0.1	10	μA

NOTES:
1. Offset voltage of op. amp. must be adjusted to 0mV (using 20kΩ potentiometer) before charge injection is measured.
2. The A.C. input voltage range differs from the D.C. input voltage range. All versions will handle any analog input within the range of plus 10V to minus 10V; however the IH5110, 5112, 5114 has the added restriction that the peak to peak swing should be less than $15V_{p-p}$ i.e. ±7.5 Vac.
3. All of the electrical characteristics specs, are guaranteed with $C_S = 0.01\mu F$ in series with 100Ω as per Fig. 2, $C_S = 0.1\mu F$ & $C_S = 0.001\mu F$ are for design aid only.
4. If supplies are reduced to ± 12VDC, analog signal range will be reduced to ± 7Vp-p.

APPLICATIONS INFORMATION

I. Typical Connection Diagram


N.C.
1
N.C.
2
ANALOG INPUT
3
*NOTE 2 0.01μF
100Ω
4
+3V
0V
N.C.
5
TTL LOGIC STROBE
6
+5V
7
8
IH5110
THRU
IH5115
16
S & H OUTPUT
15
N.C.
14
N.C.
13
20k
-15V
OFFSET
POTENTIOMETER
12
11
+15V
10
N.C.
9
-15V

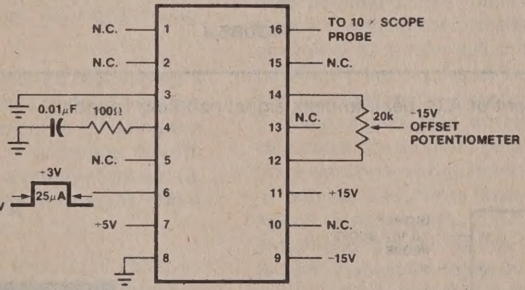
NOTES: **1.** To trim output offset to 0mV, set strobe input to sample mode (3V), set analog input to GND, adjust potentiometer until S & H output is 0mV.

2. Use a low dielectric absorption capacitor such as polystyrene.

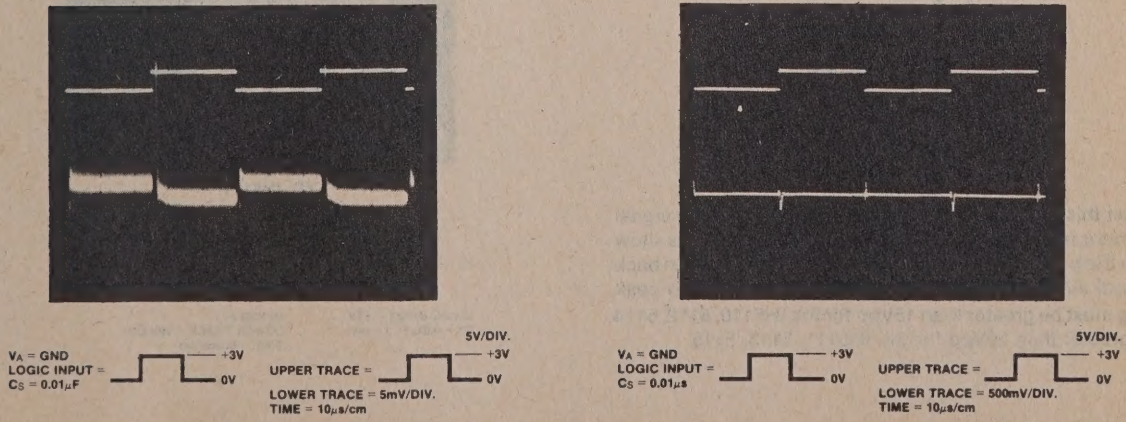
SAMPLE MODE occurs when logic input is greater than 2.4V.
HOLD MODE occurs when logic input is less than 0.8V.

FIGURE 2

II. Charge Injection (sample to hold offset) measurement circuit; also switching transients test circuit.


N.C.
1
N.C.
2
3
0.01μF
100Ω
4
N.C.
5
+3V
0V
25μA
6
+5V
7
8
16
TO 10 × SCOPE PROBE
15
N.C.
14
N.C.
13
20k
-15V
OFFSET
POTENTIOMETER
12
11
+15V
10
N.C.
9
-15V

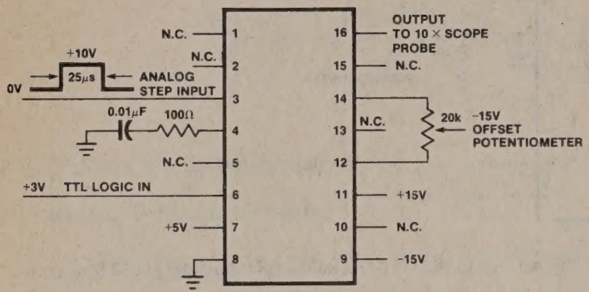
Adjust offset to 0mV before testing for charge injection. See note 1.


CHARGE INJECTION

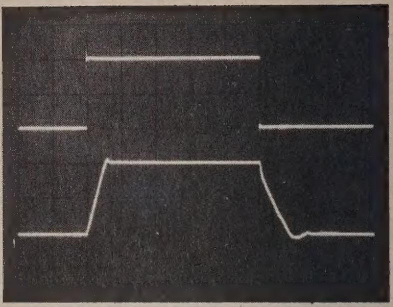
SWITCHING TRANSIENTS

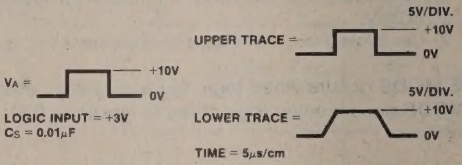
FIGURE 3

III. Typical Circuit for measurement of A.C. signal handling capability.


N.C.
1
+10V
N.C.
2
25μs
ANALOG STEP INPUT
0V
3
0.01μF
100Ω
4
N.C.
5
+3V TTL LOGIC IN
6
+5V
7
8
16
OUTPUT TO 10 × SCOPE PROBE
15
N.C.
14
N.C.
13
12
20k
−15V
OFFSET POTENTIOMETER
11
+15V
10
N.C.
9
−15V

ACQUISITION TIME

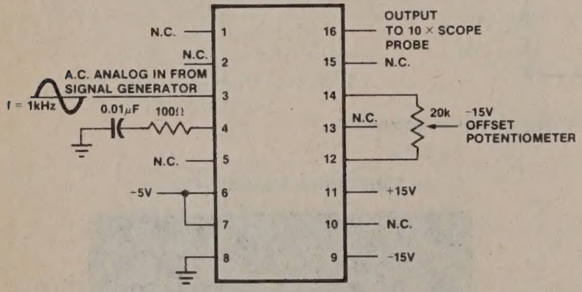




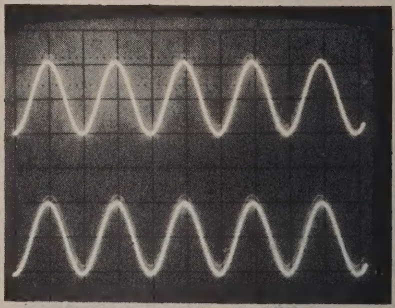
NOTE: The acquisition time is actually a settling time spec. since the reading is only taken when the output has settled within 1% of its final value. The 6μs spec. (IH5111, 5113 & 5115 is the worst reading of the t_{on} or t_{off} settling time shown above. The above test can be performed with a 0 to +7.5V or 0 to −7.5V step for the IH5110, 5112, 5114.

FIGURE 4

IV. Typical Circuit for measurement of A.C. peak to peak signal handling capability.


N.C.
1
N.C.
2
A.C. ANALOG IN FROM SIGNAL GENERATOR
3
f = 1kHz
0.01μF
100Ω
4
N.C.
5
−5V
6
7
8
16
OUTPUT TO 10 × SCOPE PROBE
15
N.C.
14
N.C.
13
12
20k
−15V
OFFSET POTENTIOMETER
11
+15V
10
N.C.
9
−15V

A.C. PEAK TO PEAK



TYP. IH5111

To test this parameter, increase the amplitude of the signal generator until the output starts to distort (it will always show up on the positive excursion of the sine wave first); then back off until all distortion is gone. The resultant peak to peak swing must be greater than 15Vpp for the IH5110, 5112, 5114 and greater than 20Vpp for the IH5111, 5113, 5115.

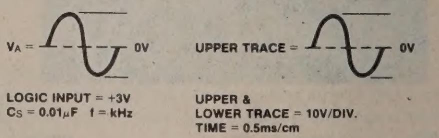

V_A =
0V
UPPER TRACE =
0V
LOGIC INPUT = +3V
Cs = 0.01μF f = kHz
UPPER & LOWER TRACE = 10V/DIV.
TIME = 0.5ms/cm

FIGURE 5

V. Application Tips:

If you are undecided as to which sample and hold to use within the family, the following will give you a pretty good idea of the outstanding differences between the six models.

First, determine the voltage range you need to sample and hold.

The even numbered parts are designed to switch smaller a.c. signal amplitudes with the goal being to minimize the charge injection effects (sample to hold offsets). This charge injection error is shown in Fig. 3. Once the voltage offset is zeroed, the 5110 has typical error amplitudes of 1 to 2mVp-p (corresponds to 10pc to 20pc of charge). Thus one could sample very low level d.c. signals with extreme accuracy. If very low level a.c. signals are being sampled, voltage offset potentiometer can be adjusted for a zero charge injection effect. Once the potentiometer has been adjusted, there will be a zero error going from sample to hold; however there will be a d.c. error caused by adjusting the potentiometer for zero charge injection and not for zero voltage offset. In general, this d.c. error will be in the area of 2mV to 5mV.

The odd numbered parts are primarily designed to handle any input in the plus or minus 10V range, regardless of whether it is a.c. or d.c.; to obtain this, the charge injection is about a factor of 2 higher than the even numbered parts.

The use of Varafet switching elements similar to Intersil's IH401/401A leads to a trade-off between AC signal swing and charge injection.

After the voltage range and charge injection requirements have been determined, all that remains is to determine the input offset voltage the system can tolerate. By using the higher numbered parts, it is possible to eliminate the offset potentiometer if system accuracy will allow 5mV (5114, 5115) or 10mV (5112, 5113) due to the low input offset voltage on these devices.

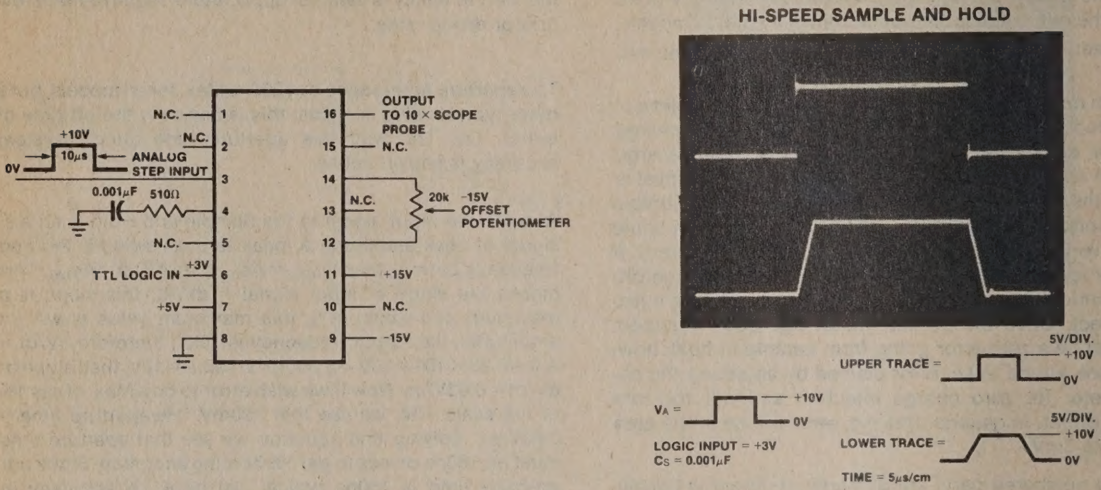
The drift rate is specified at 10mV/sec. Max. for all models: this corresponds to approximately 100pA total leakage into a 0.01μF sampling capacitor (C_S). While the 10mV/sec. is the Max. encountered, a more typical reading is less than 1mV/sec. (true for any input between −10V and +10V); thus the IH5110 family is ideal for applications requiring very low drift or droop rates.

The aperture time is spec'd at 200ns Max. for all models, but a more typical value is 150ns; this is basically the off time of switch Q_1. The way this aperture time affects system accuracy is shown below:

Assume the input signal to the Sample and Hold is an a.c. signal of peak amplitude A (peak to peak swing is 2A) and frequency $2\pi f = w$, then $V_{input} = Ae_{jwt}$ then $dV/dt = Ae_{jwt}$. This means the slope of input signal = dV/dt; this slope is a maximum at t (time) = 0, this maximum value is wA (in amplitude). (i.e.) input frequency is 10kc, therefore dV/dt = $wA = 6.28 \times 10^4 \times 10V = 6.3 \times 10^5 V/sec.$ A = 10V, then slope or dV/dt = 0.63V/μs. Now if we wish error to be a Max. of say 1% of full scale 10V, we see that 100mV (1%/aperture time = 0.63V/μs. Solving this equation we see that aperture time must be 160ns or less to get 1% holding accuracy. Since our aperture time is 150ns typical, we have 1% accuracy in holding 10kHz varying signals; for signal frequencies 1kHz and less, Max. error is 0.1%. The simple interpretation of just how the off time of the switch causes this system error is due to the fact a finite time is required for the switch to react to a hold command; this reaction time manifests itself with a system voltage error because the time varying input signal is changing to a new value before the switch has actually turned off. (i.e.) in the above example off = 10kHz and A = 10V, suppose we gave the hold command (thru TTL logic) at t = 0 (a.c. signal goes thru zero pt.) At this point we have calculated the slope to be a Max. and equal to 0.63V/μs. If there were no aperture time error, we would read 0V at output of Sample and Hold; however because of finite time for switch to respond to hold command, 150ns passes before switch goes off. During this 150ns, the input signal has gone to 100mV above or below 0V, thus the stored value of signal will be 100mV and that is the reading at the output of the Sample and Hold. If the input frequency were 1kHz, the "error voltage" would be 10mV.

VI. Connection for Hi-Speed Sample and Hold with following typical performance: w/C_S = 0.001

a. 2μs settling time (acquisition time) to 1% accuracy
b. 25mV charge injection amplitude
c. 10mV/sec drift rate


HI-SPEED SAMPLE AND HOLD

N.C.
+10V
N.C.
0V
10μs
ANALOG STEP INPUT
0.001μF
510Ω
N.C.
TTL LOGIC IN
+3V
+5V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
OUTPUT TO 10 × SCOPE PROBE
N.C.
N.C.
20k
-15V
OFFSET POTENTIOMETER
+15V
N.C.
-15V
5V/DIV.
UPPER TRACE =
+10V
0V
V_A =
+10V
0V
5V/DIV.
LOWER TRACE =
+10V
0V
LOGIC INPUT = +3V
C_S = 0.001μF
TIME = 5μs/cm

NOTE: Typical times for the Sample and Hold to acquire the input are 2μs for turn on (output) goes to +10V and 3μs for turn off (output goes down to 0V). As a general note, all the electrical specifications are guaranteed with a sampling capacitor equal to 0.01μf. As the above application (Fig. 6) shows, other values of sampling capacitors can be used but the best combinations of S & H specs may not result with values other than 0.01μF. The only advantage of using a 0.001μF for C_S is the acquisition time is 2μs typical instead of 5μs typical (with 0.01μF; however the drift rate would be worse and charge injection would be affected). To minimize drift rate, use a 0.1μF capacitor; this should produce a 0.1mV/sec rate of change and a charge injection amplitude of 0.2mVp-p. Of course the acquisition time will be slowed down to the 25μs area. Also use a 0.1μs system for slow speed changes (i.e., input frequency is less than 1kHz. The series resistor should be about 100Ω-200Ω to stabilize the system.

FIGURE 6

DEFINITION OF TERMS

Aperture Time: The time it takes to switch from sample mode to hold mode and the actual opening of switch.

Charge Injection: The amount of charge coupled across the switch with no input voltage.

Drift Rate: The amount of drift of output voltage at a rate caused by current flow through the storage capacitor.

$\left(\frac{dV}{dt} = \frac{i}{c}\right)$ This current is the leakage across the switch and the amplifier's bias current.

Feed Through: The amount of input signal that appears at the output when in the hold mode. Normally caused by capacitance across the switch.

Offset Voltage: Voltage measured at output with no input voltage and circuit in sample mode.

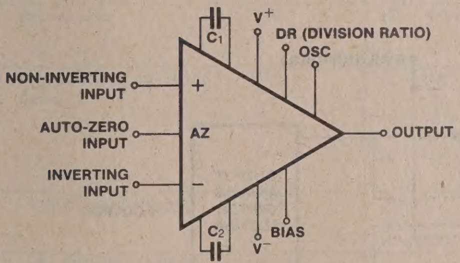
Acquisition Time: The time it takes amplifier to reach full scale output either plus or minus.

ICL7600/ICL7601
Commutating Auto-Zero (CAZ) Operational Amplifier

FEATURES

- **Exceptionally low input offset voltage -- 2 μV**
- **Low long-term input offset voltage drift -- 0.2 μV/year**
- **Low input offset voltage temperature drift -- 0.005 μV/°C**
- **Low DC input bias current -- 300 pA**
- **Low DC input offset bias current -- 150 pA**
- **Wide common mode and differential input voltage ranges**
- **Excellent low supply voltage operation -- Down to ±2V**
- **Static-protected inputs -- no special handling required**
- **Fabricated using proprietary MAXCMOS™ technology**
- **Compensated (ICL7600) or uncompensated (ICL7601) versions**

SYMBOL



GENERAL DESCRIPTION

The ICL7600/ICL7601 commutating auto-zero (CAZ) operational amplifiers are designed to replace almost any of today's hybrid or monolithic ultra-low offset op amps, and will provide almost three orders of magnitude reduction in input offset voltage compared with conventional device designs. This is achieved through Intersil's CAZ amp principle, an entirely new approach to low-frequency operational amplifier design.

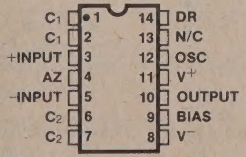
The key feature of the CAZ principle is automatic compensation for long-term drift phenomena and temperature effects. Two internal op amps are connected so that when one amplifier is processing an input signal the other is maintained in an "auto-zero" mode. The ICL7600/ICL7601 contains all of the circuitry required for system operation, including an oscillator, a counter, level translators, analog switches and operational amplifiers. Only two auto-zero capacitors are needed for complete operational amplifier function. Control of the oscillator and counter section is provided through the OSC and DR (division ratio) terminals. Internal biasing of the two on-chip op amps is programmable through a three-voltage-level terminal designated BIAS.

The ICL7600 is internally-compensated and is intended for applications which require voltage gains from unity through 20. The uncompensated ICL7601 is intended for those situations which require voltage gains of greater than 20. Major advantage of the ICL7601 over the ICL7600 at high gain settings is the reduction in commutation noise and subsequent greater accuracy.

Minimum periodic adjustments and extremely low offset voltage and temperature coefficients make the CAZ operational amplifiers very desirable for operation in adverse environments (temperature, humidity, toxic or radioactive) where equipment service is difficult. Since the device will auto-zero its internal offset errors, no adjustment is required other than that of gain, which is established by the external resistors.

PIN CONFIGURATION

(outline dwg JD, PD)



ORDERING INFORMATION

Order parts by the following part numbers:

Compensated	Uncompensated	Package	Temperature Range
ICL7600 CPD	ICL7601 CPD	Plastic	0°C to +70°C
ICL7600 IJD	ICL7601 IJD	CERDIP	−25°C to +85°C
ICL7600 MJD	ICL7601 MJD	CERDIP	−55°C to +125°C

Order dice by following part numbers: ICL7600/ICL7601/D

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (sum of both positive and negative supply voltages, V^+ and V^-)	18 Volts
DR Input Voltage	(V^+ +0.3) to (V^+ −8) Volts
Input Voltage (C_1, C_2, +INPUT, −INPUT, BIAS, OSC (Note 1))	(V^+ +0.3) to (V^- −0.3) Volts
Differential Input Voltage (Note 1)	±(V^+ +0.3) to (V^- −0.3) Volts
Duration of Output Short Circuit (Note 2)	Unlimited
Continuous Total Power Dissipation at or below +25°C free air temperature (Note 3)	
CERDIP Package	500 mW
Plastic Package	375 mW
Operating Temperature Range (ICL7600/ICL7601/MJD)	−55°C to +125°C
Operating Temperature Range (ICL7600/ICL7601/IJD)	−25°C to +85°C
Operating Temperature Range (ICL7600/ICL7601/CPD)	0 to +70°C
Storage Temperature Range	−55 to +150°C
Lead Temperature (soldering, 60 seconds)	+300°C

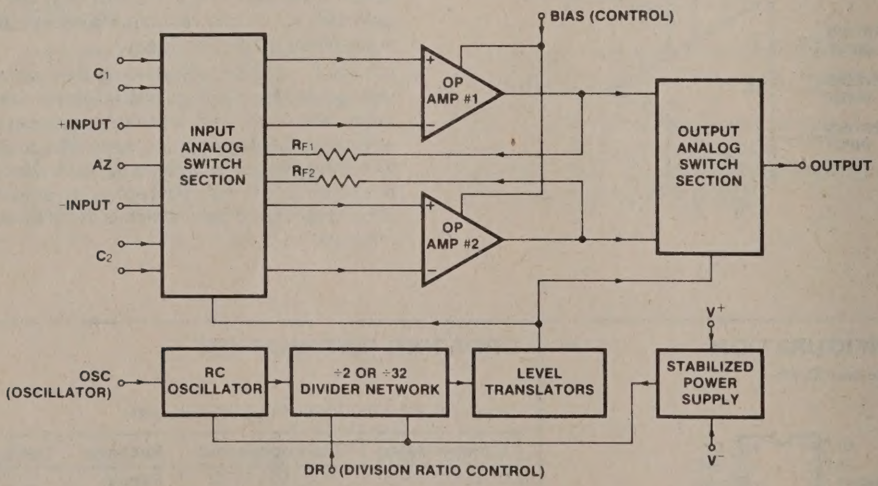
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: An SCR structure is inherent in the CMOS process used in the fabrication of these devices. If voltages in excess of (V^+ +0.3) to (V^- −0.3) volts are connected to either inputs or outputs, destructive latchup can occur. For this reason it is recommended that no inputs from sources not on the same power supply or supplies be applied before the ICL7600/ICL7601 supplies are established, and that if multiple supplies are used the ICL7600/ICL7601 supplies be activated first. No restrictions are placed on the differential input voltages on either the inverting or non-inverting inputs, so long as these voltages do not exceed the power supply voltages by more than 0.3V.

Note 2: Outputs may be shorted to ground (GND) or to either supply (V^+, V^-). Temperature and/or supply voltages must be limited to insure that the dissipation rating is not exceeded.

Note 3: For operation above 25°C free-air temperature, derate 4mW/°C from 500mW for CERDIP and 3mW/°C from 375mW for plastic.

BLOCK DIAGRAM

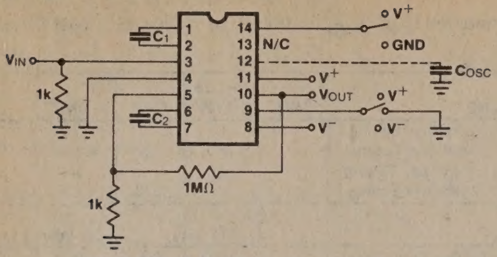

BIAS (CONTROL)
C1
+INPUT
AZ
−INPUT
C2
INPUT ANALOG SWITCH SECTION
RF1
RF2
+
OP AMP #1
−
+
OP AMP #2
−
OUTPUT ANALOG SWITCH SECTION
OUTPUT
V+
OSC (OSCILLATOR)
RC OSCILLATOR
÷2 OR ÷32 DIVIDER NETWORK
LEVEL TRANSLATORS
STABILIZED POWER SUPPLY
V−
DR (DIVISION RATIO CONTROL)

OPERATING CHARACTERISTICS:

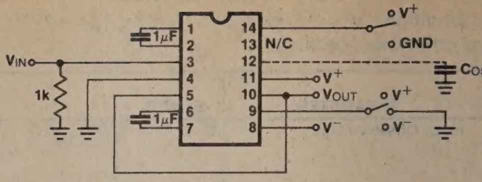
Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$), $C_1 = C_2 = 1\mu F$, Test Circuit 1, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS		VALUE		UNIT
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \le 1k\Omega$ Low Bias Setting		±2		μV
		$C_1 = C_2 = 1\mu F$ Med Bias Setting		±2	±5	μV
		High Bias Setting		±7		μV
		MIL version over temp. Med Bias Setting			±20	μV
Long Term Input Offset Voltage Stability	$V_{OS/Time}$	Low or Med Bias Settings		0.2		μV/year
Average Input Offset Voltage Temperature Coefficient	TCV_{OS}	Low or Med Bias Settings $-55°C > T_A > +25°C$		0.005	0.1	μV/°C
		$+25°C > T_A > +85°C$		0.01	0.1	μV/°C
		$+25°C > T_A > +125°C$		0.05	0.15	μV/°C
Noise Voltage (RMS)	e_n	Band Width Low Bias		0.8		μV
		0.1 to 10Hz Med Bias		0.8		μV
		$R_S \le 1k\Omega$ High Bias		1.0		μV
Equivalent Input Noise Voltage Peak-to-peak	e_{np-p}	Band Width Low Bias		4.0		μV
		0.1 to 10Hz Med Bias		4.0		μV
		$R_S \le 1k\Omega$ High Bias		5.0		μV
Spot equivalent Noise voltage	e_{n10}	f = 10Hz Band Width 1Hz			700	nV/√Hz
Spot equivalent Noise Current	i_{n10}	f = 10Hz Band Width 1Hz			0.1	pA/√Hz
Differential Input Voltage Range	DIF V_{IN}		$V^- - 0.3$	to	$V^+ + 0.3$	V
Common Mode Input Range	CMVR	Low Bias	−4.2		+4.2	V
		Med Bias	−4.0		+4.0	V
		High Bias	−3.5		+3.5	V
Common Mode Rejection Ratio	CMRR	Any Bias Setting		88		dB
Power Supply Rejection Ratio	PSRR	Any Bias Setting		110		dB
Non Inverting Input Bias Current	I_{NIB}	Any Bias Setting, (Includes charge injection currents)		0.300	3	nA
Inverting Input Bias Current	I_{IB}	Any Bias Setting, (Includes charge injection currents)		0.150	1.5	nA
Voltage Gain	A_V	$R_L = 100k\Omega$ Low Bias	90	105		dB
		Med Bias	90	105		dB
		High Bias	80	100		dB
Maximum Output Voltage Swing	V_{OUT}	$R_L = 1M\Omega$		±4.9		V
						V
		$R_L = 100k\Omega$		±4.8		V
						V
		$R_L = 10k\Omega$ Positive Swing	+4.4			V
		Negative Swing			−4.5	V
Large Signal Slew Rate	SR	Unity High Bias Setting		1.8		V/μs
		Gain Med Bias Setting		0.5		V/μs
		ICL7600 Low Bias Setting		0.2		V/μs
Unity Gain Band Width	GBW	High Bias Setting		1.2		MHz
		ICL7600 Med Bias Setting		0.3		MHz
		Test Circuit 2 Low Bias Setting		0.12		MHz
Extrapolated Unity Gain Band Width	GBW	High Bias Setting		1.8		MHz
		ICL7601 Med Bias Setting		0.4		MHz
		Low Bias Setting		0.2		MHz
BIAS Terminal Input Current	I_{BIAS}	$V^- - 0.3 \le V_{BIAS} \le V^+ + 0.3$ volt		±30		pA
BIAS Voltage to Define Current Modes	V_{BH}	Low Bias Setting	$V^+ - 0.3$	V^+	$V^+ + 0.3$	V
	V_{BM}	Med Bias Setting	$V^- + 1.4$	GND	$V^+ - 1.4$	V
	V_{BL}	High Bias Setting	$V^- - 0.3$	V^-	$V^- + 0.3$	V
DR (Division Ratio) Input Current	I_{DR}	$V^+ - 8.0V \le V_{DR} \le V^+ + 0.3V$		±30		pA
DR Voltage to define oscillator division ratio	V_{DRH}	Internal oscillator division ratio 32	$V^+ - 0.3$		$V^+ + 0.3$	V
	V_{DRL}	Internal oscillator division ratio 2	$V^+ - 8$		$V^+ - 1.4$	V
Nominal Commutation Frequency	f_{COM}	$C_{OSC} = 0$ pF DR Connected to V^+		160		Hz
		DR Connected to GND		2560		Hz
Supply Current	I_S	High Bias Setting		7	15	mA
		Medium Bias Setting		1.7	5	mA
		Low Bias Setting		0.6	1.5	mA
Operating Supply Voltage Range	$V^+ - V^-$	High Bias Setting	5		16	V
		Medium or Low Bias Setting	4		16	V

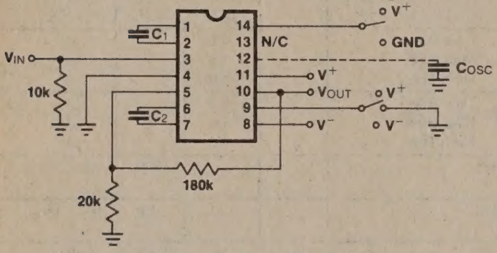
TEST CIRCUITS


V+
C1
1 2 3 4 5 6 7
14 13 12 11 10 9 8
N/C
GND
VIN
Cosc
V+
1k
VOUT
V+
C2
V−
V−
1MΩ
1k

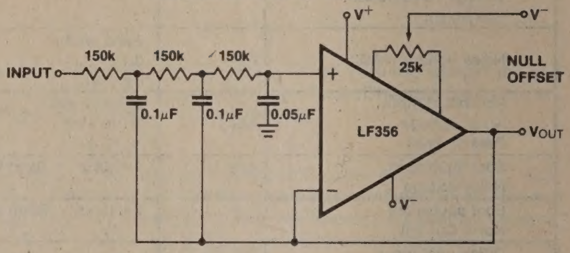
Test Circuit 1: Voltage Gain = 1000


V+
1µF
1 2 3 4 5 6 7
14 13 12 11 10 9 8
N/C
GND
VIN
Cosc
V+
1k
VOUT
V+
1µF
V−
V−

Test Circuit 2: Unity Voltage Gain


V+
C1
1 2 3 4 5 6 7
14 13 12 11 10 9 8
N/C
GND
VIN
Cosc
V+
10k
VOUT
V+
C2
V−
V−
180k
20k

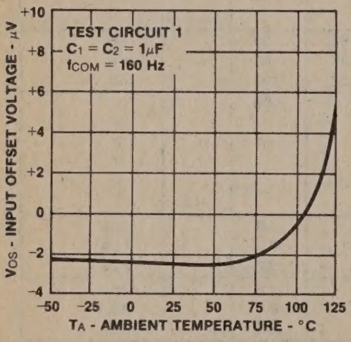
Test Circuit 3: Voltage Gain = 10


V+
V−
150k
150k
150k
INPUT
25k
NULL OFFSET
+
0.1µF
0.1µF
0.05µF
LF356
VOUT
−
V−

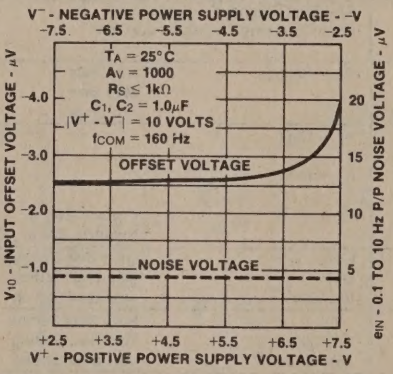
Test Circuit 4: DC to 10Hz Unity Gain Low Pass Filter

TYPICAL CHARACTERISTICS

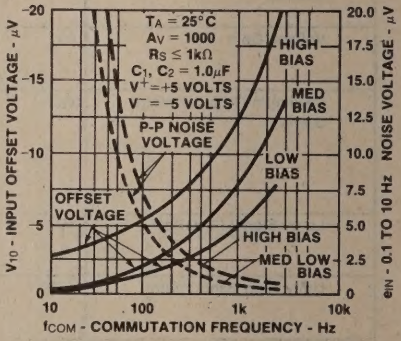
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



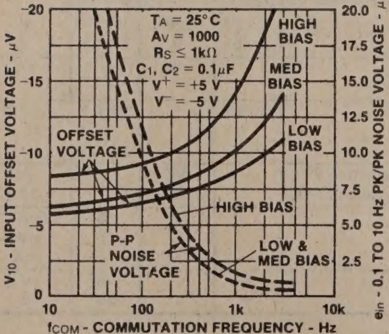
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



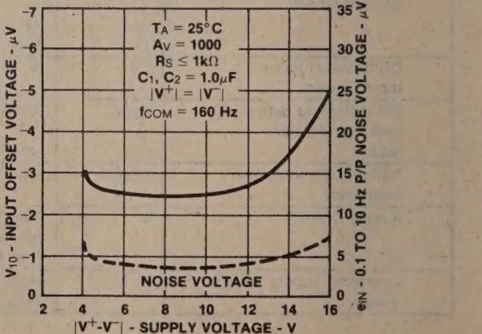
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 1µF)



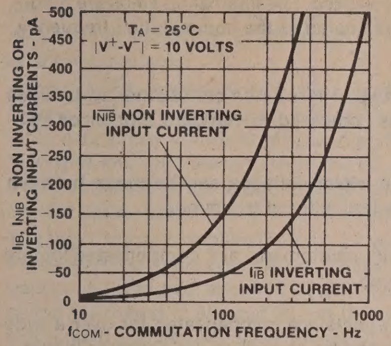
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 0.1µF)



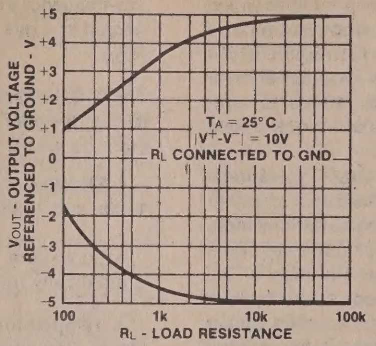
INPUT OFFSET VOLTAGE AND PK TO PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V^+-V^-)



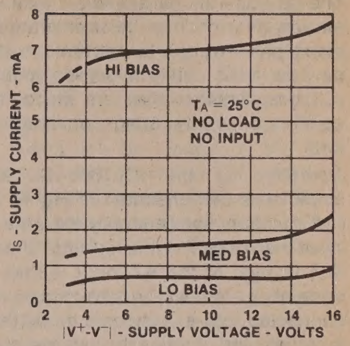
INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



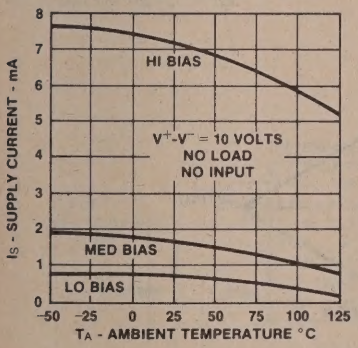
MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



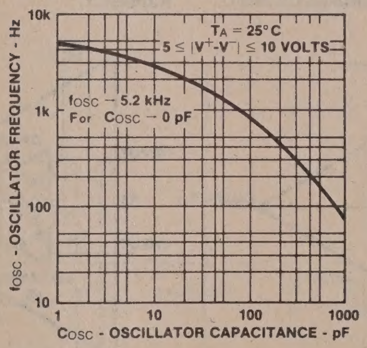
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



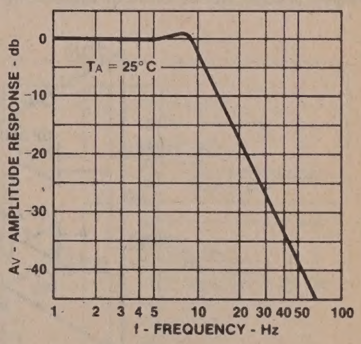
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



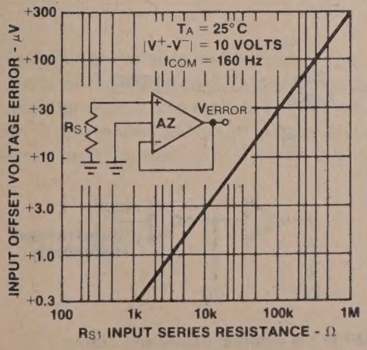
OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING



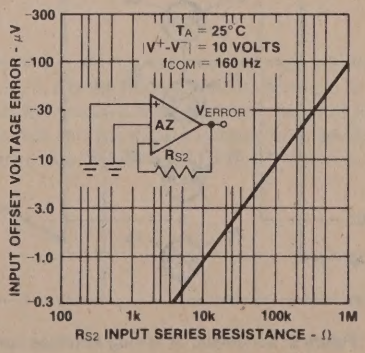
FREQUENCY RESPONSE OF THE 10 Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 4).



TOTAL EQUIVALENT INPUT OFFSET VOLTAGE AS A FUNCTION OF SOURCE IMPEDANCE — +INPUT



TOTAL EQUIVALENT INPUT OFFSET VOLTAGE AS A FUNCTION OF SOURCE IMPEDANCE — −INPUT



DETAILED DESCRIPTION

CAZ Operational Amplifier Operation

The CAZ operational amplifier functions on principles which are very different from those encountered in conventional op amp types. An important advantage of the ICL7600/ICL7601 devices is the ability to self-compensate for internal error voltages, whether they are steady-state, related to temperature or supply voltage, or variable in nature over a long term.

Operation of the ICL7600/ICL7601 CAZ operational amplifier is demonstrated in Figure 1. The basic amplifier configuration represented by the large triangles has one more input than does a regular op amp--the AZ, or auto-zero input. The voltage at the AZ input is that to which each of the internal op amps will be auto-zeroed. In Mode A, op amp #2 is connected into a unity gain mode through on-chip analog switches, and charges the external capacitor C_2 to a voltage equal to the DC offset voltage of that amplifier and the instantaneous low frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps in the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which was charged to a voltage equal to its offset and noise voltage) connected in series to its non-inverting (+) input and nulls out the input offset and noise voltage of the amplifier. While one of the op amps is processing the input signal, the other is placed in the auto-zero mode and charges its capacitor to a voltage equal to its equivalent DC and low-frequency error voltage. The internal op amps are reconnected at a rate designated as the commutation frequency, f_{COM}.

The CAZ amp concept offers a number of other advantages to the designer, as compared to standard bipolar or FET-input op amps:

- Effective input offset voltages can be made between 1000x and 10,000x less without trimming.
- Long-term drift phenomena are compensated for and dramatically reduced.
- Temperature effects are compensated for over a wide range. Reductions can be as high as 100 times or higher.
- Supply voltage sensitivity is reduced.

The on-chip op amps are connected internally to the external input and output terminals via CMOS analog switches, as shown in Figure 2. The analog switch structure shown in Figure 2 is arranged so that at any time three switches are open and three switches are conducting. Each analog switch includes a P-channel transistor in parallel with an N-channel transistor.

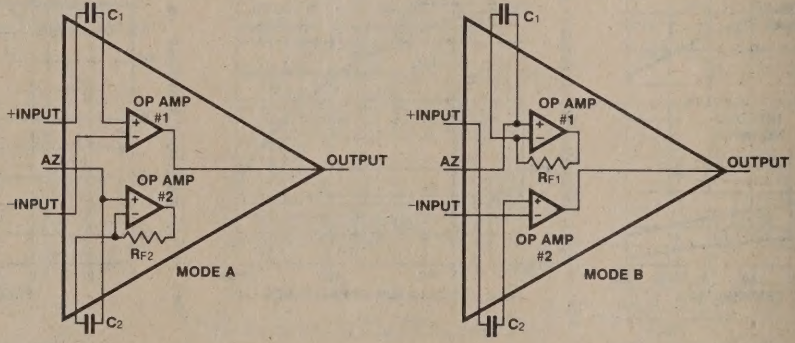


Figure 1: Diagramatic representation of the 2 half cycles of operation of the CAZ OP AMP.

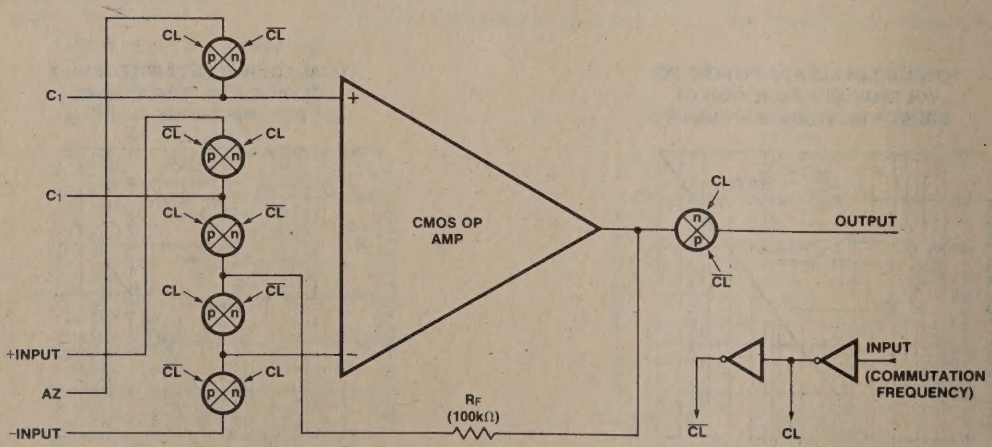


Figure 2: Schematic of analog switches connecting each internal OP AMP to the external inputs and output.

APPLICATIONS

The ICL7600/ICL7601 CAZ op amp is ideal for use as a front-end preamplifier for dual-slope A/D converters which require high sensitivity for single-ended input sources such as thermocouples.

A typical high-sensitivity A/D converter system is shown in Figure 3. The system uses an Intersil ICL7109 12-bit monolithic A/D binary converter, and is intended for direct interface with microprocessors. Both the ICL7600/ICL7601 and the ICL7109 use power supply voltages of ±5V, and the entire system consumes typically 2.5 mA of current.

The input signal is applied through a low-pass filter (150 Hz) to the CAZ op amp, which is connected in a non-inverting gain configuration of either 10 or 100. The internal oscillator of the CAZ amp is allowed to run free at about 5,200 Hz, resulting in a commutation frequency of 160 Hz, with the DR terminal connected to V^+. The error-storage capacitors C_1 and C_2 are each 1 μF value, and provide a good compromise between the minimum equivalent input offset voltage and the lowest value of low-frequency noise.

The output signal is then passed through a low-pass filter (1 MΩ and 0.1 μF), with a bandwidth of 1.5 Hz. This results in an equivalent DC offset voltage of 1 to 2 μV, and a peak-to-peak noise voltage of 1.7 μV, referred to the input of the CAZ amp. The output from the low-pass filter feeds directly into the input of the ICL7109.

In a system such as that shown in Figure 3 there is a degree of flexibility possible in assigning various gains to the ICL7600/ICL7601 pre-amplifier, and to various sensitivities for the ICL7109. For optimum performance, the CAZ op amp must amplify the input signal so that the equivalent 15μV input noise voltage of the A/D converter is masked. This implies a gain of at least 10 for the CAZ op amp preamplifier.

On the other hand, if the gain of the CAZ op amp is increased too much, its output swing will be limited by the ±5V supplies. This condition imposes a maximum gain of 200 to produce an output of ±0.000005 times 4,096 times 200, or ±4.096V, for a 5μV per count sensitivity. Use of an ICL7600 is recommended for low gains (<20) and the ICL7601 for gains of more than 20.

The values of the integrating resistor and the reference voltage must be chosen to suit the overall sensitivity of the system. For example, in a system requiring a sensitivity of 5μV per count, use a CAZ amp in a gain configuration of 50 (with ICL7601). Thus for a full scale count of 4096 (12 bits), the input voltage to the ICL7109 would be 5μV times 50 times 4096 or 1.024 volts. Since the ratio of input to reference is 2:1, the value of the reference voltage becomes 0.512 and a 50kΩ integrating resistor is recommended. A system such as that shown in Figure 3 will allow a resolution of 1°C for low sensitivity platinum/rhodium junctions. For 0.1°C resolution, use high sensitivity thermocouples having copper/constantan junctions.

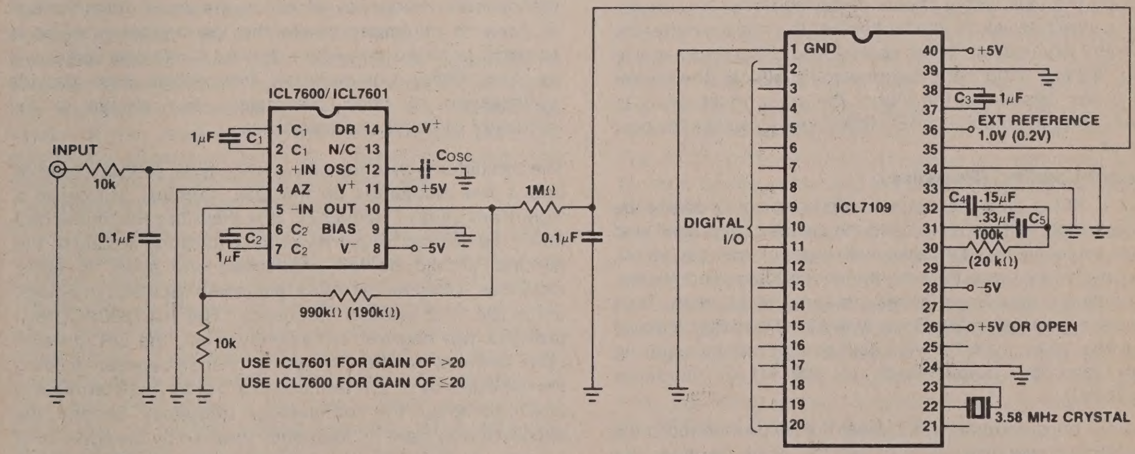


Figure 3: A/D system with 5μV resolution using an ICL7600/ICL7601 CAZ AMP preamplifier and an ICL7109 dual slope A/D converter.

The low-pass filter between the output of the CAZ op amp and the input of the ICL7109 A/D converter can be used to improve the signal-to-noise ratio of the system by reducing bandwidth. A 10 Hz filter will result in an equivalent peak-to-peak noise voltage figure of 4μV. If the bandwidth is reduced to 1.5 Hz, the peak-to-peak noise voltage will be reduced to about 1.7 μV, a reduction by a factor of three. The penalty for this reduction will be a longer system response time; however in most cases this will not be a major consideration, because of the large thermal inertia of many thermocouple probes.

SOME HELPFUL HINTS

Testing the ICL7600/ICL7601 CAZ Operational Amplifier

A simple and relatively accurate means of testing the CAZ op amp is to use a Tektronix Type 577 curve tracer, with the CAZ op amp inserted in a special 14-lead socket which plugs into a Tektronix 178, and which contains two soldered-in auto-zero capacitors of 1 μF each. This simple and convenient tester will provide most of the information needed for low-frequency parameters. The test setup will allow resolution of input offset voltages to about 10 μV.

For greater accuracy, it is suggested that a breadboard be built which minimizes thermoelectric effects and which includes an output low-pass filter of the type shown in Test Circuit #4. The output from the CAZ amp can be connected to a dual-slope A/D converter as shown in Figure 3. The low-frequency noise can then be displayed on a storage scope or on a strip chart recorder.

Bias Control

The on-chip op amps consume over 90% of the power required for the ICL7600/ICL7601. Three externally-programmable bias levels are provided. These levels are set by connecting the BIAS terminal to V^+, GND or V^-, for LOW, MED or HIGH BIAS levels, respectively. The difference between each bias setting is approximately a factor of three, which allows a 9:1 ratio between supply current and the bias setting. The reason for this current programmability is to provide the user with a choice of device power dissipation levels, slew rate values (the higher the slew rate the better the recovery from commutation spikes), and offset errors due to chip "voltage drop" and thermoelectric effects (the higher the power dissipation the higher the input offset error). In most cases, the medium (MED BIAS) setting will be the best choice.

Output Loading (Resistive)

With a 10 kΩ load the output swing can cover nearly the entire supply voltage range, and the device can be used with loads as low as 2 kΩ. However, with loads of less than 50 kΩ, the on-chip op amps become transconductance amplifiers, since their output impedances are about 50 kΩ each. Thus the open-loop gain is 20 dB less with a 2 kΩ load than it would be with a 20 kΩ load. For high gain configurations requiring high accuracy, output loads of 100 kΩ or more are suggested.

Another consideration which must not be overlooked is the additional power dissipation of the chip which results from a large output swing into a low value load. This added variable can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output to reduce high-frequency noise outside the signal passband of interest. With conventional op amps, the obvious solution would be to place a capacitor across the external feedback resistor to provide the low pass filter.

However, with the CAZ op amp, this is not feasible because of the nature of commutation voltage spikes. The voltage spikes show a low impedance characteristic in the direction of the auto-zero voltage, and a high impedance on the recovery edge, as shown in Figure 4. It can be seen that the effect of a large load capacitor is to produce an area error in the output waveform, and hence an effective gain error. The output low pass filter must be a high impedance type to avoid output voltage area errors. For example, a 1.5 Hz filter should use a 100 kΩ resistor and a 1.0 μF capacitor, or a 1.0 MΩ resistor and an 0.1μF capacitor. This effect also causes problems with integrator circuits.

Oscillator and Digital Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open-circuited. If the full divider network is used, this will result in a commutation frequency of about 160 Hz nominal. The commutation frequency is the frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents approximately the optimum frequency at which the input offset voltage is close to minimum, where the low-frequency noise is acceptable, and where errors derived from noise spikes will be low. Other commutation frequencies may provide optimization of other parameters, but always to the detriment of major characteristics.

The oscillator is of a high impedance type, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the desired frequency of the oscillation is 5.2kHz, the terminal should be left unattached and open. In other instances, it may be desirable to lock the oscillator to a clock or to run it at another frequency. The ICL7600/ICL7601 provides two degrees of flexibility. First, the DR (division ratio) terminal permits the user to choose between dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND), to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and V^+, or system ground terminals. For situations which require the commutation frequency to be locked onto a master clock, the OSC terminal can be driven from TTL logic

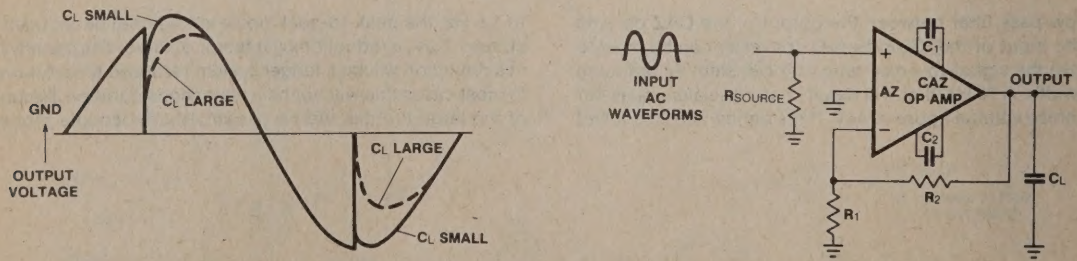


Figure 4: Effect of a load capacitor on output voltage waveforms.

(with resistive pull-up) or from CMOS logic, provided that the V^+ supply (with respect to ground) is +5V (±10%) and the logic driver also operates from a similar supply voltage. This is because the logic section -- including the oscillator -- operates from an internal −5V supply referenced to V^+ generated on-chip, and is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-precision DC amplifiers are thermoelectric, Peltier or thermocouple effects in junctions consisting of various metals, alloys, silicon, etc. Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1 μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can provide, it is essential to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. In addition, the supply voltages and power dissipation should be kept to a minimum. Use the medium bias mode as well as a high impedance load, and keep well away from heat dissipated by surrounding equipment.

Component Selection

The two required auto-zero capacitors, C_1 and C_2, should each be of 1.0 μF value. These are large values for non-electrolytic capacitors, but since the voltages impressed on them do not change significantly, problems of dielectric absorption and the like are not important.

Excellent results have been obtained in operation at commercial temperature ranges using several of the smaller-size and more economical capacitors, since the absolute values of the capacitors is not critical. Even polarized electrolytic capacitors rated at 1.0μF/50V, though not recommended, have been used with success.

Commutating Voltage Transient Effects

While in most respects the CAZ op amp behaves like a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 100 Hz. This is because of the finite switching transients which occur in the input and output terminals due to commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and include all of the higher harmonics. If the commutation frequency is higher than the highest in-band frequency, these transients can be effectively blanked with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage equal to the input offset voltage about (5-10mV) which occurs during the transition to the signal processing mode from the auto-zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must be at least 10,000 x 10 pF, or 0.1μF each.

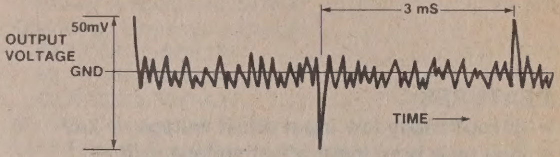


Figure 5: Output waveform from Test Circuit 1.

The charge which is injected into the op amp when it is switched into the signal-processing mode produces a rapidly-decaying voltage spike at the input, in addition to an equivalent DC bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically about 1.0 pA at ambient temperature of 25°C.

The output waveform of Test Circuit #1 (with no input) is shown in Figure 5. Note that the equivalent noise voltage shown is amplified 1000 times, and that because of the finite slew rate of the on-chip op amps the 7 mV input transients are not amplified by 1000.

The output transient voltage effects (as distinct from the input effects which are propagated through the on-chip op amps) will occur if there is a difference in the output voltage of the internal op amps between the auto-zero modes and the signal-processing modes. The output stage of the on-chip op amp must slew from its auto-zero output voltage to the desired signal-processing output voltage. This is shown in Figure 6, where the system is auto-zeroed to ground.

The duration of the output transients is greatly affected by the gain configuration and the bias setting, since these two parameters have an effect on system slew rate. At low gains and high bias settings, the output transient durations are very short. For this reason there are two versions of the CAZ op amp, the ICL7600 which is compensated for unity gain and which can be used for gain configurations up to 20, and the ICL7601, which is uncompensated and recommended for operation in gain configurations greater than 20. Thus, when a signal is being processed in a high gain configuration, the effective output signal error is greater for the ICL7600 than it is for the ICL7601.

Non-Amplifier Applications

In principle, this is one of the few "chopper-stabilized" type amplifiers that could be used as a comparator; the transient effects on the output will normally require careful synchronism of output strobes with oscillator drive.

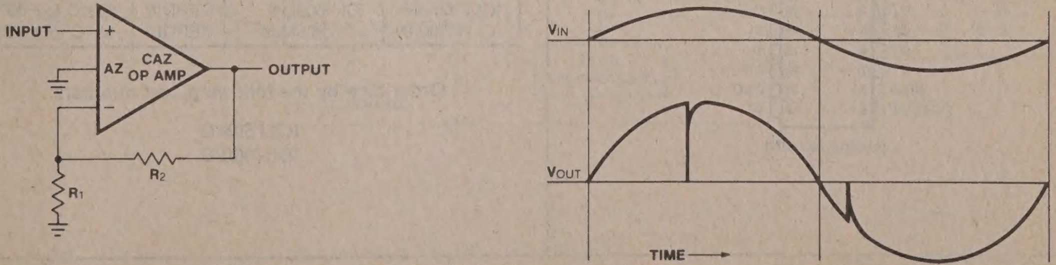


Figure 6: Simple CAZ OP AMP circuit and the output voltage waveform.

INTERSIL

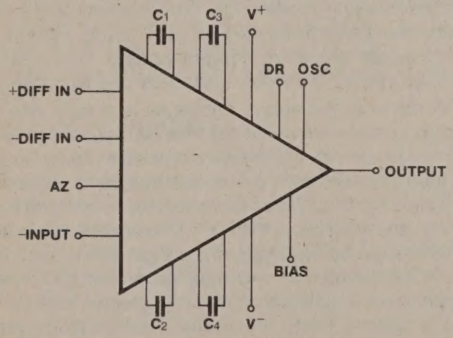
ICL7605/ICL7606

Commutating Auto-Zero (CAZ) Instrumentation Amplifier

FEATURES

- **Exceptionally low input offset voltage — 2μV**
- **Low long term input offset voltage drift — 0.2μV/year**
- **Low input offset voltage temperature drift — 0.05μV/°C**
- **Wide common mode input voltage range — 0.3V above supply rail**
- **High common mode rejection ratio — 100 dB**
- **Operates at supply voltages as low as ±2V**
- **Short circuit protection on outputs for ±5V operation**
- **Static-protected inputs — no special handling required**
- **Fabricated using proprietary MAXCMOS™ process technology**
- **Compensated (ICL7605) or uncompensated (ICL7606) versions**

SYMBOL



GENERAL DESCRIPTION

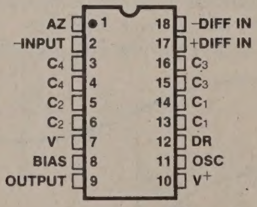
The ICL7605/ICL7606 commutating auto-zero (CAZ) instrumentation amplifiers are designed to replace most of today's hybrid or monolithic instrumentation amplifiers, for low frequency applications from DC to 10 Hz. This is made possible by the unique construction of this new Intersil device, which takes an entirely new design approach to low frequency amplifiers.

Unlike conventional amplifier designs, which employ three op amps and require ultra-high accuracy in resistor tracking and matching, the CAZ instrumentation amplifier requires no trimming except for gain. The key features of the CAZ principle involve automatic compensation for long term drift phenomena and temperature effects, and a flying capacitor input.

The ICL7605/ICL7606 is a monolithic CMOS chip which consists of two analog sections — a unity gain differential to single-ended voltage converter and a CAZ op amp. The first section senses the differential input and applies it to the CAZ amp section. This section consists of an operational amplifier circuit which continuously corrects itself for input voltage errors, such as input offset voltage, temperature effects, and long term drift.

The ICL7605/ICL7606 is intended for low-frequency operation in applications such as strain gauges, which require voltage gains from 1 to 1000 and bandwidths from DC to 10 Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. The no-adjustment feature, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

PIN CONFIGURATION



(outline dwg JN)

ORDERING INFORMATION

Order parts by the following part numbers:

Compensated	Uncompensated	Package	Temperature Range
ICL7605CJN	ICL7606CJN	CERDIP	0°C to +70°C
ICL7605IJN	ICL7606IJN	CERDIP	−25°C to +85°C
ICL7605MJN	ICL7606MJN	CERDIP	−55°C to +125°C

Order dice by the following part numbers:

ICL7605/D
ICL7606/D

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (sum of both positive and negative supply voltages V^+ to V^-)	18 Volts
DR Input Voltage	(V^+ +0.3) to (V^+ −8) Volts
Input Voltage (C_1, C_2, C_3, C_4 +DIFF IN, −DIFF IN, −INPUT, BIAS, OSC) (Note 1)	(V^+ +0.3) to (V^- −0.3) Volts
Differential Input Voltage (+DIFF IN to −DIFF IN) (Note 2)	+(V^+ +0.3) to (V^- −0.3) Volts
Duration of Output Short Circuit (Note 3)	Unlimited
Continuous Total Power Dissipation (at or below 25°C free-air temperature) (Note 4)	500 mW
Operating Temperature Range:	
ICL7605/ICL7606CJN	0 to +70°C
ICL7605/ICL7606IJN	−25°C to +85°C
ICL7605/ICL7606MJN	−55°C to +125°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering 60 seconds)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

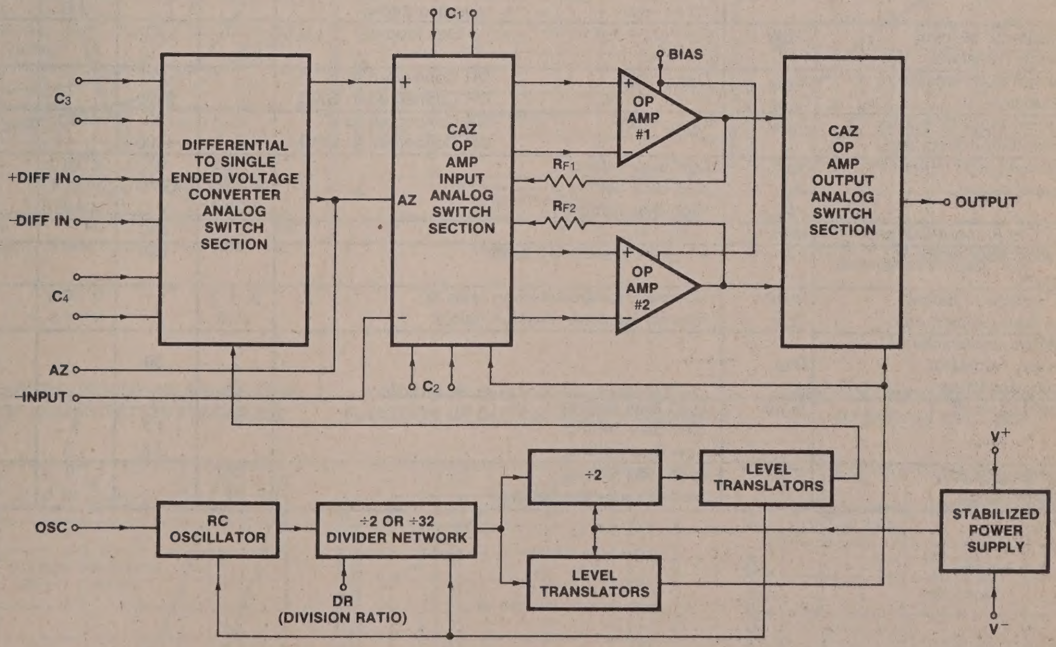
Note 1: Due to the SCR structure inherent in all CMOS devices, exceeding these limits may cause destructive latchup. For this reason, it is recommended that no inputs from sources operating on a separate power supply be applied to the 7605/6 before its own power supply is established, and that when using multiple supplies, the supply for the 7605/6 should be turned on first.

Note 2: No restrictions are placed on the differential input voltages on either the +DIFF IN or −DIFF IN inputs so long as these voltages do not exceed the power supply voltages by more than 0.3V.

Note 3: The outputs may be shorted to ground (GND) or to either supply (V^+ or V^-). Temperatures and/or supply voltages must be limited to insure that the dissipation ratings are not exceeded.

Note 4: For operation above 25°C free-air temperature, derate 4mW/°C from 500 mW above 25°C.

BLOCK DIAGRAM

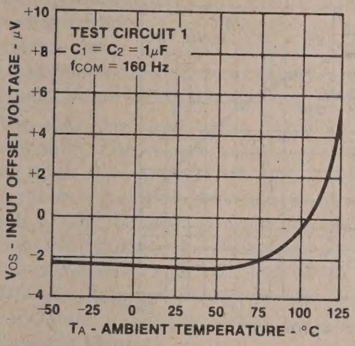

C₁
BIAS
C₃
+DIFF IN
−DIFF IN
C₄
DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER ANALOG SWITCH SECTION
+
AZ
−
CAZ OP AMP INPUT ANALOG SWITCH SECTION
OP AMP #1
OP AMP #2
R_F1
R_F2
CAZ OP AMP OUTPUT ANALOG SWITCH SECTION
OUTPUT
AZ
−INPUT
C₂
÷2
LEVEL TRANSLATORS
V+
OSC
RC OSCILLATOR
÷2 OR ÷32 DIVIDER NETWORK
DR (DIVISION RATIO)
LEVEL TRANSLATORS
STABILIZED POWER SUPPLY
V−

OPERATING CHARACTERISTICS

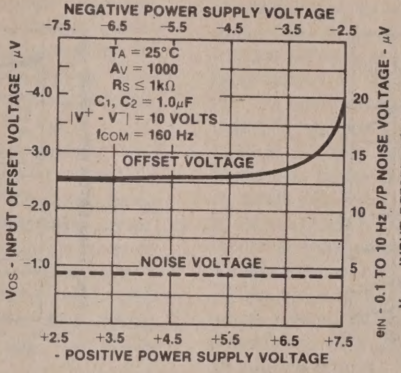
Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$, $f_{COM1} \cong 80Hz$),
$C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS		VALUE			UNIT
				MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 1k\Omega$	Low Bias Setting		±2		µV
			Med Bias Setting		±2	±5	µV
			High Bias Setting		±7		µV
		MIL version over temp.	Med Bias Setting			±20	µV
Average Input Offset Voltage Temperature Coefficient	$\Delta V_{OS}/\Delta T$	Low or Med Bias Settings	$-55°C > T_A > +25°C$		0.01	0.1	µV/°C
			$+25°C > T_A > +85°C$		0.01	0.1	µV/°C
			$+25°C > T_A > +125°C$		0.05	0.15	µV/°C
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$	Low or Med Bias Settings			0.5		µV/Year
Common Mode Input Range	CMVR			−5.3		+5.3	V
Common Mode Rejection Ratio	CMRR	$C_{OSC} = 0$, DR connected to V^+, $C_3 = C_4 = 1\mu F$			94		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 1\mu F$			100		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 10\mu F$			104		dB
Power Supply Rejection Ratio	PSRR				110		dB
-INPUT Bias Current	$-I_{BIAS}$	Any bias setting, $f_C = 160Hz$ (Includes charge injection currents)			0.15	1.5	nA
Equivalent Input Noise Voltage peak-to-peak	$\bar{e}_{np-p}$	Band Width 0.1 to 10Hz	Low Bias Mode		4.0		µV
			Med Bias Mode		4.0		µV
			High Bias Mode		5.0		µV
Equivalent Input Noise Voltage	$\bar{e}_n$	Band Width 0.1 to 1.0Hz	All Bias Modes		1.7		µV
Voltage Gain	A_V	$R_L = 100k\Omega$	Low Bias Setting	90	105		dB
			Med Bias Setting	90	105		dB
			High Bias Setting	80	100		dB
Maximum Output Voltage Swing	$\pm V_O$	$R_L = 1M\Omega$			±4.9		V
		$R_L = 100k\Omega$			±4.8		V
		$R_L = 10k\Omega$	Positive Swing	+4.4			V
			Negative Swing			−4.5	V
Band Width of Input Voltage Translator	GBW	$C_3 = C_4 = 1\mu F$	All Bias Modes		10		Hz
Nominal Commutation Frequency	f_{COM}	$C_{OSC} = 0pF$	DR Connected to V^+		160		Hz
			DR Connected to GND		2560		Hz
Nominal Input Converter Commutation Frequency	f_{COM1}	$C_{OSC} = 0pF$	DR Connected to V^+		80		Hz
			DR Connected to GND		1280		Hz
Bias Voltage to define Current Modes	V_{BA}	Low Bias Setting		$V^+-0.3$	V^+	$V^++0.3$	V
	V_{BM}	Med Bias Setting		$V^-+1.4$	GND	$V^+-1.4$	V
	V_{BL}	High Bias Setting		$V^--0.3$	V^-	$V^-+0.3$	V
Bias (Pin 8) Input Current	I_{BIAS}				±30		pA
Division Ratio Input Current	I_{DR}	$V^+ -8.0 \leq V_{DR} \leq V^+ +0.3$ volt			±30		pA
DR Voltage to define Oscillator division ratio	V_{DRH}	Internal oscillator division ratio 32		$V^+-0.3$		$V^++0.3$	V
	V_{DRL}	Internal oscillator division ratio 2		V^+-8		$V^+-1.4$	V
Effective Impedance of Voltage Translator Analog Switches	R_{AS}				30		kΩ
Supply Current	I_{SUPP}	High Bias Setting			7	15	mA
		Med Bias Setting			1.7	5	mA
		Low Bias Setting			0.6	1.5	mA
Operating Supply Voltage Range	V^+-V^-	High Bias Setting		5		10	V
		Med or Low Bias Setting		4		10	V

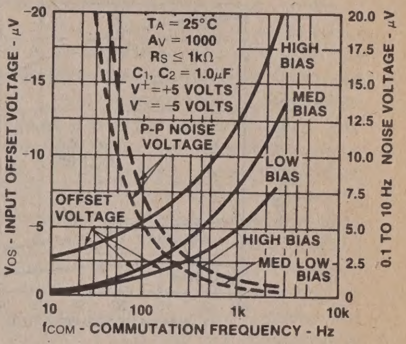
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



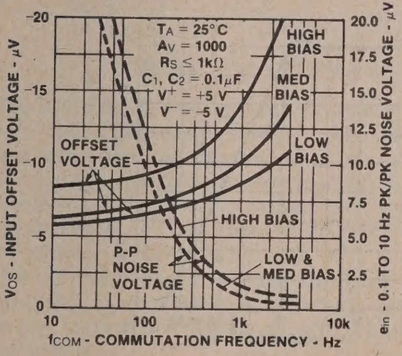
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



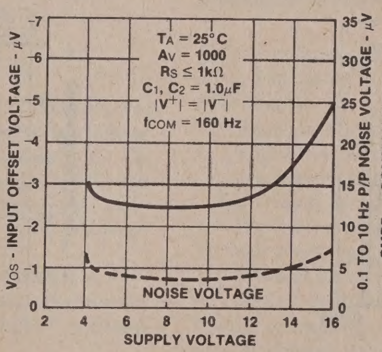
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C1, C2 = 1μF)



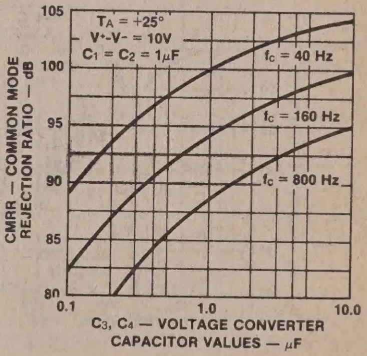
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C1, C2 = 0.1 μF)



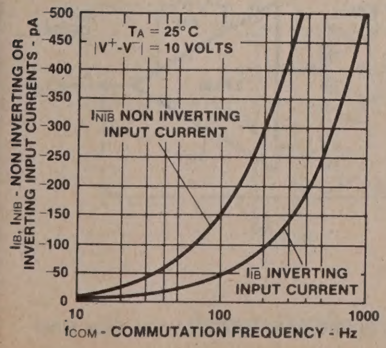
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V^+-V^-)



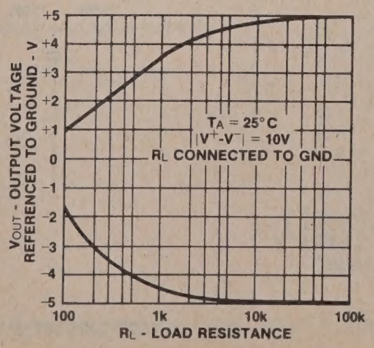
COMMON MODE REJECTION RATIO AS A FUNCTION OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER CAPACITORS



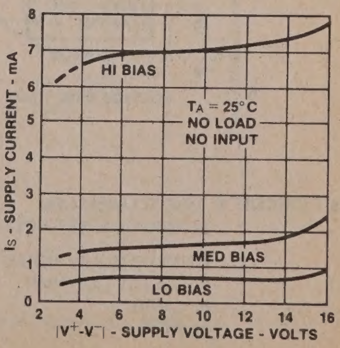
INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



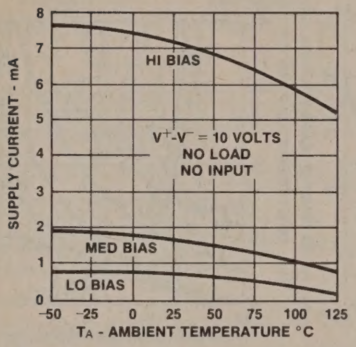
MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



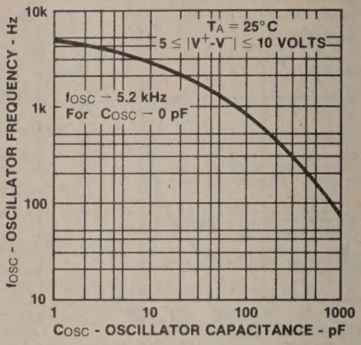
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



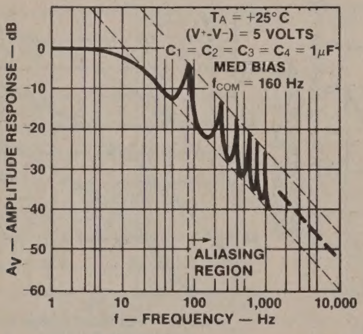
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



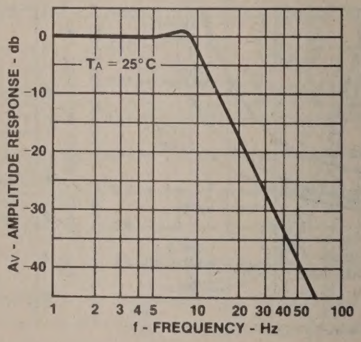
OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING

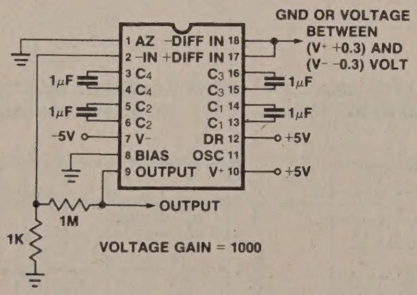


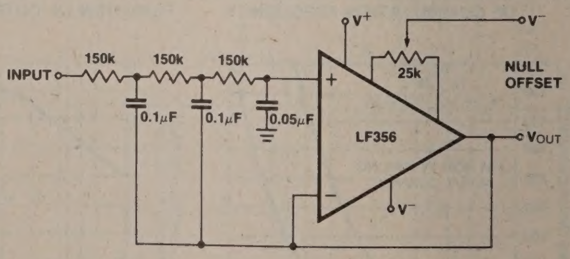
AMPLITUDE RESPONSE OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER



FREQUENCY RESPONSE OF THE 10 Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 2).




GND OR VOLTAGE BETWEEN (V+ +0.3) AND (V− −0.3) VOLT
1 AZ
−DIFF IN 18
2 −IN
+DIFF IN 17
3 C4
C3 16
4 C4
C3 15
5 C2
C1 14
6 C2
C1 13
7 V−
DR 12
8 BIAS
OSC 11
9 OUTPUT
V+ 10
1μF
1μF
1μF
1μF
−5V
+5V
+5V
OUTPUT
1M
1K
VOLTAGE GAIN = 1000


V+
V−
INPUT
150k
150k
150k
0.1μF
0.1μF
0.05μF
25k
NULL OFFSET
+
−
LF356
VOUT
V−

TEST CIRCUIT 1: USE TO MEASURE:
a) INPUT OFFSET VOLTAGE $\left(\frac{V_{OUT}}{1000}\right)$
b) INPUT EQUIV NOISE VOLTAGE
c) SUPPLY CURRENT
d) CMRR
e) PSRR

TEST CIRCUIT 2: DC to 10Hz (1Hz) Unity Gain Low Pass Filter

DETAILED DESCRIPTION

CAZ Instrumentation Amp Overview

The CAZ instrumentation amplifier operates on principles which are very different from those of the conventional three op amp designs, which must use ultra-precise trimmed resistor networks in order to achieve acceptable accuracy. An important advantage of the ICL7605/ICL7606 CAZ instrumentation amp is the provision for self-compensation for internal error voltages, whether they are derived from steady-state conditions, temperature, supply voltage fluctuations, or are variable over a long term.

The CAZ instrumentation amplifier is constructed with monolithic CMOS technology, and consists of three distinct sections, two analog and one digital. The two analog sections — a differential to single-ended voltage converter, and a CAZ op amp — have on-chip analog switches to steer the input signal. The analog switches are driven from a self-contained digital section which consists of an RC oscillator, a programmable divider, and associated voltage translators. A functional layout of the ICL7605/ICL7606 is shown in Figure 1.

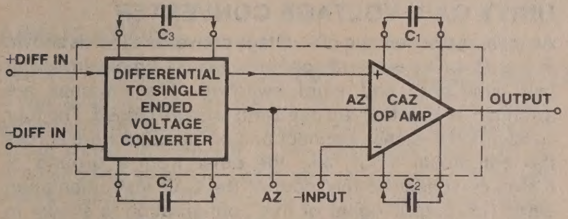


Figure 1: Simplified Block Diagram

The ICL7605/ICL7606 have approximately constant equivalent input noise voltage, CMRR, PSRR, input offset voltage and drift values independent of the gain configuration. By comparison, hybrid-type modules which use the traditional three op amp configuration have relatively poor performance at low gain (1 to 100) with improved performance above a gain of 100.

The only major limitation of the ICL7605/ICL7606 is its low-frequency operation (10 to 20 Hz maximum). However in many applications speed is not the most important parameter.

CAZ Op Amp Section

Operation of the CAZ amp section of the ICL7605/ICL7606 instrumentation amplifier is best illustrated by referring to Figure 2. The basic amplifier configuration, represented by the large triangles, has one more input than does a regular op amp — the AZ, or auto-zero terminal. The voltage on the AZ input is that level at which each of the internal op amps will be auto-zeroed. In Mode A, op amp #2 is connected in a unity gain mode through on-chip analog switches. It charges external capacitor C_2 to a voltage equal to the DC input offset voltage of the amplifier plus the instantaneous low-frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps to the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which is charged to a voltage equal to the offset and noise voltage of op amp #2) connected in series to its non-inverting (+) input in such a manner as to null out the input offset and noise voltages of the amplifier. While one of the on-chip op amps is processing the input signal, the second op amp is in an auto-zero mode, charging a capacitor to a voltage equal to its equivalent DC and low frequency error voltage. The on-chip amplifiers are connected and reconnected at a rate designated as the commutation frequency (f_{COM}), so that at all times one or the other of the on-chip op amps is processing the input signal, while the voltages on capacitors C_1 and C_2 are being updated to compensate for variables such as low frequency noise voltage and input offset voltage changes due to temperature, drift or supply voltages effects.

Compared to the standard bipolar or FET input op amps, the CAZ amp scheme demonstrates a number of important advantages:

* Effective input offset voltages can be reduced from 1000 to 10,000 times without trimming.

* Long-term offset voltage drift phenomena can be compensated and dramatically reduced.

* Thermal effects can be compensated for over a wide operating temperature range. Reductions can be as much as 100 times or better.

* Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ amp structure. The digital section is easily fabricated, and

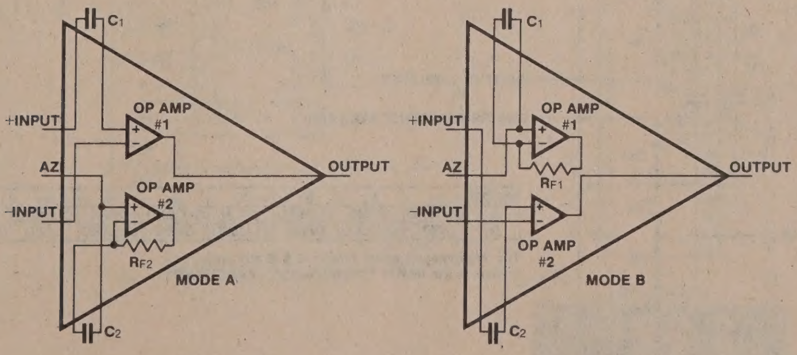


Figure 2: Diagrammatic representation of the 2 half cycles of operation of the CAZ OP AMP.

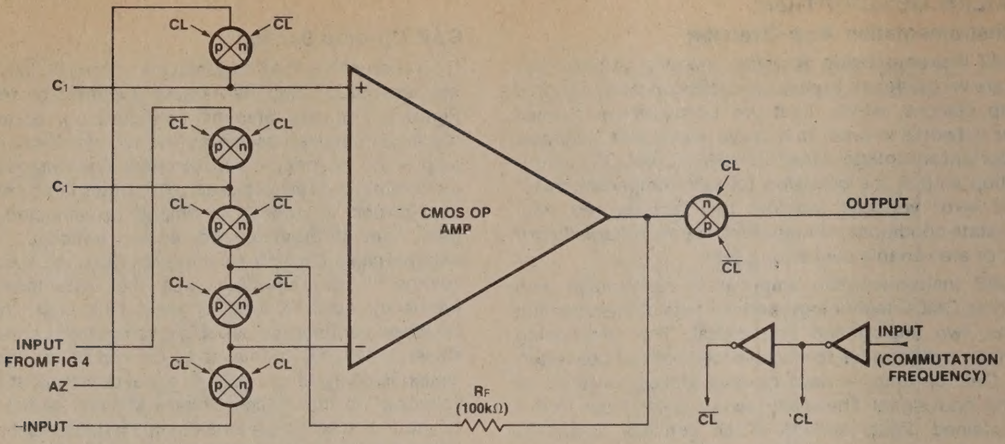

CL
$\overline{CL}$
C₁
$\overline{CL}$
CL
C₁
CL
$\overline{CL}$
CL
$\overline{CL}$
INPUT
FROM FIG 4
AZ
$\overline{CL}$
CL
–INPUT
+
–
CMOS OP
AMP
R_F
(100kΩ)
CL
n
p
$\overline{CL}$
OUTPUT
INPUT
(COMMUTATION
FREQUENCY)
$\overline{CL}$
CL

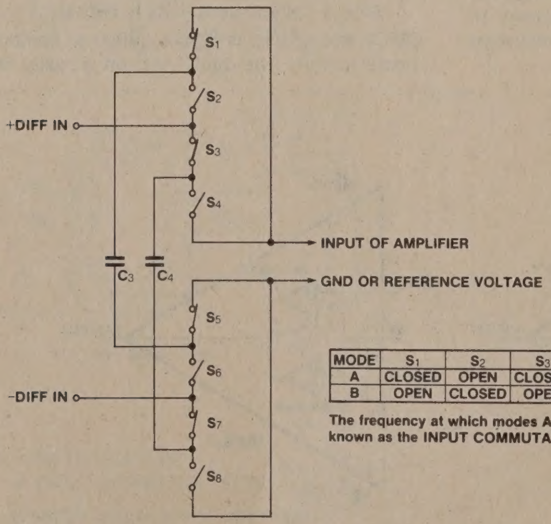
Figure 3: Schematic of analog switches connecting each internal OP AMP to its inputs and output.

the transmission gates (analog switches) which connect the on-chip op amps can be constructed for minimum charge injection and the widest operating voltage range. The analog section, which includes the on-chip op amps, contributes performance figures which are similar to bipolar or FET input designs. CMOS structure provides the CAZ amp with open-loop gains of greater than 100 dB, typical input offset voltages of ±5 mV, and ultra-low leakage currents, typically 1 pA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 3. Here, one op amp and its associated analog switches are required to connect each on-chip op amp, so that at any time three switches are open and three switches are closed. Each analog switch consists of a P-channel transistor in parallel with an N-channel transistor.

DIFFERENTIAL-TO-SINGLE-ENDED UNITY GAIN VOLTAGE CONVERTER

An idealized schematic of a voltage converter block is shown in Figure 4. The mode of operation is quite simple, involving two capacitors and eight switches. The switches are arranged so that four are open and four are closed. The four conducting switches connect one of the capacitors across the differential input, and the other from a ground or reference voltage to the input of the CAZ instrumentation amp. The output signal of this configuration is shown in Figure 5, where the voltage steps equal the differential voltage (V_A-V_B) at commutation times a, b, c, etc. The output waveform thus represents all information contained in the input signal from DC up to the commutation frequency, commutation and noise voltages are added. Sampling theory states that to preserve the integrity of the information to be processed, at least two samples must be taken within a period (1/f) of the highest frequency of the signal being


S₁
S₂
+DIFF IN
S₃
S₄
INPUT OF AMPLIFIER
C₃
C₄
GND OR REFERENCE VOLTAGE
S₅
S₆
–DIFF IN
S₇
S₈

MODE	S₁	S₂	S₃	S₄	S₅	S₆	S₇	S₈
A	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN
B	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED

The frequency at which modes A & B are cycled is known as the INPUT COMMUTATION FREQUENCY

Figure 4: Schematic of the differential to single ended voltage converter

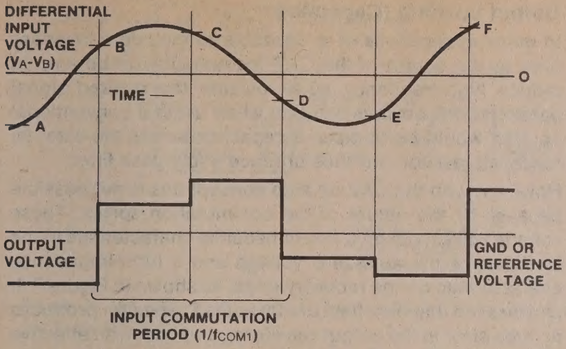

DIFFERENTIAL INPUT VOLTAGE (V_A-V_B)
A
B
C
D
E
F
O
TIME
OUTPUT VOLTAGE
GND OR REFERENCE VOLTAGE
INPUT COMMUTATION PERIOD ($1/f_{COM1}$)

Figure 5: Input to Output Voltage waveforms from the differential to single ended voltage converter. For additional information, see frequency characteristics in Amplitude Response of the Input Differential to single ended voltage converter graph on page 5.

sampled. Consequently this scheme preserves information up to the commutation frequency. Above the commutation frequency, the input signal is transferred to a lower frequency. This phenomenon is known as aliasing. Although the output responds above the commutation frequency, the frequencies of the output responses have been aliased down to frequencies below the commutation frequency.

The voltage converter is fabricated with CMOS analog switches, which contain a parallel combination of P-channel and N-channel transistors. The switches have finite ON impedances of 30kΩ, plus parasitic capacitances to the substrate. Because of the charge injection effects which appear at both the switches and the output of the voltage converter, the values of capacitors C_0 and C_0 must be about 1μF to preserve signal translation accuracies to 0.01%. The 1μF capacitors, coupled with the 30kΩ equivalent impedance of the switches, produce a low-pass filter response from the voltage converter which is approximately 3 dB at 10 Hz.

APPLICATIONS

USING THE ICL7605/ICL7606 TO BUILD A DIGITAL READOUT TORQUE WRENCH

A typical application for the ICL7605/ICL7606 is in a strain gauge system, such as the digital readout torque wrench circuit shown in Figure 6. In this application, the CAZ instrumentation amplifier is used as a preamplifier, taking the differential voltage of the bridge and converting this voltage to a single-ended voltage reference to ground. The signal is then amplified by the CAZ instrumentation amplifier and applied to the input of a 3-1/2 digit dual-slope A/D converter chip for LCD panel meter display. The A/D converter device used in this instance is the Intersil ICL7106.

In the digital readout torque wrench circuit, the reference voltage for the ICL7106 is derived from the stimulus applied to the strain gauge, to utilize the ratiometric capabilities of the A/D. In order to set the full-scale reading, it is required that, given a certain strain gauge bridge with a defined pressure voltage sensitivity, a value of gain for the ICL7605/ICL7606 instrumentation CAZ amp be selected along with an appropriate value for the reference voltage. The gain should be set so that at full scale the output will swing about 0.5V. The reference voltage required is about one-half the maximum output swing, or approximately 0.25V.

In this type of system, only one adjustment is required. Either the amplifier gain or the reference voltage must be varied for full-scale adjustment. Total current consumption of all circuitry, less the current through the strain gauge bridge, is typically 2 mA. The accuracy is limited only by resistor ratios and the transducer.

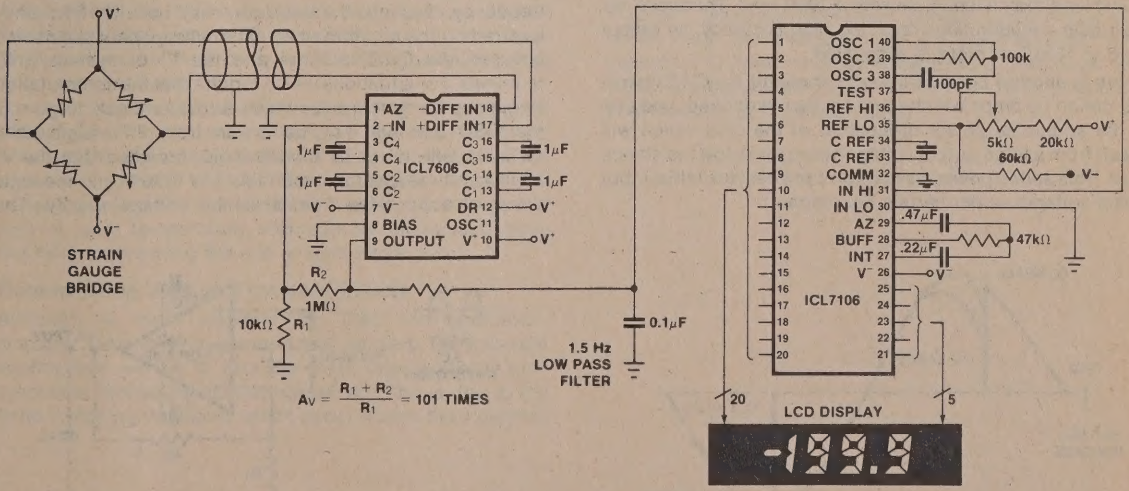

V+
V-
STRAIN GAUGE BRIDGE
1 AZ
2 -IN
3 C4
4 C4
5 C2
6 C2
7 V-
8 BIAS
9 OUTPUT
-DIFF IN 18
+DIFF IN 17
C3 16
C3 15
C1 14
C1 13
DR 12
OSC 11
V+ 10
ICL7606
1μF
1μF
1μF
1μF
V-
V+
V+
R2
1MΩ
10kΩ
R1
0.1μF
1.5 Hz LOW PASS FILTER
$A_V = \frac{R_1 + R_2}{R_1} = 101$ TIMES
OSC 1 40
OSC 2 39
OSC 3 38
TEST 37
REF HI 36
REF LO 35
C REF 34
C REF 33
COMM 32
IN HI 31
IN LO 30
AZ 29
BUFF 28
INT 27
V- 26
25
24
23
22
21
ICL7106
100k
100pF
5kΩ
20kΩ
60kΩ
V+
V-
.47μF
.22μF
47kΩ
V-
20
5
LCD DISPLAY
-199.9

Figure 6: 3-1/2 Digit Digital Readout Torque Wrench

SOME HELPFUL HINTS

Testing the ICL7605/ICL7606 CAZ Instrumentation Amplifier

Test Circuits #1 and #2 provide convenient means of measuring most of the important electrical parameters of the CAZ instrumentation amp. The output signal can be viewed on an oscilloscope after being fed through a low-pass filter. It is recommended that for most applications, a low-pass filter of about 1.0 to 1.5 Hz be used to reduce the peak-to-peak noise to about the same level as the input offset voltage.

The output low-pass filter must be of a high-input impedance type—(not simply a capacitor across the feedback resistor R_2) at about 100kΩ and 1.0μF so that the output dynamic loading on the CAZ instrumentation is about 100kΩ.

Bias Control

The on-chip op amps consume over 90% of the power required by the ICL7605/ICL7606 instrumentation op amp. For this reason, the internal op amps have externally-programmable bias levels. These levels are set by connecting the BIAS terminal to either V^+, GND, or V^- for LOW, MED or HIGH BIAS levels, respectively. The difference between each bias setting is about a factor of 3, allowing a 9:1 ratio of power supply versus bias setting. This current programmability provides the user with a choice of device power dissipation levels, slew rates (the higher the slew rate, the better the recovery from commutation spikes), and offset errors due to "IR" voltage drops and thermoelectric effects (the higher the power dissipation, the higher the input offset error). In most cases, the medium bias (MED BIAS) setting will be found to be the best choice.

Output Loading (Resistive)

With a 10kΩ load, the output voltage swing can vary across nearly the entire supply voltage range, and the device can be used with loads as low as 2kΩ.

However, with loads of less than 50kΩ, the on-chip op amps will begin to exhibit the characteristics of transconductance amplifiers, since their respective output impedances are nearly 50kΩ each. Thus the open-loop gain is 20 dB less with a 2kΩ load than it would be with a 20kΩ load. Therefore, for high gain configurations requiring high accuracy, an output load of 100kΩ or more is suggested.

There is another consideration in applying the CAZ instrumentation op amps which must not be overlooked, and that is the additional power dissipation of the chip which will result from a large output voltage swing into a low resistance load. This added power dissipation can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output of the CAZ instrumentation op amp to reduce high-frequency noise outside the desired signal passband. An obvious solution when using a conventional op amp would be to place a capacitor across the external feedback resistor and thus produce a low-pass filter.

However, with the CAZ op amp concept this is not possible because of the nature of the commutation spikes. These voltage spikes exhibit a low-impedance characteristic in the direction of the auto-zero voltage and a high-impedance characteristic on the recovery edge, as shown in Figure 7. It can be seen that the effect of a large load capacitor produces an area error in the output waveform, and hence an effective gain error. The output low-pass filter must be of a high-impedance type to avoid these area errors. For example, a 1.5 Hz filter will require a 100kΩ resistor and a 1.0μF capacitor, or a 1 MΩ resistor and an 0.1μF capacitor.

Oscillator and Digital Circuitry Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open circuit. If the full divider network is used, this will result in a nominal commutation frequency of approximately 160 Hz. The commutation frequency is that frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents the best compromise between input offset voltage and low frequency noise. Other commutation frequencies may provide optimization of some parameters, but always at the expense of others.

The oscillator has a very high output impedance, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the natural oscillator frequency is desired (5.2 kHz) the terminal remains open circuit. In other instances, it may be desirable to synchronize the oscillator with an external clock source, or to run it at another frequency. The ICL7605/ICL7606 CAZ amp provides two degrees of flexibility in this respect. First, the DR (division ratio) terminal allows a choice of either dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND) to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and the V^+ or system GND terminals. For situations which require that the commutation frequency be synchronized with a master clock, (Figure 8) the OSC terminal may be driven from TTL logic (with resistive pull-up) or by CMOS logic, provided that the V^+ supply (with respect to ground) is +5V (±10%) and the logic driver also operates from a similar voltage supply. The

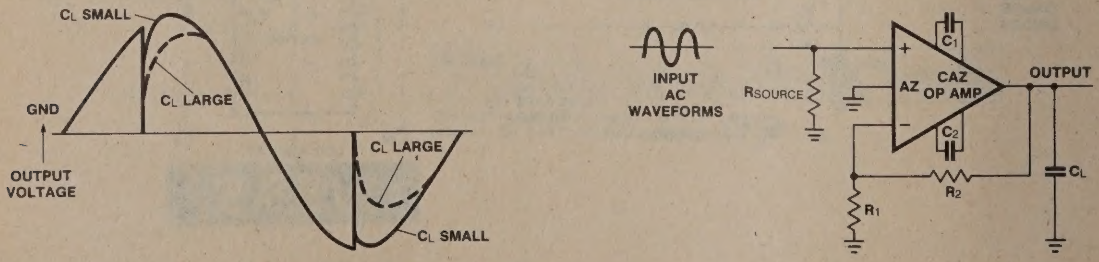


Figure 7: Effect of a load capacitor on output voltage waveforms.

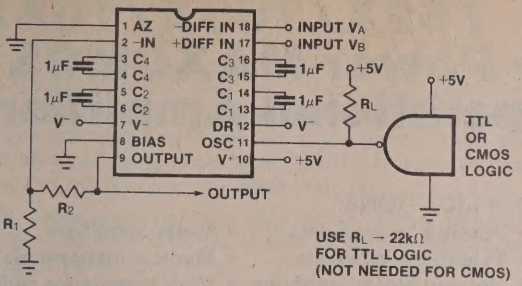


Figure 8: ICL7605 being clocked from external logic into the oscillator terminal.

reason for this requirement is that the logic section (including the oscillator) operates from an internal –5V supply, referenced to V^+ supply, which is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-sensitivity DC amplifiers are due to thermoelectric, Peltier, or thermocouple effects in electrical junctions consisting of various metals (alloys, silicon, etc.) Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can produce, it is necessary to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. In addition, the supply voltages and power dissipation should be kept to a minimum by use of the MED BIAS setting. Employ a high impedance load and keep well away from equipment which dissipates heat.

Component Selection

The four capacitors (C_1 thru C_4) should each be about 1.0μF. These are relatively large values for non-electrolytic capacitors, but since the voltages stored on them change significantly, problems of dielectric absorption, charge bleed-off and the like are as significant as they would be for integrating dual-slope A/D converter applications. Polypropylene are the best for C_3 and C_4, though Mylar may be adequate for C_1 and C_2.

Excellent results have been obtained for commercial temperature ranges using several of the less-expensive, smaller-size capacitors, since the absolute values of the capacitors are not critical. Even polarized electrolytic capacitors rated at 1.0μF and 50V have been used successfully at room temperature, although no recommendations are made concerning the use of such capacitors.

Commutation Voltage Transient Effects

Although in most respects the CAZ instrumentation amplifier resembles a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 10 Hz. The is due to the finite switching transients which occur at both the input and output terminals because of commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and including all of the higher harmonics of the commutation frequency. Assuming that the commutation frequency is higher than the highest in-band frequency, then the commutation transients can be filtered out with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage which is equal to the input offset voltages (about 5-10mV), usually occurring during the transition between the signal processing mode and the auto-zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must have values of at least 10,000 x 10 pF, or 0.1μF each.

The charge that is injected into the input of each op amp when being switched into the signal processing mode produces a rapidly-decaying voltage spike at the input, plus an equivalent DC input bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically 1.0 pA at an ambient temperature of 25°C.

The output waveform in Test Circuit #1 (with no input signal) is shown in Figure 9. Note that the equivalent noise voltage is amplified 1000 times, and that due to the slew rate of the on-chip op amps, the input transients of approximately 7 mV are not amplified by 1000.

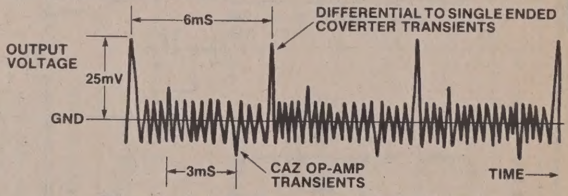


Figure 9: Output waveform from Test Circuit 1.

Layout Considerations

Care should be exercised in positioning components on the PC board, particularly the capacitors C_1, C_2, C_3 and C_4, all of which must be shielded from the OSC terminal. Also, parasitic PC board leakage capacitances associated with these four capacitors should be kept as low as possible to minimize charge injection effects.

ICL761X/ 762X/763X/764X Low Power MAXCMOS™ Operational Amplifiers

FEATURES

- **Wide operating voltage range ±0.5V to ±8V**
- **Single Ni-cad battery operation**
- **High input impedance — $10^{12}\Omega$**
- **Programmable power consumption — as low as 10μW**
- **Input current lower than BIFETs — typ 1pA**
- **Available as singles, duals, triples, and quads**
- **Output voltage swing ranges to within millivolts of V^- to V^+**
- **Low power replacement for many standard op amps**
- **Compensated and uncompensated versions**

APPLICATIONS

- **Portable instruments**
- **Telephone headsets**
- **Hearing aid/microphone amplifiers**
- **Meter amplifiers**
- **Medical instruments**
- **High impedance buffers**

A number of special options are available. They include:

- Single, dual, triple, and quad configurations
- Internally compensated and uncompensated versions
- Inputs protected to ±200V (ICL7613/15)
- Input common mode voltage range greater than supply rails (ICL7612)

Note: See page 2 for table of options.

SCHEMATIC

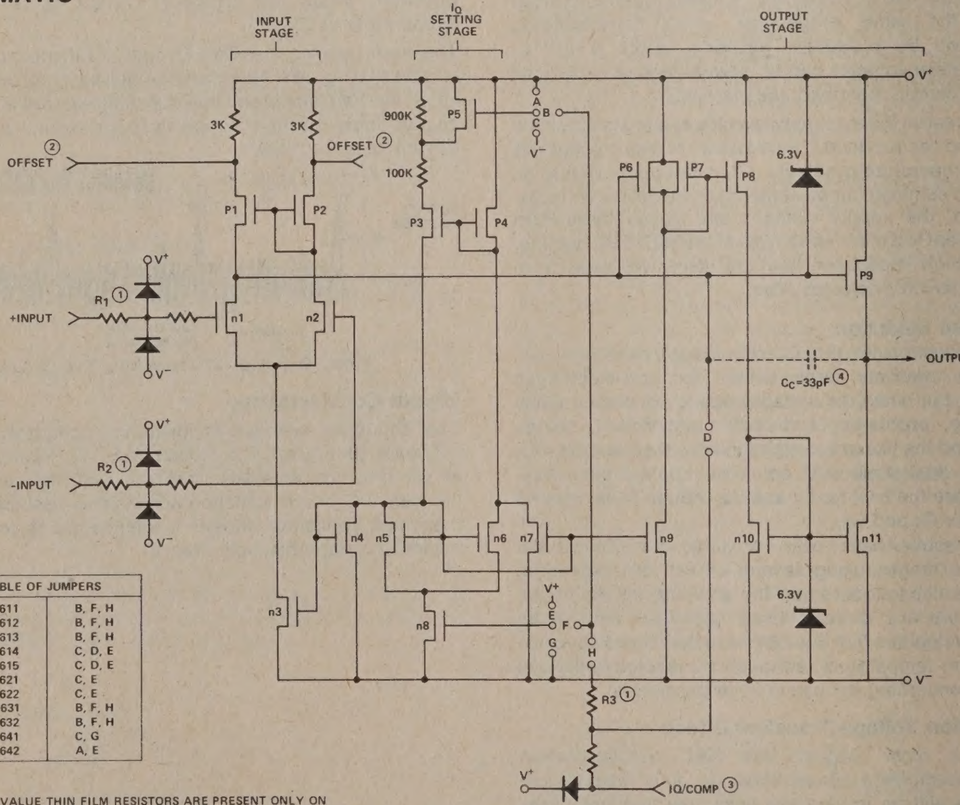

INPUT STAGE
I_Q SETTING STAGE
OUTPUT STAGE
V+
3K
3K
OFFSET ②
OFFSET ②
900K
100K
P5
A
B
C
V−
P1
P2
P3
P4
P6
P7
P8
6.3V
P9
V+
R1 ①
+INPUT
V−
n1
n2
OUTPUT
C_C=33pF ④
D
V+
R2 ①
-INPUT
V−
n4
n5
n6
n7
n9
n10
n11
n3
n8
V+
E
F
G
H
6.3V
V−
R3 ①
V+
IQ/COMP ③

TABLE OF JUMPERS	
ICL-7611	B, F, H
ICL-7612	B, F, H
ICL-7613	B, F, H
ICL-7614	C, D, E
ICL-7615	C, D, E
ICL-7621	C, E
ICL-7622	C, E
ICL-7631	B, F, H
ICL-7632	B, F, H
ICL-7641	C, G
ICL-7642	A, E

NOTES:

1. HIGH VALUE THIN FILM RESISTORS ARE PRESENT ONLY ON ICL-7613 AND 7615. FOR ALL OTHER DEVICES, THEY ARE REPLACED BY DIRECT CONNECTIONS.
2. OFFSET NULLING PINS ARE NOT AVAILABLE ON TRIPLE (ICL-763X) AND QUAD (ICL-764X) VERSIONS.
3. I_Q AND COMP TERMINALS ARE METAL MASK OPTIONS OF THE SAME BONDING PAD; ONLY ONE OF THESE FUNCTIONS IS AVAILABLE IN A GIVEN DEVICE.
4. FOR INTERNALLY COMPENSATED VERSIONS ONLY. THIS CAPACITOR IS ABSENT FOR ALL OTHER DEVICES.

GENERAL DESCRIPTION

The ICL761X/762X/763X/764X series is a family of monolithic CMOS op amps, fabricated using Intersils' proven MAXCMOS™ process. These amplifiers provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power drain are essential.

The basic amplifier will operate at supply voltages ranging from ±0.5 to ±8V, and may be operated from a single Ni-Cad battery.

A unique quiescent current programming pin allows setting of standby current to 1 mA, 100 μA, or 10 μA, with no external components. This results in power drain as low as 10 μW. Output swings range to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1 pA) input current, input noise current of .01pA/√Hz, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

The inputs are internally protected and require no special handling procedures. Outputs are fully protected against shorts to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/μs, and unity gain bandwidth of 1 MHz at I_Q = 1 mA.

Because of the low power dissipation, operating temperatures and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

SELECTION GUIDE

BASIC TYPE

76XX

OFFSET NULL CAPABILITY
Y = YES
N = NO

I_Q SETTING
L = 10μA FIXED
M = 100μA FIXED
H = 1mA FIXED
P = PROGRAMMABLE

ORDERING INFORMATION[2]

ICL76XX M N O P

V_{OS} SELECTION
A = 2mV
B = 5mV
C = 10mV
D = 15mV
E = 20mV

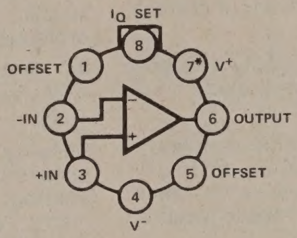
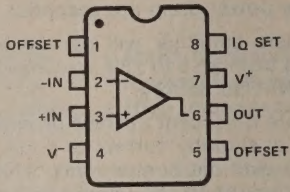
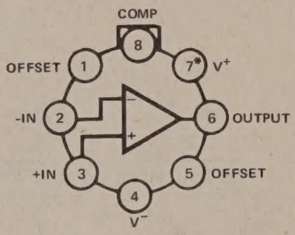
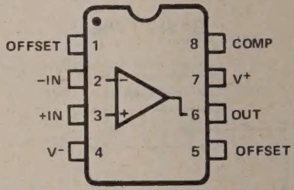
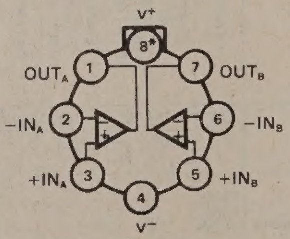
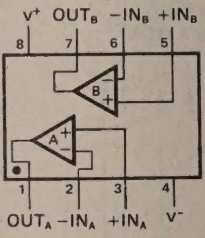
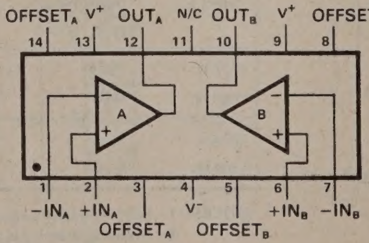
TEMP. RANGE
C = 0°C TO 70°C
M = -55°C TO +125°C

PACKAGE CODE
TY – TO-99, 8 PIN
PA – PLASTIC 8 PIN MINIDIP
PD – 14 PIN PLASTIC
PE – 16 PIN PLASTIC
JD – 14 PIN CERDIP
JE – 16 PIN CERDIP

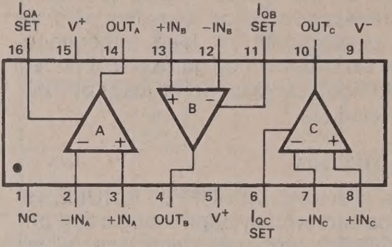
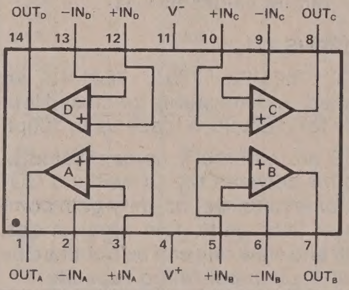
	BASIC TYPE					ORDER SUFFIX							
						TO-99		MINI DIP	PLASTIC DIP[1]	CERAMIC DIP[1]		DIE	
	COMPENSATED	EXTERNALLY COMPENSATED	COMPENSATED/ INPUT PROTECTED	EXTERNALLY COMPENSATED INPUT PROTECTED	EXTENDED CMVR	0°C to +70°C	55°C to +125°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	55°C to +125°C	0°C to +70°C	55°C to +125°C
SINGLE	7611 Y P	7614 Y M	7613 Y P	7615 Y M	7612 Y P	ACTY BCTY DCTY	AMTY BMTY —	ACPA BCPA DCPA				DC/D	
DUAL 1458 PINOUT	7621 N M					ACTY BCTY DCTY	AMTY BMTY —	ACPA BCPA DCPA				DC/D	
DUAL 747 PINOUT	7622 Y M								ACPD BCPD DCPD	ACJD BCJD DCJD	AMJD BMJD —	DC/D	
TRIPLE	7631 N P	[3] 7632 N P							BCPE CCPE ECPE	BCJE CCJE ECJE	BMJE CMJE —	EC/D	
QUAD High I_Q	7641 N H								BCPD CCPD ECPD	BCJD CCJD ECPD	BMJD CMJD —	EC/D	
QUAD Low I_Q	7642 N L								BCPD CCPD ECPD	BCJD CCJD ECJD	BCJD CCJD —	EC/D	

NOTES: 1. Duals and quads are available in 14 pin DIP packages, triples in 16 pin only.
2. Ordering code must consist of basic device and order suffix, e.g., ICL7611BCPA.
3. ICL7632 is not compensatable. Recommended for use in high gain circuits only.

PIN CONFIGURATIONS

DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7611XCPA ICL7611XCTY ICL7611XMTY ICL7612XCPA ICL7612XCTY ICL7612XMTY ICL7613XCPA ICL7613XCTY ICL7613XMTY	Internal compensation, plus offset null capability and external I$_Q$ control.	TO-99 (TOP VIEW) (outline dwg TO-99)  I$_Q$ SET 8 OFFSET 1 7* V$^+$ -IN 2 6 OUTPUT +IN 3 5 OFFSET 4 V$^-$ − + *Pin 7 connected to case. 8 PIN DIP (TOP VIEW) (outline dwg PA)  OFFSET 1 -IN 2 +IN 3 V$^-$ 4 8 I$_Q$ SET 7 V$^+$ 6 OUT 5 OFFSET − +
ICL7614XCPA ICL7614XCTY ICL7614XMTY ICL7615XCPA ICL7615XCTY ICL7615XMTY	Fixed I$_Q$ (100μA), external compensation, and offset null capability.	TO-99 (TOP VIEW) (outline dwg TO-99)  COMP 8 OFFSET 1 7* V$^+$ -IN 2 6 OUTPUT +IN 3 5 OFFSET 4 V$^-$ − + * Pin 7 connected to case. 8 PIN DIP (TOP VIEW) (outline dwg PA)  OFFSET 1 -IN 2 +IN 3 V- 4 8 COMP 7 V$^+$ 6 OUT 5 OFFSET − +
ICL7621XCPA ICL7621XCTY ICL7621XMTY	Dual op amps with internal compensation; I$_Q$ fixed at 100μA Pin compatible with Texas Inst. TL082 Motorola MC1458 Raytheon RC4558	TO-99 (TOP VIEW) (outline dwg TO-99)  V$^+$ 8* OUT$_A$ 1 7 OUT$_B$ −IN$_A$ 2 6 −IN$_B$ +IN$_A$ 3 5 +IN$_B$ 4 V$^-$ * Pin 8 connected to case. 8 PIN DIP (TOP VIEW) (outline dwg PA)  V$^+$ OUT$_B$ −IN$_B$ +IN$_B$ 8 7 6 5 B A 1 2 3 4 OUT$_A$ −IN$_A$ +IN$_A$ V$^-$
ICL7622XCPD	Dual op amps with internal compensation and offset null capability; I$_Q$ fixed at 100μA Pin compatible with Texas Inst. TL083 Fairchild μA747	14 PIN DIP (TOP VIEW) (outline dwgs JD, PD)  OFFSET$_A$ V$^+$ OUT$_A$ N/C OUT$_B$ V$^+$ OFFSET$_B$ 14 13 12 11 10 9 8 A B 1 2 3 4 5 6 7 −IN$_A$ +IN$_A$ V$^-$ +IN$_B$ −IN$_B$ OFFSET$_A$ OFFSET$_B$ **Note:** Pins 9 and 13 are internally connected.

PIN CONFIGURATIONS (Cont.)

DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7631XCPE ICL7632XCPE	Triple op amps with internal compensation (ICL7631) and no compensation (ICL7632). Adjustable I_Q Same pin configuration as ICL8023.	16 PIN DIP (TOP VIEW) (outline dwgs JE, PE)  I_{QA} SET 16 V^+ 15 OUT_A 14 $+IN_B$ 13 $-IN_B$ 12 I_{QB} SET 11 OUT_C 10 V^- 9 A B C 1 NC 2 $-IN_A$ 3 $+IN_A$ 4 OUT_B 5 V^+ 6 I_{QC} SET 7 $-IN_C$ 8 $+IN_C$ Note: Pins 5 and 15 are internally connected.
ICL7641XCPD ICL7642XCPD	Quad op amps with internal compensation. I_Q fixed at 1mA (ICL7641) I_Q fixed at 10μA (ICL7642) Pin compatible with Texas Instr. TL084 National LM324 Harris HA4741	14 PIN DIP (TOP VIEW) (outline dwg JD, PD)  OUT_D 14 $-IN_D$ 13 $+IN_D$ 12 V^- 11 $+IN_C$ 10 $-IN_C$ 9 OUT_C 8 D C A B 1 OUT_A 2 $-IN_A$ 3 $+IN_A$ 4 V^+ 5 $+IN_B$ 6 $-IN_B$ 7 OUT_B

GENERAL INFORMATION

STATIC PROTECTION

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

LATCHUP AVOIDANCE

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. (An exception to this rule concerns the inputs of the ICL7613 and ICL7615, which are protected to ±200V.) In general, the op amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2 mA to prevent latchup.

CHOOSING THE PROPER I_Q

Each device in the ICL76XX family has a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents of 10 μA, 100 μA or 1 mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12/13 and ICL7631/32 have an external I_Q control terminal, permitting user selection of each amplifiers' quiescent current. (The ICL7614/15, 7621/22, and 7641/42 have fixed I_Q settings — refer to selector guide for details.) To set the I_Q of programmable versions, connect the I_Q terminal as follows:

$I_Q = 10\mu A$ — I_Q pin to V^+

$I_Q = 100\mu A$ — I_Q pin to ground. If this is not possible, any voltage from V^+ -0.8 to V^- +0.8 can be used.

$I_Q = 1mA$ — I_Q pin to V^-

NOTE: The negative output current available is a function of the quiescent current setting. For maximum p-p output voltage swings into low impedance loads, I_Q of 1 mA should be selected.

OUTPUT STAGE AND LOAD DRIVING CONSIDERATIONS

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1M, 100K, and 10K, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB, which can supply higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

A special feature of the output stage is that it approximates a transconductance amplifier, and its gain is directly proportional to load impedance. Approximately the same open loop gains are obtained at each of the I_Q settings if corresponding loads of 10K, 100K, and 1M are used.

INPUT OFFSET NULLING

For those models provided with OFFSET NULLING pins, nulling may be achieved by connecting a 25K pot between the OFFSET terminals with the wiper connected to V^+. At quiescent currents of 1 mA and 100 μA, the nulling range provided is adequate for all V_{OS} selections; however with $I_Q = 10\mu A$, nulling may not be possible with higher values of V_{OS}.

FREQUENCY COMPENSATION

The ICL7611/12/13, 7621/22, 7631, 7641/42 are internally compensated, and are stable for closed loop gains as low as unity for capacitive loads up to 100pF.

The ICL7614 and 15 are externally compensated by connecting a capacitor between the COMP and OUT pins. A 39pF capacitor is required for unity gain compensation; for greater than unity gain applications, increased bandwidth and slew rate can be obtained by reducing the value of the compensating capacitor.

Since the g_m of the first stage is proportional to $\sqrt{I_Q}$, greatest compensation is required when $I_Q = 1$ mA. The ICL7632 is not compensated internally, nor can it be compensated externally. The device is stable when used as follows:

I_Q of 1 mA for gains ≥ 20
I_Q of 100 μA for gains ≥ 10
I_Q of 10 μA for gains ≥ 5

HIGH VOLTAGE INPUT PROTECTION

The ICL7613 and 7615 include on-chip thin film resistors and clamping diodes which allow voltages of up to ±200 to be applied to either input for an indefinite time without device failure. These devices will be useful where high common mode voltages, differential mode voltages, or high transients may be experienced. Such conditions may be found when interfacing separate systems with separate supplies. Unity gain stability is somewhat degraded with capacitive loads because of the high value of input resistors.

EXTENDED COMMON MODE INPUT RANGE

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1 volt for applications where $V_{SUPP} \geq \pm 1.5V$. For those applications where $V_{SUPP} \leq \pm 1.5V$, the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1 volt in the negative direction (e.g., for $V_{SUPP} = \pm 0.5V$, the input CMVR would be +0.1 volts to −0.6 volts).

OPERATION AT $V_{SUPP} = \pm 0.5$ VOLTS

Operation at $V_{SUPP} = \pm 0.5V$ is guaranteed at $I_Q = 10\mu A$ only. This applies to these devices with selectable I_Q, and those devices are set internally to $I_Q = 10\mu A$ (i.e., ICL7611, 7612, 7613, 7631, 7632, 7642).

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1$ MegΩ. Guaranteed input CMVR is ±0.1V minimum and typically +0.4V to -0.2 at $V_{SUPP} = \pm 0.5V$. For applications where greater common mode range is desirable, refer to description of ICL7612 above.

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

ABSOLUTE MAXIMUM RATINGS[1]

Total Supply Voltage V^+ to V^-	18V
Input Voltage	$V^+ + 0.3$ to $V^- - 0.3V$
Input Voltage ICL7613/15 Only	$V^+ + 200$ to $V^- - 200V$
Differential Input Voltage[2]	$\pm[(V^+ + 0.3) - (V^- - 0.3)]V$
Differential Input Voltage[2] ICL7613/15 Only	$\pm[(V^+ + 200) - (V^- - 200)]V$
Duration of Output Short Circuit[3]	Unlimited

Continuous Power Dissipation @ 25°C		Above 25°C derate as follows:
TO-99	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead Cerdip	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead Cerdip	500mW	4mW/°C

Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	
M Series	-55°C to +125°C
C Series	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
3. The outputs may be shorted to ground or to either supply, for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS V_{SUPP} = ±5.0V, T_A = 25°C, unless otherwise specified

			76XXA			76XXB			76XXD			
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	V_{OS}	R_S≤100KΩ, T_A=25°C			2			5			15	mV
		T_{MIN}≤T_A≤T_{MAX}			3			7			20	
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	R_S≤100KΩ		10			15			25		μV/°C
Input Offset Current	I_{OS}	T_A=25°C		0.5	30		0.5	30		0.5	30	pA
		ΔT_A=C[2]			300			300			300	
		ΔT_A=M[2]			800			800			800	
Input Bias Current	I_{BIAS}	T_A=25°C		1.0	50		1.0	50		1.0	50	pA
		ΔT_A=C			400			400			400	
		ΔT_A=M			4000			4000			4000	
Common Mode Voltage Range (Except ICL7612)	V_{CMR}	I_Q=10μA[1]	±4.4			±4.4			±4.4			V
		I_Q=100μA	±4.2			±4.2			±4.2			
		I_Q=1mA[1]	±3.7			±3.7			±3.7			
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}	I_Q=10μA	±5.3			±5.3			±5.3			V
		I_Q=100μA	+5.3 -5.1			+5.3 -5.1			+5.3 -5.1			
		I_Q=1mA	+5.3 -4.5			+5.3 -4.5			+5.3 -4.5			
Output Voltage Swing	V_{OUT}	R_L=100KΩ, T_A=25°C	±4.9			±4.9			±4.9			V
		ΔT_A=C, ΔT_A=M,	±4.8			±4.8			±4.8			
		I_Q=100μA	±4.6			±4.6			±4.6			
		R_L=10KΩ, T_A=25°C	±4.5			±4.5			±4.5			
		ΔT_A=C, ΔT_A=M,	±4.3			±4.3			±4.3			
		I_Q=1 mA	±4.0			±4.0			±4.0			
Large Signal Voltage Gain	A_{VOL}	V_O=±4.0V, R_L=1MΩ										dB
		I_Q=10μA[1], T_A=25°C	86	104		80	104		80	104		
		ΔT_A=C	80			75			75			
		ΔT_A=M	74			68			68			
		V_O=±4.0V, R_L=100kΩ										
		I_Q=100μA, T_A=25°C	86	102		80	102		80	102		
		ΔT_A=C	80			75			75			
		ΔT_A=M	74			68			68			
		V_O=±4.0V, R_L=10kΩ										
		I_Q=1mA[1], T_A=25°C	90	98		80	98		80	98		
		ΔT_A=C	85			75			75			
		ΔT_A=M	77			68			68			
Unity Gain Bandwidth	G_{BW}	I_Q=10μA[1]		0.044			0.044			0.044		MHz
		I_Q=100μA		0.48			0.48			0.48		
		I_Q=1mA[1]		1.4			1.4			1.4		
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	R_S≤100KΩ, I_Q=10μA[1]	76	96		70	96		70	96		dB
		R_S≤100KΩ, I_Q=100μA	76	91		70	91		70	91		
		R_S≤100KΩ, I_Q=1mA[1]	66	87		60	87		60	87		
Power Supply Rejection Ratio	PSRR	R_S≤100KΩ, I_Q=10μA[1]	80	94		80	94		80	94		dB
		R_S≤100KΩ, I_Q=100μA	80	86		80	86		80	86		
		R_S≤100KΩ, I_Q=1mA[1]	70	77		70	77		70	77		
Input Referred Noise Voltage	e_n	R_S=100Ω, f=1KHz		100			100			100		nV/√Hz
Input Referred Noise Current	i_n	R_S=100Ω, f=1KHz		0.01			0.01			0.01		pA/√Hz
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load										mA
		I_Q=10μA[1]		0.01	0.02		0.01	0.02		0.01	0.02	
		I_Q=100μA		0.1	0.25		0.1	0.25		0.1	0.25	
		I_Q=1mA[1]		1.0	2.5		1.0	2.5		1.0	2.5	
Channel Separation	V_{O1}/V_{O2}	A_{VOL}=100		120			120			120		dB
Slew Rate[3]	SR	A_{VOL}=1, C_L=100pF,										V/μs
		V_{IN} = 8V_{p-p}										
		I_Q=10μA[1], R_L=1MΩ		0.016			0.016			0.016		
		I_Q=100μA, R_L=100KΩ		0.16			0.16			0.16		
		I_Q=1mA[1], R_L=10KΩ		1.6			1.6			1.6		
Rise Time[3]	t_r	V_{IN}=50mV, C_L=100pF										μs
		I_Q=10μA[1], R_L=1MΩ		20			20			20		
		I_Q=100μA, R_L=100KΩ		2			2			2		
		I_Q=1mA[1], R_L=10KΩ		0.9			0.9			0.9		
Overshoot Factor[3]		V_{IN}=50mV, C_L=100pF										%
		I_Q=10μA[1], R_L=1MΩ		5			5			5		
		I_Q=100μA, R_L=100KΩ		10			10			10		
		I_Q=1mA[1], R_L=10KΩ		40			40			40		

Note: 1. ICL7611, 7612, 7613 only.

2. C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: -55°C to +125°C

3. ICL7614/15; 39pF from pin 6 to pin 8.

ELECTRICAL CHARACTERISTICS $V_{SUPP} = \pm0.5V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless otherwise specified. Specs apply to ICL7611/7612/7613 only.

PARAMETER	SYMBOL	CONDITIONS	76XXA			76XXB			UNITS
			MIN.	TYP.	MAX.	MIN	TYP.	MAX	
Input Offset Voltage	V_{OS}	$R_S \le 100K\Omega$, $T_A=25°C$ $T_{MIN} \le T_A \le T_{MAX}$			2 3			5 7	mV
Temperature Coefficient of Vos	$\Delta V_{OS}/\Delta T$	$R_S \le 100K\Omega$		10			15		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		0.5	30 300 800		0.5	30 300 800	pA
Input Bias Current	I_{BIAS}	$T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		1.0	50 500 4000		1.0	50 500 4000	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}		±0.1			±0.1			V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}		+0.1 to -0.6			+0.1 to -0.6			V
Output Voltage Swing	V_{OUT}	$R_L=1M\Omega$, $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		±0.49 ±0.48 ±0.41			±0.49 ±0.48 ±0.41		V
Large Signal Voltage Gain	A_{VOL}	$V_O=\pm0.1V$, $R_L=1M\Omega$ $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		90 80 70			90 80 70		dB
Unity Gain Bandwidth	G_{BW}			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \le 100K\Omega$		80			80		dB
Power Supply Rejection Ratio	PSRR	$R_S \le 100K\Omega$		80			80		dB
Input Referred Noise Voltage	e_n	$R_S=100\Omega$, f=1KHz		100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S=100\Omega$, f=1KHz		0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15	μA
Slew Rate	SR	$A_{VOL}=1$, $C_L=100pF$, $V_{IN}=0.2Vp\text{-}p$ $R_L=1M\Omega$		0.016			0.016		$V/\mu s$
Rise Time	t_r	$V_{IN}=50mV$, $C_L=100pF$ $R_L=1M\Omega$		20			20		μs
Overshoot Factor		$V_{IN}=50mV$, $C_L=100pF$ $R_L=1M\Omega$		5			5		%

Note: C = Commercial Temperature Range (0°C to +70°C); M = Military Temperature Range (-55°C to +125°C).

ELECTRICAL CHARACTERISTICS $V_{SUPP} = \pm 5.0V$, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXC MIN.	76XXC TYP.	76XXC MAX.	76XXE MIN.	76XXE TYP.	76XXE MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 100K\Omega$, $T_A = 25°C$			5			10			20	mV
		$T_{MIN} \le T_A \le T_{MAX}$			7			15			25	
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \le 100K\Omega$		15			20			30		µV/°C
Input Offset Current	I_{OS}	$T_A = 25°C$		0.5	30		0.5	30		0.5	30	pA
		$\Delta T_A = C$			300			300			300	
		$\Delta T_A = M$			800			800			800	
Input Bias Current	I_{BIAS}	$T_A = 25°C$		1.0	50		1.0	50		1.0	50	pA
		$\Delta T_A = C$			500			500			500	
		$\Delta T_A = M$			4000			4000			4000	
Common Mode Voltage Range	V_{CMR}	$I_Q = 10\mu A$[1]	±4.4			±4.4			±4.4			V
		$I_Q = 100\mu A$[3]	±4.2			±4.2			±4.2			
		$I_Q = 1mA$[2]	±3.7			±3.7			±3.7			
Output Voltage Swing	V_{OUT}	$R_L = 100K\Omega$, $T_A = 25°C$	±4.9			±4.9			±4.9			V
		$\Delta T_A = C$, $\Delta T_A = M$,	±4.8			±4.8			±4.8			
		$I_Q = 100\mu A$	±4.5			±4.5			±4.5			
		$R_L = 10K\Omega$, $T_A = 25°C$	±4.5			±4.5			±4.5			
		$\Delta T_A = C$, $\Delta T_A = M$,	±4.3			±4.3			±4.3			
		$I_Q = 1mA$	±4.0			±4.0			±4.0			
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm 4.0V$, $R_L = 1M\Omega$[1]										dB
		$I_Q = 10\mu A$[1], $T_A = 25°C$	86	104		80	104		80	104		
		$\Delta T_A = C$	80			75			75			
		$\Delta T_A = M$	74			68			68			
		$V_O = \pm 4.0V$, $R_L = 100k\Omega$[3]										
		$I_Q = 100\mu A$, $T_A = 25°C$	86	102		80	102		80	102		
		$\Delta T_A = C$	80			75			75			
		$\Delta T_A = M$	74			68			68			
		$V_O = \pm 4.0V$, $R_L = 10k\Omega$[2]										
		$I_Q = 1mA$[1], $T_A = 25°C$	86	98		80	98		80	98		
		$\Delta T_A = C$	80			75			75			
		$\Delta T_A = M$	74			68			68			
Unity Gain Bandwidth	G_{BW}	$I_Q = 10\mu A$[1]		0.044			0.044			0.044		MHz
		$I_Q = 100\mu A$[3]		0.48			0.48			0.48		
		$I_Q = 1mA$[2]		1.4			1.4			1.4		
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \le 100K\Omega$, $I_Q = 10\mu A$[1]	76	96		70	96		70	96		dB
		$R_S \le 100K\Omega$, $I_Q = 100\mu A$	76	91		70	91		70	91		
		$R_S \le 100K\Omega$, $I_Q = 1mA$[2]	66	87		60	87		60	87		
Power Supply Rejection Ratio	PSRR	$R_S \le 100K\Omega$, $I_Q = 10\mu A$[1]	80	94		80	94		80	94		dB
		$R_S \le 100K\Omega$, $I_Q = 100\mu A$	80	86		80	86		80	86		
		$R_S \le 100K\Omega$, $I_Q = 1mA$[2]	70	77		70	77		70	77		
Input Referred Noise Voltage	e_n	$R_S = 100\Omega$, $f = 1KHz$		100			100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S = 100\Omega$, $f = 1KHz$		0.01			0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load										mA
		$I_Q = 10\mu A$[1]		0.01	0.022		0.01	0.022		0.01	0.022	
		$I_Q = 100\mu A$		0.1	0.25		0.1	0.25		0.1	0.25	
		$I_Q = 1mA$[2]		1.0	2.5		1.0	2.5		1.0	2.5	
Channel Separation	V_{O1}/V_{O2}	$A_{VOL} = 100$		120			120			120		dB
Slew Rate[4]	SR	$A_{VOL} = 1$, $C_L = 100pF$, $V_{IN} = 8V_{p-p}$										V/µs
		$I_Q = 10\mu A$[1], $R_L = 1M\Omega$		0.016			0.016			0.016		
		$I_Q = 100\mu A$, $R_L = 100K\Omega$		0.16			0.16			0.16		
		$I_Q = 1mA$[1], $R_L = 10K\Omega$[2]		1.6			1.6			1.6		
Rise Time[4]	t_r	$V_{IN} = 50mV$, $C_L = 100pF$										µs
		$I_Q = 10\mu A$[1], $R_L = 1M\Omega$		20			20			20		
		$I_Q = 100\mu A$, $R_L = 100K\Omega$		2			2			2		
		$I_Q = 1mA$[2], $R_L = 10K\Omega$		0.9			0.9			0.9		
Overshoot Factor[4]		$V_{IN} = 50mV$, $C_L = 100pF$										%
		$I_Q = 10\mu A$[1], $R_L = 1M\Omega$		5			5			5		
		$I_Q = 100\mu A$, $R_L = 100K\Omega$		10			10			10		
		$I_Q = 1mA$[2], $R_L = 10K\Omega$		40			40			40		

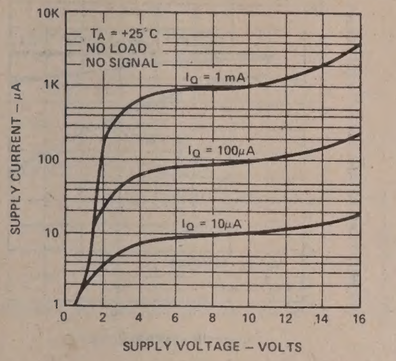
Note: 1. Does not apply to 7641.
2. Does not apply to 7642.
C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: -55°C to +125°C
3. ICL7631/32 only.
4. Does not apply to 7632.

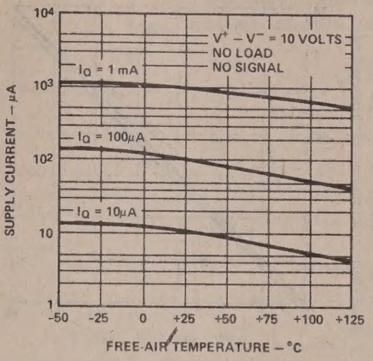
ELECTRICAL CHARACTERISTICS $V_{SUPP} = \pm 0.5V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless otherwise specified. Specs apply to ICL7631/7632/7642 only.

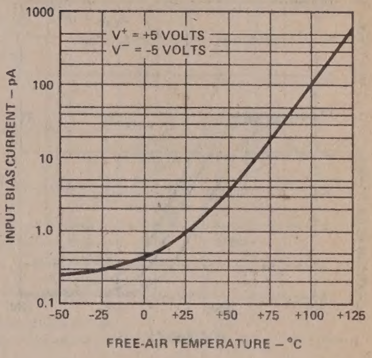
PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXC MIN	76XXC TYP.	76XXC MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 100K\Omega$, $T_A=25°C$ $T_{MIN} \le T_A \le T_{MAX}$			5 7			10 12	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \le 100K\Omega$		15			20		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		0.5	30 300 800		0.5	30 300 800	pA
Input Bias Current	I_{BIAS}	$T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		1.0	50 500 4000		1.0	50 500 4000	pA
Common Mode Voltage Range	V_{CMR}		±0.1			±0.1			V
Output Voltage Swing	V_{OUT}	$R_L=1M\Omega$, $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		±0.49 ±0.48 ±0.41			±0.49 ±0.48 ±0.41		V
Large Signal Voltage Gain	A_{VOL}	$V_O=\pm 0.1V$, $R_L=1M\Omega$ $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		90 80 70			90 80 70		dB
Unity Gain Bandwidth	G_{BW}			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \le 100K\Omega$		80			80		dB
Power Supply Rejection Ratio	PSRR			80			80		dB
Input Referred Noise Voltage	e_n	$R_S=100\Omega$, f=1KHz		100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S=100\Omega$, f=1KHz		0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15	μA
Channel Separation	V_{O1}/V_{O2}	$A_{VOL}=100$		120			120		dB
Slew Rate	SR	$A_{VOL}=1$, $C_L=100pF$, $V_{IN}=0.2Vp\text{-}p$ $R_L=1M\Omega$		0.016			0.016		$V/\mu s$
Rise Time	t_r	$V_{IN}=50mV$, $C_L=100pF$ $R_L=1M\Omega$		20			20		μs
Overshoot Factor		$V_{IN}=50mV$, $C_L=100pF$ $R_L=1M\Omega$		5			5		%

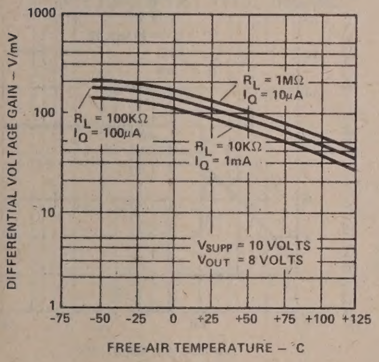
Note: C = Commercial Temperature Range (0°C to +70°C); M = Military Temperature Range (-55°C to +125°C).

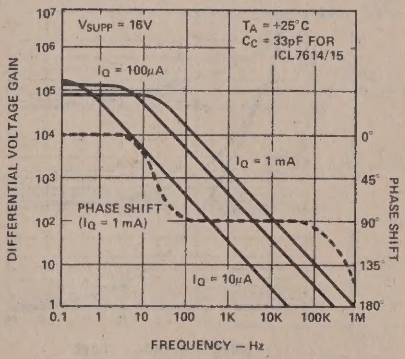
TYPICAL PERFORMANCE CHARACTERISTICS

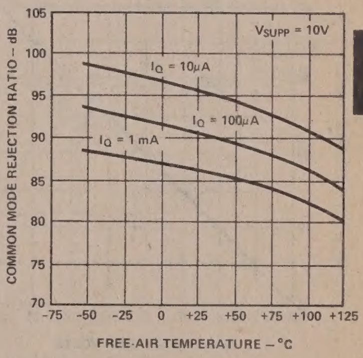

SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF SUPPLY VOLTAGE


SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF FREE-AIR TEMPERATURE

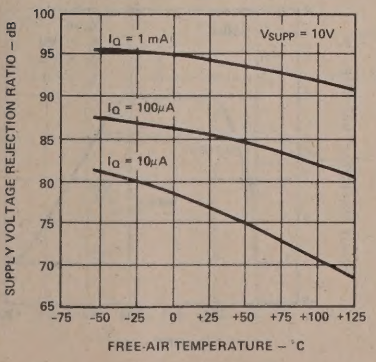

INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE

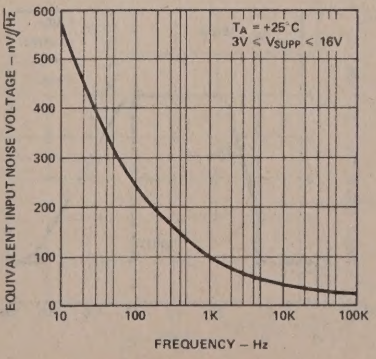

LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF FREE-AIR TEMPERATURE

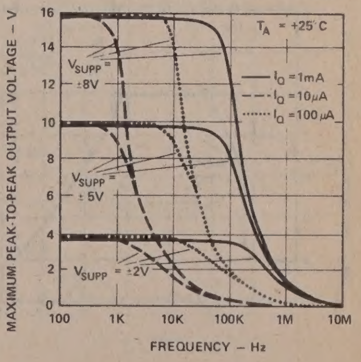

LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT AS A FUNCTION OF FREQUENCY


COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE

5

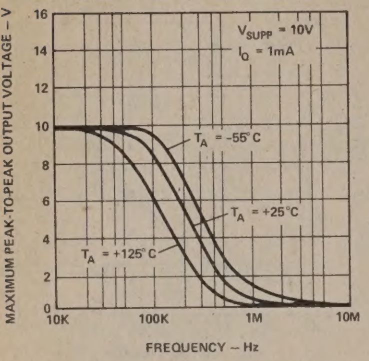

POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE


EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

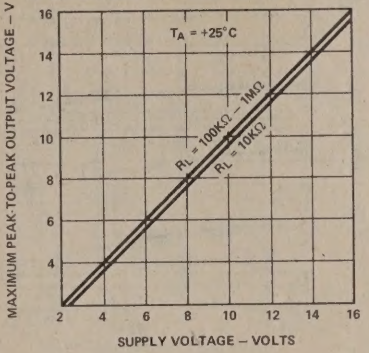

PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY

TYPICAL PERFORMANCE CHARACTERISTICS

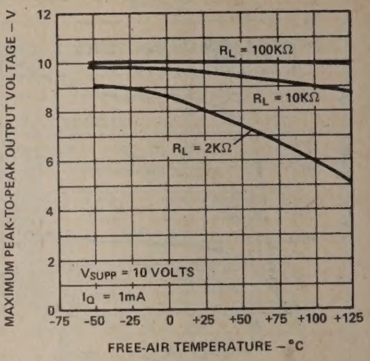
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



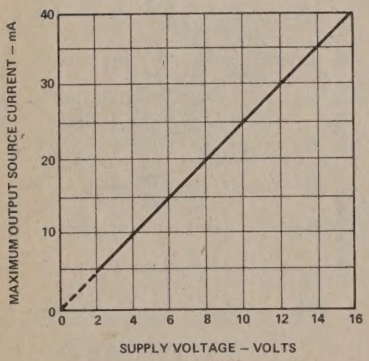
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



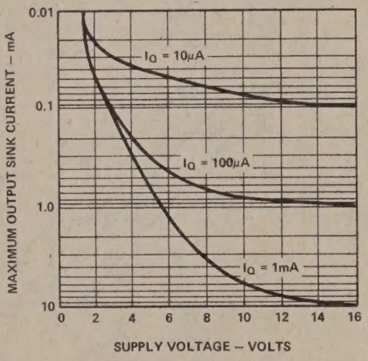
MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE



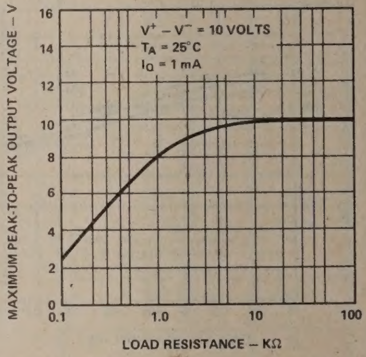
MAXIMUM OUTPUT/SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



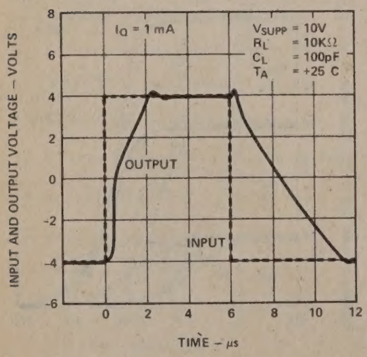
MAXIMUM OUTPUT SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



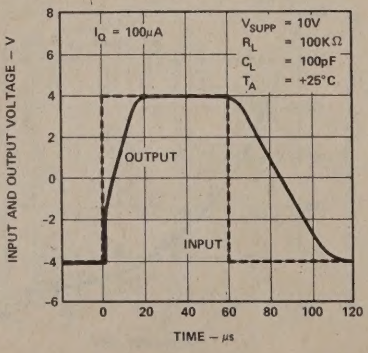
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



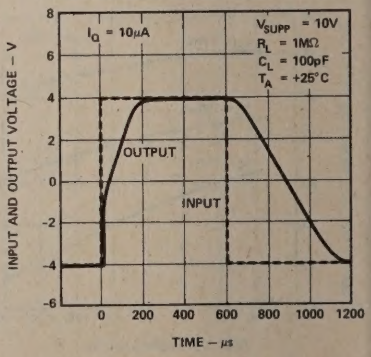
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



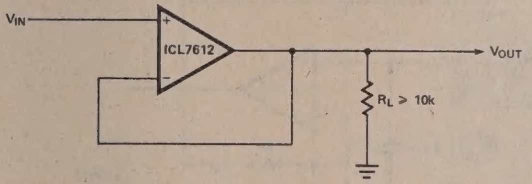
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



APPLICATIONS

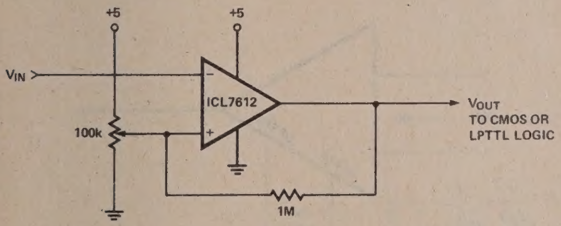
Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

SIMPLE FOLLOWER*


VIN
ICL7612
+
−
VOUT
RL ≥ 10k

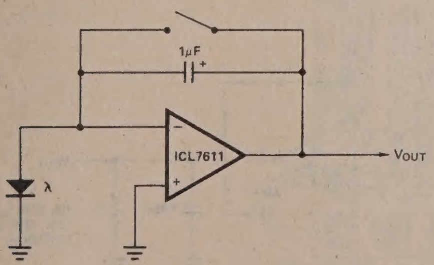
LEVEL DETECTOR*

*By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.


+5
+5
VIN
100k
ICL7612
−
+
VOUT
TO CMOS OR
LPTTL LOGIC
1M

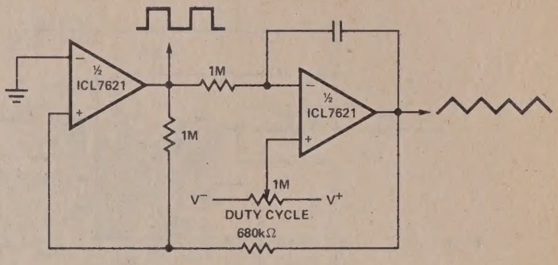
PHOTOCURRENT INTEGRATOR

Low leakage currents allow integration times up to several hours.


1μF
+
−
+
ICL7611
VOUT
λ

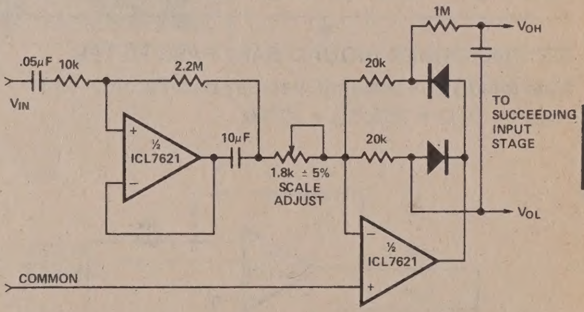
PRECISE TRIANGLE/SQUARE WAVE GENERATOR

Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.


½
ICL7621
−
+
1M
1M
½
ICL7621
−
+
1M
V−
V+
DUTY CYCLE
680kΩ

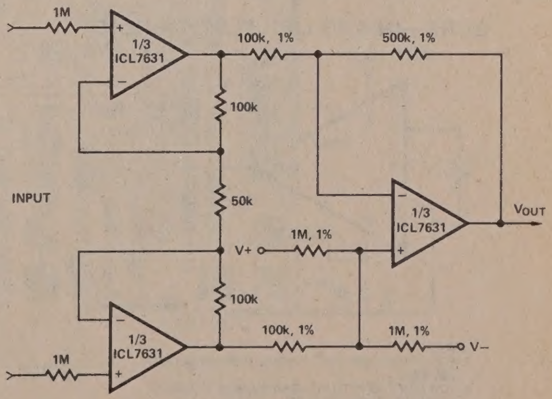
WAVEFORM GENERATOR

AVERAGING AC TO DC CONVERTER FOR A/D CONVERTERS SUCH AS ICL7106, 7107, 7109, 7116, 7117.


1M
VOH
.05μF
10k
2.2M
20k
VIN
TO
SUCCEEDING
INPUT
STAGE
+
½
ICL7621
−
10μF
20k
1.8k ± 5%
SCALE
ADJUST
VOL
½
ICL7621
−
+
COMMON

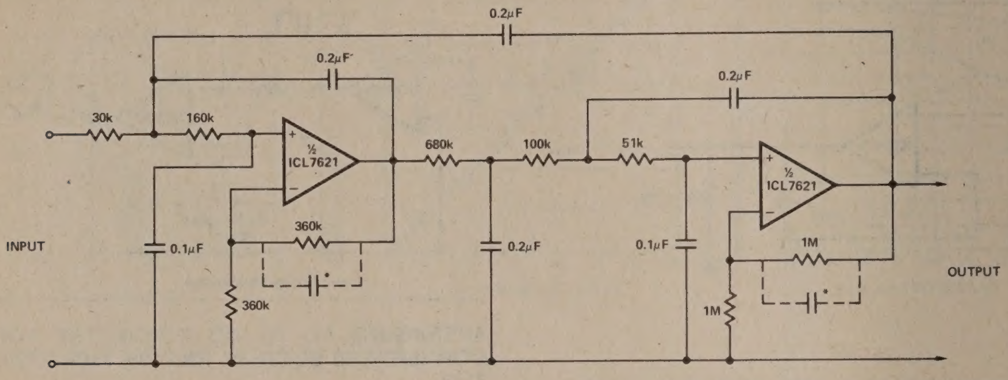
MEDICAL INSTRUMENT PREAMP

Note that $A_{VOL} = 25$; single Ni-cad battery operation. Input current (from sensors connected to patient) limited to $< 5\mu A$ under fault conditions.


1M
+
1/3
ICL7631
−
100k, 1%
500k, 1%
100k
INPUT
50k
V+
1M, 1%
−
1/3
ICL7631
+
VOUT
100k
−
1/3
ICL7631
+
100k, 1%
1M, 1%
V−
1M

FIFTH ORDER CHEBYSHEV MULTIPLE FEEDBACK LOW PASS FILTER

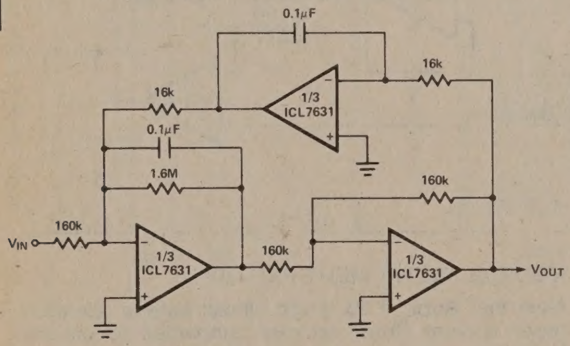
The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. $f_c = 10Hz$, $A_{VOL} = 4$, Passband ripple = 0.1 dB.


0.2µF
0.2µF
0.2µF
30k
160k
½ ICL7621
680k
100k
51k
½ ICL7621
INPUT
0.1µF
360k
360k
0.2µF
0.1µF
1M
1M
OUTPUT
*

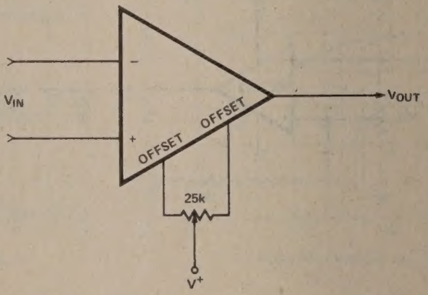
*Note that small capacitors (25-50pF) may be needed for stability in some cases.

SECOND ORDER BIQUAD BANDPASS FILTER

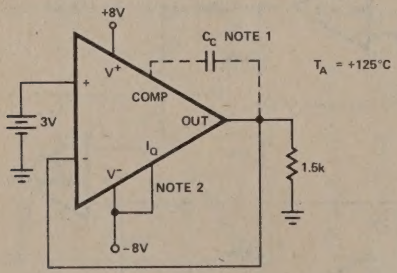
Note that I_Q on each amplifier may be different. $A_{VOL} = 10$, $Q = 100$, $f_o = 100Hz$.


0.1µF
16k
16k
1/3 ICL7631
0.1µF
1.6M
160k
160k
VIN
1/3 ICL7631
160k
1/3 ICL7631
VOUT

V_{OS} NULL CIRCUIT

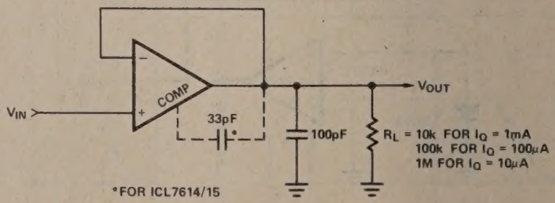

VIN
VOUT
OFFSET
OFFSET
25k
V+

BURN—IN AND LIFE TEST CIRCUIT


+8V
CC NOTE 1
TA = +125°C
V+
COMP
3V
OUT
IQ
1.5k
V−
NOTE 2
−8V

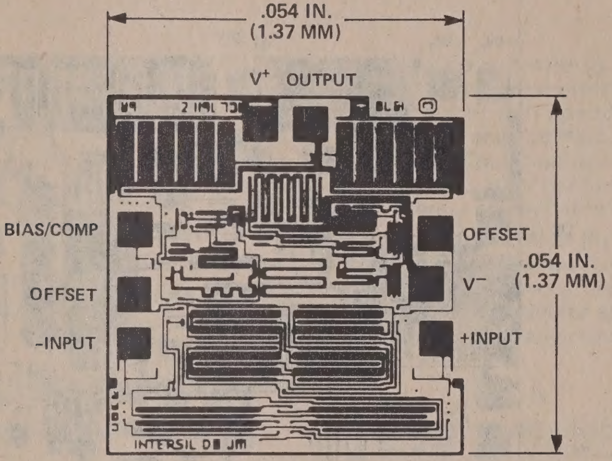
NOTES:
1. FOR DEVICES WITH EXTERNAL COMPENSATION, USE 33pF.
2. FOR DEVICES WITH PROGRAMMABLE STANDBY CURRENT, CONNECT I_Q PIN TO V^- (I_Q = 1mA MODE).

UNITY GAIN FREQUENCY COMPENSATION

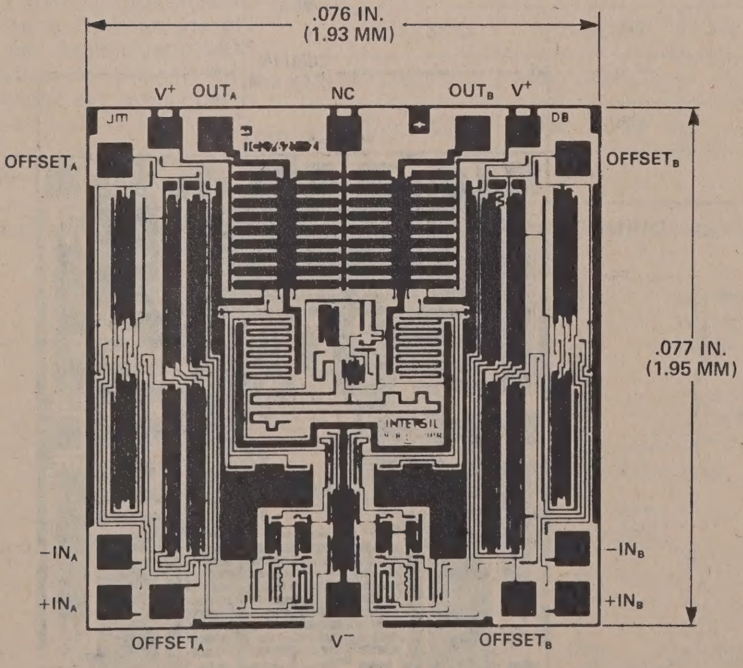

COMP
VIN
33pF
*
100pF
VOUT
RL = 10k FOR IQ = 1mA
100k FOR IQ = 100µA
1M FOR IQ = 10µA

*FOR ICL7614/15

CHIP TOPOGRAPHY

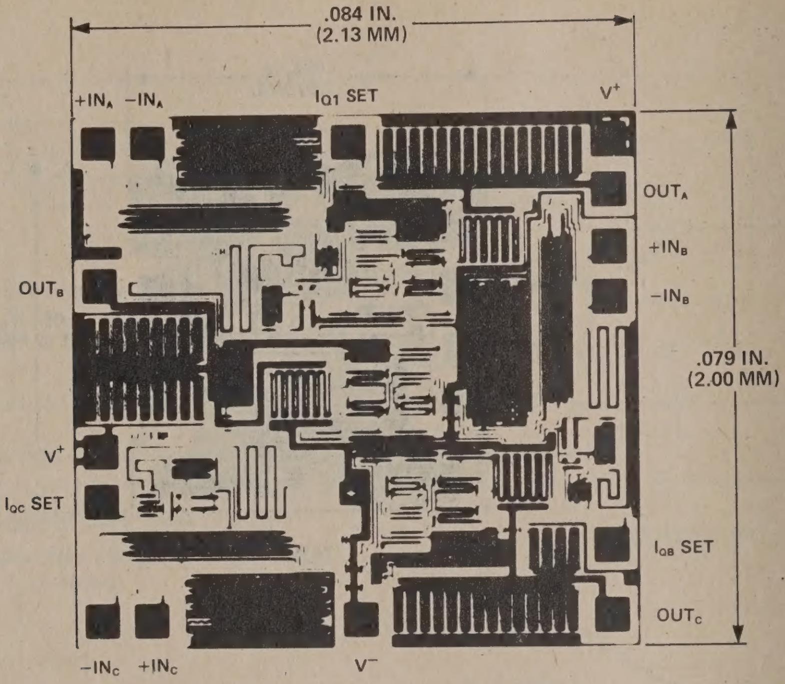

.054 IN.
(1.37 MM)
V$^+$
OUTPUT
BIAS/COMP
OFFSET
OFFSET
V$^-$
.054 IN.
(1.37 MM)
-INPUT
+INPUT
INTERSIL DB JM

761X

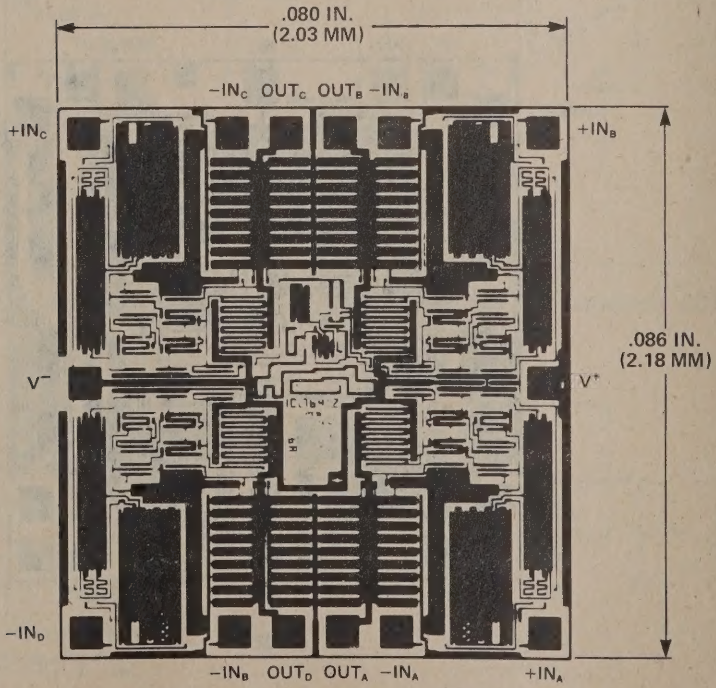

.076 IN.
(1.93 MM)
V$^+$
OUT$_A$
NC
OUT$_B$
V$^+$
JM
DB
OFFSET$_A$
OFFSET$_B$
INTERSIL
.077 IN.
(1.95 MM)
$-$IN$_A$
$-$IN$_B$
+IN$_A$
+IN$_B$
OFFSET$_A$
V$^-$
OFFSET$_B$

762X

CHIP TOPOGRAPHY (Cont.)


.084 IN.
(2.13 MM)
$+IN_A$
$-IN_A$
I_{Q1} SET
V^+
OUT_A
$+IN_B$
$-IN_B$
OUT_B
.079 IN.
(2.00 MM)
V^+
I_{QC} SET
I_{QB} SET
OUT_C
$-IN_C$
$+IN_C$
V^-

763X


.080 IN.
(2.03 MM)
$-IN_C$ OUT_C OUT_B $-IN_B$
$+IN_C$
$+IN_B$
.086 IN.
(2.18 MM)
V^-
V^+
$-IN_D$
$-IN_B$ OUT_D OUT_A $-IN_A$
$+IN_A$

764X

INTERSIL

PRELIMINARY
Specifications Subject To Change Without Notice

ICL7650
CHOPPER STABILIZED OPERATIONAL AMPLIFIER

FEATURES

- **Extremely low input offset voltage — 1 μV over temperature range**
- **Low long term and temperature drift of input offset voltage**
- **Low D.C. input bias current — 10pA**
- **Extremely high gain, CMRR and PSRR — min 120dB**
- **High slew rate — 2.5V/μS**
- **Wide bandwidth — 2MHz GBW product**
- **Internally compensated for unity gain operation**
- **Very low intermodulation effects (phase shift <10°)**
- **Clamp circuit to avoid overload recovery problems, allow comparator use**
- **Extremely low chopping spikes at input and output**

GENERAL DESCRIPTION

The ICL7650 chopper stabilized amplifier is a high performance device designed to be used in a wide variety of applications. This amplifier offers exceptionally low offset voltage and input bias parameters combined with excellent bandwidth and speed characteristics. Intersil's unique approach to chopper stabilized amplifier design, using Intersil's well established CMOS process, yields a versatile precision component which can replace more expensive hybrid or modular parts, while out-performing them and other monolithic devices.

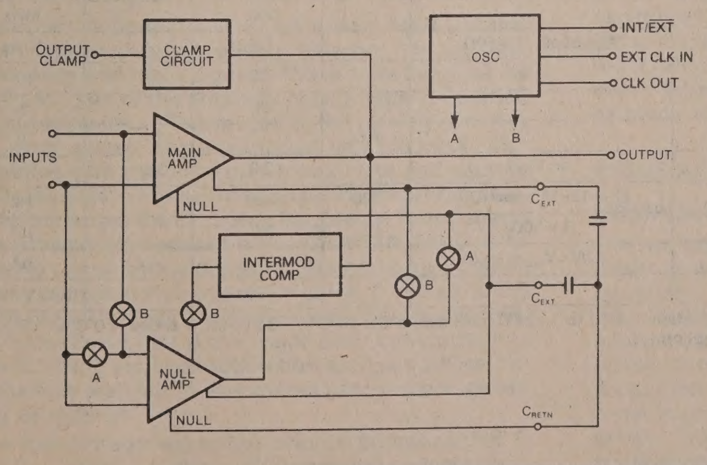
The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier that spends alternate clock phases nulling itself and the main amplifier. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs. These are the only external components necessary.

The clock oscillator and all of the other control circuitry is entirely self-contained. However, the 14-pin version includes a provision for the use of an external clock if required for a particular application. In addition, the ICL7650 is internally compensated for unity gain operation.

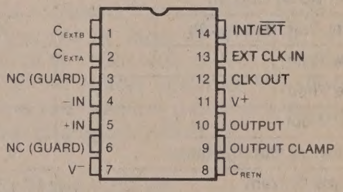
ORDERING INFORMATION

TEMP RANGE	PACKAGE	ORDER #
0°C to 70°C	14pin plastic	ICL7650CPD
−20°C to 85°C	14pin CERDIP	ICL7650IJD
0°C to 70°C	8pin TO-99	ICL7650CTY
−20°C to 85°C	8pin TO-99	ICL7650ITY
−55°C to 125°C	14pin CERDIP	
−55°C to 125°C	8pin TO-99	

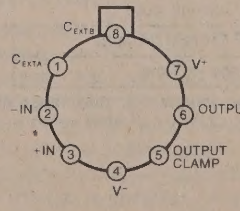
FIG. 1 BLOCK DIAGRAM


OUTPUT CLAMP
CLAMP CIRCUIT
OSC
INT/$\overline{EXT}$
EXT CLK IN
CLK OUT
A
B
INPUTS
MAIN AMP
OUTPUT
NULL
C_{EXT}
INTERMOD COMP
A
B
C_{EXT}
B
B
A
NULL AMP
NULL
C_{RETN}

PIN CONFIGURATION


C_{EXTB} 1
C_{EXTA} 2
NC (GUARD) 3
−IN 4
+IN 5
NC (GUARD) 6
V^- 7
14 INT/$\overline{EXT}$
13 EXT CLK IN
12 CLK OUT
11 V^+
10 OUTPUT
9 OUTPUT CLAMP
8 C_{RETN}

(outline dwg JD, PD)


C_{EXTB} 8
C_{EXTA} 1
7 V^+
−IN 2
6 OUTPUT
+IN 3
5 OUTPUT CLAMP
4 V^-

(outline dwg TO-99)

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	18 Volts
Input Voltage	V^+ +0.3 to V^- −0.3 Volts
except EXT CLOCK IN:	V^+ +0.3 to V^+ −6.0 Volts
Storage Temp. Range	−55°C to 150°C
Operating Temp. Range	−20°C to 85°C
(C series	0°C to +70°C)
Lead Temperature (Soldering, 10 sec)	300°C
Voltage on control pins	V^+ to V^-
Duration of Output short ckt	Indefinite
Current into any pin	10mA
—while operating	100 µA

Cont. Total Power Dissipn (T_A =25°C)	
CERDIP Package	500 mW
Plastic Package	375 mW
TO-99	250 mW

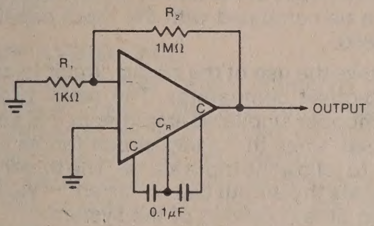
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS: Test Conditions: V^+ = +5V, V^- = −5V, T_A=25°C, Test Ckt (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS		UNIT
			MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OS}	T_A=25°C over operating temp. range (note 1)		±0.7 ±1.0	±5	µV
Average Temp. Coefficient of Input Offset Voltage	$\Delta V_{OS}/\Delta T$	over operating temp. range (note 1)		0.01		µV/°C
Input Bias Current (doubles every 10°C)	I_{BIAS}	T_A=25°C 0°C<T_A<+70°C −20°C<T_A<+85°C		1.5 35 100	10	pA
Input Offset Current	I_{OS}	T_A=25°C		0.5		pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ	1	5		V/µV
Output Voltage Swing	V_{OUT}	R_L = 10kΩ		±4.8		V
Common Mode Voltage Range	CMVR		−5.0	−5.2 to +2.6	+2.3	V
Common Mode Rejection Ratio	CMRR	CMV = −5V to +2.3V	120	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ± 7.5V	120	130		dB
Input Noise Voltage	e_n	R_S=100Ω 0 to 10Hz		2		µVp-p
Input Noise Current	i_n	f=10Hz		0.01		pA/√Hz
Unity Gain Bandwidth	GBW			2.0		MHz
Slew Rate	SR	C_L=50pF, R_L=50Ω		2.5		V/µs
Rise Time	t_r			0.2		µs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		6.0		16	V
Supply Current	I_{SUPP}	no load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	pins 12–14 open (DIP)	120	200		Hz
Clamp ON Current (note 2)		R_L=100K		70		µA
Clamp OFF Current (note 2)		−4.0V<V_{OUT}<+4.0V		1		pA
Offset Voltage vs Time				100		nV/√mnth

NOTE 1: Operating temperature range for M series parts is −55°C to +125°C, for I series is −20°C to +85°C, for C series is 0°C to +70°C.
NOTE 2: See OUTPUT CLAMP under detailed description.

TEST CIRCUIT



DETAILED DESCRIPTION

AMPLIFIER

The block diagram shows the major elements of the ICL7650. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset null capability. The main amplifier is connected full time from the input to the output, while the nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET back gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials, and the necessary nulling loop time constants. The nulling arrangement operates over the full common mode and power supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, and is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

The null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin (in the case of 14 pin devices) or the V^- pin (in the case of the 8 pin devices). This connection should be made directly to V^- by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry.

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differential inputs are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

CLOCK

The ICL7650 has an internal oscillator giving a chopping frequency of 200 Hz, available at the CLOCK OUT pin on the 14 pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{\text{EXT}}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT. CLOCK IN pin. At low frequencies the duty cycle of the external clock is not critical, since an internal divide-by-two provides the desired 50% switching duty cycle. However, since the capacitors are charged only when EXT CLK IN is HIGH, a 50–80% positive duty cycle is favored for frequencies above 500Hz to ensure that any transients have time to settle before the capacitors are turned OFF. The external clock should swing between V^+ and GROUND for power supplies up to ±6V, and between V^+ and $V^+ - 6V$ for higher supply voltages. Note that a signal of about 400Hz will be present at the EXT CLK IN pin with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a STROBE signal is connected to EXT CLK IN during the time that the unknown signal is applied to the amplifier, neither capacitor will be charged as long as STROBE is low. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10μV/sec, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

COMPONENT SELECTION

The two required capacitors, C_{EXTA} and C_{EXTB} have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1μF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion. A high quality film type capacitor such as mylar is preferred, although a ceramic or other lower grade capacitor may prove suitable in many applications.

PIN COMPATIBILITY

The basic pinout of the 8-pin device corresponds, where possible to that of the industry standard 8-pin devices, the LM741, LM101, etc. The null storing external capacitors are connected to pins 1 and 8, usually used for offset null, compensation capacitors, or not connected. The output clamp pin (5) is similarly used. In the case of the OP-05 and OP-07 devices, the replacement of the offset null pot, connected between pins 1 and 8 and V^+, by two capacitors from those pins to V^- will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to V^- is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, µA748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert to the ICL7650.

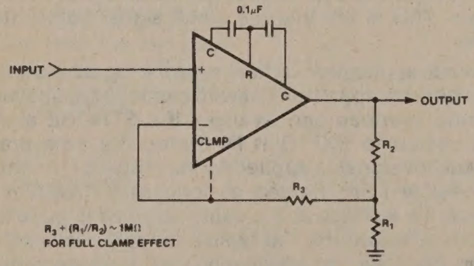
TYPICAL APPLICATIONS

Clearly the applications of the ICL7650 will mirror those of other op. amps. Thus, anywhere that the performance of a circuit can be significantly improved by a reduction of input offset voltage and bias current, the ICL7650 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figs. 2 and 3. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op. amps by the ICL7650 are the supply voltage (±8V max.) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Fig. 4, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650.

Fig. 5 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current ~ V_{IN}/R without disturbing other portions of the system.

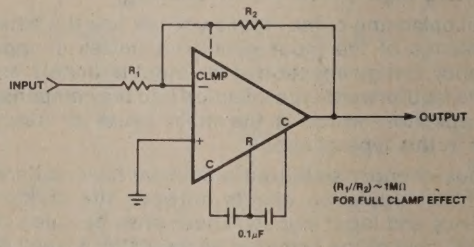
Normal logarithmic amplifiers are limited in dynamic range in the voltage input mode by their input offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be expanded to a voltage input dynamic range of close to 6 decades by using the ICL7650 to offset-null the ICL8048, as shown in Fig. 6. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps, to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

Mixing the ICL7650 with circuits operating at ±15V supplies requires the provision of a lower voltage. Although this can be met fairly easily, a highly efficient voltage divider can be built using the ICL7660 voltage converter circuit 'backwards'. A suitable connection is shown in Fig. 7.



$R_3 + (R_1 // R_2) \sim 1M\Omega$
FOR FULL CLAMP EFFECT

FIG. 2 NON INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP



$(R_1 // R_2) \sim 1M\Omega$
FOR FULL CLAMP EFFECT

FIG. 3 INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP

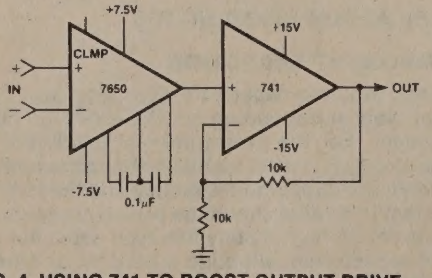


FIG. 4 USING 741 TO BOOST OUTPUT DRIVE CAPABILITY

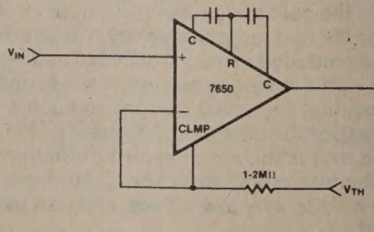


FIG. 5 LOW OFFSET COMPARATOR

STATIC PROTECTION

All device pins are static protected by the use of input diodes. However strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input leakage currents.

LATCH-UP AVOIDANCE

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

OUTPUT STAGE/LOAD DRIVING

The output circuit is a high-impedance stage (approximately 18kΩ), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open loop gain is proportional to load resistance. For example the open loop gain will be 17 dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10k or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

THERMO-ELECTRIC EFFECTS

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermo-couple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermo-electric coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

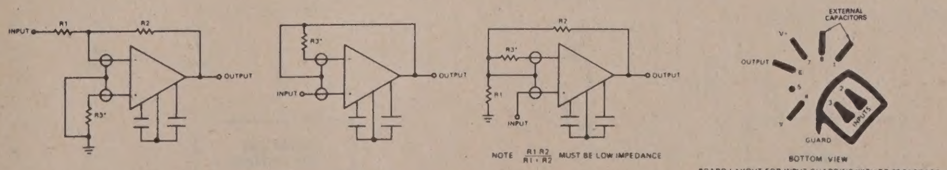
GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage at the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

CONNECTION OF INPUT GUARDS



NOTE $\frac{R1\,R2}{R1+R2}$ MUST BE LOW IMPEDANCE

BOTTOM VIEW

BOARD LAYOUT FOR INPUT GUARDING WITH TO 99 PACKAGE

*USE TO COMPENSATE FOR LARGE SOURCE RESISTANCES

INVERTING AMPLIFIER FOLLOWER NON-INVERTING AMPLIFIER

TYPICAL APPLICATIONS (Contd.)

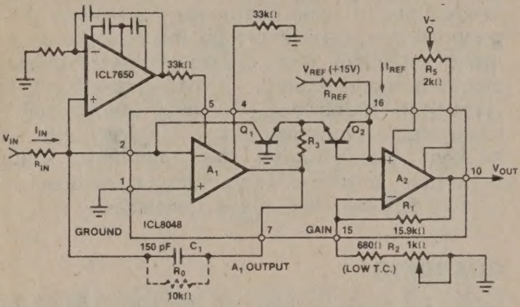

ICL7650
33kΩ
33kΩ
V-
V_{REF} (+15V)
R_{REF}
I_{REF}
R_5
2kΩ
5
4
16
V_{IN}
I_{IN}
R_{IN}
2
1
Q_1
R_3
Q_2
A_1
A_2
10
V_{OUT}
R_1
15.9kΩ
GROUND
ICL8048
7
GAIN
15
150 pF
C_1
R_0
10kΩ
A_1 OUTPUT
680Ω
R_2
1kΩ
(LOW T.C.)

FIG. 6 ICL8048 OFFSET NULLED BY ICL7650

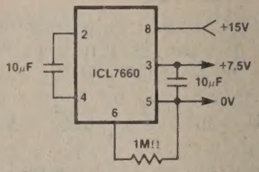

2
8
+15V
10μF
ICL7660
3
+7.5V
10μF
4
5
0V
6
1MΩ

FIG. 7 SPLITTING +15V WITH ICL7660.
SAME FOR −15V. >95% EFF.

INTERSIL

ICL7660
Monolithic MAXCMOS® Voltage Converter

PRELIMINARY
Specifications Subject To Change Without Notice

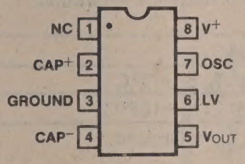
FEATURES

- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication ($V_{OUT} \doteq (-)\ nV_{IN}$)**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **98% Typical Power Efficiency**
- **Wide Operating Voltage Range 1.5V to 10.0V**
- **Easy to use - Requires only 2 External Non-Critical Passive Components**

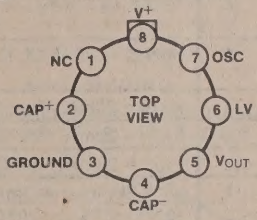
APPLICATIONS

- On Board Negative Supply for up to 64 Dynamic RAMs.
- Localized μ-Processor (8080 type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

PIN CONFIGURATIONS



(outline dwg PA)



(outline dwg TO-99)

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7660CTY	−20° to +70°C	TO-99
ICL7660CPA	−20° to +70°C	8 PIN MINI DIP
ICL7660MTY	−55° to +125°C	TO-99
ICL7660/D		DICE

GENERAL DESCRIPTION

The Intersil ICL7660 is a monolithic MAXCMOS® power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of −1.5 to −10.0V with the addition of only 2 non-critical external capacitors needed for the charge pump and charge reservoir functions. Note that an additional diode is required for V_{SUPPLY} >6.5V.

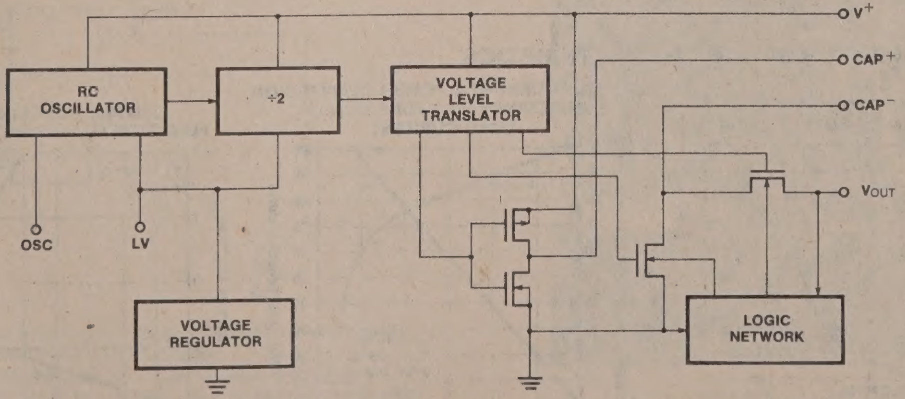
Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

Typical applications for the ICL7660 will be data acquisition and microprocessor based systems where there is a +5 volt supply available for the digital functions and an additional −5 volt supply is required for the analog functions. The ICL7660 is also ideally suited for providing low current, −5V body bias supply for dynamic RAMs.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	10.5V
Oscillator Input Voltage (Note 1)	−0.3V to (V^+ +0.3V) for $V^+ < 5.5V$ (V^+ −5.5V) to (V^+ +0.3V) for $V^+ > 5.5V$ −0.3V to (V^+ +0.3V) for $V^+ < 3.5V$
LV (Note 1)	No connection for V > 3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$)	Continuous
Power Dissipation (Note 2)	
ICL7660CTY	500mW
ICL7660CPA	300mW
ICL7660MTY	500mW

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS $V^+ = 5V$, $T_A = 25°C$, $C_{OSC} = 0$, Test Circuit Figure 1 (unless otherwise specified)

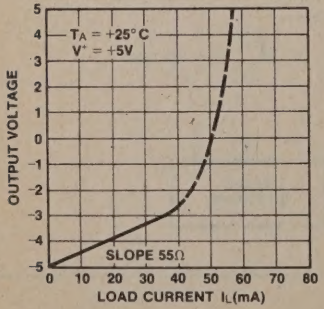
SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I^+	Supply Current		170	500	μA	$R_L = \infty$
V^+_{H1}	Supply Voltage Range - Hi (Dx out of circuit)	3.0		6.5	V	$0°C \leq T_A \leq 70°C$, $R_L = 10k\Omega$, LV = No Connection
		3.0		5.0	V	$-55°C \leq T_A \leq 125°C$, $R_L = 10k\Omega$, LV = Ground
V^+_{L1}	Supply Voltage Range - Lo (Dx out of circuit)	1.5		3.5	V	MIN $\leq T_A \leq$ MAX, $R_L = 10k\Omega$, LV = Ground
V^+_{H2}	Supply Voltage Range - Hi (Dx in circuit)	3.0		10.0	V	MIN $\leq T_A \leq$ MAX, $R_L = 10k\Omega$, LV = No Connection
V^+_{L2}	Supply Voltage Range - Lo (Dx in circuit)	1.5		3.5	V	MIN $\leq T_A \leq$ MAX, $R_L = 10k\Omega$, LV = Ground
R_{OUT}	Output Source Resistance		55	100	Ω	$I_{OUT} = 20mA$, $T_A = 25°C$
				120	Ω	$I_{OUT} = 20mA$, $-20°C \leq T_A \leq +70°C$
				150	Ω	$I_{OUT} = 20mA$, $-55°C \leq T_A \leq +125°C$
				300	Ω	$V^+ = 2V$, $I_{OUT} = 3mA$, LV = Ground, $-20°C \leq T_A \leq +70°C$
				400	Ω	$V^+ = 2V$, $I_{OUT} = 3mA$, LV = Ground, $-55°C \leq T_A \leq +125°C$, Dx in circuit
f_{OSC}	Oscillator Frequency		10		kHz	
P_{Ef}	Power Efficiency	95	98		%	$R_L = 5k\Omega$
$V_{OUT\ Ef}$	Voltage Conversion Efficiency	97	99.9		%	$R_L = \infty$
Z_{OSC}	Oscillator Impedance		1.0		MΩ	$V^+ = 2$ Volts
			100		kΩ	$V^+ = 5$ Volts

Notes: **1.** Connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.

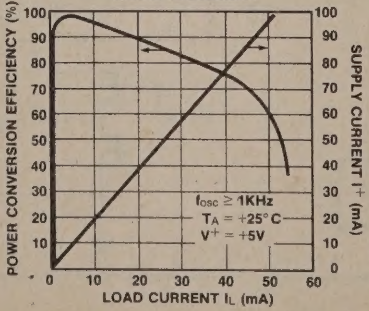
2. Derate linearly above 50°C by 5.5mW/°C.

TYPICAL PERFORMANCE CHARACTERISTICS

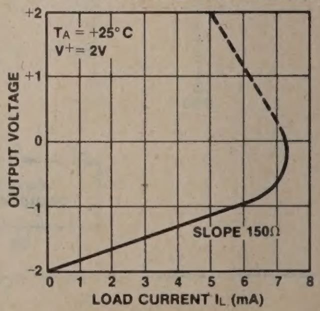
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



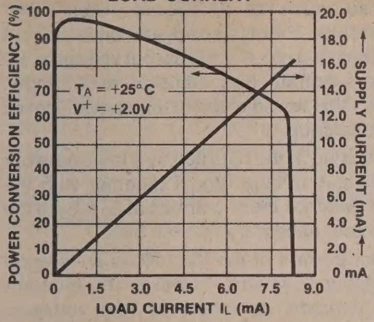
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



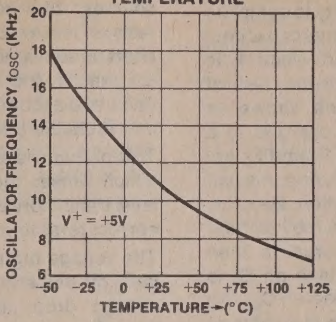
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



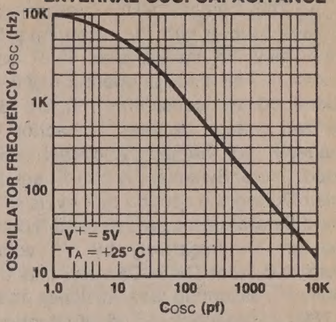
SUPPLY CURRENT POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



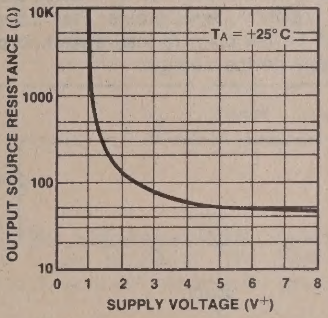
UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



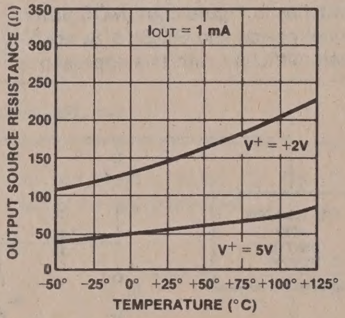
FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



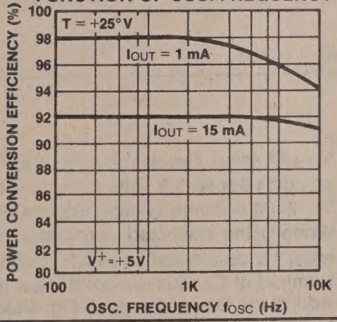
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



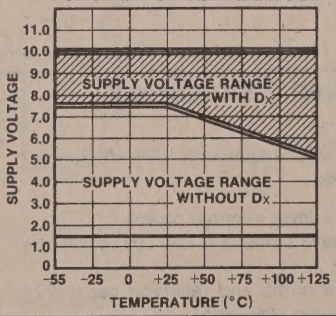
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE

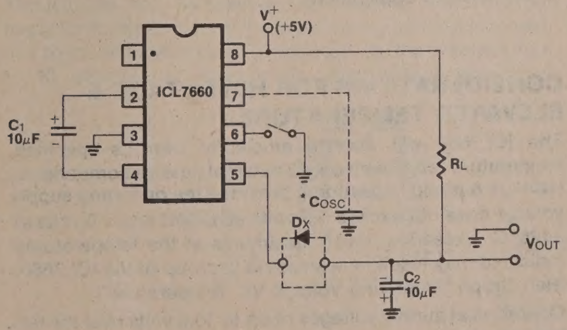


POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE




V+
(+5V)
ICL7660
1
2
3
4
8
7
6
5
C1
10μF
RL
*COSC
DX
VOUT
C2
10μF

NOTES: 1. For large value of COSC (>1000pF) the values of C1 and C2 should be increased to 100μF.

2. DX is required for supply voltages greater than 6.5V @ -55° ≤ TA ≤ +70°C; refer to performance curves for additional information.

Figure 1: ICL7660 Test Circuit

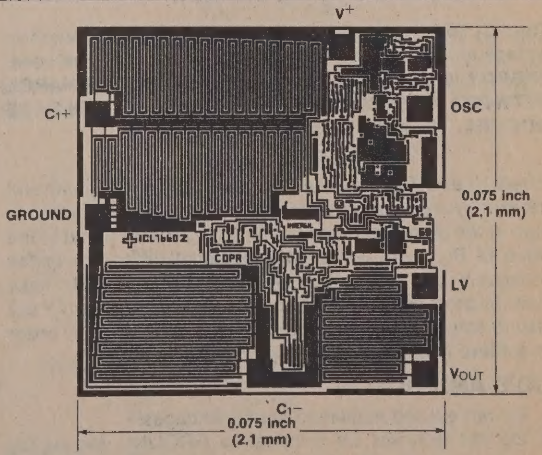

V+
C1+
OSC
GROUND
0.075 inch
(2.1 mm)
LV
VOUT
C1−
0.075 inch
(2.1 mm)
ICL7660Z
COPR
INTERSIL

Figure 2: Chip Topography

CIRCUIT DESCRIPTION

The ICL7660 contains all the necessary circuitry to complete a voltage doubler, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 3, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660, the 4 switches in Figure 3 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators and switches the substrates or S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 is an integral part of the anti-latchup circuitry, however it's inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

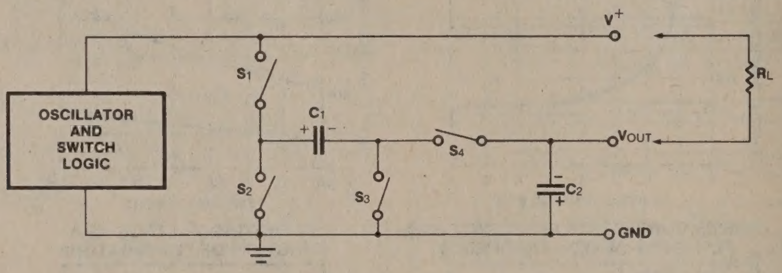


Figure 3: Idealized Voltage Doubler

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = 1/2\, C_1 (V_1{}^2 - V_2{}^2)$$

Where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Fig. 3) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1 Do not exceed maximum supply voltages.

2 Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.

3 Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.

4 When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and the + terminal of C_2 must be connected to GROUND.

5 Add diode D_X as shown in Fig. 1 for hi-voltage, elevated temperature applications.

CONSIDERATIONS FOR HI-VOLTAGE & ELEVATED TEMPERATURE

The ICL7660 will operate efficiently over its specified temperature range with only 2 external passive components (storage & pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70°C and 5.0 volts at +125°C. Exceeding these maximums at the temperatures indicated may result in destructive latch-up of the ICL7660. (Ref: Graph "Operating Voltage Vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latch-up can be achieved by adding a general purpose diode in series with the ICL7660 output, as shown by "Dx" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

TYPICAL APPLICATIONS

1. Simple Negative Voltage Converter

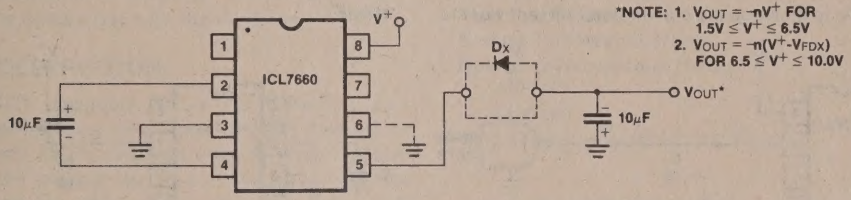
The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 4 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +10.0 volts, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5 volts, and that diode D_X must be included for proper operation at higher voltages and/or elevated temperatures.

The output characteristics of the circuit in Figure 4 are those of a nearly ideal voltage source in series with 70 ohms. Thus for a load current of −10mA and a supply voltage of +5 volts, the output voltage will be −4.3 volts. The dynamic output impedance due to the capacitor impedances is $1/\omega C$ where

$$C = C_1 = C_2$$

$$\text{giving} \quad \frac{1}{\omega C} = \frac{1}{2\pi f_{OSC} \times 10^{-5}} = 3 \text{ ohms}$$

for $C = 10\mu F$ and $f_{OSC} = 5kHz$ (1/2 of oscillator frequency)



*NOTE: 1. $V_{OUT} = -nV^+$ FOR $1.5V \le V^+ \le 6.5V$
2. $V_{OUT} = -n(V^+ - V_{FDX})$ FOR $6.5 \le V^+ \le 10.0V$

Figure 4: Simple Negative Converter

2. Paralleling Devices

Any number of ICL7660 voltage convertors may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately

$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7660)}}{n \text{ (number of devices)}}$$

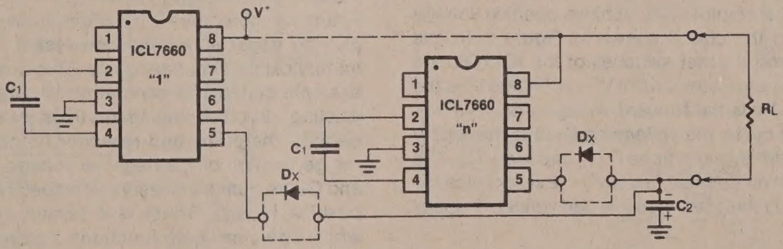


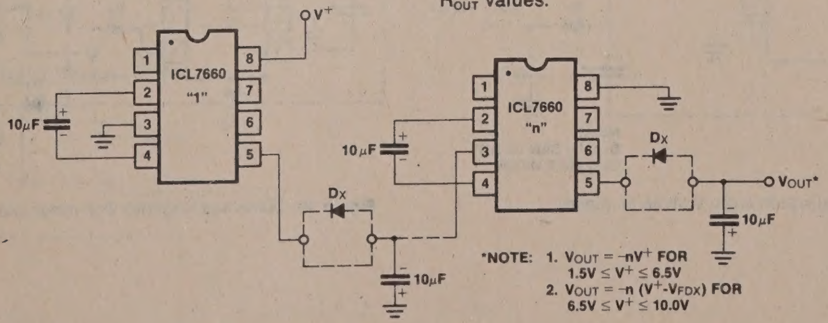
Figure 5: Paralleling Devices

3. Cascading Devices

The ICL7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage, however, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\,(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 R_{OUT} values.



*NOTE: 1. $V_{OUT} = -nV^+$ FOR $1.5V \le V^+ \le 6.5V$
2. $V_{OUT} = -n\,(V^+ - V_{FDX})$ FOR $6.5V \le V^+ \le 10.0V$

Figure 6: Cascading Devices for Increased Output Voltage

4. Changing the ICL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the ICL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 8. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10μF to 100μF).

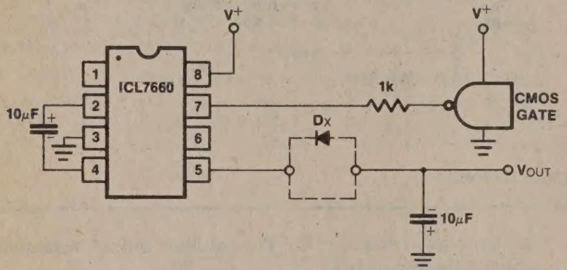


Figure 7: External Clocking

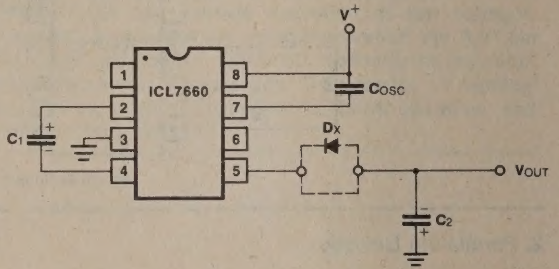
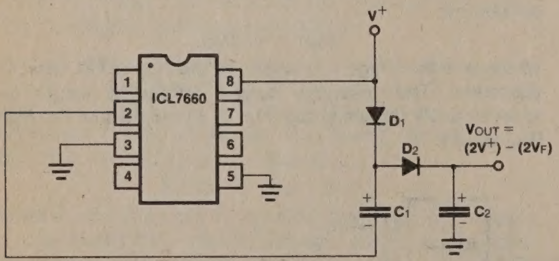


Figure 8: Lowering Oscillator Frequency

5. Positive Voltage Multiplication

The ICL7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 9. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.



NOTE:
D1 & D2 CAN BE ANY SUITABLE DIODE

Figure 9: Positive Voltage Multiplier

6. Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 4 and 9 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

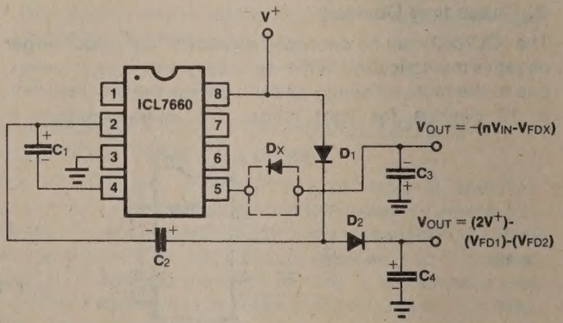


Figure 10: Combined Negative Converter and Positive Multiplier

ICL8001
Precision Comparator

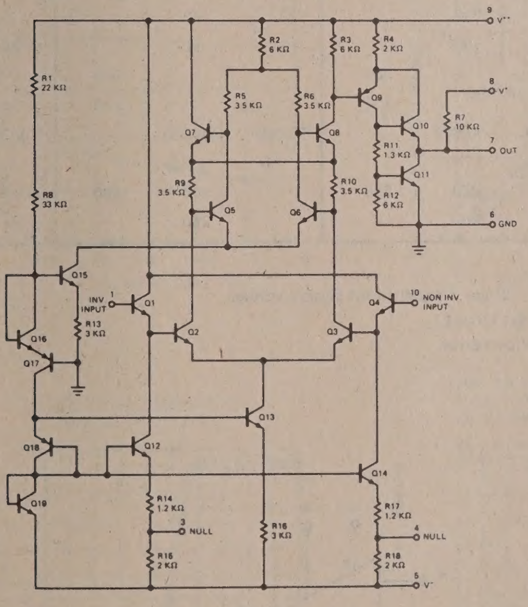
FEATURES

- Low Input Current ≤ 250 nA
- Low Power Consumption 30 mW
- Large Input Voltage Range $\geq \pm 10$V
- Low Offset Voltage Drift 3 μV/°C
- Output Swing Compatible with Bipolar Logic

GENERAL DESCRIPTION

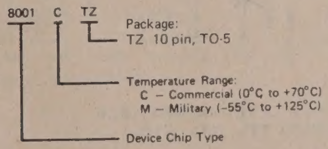
The Intersil 8001 integrated circuit is a monolithic voltage comparator featuring low input currents, low power consumption, and 250 ns response time. A versatile output stage enables the designer to control the output voltage swing. The use of thin film resistors ensures excellent long term stability and the device is particularly suitable for low power space and airborne applications.

SCHEMATIC DIAGRAM



9 V⁺⁺
R1 22 KΩ
R2 6 KΩ
R3 6 KΩ
R4 2 KΩ
8 V⁺
R5 3.5 KΩ
R6 3.5 KΩ
Q9
Q7
Q8
Q10
R7 10 KΩ
7 OUT
R11 1.3 KΩ
Q11
R8 33 KΩ
R9 3.5 KΩ
R10 3.5 KΩ
R12 6 KΩ
Q5
Q6
6 GND
Q15
1 INV INPUT
Q1
R13 3 KΩ
Q4
10 NON INV INPUT
Q16
Q2
Q3
Q17
Q13
Q18
Q12
Q14
Q19
R14 1.2 KΩ
3 NULL
R16 3 KΩ
R17 1.2 KΩ
4 NULL
R15 2 KΩ
R18 2 KΩ
5 V⁻

ORDERING INFORMATION



Package:
TZ 10 pin, TO-5

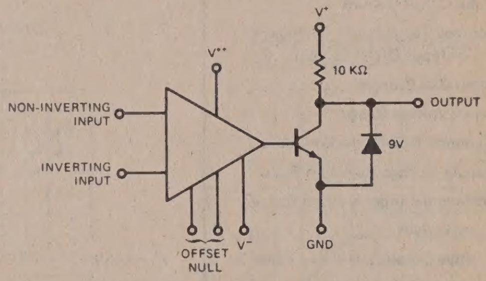
Temperature Range:
C – Commercial (0°C to +70°C)
M – Military (–55°C to +125°C)

Device Chip Type

ABSOLUTE MAXIMUM RATINGS

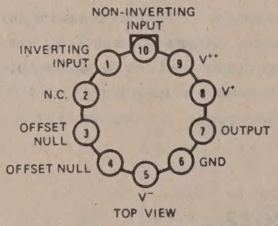
Supply Voltage	±18V
Input Voltage (Note 2)	±18V
Differential Input Voltage	±15V
Internal Power Dissipation (Note 1)	500 mW
Peak Output Current	15 mA
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	
(8001C)	0°C to +70°C
(8001M)	–55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

EQUIVALENT CIRCUIT



V⁺
V⁺⁺
10 KΩ
NON-INVERTING INPUT
OUTPUT
9V
INVERTING INPUT
OFFSET NULL
V⁻
GND

PIN CONFIGURATION



NON-INVERTING INPUT
10
INVERTING INPUT 1
9 V⁺⁺
N.C. 2
8 V⁺
OFFSET NULL 3
7 OUTPUT
OFFSET NULL 4
6 GND
5 V⁻
TOP VIEW

(outline dwg TO-100)

NOTE: Pin 5 connected to case.

NOTES and Additional Electrical Characteristics on Page 5-168.

ELECTRICAL CHARACTERISTICS (V^{++} = 15V, V$^+$ = 5V, V$^-$ = –15V unless otherwise specified)

PARAMETER	CONDITIONS	8001M MIN	8001M TYP	8001M MAX	8001C MIN	8001C TYP	8001C MAX	UNITS
The following specifications apply for T_A = +25°C:								
Input Offset Voltage	$R_S \leq 10$ kΩ		0.5	3.0		1.0	5.0	mV
Input Offset Current			2	20		10	50	nA
Input Bias Current			40	100		50	250	nA
Input Resistance			10			10		MΩ
Power Consumption	V_{OUT} = 2.5V		30	60		30	60	mW
The following specifications apply for $-55°C \leq T_A \leq +125°C$ (8001M) $0°C \leq T_A \leq +70°C$ (8001C)								
Input Offset Voltage	$R_S \leq 10$ kΩ			4.0			6.0	mV
Average Temperature Coefficient of Input Offset Voltage			2.0	20		3.0	30	μV/°C
Input Offset Current			7	100		15	100	nA
Average Temperature Coefficient of Input Offset Current			35			35		pA/°C
Input Bias Current				250			300	nA
Input Voltage Range		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		dB
Supply Voltage Rejection Ratio				300			300	μV/V
Differential Input Voltage Range				±15			±15	V
Voltage Gain		15,000	60,000		15,000	60,000		V/V
Positive Output Level Max (Note 3)	V$^+$ = +15V	7.0	9.0		7.0	9.0		V
Negative Output Level	At 2 mA Sink Current		200	500		200	400	mV
Response Time (Note 4)			250			250		ns

NOTE 1: Rating applies for ambient temperatures to +70°C.

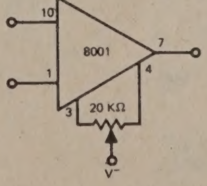
NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 3: Positive output level can be adjusted below 9V by changing V$^+$. See circuit.

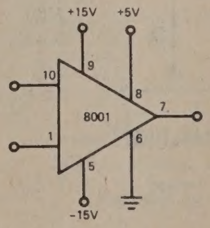
NOTE 4: The response time specified is for a 100 mV input step with 5 mV overdrive.

NOTE 5: Input bias current is independent of V$^-$.

CIRCUIT NOTES:



VOLTAGE OFFSET
NULL CIRCUIT

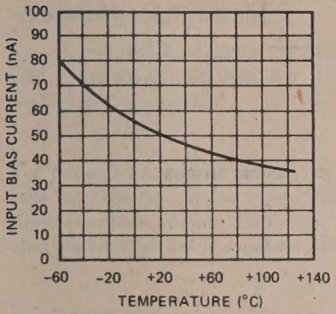


OUTPUT LEVEL COMPATIBLE
WITH TTL, DTL, ETC.

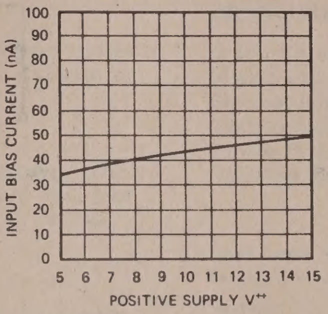
NOTE: As with all high gain comparators, care must be taken to avoid feedback between output and input. Where possible, hysteresis should be used to provide a small deadband.

TYPICAL PERFORMANCE CURVES

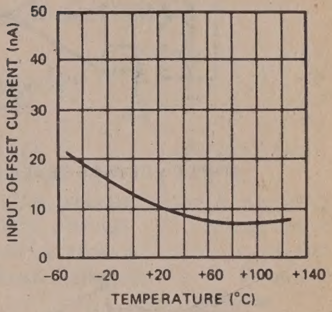
INPUT BIAS CURRENT
AS A FUNCTION OF
AMBIENT TEMPERATURE



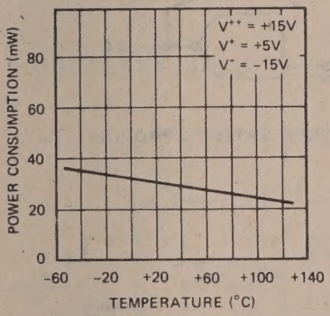
INPUT BIAS CURRENT
AS A FUNCTION OF
V⁺⁺ (NOTE 5)



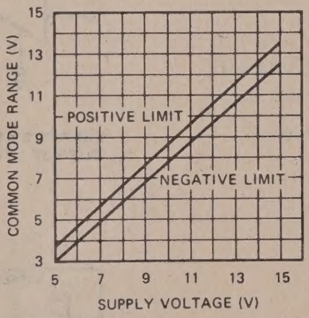
INPUT OFFSET CURRENT
AS A FUNCTION OF
AMBIENT TEMPERATURE



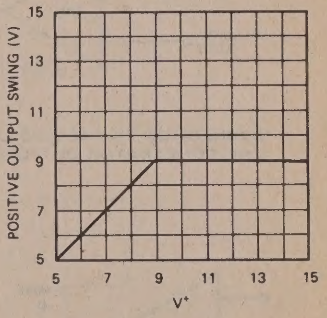
POWER CONSUMPTION
AS A FUNCTION OF
AMBIENT TEMPERATURE



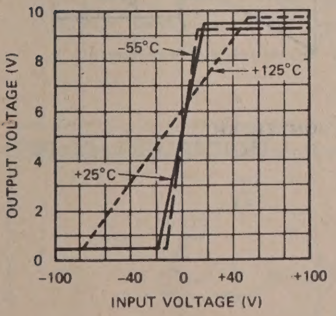
COMMON MODE RANGE
AS A FUNCTION OF
SUPPLY VOLTAGE



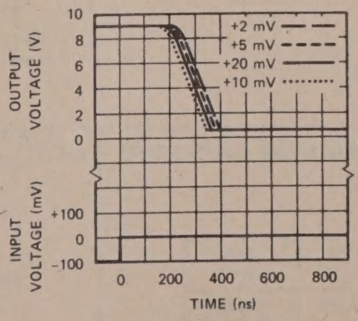
POSITIVE OUTPUT SWING
AS A FUNCTION OF V⁺



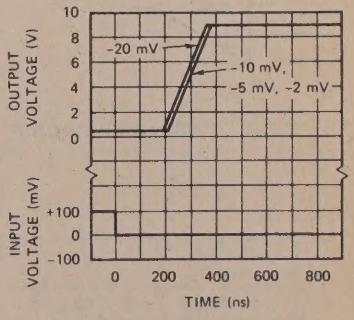
VOLTAGE TRANSFER
CHARACTERISTICS



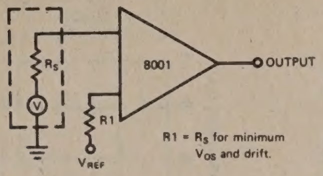
RESPONSE TIME FOR
VARIOUS INPUT
OVERDRIVES



RESPONSE TIME FOR
VARIOUS INPUT
OVERDRIVES

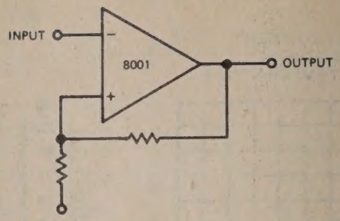


CIRCUIT AND APPLICATION NOTES



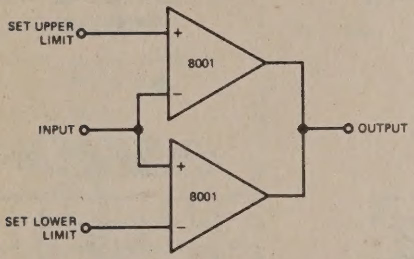
R_S
V
R1
8001
OUTPUT
V_{REF}
R1 = R_S for minimum V_{OS} and drift.

SIMPLE VOLTAGE LEVEL DETECTOR



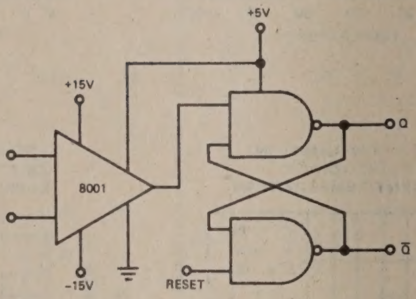
INPUT
−
+
8001
OUTPUT

COMPARATOR WITH HYSTERESIS



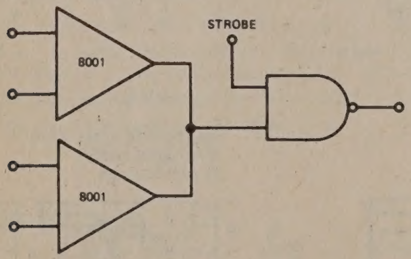
SET UPPER LIMIT
+
−
8001
INPUT
OUTPUT
+
−
8001
SET LOWER LIMIT

CONNECTION TO PROVIDE LOGICAL OR OF TWO COMPARATOR OUTPUTS



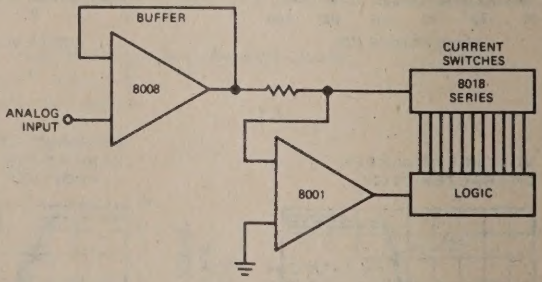
+5V
+15V
8001
−15V
RESET
Q
$\bar{Q}$

USE OF EXTERNAL NAND GATES TO PROVIDE OUTPUT STORAGE



8001
8001
STROBE

WINDOW DETECTOR



BUFFER
8008
ANALOG INPUT
CURRENT SWITCHES
8018 SERIES
8001
LOGIC

A TO D CONVERTER

INTERSIL

ICL8007
FET Input Operational Amplifier

GENERAL DESCRIPTION

The Intersil 8007 integrated circuit is a low input current FET input operational amplifier. The 8007A is selected for 1 pA max input current.

The devices are designed for use in very high input impedance applications. Because of their high slew rate, high common mode voltage range and absence of "latch-up", they are ideal for use as a voltage follower.

The Intersil 8007 and 8007A are short circuit protected. They require no external components for frequency compensation because the internal 6 dB/roll-off insures stability in closed loop applications. A unique bootstrap circuit insures unusually good commonmode rejection for an FET input amp and prevents large input currents as seen in some amplifiers at high common mode voltage.

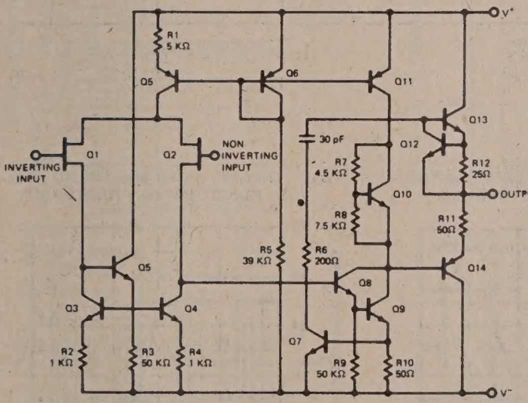
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
8007M, 8007AM	−55°C to +125°C
8007C, 8007AC	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

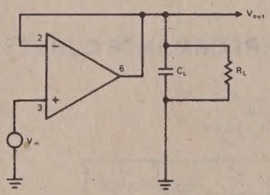
NOTES:

1. Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

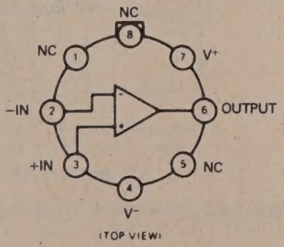
EQUIVALENT CIRCUIT


V+
R1 5 KΩ
Q5
Q6
Q11
Q13
Q1
Q2
NON INVERTING INPUT
INVERTING INPUT
30 pF
Q12
R7 4.5 KΩ
R12 25Ω
OUTPUT
Q10
R8 7.5 KΩ
R11 50Ω
R5 39 KΩ
R6 200Ω
Q5
Q14
Q8
Q3
Q4
Q9
Q7
R2 1 KΩ
R3 50 KΩ
R4 1 KΩ
R9 50 KΩ
R10 50Ω
V−

TRANSIENT RESPONSE TEST CIRCUIT


Vout
2
−
+
3
6
CL
RL
Vin

PIN CONFIGURATION (outline dwg TO-99)


NC
8
NC
1
7
V+
−IN
2
6
OUTPUT
+IN
3
5
NC
4
V−
(TOP VIEW)

NOTE: Pin 4 connected to case

ORDERING INFORMATION

Part Number	Temperature Range	dice	To-99 Can
ICL8007C	0°C to +70°C	ICL8007C/D	ICL8007CTV
ICL8007AC		ICL8007AC/D	ICL8007ACTV
ICL8007M	−55°C to +125°C	ICL8007M/D	ICL8007MTV
ICL8007AM		ICL8007AM/D	ICL8007AMTV*

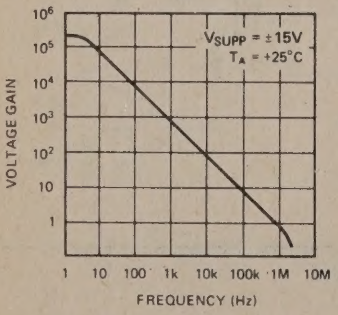
* Add /883B to order number if 883B processing is desired.

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$ unless otherwise specified)

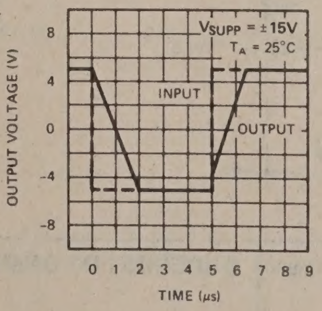
CHARACTERISTICS	CONDITIONS	8007M			8007C			8007AM & 8007AC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
The following specifications apply for $T_A = 25°C$:											
Input Offset Voltage	$R_S \leq 100\ k\Omega$		10	20		20	50		15	30	mV
Input Offset Current			0.5			0.5			0.2		pA
Input Current (either input)			2.0	20		3.0	50		0.5	4.0	pA
Input Resistance			10^6			10^6			10^6		MΩ
Input Capacitance			2.0			2.0			2.0		pF
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10V$	50,000			20,000			20,000			V/V
Output Resistance			75			75			75		Ω
Output Short-Circuit Current			25			25			25		mA
Supply Current			3.4	5.2		3.4	6.0		3.4	6.0	mA
Power Consumption			102	156		102	180		102	180	mW
Slew Rate			6.0			6.0		2.5	6.0		V/μs
Unity Gain Bandwidth			1.0			1.0			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100\ pF$, $R_L = 2\ k\Omega$										
Risetime			300			300			300		ns
Overshoot			10			10			10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$ (8007C and 8007AC), $-55°C \leq T_A \leq +125°C$ (8007M and 8007AM):											
Input Voltage Range		±10	±12		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		86	95		dB
Supply Voltage Rejection Ratio			70	300		70	600		70	200	μV/V
Large Signal Voltage Gain		25,000			15,000			15,000			V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		±10	±13		V
Input Current (either input)	$T_A = +125°C$		2.0						1.0		nA
	$T_A = +70°C$					50			30		pA
Average Temperature Coefficient of Input Offset Voltage				75			75			50	μV/°C

TYPICAL PERFORMANCE CURVES

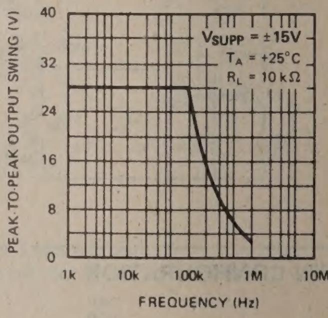
OPEN LOOP VOLTAGE GAIN



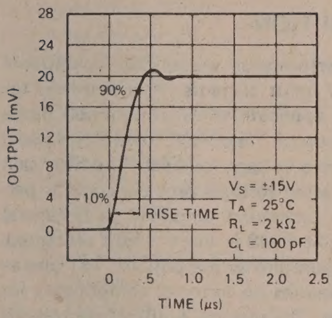
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



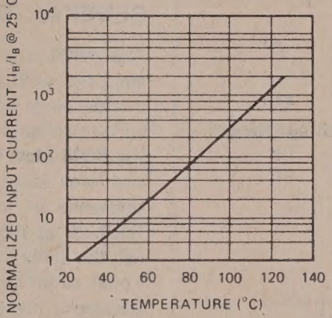
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



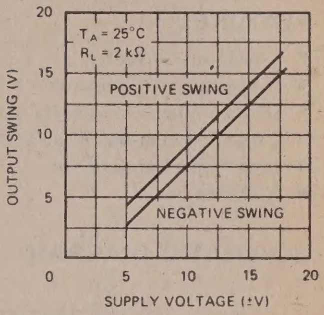
TRANSIENT RESPONSE



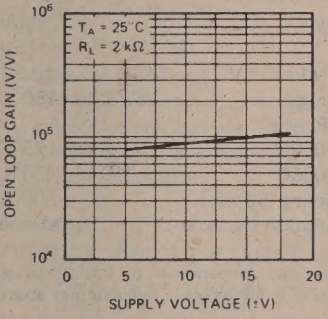
INPUT CURRENT AS A FUNCTION OF TEMPERATURE



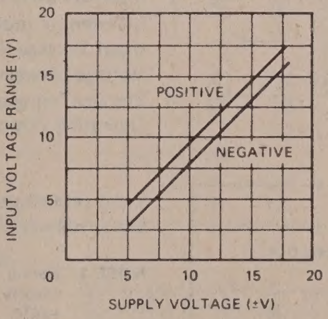
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



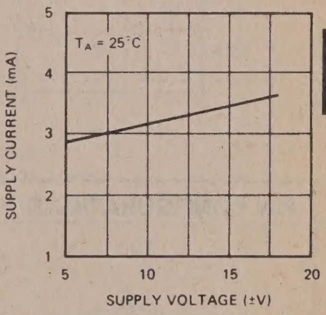
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



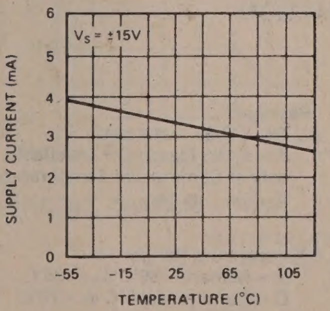
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



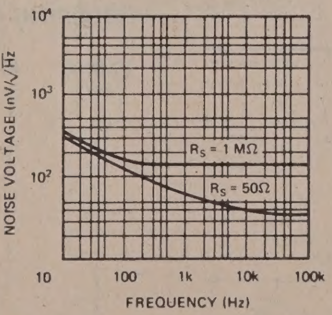
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



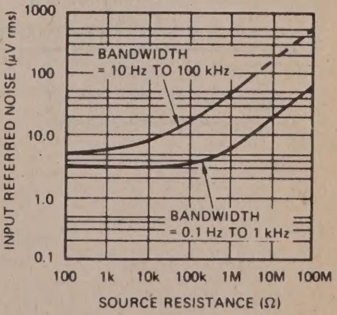
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



For additional information, see Application Bulletin A005.

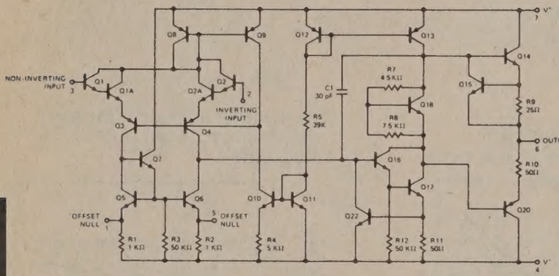
ICL8008

Low Input Current Operational Amplifier

FEATURES

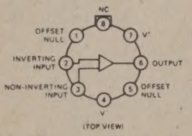
- Low Input Current
- No Frequency Compensation Required
- Offset Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch up

SCHEMATIC DIAGRAM


V⁺
7
Q8
Q9
Q12
Q13
Q14
NON-INVERTING INPUT
3
Q1
Q1A
Q2A
Q2
2
INVERTING INPUT
C1
30 pF
R7
4.5 KΩ
Q15
Q18
R9
25Ω
Q3
Q4
R5
39K
R8
7.5 KΩ
OUTPUT
6
Q7
Q16
R10
50Ω
Q17
Q5
Q6
Q10
Q11
Q20
Q22
OFFSET NULL
1
5
OFFSET NULL
R1
1 KΩ
R3
50 KΩ
R2
1 KΩ
R4
5 KΩ
R12
50 KΩ
R11
50Ω
V⁻
4

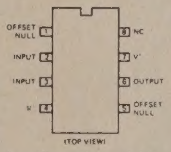
PIN CONFIGURATIONS

TO-5


NC
8
OFFSET NULL
1
7
V⁺
INVERTING INPUT
2
6
OUTPUT
NON-INVERTING INPUT
3
5
OFFSET NULL
4
V⁻
(TOP VIEW)

(outline dwg TO-99)

Plastic DIP


OFFSET NULL
1
INPUT
2
INPUT
3
V⁻
4
8
NC
7
V⁺
6
OUTPUT
5
OFFSET NULL
(TOP VIEW)

(outline dwg PA)

NOTE: Pin 4 CONNECTED TO CASE

GENERAL DESCRIPTION

The 8008 is a high performance monolithic operational amplifier with very low input currents. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the 8008 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The 8008 is short-circuit protected, has the same pin configuration as the popular 741 operational amplifier, and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V⁻	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
8008M	−55°C to +125°C
8008C	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

NOTE 1: Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 3: Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

ORDERING INFORMATION

ICL8008 M TY

Package:
TY—TO-99 metal can
PA—8 Pin Plastic DIP (Available only at Commercial Temperature Range) ID Dice

Temperature Range:
M—Military −55°C to +125°C
C —Commercial 0°C to +70°C

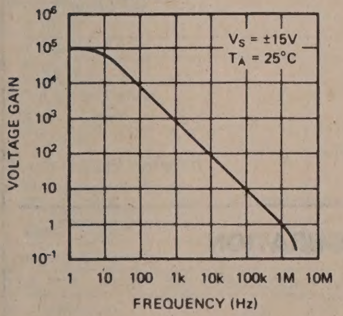
Device Type

ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

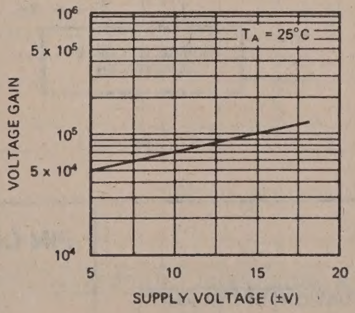
CHARACTERISTICS	CONDITIONS	8008M			8008C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	5		1.0	6.0	mV
Input Offset Current			1.0	5		2.0	20	nA
Input Bias Current			2	10		5	25	nA
Input Resistance		5	25		5	25		MΩ
Input Capacitance			1.5			1.5		pF
Offset Voltage Adjustment Range			±15			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	20,000	200,000		20,000	200,000		V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	V_{IN} = 20 mV, R_L = 2 kΩ,							
Risetime	$C_L \leq 100$ pF		0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate (unity gain)	$R_L \geq 2\ k\Omega$		0.5			0.5		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8008C), −55°C ≤ T_A ≤ +125°C (8008M):								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.5	6		1.5	7.5	mV
Input Offset Voltage Average Temperature Coefficient	$R_S \leq 10\ k\Omega$		7			15		μV/°C
Input Offset Current				30			30	nA
Input Bias Current				50			50	nA
Input Voltage Range		±10	±12		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	15,000			15,000			V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V

TYPICAL PERFORMANCE CURVES

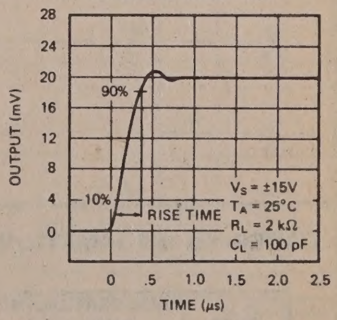
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

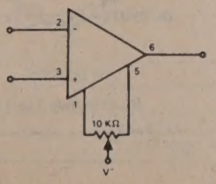


TRANSIENT RESPONSE

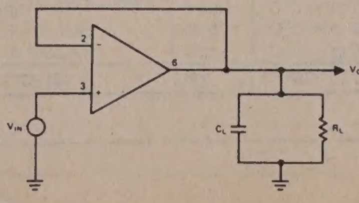


CIRCUIT NOTES:

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



INTERSIL

ICL8013

Four Quadrant Analog Multiplier

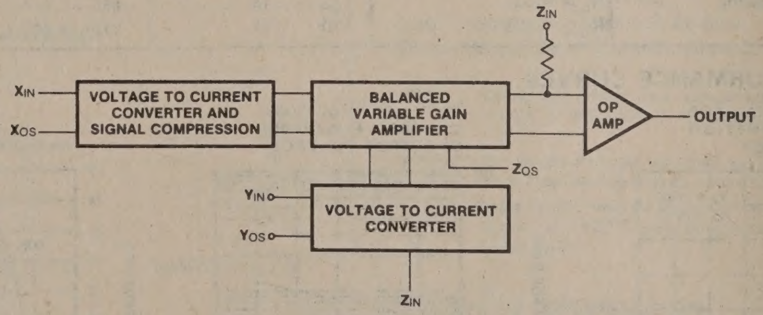
FEATURES

- **Accuracy of ±0.5% ("A" version)**
- **Full ±10V I/O voltage range**
- **1 MHz bandwidth**
- **Uses standard ±15V supplies**
- **Built in op amp provides level shifting, division and square root functions.**

GENERAL DESCRIPTION

The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 makes it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment, frequency doublers, balanced modulators and demodulators, function generators, and systems process controls.

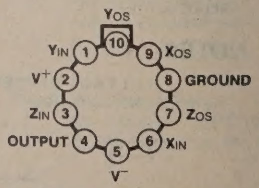
BLOCK DIAGRAM (MULTIPLIER)


ZIN
XIN
XOS
VOLTAGE TO CURRENT CONVERTER AND SIGNAL COMPRESSION
BALANCED VARIABLE GAIN AMPLIFIER
OP AMP
OUTPUT
ZOS
YIN
YOS
VOLTAGE TO CURRENT CONVERTER
ZIN

ORDERING INFORMATION

TYPE	TEMPERATURE RANGE	MULTIPLICATION ERROR	ORDER PART NUMBER
ICL8013AM	-55°C to +125°C	±.5% MAX	ICL8013AM TZ
ICL8013BM	-55°C to +125°C	±1%	ICL8013BM TZ
ICL8013CM	-55°C to +125°C	±2%	ICL8013CM TZ
ICL8013AC	0°C to +70°C	±.5%	ICL8013AC TZ
ICL8013BC	0°C to +70°C	±1%	ICL8013BC TZ
ICL8013CC	0°C to +70°C	±2%	ICL8013CC TZ
ICL8013C/D	0°C to +70°C	±2% TYP	ICL8013C/D

PIN CONFIGURATION


YOS
10
YIN 1
9 XOS
V+ 2
8 GROUND
ZIN 3
7 ZOS
OUTPUT 4
6 XIN
5
V−

TOP VIEW

(outline dwg TO-100)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±18V
Power Dissipation (Note 1) .... 500 mW
Input Voltages (X, Y, Z, X_O, Y_O, Z_O) .... V_{SUPP}
Lead Temperature (soldering, 10 sec) .... 300°C
Storage Temperature Range .... −65°C to +150°C

NOTE 1: Derate at 6.8 mW/°C for operation at ambient temperature above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified $T_A = 25°C$, $V_{SUPP} = \pm 15V$, Gain and Offset Potentiometers Externally Trimmed)

PARAMETER	CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Multiplier Function			$\frac{XY}{10}$			$\frac{XY}{10}$			$\frac{XY}{10}$		
Multiplication Error	−10 < X < 10 −10 < Y < 10			.5			1.0		2.0*	2.0	% Full Scale
Divider Function			$\frac{10Z}{X}$			$\frac{10Z}{X}$			$\frac{10Z}{X}$		
Division Error	X = −10 X = −1		0.3 1.5			0.3 1.5			0.3 1.5		% Full Scale % Full Scale
Feedthrough	X = 0 Y = 20V_{p-p} f = 50Hz Y = 0 X = 20V_{p-p} f = 50Hz			50 50			100 100		200* 150*	200 150	mV_{p-p} mV_{p-p}
Nonlinearity X Input	X = 20V_{p-p} Y = ±10Vdc		±0.5			±0.5			±0.8		%
Y Input	Y = 20V_{p-p} X = ±10Vdc		±0.2			±0.2			±0.3		%
Frequency Response Small Signal Bandwidth (−3dB)			1.0			1.0			1.0		MHz
Full Power Bandwidth			750			750			750		kHz
Slew Rate			45			45			45		V/μs
1% Amplitude Error			75			75			75		kHz
1% Vector Error (0.5° Phase Shift)			5			5			5		kHz
Settling Time (to ±2% of Final Value)	V_{IN} = ±10V		1			1			1		μs
Overload Recovery (to ±2% of Final Value)			1			1			1		μs
Output Noise	5 Hz to 10 kHz 5 Hz to 5 MHz		0.6 3			0.6 3			0.6 3		mV rms mV rms
Input Resistance X Input			10			10			10		MΩ
Y Input			6			6			6		MΩ
Z Input			36			36			36		kΩ
Input Bias Current X or Y Input			2	5			7.5			10	μA
Z Input			25			25			25		μA
Power Supply Variation Multiplication Error			0.2			0.2			0.2		%/%
Output Offset				50			75			100	mV/V
Scale Factor			0.1			0.1			0.1		%/%
Quiescent Current			3.5	6.0		3.5	6.0		3.5	6.0	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES											
Multiplication Error	−10 < X < 10, −10 < Y < 10		1.5			2			3		% Full Scale
Average Temperature Coefficient of Accuracy			0.06			0.06			0.06		%/°C
Output Offset			0.2			0.2			0.2		mV/°C
Scale Factor			0.04			0.04			0.04		%/°C
Input Bias Current X or Y Input				5			5			10	μA
Z Input				25			25			35	μA
Input Voltage (X, Y, or Z)				±10			±10			±10	V
Output Voltage Swing	R_L ≥ 2k C_L < 1000 pF		±10			±10			±10		V

*Dice only

CIRCUIT DESCRIPTION

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 1.

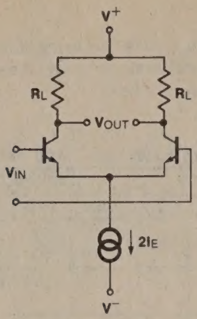


Figure 1: Differential Amplifier

The small signal differential voltage gain of this circuit is given by

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_L}{r_e}$$

Substituting $r_e = \frac{1}{g_m} = \frac{kT}{qI_E}$

$$V_{OUT} = V_{IN} \frac{R_L}{r_e} = V_{IN} \bullet \frac{qI_E R_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage V_{IN} and the emitter current I_E. In the simple transconductance multiplier of Figure 2, a current source comprising Q_3, D_1, and R_Y is used. If V_Y is large compared with the drop across D_1, then

$$I_D \simeq \frac{V_Y}{R_Y} = 2I_E \text{ and}$$

$$V_{OUT} = \frac{qR_L}{kTR_Y}(V_X \bullet V_Y)$$

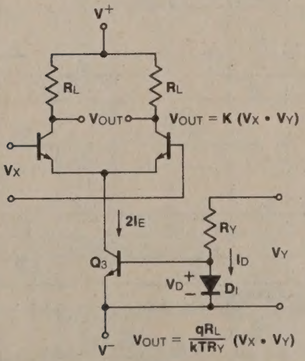


Figure 2: Transconductance Multiplier

There are several difficulties with this simple modulator:

1: V_Y must be positive and greater than V_D

2: Some portion of the signal at V_X will appear at the output unless $I_E = 0$.

3: V_X must be a small signal for the differential pair to be linear.

4: The output voltage is not centered around ground.

The first problem relates to the method of converting the V_Y voltage to a current to vary the gain of the V_X differential pair. A better method, Figure 3, uses another differential pair but with considerable emitter degeneration. In this circuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0 volts to ±10 volts with excellent linearity.

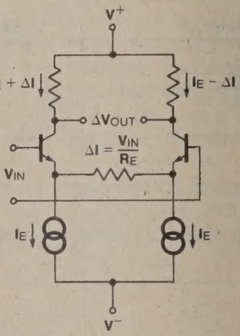


Figure 3: Voltage to Current Converter

The second problem is called feedthrough; i.e. the product of zero and some finite input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 4A, B, and C overcomes this problem and forms the heart of many multiplier circuits in use today.

This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in 4A of exactly equal current sources biasing the two pairs. With a small positive signal at V_{IN}, the collector current of Q_1 and Q_4 will increase but the collector currents of Q_2 and Q_3 will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V_{IN} input voltage.

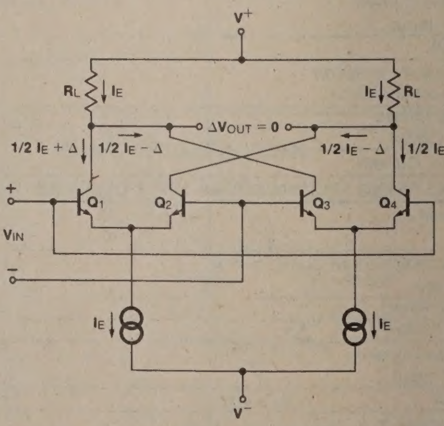


Figure 4A: Input Signal with Balanced Current Sources $\Delta V_{OUT} = 0V$

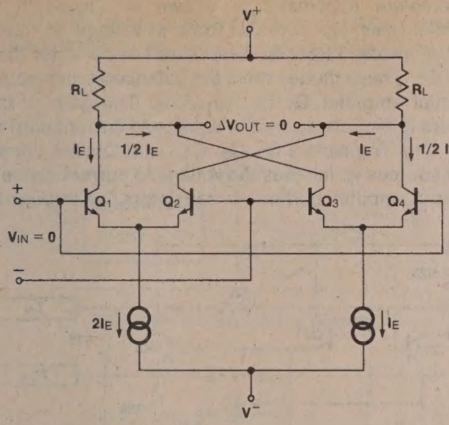

V+
RL
RL
ΔVOUT = 0
IE
1/2 IE
IE
1/2 IE
+
Q1
Q2
Q3
Q4
VIN = 0
−
2IE
IE
V−

Figure 4B: No Input Signal with Unbalanced Current Sources
Δ V_{OUT} = 0V

In Figure 4B, notice that with $V_{IN} = 0$ any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 4C we apply a differential input voltage with unbalanced current sources. If I_{E1} is twice I_{E2}, the gain of differential pair Q_1 and Q_2 is twice the gain of pair Q_3 and Q_4. Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage to current converter of Figure 3 we have a balanced multiplier circuit capable of four quadrant operation (Figure 5).

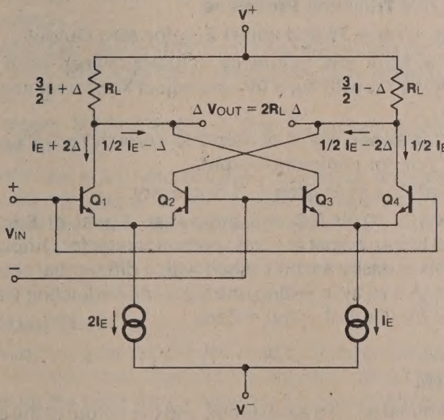

V+
3/2 I + Δ
RL
3/2 I − Δ
RL
Δ VOUT = 2RL Δ
IE + 2Δ
1/2 IE − Δ
1/2 IE − 2Δ
1/2 IE + Δ
+
Q1
Q2
Q3
Q4
VIN
−
2IE
IE
V−

Figure 4C: Input Signal with Unbalanced Current Sources, Differential Output Voltage

This circuit of Fig. 5 still has the problem that the input voltage V_{IN} must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.

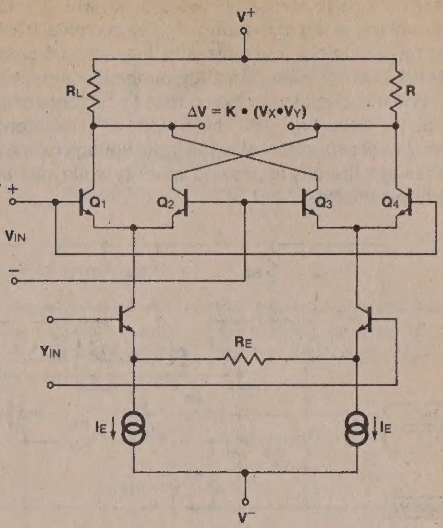

V+
RL
R
ΔV = K • (VX•VY)
+
Q1
Q2
Q3
Q4
VIN
−
YIN
RE
IE
IE
V−

Figure 5: Typical Four Quadrant Multiplier-Modulator

Figure 3 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Fig. 6A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 6A is the

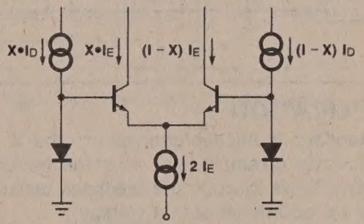

X•ID
X•IE
(I − X) IE
(I − X) ID
2 IE

Figure 6A: Current Gain Cell

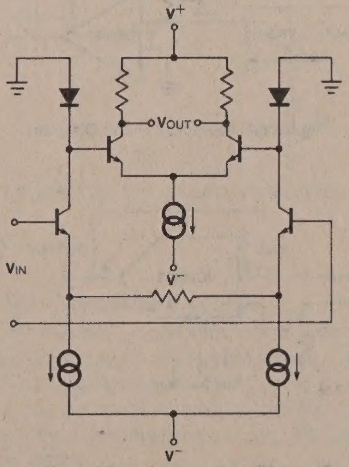
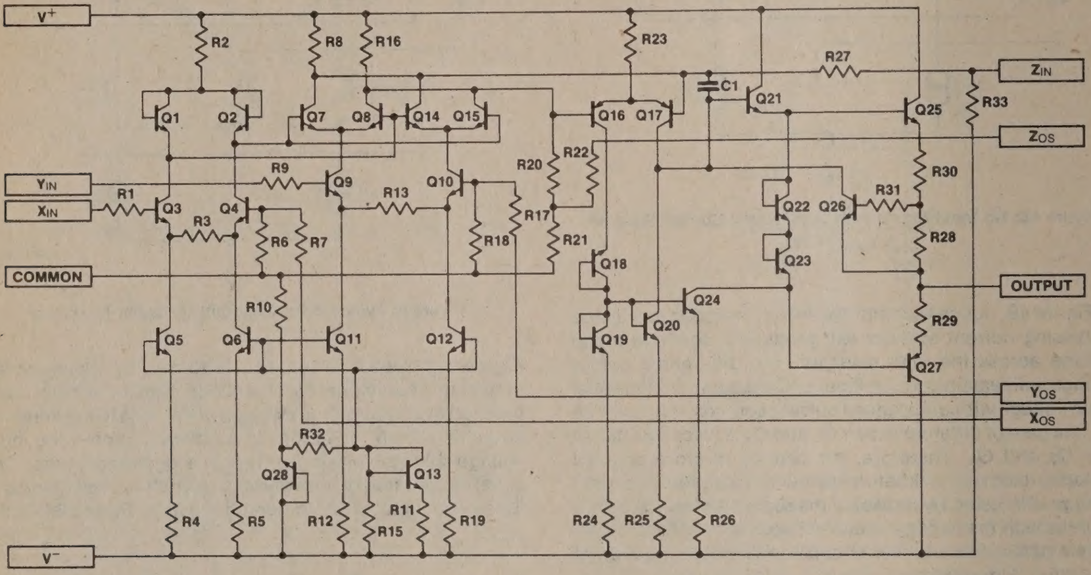

V+
VOUT
VIN
V−
V−

Figure 6B: Voltage Gain with Signal Compression

difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Fig. 3, we have Fig. 6B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

The complete schematic is shown in Figure 7. The differential pair Q_3 and Q_4 form a voltage to current converter whose output is compressed in collector diodes Q_1 and Q_2. These diodes drive the balanced cross-coupled differential amplifier Q_7/Q_8 Q_{14}/Q_{15}. The gain of these amplifiers is modulated by the voltage to current converter Q_9 and Q_{10}. Transistors Q_5, Q_6, Q_{11}, and Q_{12} are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors Q_{16} through Q_{27}.

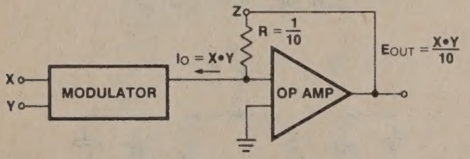


V+
R2
R8
R16
R23
R27
C1
ZIN
Q1
Q2
Q7
Q8
Q14
Q15
Q16
Q17
Q21
Q25
R33
ZOS
R22
R20
R9
Q9
Q10
R30
YIN
XIN
R1
Q3
Q4
R3
R13
R17
Q22
Q26
R31
R6
R7
R18
R21
R28
Q23
COMMON
Q18
OUTPUT
R10
Q24
R29
Q20
Q5
Q6
Q11
Q12
Q19
Q27
YOS
XOS
R32
Q28
Q13
R11
R4
R5
R12
R15
R19
R24
R25
R26
V−

Figure 7: ICL8013 Schematic

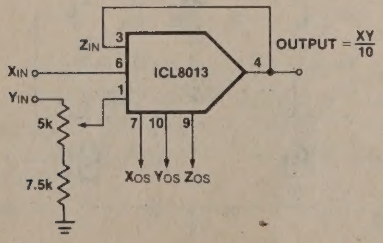
MULTIPLICATION

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R27 and produces a proportional output voltage.



Z
R = 1/10
$I_O = X \bullet Y$
X
Y
MODULATOR
OP AMP
$E_{OUT} = \frac{X \bullet Y}{10}$

Figure 8A: Multiplier Block Diagram



ZIN
3
6
1
XIN
YIN
ICL8013
4
OUTPUT = XY/10
5k
7.5k
7
10
9
XOS YOS ZOS

Figure 8B: Actual Circuit Connection

MULTIPLIER Trimming Procedure

1. Set $X_{IN} = Y_{IN} = 0V$ and adjust Z_{OS} for zero Output.
2. Apply a ±10V low frequency (≤100Hz) sweep (sine or triangle) to Y_{IN} with $X_{IN} = 0V$, and adjust X_{OS} for minimum output.
3. Apply the sweep signal of Step 2 to X_{IN} with $Y_{IN} = 0V$ and adjust Y_{OS} for minimum Output.
4. Readjust Z_{OS} as in Step 1, if necessary.
5. With X_{IN} = 10.0V DC and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output = Y_{IN}. This is easily accomplished with a differential scope plug-in (A + B) by inverting one signal and adjusting Gain control for (Output − Y_{IN}) = Zero.

DIVISION

If the Z terminal is used as an input, and the output of the op-amp connected to the Y input, the device functions as a divider. Since the input to the op-amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

$$\text{Therefore } I_O = X \bullet Y = \frac{Z}{R} = 10Z$$

$$\text{Since } Y = E_{OUT},\ E_{OUT} = \frac{10Z}{X}$$

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.

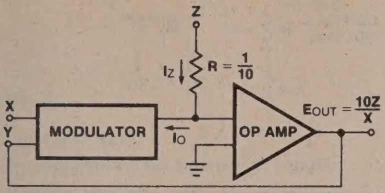

Z
I_Z
$R = \frac{1}{10}$
X
Y
MODULATOR
I_O
OP AMP
$E_{OUT} = \frac{10Z}{X}$

Figure 9A: Division Block Diagram

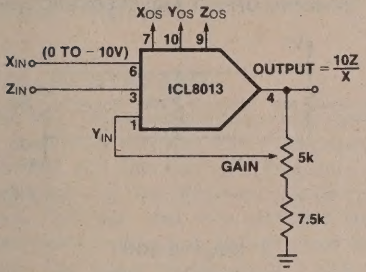

X_{OS} Y_{OS} Z_{OS}
7 10 9
X_{IN} (0 TO − 10V)
Z_{IN}
Y_{IN}
6
3
1
ICL8013
4
OUTPUT = $\frac{10Z}{X}$
GAIN
5k
7.5k

Figure 9B: Actual Circuit Connection

DIVIDER Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_{OS}, Y_{OS}, Z_{OS}) for zero volts.
2. With $Z_{IN} = 0V$, trim Z_{OS} to hold the Output constant, as X_{IN} is varied from −10V through −1V.
3. With $Z_{IN} = 0V$ and $X_{IN} = -10.0V$ adjust Y_{OS} for zero Output voltage.
4. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust X_{OS} for minimum worst-case variation of Output, as X_{IN} is varied from −10V to −1V.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust the gain control until the output is the closest average around +10.0V (−10V for $Z_{IN} = -X_{IN}$) as X_{IN} is varied from −10V to −3V.

SQUARING

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since $\cos^2 \omega = 1/2 (\cos 2\omega + 1)$.

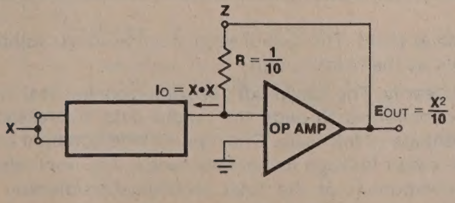

Z
$R = \frac{1}{10}$
$I_O = X \bullet X$
X
OP AMP
$E_{OUT} = \frac{X^2}{10}$

Figure 10A: Squarer Block Diagram

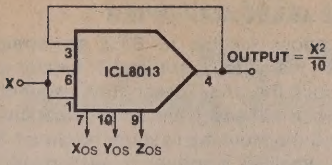

3
6
1
X
ICL8013
4
OUTPUT = $\frac{X^2}{10}$
7 10 9
X_{OS} Y_{OS} Z_{OS}

Figure 10B: Actual Circuit Connection

SQUARE ROOT

Tying the X and Y inputs together and using overall feedback from the Op Amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O = X \bullet Y = (-E_{OUT})^2 = 10Z$$

$$E_{OUT} = -\sqrt{10Z}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the Op Amp output prevents the latchup that would otherwise occur for negative input voltages.

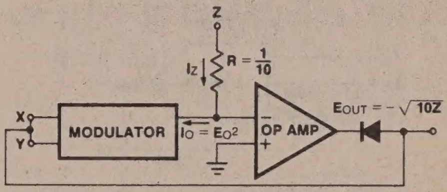

Z
I_Z
$R = \frac{1}{10}$
X
Y
MODULATOR
$I_O = E_O^2$
OP AMP
−
+
$E_{OUT} = -\sqrt{10Z}$

Figure 11A: Square Root Block Diagram

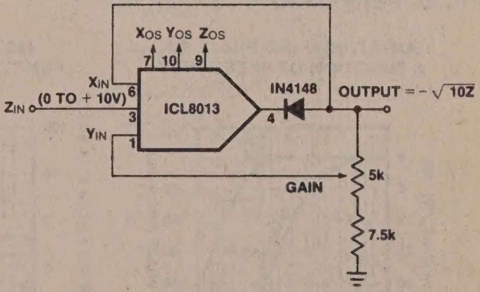

X_{OS} Y_{OS} Z_{OS}
7 10 9
X_{IN}
Z_{IN} (0 TO + 10V)
Y_{IN}
6
3
1
ICL8013
4
IN4148
OUTPUT = $-\sqrt{10Z}$
GAIN
5k
7.5k

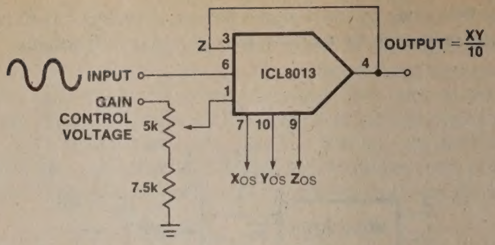
Figure 11B: Actual Circuit Connection

SQUARE ROOT Trimming Procedure

1. Connect the ICL8013 in the *Divider* configuration.
2. Adjust Z_{OS}, Y_{OS}, X_{OS}, and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the Output and inserting a diode between Pin 4 and the Output node.
4. With $Z_{IN} = 0V$ adjust Z_{OS} for zero Output voltage.

VARIABLE GAIN AMPLIFIER

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.

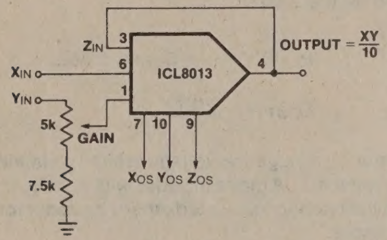


Z
3
6
1
4
ICL8013
OUTPUT = $\frac{XY}{10}$
INPUT
GAIN CONTROL VOLTAGE
5k
7.5k
7
10
9
Xos Yos Zos

Figure 12: Variable Gain Amplifier

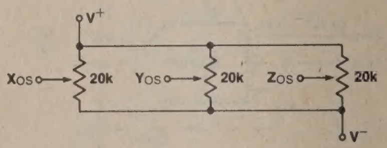
TYPICAL APPLICATIONS

MULTIPLICATION



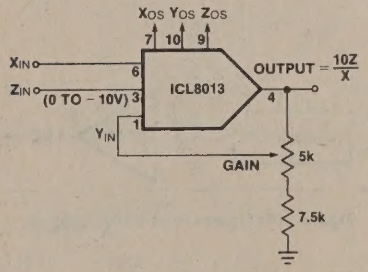
ZIN
3
6
1
4
XIN
YIN
ICL8013
OUTPUT = $\frac{XY}{10}$
5k
GAIN
7.5k
7
10
9
Xos Yos Zos

POTENTIOMETERS FOR TRIMMING OFFSET AND FEEDTHROUGH



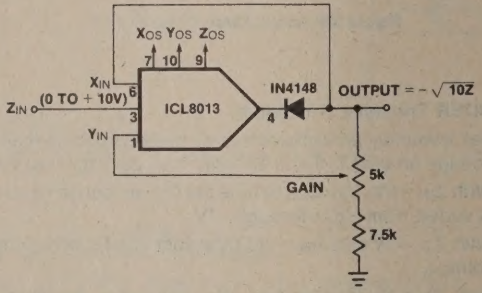
V+
Xos
20k
Yos
20k
Zos
20k
V−

DIVISION



Xos Yos Zos
7
10
9
XIN
6
ZIN
(0 TO − 10V)
3
1
YIN
ICL8013
4
OUTPUT = $\frac{10Z}{X}$
GAIN
5k
7.5k

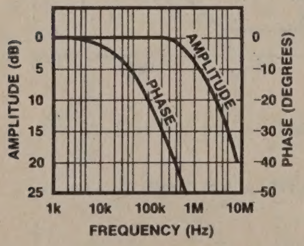
SQUARE ROOT



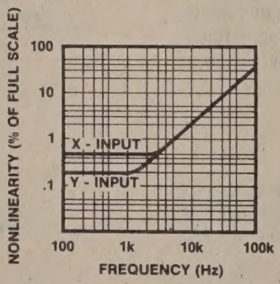
Xos Yos Zos
7
10
9
XIN
(0 TO + 10V)
6
ZIN
3
YIN
1
ICL8013
4
IN4148
OUTPUT = $-\sqrt{10Z}$
GAIN
5k
7.5k

TYPICAL PERFORMANCE CURVES

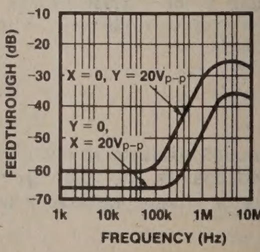
AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY



NONLINEARITY AS A FUNCTION OF FREQUENCY



FEEDTHROUGH AS A FUNCTION OF FREQUENCY



DEFINITION OF TERMS

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

INTERSIL

ICL 8017
High Speed Inverting Amplifier

FEATURES

- 130 V/µs Slew Rate
- Fast Settling Time
- 50 nA Input Current
- 10 MHz Bandwidth
- Simple Frequency Compensation
- Short Circuit Protection

APPLICATIONS

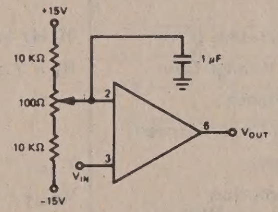
- High Speed Inverting Amplifier
- D/A Converter
- A/D Converter
- Pulse Amplifier
- Active Filter
- Sample and Hold Circuit
- Peak Detector

GENERAL DESCRIPTION

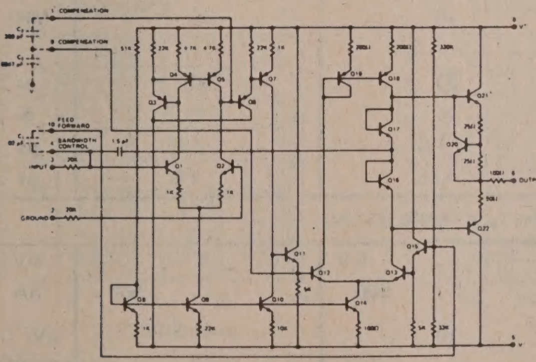
The 8017 integrated circuit is a high speed inverting amplifier combining excellent input characteristics with wide bandwidth and high slew rate. Frequency compensation is achieved with the minimum number of external components. The high slew rate and fast settling time ensure exceptional performance in high speed data acquisition circuits. Full power bandwidth of 2 MHz makes the 8017 amplifier suitable for all applications where large amplitude, high frequency signals are encountered.

The 8017 is available in the military version, 8017M, with a temperature range from −55°C to +125°C and in the commercial version, 8017C, from 0°C to +70°C.

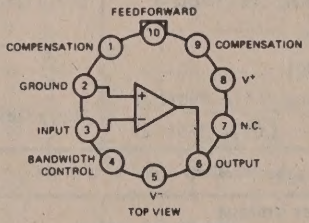
VOLTAGE OFFSET NULL CIRCUIT


+15V
10 KΩ
.1 µF
100Ω
2
6
V_OUT
10 KΩ
3
V_IN
−15V

SCHEMATIC DIAGRAM


1 COMPENSATION
9 COMPENSATION
10 FEED FORWARD
4 BANDWIDTH CONTROL
INPUT
GROUND
OUTPUT
V+
V−

PIN CONFIGURATION


FEEDFORWARD
10
COMPENSATION 1
9 COMPENSATION
8 V+
GROUND 2
INPUT 3
7 N.C.
BANDWIDTH CONTROL 4
6 OUTPUT
5
V−
TOP VIEW

(outline dwg TO-100)

ORDERING INFORMATION

ICL8017 M TW
Package: TW – TO-100 metal can
Temperature Range
M – Military (−55°C to +125°C)
C – Commercial (0°C to 70°C)
Device Chip Type

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Operating Temperature Range	
ICL8017M	$-55^\circ C$ to $+125^\circ C$
ICL8017C	$0^\circ C$ to $+70^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (60 secs)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$)

PARAMETER	CONDITIONS	8017M MIN	8017M TYP	8017M MAX	8017C MIN	8017C TYP	8017C MAX	UNITS
The following specifications apply for $T_A = 25^\circ C$:								
Input Offset Voltage			2.0	5.0		2.0	7.0	mV
Input Current			50	200		50	200	nA
Input Noise Voltage (rms)	10 Hz to 1 MHz		20			20		µV
Large Signal Voltage Gain	$R_L = 2\ k\Omega$	25	1000		25	1000		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current	$V_{OUT} = 0V$		5.0	7.0		5.0	8.0	mA
Power Consumption	$V_{OUT} = 0V$		150	210		150	240	mW
Slew Rate	$R_{BW} = 20\ k\Omega$		130			130		V/µs
Unity Gain Bandwidth (Note 3)	$R_{BW} = 20\ k\Omega$		10			10		MHz
Transient Response (Note 3)	Unity Gain, $R_{BW} = 20\ k\Omega$							
Risetime			30			30		ns
Overshoot			5			5		%
Settling Time (0.1%) (Note 3)	Unity Gain, $R_{BW} = 20\ k\Omega$		1.0			1.0		µs
(.01%) (Note 3)			3.5			3.5		µs
The following specifications apply for $0^\circ C \leq T_A \leq +70^\circ C$ (8017C), $-55^\circ C \leq T_A \leq +125^\circ C$ (8017M):								
Input Offset Voltage				6.0			7.5	mV
Input Current				500			500	nA
Average Temperature Coefficient of Input Offset Voltage	$-55^\circ C \leq T_A \leq +125^\circ C$ $0^\circ C \leq T_A \leq +70^\circ C$		10			10		µV/°C µV/°C
Large Signal Voltage Gain		15			15			V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$	±10			±10			V
Supply Voltage Rejection Ratio				300			300	µV/V
Supply Current	$V_{OUT} = 0V$			9.0			9.0	mA

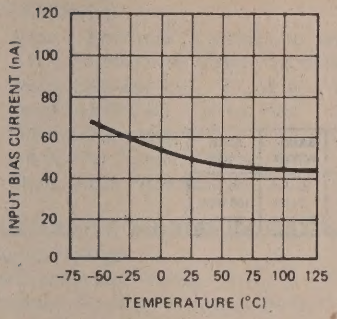
NOTE 1: The maximum junction temperature of the 8017M is 150°C, while that of the 8017C is 100°C. For operating at elevated temperatures the package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. Above 100°C it may be necessary to use a heatsink with the 8017M to avoid exceeding the maximum chip temperature.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

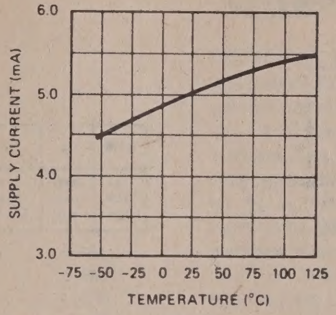
NOTE 3: Circuit and compensation as in Figure 1.

TYPICAL PERFORMANCE CURVES*

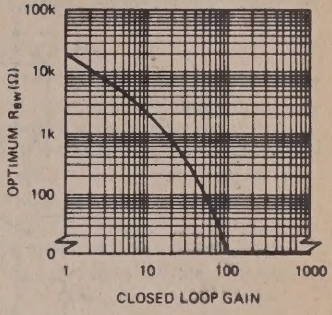
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



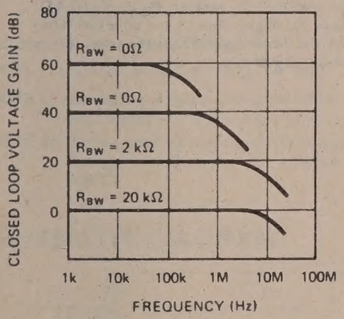
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



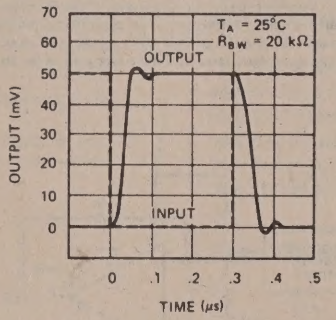
OPTIMUM VALUE OF R_{BW} AS A FUNCTION OF CLOSED LOOP GAIN (SEE FIG. 1)



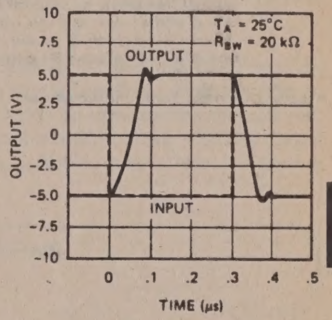
FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



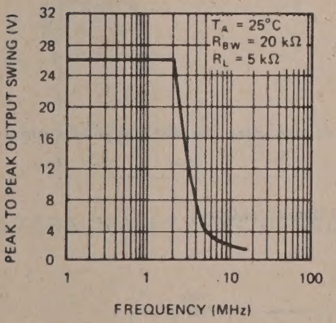
UNITY GAIN TRANSIENT RESPONSE



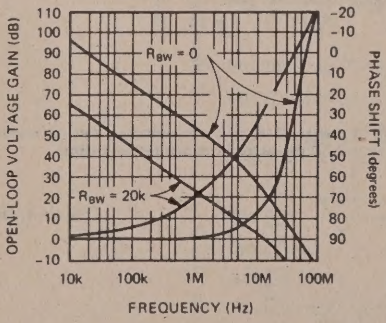
UNITY GAIN LARGE SIGNAL PULSE RESPONSE



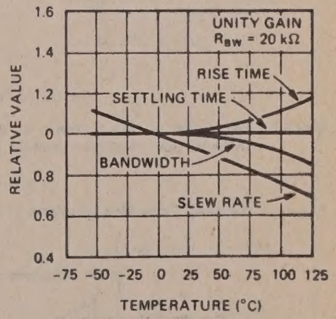
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



OPEN-LOOP FREQUENCY RESPONSE



FREQUENCY CHARACTERISTICS AS A FUNCTION OF TEMPERATURE



*8017C only guaranteed for $0^\circ C \leq T_A \leq +70^\circ C$

DEFINITION OF TERMS

Input Offset Voltage: Voltage which must be applied to input terminal to obtain zero output voltage.

Input Current: Current into input terminal when at ground potential.

Large Signal Voltage Gain: The ratio of maximum output swing with load to the required change in input drive voltage.

Slew Rate: The maximum rate of change of output voltage in response to a large amplitude input pulse.

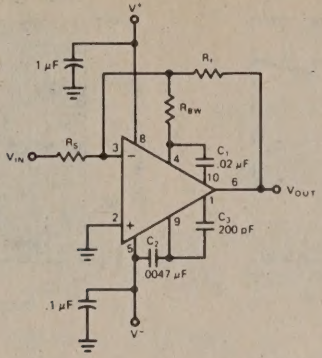
Unity Gain Bandwidth: The frequency at which the small signal gain is 3 dB below its low frequency value.

Transient Response: The 10% to 90% closed loop step-function response of the amplifier under small signal conditions.

Settling Time: The elapsed time between the application of a fast input pulse and the time at which the output has settled to its final value within a specified limit of accuracy.

APPLICATIONS INFORMATION

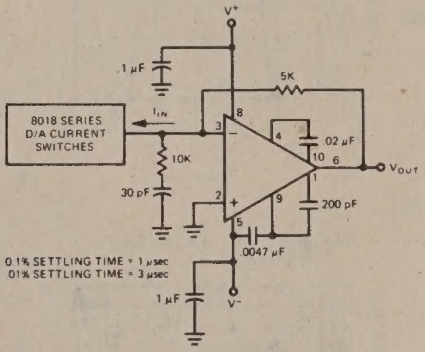
Figure 1. Inverting Voltage Amplifier


V+
1 µF
Rf
RBW
RS
VIN
3
8
4
C1
.02 µF
10
6
VOUT
1
2
9
C3
200 pF
5
C2
0047 µF
.1 µF
V-

GAIN	R_S	R_f	R_{BW}	BAND-WIDTH	SLEW RATE
1X	10 kΩ	10 kΩ	20 kΩ	10 MHz	130 V/µs
10X	10 kΩ	100 kΩ	2 kΩ	6 MHz	100 V/µs
100X	1 kΩ	100 kΩ	short	800 kHz	50 V/µs

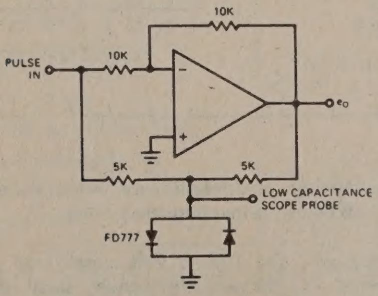
NOTE: If no bandwidth control resistor (R_{BW}) is connected between pins 3 and 4, the amplifier is unconditionally stable for normal feedback configurations. Some improvement in frequency performance can be realized by setting R_{BW} = 20 kΩ; the amplifier will still be unconditionally stable. However, for optimum frequency response, R_{BW} should be selected from the curve on page 3, based on the closed loop gain of the circuit. Additional control of the bandwidth/stability trade-off is possible by bypassing R_f with a low value capacitor. It is not necessary to alter the value of C_1, C_2 or C_3.

Figure 2. Current Summing Amplifier


V+
.1 µF
5K
IIN
8018 SERIES
D/A CURRENT
SWITCHES
3
8
4
.02 µF
10
6
VOUT
10K
1
30 pF
2
9
200 pF
5
.0047 µF
0.1% SETTLING TIME = 1 µsec
01% SETTLING TIME = 3 µsec
1 µF
V-

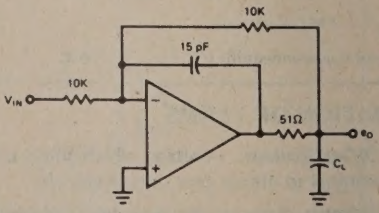
NOTE: The analog output current of thé 8018 Series D/A current switches can be converted to voltage using the 8017 as shown. Input compensation of approximately 10 kΩ and 30 pF helps improve settling time.

Figure 3. Settling Time Measurement


10K
PULSE IN
10K
eO
5K
5K
LOW CAPACITANCE SCOPE PROBE
FD777

NOTE: Settling time is measured by creating a dummy summing junction and observing the error voltage waveform on a scope. The junction is clamped with high speed diodes to avoid overdriving the scope preamp.

Figure 4. Isolation of Capacitive Loads


10K
15 pF
10K
VIN
51Ω
eO
CL

NOTE: Excess phase shift caused by heavy capacitive loading (above 200 to 300 pF) can cause stability problems. By providing the amplifier with a minimum real load impedance (51Ω), these difficulties can be overcome. Note that at high output currents, maximum voltage swing will be reduced.

INTERSIL

ICL8021—ICL8023 Low Power Operational Amplifiers

FEATURES

- ΔV_{os} = 3 mV max (adjustable to zero).
- ±1V to ±18V Power Supply Operation.
- Power Consumption – 20 µW @ ± 1V.
- Input Bias Current – 30 nA max.
- Internal Compensation.
- Pin-For-Pin Compatible With 741.
- Short Circuit Protected.

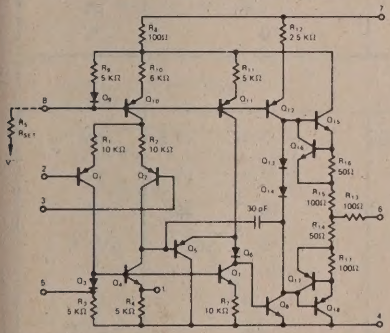
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±15V
Common Mode Input Voltage (Note 1)	±15V
Output Short Circuit Duration	Indefinite
Power Dissipation (Note 2)	300 mW
Operating Temperature Range	
8021M	−55°C to +125°C
8021C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

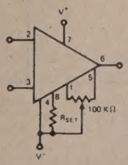
NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

SCHEMATIC DIAGRAM


7
R_8 100Ω
R_{12} 2.5 KΩ
R_9 5 KΩ
R_{10} 6 KΩ
R_{11} 5 KΩ
8
Q_9
Q_{10}
Q_{11}
Q_{12}
Q_{15}
R_5 R_{SET}
V⁻
R_1 10 KΩ
R_2 10 KΩ
Q_{16}
2
Q_1
Q_2
Q_{13}
R_{16} 50Ω
3
Q_{14}
R_{15} 100Ω
R_{13} 100Ω
6
30 pF
R_{14} 50Ω
Q_5
Q_6
R_{17} 100Ω
5
Q_3
Q_4
1
Q_7
Q_{17}
R_3 5 KΩ
R_4 5 KΩ
R_7 10 KΩ
Q_8
Q_{18}
4

VOLTAGE OFFSET NULL CIRCUIT


V⁺
2
7
6
3
5
4
8
100 KΩ
R_{SET}
V⁻

ORDERING INFORMATION

ICL8021 C TY

Basic
Part Number
8021—Single
8022—Dual
8023—Triple

Package
TV— TO-99 Metal Can
PA—8 pin Minidip **8021 only**

JD— 14 pin CERDIP
PD— 14 pin Plastic DIP **8022 only**

JE— 16 pin CERDIP
PE— 16 pin Plastic DIP **8023 only**

Temperature
C— Commercial — 0°C to 70°C
M— Military −55°C to +125°C

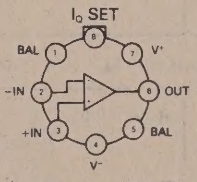
GENERAL DESCRIPTION

The Intersil 8021 integrated circuit is a low power operational amplifier specifically designed for applications requiring very low standby power consumption over a wide range of supply voltages. The electrical characteristics of the 8021 can be tailored to a particular application by adjusting an external resistor, R_{SET}, which controls the quiescent current. This is advantageous because I_Q can be made independent of the supply voltages: it can be set to an extremely low value where power is critical, or to a larger value for high slew rate or wideband applications.

Other features of the 8021 include low input current that remains constant with temperature, low noise, high input impedance, internal compensation and pin-for-pin compatibility with the 741.

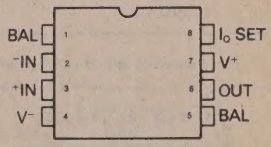
The Intersil 8022 (8023) consists of two (three) low power operational amplifiers in a single 14-pin DIP. Each amplifier is identical to an 8021 low power op amp, and has separate connections for adjusting its electrical characteristics by means of an external resistor, R_{SET}, which controls the quiescent current of that amplifier.

PIN CONFIGURATIONS

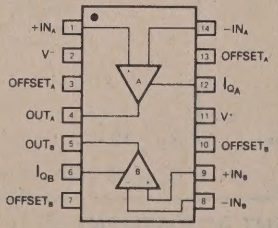

I_Q SET
8
BAL
1
7
V⁺
−IN
2
6
OUT
+IN
3
5
BAL
4
V⁻

(outline dwg TO-99)

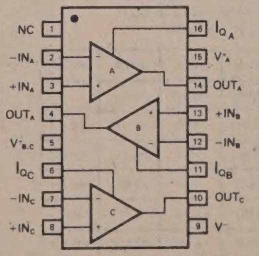
NOTE: Pin 4 connected to case.


BAL 1
−IN 2
+IN 3
V⁻ 4
8 I_Q SET
7 V⁺
6 OUT
5 BAL

(outline dwg PA)


$+IN_A$ 1
V⁻ 2
$OFFSET_A$ 3
OUT_A 4
OUT_B 5
I_{QB} 6
$OFFSET_B$ 7
A
B
14 $-IN_A$
13 $OFFSET_A$
12 I_{QA}
11 V⁺
10 $OFFSET_B$
9 $+IN_B$
8 $-IN_B$

(outline dwg JD, PD)


NC 1
$-IN_A$ 2
$+IN_A$ 3
OUT_A 4
$V^-_{B,C}$ 5
I_{QC} 6
$-IN_C$ 7
$+IN_C$ 8
A
B
C
16 I_{QA}
15 V^+_A
14 OUT_A
13 $+IN_B$
12 $-IN_B$
11 I_{QB}
10 OUT_C
9 V⁻

(outline dwg JE, PE)

ELECTRICAL CHARACTERISTICS (V_S = ±6V, I_Q = 30 μA, unless otherwise specified.)

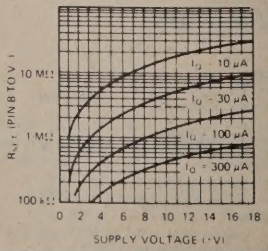
CHARACTERISTICS	CONDITIONS	8021M MIN	8021M TYP	8021M MAX	8021C MIN	8021C TYP	8021C MAX	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 100\ k\Omega$		2	3		2	6	mV
Input Offset Current			.5	7.5		.7	10	nA
Input Bias Current			5	20		7	30	nA
Input Resistance		3	10		3	10		MΩ
Input Voltage Range	V_S = ±15V	±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	80		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Output Resistance	Open Loop		2			2		kΩ
Output Voltage Swing	$R_L \geq 20\ k\Omega$, V_S = ±15V	±12	±14		±12	±14		V
	$R_L \geq 10\ k\Omega$, V_S = ±15V	±11	±13		±11	±13		V
Output Short-Circuit Current			±13			±13		mA
Power Consumption	V_{OUT} = 0		360	480		360	600	μW
Slew Rate (Unity Gain)			0.16			0.16		V/μs
Unity Gain Bandwidth	R_L = 20 kΩ, V_{IN} = 20 mV		270			270		kHz
Transient Response (Unity Gain)	R_L = 20 kΩ, V_{IN} = 20 mV							
Risetime			1.3			1.3		μs
Overshoot			10			10		%
The following specifications apply for 0 C < T_A < +70 C (8021C) −55 C < +125 C (8021M)								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2.0	4.0		2.0	7.5	mV
Input Offset Current			1.0	5		1.5	15	nA
Input Bias Current			10	15		15	50	nA
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 10\ k\Omega$		5			5		μV/°C
Average Temperature Coefficient of Input Offset Current			1.7			0.8		pA/°C
Large Signal Voltage Gain	R_L = 10 kΩ	50	200		50	200		V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±10	±13		±10	±13		V

QUIESCENT CURRENT ADJUSTMENT

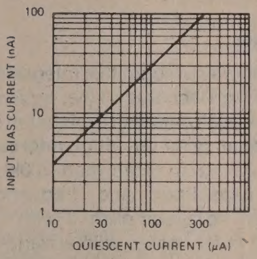
QUIESCENT CURRENT SETTING RESISTOR (PIN 8 TO V^-)

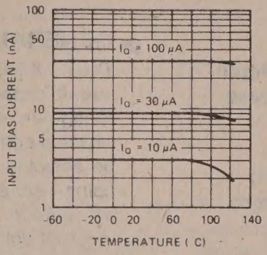
V_S \ I_Q	10 μA	30 μA	100 μA	300 μA
±1.5	1.5 MΩ	470 kΩ	150 kΩ	
± 3	3.3 MΩ	1.1 MΩ	330 kΩ	100 kΩ
± 6	7.5 MΩ	2.7 MΩ	750 kΩ	220 kΩ
± 9	13 MΩ	4 MΩ	1.3 MΩ	350 kΩ
± 12	18 MΩ	5.6 MΩ	1.5 MΩ	510 kΩ
± 15	22 MΩ	7.5 MΩ	2.2 MΩ	620 kΩ

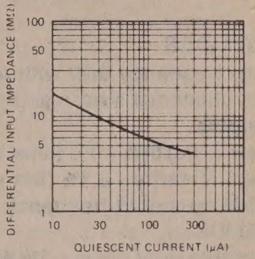
QUIESCENT CURRENT SETTING RESISTOR (PIN 8 TO V^-)

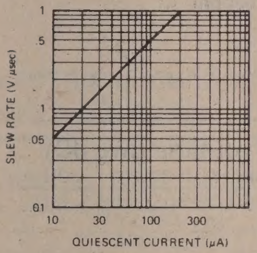


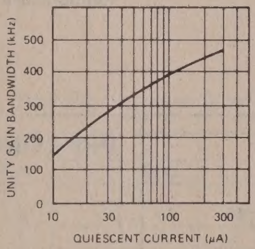
TYPICAL PERFORMANCE CURVES* (T_A = +25°C, V_S = ±6V, I_Q = 30 µA, unless otherwise specified.)

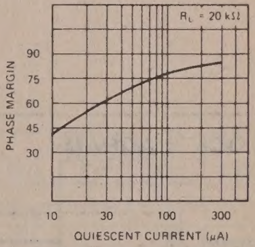

INPUT BIAS CURRENT VS QUIESCENT CURRENT

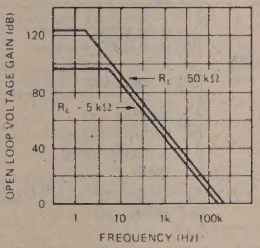

INPUT BIAS CURRENT VS AMBIENT TEMPERATURE

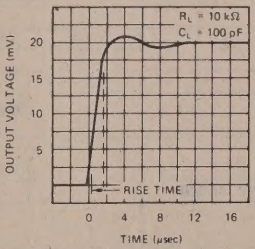

DIFFERENTIAL INPUT IMPEDANCE VS QUIESCENT CURRENT

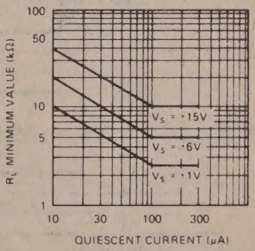

SLEW RATE VS QUIESCENT CURRENT

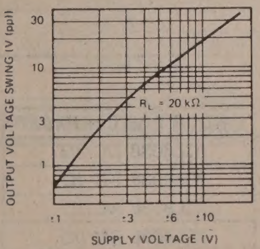

FREQUENCY RESPONSE VS QUIESCENT CURRENT

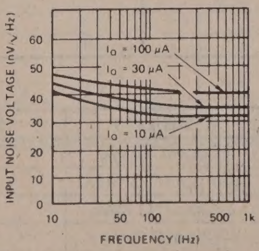

PHASE MARGIN VS QUIESCENT CURRENT

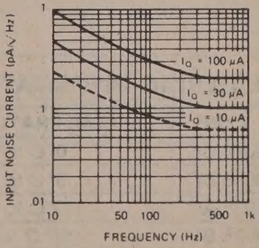

OPEN-LOOP FREQUENCY RESPONSE


TRANSIENT RESPONSE


MAXIMUM LOAD VS QUIESCENT CURRENT


OUTPUT VOLTAGE SWING VS SUPPLY VOLTAGE


EQUIVALENT INPUT NOISE VOLTAGE VS FREQUENCY


EQUIVALENT INPUT NOISE CURRENT VS FREQUENCY

*ICL8021C guaranteed only for 0°C ≤ T_A ≤ +70°C

INTERSIL

ICL8038
Precision Waveform Generator/Voltage Controlled Oscillator

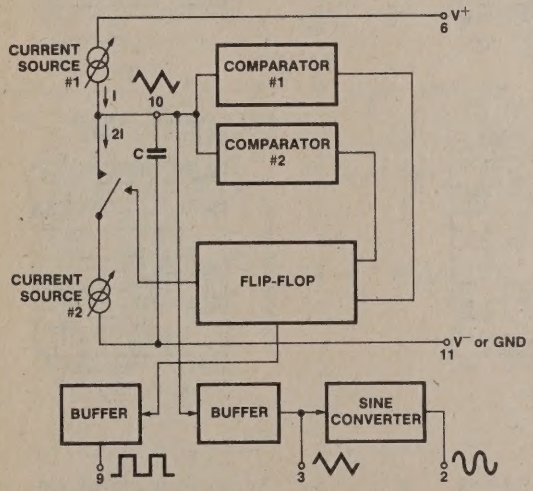
FEATURES

- **Low frequency drift with temperature - 50ppm/°C**
- **Simultaneous sine, square, and triangle wave outputs**
- **Low distortion - 1% (sine wave output)**
- **High linearity - 0.1% (triangle wave output)**
- **Wide operating frequency range - 0.001Hz to 0.3MHz**
- **Variable duty cycle - 2% to 98%**
- **High level outputs - TTL to 28V**
- **Easy to use - just a handful of external components required**

GENERAL DESCRIPTION

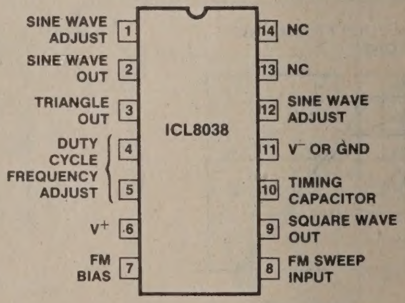
The ICL8038 Waveform Generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 50ppm/°C.

BLOCK DIAGRAM



V+
6
CURRENT SOURCE #1
COMPARATOR #1
I
10
2I
C
COMPARATOR #2
CURRENT SOURCE #2
FLIP-FLOP
V− or GND
11
BUFFER
BUFFER
SINE CONVERTER
9
3
2

PIN CONFIGURATION (outline dwg JD)



SINE WAVE ADJUST 1
SINE WAVE OUT 2
TRIANGLE OUT 3
DUTY CYCLE FREQUENCY ADJUST 4
5
V+ 6
FM BIAS 7
ICL8038
14 NC
13 NC
12 SINE WAVE ADJUST
11 V− OR GND
10 TIMING CAPACITOR
9 SQUARE WAVE OUT
8 FM SWEEP INPUT

ORDERING INFORMATION

TYPE	TEMPERATURE RANGE	STABILITY	PACKAGE	ORDER PART NUMBER
8038 CC	0°C to +70°C	50ppm/°C typ	CERDIP	ICL8038 CC JD
8038 BC	0°C to +70°C	100 ppm/°C max	CERDIP	ICL8038 BC JD
8038 AC	0°C to +70°C	50ppm/°C max	CERDIP	ICL8038 AC JD
8038 BM	−55°C to +125°C	100ppm/°C max	CERDIP	ICL8038 BM JD
8038 AM	−55°C to +125°C	50ppm/°C max	CERDIP	ICL8038 AM JD

MAXIMUM RATINGS

Supply Voltage	±18V or 36V Total
Power Dissipation(1)	750mW
Input Voltage (any pin)	Not To Exceed Supply Voltages
Input Current (Pins 4 and 5)	25mA
Output Sink Current (Pins 3 and 9)	25mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range:	
8038AM, 8038BM	−55°C to +125°C
8038AC, 8038BC, 8038CC	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C.

ELECTRICAL CHARACTERISTICS

(V_{SUPP} = ±10V or +20V, T_A = 25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified)

SYMBOL	GENERAL CHARACTERISTICS	8038CC			8038BC/BM			8038AC/AM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{SUPP}	Supply Voltage Operating Range										
V^+	Single Supply	+10		+30	+10		30	+10		30	V
V^+, V^-	Dual Supplies	±5		±15	±5		±15	±5		±15	V
I_{SUPP}	Supply Current (V_{SUPP} = ±10V)(2)										
	8038AM, 8038BM					12	15		12	15	mA
	8038AC, 8038BC, 8038CC		12	20		12	20		12	20	mA
FREQUENCY CHARACTERISTICS (all waveforms)											
f_{max}	Maximum Frequency of Oscillation	100,000			100,000			100,000			Hz
f_{sweep}	Sweep Frequency of FM		10			10			10		kHz
	Sweep FM Range(3)		40:1			40:1			40:1		
	FM Linearity 10:1 Ratio		0.5			0.2			0.2		%
$\Delta f/\Delta T$	Frequency Drift With Temperature(5)		50			50	100		20	50	ppm/°C
$\Delta f/\Delta V$	Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05			0.05			0.05		%/V_{SUPP}
	Recommended Programming Resistors (R_A and R_B)	1000		1M	1000		1M	1000		1M	Ω
OUTPUT CHARACTERISTICS											
	Square-Wave										
I_{OLK}	Leakage Current (V_9 = 30V)			1			1			1	μA
V_{SAT}	Saturation Voltage (I_{SINK} = 2mA)		0.2	0.5		0.2	0.4		0.2	0.4	V
t_r	Rise Time (R_L = 4.7kΩ)		100			100			100		ns
t_f	Fall Time (R_L = 4.7kΩ)		40			40			40		ns
	Duty Cycle Adjust	2		98	2		98	2		98	%
	Triangle/Sawtooth/Ramp										
	Amplitude (R_{TRI} = 100kΩ)	0.30	0.33		0.30	0.33		0.30	0.33		xV_{SUPP}
	Linearity		0.1			0.05			0.05		%
Z_{OUT}	Output Impedance (I_{OUT} = 5mA)		200			200			200		Ω
	Sine-Wave										
	Amplitude (R_{SINE} = 100kΩ)	0.2	0.22		0.2	0.22		0.2	0.22		xV_{SUPP}
	THD (R_S = 1MΩ)(4)		0.8	5		0.7	3		0.7	1.5	%
	THD Adjusted (Use Fig. 8b)		0.5			0.5			0.5		%

NOTE 2: R_A and R_B currents not included.
NOTE 3: V_{SUPP} = 20V; R_A and R_B = 10kΩ, f ≅ 9kHz; Can be extended to 1000.1. See Figures 13 and 14.
NOTE 4: 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B.)
NOTE 5: Over operating temperature range, Fig. 2, pins 7 and 8 connected, V_{SUPP} = ±10V. See Fig. 6c for T.C. vs V_{SUPP}.

TEST CONDITIONS

PARAMETER	R_A	R_B	R_L	C_1	SW_1	MEASURE
Supply Current	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current into Pin 6
Maximum Frequency of Oscillation	1kΩ	1kΩ	4.7kΩ	100pf	Closed	Frequency at Pin 9
Sweep FM Range(1)	10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Frequency Drift with Supply Voltage(2)	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude: Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 2
Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 3
Leakage Current (off)(3)	10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
Saturation Voltage (on)(3)	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Output (low) at Pin 9
Rise and Fall Times	10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust: MAX	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
MIN	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

NOTE 1: The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{hi}) and then connecting pin 8 to pin 6 (f_{lo}). Otherwise apply Sweep Voltage at pin 8 $(2/3\ V_{SUPP}\ +2V) \leq V_{SWEEP} \leq V_{SUPP}$ where V_{SUPP} is the total supply voltage. In Fig. 2, pin 8 should vary between 5.3V and 10V with respect to ground.

NOTE 2: $10V \leq V^+ \leq 30V$, or $\pm 5V \leq V_{SUPP} \leq \pm 15V$.

NOTE 3: Oscillation can be halted by forcing pin 10 to +5 volts or −5 volts.

DEFINITION OF TERMS:

Supply Voltage (V_{SUPP}). The total supply voltage from V^+ to V^-.

Supply Current. The supply current required from the power supply to operate the device, excluding load currents and the currents through R_A and R_B.

Frequency Range. The frequency range at the square wave output through which circuit operation is guaranteed.

Sweep FM Range. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range

$$(2/3\ V_{SUPP} + 2V) < V_{SWEEP} < V_{SUPP}$$

FM Linearity. The percentage deviation from the best-fit straight line on the control voltage versus output frequency curve.

Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs.

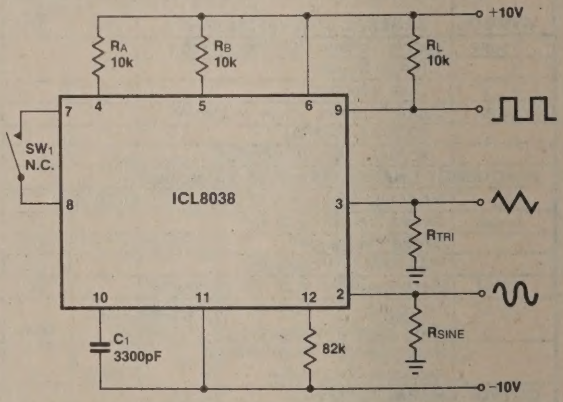
Saturation Voltage. The output voltage at the collector of Q_{23} when this transistor is turned on. It is measured for a sink current of 2mA.

Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

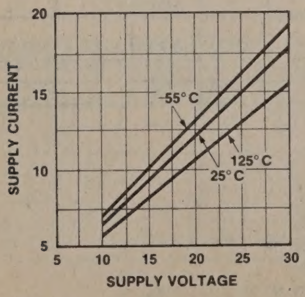
Triangle Waveform Linearity. The percentage deviation from the best-fit straight line on the rising and falling triangle waveform.

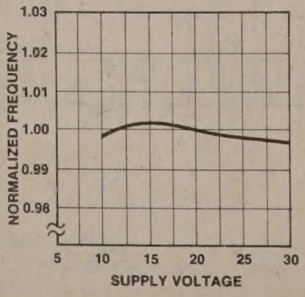
Total Harmonic Distortion. The total harmonic distortion at the sine-wave output.

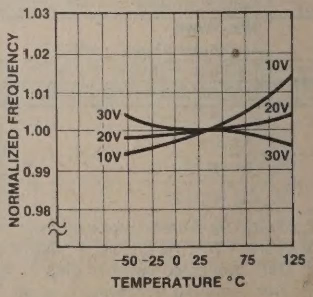
TEST CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTICS







THEORY OF OPERATION (see block diagram, first page)

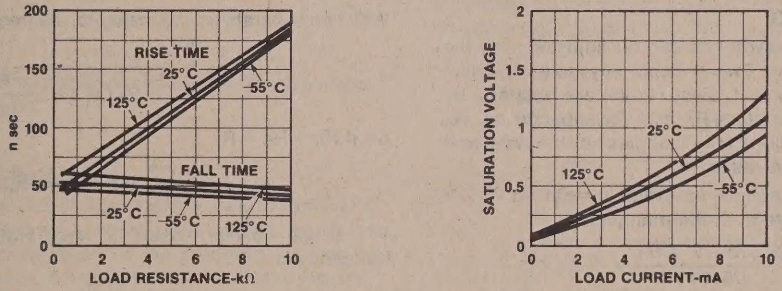
An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearily with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square-wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

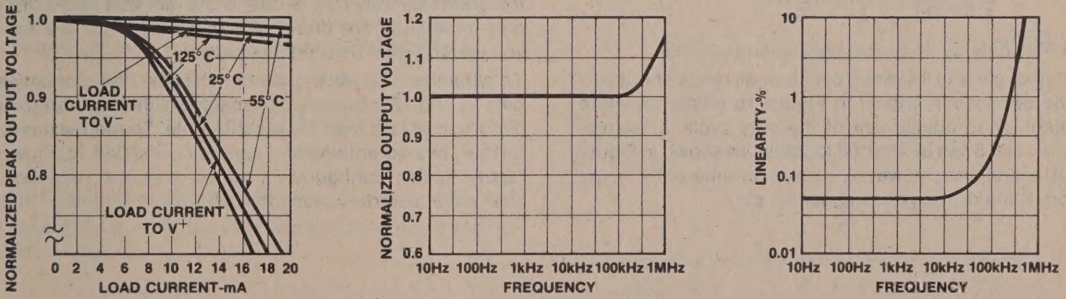
The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

The sine-wave is created by feeding the triangle-wave into a non-linear network (sine-converter). This network provides a decreasing shunt-impedance as the potential of the triangle moves toward the two extremes.

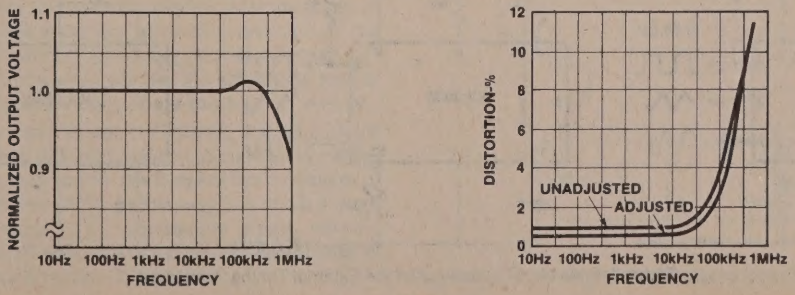
Performance of the Square-Wave Output

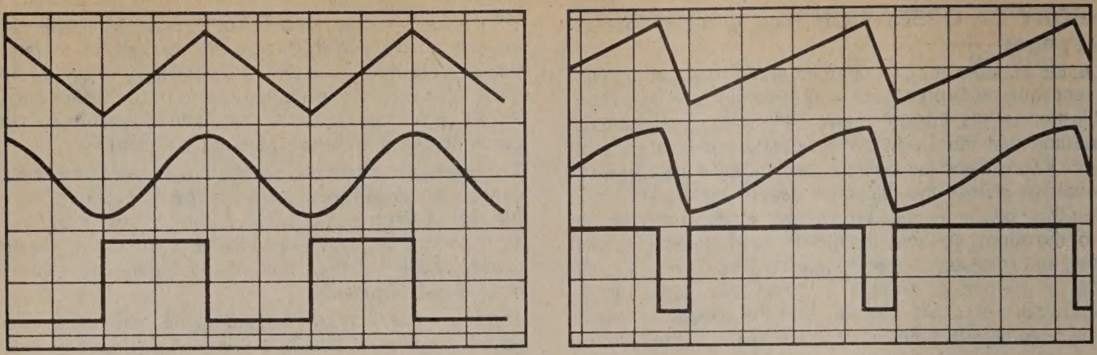


Performance of Triangle-Wave Output



Performance of Sine-Wave Output





Square-Wave Duty Cycle — 50%

Square-Wave Duty Cycle — 80%

Phase Relationship of Waveforms

WAVEFORM TIMING

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 1. Best results are obtained by keeping the timing resistors R_A and R_B separate (a). R_A controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at 1/3 V_{SUPP}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V^+ \times R_A}{1/5 \times V^+} = \frac{5}{3} R_A \times C$$

The falling portion of the triangle and sine-wave and the 0 state of the square-wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times 1/3\, V^+}{\frac{2}{5} \times \frac{V_{SUPP}}{R_B} - \frac{1}{5} \times \frac{V_{SUPP}}{R_A}} = \frac{5}{3} \times \frac{R_A R_B C}{2 R_A - R_B}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 1b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorted together, as shown in Figure 1c. This connection, however, causes an inherently larger variation of the duty-cycle, frequency, etc.

With two separate timing resistors, the frequency is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{5}{3} R_A C \left(1 + \frac{R_B}{2 R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = \frac{0.3}{RC} \text{ (for Figure 1a)}$$

If a single timing resistor is used (Figure 1c only), the frequency is

$$f = \frac{0.15}{RC}$$

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents *and* thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

To minimize *sine-wave* distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 2; this configuration allows a typical reduction of sine-wave distortion close to 0.5%.

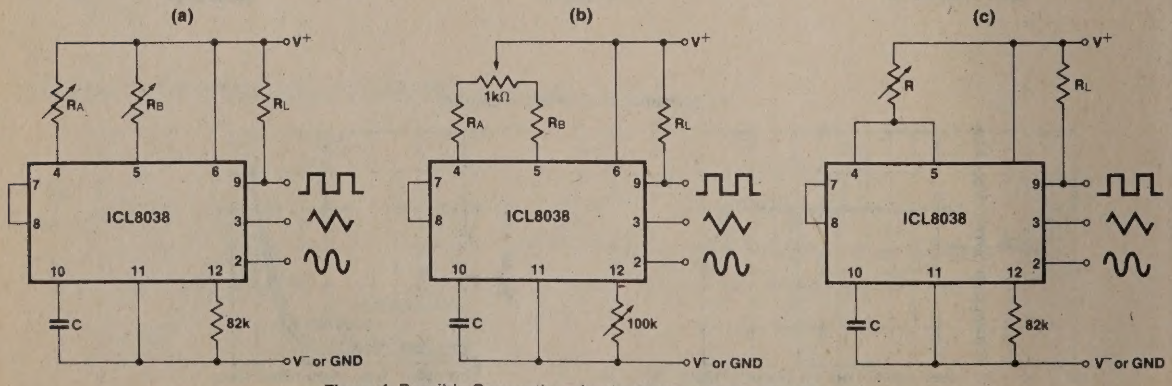


Figure 1: Possible Connections for the External Timing Resistors.

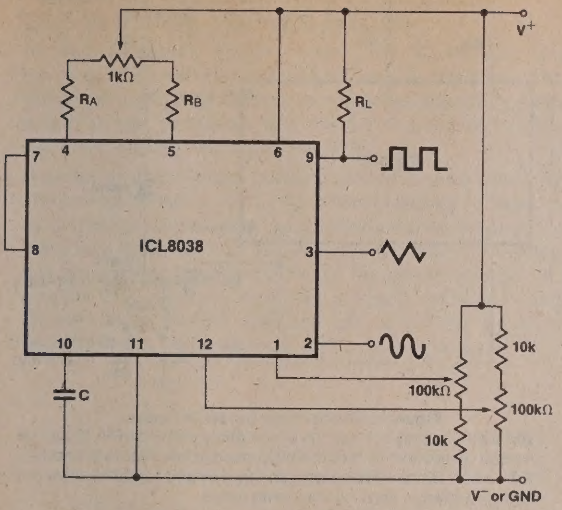


Figure 2: Connection to Achieve Minimum Sine-Wave Distortion.

SELECTING R_A, R_B AND C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents ($I > 5mA$), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times V_{SUPP}}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{V_{SUPP}}{5R_A}$$

A similar calculation holds for R_B.

The capacitor value should be chosen at the upper end of its possible range.

WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between V^+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output can be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.

FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from V^+). By altering this voltage, frequency modulation is performed.

For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 3a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 3b). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created ($f = 0$ at $V_{sweep} = 0$). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V^+ by ($1/3\ V_{SUPP} - 2V$).

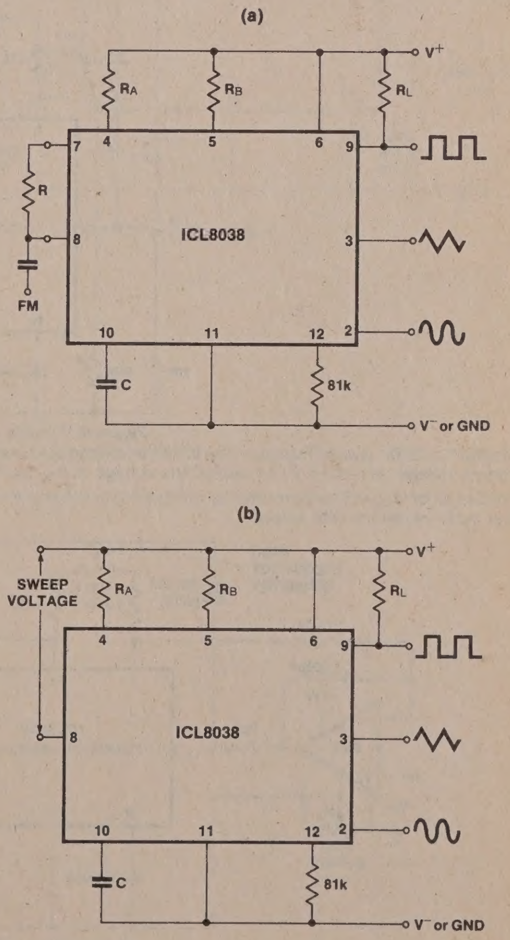


Figure 3: Connections for Frequency Modulation (a) and Sweep (b)

APPLICATIONS

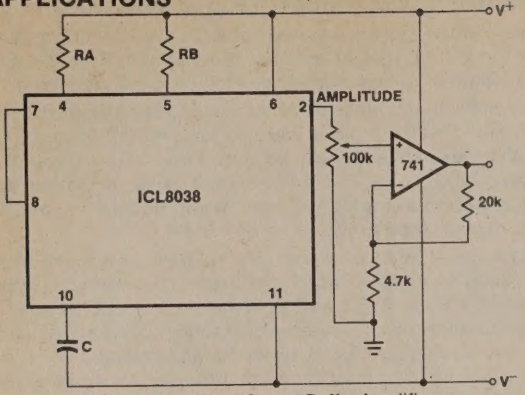

V+
RA
RB
7
4
5
6
2
AMPLITUDE
100k
741
20k
8
ICL8038
4.7k
10
11
C
V−

Figure 4: Sine Wave Output Buffer Amplifiers.

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 4 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

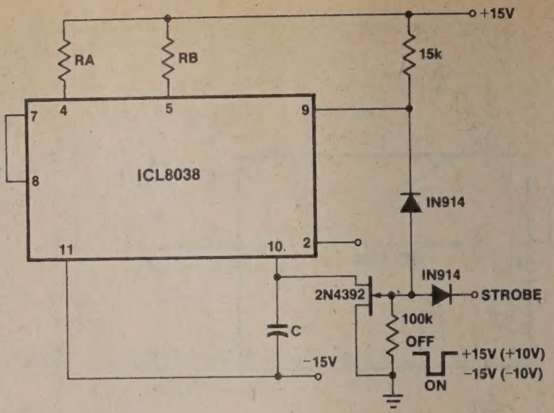

+15V
RA
RB
15k
7
4
5
9
8
ICL8038
IN914
11
10
2
IN914
2N4392
STROBE
100k
C
OFF
−15V
+15V (+10V)
−15V (−10V)
ON

Figure 5: Strobe-Tone Burst Generator.

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the 8038 oscillation. Figure 5 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

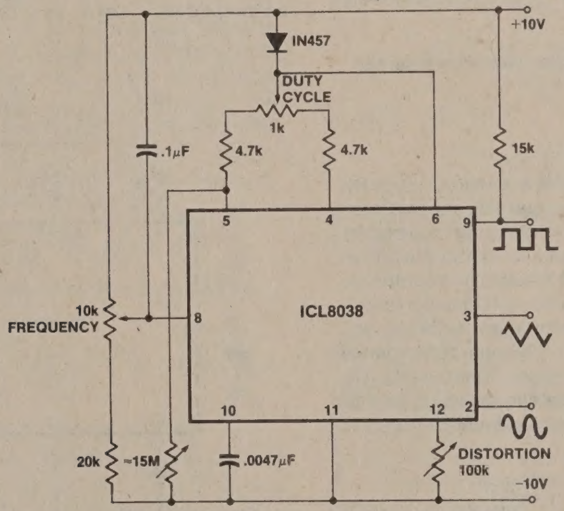

IN457
+10V
DUTY CYCLE
1k
.1μF
4.7k
4.7k
15k
5
4
6
9
10k FREQUENCY
8
ICL8038
3
10
11
12
2
20k
≈15M
.0047μF
DISTORTION 100k
−10V

Figure 6: Variable Audio Oscillator, 20Hz to 20kHz.

To obtain a 1000:1 Sweep Range on the 8038 the voltage across external resistors R_A and R_B must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of R_A and R_B by a few hundred millivolts.

The Circuit of Figure 6 achieves this by using a diode to lower the effective supply voltage on the 8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

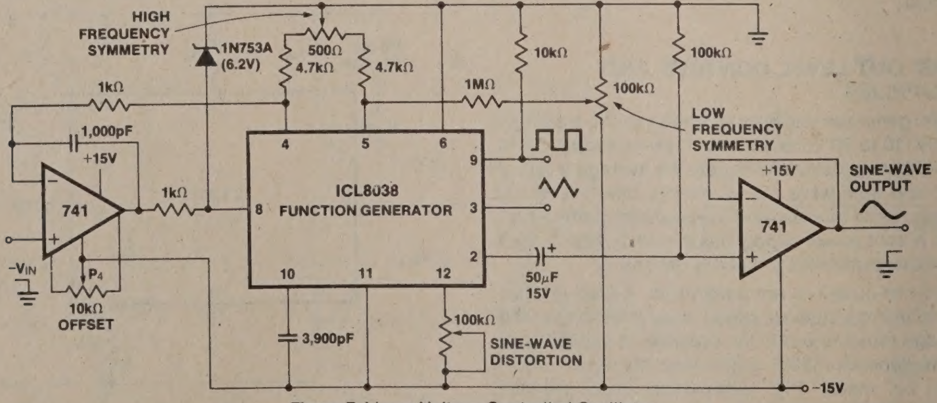

HIGH FREQUENCY SYMMETRY
1N753A (6.2V)
500Ω
4.7kΩ
4.7kΩ
10kΩ
100kΩ
1kΩ
1MΩ
100kΩ
LOW FREQUENCY SYMMETRY
1,000pF
+15V
4
5
6
9
741
1kΩ
ICL8038 FUNCTION GENERATOR
8
3
+15V
SINE-WAVE OUTPUT
741
−VIN
P4
2
10
11
12
50μF 15V
10kΩ OFFSET
3,900pF
100kΩ
SINE-WAVE DISTORTION
−15V

Figure 7: Linear Voltage Controlled Oscillator

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 7.

USE IN PHASE-LOCKED LOOPS

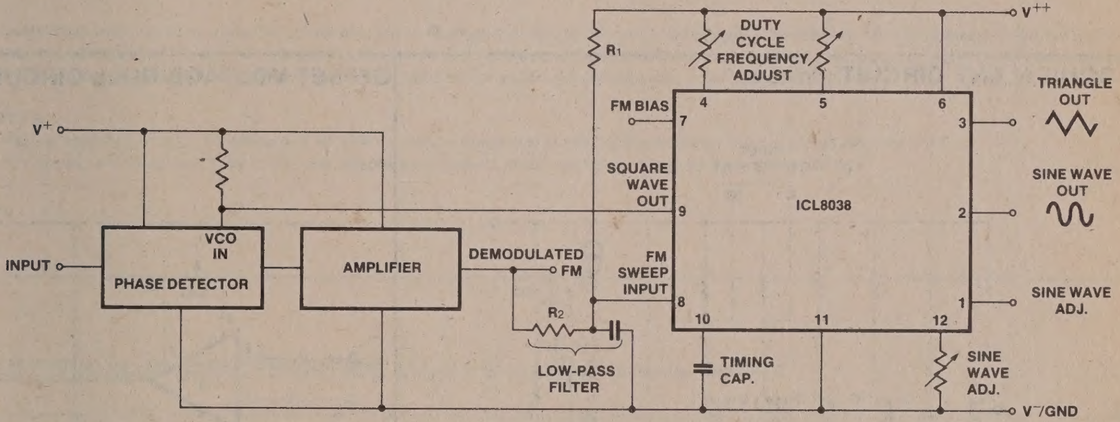
Its high frequency stability makes the ICL8038 an ideal building block for a phase-locked loop. In this application the remaining functional blocks, the phase-detector and the amplifier, can be formed by a number of available IC's (e.g. MC 4344, NE 562, HA 2800, HA 2820).

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase-detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, 0.8 × V^+). The simplest solution here is to provide a voltage divider to V^+ (R_1, R_2 as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but it also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Intersil Application Bulletin A013, "Everything You Always Wanted to Know About The 8038."



V++
R1
DUTY CYCLE FREQUENCY ADJUST
4
5
6
FM BIAS
7
TRIANGLE OUT
3
V+
SQUARE WAVE OUT
9
ICL8038
2
SINE WAVE OUT
VCO IN
PHASE DETECTOR
INPUT
AMPLIFIER
DEMODULATED FM
FM SWEEP INPUT
8
1
SINE WAVE ADJ.
R2
10
11
12
LOW-PASS FILTER
TIMING CAP.
SINE WAVE ADJ.
V−/GND

Figure 8: Waveform Generator Used as Stable VCO in a Phase-Locked Loop

ICL 8043

Dual Fet Input OpAmp

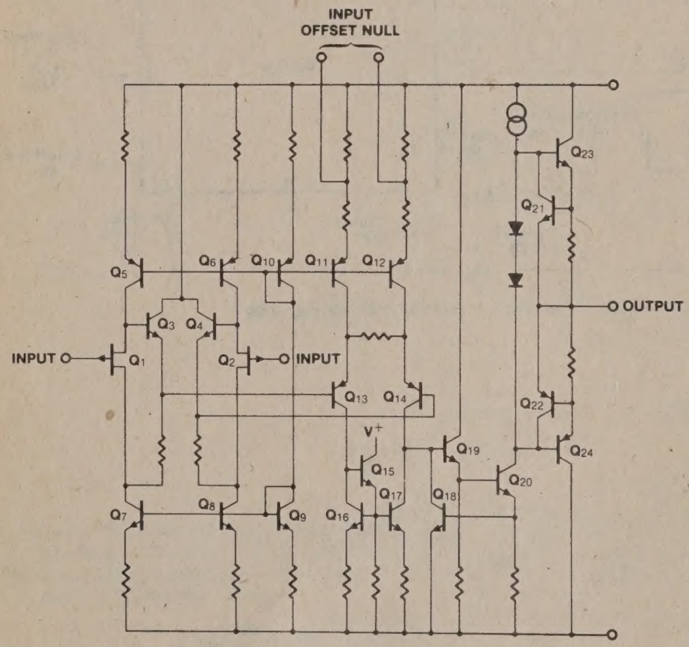
FEATURES

- **Very low input current — 1pA**
- **High slew rate — 6V/μs**
- **Internal frequency compensation**
- **Low power dissipation — 135mW typ**
- **Monolithic construction**

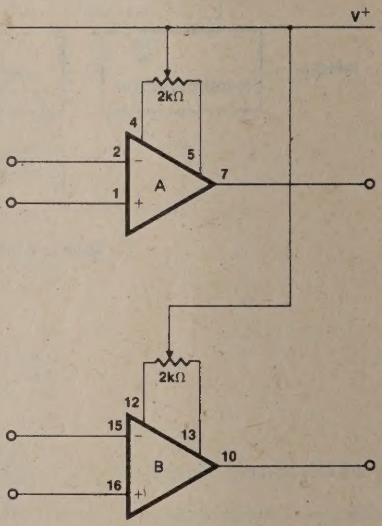
GENERAL DESCRIPTION

The ICL8043 contains two FET input op amps, each similar in performance to the ICL8007. The inputs and outputs are fully short circuit protected, and no latch-up problems exist. Offset nulling is accomplished by using a single pot (for each amplifier) connected to the positive supply voltage. The devices have excellent common mode rejection.

EQUIVALENT CIRCUIT (One Side)


INPUT OFFSET NULL
Q23
Q21
Q5
Q6
Q10
Q11
Q12
OUTPUT
Q3
Q4
INPUT
Q1
Q2
INPUT
Q13
Q14
Q22
V+
Q19
Q24
Q15
Q20
Q17
Q18
Q7
Q8
Q9
Q16

OFFSET VOLTAGE NULL CIRCUIT

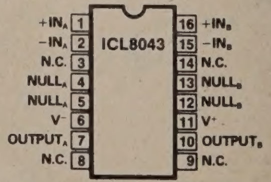

V+
2kΩ
4
2
5
7
1
A
−
+
2kΩ
12
15
13
10
B
16

ORDERING INFORMATION

TYPE	ORDER PART NUMBER	PACKAGE	TEMPERATURE RANGE
8043M	ICL8043MJE	Ceramic 16 Pin DIP	−55°C to 125°C
8043C	ICL8043CPE	Plastic 16 Pin DIP	0°C to 70°C
8043C	ICL8043CJE	Ceramic 16 Pin DIP	0°C to 70°C

PIN CONFIGURATION

16 PIN DIP (TOP VIEW)


ICL8043
+IN_A 1
−IN_A 2
N.C. 3
NULL_A 4
NULL_A 5
V− 6
OUTPUT_A 7
N.C. 8
16 +IN_B
15 −IN_B
14 N.C.
13 NULL_B
12 NULL_B
11 V+
10 OUTPUT_B
9 N.C.

(outline dwgs JE, PE)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V^+	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
8043M	−55°C to +125°C
8043C	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration	Indefinite

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES:

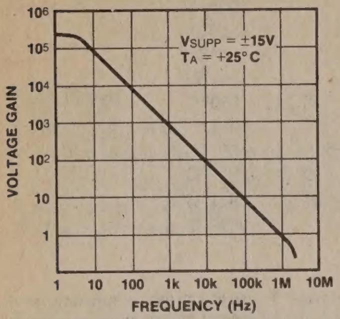
1. Rating applies for case temperatures to 125°C; derate linearly at 9mW/°C for ambient temperatures above +95°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (V_{SUPP} = ±15V unless otherwise specified)

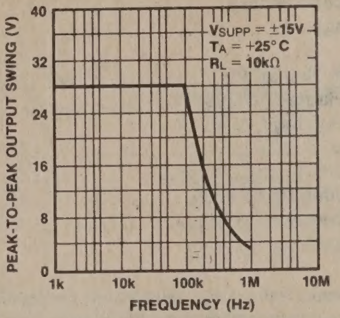
SYMBOL	CHARACTERISTICS	CONDITIONS	8043M MIN.	8043M TYP.	8043M MAX.	8043C MIN.	8043C TYP.	8043C MAX.	UNITS
The following specifications apply for $T_A = 25°C$:									
V_{OS}	Input Offset Voltage	$R_S < 100k\Omega$		10	20		20	50	mV
I_{OS}	Input Offset Current			0.5			0.5		pA
I_{IN}	Input Current (either input)			2.0	20		3.0	50	pA
R_{IN}	Input Resistance			10^6			10^6		MΩ
C_{IN}	Input Capacitance			2.0			2.0		pF
A_V	Large Signal Voltage Gain	$R_L > 2k\Omega$, $V_{out} = \pm10V$	50,000			20,000			V/V
R_O	Output Resistance			75			75		Ω
I_{SC}	Output Short-Circuit Current			25			25		mA
I_{SUPP}	Supply Current (Total)			4.5	6		4.5	6.8	mA
Pd	Power Consumption			135	180		135	204	mW
SR	Slew Rate			6.0			6.0		V/μs
GBW	Unity Gain Bandwidth			1.0			1.0		MHz
t_r	Transient Response (Unity Gain)	$C_L < 100pF$, $R_L = 2k\Omega$							
	Risetime			300			300		ns
	Overshoot			10			10		%
The following specifications apply for $0°C < T_A < +70°C$ (8043C), $-55°C < T_A < +125°C$ (8043M):									
ΔV_{IN}	Input Voltage Range		±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio		70	90		70	90		dB
PSRR	Supply Voltage Rejection Ratio			70	300		70	600	μV/V
A_V	Large Signal Voltage Gain		25,000			15,000			V/V
$\pm V_O$	Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
		$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
V_{OS}	Input Offset Voltage			15	30		30	60	mV
I_{IN}	Input Current (either input)	$T_A = +125°C$		2.0	15				nA
		$T_A = +70°C$					50	175	pA
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage				75			75	μV/°C

TYPICAL PERFORMANCE CURVES

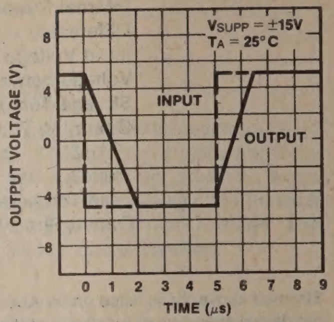
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



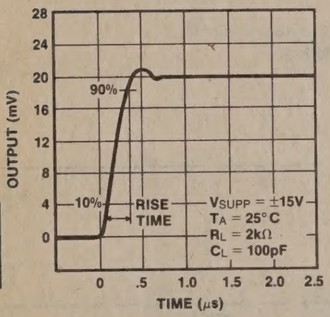
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



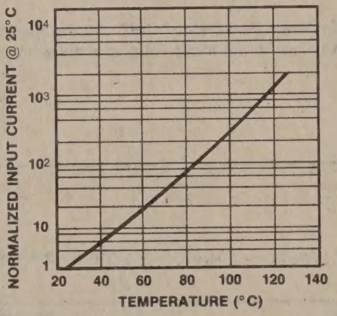
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



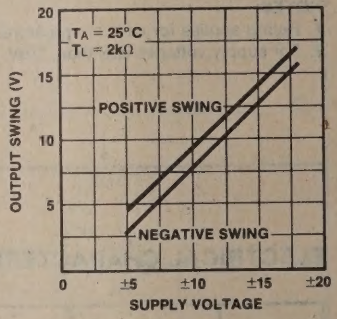
TRANSIENT RESPONSE



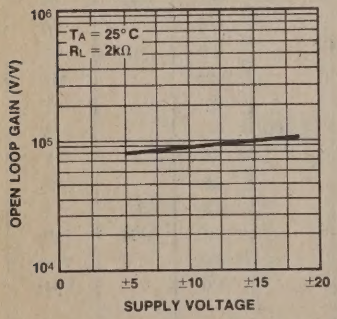
INPUT CURRENT AS A FUNCTION OF TEMPERATURE



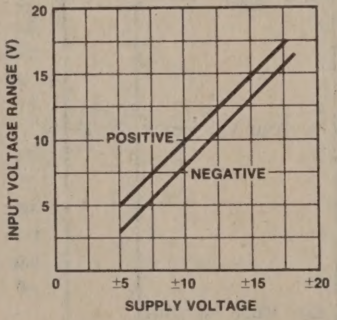
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



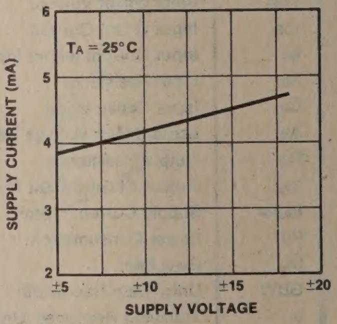
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



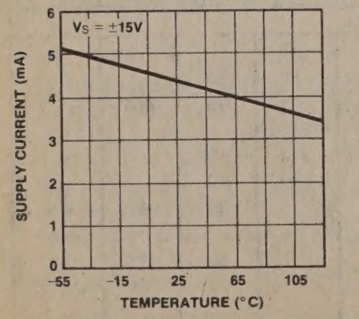
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



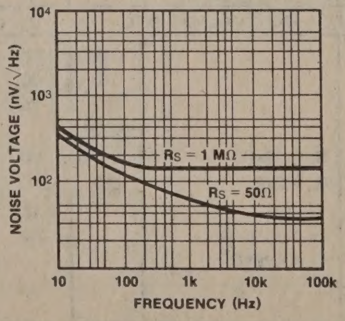
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



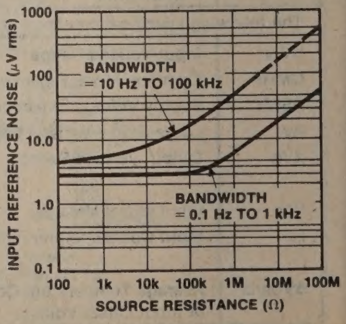
TOTAL QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



CHANNEL SEPARATION

Channel separation or crosstalk is measured using the circuit of Figure 1. One amplifier is driven so that its output swings ±10V; the signal amplitude seen in the other amplifier (referred to the input) is then measured. Typical performance is shown in Figure 2.

$$\text{Channel Separation} = 20 \log \left(\frac{V_{OUT(A)}}{V_{IN(B)}}\right)$$

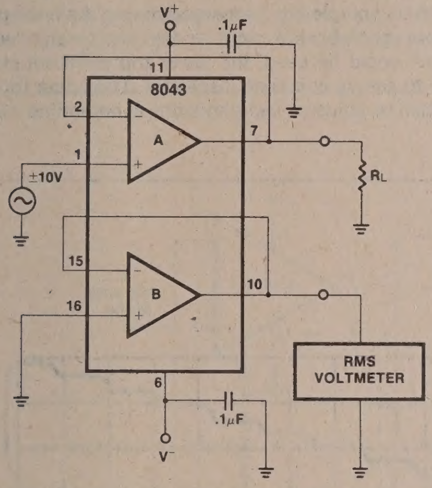


Figure 1

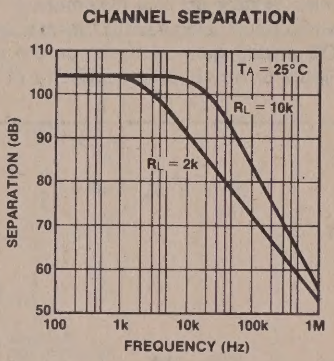


Figure 2

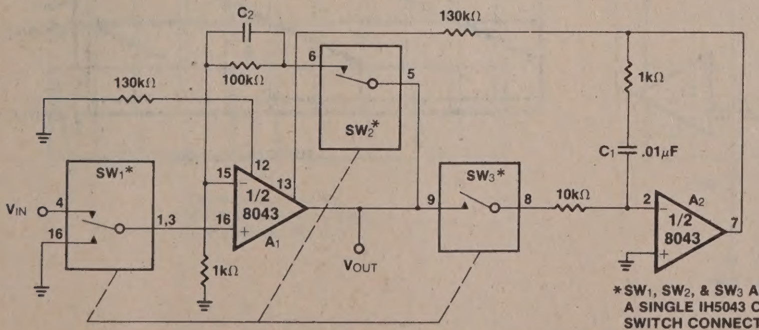
APPLICATIONS

Applications for any dual amplifier fall into two categories. There are those which use the two-in-one package concept simply to save circuit-board space and cost, but more interesting are those circuits where the two sides of the dual are used to complement one another in a subsystem application. The circuits which follow have been selected on this basis.

AUTOMATIC OFFSET SUPPRESSION CIRCUIT

The circuit shown in Figure 3 uses one amplifier (A_1) as a normal gain stage, while the other (A_2) forms part of an offset voltage zeroing loop. There are two modes of operation which occur sequentially; first, an offset null correction mode during which the offset voltage of A_1 is nulled out. Following this nulling operation, A_1 is used as a normal amplifier while the voltage necessary to zero its offset voltage is stored on the integrator comprised of A_2 and C_1.

The advantage of this circuit is that it allows chopper amplifier performance to be achieved at one-tenth the cost. The only limitation is that during the offset nulling mode, A_1 is disconnected from the input. However, in most data acquisition systems, many inputs are scanned sequentially. It is fairly simple to synchronize the offset nulling operation so that it does not occur when that particular amplifier is being "looked at". For the component values shown in Figure 3, and assuming a total leakage of 50pA at the inverting input of A_2, the offset voltage referred to the input of A_1 will drift away from zero at only 40µV/sec. Thus, the offset nulling information stored on C_1 can be "refreshed" relatively infrequently. The measured offset voltage of A_1 during the amplification mode was 11µV; offset voltage drift with temperature was less than 0.1µV/°C.



*SW₁, SW₂, & SW₃ ARE ALL PART OF A SINGLE IH5043 CMOS ANALOG SWITCH CONNECTED AS SHOWN IN FIGURE 3B

Figure 3A.

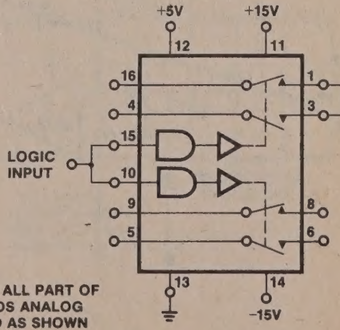


Figure 3B.

STAIRCASE GENERATOR

The circuit shown in Figure 4 is a high input impedance version of the so-called "diode pump" or staircase generator. Note that charge transfer takes place at the negative-going edge of the input-signal.

The most common application for staircase generators is in low cost counters. By resetting the capacitor when the output reaches a predetermined level, the circuit may be made to count reliably up to a maximum of about 10. A straightforward circuit using a LM311 for the level detector, and a CMOS analog gate to discharge the capacitor, is shown in Figure 5. An important property of this type of counter is the ease with which the count can be changed; it is only necessary to change the voltage at which the comparator trips. A low cost A-D converter can also be designed using the same principle since the digital count between reset periods is directly proportional to the analog voltage used as a reference for the comparator.

A considerable amount of hysteresis is used in the comparator shown in Figure 5. This ensures that the capacitor is completely discharged during the reset period. In a more sophisticated circuit, a dual comparator "window detector" could be used, the lower trip point set close to ground to assure complete discharge. The upper trip point could then be adjusted independently to determine the pulse count.

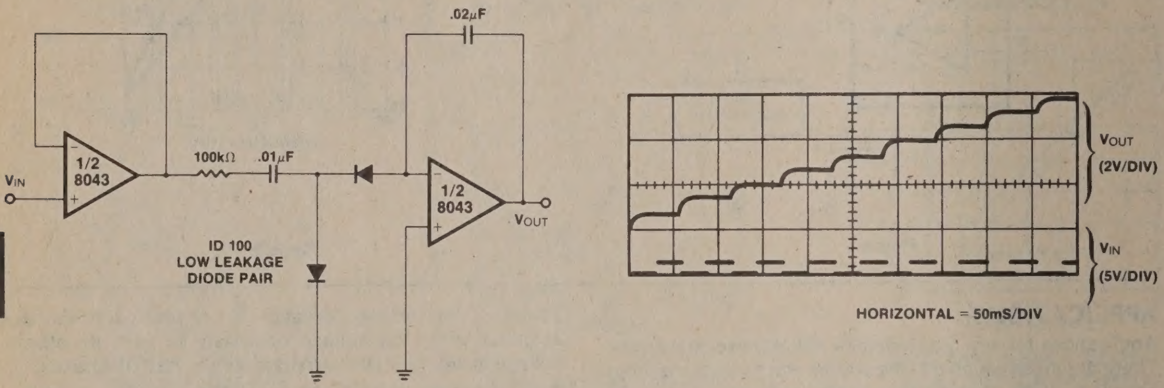

.02µF
VIN
1/2
8043
100kΩ
.01µF
1/2
8043
VOUT
ID 100
LOW LEAKAGE
DIODE PAIR
VOUT
(2V/DIV)
VIN
(5V/DIV)
HORIZONTAL = 50mS/DIV

Figure 4

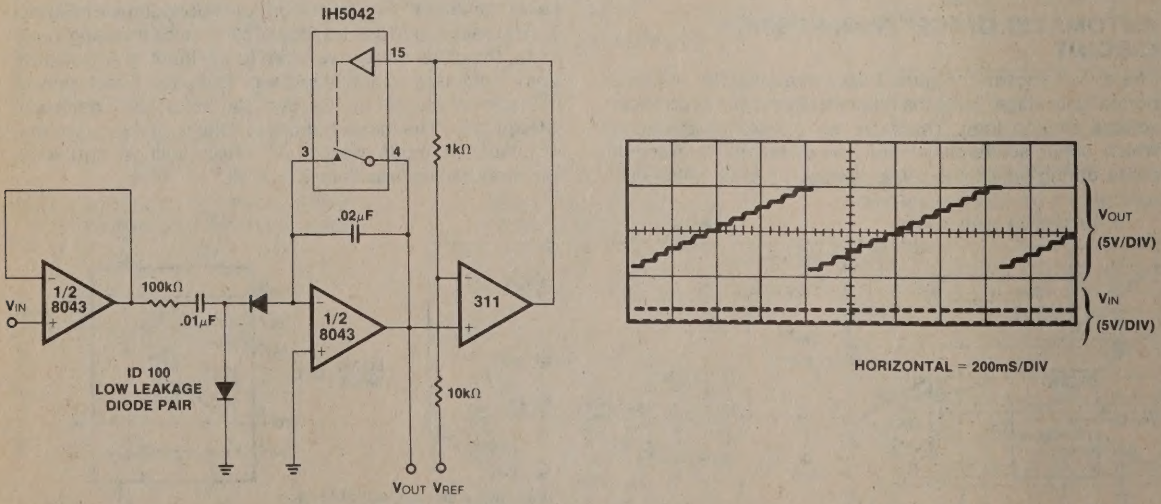

IH5042
15
3
4
1kΩ
.02µF
VIN
1/2
8043
100kΩ
.01µF
1/2
8043
311
ID 100
LOW LEAKAGE
DIODE PAIR
10kΩ
VOUT
VREF
VOUT
(5V/DIV)
VIN
(5V/DIV)
HORIZONTAL = 200mS/DIV

Figure 5

SAMPLE & HOLD CIRCUIT

Two important properties of the 8043 are used to advantage in this circuit. The low input bias currents give rise to slow output decay rates ("droop") in the hold mode, while the high slew rate (6V/μS) improves the tracking speed and the response time of the circuit. See Figure 6.

The ability of the circuit to track fast moving inputs is shown in Figure 7A. The upper waveform is the input (10V/div), the lower waveform the output (5V/div). The logic input is high.

Actual sample and hold waveforms are shown in Figure 7B. The center waveform is the analog input, a ramp moving at about 67V/ms, the lower waveform is the logic input to the sample & hold; a logic "1" initiates the sample mode. The upper waveform is the output, displaced by about 1 scope division (2V) from the input to avoid superimposing traces. The hold mode, during which the output remains constant, is clearly visible. At the beginning of a sample period, the output takes about 8μsec to catch up with the input, after which it tracks until the next hold period.

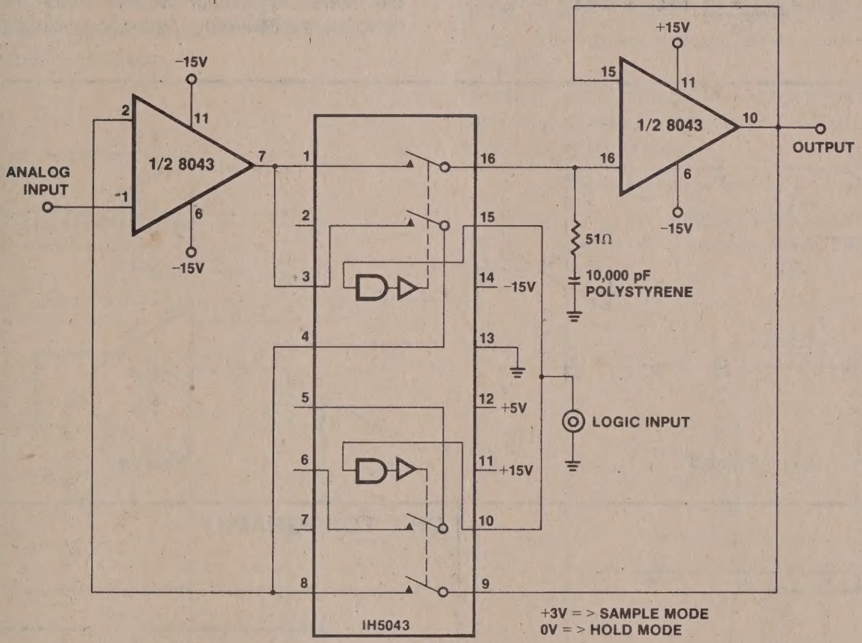
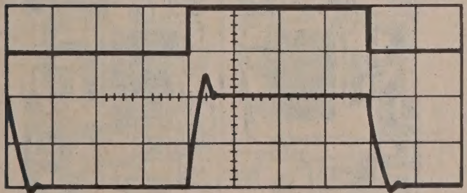
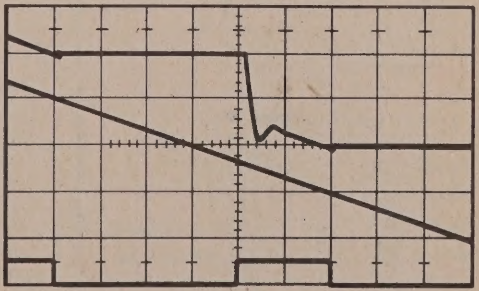

-15V
11
2
-1
1/2 8043
7
6
-15V
ANALOG INPUT
1
2
3
4
5
6
7
8
16
15
14
-15V
13
12
+5V
11
+15V
10
9
IH5043
+15V
15
11
1/2 8043
10
16
6
-15V
OUTPUT
51Ω
10,000 pF POLYSTYRENE
LOGIC INPUT
+3V = > SAMPLE MODE
0V = > HOLD MODE

Figure 6



TOP: INPUT (10V/DIV)
BOTTOM: OUTPUT (5V/DIV)
HORIZONTAL: 10μs/DIV

Figure 7A



TOP: 2V/DIV
CENTER: 2V/DIV
BOTTOM: 10V/DIV
HORIZONTAL: 10μs/DIV

Figure 7B

INSTRUMENTATION AMPLIFIER

A dual FET input operational amplifier is an attractive component around which to build an instrumentation amplifier because of the high input resistance. The circuit shown in Figure 8 uses the popular triple op-amp approach. The output amplifier is a High Speed 741 (741 HS, slew rate guaranteed ≥0.7V/μs) so as to utilize the high slew rate of the 8043 to the maximum extent. Input resistance of the circuit (either input, regardless of gain configuration) is in excess of 10^{12} ohms.

For the component values shown, the overall amplifier gain is 200 (front end gain = $\frac{2R_1 + R_2}{R_2}$, back end gain, = R_6/R_4).

Common mode rejection is largely determined by the matching between R_4 and R_5, and R_6 and R_7. In applications where offset nulling is required, a single potentiometer can be connected as shown in Figure 9.

Another popular circuit is given in Figure 10. In this case the gain is $1 + R_1/R_2$, and the CMRR determined by the match between R_1 and R_4, R_2 and R_3.

For more information on FET input operational amplifiers, see Intersil Application Bulletin A005 "The 8007: A High Performance FET-input Operational Amplifier."

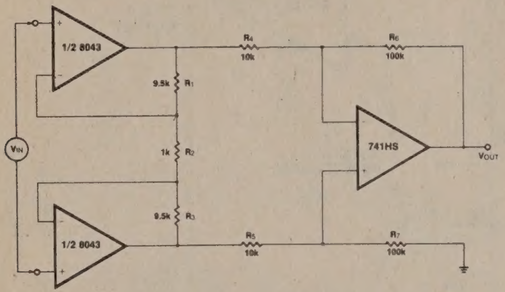

1/2 8043
R4
10k
R6
100k
9.5k R1
1k R2
9.5k R3
VIN
741HS
VOUT
1/2 8043
R5
10k
R7
100k

Figure 8

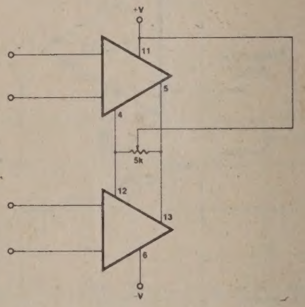

+V
11
5
4
5k
12
13
6
-V

Figure 9

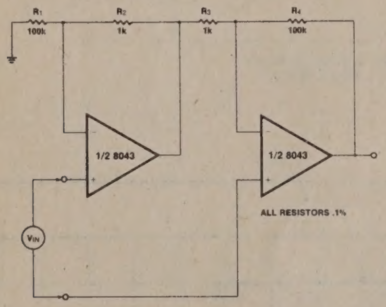
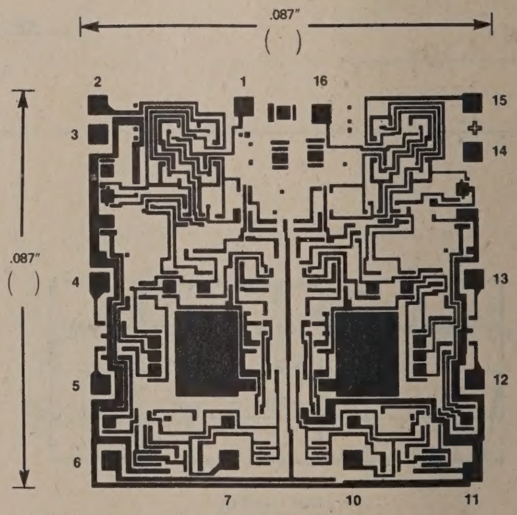

R1
100k
R2
1k
R3
1k
R4
100k
1/2 8043
1/2 8043
VIN
ALL RESISTORS .1%

Figure 10

CHIP TOPOGRAPHY


.087"
( )
.087"
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2
1
16
15
3
14
4
13
5
12
6
7
10
11

ICL8048, ICL8049
Monolithic Log Amplifier
Monolithic Antilog Amplifier

5

FEATURES

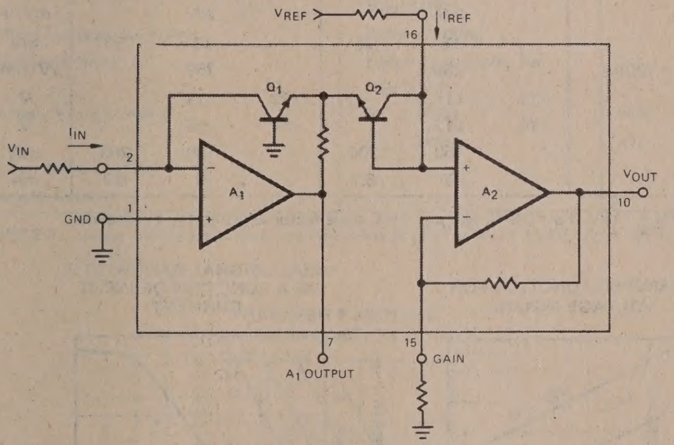
- 1/2% Full Scale Accuracy
- Temperature Compensated 0°C to 70°C
- Scale Factor 1V/Decade, Adjustable
- 120dB Dynamic Current Range (8048)
- 60dB Dynamic Voltage Range (8048 & 8049)
- Dual FET-Input Op-Amps

GENERAL DESCRIPTION

The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

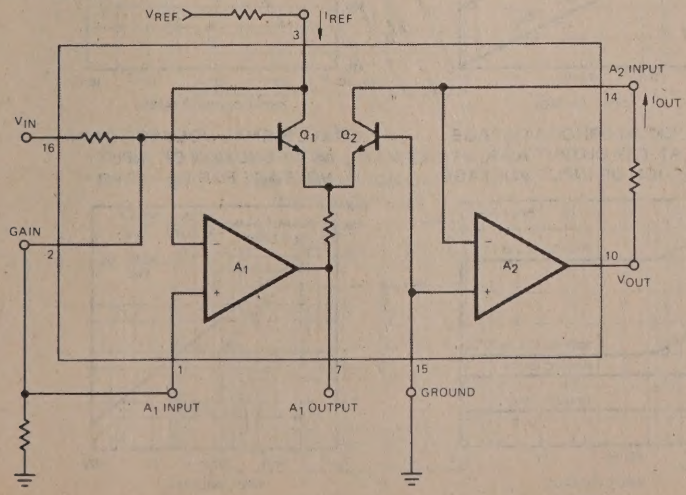
The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1-volt change at the input.

8048 SCHEMATIC DIAGRAM



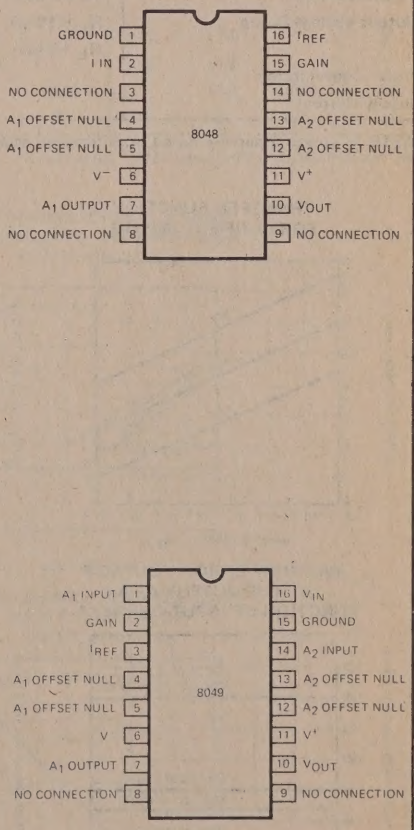
VREF
IREF
16
Q1
Q2
IIN
VIN
2
A1
A2
VOUT
10
GND
1
7
15
A1 OUTPUT
GAIN

8049 SCHEMATIC DIAGRAM



VREF
IREF
3
A2 INPUT
14
IOUT
VIN
16
Q1
Q2
GAIN
2
A1
A2
10
VOUT
1
7
15
A1 INPUT
A1 OUTPUT
GROUND

PIN CONFIGURATION
(outline dwgs DE, PE)



GROUND 1
I IN 2
NO CONNECTION 3
A1 OFFSET NULL 4
A1 OFFSET NULL 5
V− 6
A1 OUTPUT 7
NO CONNECTION 8
8048
16 IREF
15 GAIN
14 NO CONNECTION
13 A2 OFFSET NULL
12 A2 OFFSET NULL
11 V+
10 VOUT
9 NO CONNECTION
A1 INPUT 1
GAIN 2
IREF 3
A1 OFFSET NULL 4
A1 OFFSET NULL 5
V 6
A1 OUTPUT 7
NO CONNECTION 8
8049
16 VIN
15 GROUND
14 A2 INPUT
13 A2 OFFSET NULL
12 A2 OFFSET NULL
11 V+
10 VOUT
9 NO CONNECTION

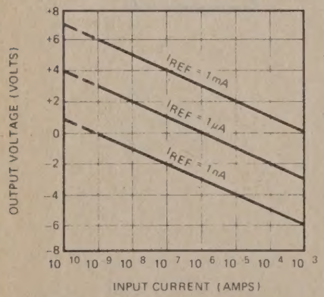
MAXIMUM RATINGS

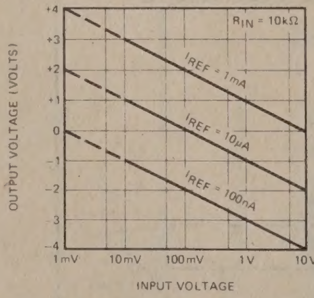
Supply Voltage	±18 V
I_{in} (Input Current)	2 mA
I_{ref} (Reference Current)	2 mA
Voltage between Offset Null and V^+	±0.5 V
Power Dissipation	750 mW
Operating Temperature Range	0°C to +70°C
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 60 sec.)	300°C

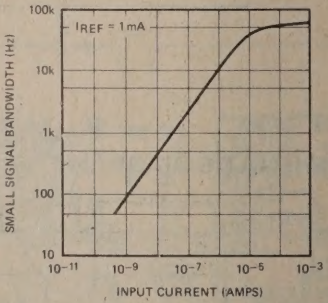
ELECTRICAL CHARACTERISTIC (Note 1)

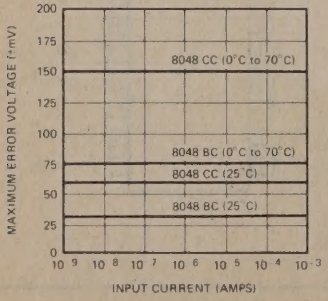
PARAMETER	CONDITION	8048BC MIN.	8048BC TYP.	8048BC MAX.	8048CC MIN.	8048CC TYP.	8048CC MAX.	UNITS
Dynamic Range								
I_{in} (1 nA–1 mA)		120			120			dB
V_{in} (10 mV–10 V)	R_{IN} = 10 kΩ	60			60			dB
Error, % of Full Scale	T_A = 25°C, I_{IN} = 1 nA to 1 mA		.20	0.5		.25	1.0	%
Error, % of Full Scale	T_A = 0°C to +70°C, I_{IN} = 1 nA to 1 mA		.60	1.25		.80	2.5	%
Error, Absolute Value	T_A = 25°C, I_{IN} = 1 nA to 1 mA		12	30		14	60	mV
Error, Absolute Value	T_A = 0°C to +70°C, I_{IN} = 1 nA to 1 mA		36	75		50	150	mV
Temperature Coefficient of V_{OUT}	I_{IN} = 1 nA to 1 mA		0.8			0.8		mV/°C
Power Supply Rejection Ratio	Referred to Output		2.5			2.5		mV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	At Output, for I_{IN} = 100 μA		250			250		μV (RMS)
Output Voltage Swing	R_L = 10 kΩ	±12	±14		±12	±14		V
	R_L = 2 kΩ	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

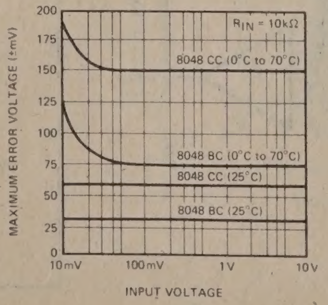
NOTE 1: Unless otherwise noted, specifications apply for V_S = ±15V, T_A = 25°C, I_{REF} = 1mA, scale factor adjusted for 1V/decade.

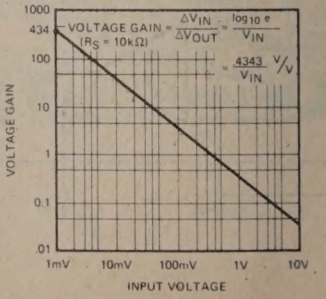

TRANSFER FUNCTION FOR CURRENT INPUTS


TRANSFER FUNCTION FOR VOLTAGE INPUTS


SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT CURRENT


MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT CURRENT


MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT VOLTAGE


SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE FOR R_S = 10 kΩ

MAXIMUM RATINGS

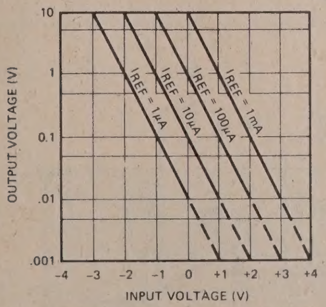
Supply Voltage	±18V
V_{in} (Input Voltage)	±15V
I_{ref} (Reference Current)	2mA
Voltage between Offset Null and V^+	±0.5V
Power Dissipation	750mW
Operating Temperature Range	0°C to +70°C
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTIC (Note 1)

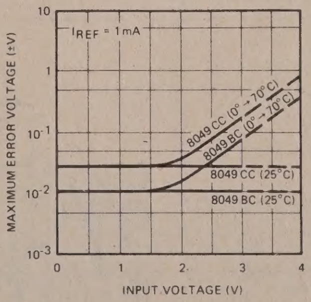
PARAMETER	CONDITION	8049BC MIN.	TYP.	MAX.	8049CC MIN.	TYP.	MAX.	UNITS
Dynamic Range (V_{OUT})	V_{OUT} = 10mV to 10V	60			60			dB
Error, Absolute Value	T_A = 25°C, $0V \leq V_{IN} \leq 3V$		3	10		5	25	mV
Error, Absolute Value	T_A = 0°C to +70°C, $0V \leq V_{IN} \leq 3V$		20	75		30	150	mV
Temperature Coefficient, Referred to V_{IN}	V_{IN} = 3V		0.38			0.55		mV/°C
Power Supply Rejection Ratio	Referred to Input, for V_{IN} = 0V		2.0			2.0		µV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	Referred to Input, for V_{IN} = 0V		26			26		µV(RMS)
Output Voltage Swing	R_L = 10kΩ	±12	±14		±12	±14		V
	R_L = 2kΩ	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

NOTE 1: Unless otherwise noted, specifications apply for V_S = ±15V, T_A = 25°C, I_{REF} = 1mA, scale factor adjusted for 1 decade (out) per volt (in).

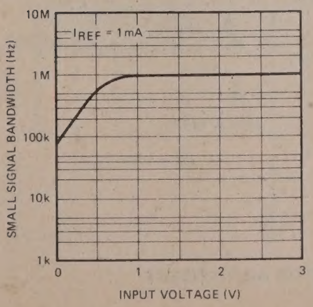
TRANSFER FUNCTION (V_{OUT} AS A FUNCTION OF V_{IN})



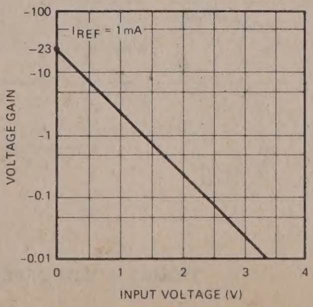
MAXIMUM ERROR VOLTAGE REFERRED TO THE INPUT AS A FUNCTION OF V_{IN}



SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT VOLTAGE



SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE



THEORY OF OPERATION

The 8048 relies for its operation on the well-known exponential relationship between the collector current and the base-emitter voltage of a transistor:

$$I_C = I_S\left[e^{qV_{BE}/kT} - 1\right] \qquad (1)$$

For base-emitter voltages greater than 100mV, Eq. (1) becomes

$$I_C = I_S\, e^{qV_{BE}/kT} \qquad (2)$$

From Eq. (2), it can be shown that for two identical transistors operating at different collector currents, the V_{BE} difference (ΔV_{BE}) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log_{10}\left[{}^{I_{C1}}\!/_{I_{C2}}\right] \qquad (3)$$

Referring to Fig. 1, it is clear that the potential at the collector of Q_2 is equal to the ΔV_{BE} between Q_1 and Q_2. The output voltage is ΔV_{BE} multiplied by the gain of A_2:

$$V_{OUT} = -2.303\left(\frac{R_1 + R_2}{R_2}\right)\left(\frac{kT}{q}\right)\log_{10}\left[{}^{I_{IN}}\!/_{I_{REF}}\right] \qquad (4)$$

The expression $2.303 \times \frac{kT}{q}$ has a numerical value of 59mV at 25°C; thus in order to generate 1 volt/decade at the output, the ratio $(R_1 + R_2)/R_2$ is chosen to be 16.9. For this scale factor to hold constant as a function of temperature, the $(R_1 + R_2)/R_2$ term must have a 1/T characteristic to compensate for kT/q.

In the 8048 this is achieved by making R_1 a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at 25°C, and its temperature coefficient is carefully designed to provide the necessary compensation. Resistor R_2 is external and should be a low T.C. type; it should have a nominal value of 1kΩ to provide 1 volt/decade, and must have an adjustment range of ±20% to allow for production variations in the absolute value of R_1.

OFFSET AND SCALE FACTOR ADJUSTMENT

A log amp, unlike an op-amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q_1 of collector current and open the feedback loop around A_1. Instead, it is necessary to zero the offset voltage of A_1 and A_2 separately, and then to adjust the scale factor. Referring to Fig. 1, this is done as follows:

1) Temporarily connect a 10kΩ resistor (R_0) between pins 2 and 7. With no input voltage, adjust R_4 until the output of A_1 (pin 7) is zero. Remove R_0.

   Note that for a current input, this adjustment is not necessary since the offset voltage of A_1 does not cause any error for current-source inputs.

2) Set $I_{IN} = I_{REF} = 1$mA. Adjust R_5 such that the output of A_2 (pin 10) is zero.

3) Set $I_{IN} = 1\mu$A, $I_{REF} = 1$mA. Adjust R_2 for $V_{OUT} = 3$ volts (for a 1 volt/decade scale factor) or 6 volts (for a 2 volt/decade scale factor).

Step #3 determines the scale factor. Setting $I_{IN} = 1\mu$A optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the 8048 is to be used for inputs which only span the range 100μA to 1mA, it would be better to set $I_{IN} = 100\mu$A in Step #3. Similarly, adjustment for other scale factors would require different I_{IN} and V_{OUT} values.

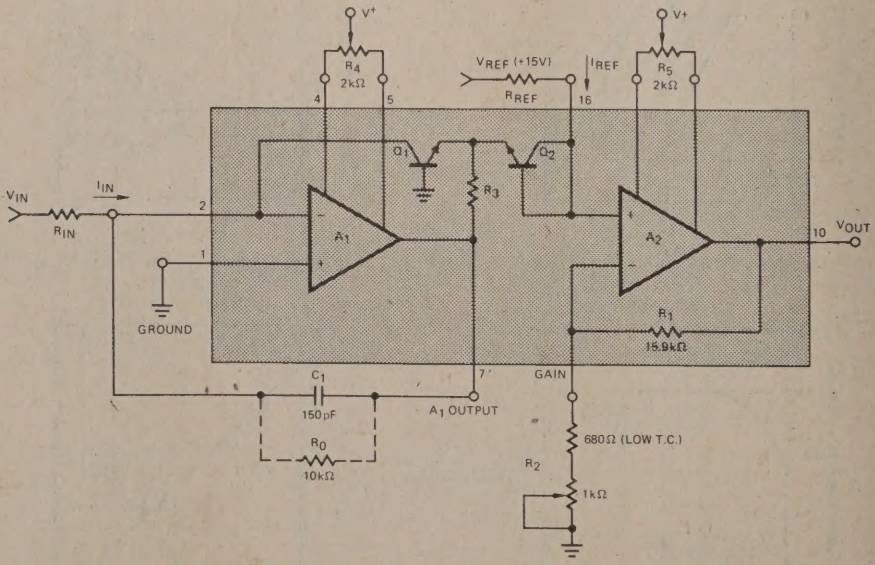


FIGURE 1. 8048 OFFSET AND SCALE FACTOR ADJUSTMENT

THEORY OF OPERATION

The 8049 relies on the same logarithmic properties of the transistor as the 8048. The input voltage forces a specific ΔV_{BE} between Q_1 and Q_2 (Fig. 2). This V_{BE} difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on Page 3 and is as follows:

$$I_{C_1}/I_{C_2} = \exp\left[q\Delta V_{BE}/kT\right] \qquad (5)$$

When numerical values for q/kT are put into this equation, it is found that a ΔV_{BE} of 59mV (at 25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1 volt change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising R_1 and R_2. In order that scale factors other than one decade per volt may be selected, R_2 is external to the chip. It should have a value of 1kΩ, adjustable ±20%, for one decade per volt. R_1 is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of equation 5, as explained on Page 3.

The overall transfer function is as follows:

$$I_{OUT}/I_{REF} = \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{qV_{IN}}{kT}\right] \qquad (6)$$

Substituting $V_{OUT} = I_{OUT} \times R_{OUT}$ gives:

$$V_{OUT} = R_{OUT}\, I_{REF} \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{qV_{IN}}{kT}\right] \qquad (7)$$

For voltage references equation 7 becomes

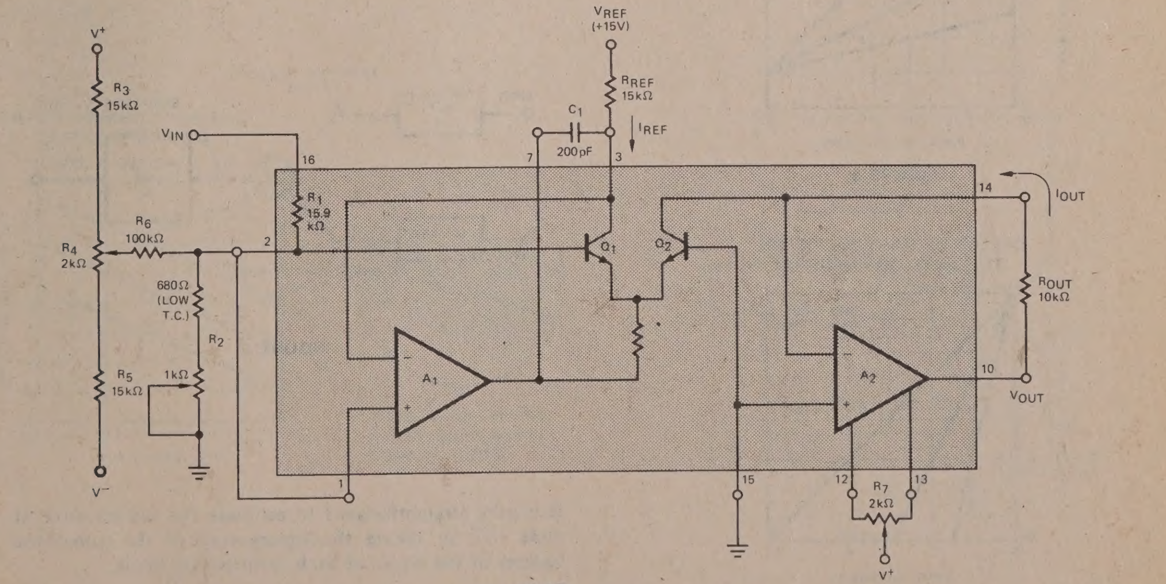
$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{qV_{IN}}{kT}\right] \qquad (8)$$

OFFSET AND SCALE FACTOR ADJUSTMENT

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of A_2. This is accomplished by reverse biasing the base-emitter of Q_2. A_2 then operates as a unity gain buffer with a grounded input. The second step forces $V_{IN} = 0$; the output is adjusted for $V_{OUT} = 10V$. This step essentially "anchors" one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Fig. 2, the exact procedure for 1 decade/volt is as follows:

1) Connect the input (pin #16) to +15V. This reverse biases the base-emitter of Q_2. Adjust R_7 for $V_{OUT} = 0V$. Disconnect the input from +15V.
2) Connect the input to Ground. Adjust R_4 for $V_{OUT} = 10V$. Disconnect the input from Ground.
3) Connect the input to a precise 2V supply and adjust R_2 for $V_{OUT} = 100mV$.

The procedure outlined above optimizes the performance over a 3 decade range at the output (i. e., V_{OUT} from 10mV to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1 volt supply and adjust for $V_{OUT} = 1V$. For other scale factors and/or starting points, different values for R_2 and R_{REF} will be needed, but the same basic procedure applies.



8049
FIGURE 2

APPLICATIONS INFORMATION

Scale Factor Adjustment

The scale factor adjustment procedures outlined on Page 3 (8048) and Page 5 (8049) are primarily directed towards setting up 1 volt (ΔV_{OUT}) per decade (ΔI_{IN} or ΔV_{IN}) for the log amp, or one decade (ΔV_{OUT}) per volt (ΔV_{IN}) for the antilog amp.

This corresponds to K = 1 in the respective transfer functions:

$$\text{Log Amp:}\quad V_{OUT} = -K \log_{10}\left[{}^{I_{IN}}/_{I_{REF}}\right] \qquad (9)$$

$$\text{Antilog Amp:}\quad V_{OUT} = R_{OUT}\, I_{REF}\ 10^{-V_{IN}/K} \qquad (10)$$

By adjusting R_2 (Fig. 1 and Fig. 2) the scale factor "K" in equation 9 and 10 can be varied. The effect of changing K is shown graphically in Fig. 3 for the log amp, and Fig. 4 for the antilog amp. The nominal value of R_2 required to give a specific value of K can be determined from equation 11. It should be remembered that R_1 has a ±20% tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R_2 by ±20%.

$$R_2 = \frac{941}{(K - .059)}\ \Omega \qquad (11)$$

EFFECT OF VARYING "K" ON THE LOG AMPLIFIER

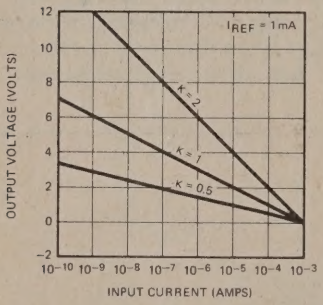


FIGURE 3

EFFECT OF VARYING "K" ON THE ANTILOG AMPLIFIER

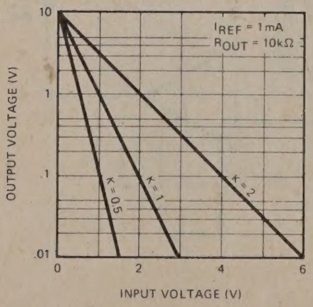


FIGURE 4

Frequency Compensation

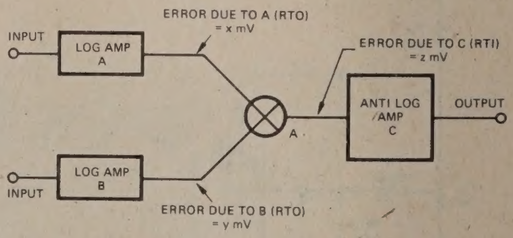
Although the op-amps in both the 8048 and the 8049 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the 8048, 150 pF should be connected between Pins 2 and 7 (Fig. 1). In the 8049, 200 pF between Pins 3 and 7 is recommended (Fig. 2).

Error Analysis

Performing a meaningful error analysis of a circuit containing log and antilog amplifiers is more complex than dealing with a similar circuit involving only op-amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op-amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given on Pages 2 and 4.

The various error terms in the log amplifier, the 8048, are referred to the output (RTO) of the device. The error terms in the antilog amplifier, the 8049, are referred to the input (RTI) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Fig. 5.



ERROR DUE TO A (RTO) = x mV
INPUT
LOG AMP A
ERROR DUE TO C (RTI) = z mV
ANTI LOG AMP C
OUTPUT
A
INPUT
LOG AMP B
ERROR DUE TO B (RTO) = y mV

FIGURE 5

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2 + y^2 + z^2}\quad \text{at (A)}$$

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain plot on Page 4.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots given on Pages 2 and 4. For example, with the 8048BC, the maximum error at the output is 30mV at 25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures on Page 3. Fig. 6 illustrates this point.

To determine the maximum error over the operating temperature range, the 0 to 70°C absolute error values given in the table of electrical characteristics should be used. For intermediate temperatures, assume a linear increase in the error between the 25°C value and the 70°C value.

For the antilog amplifier, the only difference is that the error refers to the input, i. e., the horizontal axis. It will be noticed that the maximum error voltage of the 8049, over the temperature range, is strongly dependent on the input voltage. This is because the output amplifier, A_2, has an offset voltage drift which is directly transmitted to the output. When this error is referred to the input, it must be divided by the voltage gain, which is input voltage dependent. At $V_{IN} = 3V$, for example, errors at the output are multiplied by 1/.023 (= 43.5) when referred to the input.

It is important to note that both the 8048 and the 8049 require positive values of I_{REF}, and the input (8048) or output (8049) currents (or voltages) respectively must also be positive. Application of negative I_{IN} to the 8048 or negative I_{REF} to either circuit will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

SETTING UP THE REFERENCE CURRENT

In both the 8048 and the 8049 the input current reference pin (I_{REF}) is not a true virtual ground. For the 8048, a fraction of the output voltage is seen on Pin 16 (Fig. 1). This does not constitute an appreciable error provided V_{REF} is much greater than this voltage. A 10V or 15V reference satisfies this condition. For the 8049, a fraction of the input voltage appears on Pin 3 (Fig. 2), placing a similar restraint on the value of V_{REF}.

Alternatively, I_{REF} can be provided from a true current source. One method of implementing such a current source is shown in Fig. 7.

LOG OF RATIO CIRCUIT, DIVISION

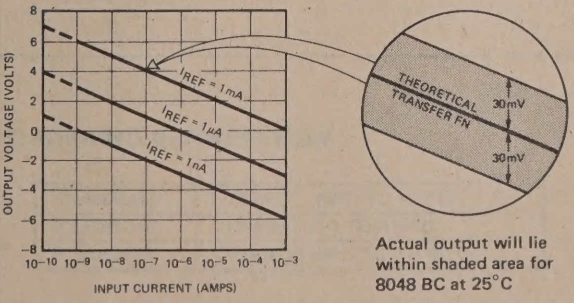
The 8048 may be used to generate the log of a ratio by modulating the I_{REF} input. The transfer function remains the same, as defined by equation 9:

$$V_{OUT} = -K \log_{10} \left[{}^{I_{IN}}\!/_{I_{REF}} \right] \qquad (9)$$

Clearly it is possible to perform division using just one 8048, followed by an 8049. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I_{REF} input not being a true virtual ground (discussed in the previous section), the circuit of Fig. 7 is again recommended if the I_{REF} input is to be modulated.

TRANSFER FUNCTION FOR
CURRENT INPUTS



Actual output will lie within shaded area for 8048 BC at 25°C

FIGURE 6

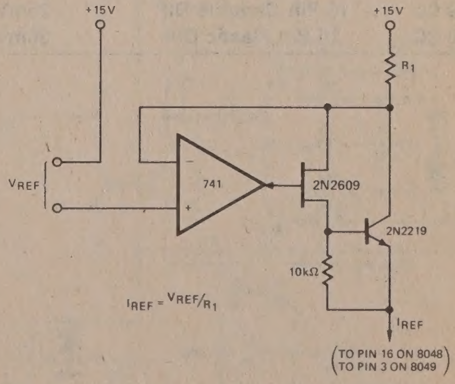


FIGURE 7

DEFINITION OF TERMS

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on Page 6.

DYNAMIC RANGE The dynamic range of the 8048 refers to the range of input voltages or currents over which the device is guaranteed to operate. For the 8049 the dynamic range refers to the range of output voltages over which the device is guaranteed to operate.

ERROR, ABSOLUTE VALUE The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined on Pages 3 (8048) or 5 (8049). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the 8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage. For the 8049 it is a measure of the deviation from the theoretical input voltage required to generate a specific output voltage.

The absolute error specification is guaranteed over the dynamic range.

ERROR, % OF FULL SCALE The error as a percentage of full scale can be obtained from the following relationship:

$$\text{Error, \% of Full Scale} = \frac{100 \times \text{Error, absolute value}}{\text{Full Scale Output Voltage}}$$

TEMPERATURE COEFFICIENT OF V_{OUT} OR V_{IN} For the 8048 the temperature coefficient refers to the drift with temperature of V_{OUT} for a constant input current. For the 8049 it is the temperature drift of the input voltage required to hold a constant value of V_{OUT}.

POWER SUPPLY REJECTION RATIO The ratio of the voltage change in the linear axis of the transfer function (V_{OUT} for the 8048, V_{IN} for the 8049) to the change in the supply voltage, assuming that the log axis is held constant.

WIDEBAND NOISE For the 8048, this is the noise occurring at the output under the specified conditions. In the case of the 8049, the noise is referred to the input.

SCALE FACTOR For the log amp, the scale factor (K) is the voltage change at the output for a decade (i. e. 10:1) change at the input. For the antilog amp, the scale factor is the voltage change required at the input to cause a one decade change at the output. See equations 9 and 10.

ORDERING INFORMATION

TYPE	PACKAGE	MAX. ABSOLUTE ERROR (25°C)	TEMPERATURE RANGE	ORDER PART NUMBER
8048 BC	16 Pin Ceramic DIP	30mV	0°C to +70°C	ICL 8048 BC DE
8048 BC	16 Pin Plastic DIP	30mV	0°C to +70°C	ICL 8048 BC PE
8048 CC	16 Pin Ceramic DIP	60mV	0°C to +70°C	ICL 8048 CC DE
8048 CC	16 Pin Plastic DIP	60mV	0°C to +70°C	ICL 8048 CC PE
8049 BC	16 Pin Ceramic DIP	10mV	0°C to +70°C	ICL 8049 BC DE
8049 BC	16 Pin Plastic DIP	10mV	0°C to +70°C	ICL 8049 BC PE
8049 CC	16 Pin Ceramic DIP	25mV	0°C to +70°C	ICL 8049 CC DE
8049 CC	16 Pin Plastic DIP	25mV	0°C to +70°C	ICL 8049 CC PE

ICL8063

Power Transistor Driver-Amplifier

FEATURES:

- **Converts ±12V Outputs from Op Amps and other linear functions to ±30V levels**
- **When used in conjunction with general-purpose op amps and external complementary power transistors, system can deliver > 50 Watts to external loads**
- **Has built-in Safe Area Protection and short-circuit protection**
- **Produces 25mA quiescent current in power amp configuration while delivering ±2 Amps output current**
- **Has built in ±13V Regulators to power op amps or other external functions**

500kΩ input impedance with R_{BIAS} = 1MΩ

GENERAL DESCRIPTION

The ICL8063 is a unique monolithic power transistor driver and amplifier that allows construction of minimum chip power amplifier systems, complete with built in safe operating area circuitry, short circuit protection and voltage regulators. It is primarily intended for complementary symmetrical outputs.

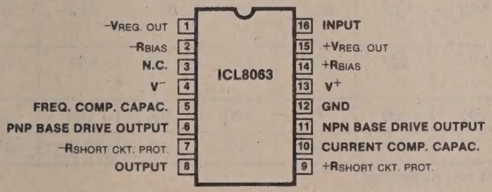
Designed to operate with all varieties of operational amplifiers and other functions, two external power transistors of any construction technique, and 8 to 10 passive components, the ICL8063 is ideal for use in such applications as linear and rotary actuator drivers, stepper motor drivers, servo motor drivers, power supplies, power DACs and electronically controlled orifices.

The ICL8063 takes the output levels (typically ±11V) from an op amp and boosts them to ±30V to drive power transistors, (e.g. 2N3055 (NPN) and 2N3789 (PNP)). The outputs from the ICL8063 supply up to 100mA to the base leads of the external power transistors.

This amplifier-driver contains internal positive and negative regulators, to drive an op amp or numerous other functions; thus, only ±30V supplies are needed for a complete power amp.

The ICL8063 provides built-in power supplies and will operate from inputs generated by most of the op amps in use today—regardless of technology—as well as many other linear functions, such as timers, comparators and waveform generators. And it will drive almost all power transistors with breakdown voltages up to 70 volts.

PIN CONFIGURATION



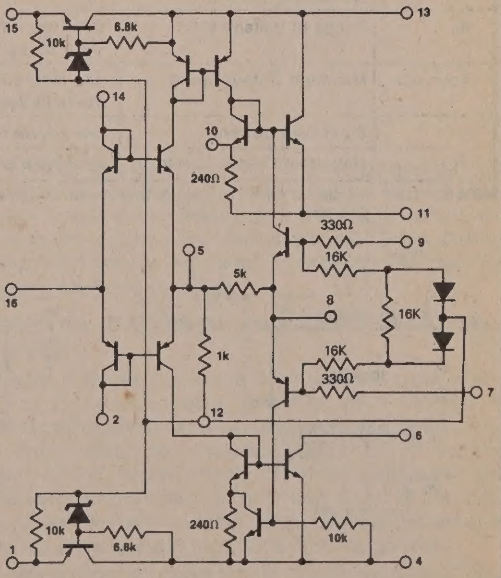
ICL8063
−VREG. OUT 1
−RBIAS 2
N.C. 3
V− 4
FREQ. COMP. CAPAC. 5
PNP BASE DRIVE OUTPUT 6
−RSHORT CKT. PROT. 7
OUTPUT 8
16 INPUT
15 +VREG. OUT
14 +RBIAS
13 V+
12 GND
11 NPN BASE DRIVE OUTPUT
10 CURRENT COMP. CAPAC.
9 +RSHORT CKT. PROT.

(outline dwg JE, PE)

ORDERING INFORMATION

ICL8063MJE	- CERDIP, −55°C TO 125°C
ICL8063CJE	- CERDIP, 0°C TO +70°C
ICL8063CPE	- PLASTIC DIP, 0°C TO 70°C

SCHEMATIC DIAGRAM



15
10k
6.8k
13
14
10
240Ω
11
330Ω
9
16K
5
5k
16
8
16K
1k
16K
330Ω
7
2
12
6
10k
6.8k
240Ω
10k
1
4

ABSOLUTE MAXIMUM RATINGS @ T_A = 25°C

Supply Voltage	±35V
Power Dissipation	500mW
Input Voltage (Note 1)	±30V
Operating Temperature Range	ICL8063MJE −55°C to +125°C ICL8063CPE 0°C to 70°C ICL8063CJE 0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Regulator Output Currents	10 mA

Note 1: For supply voltages less than ±30V the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C; V_{SUPP} = ±30V)

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN/MAX LIMITS						UNITS
			ICL8063M			ICL8063C			
			−55°C	+25°C	+125°C	0°C	+25°C	+70°C	
V_{OS}	Max. Offset Voltage	See Figure 1	150	50	50	150	75	75	mV
I_{OH}	Min. Positive Drive Current	See Figure 2	50	50	50	40	40	40	mA
I_{OQ}	Max. Positive Output Quiescent Current	See Figure 3	500	250	250	600	300	300	μA
I_{OL}	Min. Negative Drive Current	See Figure 2	25	25	25	20	20	20	mA
I_{QL}	Max. Negative Output Quiescent Current	See Figure 4	500	250	250	600	300	300	μA
$V_{\pm REG}$	Regulator Output Voltages Range	See Figure 5	±13.7 ±1.2V	±13.7 ±1.0V	±13.7 ±1.5V	±13.7 ±1.0V	±13.7 ±1.0V	±13.7 ±1.0V	V
Z_{IN}	A.C. Input Impedance	See Figure 6	400	400	400	400	400	400	kΩ
V_{SUPP}	Power Supply Range		±5 to ±35V						V
I_Q	Power Supply Quiescent Currents		10	6	6	12	7	7	mA
A_V	Range of Voltage Gain	See Figure 7 V_{IN} = 8Vp-p	6±2	6±2	6±2	6±2	6±2	6±2	V/V
$V_{OUT(MIN)}$	Minimum Output Swing	See Figure 7; Increase V_{IN} until V_{OUT} flattens	±27	±27	±27	±27	±27	±27	V
I_{IN}	Input Bias Current	See Figure 8	100	100	100	100	100	100	μA
I_{REG}	Regulator Output Current	(See Note 2)	10	10	7	10	10	7	mA

Note 2: Care should be taken to ensure that maximum power dissipation is not exceeded.

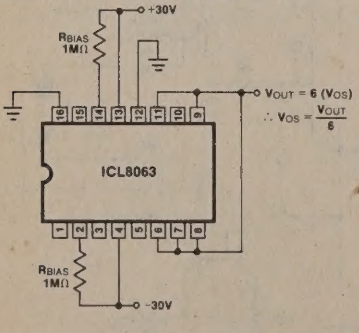
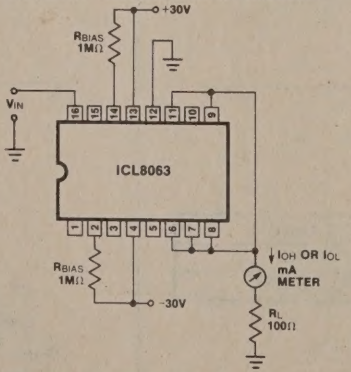


Figure 1: Offset Voltage Measurement



FOR I_{OUT}: V_{IN} IS POSITIVE: INCREASE V_{IN} UNTIL I_{OUT} LIMITS
FOR I_{OUT}: V_{IN} IS NEGATIVE: INCREASE V_{IN} UNTIL I_{OUT} LIMITS

Figure 2: Output Current Measurement

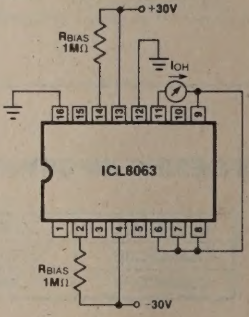


Figure 3: Positive Output Quiescent Current

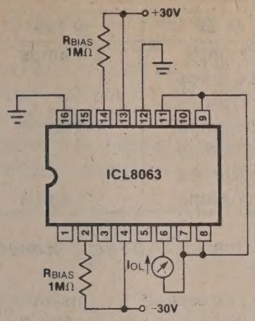

+30V
RBIAS 1MΩ
16 15 14 13 12 11 10 9
ICL8063
1 2 3 4 5 6 7 8
IOL
RBIAS 1MΩ
-30V

Figure 4: Negative Output Quiescent Current

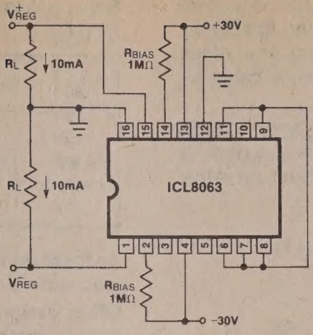

V+REG
RL
10mA
RBIAS 1MΩ
+30V
ICL8063
RL
10mA
V-REG
RBIAS 1MΩ
-30V

Figure 5: On Chip Regulator Measurement

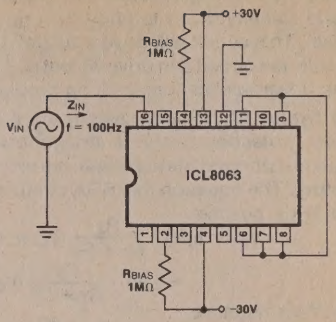

+30V
RBIAS 1MΩ
ZIN
VIN
f = 100Hz
ICL8063
RBIAS 1MΩ
-30V

Figure 6: A.C. Input Impedance Measurement

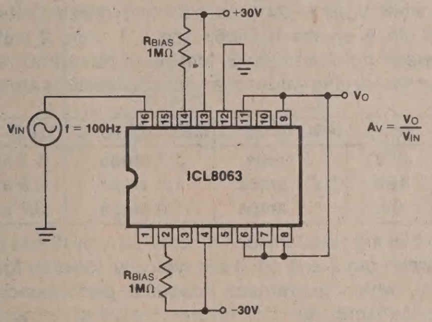

+30V
RBIAS 1MΩ
VO
VIN
f = 100Hz
AV = VO/VIN
ICL8063
RBIAS 1MΩ
-30V

Figure 7: Gain and Output Voltage Swing Measurement

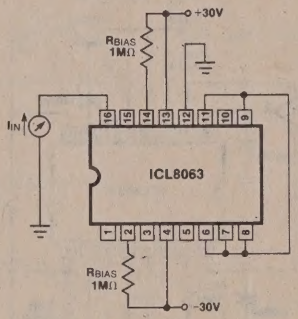

+30V
RBIAS 1MΩ
IIN
ICL8063
RBIAS 1MΩ
-30V

Figure 8: Input Bias Current Measurement

APPLICATION

One problem faced almost every day by circuit designers is how to interface low voltage, low current output world of standard linear and digital devices to that of power transistors and darlingtons—higher by several orders of magnitude.

For example, a low level op amp has a typical voltage range of ±6 to ±12V, and output current usually on the order of about 5 milliamperes. A power transistor with a ±35 volt supply, a collector current of 5 amperes, and a beta, or gain of 100 needs at least 50 milliamperes of drive.

In the past, connecting two transistors with widely dissimilar requirements meant that a rather ornate discrete circuit had to be built to convert the weak output signals from the first into levels large enough to drive the second. However, in addition to converting voltage and current, it was also necessary to include a number of protection circuits to guard against damage from shorts, for example, and all this design work was both tedious and expensive.

The ICL8063 provides a solution to these problems. It's a monolithic power transistor driver and power transistor amplifier circuit on the same chip, has all the necessary safe operating area circuitry and short circuit protection, and has on-chip ±13V voltage regulators to eliminate the need for extra external power supplies.

1. Using the ICL8063 to make a complete Power Amplifier

As Figure 9 shows, using the ICL8063 allows the circuit designer to build a power amplifier block capable of delivering ±2 amperes at ±25 volts (50 watts) to any load, with only three additional discrete devices and 8 passive components. Moreover, the circuit draws only about ±30 milliamperes of quiescent current from either of the ±30V power supplies. A similar design using discrete components would require anywhere from 50 to 100 components.

Slew rate is about the same as that of a 741 op amp, except that the output current can slew up to 2 amps at roughly 1V/μs (that's a 10 ohm load to ground and ±20V output across this resistance). Input current, voltage offset, CMRR and PSRR are also the same. Use of 1,000 picofarad compensation capacitors (three in this configuration) allows good stability down to unity gain non-inverting (the worst case). This circuit will drive a 1000pF C_L to Gnd, or in other words, the circuit can drive 30 feet of RG-58 coaxial cable for line driver applications with no problems.

As Figure 10 indicates, setting up a current limiting (safe area) protection circuit is straightforward. The 0.4 ohm, 5 watt resistors set the maximum current one can get out of the output. The equation this SOA circuit follows is:

for V_{OUT} positive,

$$V_{be} = I_L R_3 - \frac{R_2}{R_1 + R_2}(V_{OUT} + I_L R_3 - 0.7V)$$

$$\approx I_L R_3 - \frac{R_2}{R_1 + R_2}(V_{OUT})$$

for V_{OUT} negative,

$$V_{be} = I_L R_3 - \frac{R_2}{R_1 + R_2 + R_4}(V_{OUT} + I_2 R_3 + 0.7)$$

$$\approx I_L R_3 - \frac{R_2}{R_1 + R_2 + R_4}(V_{OUT})$$

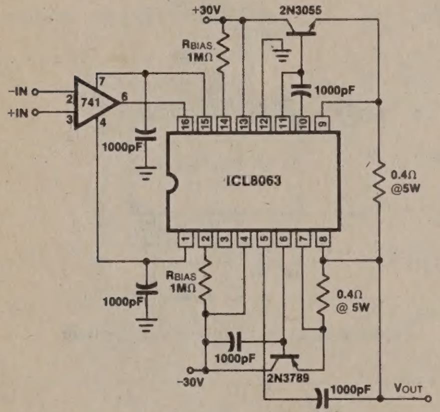

+30V
2N3055
RBIAS 1MΩ
1000pF
-IN
+IN
741
2
3
7
6
4
16
15
14
13
12
11
10
9
1000pF
ICL8063
0.4Ω @5W
1
2
3
4
5
6
7
8
RBIAS 1MΩ
1000pF
0.4Ω @ 5W
1000pF
-30V
2N3789
1000pF
VOUT

Figure 9: Standard Circuit Diagram

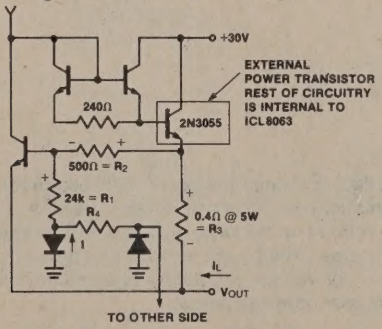

+30V
EXTERNAL POWER TRANSISTOR REST OF CIRCUITRY IS INTERNAL TO ICL8063
240Ω
2N3055
-
+
500Ω = R2
+
24k = R1
R4
I
+
0.4Ω @ 5W = R3
-
IL
VOUT
TO OTHER SIDE

Figure 10: Current Limiting (Safe Area) Protection Circuit (one side shown)

Solving these equations we get the following:

V_{OUT}	I	I_L @ 25°C	I_L @ 125°C
24V	1mA	3 amps	2.4 amps
20V	830μA	2.8 amps	
16V	670μA	2.6 amps	
12V	500μA	2.4 amps	1.8 amps
8V	333μA	2.1 amps	
4V	167μA	1.9 amps	
0V	0μA	1.7 amps	1.1 amps

As these equations indicate, maximum power delivered to a load is obtained when $V_{OUT} \geq 24V$.

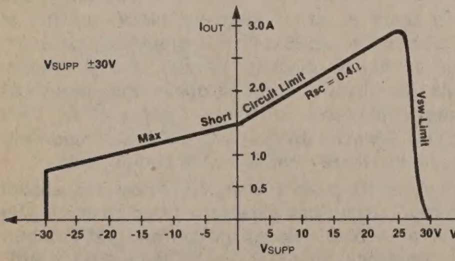
Often design requirements necessitate an unsymmetrical output current capability. In that case, instead of the 0.4 ohm resistors protecting the npn and pnp output stages, as shown in Figure 9, simply substitute any other value. For example, if up to 3 amps are required when $V_{OUT} \geq +24V$ and only 1 amp out when $V_{OUT} \geq -24V$, use a 0.4 ohm resistor between pin 8 and pin 9 on the ICL8063 and a 1 ohm, 2 watt resistor between pin 7 and pin 8. Maximum output current versus V_{OUT} for varying values of protection resistors are as follows:

V_{OUT}	0.4Ω @ 25°C	0.68Ω @ 25°C	1Ω @ 25°C
24V	3 amps	1.7 amps	1.2 amps
12V	2.4 amps	1.4 amps	0.9 amps
0V	1.7 amps	1.0 amps	0.7 amps

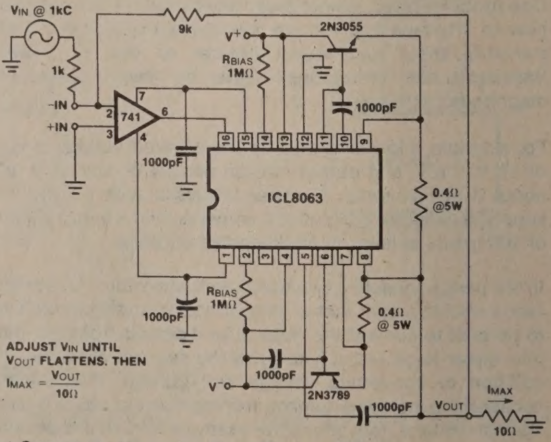
The biasing resistors located between pin 13 and pin 14 and between pin 2 and pin 4 are typically 1M-ohm for V_{SUPP} = ±30V, which guarantees adequate performance in such applications as DC motor drivers, power DACs, programmable power supplies and line drivers (with ±30 volt supplies). The table that follows shows the proper value for R_{BIAS} for optimum output current capability with supply voltages between ±5V and ±30V.

$\pm V_{CC}$	R_{BIAS}
30V	1 MΩ
25V	680kΩ
20V	500kΩ
15V	300kΩ
10V	150kΩ
5V	62kΩ

If 30V and 1 meg ohms are used, performance curves appear as shown in Figure 11.



Source Current only is shown. Sink Current is identical with Reversed Scales.


VIN @ 1kC
9k
1k
V+
2N3055
RBIAS 1MΩ
1000pF
-IN
+IN
741
2
3
7
6
4
16
15
14
13
12
11
10
9
1000pF
ICL8063
0.4Ω @5W
1
2
3
4
5
6
7
8
RBIAS 1MΩ
1000pF
0.4Ω @ 5W
1000pF
V-
2N3789
1000pF
VOUT
IMAX
10Ω

ADJUST V_{IN} UNTIL V_{OUT} FLATTENS. THEN $I_{MAX} = \frac{V_{OUT}}{10\Omega}$

Figure 11: Typical Performance Curve of Max. Output Current Vs. V_{SUPP} For Fixed R_{BIAS} = 1MΩ

When buying external power transistors, careful attention should be paid to beta values. For 2N3055 and 2N3789 transistors used in this circuit, beta should be no more than 150 max at $I_C = 20mA$ and $V_{CE} = 30V$. This beta value sets the quiescent current at less than 30mA when not delivering power to a load.

The design in Figure 9 will tolerate a short to ground indefinitely, provided adequate heat sinking is used. However if V_{OUT} is shunted to ±30V the output transistors (2N3055 and 2N3789) will be destroyed, but since the safe operating area for these devices is 4 amps at 30 volts, the problem does not occur for $V_{SUPP} = \pm15V$.

A typical bode plot of the power amplifier system is shown in Figure 12. Referring to Figure 6, the schematic for this bode plot is shown below:

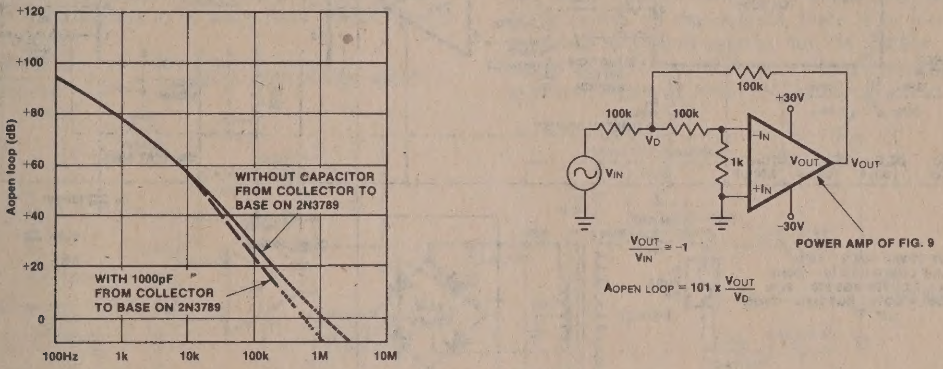


Figure 12: Bode Plot of Open Loop Gain of Above Schematic

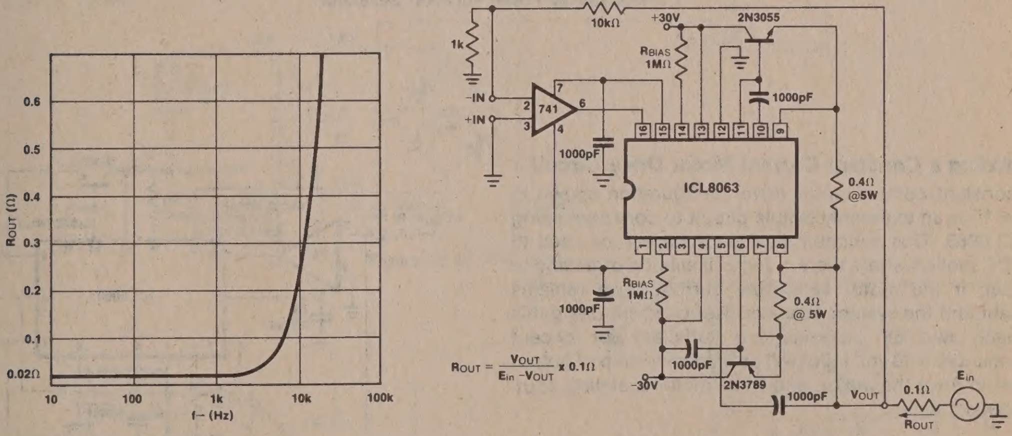


Figure 13: Typical Performance of R_{OUT} vs. Frequency of Power Amplifier System

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2. Designing A Simple Function Generator

Using a variation of the fundamental power amplifier building block described in the previous section, the ICL8063 can be implemented in the design of a simple, low cost function generator (Figure 14). It will supply sine waves, triangular waves and square waves from 2 hertz to 20 kilohertz. This complete test instrument can be plugged into a standard 110VAC line for power. V_{OUT} will be up to ±25V (50V p-p) across loads as small as 10 ohms (about 2.5 amps maximum output current).

Capacitor working voltages should be greater than 50V DC and all resistors should be 1/2W, unless otherwise indicated. The interconnecting leads from the 741 pins 2 and 3 to their respective resistors should be kept short, less than 2 inches if possible; longer leads may result in oscillation.

Full output swing is possible to about 5KHz; after that the output begins to taper off due to the slew rate of the 741, until at 20KHz the output swing will be about $20V_{pp}$ (±10V). This problem can be remedied by simply using an op amp with a higher slew rate, such as the LF156.

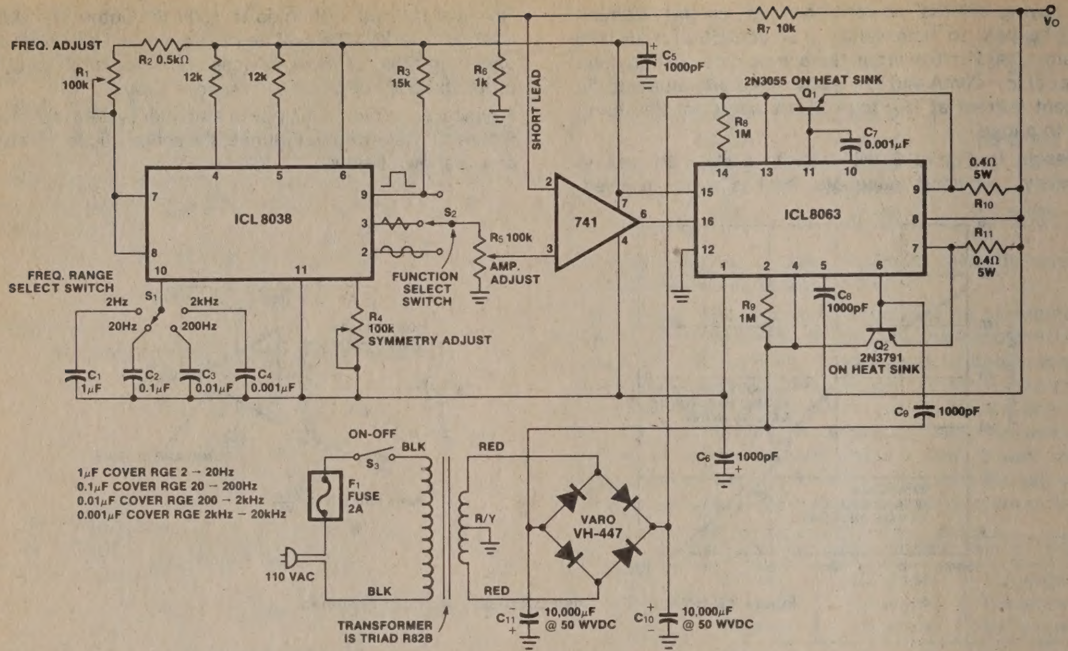

FREQ. ADJUST
R2 0.5kΩ
R1 100k
12k
12k
R3 15k
R6 1k
SHORT LEAD
R7 10k
C5 1000pF
Vo
2N3055 ON HEAT SINK
Q1
R8 1M
C7 0.001µF
14 13 11 10
15
16
12
9
8
7
1 2 4 5 6
ICL8063
0.4Ω 5W
R10
R11
0.4Ω 5W
ICL 8038
4 5 6
7
9
3
2
8
10
11
S2
R5 100k
AMP. ADJUST
FUNCTION SELECT SWITCH
741
R4 100k SYMMETRY ADJUST
FREQ. RANGE SELECT SWITCH
S1
2Hz
2kHz
20Hz
200Hz
C1 1µF
C2 0.1µF
C3 0.01µF
C4 0.001µF
R9 1M
C8 1000pF
Q2 2N3791 ON HEAT SINK
C9 1000pF
C6 1000pF
ON-OFF
S3
BLK
RED
F1 FUSE 2A
1µF COVER RGE 2 → 20Hz
0.1µF COVER RGE 20 → 200Hz
0.01µF COVER RGE 200 → 2kHz
0.001µF COVER RGE 2kHz – 20kHz
R/Y
VARO VH-447
110 VAC
BLK
RED
TRANSFORMER IS TRIAD R828
C11 10,000µF @ 50 WVDC
C10 10,000µF @ 50 WVDC

Figure 14: Power Function Generator

3. Building a Constant Current Motor Drive Circuit

The constant current motor drive configuration shown in Figure 15 is an extremely simple circuit to construct using the ICL8063. This minimum device circuit can be used to drive DC motors where there is some likelihood of stalling or lock up; if the motor locks, the current drive remains constant and the system does not destroy itself. Using this approach two 6V batteries are sufficient for decent performance. A 10 volt input will produce one amp of output current to drive the motor, and if the motor is stalled, I_{OUT} remains at 1 amp.

For example, suppose it's necessary to drive a 24V DC motor with 1 amp of drive current. First make V_{SUPP} at least 6 volts more than the motor being driven (in this case 30 volts). Next select R_{BIAS} according to V_{SUPP} from the data sheet, which indicates R_{BIAS} = 1MΩ. Then choose R_1, R_2, and R_a for optimum sensitivity. That means making $R_a = 1\Omega$ to minimize the voltage drop across R_a (the drop will be 1 amp x 1 ohm or 1 volt). If 1 amp/volt sensitivity is desirable let $R_2 = R_1 = 10\text{k}\Omega$ to minimize feedback current error. Then a ±1V input voltage will produce a ±1 amp current through the motor.

Capacitors should be at least 50 volts working voltage and all resistors 1/2W, except for those valued at 0.4 ohms, and R_a. Power across $R_a = I \times V = 1$ amp x 1 volt = 1 watt, so at least a 2 watt value should be used. Use large heat sinks for the 2N3055 and 2N3791 power transistors. A Delta NC-641 or the equivalent is appropriate. Use a thermal compound when mounting the transistor to the heat sink. (See Intersil ICH8510 data sheet).

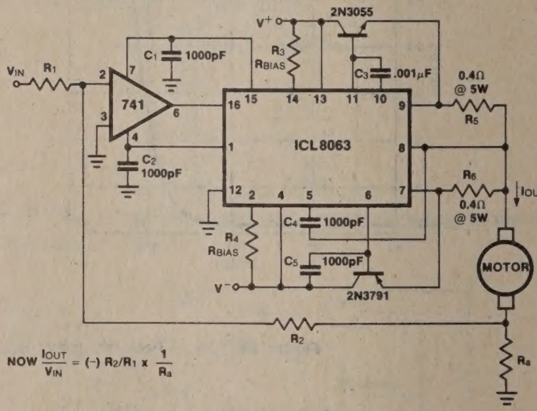

V+
2N3055
C1 1000pF
R3 RBIAS
VIN
R1
2
7
741
6
3
4
C2 1000pF
C3 .001µF
0.4Ω @ 5W
R5
16 15 14 13 11 10 9
ICL8063
1
8
12 2 4 5 6 7
R6
IOUT
0.4Ω @ 5W
C4 1000pF
R4 RBIAS
C5 1000pF
V−
2N3791
MOTOR
R2
Ra
NOW IOUT/VIN = (−) R2/R1 x 1/Ra

Figure 15: Constant Current Motor Drive

4. Building A Low Cost 8 ohm per channel Hi-fi Amplifier.

For about $20 per channel, it's possible to build a high fidelity amplifier using the ICL8063 to drive 8 ohm speakers. A channel is defined here as all amplification between turntable or tape output and power out. (Figure 16)

The input 741 stage is a preamplifier with R.I.A.A. equalization for records. Following the first 741 stage is a 10kΩ control pot, whose wiper arm feeds into the power amplifier stage consisting of a second 741, the ICL8063 and the power transistors. To achieve good listening results, selection of proper resistance values in the power amplifier stage is important. Best listening is to be found at a gain value of 6 $[(5k\Omega + 1k\Omega/1k\Omega = 6)]$. 3 is a practical minimum, since the first stage 741 preamp puts out only ±10 volt maximum signals, and if maximum power is necessary this value must be multiplied by 3 to get ±30 volt levels at the output of the power amp stage.

Each channel delivers about 56 volts p-p across an 8 ohm speaker and this converts to 50 watts RMS power. This is derived as follows:

$$\text{Power} = \frac{V_{rms}^2}{8\ \text{ohms}},\quad V_{rms} = \frac{56\text{V p-p}}{2.82} = 20\text{V},\ 20\text{V}^2 = 400\text{V}^2$$

$$\therefore \text{Power} = \frac{400^2}{8\ \text{ohms}} = 50 \text{ watts RMS Power.}$$

Distortion will be < 0.1% up to about 100Hz, and then it increases as the frequency increases, reaching about 1% at 20kHz.

The ganged switch at the input is for either disc playing or FM, either from an FM tuner or a tape amplifier. Assuming DC coupling on the outputs, there is no need for a DC reference to ground (resistor) for FM position. To clear the signal in the FM position, place a 51kΩ resistor to ground as shown in Figure 16 (from FM input position to ground).

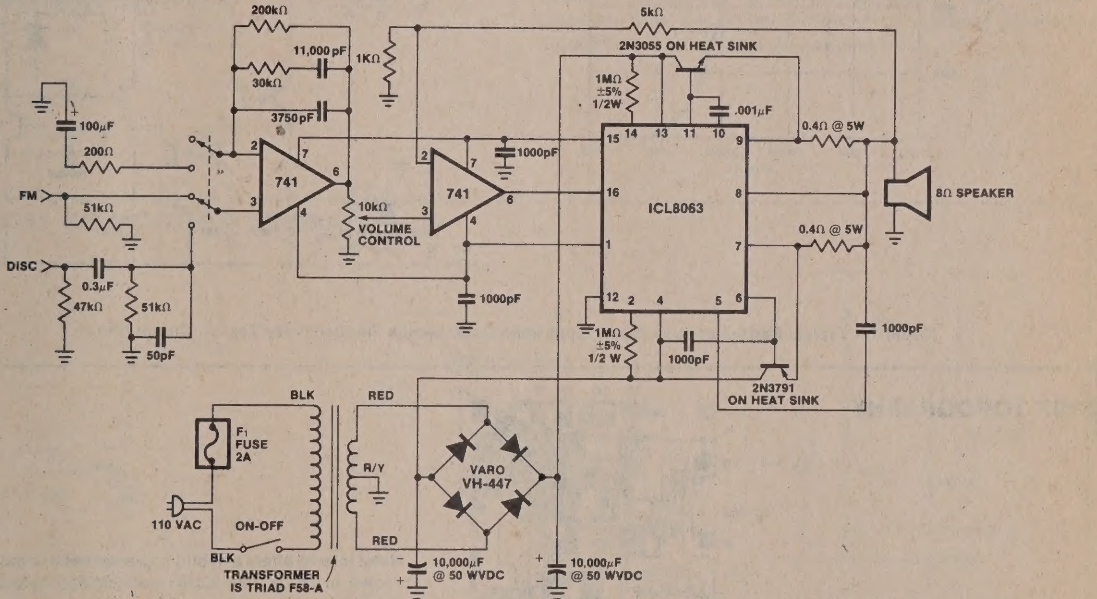

200kΩ
11,000pF
30kΩ
1kΩ
3750pF
5kΩ
2N3055 ON HEAT SINK
1MΩ ±5% 1/2W
.001μF
100μF
200Ω
FM
51kΩ
741
10kΩ VOLUME CONTROL
741
1000pF
ICL8063
0.4Ω @ 5W
8Ω SPEAKER
DISC
0.3μF
47kΩ
51kΩ
50pF
1000pF
1MΩ ±5% 1/2 W
1000pF
2N3791 ON HEAT SINK
1000pF
BLK
RED
F1 FUSE 2A
R/Y
VARO VH-447
110 VAC
ON-OFF
RED
BLK
TRANSFORMER IS TRIAD F58-A
10,000μF @ 50 WVDC
10,000μF @ 50 WVDC

Figure 16: Hi Fi Amplifier

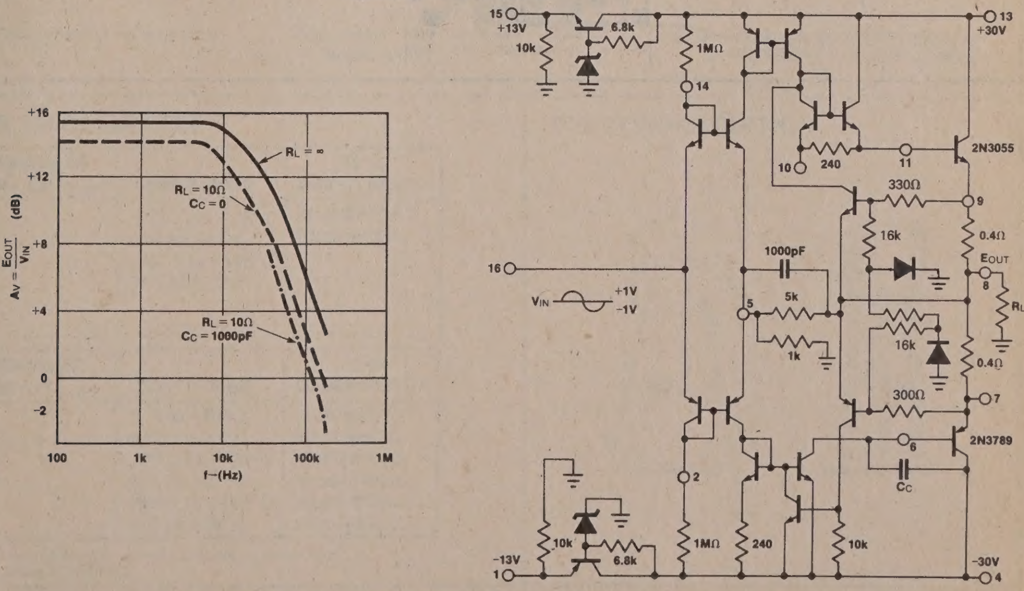


Figure 17: Typical Performance Curve of $\frac{E_{OUT}}{V_{IN}}$ vs. Frequency For Typical Circuit Shown

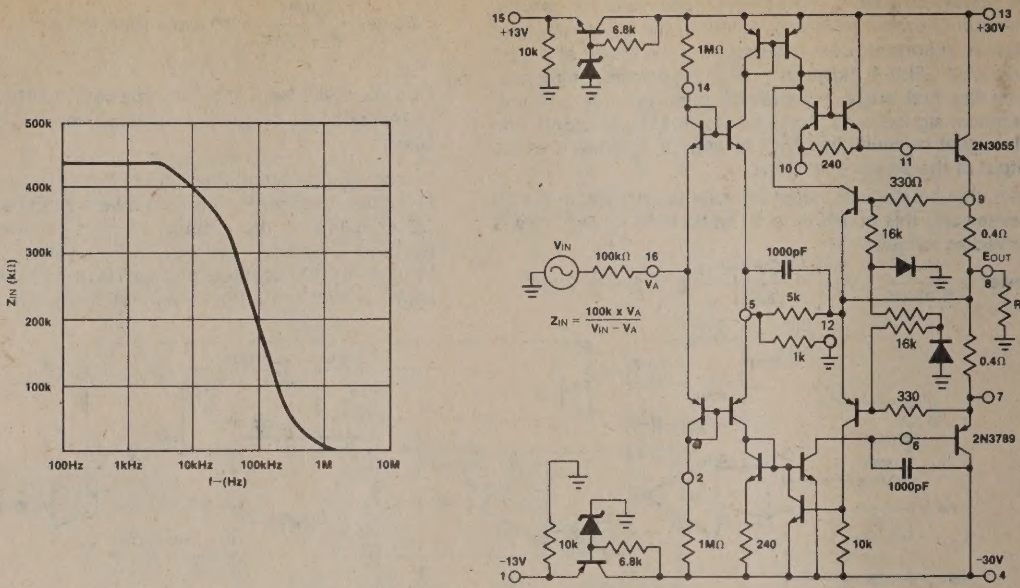
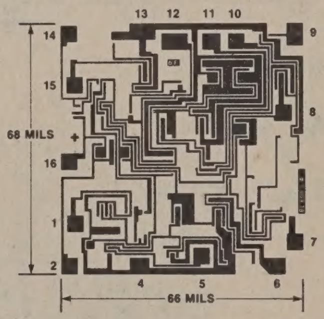


Figure 18: Typical Performance Curve of Input Impedance Versus Frequency for Typical Circuit Shown

CHIP TOPOGRAPHY


13
12
11
10
14
9
15
8
68 MILS
16
1
7
2
4
5
6
66 MILS

Note: Intersil offers a hybrid power amplifier similar to that shown in fig. 9. See ICH8510/8520/8530 data sheet for details.

INTERSIL

ICL8069 Series
Low Voltage Reference

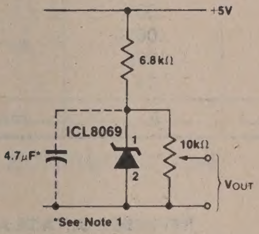
FEATURES

- **Temperature Coefficient guaranteed to 10 ppm/° C max.**
- **Low Bias Current . . . 50μA min**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

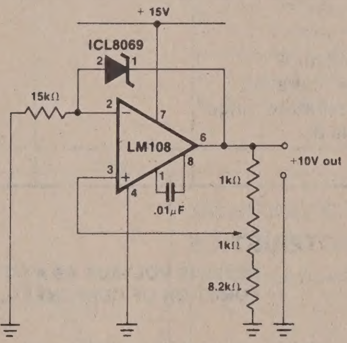
GENERAL DESCRIPTION

The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

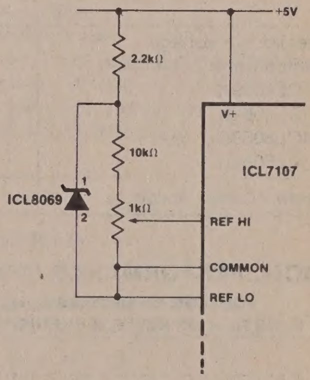
TYPICAL CONNECTION DIAGRAMS


+5V
6.8kΩ
ICL8069
1
2
4.7μF*
10kΩ
VOUT
*See Note 1

(a) Simple Reference (1.2 volts or less)


+15V
ICL8069
2
1
15kΩ
2
7
LM108
6
8
3
4
1
.01μF
+10V out
1kΩ
1kΩ
8.2kΩ

(b) Buffered 10V Reference using a single supply.


+5V
2.2kΩ
V+
10kΩ
ICL7107
ICL8069
1
2
1kΩ
REF HI
COMMON
REF LO

(c) Double regulated 100mV reference for ICL7107 one-chip DPM circuit.

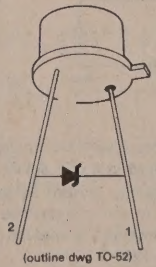
ORDERING INFORMATION

MAX. TEMPERATURE COEFFICIENT OF V_{REF}	TEMP RANGE	TO-92 ORDER PART #
.005 %/° C	−55° C to +125° C	ICL8069CCA
.005 %/° C	0° C to +70° C	ICL8069DCA
.01 %/° C	−55° C to +125° C	
.01 %/° C	0° C to +70° C	

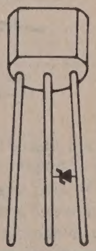
MAX. TEMPERATURE COEFFICIENT OF V_{REF}	TEMP RANGE	TO-52 ORDER PART #
.001%/° C	0° C to +70° C	ICL8069ACQ
.0025 %/° C	0° C to +70° C	ICL8069BCQ
.005 %/° C	−55° C to +125° C	ICL8069CMQ
.005 %/° C	0° C to +70° C	ICL8069CCQ
.01 %/° C	−55° C to +125° C	ICL8069DMQ
.01 %/° C	0° C to +70° C	ICL8069DCQ

NOTE: ICL8069DC and ICL8069DM are also available as dice. Order ICL8069DC/D and ICL8069DM/D

PIN CONFIGURATION



(outline dwg TO-52)



(outline dwg TO-92)

ABSOLUTE MAXIMUM RATINGS

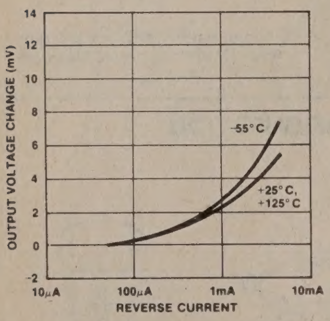
Reverse Voltage .... See Note 2
Forward Current 10mA
Reverse Current 10mA
Power Dissipation . Limited by max forward/reverse current
Storage Temperature .... −65° C to +200° C
Operating Temperature
ICL8069C .... 0° C to +70° C
ICL8069M .... −55° C to +125° C
Lead Temperature (Soldering, 10 Sec) .... 300° C

ELECTRICAL CHARACTERISTICS (@ 25° C unless otherwise noted)

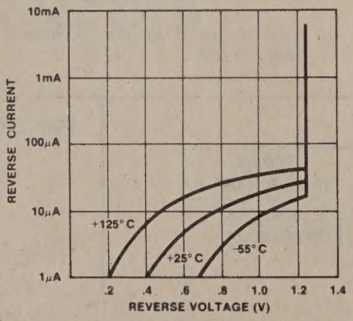
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse breakdown Voltage	$I_R = 500\mu A$	1.20	1.23	1.25	V
Reverse breakdown Voltage change	$50\mu A \leq I_R \leq 5mA$		15	20	mV
Reverse dynamic Impedance	$I_R = 50\mu A$ $I_R = 500\mu A$		1 1	2 2	Ω
Forward Voltage Drop	$I_F = 500\mu A$		.7	1	V
RMS Noise Voltage	$10Hz \leq f \leq 10kHz$ $I_R = 500\mu A$		5		μV
Breakdown voltage Temperature coefficient: ICL8069A ICL8069B ICL8069C ICL8069D	$I_R = 500\mu A$ T_A = operating temperature range (Note 3)			.001 .0025 .005 .01	%/° C
Reverse Current Range		.050		5	mA

TYPICAL PERFORMANCE CHARACTERISTICS

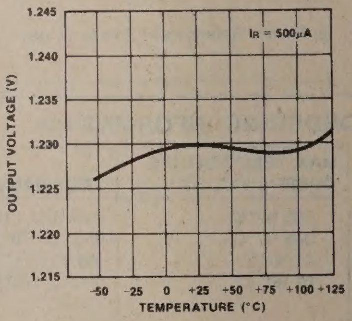
VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT



REVERSE VOLTAGE AS A FUNCTION OF CURRENT



REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE



Notes:

1) The diode should not be operated with shunt capacitances between 200pF and 0.22μF, as it may oscillate at some currents. If circuit strays in excess of 200pF are anticipated, a 4.7μF shunt capacitor will ensure stability under all operating conditions.
2) In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.
3) For the military part, measurements are made at 25° C, −55° C, and +125° C. The unit is then classified as a function of the worst case T.C. from 25° C to −55° C, or 25° C to +125° C.

INTERSIL

ICL8211, ICL8212

Programmable Voltage Reference

$2.95

FEATURES

- **High accuracy voltage sensing and generation: internal reference 1.15 volts typical**
- **Low sensitivity to supply voltage and temperature variations**
- **Wide supply voltage range: Typ. 1.8 to 30 volts**
- **Essentially constant supply current over full supply voltage range**
- **Easy to set hysteresis voltage range**
- **Defined output current limit - ICL8211**
  High output current capability - ICL8212

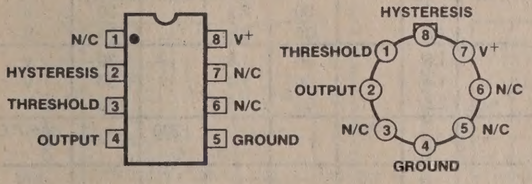
GENERAL DESCRIPTION

The Intersil ICL8211/12 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

Applications include:
1. Low voltage sensor/indicator
2. High voltage sensor/indicator
3. Non volatile out-of-voltage range sensor/indicator
4. Programmable voltage reference or zener diode
5. Series or shunt power supply regulator
6. Fixed value constant current source

PIN CONFIGURATION

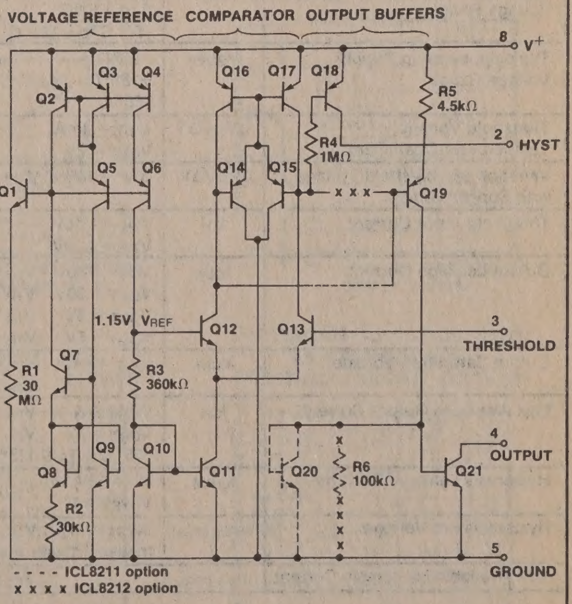

N/C 1
HYSTERESIS 2
THRESHOLD 3
OUTPUT 4
8 V+
7 N/C
6 N/C
5 GROUND
HYSTERESIS 8
THRESHOLD 1
7 V+
OUTPUT 2
6 N/C
N/C 3
5 N/C
4 GROUND

(outline dwg PA) (outline dwg TO-99)

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL8211CPA	0 to +70°C	8 lead Mini DIP
ICL8211CTY	0 to +70°C	TO-99 Can
ICL8211MTY	−55° to +125°C	TO-99 Can
ICL8212CPA	0 to 70°C	8 lead Mini DIP
ICL8212CTY	0 to 70°C	TO-99 Can
ICL8212MTY	−55 to +125°C	TO-99 Can
ICL8211D	Dice only	
ICL8212D	Dice only	

SCHEMATIC DIAGRAM


VOLTAGE REFERENCE
COMPARATOR
OUTPUT BUFFERS
8 V+
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
R1 30 MΩ
R2 30kΩ
R3 360kΩ
R4 1MΩ
R5 4.5kΩ
R6 100kΩ
1.15V VREF
2 HYST
3 THRESHOLD
4 OUTPUT
5 GROUND
- - - - ICL8211 option
x x x x ICL8212 option

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	–0.5 to +30 volts
Output Voltage	–0.5 to +30 volts
Hysteresis Voltage	+0.5 to –10 volts
Threshold Input Voltage	+30 to –5 volts with respect to GROUND and +0 to –30 volts with respect to V^+
Current into Any Terminal	±30mA
Power Dissipation (Note 1 & 2)	300mW
Operating Temperature Range ICL8211M/12M	–55°C to +125°C
Operating Temperature Range ICL8211C/12C	0 to +70°C
Storage Temperature Range	–65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Rating applies for case temperatures to 125°C to ICL8211MTY/12MTY products. Derate linearly at –10mW/°C for ambient temperatures above 100°C.

NOTE 2: Derate linearly above 50°C by –10mW/°C for ICL8211C/12C products. The threshold input voltage may exceed +7 volts for short periods of time. However for continuous operation this voltage must be maintained at a value less than 7 volts.

TYPICAL OPERATING CHARACTERISTICS (V^+ = 5V, T_A = 25°C unless otherwise specified)

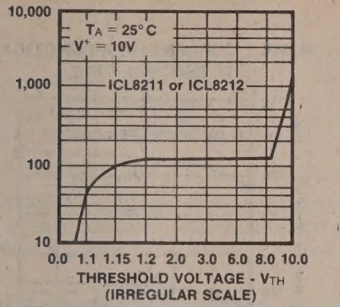
PARAMETER	SYMBOL	CONDITIONS	ICL8211			ICL8212			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I^+	$2.0 < V^+ < 30$							
		$V_T = 1.3V$	10	22	40	50	110	250	μA
		$V_T = 0.9V$	50	140	250	10	20	40	μA
Threshold Trip Voltage	V_{TH}	$I_{OUT} = 4mA$ $V^+ = 5V$	0.98	1.15	1.19	1.00	1.15	1.19	V
		$V_{OUT} = 2V$ $V^+ = 2V$	0.98	1.145	1.19	1.00	1.145	1.19	V
		$V^+ = 30V$	1.00	1.165	1.20	1.05	1.165	1.20	V
Threshold Voltage Disparity Between Output & Hysteresis Output	V_{THP}	$I_{OUT} = 4$ mA $V_{OUT} = 2V$ $I_{HYST} = 7\mu A$ $V_{HYST} = 3V$		–8.0			–0.5		mV
Guaranteed Operating Supply Voltage Range	V_{SUPP}	+25°C	2.0		30	2.0		30	V
		0 to +70°C	2.2		30	2.2		30	V
		–55°C to +125°C	2.8		30	2.8		30	V
Typical Operating Supply Voltage Range	V_{SUPP}	+25°C	1.8		30	1.8		30	V
		+125°C	1.4		30	1.4		30	V
		–55°C	2.5		30	2.5		30	V
Threshold Voltage Temperature Coefficient	$\Delta V_{TH}/\Delta T$	$I_{OUT} = 4mA$ $V_{OUT} = 2V$		+200			+200		ppm/°C
Variation of Threshold Voltage with Supply Voltage	$\Delta V_{TH}/\Delta V^+$	$\Delta V^+ = 10\%$ at $V^+ = 5V$		1.0			1.0		mV
Threshold Input Current	I_{TH}	$V_{TH} = 1.15V$		100	250		100	250	nA
		$V_{TH} = 1.00V$		5			5		nA
Output Leakage Current	I_{OLK}	$V_{OUT} = 30V$ $V_{TH} = 1.0V$						10	μA
		$V_{OUT} = 30V$ $V_{TH} = 1.3V$			10				μA
		$V_{OUT} = 5V$ $V_{TH} = 1.0V$						1	μA
		$V_{OUT} = 5V$ $V_{TH} = 1.3V$			1				μA
Output Saturation Voltage	V_{SAT}	$I_{OUT} = 4mA$ $V_{TH} = 1.0V$		0.17	0.4				V
		$V_{TH} = 1.3V$					0.17	0.4	V
Max Available Output Current	I_{OH}	(Note 3 & 4) $V_{TH} = 1.0V$	4	7.0	12			mA	
		$V_{OUT} = 5V$ $V_{TH} = 1.3V$				15	35		mA
		$-55°C \leq T_A \leq 125°C$ $V_{TH} = 1.0V$			15	12			mA
Hysteresis Leakage Current	I_{LHYS}	$V^+ = 10V$ $V_{TH} = 1.0V$ $V_{HYST} = V^-$			0.1			0.1	μA
Hysteresis Sat Voltage	$V_{HYS\,(max)}$	$I_{HYST} = -7\mu A$ $V_{TH} = 1.3V$ measured with respect to V^+		–0.1	–0.2		–0.1	–0.2	V
Max Available Hysteresis Current	$I_{HYS\,(max)}$	$V_{TH} = 1.3V$	–15	–21		–15	–21		μA

NOTE 3: The maximum output current of the ICL8211 is limited by design to 15ma under any operating conditions. The output voltage may be sustained at any voltage up to +30 as long as the maximum power dissipation of the device is not exceeded.

NOTE 4: The maximum output current of the ICL8212 is not defined, and systems using the ICL8212 must therefore ensure that the output current does not exceed 30ma and that the maximum power dissipation of the device is not exceeded.

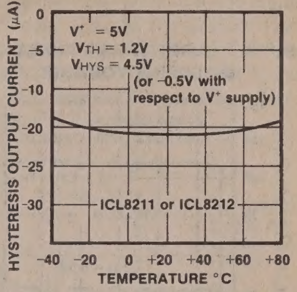
TYPICAL OPERATING CHARACTERISTICS

THRESHOLD INPUT CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



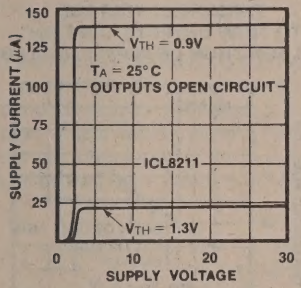
Characteristics common to both the ICL8211 and the ICL8212

HYSTERESIS OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE

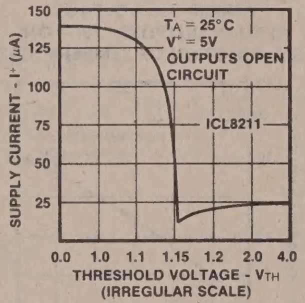


Characteristics ICL8211

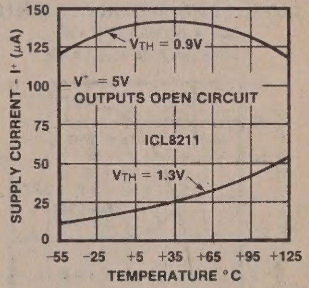
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



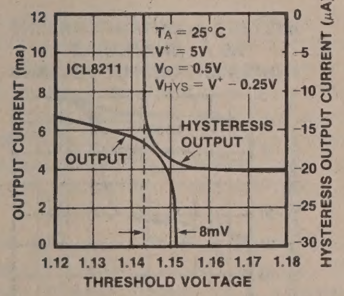
SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



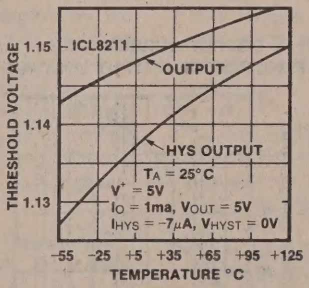
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



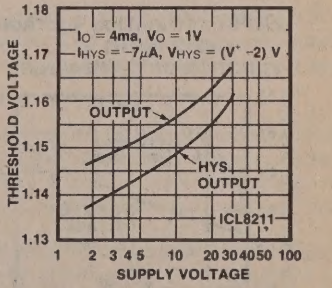
OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



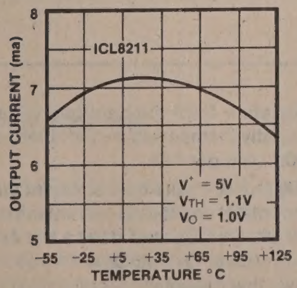
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



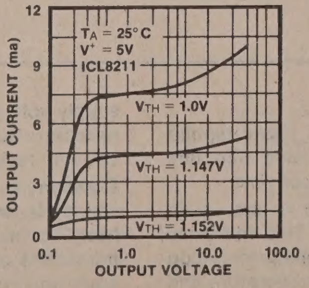
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



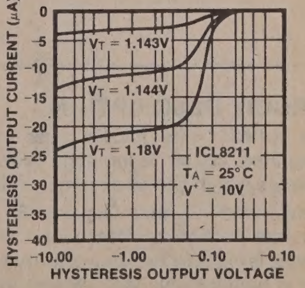
OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



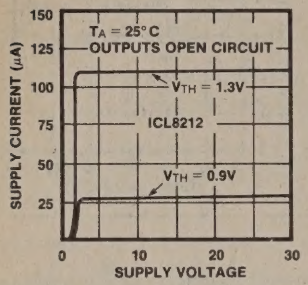
HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



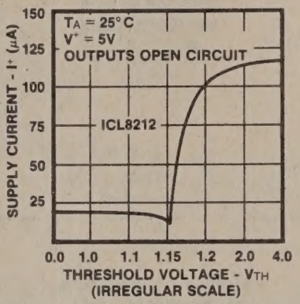
TYPICAL OPERATING CHARACTERISTICS

Characteristics ICL8212

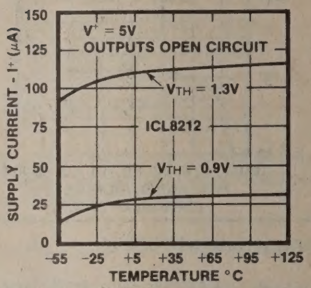
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



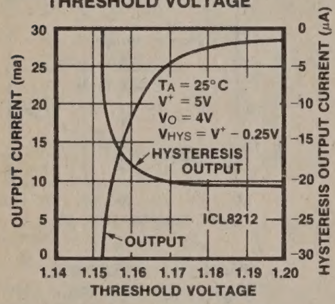
SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



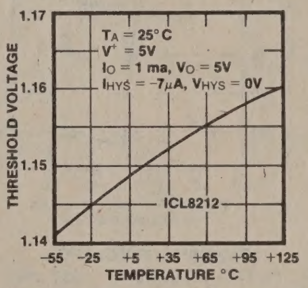
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



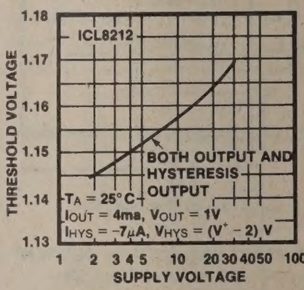
OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



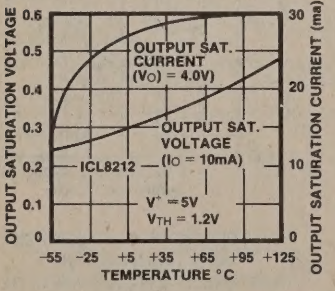
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



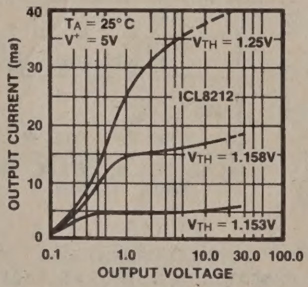
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



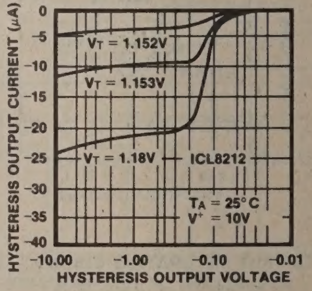
OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



CIRCUIT DESCRIPTION

The ICL8211 and ICL8212 use standard linear bipolar integrated circuit technology with high value thin film resistors which define extremely low value currents.

Components Q_1 thru Q_{10} and R_1, R_2 and R_3 set up an accurate voltage reference of 1.15 volts. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors (−5000 ppm per °C).

Components Q_2 thru Q_9 and R_2 make up a constant current source; Q_2 and Q_3 are identical and form a current mirror. Q_8 has 7 times the emitter area of Q_9, and due to the current mirror, the collector currents of Q_8 and Q_9 are forced to be equal and it can be shown that the collector current in Q_8 and

Q_9 is

$$I_C\,(Q_8 \text{ or } Q_9) = \frac{1}{R_2} \times \frac{kT}{q}\,\ell n\, 7$$

or approximately 1μA at 25°C

Where k = Boltzman's constant
q = charge on an electron
and T = absolute temperature in °K

Transistors Q_5, Q_6, and Q_7 assure that the V_{CE} of Q_3, Q_4, and Q_9 remain constant with supply voltage variations. This ensures a constant current supply free from variations.

The base current of Q_1 provides sufficient start up current for the constant current source; there being two stable states for this type of circuit - either ON as defined above, or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

Q_4 is matched to Q_3 and Q_2; Q_{10} is matched to Q_9. Thus the I_C and V_{BE} of Q_{10} are identical to that of Q_9 or Q_8. To generate the bandgap voltage, it is necessary to sum a voltage equal to the base emitter voltage of Q_9 to a voltage proportional to the difference of the base emitter voltages of two transistors Q_8 and Q_9 operating at two current densities.

$$\text{Thus } 1.15 = V_{BE}\,(Q_9 \text{ or } Q_{10}) + \frac{R_3}{R_2} \times \frac{kT}{q}\,\ell n\, 7$$

$$\text{which provides } \frac{R_3}{R_2} = 12 \text{ (approx.)}$$

The total supply current consumed by the voltage reference section is approximately 6μA at room temperature. A voltage at the THRESHOLD input is compared to the reference 1.15 volts by the comparator consisting of transistors Q_{11} thru Q_{17}. The outputs from the comparator are limited to two diode drops less than V^+ or approximately 1.1 volts. Thus the base current into the hysteresis output transistor is limited to about 500nA and the collector current of Q_{19} to 100μA.

In the case of the ICL8211, Q_{21} is proportioned to have 70 times the emitter area of Q_{20} thereby limiting the output current to approximaely 7mA, whereas for the ICL8212 almost all the collector current of Q_{19} is available for base drive to Q_{21}, resulting in a maximum available collector current of the order of 30mA. It is advisable to externally limit this current to 25mA or less.

APPLICATIONS

The ICL8211 and ICL8212 are similar in many respects, especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices, and where differences occur they are clearly noted.

1. GENERAL INFORMATION

THRESHOLD INPUT CONSIDERATIONS

Although any voltage between −5V and V^+ may be applied to the THRESHOLD terminal, it is recommended that the THRESHOLD voltage does not exceed about +6 volts since above that voltage the threshold input current increases sharply. Also, prolonged operation above this voltage will lead to degradation of device characteristics.

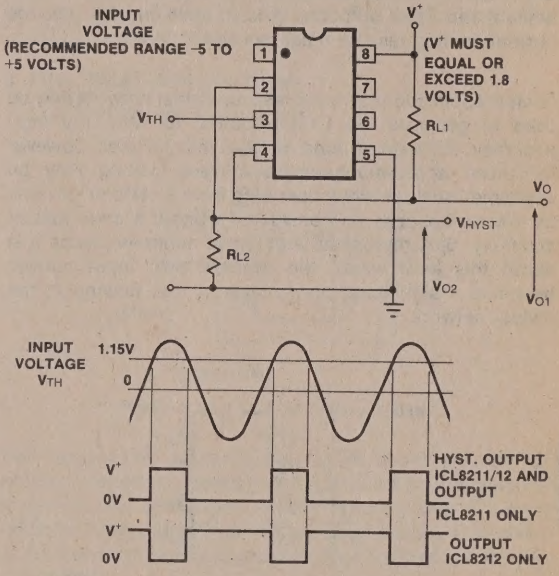

INPUT VOLTAGE (RECOMMENDED RANGE −5 TO +5 VOLTS)
V⁺
(V⁺ MUST EQUAL OR EXCEED 1.8 VOLTS)
1
2
3
4
5
6
7
8
VTH
RL1
RL2
VO
VHYST
VO2
VO1
INPUT VOLTAGE VTH
1.15V
0
V⁺
0V
V⁺
0V
HYST. OUTPUT ICL8211/12 AND OUTPUT ICL8211 ONLY
OUTPUT ICL8212 ONLY

Figure 1: Voltage Level Detection

The outputs change states with an input THRESHOLD voltage of approximately 1.15 volts. Input and output waveforms are shown in Figure 1 for a simple 1.15 volt level detector.

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to 10μA or less.

The regular OUTPUT's from either the ICL8211 or ICL8212 may be used to drive most of the common logic families such as TTL or C-MOS using a single pullup resistor. There is a guaranteed TTL fanout of 2 for the ICL8211 and 4 for the ICL8212.

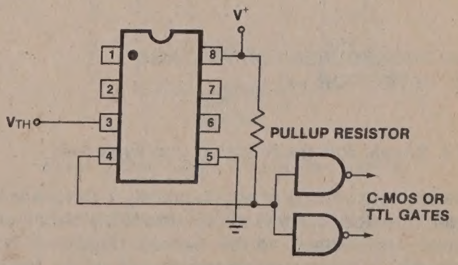


Figure 2: Output Logic Interface

A principal application of the ICL8211 is voltage level detection, and for that reason the OUTPUT current has been limited to typically 7mA to permit direct drive of an LED connected to the positive supply without a series current limiting resistor.

On the other hand the ICL8212 is intended for applications such as programmable zener references, and voltage regulators where output currents well in excess of 7mA are desirable. Therefore, the output of the ICL8212 is not current limited, and if the output is used to drive an LED, a series current limiting resistor must be used.

In most applications an input resistor divider network may be used to generate the 1.15V required for V_{TH}. For high accuracy, currents as large as 50μA may be used, however for those applications where current limiting may be desirable, (such as when operating from a battery) currents as low as 6μA may be considered without a great loss of accuracy. 6μA represents a practical minimum, since it is about this level where the device's own input current becomes a significant percentage of that flowing in the divider network.

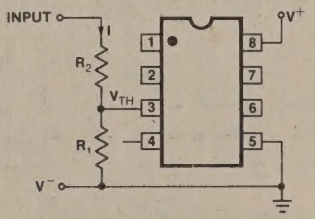


Figure 3: Input Resistor Network Considerations

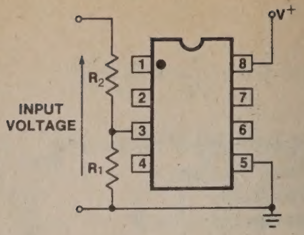
Case 1. High accuracy required, current in resistor network unimportant Set I = 50μA for V_{TH} = 1.15 volts ∴ R_1 → 20k ohms.

Case 2. Good accuracy required, current in resistor network important Set I = 7.5μA for V_{TH} = 1.15 volts ∴ R_1 → 150k ohms.

SETUP PROCEDURES FOR VOLTAGE LEVEL DETECTION

Case 1. Simple voltage detection - no hysteresis

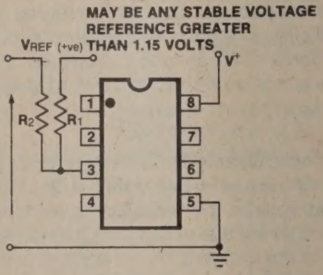
Unless an input voltage of approximately 1.15 volts is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 4 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity.



a) Range of input voltage greater than +1.15 volts.

Input voltage to change the output states

$$= \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts}$$



b) Range of input voltage less than +1.15 volts.

Input voltage to change the output states

$$= \frac{(R_1 + R_2) \times 1.15}{R_1} - \frac{R_2 V_{REF}}{R_1}$$

Figure 4: Input Resistor Network Setup Procedures

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 5.

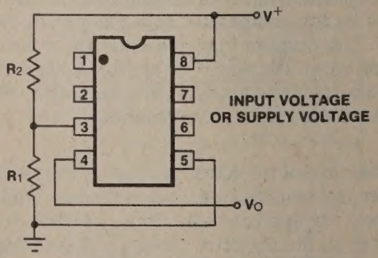


Figure 5: Combined Input and Supply Voltages

Conditions for correct operation of OUTPUT (terminal #4).

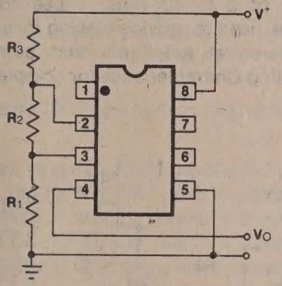
1. ICL8211
   $1.8V \le V^+ \le 30V$
2. ICL8212
   $0 \le V^+ \le 30V$

Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range where the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications - refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 6.

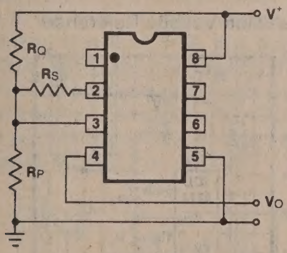


a) Low trip voltage

$$V_{TR1} = \left[\frac{(R_1 + R_2) \text{ X } 1.15}{R_1} + 0.1\right] \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \text{ X } 1.15 \text{ volts}$$



b) Low trip voltage

$$V_{TR1} = \left[\frac{R_Q R_S}{(R_Q + R_S)} + R_P\right] \text{ X } \frac{1}{R_P} \text{ X } 1.15 \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_P + R_Q)}{R_P} \text{ X } 1.15 \text{ volts}$$

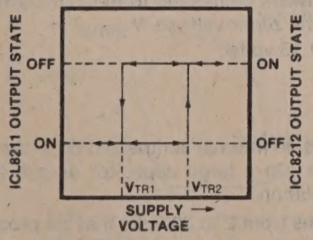


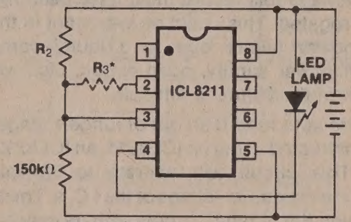
Figure 6: Two alternative voltage detection circuits employing hysteresis to provide pairs of well defined trip voltages.

Circuit (a) requires that the full current flowing in the resistor network be sourced by the HYSTERESIS output whereas for circuit (b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis circuit (b) is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESHOLD terminals thereby reducing the total external resistance between the THRESHOLD and GROUND when the OUTPUT is switched on.

3. PRACTICAL APPLICATIONS

a) Low Voltage Battery Indicator



*R3 OPTIONAL

Figure 7: Low Voltage Battery Indicator

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35μA which will increase to 7mA when the lamp is turned on. R3 will provide hysteresis if required.

b) |Non-Volatile| Low Voltage Detector

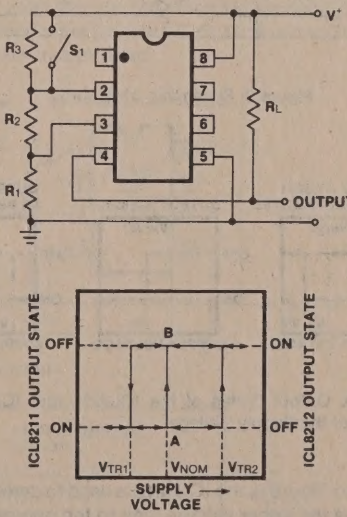


Figure 8: Low Voltage Detector and Memory

In this application the high trip voltage V_{TR2} is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S1 the operating point changes to B and will remain at B until the supply voltage drops below V_{TR1}, at which time the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V_{TR1} (even to zero volts) and then raised back to V_{NOM}.

c) (Non-volatile) Power Supply Malfunction Recorder

In many systems a transient or an extended abnormal (or absence of a) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

It is, therefore, necessary to be able to detect and store the fact that an **out-of-operating range** supply voltage condition has occurred, even in the case where a supply voltage may have dropped to zero. Upon power up to the normal operating voltage this record must have been retained and easily interrogated. This could be important in the case of a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.

A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30 volts without exceeding the maximum ratings of the I.C.'s. The two voltage limits defining the in range supply voltage may be set to any value between 2.0 and 30 volts.

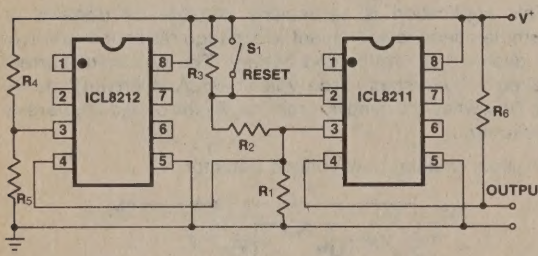


Figure 9: Schematic of Recorder

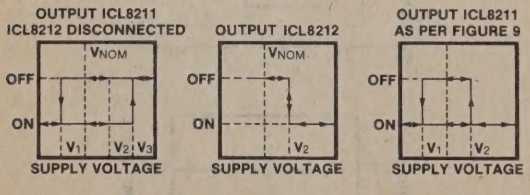


Figure 10: Output States of the ICL8211 and ICL8212 as a Function of the Supply Voltage

Referring to Figure 9, the ICL8212 is used to detect a voltage, V_2, which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range, V_1. Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range V_1 to V_2 by making V_3 - the upper trip point of the ICL8211 much higher in voltage than V_2.

The output of the ICL8212 is used to force the output of the ICL8211 into the ON state above V_2. Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out R_3 for values of supply voltage between V_1 and V_2.

d) Constant Current Sources

The ICL8212 may be used as a constant current source of value of approximately 25µA by connecting the THRESHOLD terminal to GROUND. Similarly the ICL8211 will provide a 130µA constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2 to 30 volts. These constant current sources may be used to provide biasing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

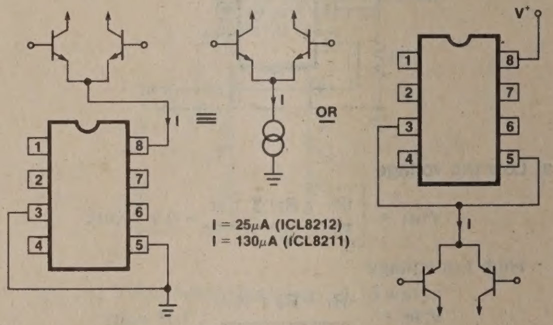


Figure 11: Constant Current Source Applications

e) Zener or Precision Voltage Reference

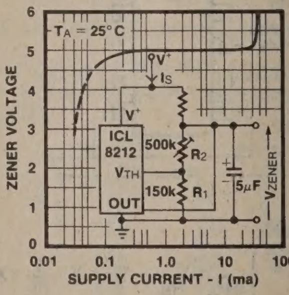


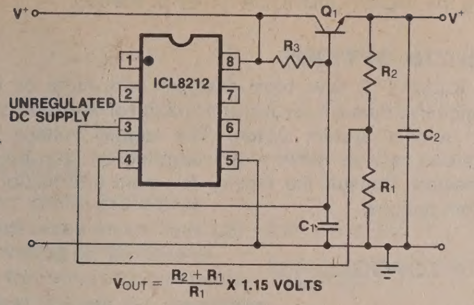
Figure 12: Programmable Zener or Voltage Reference

The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V_Z output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage ($V_{zener} = \frac{(R_1 + R_2)}{R_1} \times 1.15$ volts).

Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

Zener voltages from 2 to 30 volts may be programmed and typical impedance values between 300µA and 25mA will range from 4 to 7Ω. The knee is sharper and occurs at a significantly lower current than other similar devices available.

f) Precision Voltage Regulators


V+
Q1
V+
R3
ICL8212
R2
UNREGULATED DC SUPPLY
C2
R1
C1
1
2
3
4
5
6
7
8

$V_{OUT} = \frac{R_2 + R_1}{R_1} \times 1.15$ VOLTS

Figure 13: Simple Voltage Regulator

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed, using a resistor divider network R_1 and R_2. Two capacitors C_1 and C_2 are required to ensure stability since the ICL8212 is uncompensated internally.

This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

f) High supply voltage dump circuit

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5mA this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors R_1 and R_2 set up the disconnect voltage and R_3 provides optional voltage hysteresis if so desired.

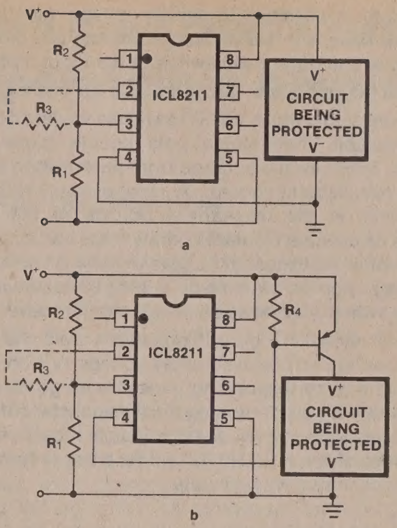
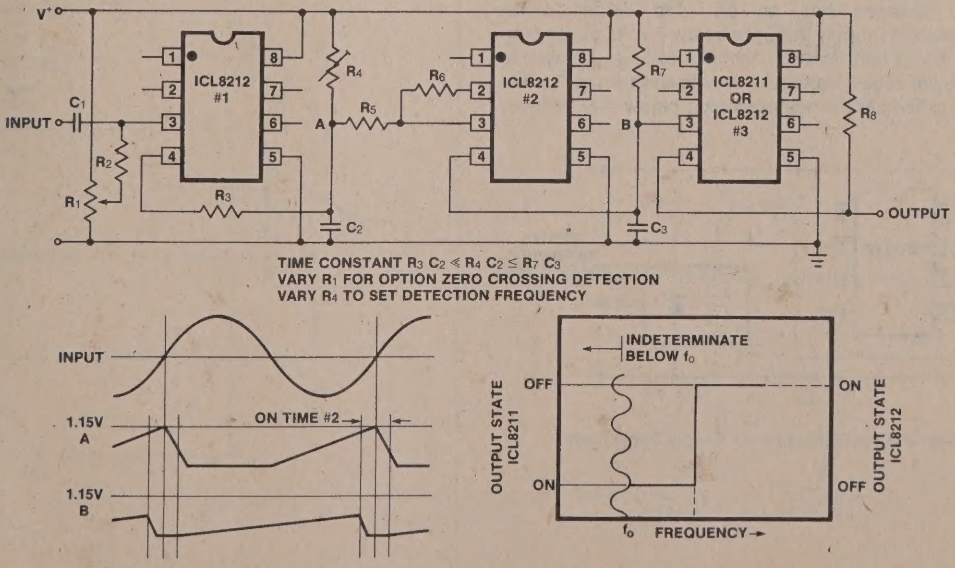

V+
R2
R3
R1
ICL8211
V+
CIRCUIT BEING PROTECTED
V−
a
V+
R2
R3
R1
ICL8211
R4
V+
CIRCUIT BEING PROTECTED
V−
b
1
2
3
4
5
6
7
8

Figure 14: High Voltage Dump Circuits

g) Frequency limit detectors

Simple frequency limit detectors providing a GO/NO-GO output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/12. In the application shown, the first ICL8212 is used as a zero crossing detector. The output circuit consisting of R_3, R_4 and C_2 results in a slow output positive ramp. The negative range is much faster than the positive range. R_5 and R_6 provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge C_3. The time constant of R_7 C_3 is much greater than R_4 C_2. Depending upon the desired output polarities for low and high input frequencies, either an ICL8211 or an ICL8212 may be used as the output driver.

5


V+
ICL8212 #1
ICL8212 #2
ICL8211 OR ICL8212 #3
C1
INPUT
R2
R1
R3
R4
R5
R6
R7
R8
C2
C3
A
B
OUTPUT
INPUT
1.15V A
ON TIME #2
1.15V B
INDETERMINATE BELOW fo
OFF
ON
ON
OFF
OUTPUT STATE ICL8211
OUTPUT STATE ICL8212
fo
FREQUENCY

TIME CONSTANT $R_3 C_2 \ll R_4 C_2 \leq R_7 C_3$
VARY R_1 FOR OPTION ZERO CROSSING DETECTION
VARY R_4 TO SET DETECTION FREQUENCY

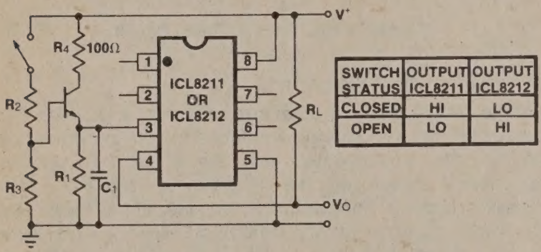
Figure 15: Frequency Limit Detector

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.

h) Switch bounce filter

Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches. SPST switches range from push button and slide types to calculator keyboards. A major problem with the use of switches is the mechanical bounce of the elctrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times.

The circuit shown in Figure 16 provides a rapid charge up of C_1 to close to the positive supply voltage (V^+) on a switch closure and a corresponding slow discharge of C_1 on a switch break. By proportioning the time constant of $R_1 C_1$ to approximately the manufacturer's bounce time the output as terminal #4 of the ICL8211/12 will be a single transition of state per desired switch closure.



SWITCH STATUS	OUTPUT ICL8211	OUTPUT ICL8212
CLOSED	HI	LO
OPEN	LO	HI

Figure 16: Switch Bounce Filter

j) Low voltage power disconnector

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9 volts causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9 volts and turn the power supply off to the LM199 heater section below that voltage.

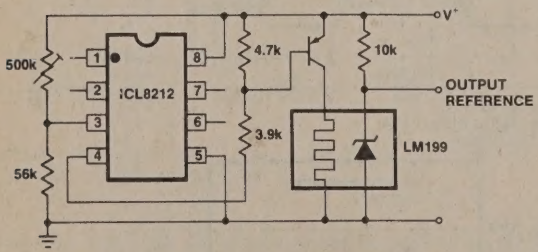


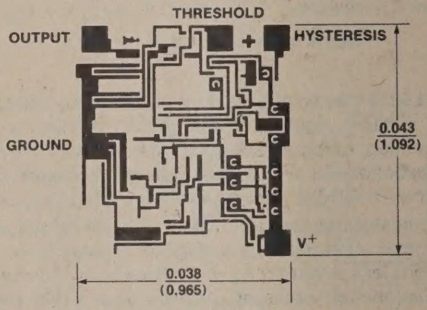
Figure 17: Low Voltage Power Supply Disconnect

For further applications, see A027 "Power Supply Design using the ICL8211 and ICL8212" by D. Watson.

CUSTOM OPTIONS

The ICL8211/12 have been designed with more on chip components than are used, in anticipation of more dedicated high volume system usage. The trigger voltage and hysteresis resistor network is integrated on chip but not connected. Consult the factory for more information on custom options.

CHIP TOPOGRAPHY



DIE IS PASSIVATED WITH A DEPOSITED OXIDE. BONDING PAD OXIDE WINDOWS ARE 3.6 x 3.6 MILS SQUARE.

INTERSIL

ICH8500/A
Ultra Low Bias Current Operational Amplifier

FEATURES

- **Input diode protection**
- **Input bias current less than 0.01 pA at all operating temperatures**
- **No frequency compensation required**
- **Offset voltage null capability**
- **Short circuit protection**
- **Low power consumption**

APPLICATIONS

- **Femto Ammeter**
- **Electrometers**
- **Long time integrators**
- **Flame detectors**
- **pH meter**
- **Proximity detector**
- **Sample and Hold Circuits**

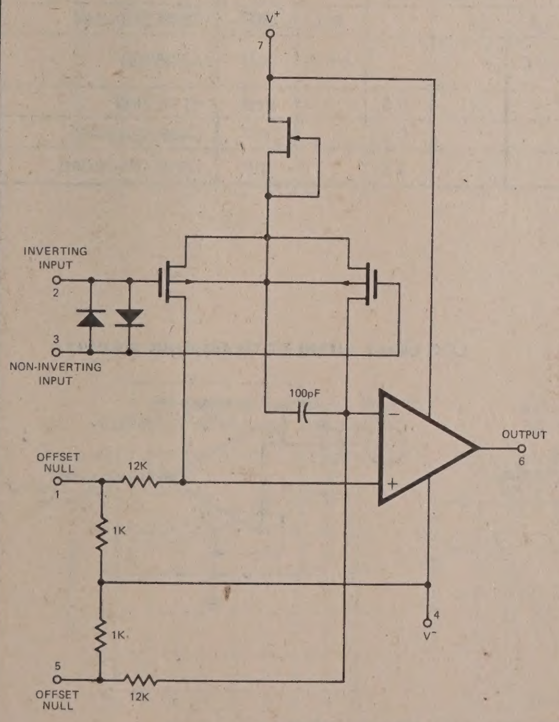
GENERAL DESCRIPTION

The ICM8500 and ICH8500A are hybrid circuits designed for ultra low input bias current operational amplifier applications. They are ideally suited for analog and electrometer applications where high input resistance and low input current are of prime importance.

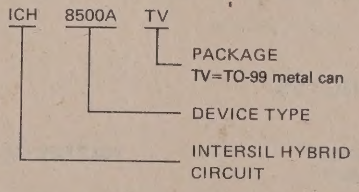
Functionally, they are pin for pin identical to the popular 741 monolithic amplifier. These amplifiers are unconditionally stable and the input offset voltage can be adjusted to zero with an external 20k potentiometer. The input bias current for the inverting and non-inverting inputs is 0.1 pA maximum for the ICH8500, and 0.01 pA maximum for the ICH8500A and are constant over the operating temperature range of -25° C to +85° C.

Pin 8 is connected to the case. This permits the designer to operate the case at any desired potential, the key to achieving the ultra low input currents associated with these two amplifiers. Forcing the case to the same potential as the inputs eliminates current flow between the case and the input pins, and leakage currents that may have otherwise existed between any of the other pins and the inputs are intercepted by the case.

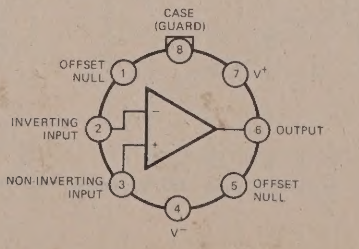
SCHEMATIC DIAGRAM


V+
7
INVERTING INPUT
2
3
NON-INVERTING INPUT
100pF
−
+
OUTPUT
6
OFFSET NULL
1
12K
1K
4
V−
1K
5
OFFSET NULL
12K

ORDERING INFORMATION


ICH
8500A
TV
PACKAGE
TV=TO-99 metal can
DEVICE TYPE
INTERSIL HYBRID CIRCUIT

PIN CONFIGURATION (outline dwg TO-99)


CASE (GUARD)
8
OFFSET NULL
1
7
V+
INVERTING INPUT
2
−
+
6
OUTPUT
NON-INVERTING INPUT
3
5
OFFSET NULL
4
V−

ICH8500/A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation[1]	500 mW
Differential Voltage	±0.5V
Storage Temperature	-65°C to +150°C
Operating Temperature	-25°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Output Short Circuit Duration	Indefinite

Note: 1. Rating applies for ambient temperature to +70°C.

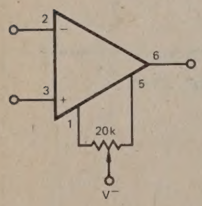
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified, V_{SUPP} = ±15V)

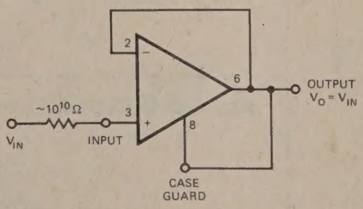
CHARACTERISTICS	SYMBOL	ICH8500 MIN	ICH8500 TYP.	ICH8500 MAX	ICH8500A MIN	ICH8500A TYP	ICH8500A MAX	UNITS	TEST CONDITIONS
Input Leakage Current (Inverting and Non-Inverting)	I_{ILK}			0.1			0.01	pA	Case at same potential as inputs
Input Offset Voltage	V_{OS}			50			50	mV	
Offset Voltage Adjustment Range	$\pm V_{OS}$			±50			±50	mV	20kΩ Potentiometer
Change in Input Offset Voltage Over Temperature	$\Delta V_{OS}/\Delta T$						±5.0 ±5.0	mV mV	+25 to +85°C -25 to +25°C
Common Mode Rejection Ratio	CMRR	60	75		60	75		dB	±5 volts common mode voltage
Output Voltage Swing	$\pm V_O$	±11			±11			V	$R_L \geq 10k\Omega$
Common Mode Voltage Range	CMVR	±10			±10			V	
Large Signal Voltage Gain	A_{VOL}	20,000	10^5		20,000	10^5		—	
Feedback Capacitance	C_{fb}			0.1			0.1	pF	Case guarded
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$			±3.0			±3.0	mV	At 25°C
Slew Rate	SR		0.5			0.5		V/µs	$R_L \geq 2k\Omega$
Input Capacitance	C_{IN}		0.7			0.7		pF	Case guarded
Input Capacitance	C_{IN}		1.5			1.5		pF	Case grounded

CIRCUIT NOTES

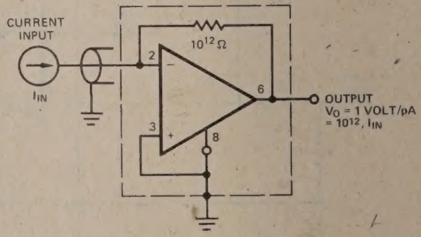
VOLTAGE OFFSET NULL CIRCUIT



VOLTAGE FOLLOWER



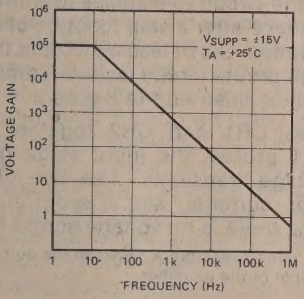
LOW LEVEL CURRENT MEASURING CIRCUIT



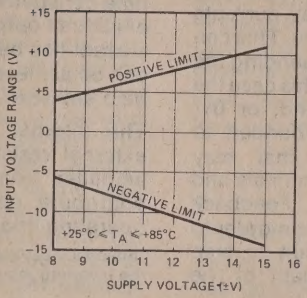
NOTE: Adjust input offset voltage to 0mV ±1mV before measuring leakage.

TYPICAL PERFORMANCE CURVES

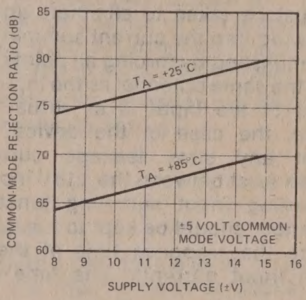
OPEN LOOP VOLTAGE GAIN vs. FREQUENCY



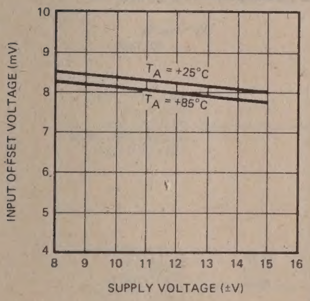
INPUT VOLTAGE RANGE vs. SUPPLY VOLTAGE



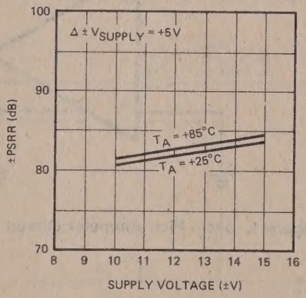
COMMON MODE REJECTION RATIO vs. SUPPLY VOLTAGE



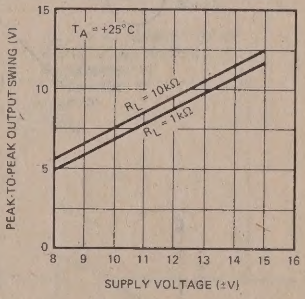
INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



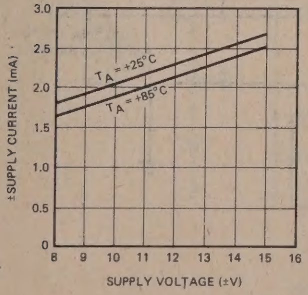
±POWER SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



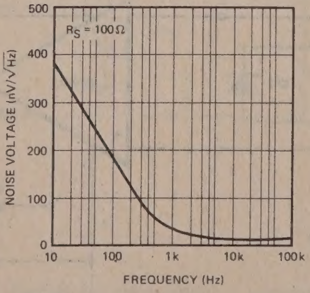
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE



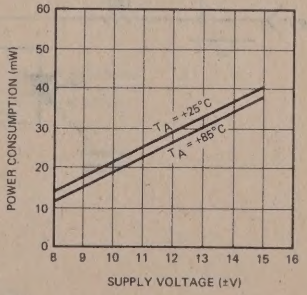
±QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



INPUT REFERRED NOISE VOLTAGE



POWER CONSUMPTION vs. SUPPLY VOLTAGE



APPLICATIONS

The Pico Ammeter

A very sensitive pico ammeter can be constructed with the ICH8500. The basic circuit (illustrated in Figure 1) employs the amplifier in the inverting or current summing mode.

Care must be taken to eliminate any stray currents from flowing into the current summing node. This can be accomplished by forcing all points surrounding the input to the same potential as the input. In this case the potential of the input is at virtual ground, or 0V, therefore, the case of the device is grounded to intercept any stray leakage currents that may otherwise exist between the ±15V input terminals and the inverting input summing junctions. Feedback capacitance* should be kept to a minimum in order to maximize the response time of the circuit to step function input currents. The time constant of the circuit is approximately the product of the feedback capacitance C_{fb} times the feedback resistor R_{fb}. For instance, the time constant of the circuit in Figure 1 is 1 sec if $C_{fb} = 1$ pF. Thus, it takes approximately 5 sec (5 time constants) for the circuit to stabilize to within 1% of its final output voltage after a step function of input current has been applied. C_{fb} of less than 0.2 to 0.3 pF can be achieved with proper circuit layout. A practical pico ammeter circuit is illustrated in Figure 2.

The internal diodes CR1 and CR2 together with external resistor R1 protect the input stage of the amplifier from voltage transients. The two diodes contribute no error currents, since under normal operating conditions there is no voltage across them.

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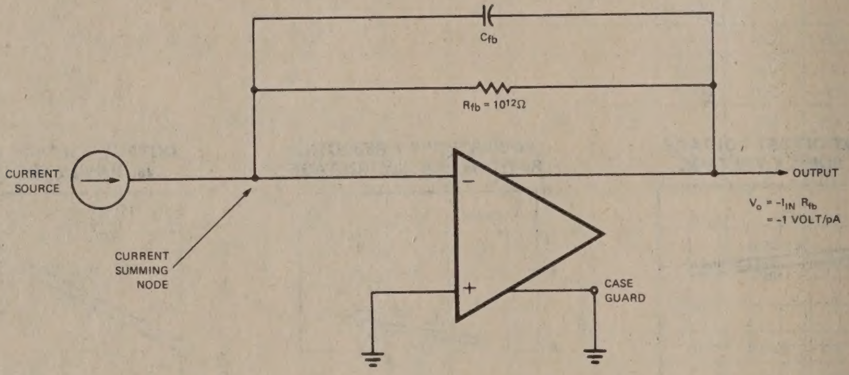
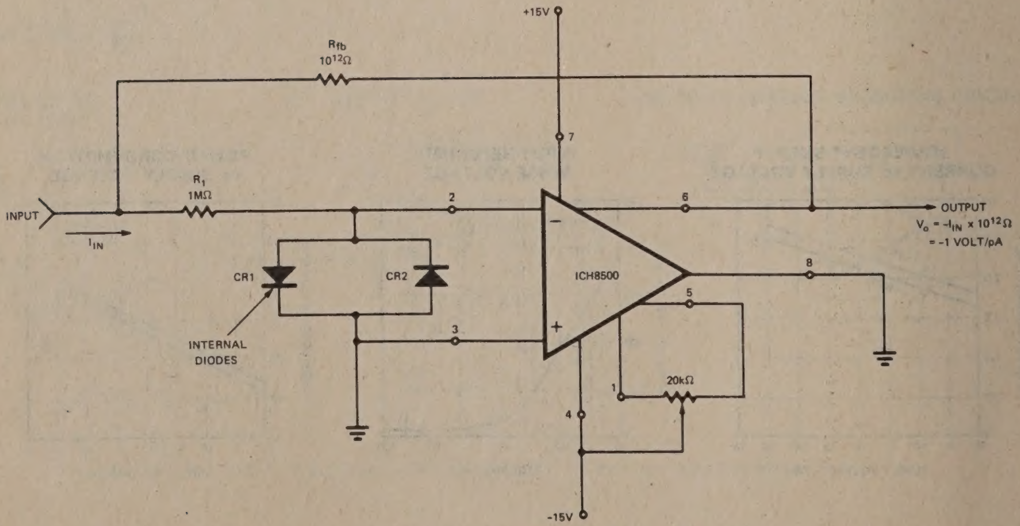
*Feedback capacitance is the capacitance between the output and the inverting input terminal of the amplifier.



C_{fb}
$R_{fb} = 10^{12}\Omega$
CURRENT SOURCE
−
OUTPUT
$V_o = -I_{IN} R_{fb}$
$= -1$ VOLT/pA
CURRENT SUMMING NODE
+
CASE GUARD

Figure 1. Basic Pico Ammeter Circuit



+15V
R_{fb}
$10^{12}\Omega$
7
R_1
1MΩ
INPUT
I_{IN}
2
6
OUTPUT
$V_o = -I_{IN} \times 10^{12}\Omega$
$= -1$ VOLT/pA
−
CR1
CR2
ICH8500
8
5
+
3
INTERNAL DIODES
1
20kΩ
4
−15V

Figure 2. Pico Ammeter Circuit

Sample and Hold Circuit (Figure 3)

The basic principle of this circuit is to rapidly charge a capacitor C_{STO} to a voltage equal to an input signal. The input signal is then electrically disconnected from the capacitor with the charge still remaining on C_{STO}. Since C_{STO} is in the negative feedback loop of the operational amplifier, the output voltage of the amplifier is equal to the voltage across the capacitor. Ideally, the voltage across C_{STO} will remain constant, thus the output of the amplifier will also be constant, however, the voltage across C_{STO} will decay at a rate proportional to the current being injected or taken out of the current summing node of the amplifier. This current can come from four sources: leakage resistance of C_{STO}, leakage current due to the solid state switch SW2, currents due to high resistance paths on the circuit fixture, and most important, bias current of the operational amplifier. If the ICH8500A operational amplifier is employed, this bias current is almost non-existant (<0.01 pA). Note that the voltages on the source, drain and gate of switch SW2 are zero or near zero when the circuit is in the hold mode. Careful construction will eliminate stray resistance paths and capacitor resistance can be eliminated if a quality capacitor is selected. The net result is a quality sample and hold circuit.

As an example, suppose the leakage current due to all sources flowing into the current summing node of the sample and hold circuit is 100pA. The rate of change of the voltage across the 0.01 μF storage capacitor is then 10mV/sec. In contrast, if an operational amplifier which exhibited an input bias current of 1 nA were employed, the rate of change of the voltage across C_{STO} would be 0.1V/sec. An error build up such as this could not be tolerated in most applications.

Wave forms illustrating the operation of the sample and hold circuit are shown in Figure 4.

The Gated Integrator

The circuit in Figure 3 can double as an integrator. In this application the input voltage is applied to the integrator input terminal. The time constant of the circuit is the product of R1 and C_{STO}. Because of the low leakage current associated with the ICH8500 and ICH8500A, very large values of R1 (Up to 10^{12} ohms) can be employed; this permits the use of small values of integrating capacitor (C_{STO}) in applications that require long time delays. Waveforms for the integrator circuit are illustrated in Figure 5.

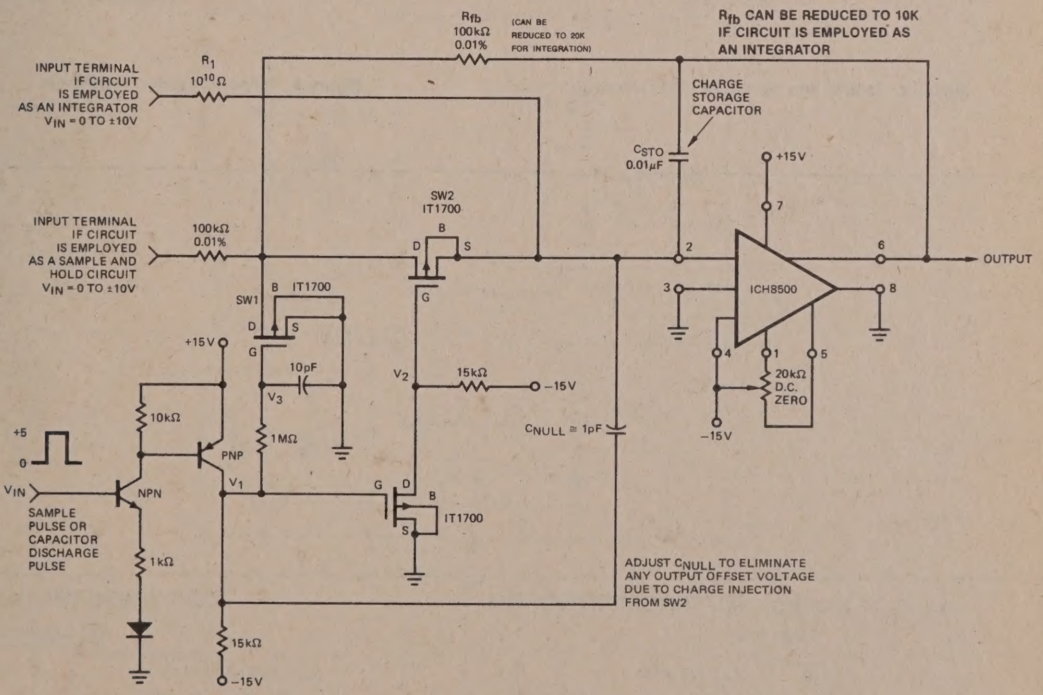

Rfb
100kΩ
0.01%
(CAN BE REDUCED TO 20K FOR INTEGRATION)
Rfb CAN BE REDUCED TO 10K IF CIRCUIT IS EMPLOYED AS AN INTEGRATOR
INPUT TERMINAL IF CIRCUIT IS EMPLOYED AS AN INTEGRATOR
VIN = 0 TO ±10V
R1
10^10 Ω
CHARGE STORAGE CAPACITOR
CSTO
0.01μF
+15V
7
SW2
IT1700
B
D
S
G
INPUT TERMINAL IF CIRCUIT IS EMPLOYED AS A SAMPLE AND HOLD CIRCUIT
VIN = 0 TO ±10V
100kΩ
0.01%
2
6
OUTPUT
3
ICH8500
8
SW1
B IT1700
D
S
G
+15V
10pF
V3
V2
15kΩ
−15V
4
1
5
20kΩ
D.C.
ZERO
−15V
10kΩ
+5
0
PNP
1MΩ
CNULL ≅ 1pF
VIN
NPN
V1
G
D
B
IT1700
S
SAMPLE PULSE OR CAPACITOR DISCHARGE PULSE
1kΩ
ADJUST CNULL TO ELIMINATE ANY OUTPUT OFFSET VOLTAGE DUE TO CHARGE INJECTION FROM SW2
15kΩ
−15V

Figure 3. Sample and Hold Circuit or Integrator Circuit

WAVEFORMS

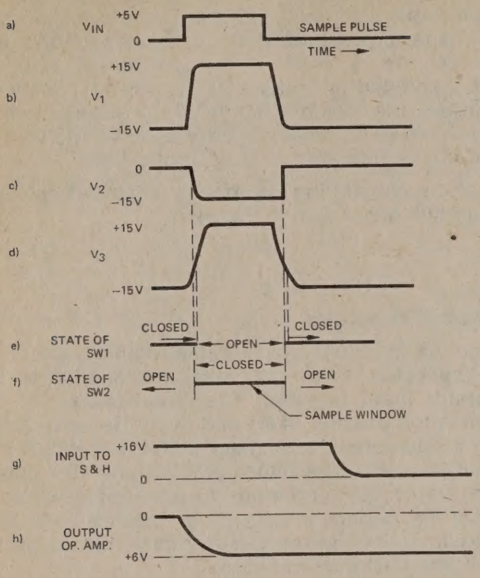


Figure 4. Sample and Hold Circuit Waveforms

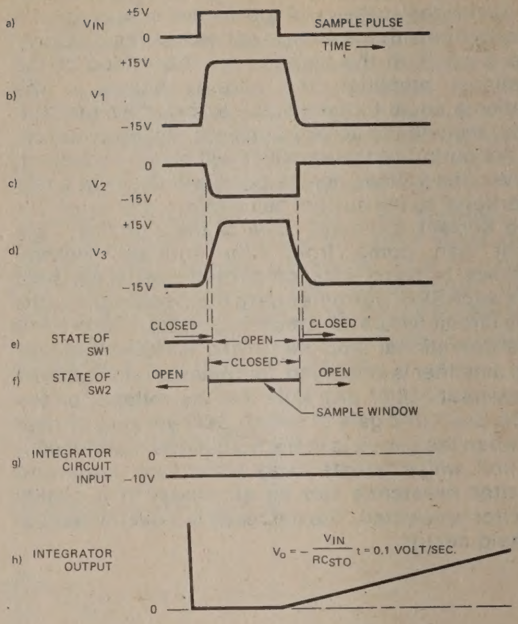


Figure 5. Gated Integrator Waveforms

ICH8510/8520/8530
Power Amplifier/ Motor & Actuator Driver

KEY FEATURES:

- Capable of delivering 2.7 amps @ 24–28V d.c. operation (30V supplies)
- Protected against inductive kick back with internal power limiting
- Programmable current limiting (short circuit protection)
- Package is electrically isolated (allowing easy heat sinking)
- DC gain 100dB
- 20mA typical standy quiescent current
- Popular 8 pin TO-3 package
- Internal frequency compensation
- Can drive up to 0.1 horsepower motors.

DESCRIPTION:

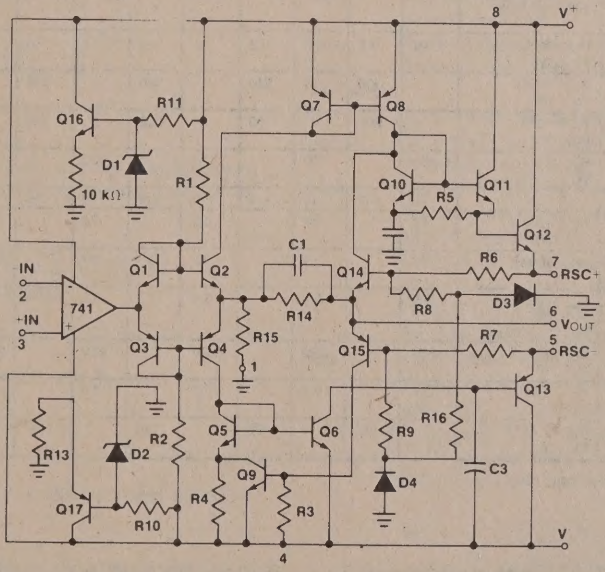
The ICH8510/8520/8530 is a family of hybrid power amplifiers that have been specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and DC & AC motors.

There are three models available for up to ±30V power supply operation, 2.7 amps @24 volt output levels, 2 amps @24V, and 1 amp @24V. All amplifiers are protected against shorts to ground by the addition of 2 external protection resistors.

The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and internal frequency compensating capacitors. The chips are mounted on a beryllium oxide substrate for optimum heat transfer to the metal package; this substrate provides electrical isolation between amplifiers and metal package.

The I.C. power driver chip has built-in regulators to drive the 741 @ typically ±13v supply voltages.

SCHEMATIC DIAGRAM

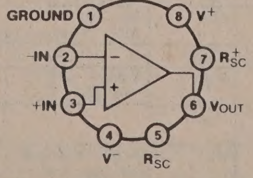

8
V+
Q16
R11
Q7
Q8
D1
R1
10 kΩ
Q10
Q11
R5
Q12
C1
-IN
2
+IN
3
741
Q1
Q2
Q14
R6
7
RSC+
R14
R8
D3
6
VOUT
Q3
Q4
R15
1
Q15
R7
5
RSC-
Q13
R16
R13
D2
R2
Q5
Q6
R9
Q9
C3
D4
Q17
R10
R4
R3
V
4

ORDERING INFORMATION

ICH8510 M KA
Package
KA=8 lead TO-3 can
Temperature Range
M=Military −55°C to +125°C
I=Industrial −20°C to +85°C
Basic Part Number
8510=1A output
8520=2A output
8530=2.7A output

PIN CONFIGURATION (OUTLINE DWG. KA)

(TOP VIEW)


GROUND 1
8 V+
−IN 2
7 R+SC
+IN 3
6 VOUT
4 V−
5 RSC
−
+

ABSOLUTE MAXIMUM RATINGS @ T_A = 25°C

Supply Voltage	±32V
Power Dissipation, Safe Operating Area	See Curves
Differential Input Voltage	±30V
Input Voltage	±15V (Note 1)
Peak Output Current	See Curves (Note 2)
Output Short Circuit Duration (to ground)	Continuous (Note 2)
Operating Temperature Range M	−55°C → +125°C
I	−20°C → +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Max Case Temperature	150°C

Note 1: Rating applies to supply voltages of ±15V. For lower supply voltages, $V_{INMAX} = V_{SUPP}$.
Note 2: Rating applies as long as package dissipation is not exceeded for heat sink attached. (See Figure 8.)

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS T_A = +25°C. V_{SUPP} = ±30V (unless otherwise stated)

DESCRIPTION	SYMBOL	CONDITIONS	ICH8510I		ICH8510M		ICH8520I		ICH8520M		ICH8530I		ICH8530M		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX	MIN.	MAX.	UNITS
Input Offset Voltage Change with Power Dissipation	$\Delta V_{OS}/\Delta Pd$	Mtd. on Wakefield 403 Heat Sink		4		2		4		2		4		2	mV/W
Input Offset Voltage	V_{OS}	R_S ≤ 10 kΩ Pd < 1W	−6	+6	−3	+3	−6	+6	−3	+3	−6	+6	−3	+3	mV
Input Bias Current	I_{BIAS}	R_S ≤ 10 kΩ Pd < 1W		500		250		500		250		500		250	nA
Input Offset Current	I_{OS}	R_S ≤ 10 kΩ Pd < 1W		200		100		200		100		200		100	nA
Large Signal Voltage Gain	A_{VOL}	R_L = 20Ω V_O = 2/3 V_{SUPP}	100		100		100		100		100		100		dB
Input Voltage Range	V_{CMR}		−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	V
Common Mode Rejection Ratio	CMRR	R_S ≤ 10 kΩ	70		70		70		70		70		70		dB
Power Supply Rejection Ratio	PSRR	R_S ≤ 10 kΩ	77		77		77		77		77		77		dB
Slew Rate	SR	C_L = 3 pF, A_V = 1 R_L = 10Ω V_O = 2/3 V_{SUPP}	0.5		0.5		0.5		0.5		0.5		0.5		V/μs
Output Voltage Swing	V_{OMAX}	R_L = 20Ω A_V = 10	±25V		±25V		±26V		±26V		(R_L = 30Ω) ±26V		(R_L = 30Ω) ±26V		V
Output Current (3)	I_{MAX}	R_L = 8Ω A_V = 10	2.7		2.7		2.0		2.0		1.0		1.0		A
Power Supply Quiescent Current	I_Q	R_L = ∞ V_{IN} = 0V		125		100		125		100		125		100	mA

Note 3: See Figure #9 if Power Supplies are less than ±30V.

ELECTRICAL SPECIFICATIONS (continued) T_A = −55°C. to +125°C.(M) or T_A = −20°C. to +85°C.(I)

Input Offset Voltage	V_{OS}	Pd < 1W	−10	+10	−9	+9	−10	+10	−9	+9	−10	+10	−9	+9	MV
Input Bias Current	I_{BIAS}	Pd < 1W		1500		750		1500		750		1500		750	nA
Input Offset Current	I_{OS}			500		200		500		200		500		200	nA
Large Signal Voltage Gain	A_{VOL}	R_L = 20Ω ΔV_O = 2/3 V_{SUPP}	90		90		90		90		90		90		dB
Output Voltage Swing	V_{OMAX}	R_L = 20Ω, A_V = 10	±24		±24		±24		±24		±24		±24		V
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Without Heat Sink		40		40		40		40		40		40	°C/W
Thermal Resistance Junction to Case	$R_{\theta JC}$			2.5		2.5		2.5		2.5		2.5		2.5	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Mtd. on Wakefield 403 Heat Sink		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0	°C/W
Supply Voltage Range	V_{SUPP}		±18	±30	±18	±30	±18	±30	±18	±30	±18	±30	±18	±30	V

How To Set The Externally Programmable, Current Limiting Resistors:

The maximum output current is set by the addition of two external resistors, R^{+}_{SC} and R^{-}_{SC}. Because of the current power limiting circuitry, the maximum output current is available only when V_O is close to either power supply. As V_O moves away from V_{SUPP}, the maximum output current decreases in proportion to output voltage. The curve below shows maximum output current versus output voltage.

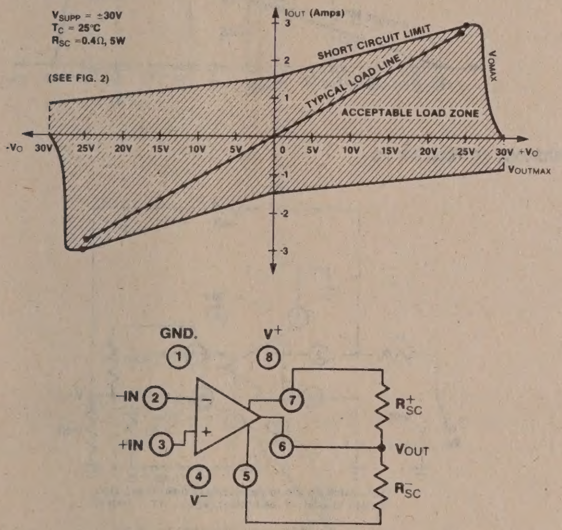


Figure 1: Maximum Output Current for Given RSC

In general, for a given V_O, I_{SC} limit, and case temperature T_C, R_{SC} can be calculated from the equation below for V_O positive, I_{OUT} positive.

$$R_{SC} = \frac{(20.6V_O)^{*} + 680 - 2.2\,(T_C - 25°C)}{I_{SC(LIMIT)}}$$

*For V_O negative, replace this term with $10.3\,(V_O - 1.2)$

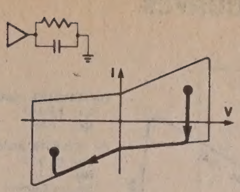
For example, for $I_O = 1.5A$ @ $V_O = 25V$ and $T_C = 25°C$,

$$R_{SC} = \frac{1195}{1500} = 0.797$$

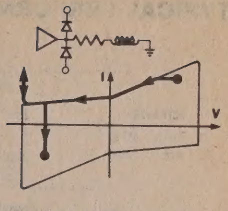
Therefore for this application, $R_{SC} = .82\Omega$ (closest standard value)

When 0.82Ω is used, I_{SC} @ $V_O = 0V$ will be reduced to about 1A. Except for small changes in the "$\pm V_{O(max)}$ Limit" area, the effects of changing R_{SC} on the I_{OUT} vs V_{OUT} characteristics can be determined by merely changing the I_{OUT} scale on Fig. 1 to correspond to the new value. Changes in T_C move the limit curve bodily up and down.

This internal power limiting circuitry however does not at all restrict the normal use of the driver. For any normal load, the static load line will be similar to that shown in Figure 1. Clearly, as V_O decreases, the I_O requirement falls also, more steeply than the I_O available. For reactive loads, the dynamic load lines are more complex. Two typical operating point loci are sketched here:



Capacitive Load



Inductive Load
(Note catch diode)

Thus the limiting circuitry protects the load and avoids needless damage to the driver during abnormal conditions. For any 24-28VDC motor/actuator, the R_{SC} resistors must be calculated to get proper power delivered to the motor (up to a maximum of 2.7A) and V_{SUPP} set at ±30V. For lower supply and/or output voltages, the maximum output current will follow graphs of Figures 1 and 5.

NOTE ON AMPLIFIER POWER DISSIPATION

The steady state power dissipation limit is given by

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\theta JC} + R_{\theta CH} + R_{\theta HA}}$$

where

$T_J =$	Maximum junction temperature
$T_A =$	Ambient temperature
$R_{\theta JC} =$	Thermal resistance from transistor junction to case of package
$R_{\theta CH} =$	Thermal resistance from case to heat sink
$R_{\theta HA} =$	Thermal resistance from heat sink to ambient air

And since

$T_J =$	200°C for silicon transistors
$R_{\theta JC} \cong$	2.0C/WATT for a steel bottom TO-3 package with die attachment to beryllia substrate to header
$R_{\theta CH} =$	.045° C/W for 1 mil thickness of Wakefield type 120 thermal joint compound .09° C/W for 2 mil thickness of type 120 .13° C/W for 3 mil thickness of type 120 .17° C/W for 4 mil thickness for type 120 .21° C/W for 5 mil thickness of type 120 .24° C/W for 6 mil thickness of type 120
$R_{\theta HA} =$	The choice of heat sink that a user selects depends upon the amount of room available to mount the heat sink. A sample calculation follows: by choosing a Wakefield 403 heat sink, with free air, natural convection (no fan). $R_{\theta HA} \cong 2.0°C/W$. Using 4 mil joint compound,

$$P_D = \frac{200°C - T_A}{2.0° + 0.17° + 2.0} = \frac{200°C - T_A}{4.17°C/W}$$

or @ $T_A = 25°C$,

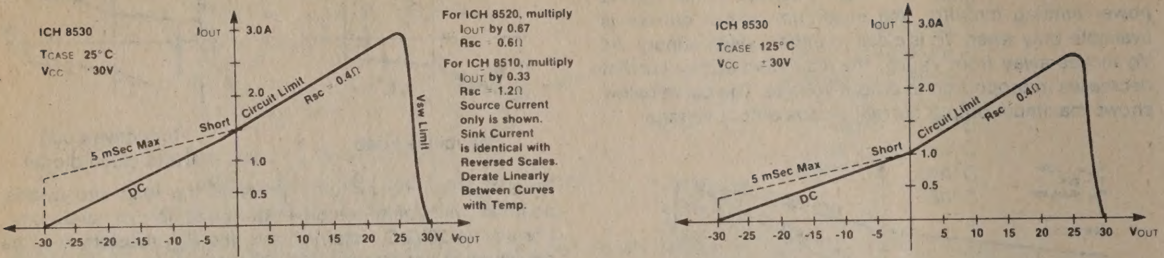
$$\frac{200°C - 25°C}{4.17°C/W} = 42W$$

and @ $T_A = 125°C$,

$$\frac{200°C - 125°C}{4.17°C/W} = 18W$$

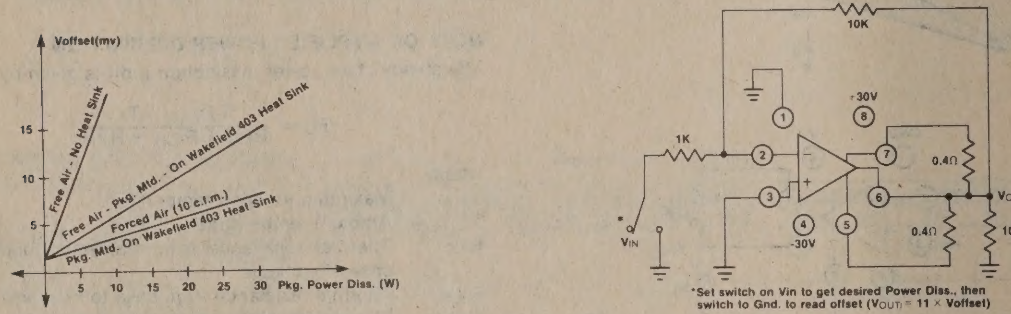
From Fig. 2 the worst case steady state power dissipation for an IH8520 ($R_{SC} = 0.62\Omega$) is about 30W and 18W respectively. Thus this heat sink is adequate.

TYPICAL PERFORMANCE CURVES



For ICH 8520, multiply
IOUT by 0.67
Rsc = 0.6Ω
For ICH 8510, multiply
IOUT by 0.33
Rsc = 1.2Ω
Source Current only is shown. Sink Current is identical with Reversed Scales. Derate Linearly Between Curves with Temp.

Figure 2: Safe Operating Area; IOUT vs VOUT vs TC



*Set switch on Vin to get desired Power Diss., then switch to Gnd. to read offset (VOUT = 11 × Voffset)

Figure 3: Input Offset Voltage vs Power Dissipation

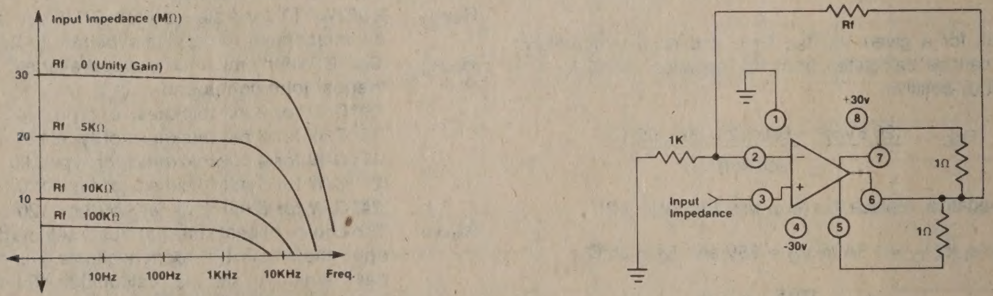


Figure 4: Input Impedance vs Gain vs Frequency

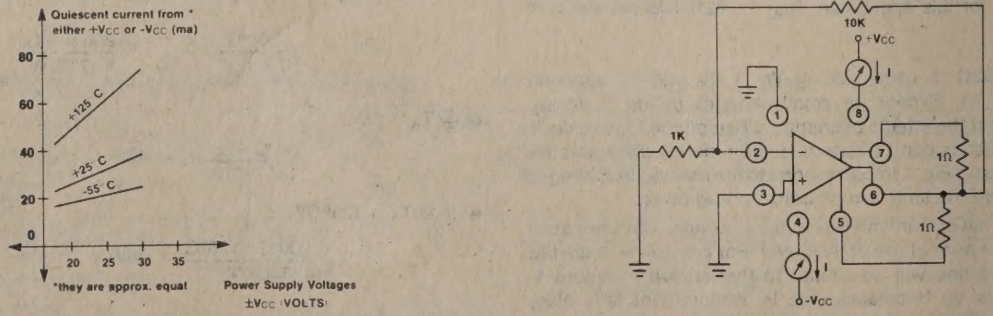


Figure 5: Quiescent Current vs Power Supply Voltage

TYPICAL PERFORMANCE CURVES, CONTINUED.

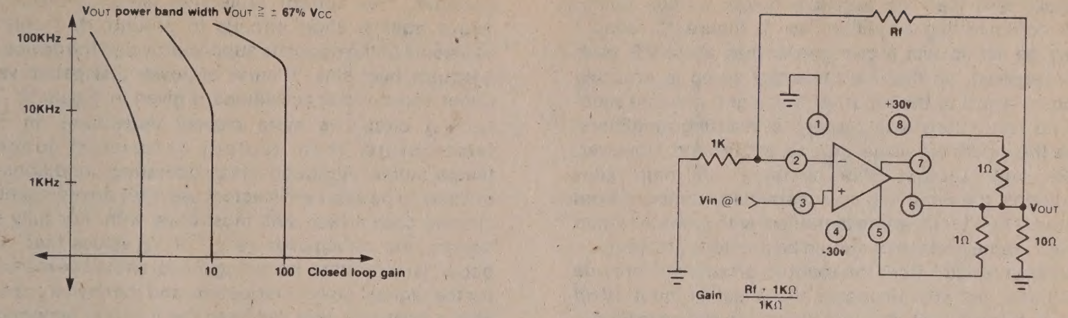


Figure 6: Large Signal Power Band Width

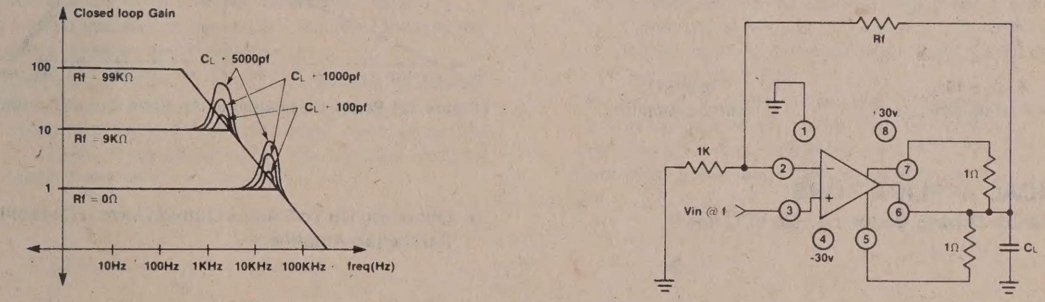


Figure 7: Small Signal Frequency Response

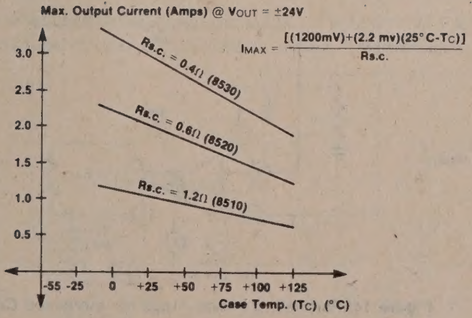


Figure 8: Maximum Output Current vs. Case Temperature

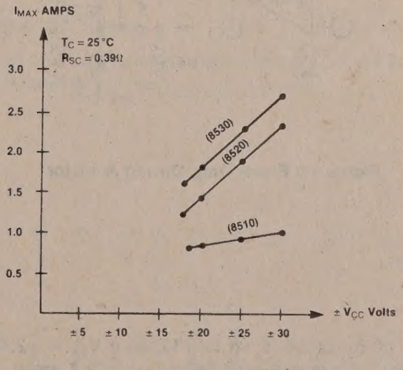


Figure 9: Maximum Output Current vs. V_{SUPP}

BRIEF APPLICATION NOTES

The maximum input voltage range, for $V_{SUPP} < \pm 15V$, is substantially less than the available output voltage swing. Thus non-inverting amplifiers, as in Figure 10, should always be set up with a gain greater than about 2.5, (with ±30V supplies), so that the full output swing is available without hazard to the input. At first sight, it would seem that no restrictions would apply to inverting amplifiers, since the inputs are virtual ground and ground. However, under fault (output short-circuited) or high slew conditions, the input can be substantially removed from ground. Thus for inverting amplifiers with gains less than about 5, some protection should be provided at this input. A suitable resistor from the input to ground will provide protection, but also increases the effect of input offset voltage at the output. A pair of diodes, as shown in Figure 12, has no effect on normal operation, but gives excellent protection.

Power dissipation is another important parameter to consider. The current protection circuit protects the device against short circuits to ground, (but only for transients to the opposite supply) provided the device has adequate heat sink. A curve of power dissipation vs V_O under short circuit conditions is given in Figure 12. The limiting circuit is more closely dependent on case temperature than (output transistor) junction temperatures. Although these operating conditions are unlikely to be attained in actual use, they do represent the limiting case a heat sink must cope with. For fully safe design, the anticipated range of V_O values that could occur, (steady state, including faults) should be examined for the highest power dissipation, and the device provided with a heat sink that will keep the junction temperature below 200° C and the case temperature below 150° C with the worst case ambient temperature expected.

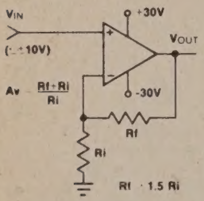


Figure 10: Non-Inverting Amplifier

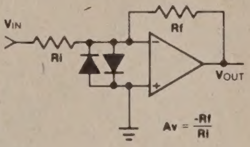


Figure 11: Inverting Amplifier

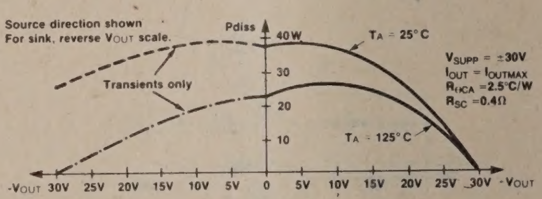


Figure 12: Power Dissipation under Short Circuit Conditions

TYPICAL APPLICATIONS

I. Actuator Driving Circuit (24–28 VDC rated)

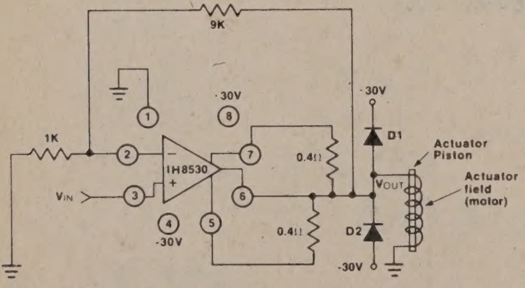


Figure 13: Power Amp Driving Actuator

The gain of the circuit is set to +10, so a V_{IN} = +2.4V will produce a +24V output (and deliver up to 2.7 amps output current). To reverse the piston travel, invert V_{IN} to −2.4V and V_{OUT} will go to −24V. Diodes D1 and D2 absorb the inductive kick of the motor during transients (turn-on or turn-off); their breakdown should exceed 60V.

II. Obtaining Up To 5 Amps Output Current Capability By Paralleling Amplifiers

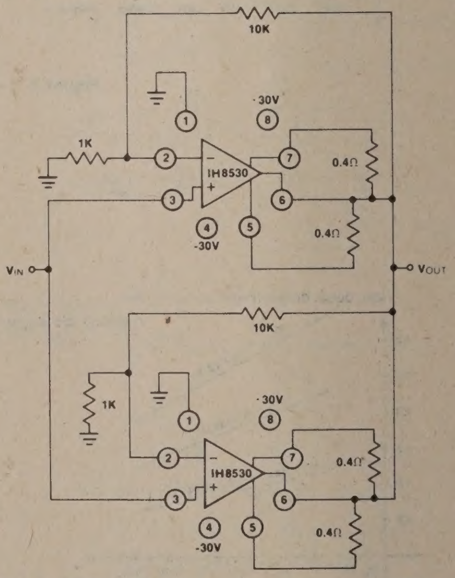
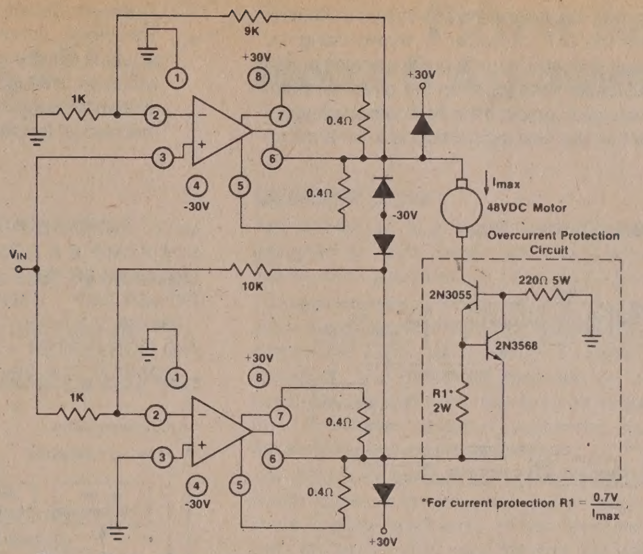


Figure 14: Paralleling Power Amps for Increased Current Capability

This paralleling procedure can be repeated to get any desired output current. However, care must be taken to provide sufficient load to avoid the amplifiers pulling against each other.

III. Driving A 48VDC Motor


9K
+30V
1K
0.4Ω
-30V
VIN
10K
+30V
Imax
48VDC Motor
Overcurrent Protection Circuit
2N3055
220Ω 5W
2N3568
R1*
2W
1K
0.4Ω
-30V
+30V
*For current protection R1 = 0.7V / Imax

A V_{IN} = +2.4V will deliver output of 48V across motor

Figure 15: Power Amp Driving 48 VDC Motor

IV. Precise Rate Control of an Electronic Valve

There are two methods to get very fine control of the opening of an orifice driven by an electronic valve.

1. Keep the voltage constant, i.e., 24VDC or 12VDC, and vary the time the voltage is applied, i.e., if it takes five seconds to completely open an orifice at 24VDC, then applying 24V for only 2½ seconds opens it only 50%.
2. Simply vary the DC driving voltage to valve. Most valves obtain full opening as an inverse of applied voltage, i.e., valves open 100% in five seconds at 24VDC and in 10 seconds at 12VDC.

A circuit to perform the second method is shown below; the advantage of this is that digit switches can precisely set driving voltage to 0.2% accuracy (8-bit DAC), thereby controlling the rate at which the valve opens.

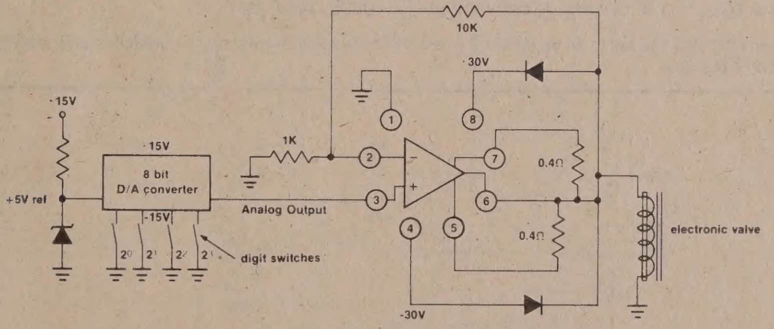
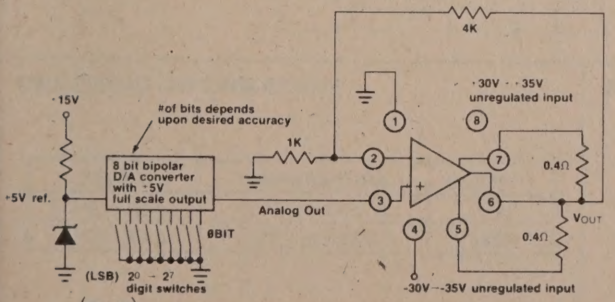

10K
+30V
+15V
+15V
8 bit D/A converter
+5V ref
-15V
1K
Analog Output
0.4Ω
0.4Ω
electronic valve
digit switches
-30V

Figure 16: Digitally Controlled Electronic Value

V. The circuit presented in Fig. 16 is also an excellent way to get a precise power supply voltage; in fact, it is possible to build a precision variable power supply using a BCD coded DAC with BCD Thumbwheel switches.


4K
+15V
#of bits depends upon desired accuracy
+30V – +35V unregulated input
1K
8 bit bipolar D/A converter with ±5V full scale output
+5V ref.
Analog Out
0.4Ω
VOUT
0.4Ω
0BIT
(LSB) 2⁰ – 2⁷ digit switches
-30V – -35V unregulated input

$V_{OUT} = \pm 5V \left(\frac{4K + 1K}{1K}\right) \times$ digital # set by Sws. and can deliver up to 3 amps.

Figure 17: Digitally Programmable Power Supply

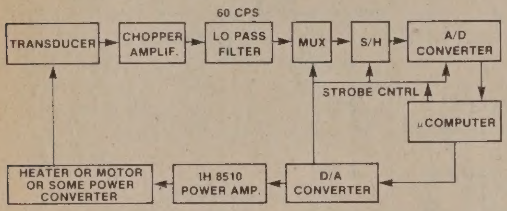
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	0 BIT	Vout
1	1	1	1	1	1	1	1	1	+25VDC
1	1	1	1	1	1	1	1	0	−25VDC
0	1	0	1	1	0	0	1	1	+15VDC
0	1	0	1	1	0	0	1	0	−15VDC
1	0	0	0	0	0	0	0	1	+0.098VDC
1	0	0	0	0	0	0	0	0	−0.098VDC

Etc.

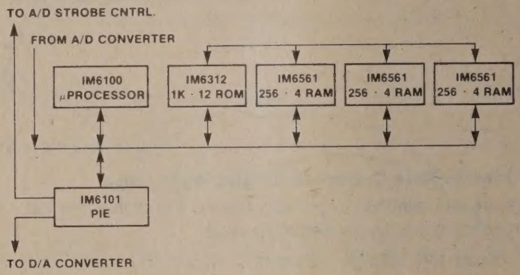
The power supply can be set to ±0.1VDC.

VI. There is great power available in the sub-systems shown in IV and V; there the D/A converter is shown being set manually (via digit switches) to get a precise analog output (binary # × full scale voltage), then the driver amplifier multiplies this voltage to produce the final output voltage. It seems obvious that the next logical step is to let a microprocessor (local) or C.P.U. program the D/A converter. Then total, pre-programmable, electronic control of an actuator, electronic valve, motor, etc., is obtained. This would be used in conjunction with a transducer/multiplex system for electronic monitoring and control of any electromechanical function.

ELECTRONIC CONTROL SYSTEM:


60 CPS
TRANSDUCER
CHOPPER AMPLIF.
LO PASS FILTER
MUX
S/H
A/D CONVERTER
STROBE CNTRL
μCOMPUTER
HEATER OR MOTOR OR SOME POWER CONVERTER
IH 8510 POWER AMP.
D/A CONVERTER

MUX = INTERSIL IH5060 (1/16) or IH5070 (2/16)
S/H (SAMPLE & HOLD) = INTERSIL IH5111
D/A CONVERTER = INTERSIL 7520 or INTERSIL 7105
POWER AMP = IH8510 (1 AMP) or IH8520 (2 AMP) or IH8530 (2.7 AMP)
A/D CONVERTER = ICL8052/7103 or ICL8052/7104
μ COMPUTER = IM6100 family:


TO A/D STROBE CNTRL.
FROM A/D CONVERTER
IM6100 μPROCESSOR
IM6312 1K · 12 ROM
IM6561 256 · 4 RAM
IM6561 256 · 4 RAM
IM6561 256 · 4 RAM
IM6101 PIE
TO D/A CONVERTER

HEAT SINK INFORMATION

Heat sinks are available from Intersil. Order part number 29-0305 ($10.00 ea.) with a $R_{\theta HA}$ = 1.3°C/watt. A convenient mating connector is also available. Order part number 29-0306 ($4.50 ea.).

NOTE: This product contains Beryllia. If used in an application where the package integrity may be breached and the internal parts crushed or machined, avoid inhalation of the dust.

INTERSIL

PRELIMINARY
Specifications Subject To Change Without Notice

ICH8515
Power Amplifier Motor & Actuator Driver

KEY FEATURES:

- **Delivers up to 1.5 amps @ +12VDC (±15VDC supplies)**
- **Protected against inductive kick back by internal power limiting**
- **Programmable current limiting (short circuit protection)**
- **Package is electrically isolated (allowing easy heat sinking)**
- **DC gain > 100dB**
- **Popular 8 pin TO-3 package**
- **Internal frequency compensation**
- **Can drive up to 0.033 horsepower motors**
- **Pin equivalent to ICH8510/20/30 family**

DESCRIPTION:

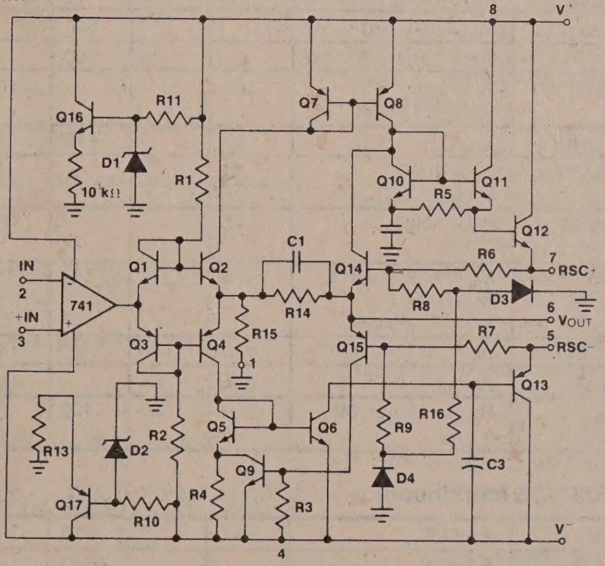
The ICH8515 is a hybrid power amplifier specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and DC & AC motors.

The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and an internal frequency compensating capacitor. The chips are mounted on a beryllium oxide substrate, for optimum heat transfer to the metal package; this substrate provides electrical isolation between the amplifier and the metal package.

The 8515 has special SOA (safe operating area) circuitry which allows it to withstand a direct short to ground or to either supply indefinitely. It has been designed to operate with ±12 or ±15VDC supplies and will deliver typically 1.5 to 1.8A @ 13V out using +15V supplies.

Internal frequency compensation provides stability down to unity gain (either inverting or noninverting) even when using inductive loads.

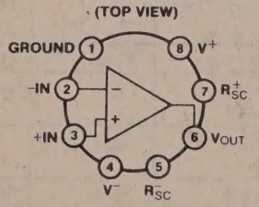
SCHEMATIC DIAGRAM


8
V+
Q16
R11
Q7
Q8
D1
R1
10 kΩ
Q10
R5
Q11
Q12
C1
R6
7
RSC+
IN
Q1
Q2
Q14
2
741
R14
R8
D3
+IN
3
R15
6
VOUT
1
Q3
Q4
Q15
R7
5
RSC−
Q13
Q5
Q6
R16
R9
R13
D2
R2
C3
Q9
D4
R4
R3
Q17
R10
V−
4

ORDERING INFORMATION

DEVICE	TEMPERATURE	OUTPUT
ICH8515MKA	−55°C to +125°C	1.5A
ICH8515IKA	−20°C to +85°C	1.25A

PIN CONFIGURATION (OUTLINE DWG. KA)


(TOP VIEW)
GROUND 1
8 V+
−IN 2
7 R_{SC}^{+}
+IN 3
6 VOUT
4
5
V−
R_{SC}^{-}
−
+

ABSOLUTE MAXIMUM RATINGS @ $T_A = 25°C$

Supply Voltage	±18V
Power Dissipation, Safe Operating Area	See Curves
Differential Input Voltage	±30V
Input Voltage	±15V (Note 1)
Peak Output Current	See Curves (Note 2)
Output Short Circuit Duration (to ground)	Continuous (Note 2)
Operating Temperature Range M	−55°C → +125°C
I	−20°C → +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Max Case Temperature	150°C

Note 1: Rating applies to supply voltages of ±15V. For lower supply voltages, $V_{INMAX} = V_{SUPP}$.
Note 2: Rating applies as long as package dissipation is not exceeded for heat sink attached.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS $T_A = +25°C$. $V_{SUPP} = ±15V$ (unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	ICH8515I			ICH8515M			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage Change with Power Dissipation	$\Delta V_{OS}/\Delta Pd$	Mtd. on Wakefield 403 Heat Sink			4			2	mV/W
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$, $Pd < 1W$	−6	1	6	−3	0.7	3	mV
Input Bias Current	I_{BIAS}	$R_S \leq 10k\Omega$, $Pd < 1W$			500			250	nA
Input Offset Current	I_{OS}	$R_S \leq 10k\Omega$, $Pd < 1W$			200			100	nA
Large Signal Voltage Gain	A_{VOL}	$R_L = 10\Omega$, $V_O > 2/3\ V_{SUPP}$	100			100			dB
Input Voltage Range	V_{CMR}		−10		+10	−10		+10	V
Common Mode Rejection Ratio	CMRR	$R_S = 10k\Omega$	70			70			dB
Power Supply Rejection Ratio	PSRR	$R_S = 10k\Omega$	77			77			dB
Slew Rate	SR	$C_L = 30pF$, $A_V = 1$, $R_L = 10\Omega$ $V_O \geq 2/3\ V_{SUPP}$	0.5			0.5			V/µs
Output Voltage Swing	V_{OMAX}	$R_L = 10\Omega$, $A_V = 10$	±12			±12			V
Output Current	I_{MAX}	$R_L = 5\Omega$, $A_V = 10$	±1.25	1.4		±1.5	1.8		A
Power Supply Quiescent Current	I_Q	$R_L = \infty$, $V_{IN} = 0V$		80	125		70	100	mA

OPERATING CHARACTERISTICS (continued) $T_A = -55°C$. to $+125°C$ (M) or $T_A = -20°C$. to $+85°C$. (I)

PARAMETER	SYMBOL	TEST CONDITIONS	ICH8515I MIN.	ICH8515I TYP.	ICH8515I MAX.	ICH8515M MIN.	ICH8515M TYP.	ICH8515M MAX.	UNITS
Input Offset Voltage	V_{OS}	$Pd < 1W$	−10		+10	−9		+9	mV
Input Bias Current	I_{BIAS}	$Pd < 1W$			1500			750	nA
Input Offset Current	I_{OS}				500			200	nA
Large Signal Voltage Gain	A_{VOL}	$R_L = 10\Omega$, $\Delta V_O = 2/3\ V_{SUPP}$	90			90			dB
Output Voltage Swing	V_{OMAX}	$R_L = 10\Omega$, $A_V = 10$	±10			±10			V
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Without Heat Sink			40			40	°C/W
Thermal Resistance Junction to Case	$R_{\theta JC}$				3.0			3.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Mtd. on Wakefield 403 Heat Sink		4.5			4.5		°C/W
Supply Voltage Range	V_{SUPP}		±11		±17	±11		±17	V

How To Set The Externally Programmable, Current Limiting Resistors:

The maximum output current is set by the addition of two external resistors, R^{+}_{SC} and R^{-}_{SC}. Because of the current power limiting circuitry, the maximum output current is available only when V_O is close to either power supply. As V_O moves away from V_{SUPP}, the maximum output current decreases in proportion to output voltage. The curve below shows maximum output current versus output voltage.

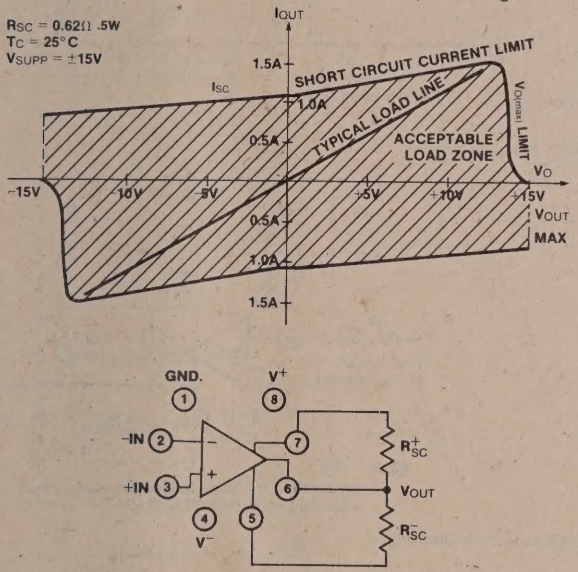


Figure 1: Maximum Output Current for Given R_{SC}

In general, for a given V_O, I_{SC} limit, and case temperature T_C, R_{SC} can be calculated from the equation below for V_O positive, I_{OUT} positive.

$$R_{SC} = \frac{(20.6V_O)^{*} + 680 - 2.2\,(T_C - 25°C)}{I_{SC\,(limit)} \text{ in mA}}$$

*For V_O negative, replace this term with $10.3\,(V_O - 1.2)$

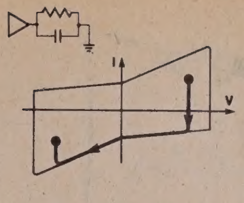
For example, for $I_O = 1.5A$ @ $V_O = 12V$ and $T_C = 25°C$,

$$R_{SC} = \frac{(20.6)(12) + 680}{1500} = \frac{927.2}{1500} = .618$$

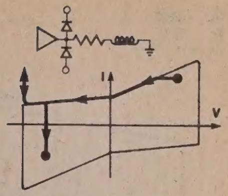
Therefore for this application, $R_{SC} = .62\Omega$ (closest standard value)

When 0.62Ω is used, I_{SC} @ V_O = 0V will be reduced to about 1A. Except for small changes in the "$\pm V_{O(max)}$ Limit" area, the effects of changing R_{SC} on the I_{OUT} vs V_{OUT} characteristics can be determined by merely changing the I_{OUT} scale on Fig. 1 to correspond to the new value. Changes in T_C move the limit curve bodily up and down.

This internal power limiting circuitry however does not at all restrict the normal use of the driver. For any normal load, the static load line will be similar to that shown in Figure 1. Clearly, as V_O decreases, the I_O requirement falls also more steeply than the I_O available. For reactive loads, the dynamic load lines are more complex. Two typical operating point loci are sketched here:



Capacitive Load



Inductive Load
(Note catch diode)

Thus the limiting circuitry protects the load and avoids needless damage to the driver during abnormal conditions. For any 12VDC motor/actuator, the R_{SC} resistors must be calculated to get proper power delivered to the motor (up to a maximum of 1.5 amps) and V_{SUPP} set at ±15V. For lower supply and/or output voltages, the maximum output current will follow graphs of Figures 1 and 9.

NOTE ON AMPLIFIER POWER DISSIPATION

The steady state power dissipation limit is given by

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\theta JC} + R_{\theta CH} + R_{\theta HA}}$$

where

T_J =	Maximum junction temperature
T_A =	Ambient temperature
$R_{\theta JC}$ =	Thermal resistance from transistor junction to case of package
$R_{\theta CH}$ =	Thermal resistance from case to heat sink
$R_{\theta HA}$ =	Thermal resistance from heat sink to ambient air

And since

T_J =	150°C for silicon transistors
$R_{\theta JC} \cong$	2.0C/WATT for a steel bottom TO-3 package with die attachment to beryllia substrate to header
$R_{\theta CH}$ =	.045° C/W for 1 mil thickness of Wakefield type 120 thermal joint compound .09° C/W for 2 mil thickness of type 120 .13° C/W for 3 mil thickness of type 120 .17° C/W for 4 mil thickness for type 120 .21° C/W for 5 mil thickness of type 120 .24° C/W for 6 mil thickness of type 120
$R_{\theta HA}$ =	The choice of heat sink that a user selects depends upon the amount of room available to mount the heat sink. A sample calculation follows: by choosing a Wakefield 403 heat sink, with free air, natural convection (no fan). $R_{\theta HA} \cong 2.0°C/W$. Using 4 mil joint compound,

$$P_D = \frac{150°C - T_A}{2.0° + 0.17° + 2.0} = \frac{150°C - T_A}{4.17°C/W}$$

or @ T_A = 25°C,

$$\frac{150°C - 25°C}{4.17°C/W} = 30W$$

and @ T_A = 125°C,

$$\frac{150°C - 125°C}{4.17°C/W} = 6W$$

From Fig. 2 the worst case steady state power dissipation for the IH8515 ($R_{SC} = 0.62\Omega$) is about 15W and 11W respectively. Thus this heat sink is adequate.

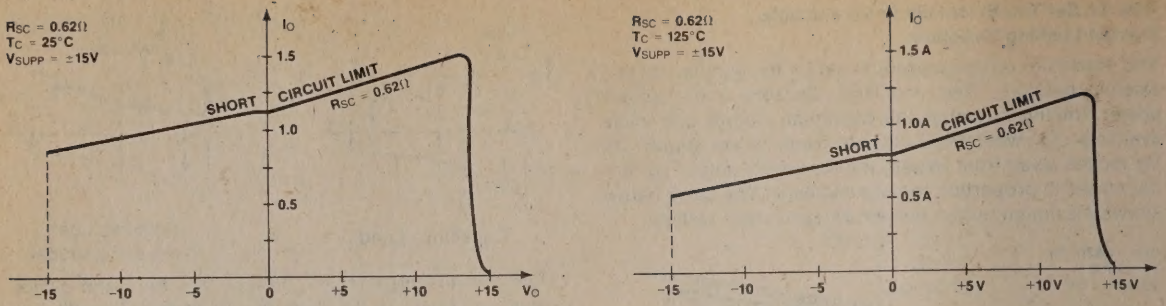
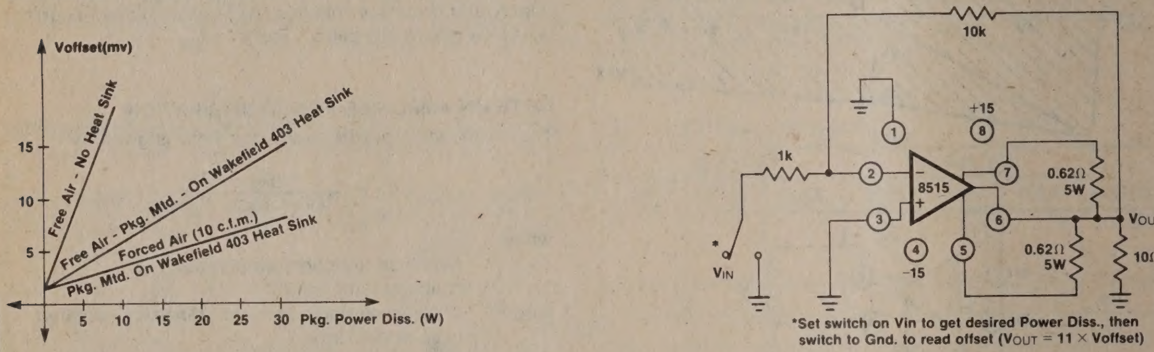


Figure 2: IOUT vs. VOUT

TYPICAL PERFORMANCE CURVES



*Set switch on Vin to get desired Power Diss., then switch to Gnd. to read offset (VOUT = 11 × Voffset)

Figure 3: Input Offset Voltage vs Power Dissipation

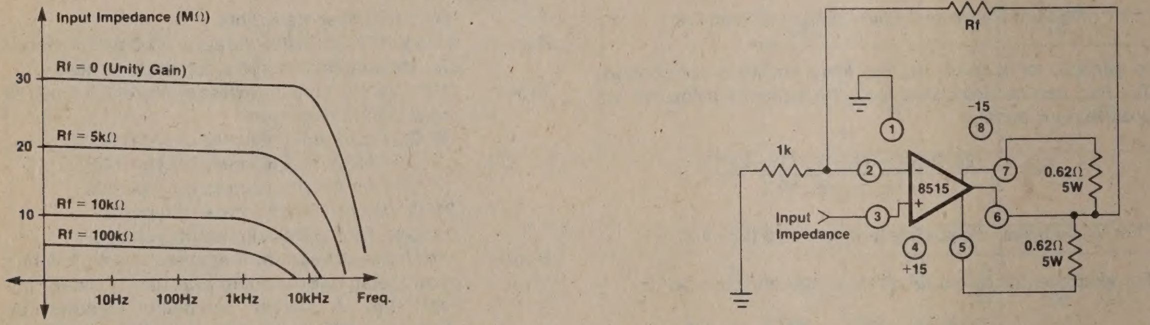


Figure 4: Input Impedance vs Gain vs Frequency

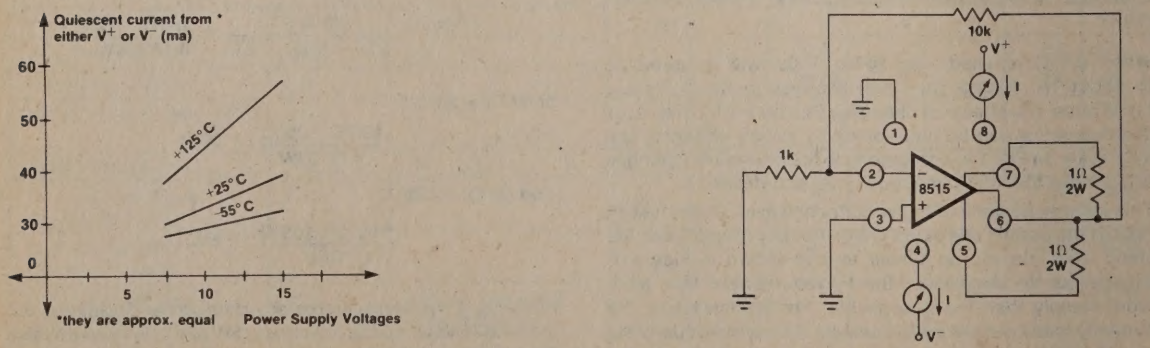


Figure 5: Quiescent Current vs Power Supply Voltage

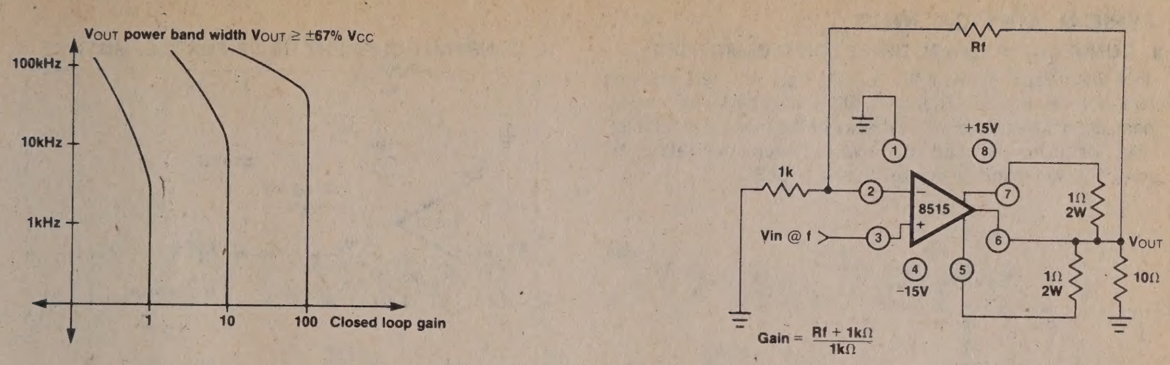


Figure 6: Large Signal Power Band Width

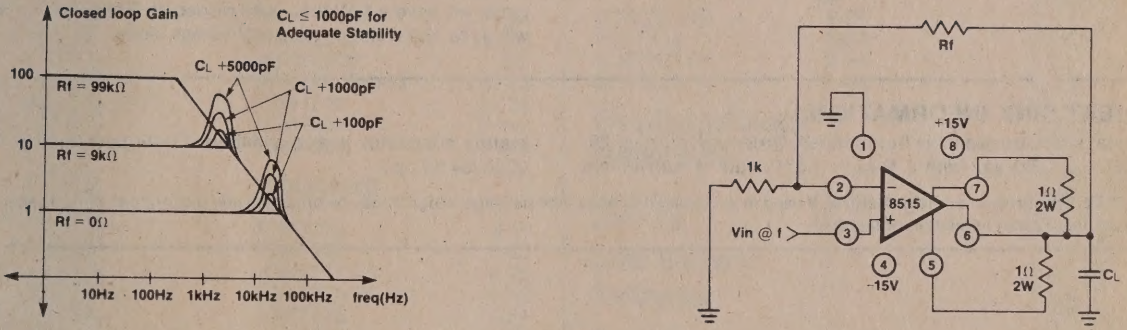


Figure 7: Small Signal Frequency Response

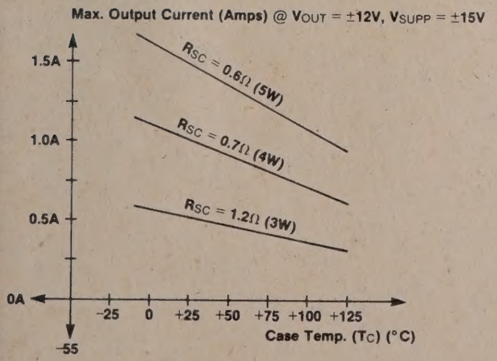


Figure 8: Maximum Output Current vs. Case Temperature

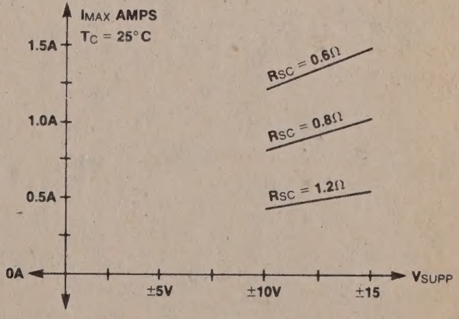
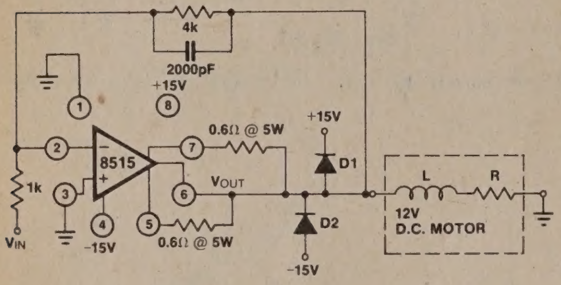


Figure 9: Maximum Output Current vs. V_{SUPP}

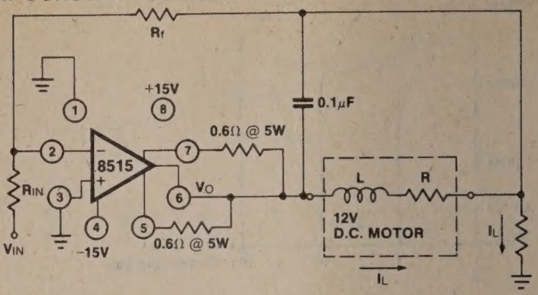
TYPICAL APPLICATIONS

I. CONSTANT VOLTAGE DRIVE FOR D.C. MOTORS

Here $V_{OUT}/V_{IN} = 4$, and if $V_{IN} = -3V$, $V_{OUT} = +12V$, and vice versa for $V_{IN} = +3V$. Diodes D1, D2 should be 1N4001 types; these absorb the inductive kickbacks of the motor. The 2000pF Miller capacitor is used to prevent system oscillation, by providing gain rolloff @ approx. 20kHz (−3dB).


4k
2000pF
+15V
1
8
2
8515
7
0.6Ω @ 5W
+15V
D1
1k
3
6
VOUT
L
R
12V
D.C. MOTOR
4
5
D2
VIN
-15V
0.6Ω @ 5W
-15V

II. CONSTANT CURRENT DRIVE FOR D.C. MOTORS


Rf
+15V
1
8
0.1μF
0.6Ω @ 5W
2
8515
7
RIN
3
6
VO
L
R
12V
D.C. MOTOR
IL
4
5
0.6Ω @ 5W
VIN
-15V
IL

$$\frac{I_L}{V_{IN}} = -\frac{R_f}{R_{IN}} \bullet \frac{1}{R_L},\ \text{assuming } R_f >> R_L.$$

This circuit allows precisely set motor drive current with op. amp. feedback accuracy. If $R_{IN} = R_F = 1k\Omega$, and $R_L = 10\Omega$, then $\frac{I_L}{V_{IN}} = -0.1$ Amps/Volt, and if $R_L = 1\Omega$ (use 4W or more) and $R_F = R_{IN} = 1k\Omega$, $\frac{I_L}{V_{IN}} = -1 \times 1 = \frac{1\ \text{Amp}}{\text{Volt}}$. Thus if $V_{IN} = 1.5V$, 1.5 amps will flow thru the motor. Since one side of the motor will have a 1.5V drop (with respect to GND), the V_O point will go to 13.5V and develop 12V across motor.

HEAT SINK INFORMATION

Heat sinks are available from Intersil. Order part number 29-0305 ($10.00 ea.) with a $R_{\theta HA} = 1.3°C/watt$. A convenient mating connector is also available. Order part number 29-0306 ($4.50 ea.).

NOTE: This product contains Beryllia. If used in an application where the package integrity may be breached and the internal parts crushed or machined, avoid inhalation of the dust.

Timers, Counters, and Display Drivers

Timers

	Page
NE/SE555	6-3
NE/SE556	6-7
ICM7240/50/60	6-123
ICM7242	6-134
ICM7555	6-140
ICM7556	6-140

Counters

ICM7208	6-15
ICM7216	6-40
ICM7217/27	6-55
ICM7224/25	6-76
ICM7226	6-83
ICM7236	6-118

Counter Timebase

ICM7207/A 6-11

Display Drivers

ICM7211/12	6-25
ICM7218	6-67
ICM7231-34	6-94
ICM7235	6-112

Oscillator/Clock Generator

ICM7209	6-22
ICM7213	6-35

Low Battery Indicator

ICM7201 6-9

Counters, Timers and Display Drivers

Part Number	Circuit Description	Package	Crystal Frequency	Output
ICM7045A	Complete industrial stopwatch precision decade timer to count seconds, minutes or hours by selection of suitable oscillator frequencies.	28-Pin DIP	Seconds: 1.31 MHz Minutes: 2.18 MHz Hours: 3.64 MHz	Seven-digit common-cathode LED drive. Displays up to 240.000 seconds, 2,400 minutes, 24-hours.
ICM7201	Low battery voltage indicator	TO-72	Not applicable	Lights LED at voltage below 2.9V.
ICM7206	Touch-tone encoder; requires single contact per key.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206A	Touch-tone encoder; requires one contact per key with common line connected to + supply.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206B	Touch-tone encoder; requires 2 contacts per key with common line connected to negative supply; oscillator enabled when key is pressed.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206C	Touch-tone encoder requires single contact per key; oscillator enabled only when key is depressed.	16-Pin DIP	2.57954 MHz	2-of-8 sine wave for tone dialing
ICM7207 ICM7202A	Frequency counter timebase.	14-Pin DIP 14-Pin DIP	6.5536 MHz 5.2488 MHz	0.01, 0.1, or 1-second count window plus store, reset and MUX.
ICM7208	7-digit unit counter. With addition of 7207 the circuit becomes a complete timer-frequency counter.	28-Pin DIP	—	LED display drive
ICM7209	High-frequency clock-generator for 5-volt systems	8-Pin DIP	to 10 MHz	Crystal frequency, plus 8 divider stage
ICM7211 ICM7212	Four-digit display decoder drivers; ICM7211 is LCD; ICM7212 is LED; Non-multiplexed for low noise, BCD input, decoded display drive output.	40-Pin DIP (plastic)	—	Four-digit, seven-segment direct display drive; LED or LCD
ICM7213	Oscillator and frequency divider	14-Pin DIP (plastic)	to 10 MHz	1pps, 1ppm, 10 Hz, composite
ICM7216 ICM7226	Eight-digit universal counter measures frequency, period, frequency ratio, time interval, units; on-board time base.	28-Pin DIP 40-Pin DIP (Cerdip or plastic)	1 or 10 MHz	Eight-digit-common anode or common cathode direct LED drive; BCD output
ICM7217 ICM7227	Four-digit CMOS up/down counter: presettable start/count and compare register; for hard-wired or microprocessor control applications; cascadable.	28-Pin Cerdip or plastic	—	Four-digit, seven-segment common anode or common cathode direct LED display drive; equal, zero, carry/borrow
ICM7218A/D ICM7218E	LED display driver system with 8x8 memory; numeric or dot (1 of 64) decoding; microprocessor compatible.	28-Pin DIP 40-Pin DIP (Cerdip or plastic)	—	Eight-digit, seven-segment plus decimal point; common cathode or common anode
ICM7224 ICM7225	4½-digit high speed counter/decoder/driver; 25 MHz typ; ICM7224 is LCD, ICM7225 is LED; direct display drive, cascadable.	40-Pin DIP (plastic)	—	4½-digit seven-segment direct display driver; LED or LCD
ICM7231	8-digit CMOS multiplexed LCD driver. Parallel input.	40-Pin DIP (plastic)	—	Eight-digit, seven-segment plus two flags per digit
ICM7232	10½-digit CMOS multiplexed LCD driver. Serial input.	40-Pin DIP (plastic)	—	10½-digit, seven-segment plus two flags per digit
ICM7233	4-character CMOS multiplexed LCD driver. Parallel alphanumeric (6-bit ASCII) input.	40-Pin DIP (plastic)	—	Four-character, 16-segment plus colon
ICM7234	5-character CMOS multiplexed LCD driver. Serial alphanumeric (6-bit ASCII) input.	40-Pin DIP (plastic)	—	Five-character, 16-segment plus colon
ICM7235/A	4-digit CMOS decoder/driver for direct drive vacuum fluorescent displays. BCD input.	40-Pin DIP (plastic)	—	Four-digit, seven-segment, vacuum fluorescent display drive; either HEX or CODE B
ICM7235M/AM	Same as above but microprocessor compatible.			
ICM7236	4½-digit high speed CMOS counter/decoder/driver for vacuum fluorescent displays; 25 MHz typ. counting speed.	40-Pin DIP (plastic)	—	4½-digit, seven-segment, vacuum fluorescent display drive
ICM7236A	Same as above but counting to 15959.	40-Pin DIP (plastic)	—	4½-digit, seven-segment, vacuum fluorescent display drive
ICM7240 ICM7250 ICM7260	Programmable CMOS counter/timers using external RC time base. Programmable from μs to years.	16-Pin DIP	External	Timed output
ICM7242	Fixed CMOS counter/timer. Uses external RC time base; sequence timing from μs to minutes.	8-Pin DIP	External	Timed output
ICM7243	8-character multiplexed LED display driver with alphanumeric (6-bit ASCII) input.	40-Pin Cerdip	—	Eight-character, 14/16-segment common cathode alphanumeric LED display drive
UCM7555 ICM7556	Single or dual CMOS version of industry-standard 555 timer; 80 μA typ. supply current; 500 kHz guaranteed; 2-18V power supply.	8-Pin DIP 14-Pin DIP	—	

INTERSIL

555
Precision Timer

FEATURES

- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **High current output can source or sink 200mA**
- **Output can drive TTL**
- **Temperature stability of 0.005%/° C**

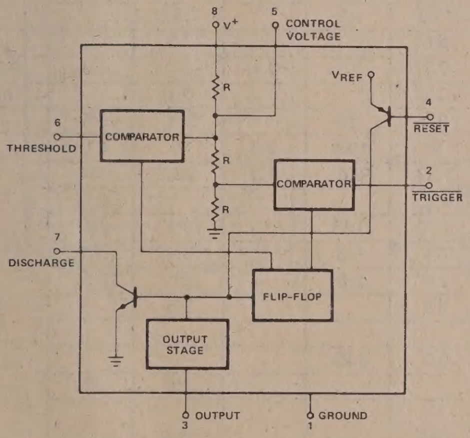
APPLICATIONS

- **Precision Timing**
- **Pulse Generation**
- **Sequential Timing**
- **Time Delay Generation**
- **Pulse Width Modulation**
- **Pulse Position Modulation**
- **Missing Pulse Detector**

GENERAL DESCRIPTION

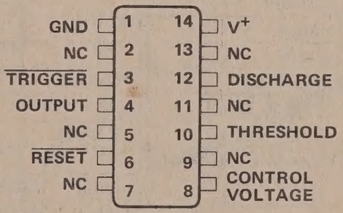
The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor; the circuit may be triggered and reset on falling waveforms, and the output structure can source or sink large currents or drive TTL circuits.

BLOCK DIAGRAM

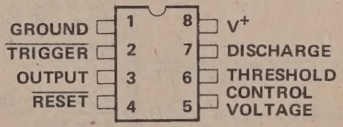

8
V+
5
CONTROL VOLTAGE
R
VREF
4
RESET
6
THRESHOLD
COMPARATOR
R
COMPARATOR
2
TRIGGER
R
7
DISCHARGE
FLIP-FLOP
OUTPUT STAGE
OUTPUT
3
GROUND
1

PIN CONFIGURATIONS

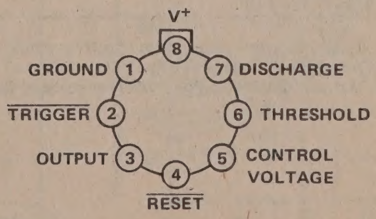
(OUTLINE DRAWING JD)


GND 1
NC 2
TRIGGER 3
OUTPUT 4
NC 5
RESET 6
NC 7
14 V+
13 NC
12 DISCHARGE
11 NC
10 THRESHOLD
9 NC
8 CONTROL VOLTAGE

(OUTLINE DRAWING PA)


GROUND 1
TRIGGER 2
OUTPUT 3
RESET 4
8 V+
7 DISCHARGE
6 THRESHOLD
5 CONTROL VOLTAGE

(OUTLINE DRAWING TO-99)


V+ 8
GROUND 1
7 DISCHARGE
TRIGGER 2
6 THRESHOLD
OUTPUT 3
5 CONTROL VOLTAGE
4 RESET

ORDERING INFORMATION

NE555/D	0° C to +70° C	Dice
NE555F		14 pin CERDIP
NE555N		8 pin plastic DIP
NE555T		TO-99 can
SE555/D	-55° C to +125° C	Dice
SE555F*		14 pin CERDIP
SE555T*		TO-99 can

*Add /883B to order number if 883B processing is desired.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Power Dissipation	600mW
Operating Temperature Range	
NE555	0°C to +70°C
SE555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

ELECTRICAL CHARACTERISTICS

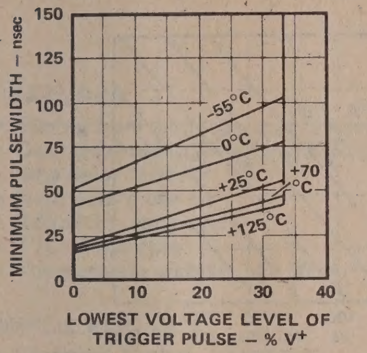
TEST CONDITIONS: $T_A = 25°C$, $V^+ = +5V$ to $+15$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE555			NE555			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	$V^+ = 5V$ $R_L = \infty$		3	5		3	6	mA
	$V^+ = 15V$ $R_L = \infty$		10	12		10	15	
	Low State, Note 1							
Timing Error	R_A, R_B = 1kΩ to 100kΩ							
Initial Accuracy	C = 0.1μF Note 2		0.5	2		1		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.005	0.02		0.01		%/Volt
Threshold Voltage			2/3			2/3		X V_{CC}
Trigger Voltage	$V^+ = 15V$	4.8	5	5.2		5		V
	$V^+ = 5V$	1.45	1.67	1.9		1.67		
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	.25		0.1	.25	μA
Control Voltage Level	$V^+ = 15V$	9.6	10	10.4	9.0	10	11	V
	$V^+ = 5V$	2.9	3.33	3.8	2.6	3.33	4	
Output Voltage Drop (low)	$V^+ = 15V$							
	$I_{SINK} = 10mA$		0.1	0.15		0.1	.25	
	$I_{SINK} = 50mA$		0.4	0.5		0.4	.75	
	$I_{SINK} = 100mA$		2.0	2.2		2.0	2.5	
	$I_{SINK} = 200mA$		2.5			2.5		
	$V^+ = 5V$							
	$I_{SINK} = 8mA$		0.1	0.25				
	$I_{SINK} = 5mA$					.25	.35	
Output Voltage Drop (high)	$I_{SOURCE} = 200mA$		12.5			12.5		
	$V^+ = 15V$							
	$I_{SOURCE} = 100mA$							
	$V+ = 15V$	13.0	13.3		12.75	13.3		
	$V^+ = 5V$	3.0	3.3		2.75	3.3		
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		

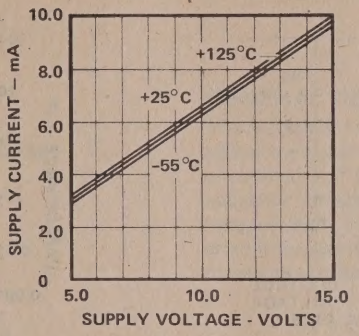
NOTE 1: Supply Current when output high typically 1mA less.
NOTE 2: Tested at $V^+ = 5V$ and $V^+ = 15V$.
NOTE 3: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total R = 20 MΩ.

TYPICAL CHARACTERISTICS

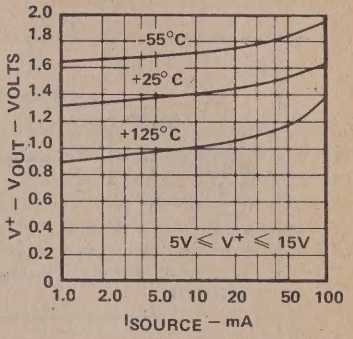
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



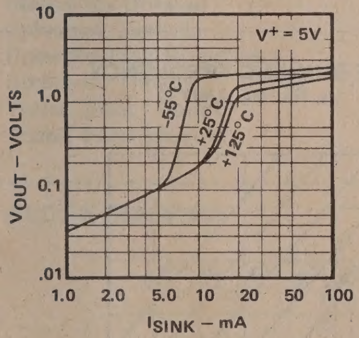
SUPPLY CURRENT vs. SUPPLY VOLTAGE



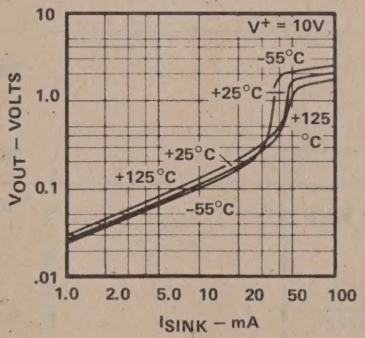
HIGH OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



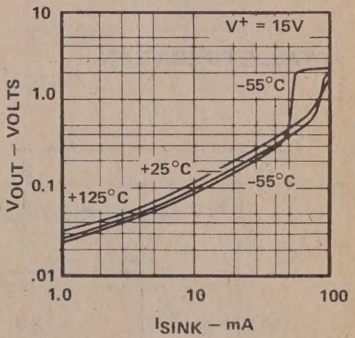
LOW OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



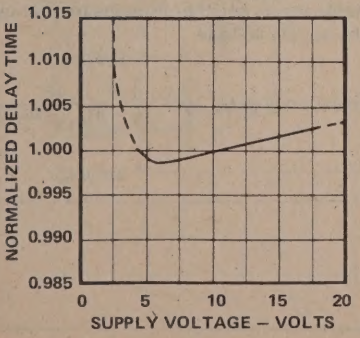
LOW OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



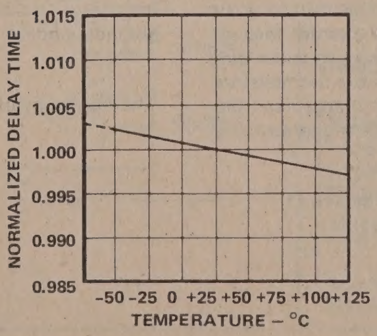
LOW OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



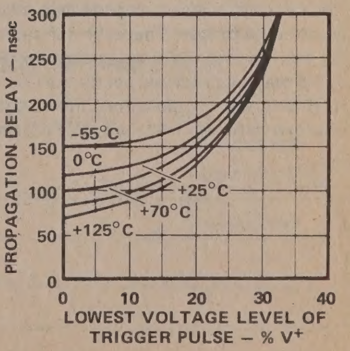
DELAY TIME vs. SUPPLY VOLTAGE



DELAY TIME vs. TEMPERATURE

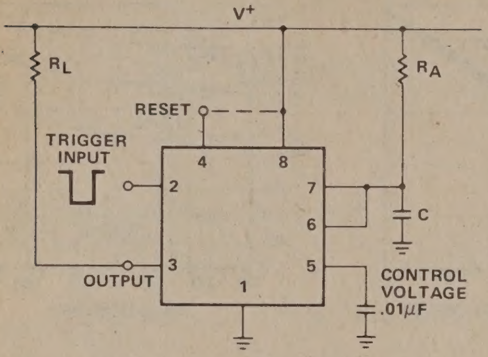


PROPAGATION DELAY vs. VOLTAGE LEVEL OF TRIGGER PULSE

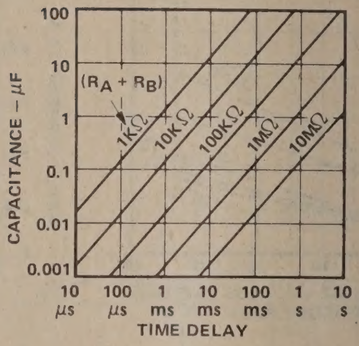


APPLICATION INFORMATION

MONOSTABLE OPERATION

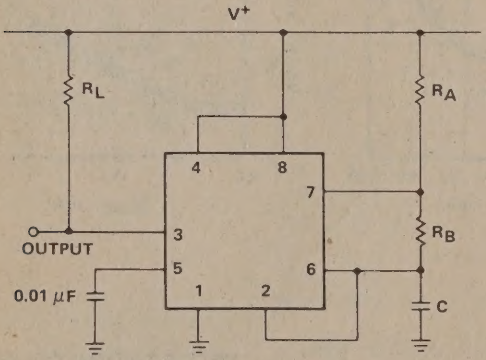


TIME DELAY vs. R_A, R_B AND C

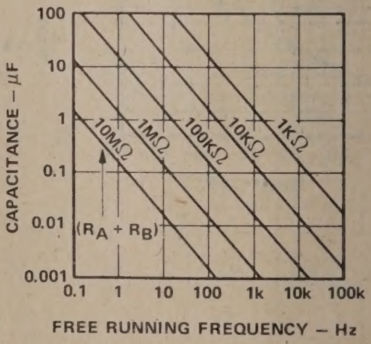


In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative trigger pulse to pin 2, a flip-flop is set which releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor increases exponentially with the time constant $\tau R_A C$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and drives the output to its low state.

ASTABLE OPERATION



FREE RUNNING FREQUENCY vs. R_A, R_B AND C



The circuit can also be connected to trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 V^+ and 2/3 V^+. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

The frequency of oscillation is given by: $f = \frac{1}{t} = \frac{1.46}{(R_A + 2R_B)\,C}$

INTERSIL

556
Dual Precision Timer

FEATURES

- **Timing from microseconds to hours**
- **Operates in both astable and monostable time delay modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005%/°C**

APPLICATIONS

- **Precision Timing**
- **Sequential Timing**
- **Pulse Shaping**
- **Pulse Generator**
- **Missing Pulse Detector**
- **Tone Burst Generator**
- **Pulse Width Modulation**
- **Time Delay Generator**
- **Frequency Division**
- **Industrial Controls**
- **Pulse Position Modulation**
- **Appliance Timing**
- **Traffic Light Control**
- **Touch Tone Encoder**

GENERAL DESCRIPTION

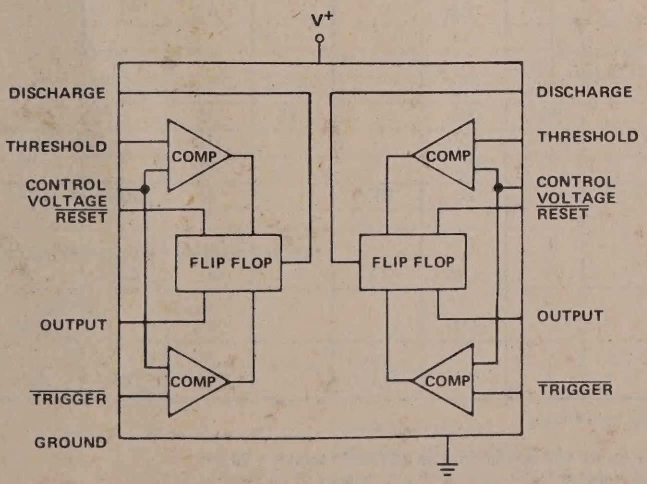
The NE/SE556 Dual 555 Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. Timing is provided by an external resistor and capacitor for each timing function; the two timers operate independently of each other sharing only V^+ and ground. The circuits may be triggered and reset on falling waveforms. The output structures will sink or source 150mA.

ABSOLUTE MAXIMUM RATINGS

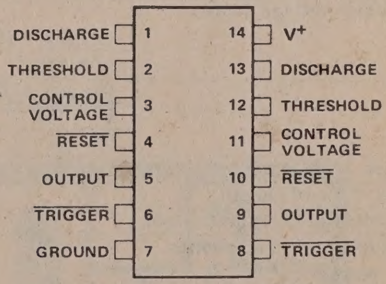
Supply Voltage	+18V
Power Dissipation*	800mW
Operating Temperature Range NE556	0°C to +70°C
SE556	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

*Derate linearly at 6.5mV/°C above ambient temperature of 75°C.

BLOCK DIAGRAM


V+
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER
GROUND
COMP
COMP
FLIP FLOP
FLIP FLOP
COMP
COMP
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER

PIN CONFIGURATION


DISCHARGE 1
THRESHOLD 2
CONTROL VOLTAGE 3
RESET 4
OUTPUT 5
TRIGGER 6
GROUND 7
14 V+
13 DISCHARGE
12 THRESHOLD
11 CONTROL VOLTAGE
10 RESET
9 OUTPUT
8 TRIGGER

(OUTLINE DRAWINGS JD, PD)

ORDERING INFORMATION

NE556/D	0°C to +70°C	Dice
NE556F		14 pin CERDIP
NE556N		14 pin plastic DIP
SE556/D	-55°C to +125°C	Dice
SE556F*		14 pin CERDIP

*Add /883B to order number if 883B processing is desired.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $T_A = 25°C$, $V^+ = +5V$ to $+15$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE556 MIN	SE556 TYP	SE556 MAX	NE556 MIN	NE556 TYP	NE556 MAX	UNITS
Supply Voltage		4.5		18	4.5		16	V
Supply Current	$V^+ = 5V$ $R_L = \infty$		3	5		3	6	mA
(each device)	$V^+ = 15V$ $R_L = \infty$ Low State, Note 1		10	11		10	14	
Timing Error (Monostable)	$R_A = 2K\Omega$ to $100K\Omega$							
Initial Accuracy	$C = 0.1\mu F$ Note 2		0.5	1.5		0.75		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%/V
Timing Error (Astable)	R_A, $R_B = 2K\Omega$ to $100K\Omega$							
Initial Accuracy	$C = 0.1\mu F$ Note 2		1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Drift with Supply Voltage			0.15			0.3		%/V
Threshold Voltage			2/3			2/3		V^+
Threshold Current	Note 3		30	100		30	100	nA
Trigger Voltage	$V^+ = 15V$	4.8	5	5.2		5		V
	$V^+ = 5V$	1.45	1.67	1.9		1.67		
Trigger Current			0.5			0.5		µA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Control Voltage Level	$V^+ = 15V$	9.6	10	10.4	9.0	10	11	V
	$V^+ = 5V$	2.9	3.33	3.8	2.6	3.33	4	
Output Voltage (low)	$V^+ = 15V$							
	$I_{SINK} = 10mA$		0.1	0.15		0.1	.25	
	$I_{SINK} = 50mA$		0.4	0.5		0.4	.75	
	$I_{SINK} = 100mA$		2.0	2.25		2.0	2.75	
	$I_{SINK} = 200mA$		2.5			2.5		
	$V^+ = 5V$							
	$I_{SINK} = 8mA$		0.1	0.25				
	$I_{SINK} = 5mA$					.25	.35	
Output Voltage (high)	$I_{SOURCE} = 200mA$		12.5			12.5		
	$V^+ = 15V$							
	$I_{SOURCE} = 100mA$							
	$V^+ = 15V$	13.0	13.3		12.75	13.3		
	$V^+ = 5V$	3.0	3.3		2.75	3.3		
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		
Discharge Leakage Current			20	100		20	100	nA
Matching Characteristics (Note 4) Initial Timing Accuracy			0.05	0.1		0.1	0.2	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%/V

NOTES:
1. Supply current when output is high is typically 1.0mA less.
2. Tested at $V^+ = 5V$ and $V^+ = 15V$.
3. This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total $R = 20\ M\Omega$.
4. Matching characteristics refer to the difference between performance characteristics of each timer section.

INTERSIL

ICM7201
Low Battery Voltage Indicator

FEATURES

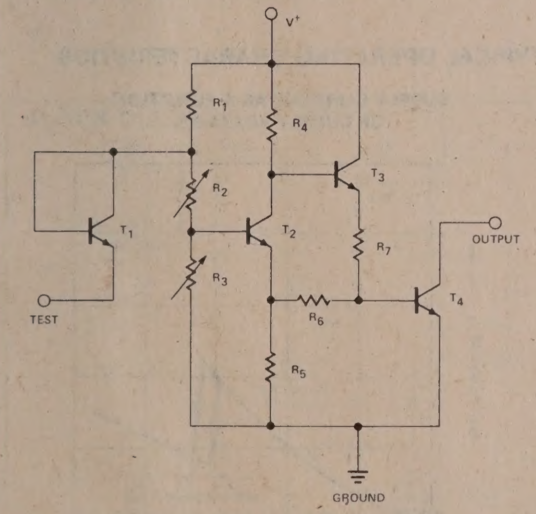
- **Accurate voltage indication: 2.9 V $\leq V_{th} \leq$ 3.3 V**
- **Simple to use: requires only an additional LED lamp for complete system**
- **Low power consumption: 4.5 mW at $V^+ =$ 3.6 V**
- **Good noise rejection — 0.2 V of hysteresis for device threshold voltage**

DESCRIPTION

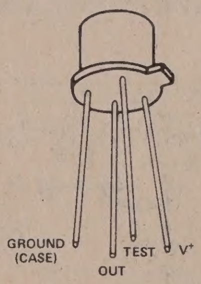
The ICM7201 is designed for use in battery operated systems which require an indication when the battery stack has depleted to a fixed voltage. The LED will light at voltages below 2.9 volts; at voltages above 2.9 volts the LED may be lit by connecting the TEST terminal to GROUND.

The ICM7201 has hysteresis designed into its threshold voltage trigger point so that the LED will not flicker with supply voltage noise and will not be turned on gradually at the trigger voltage. Under all normal circumstances the LED will either be fully on or fully off.

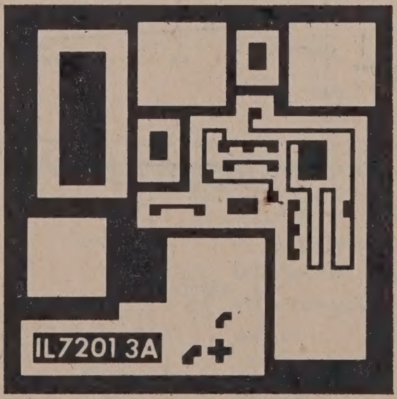
SCHEMATIC ICM7201



PIN CONFIGURATION (OUTLINE DRAWING TO-72)



CHIP TOPOGRAPHY



ORDERING INFORMATION

ICM7201 I DR

Package (DR = TO-72)

Temperature Range Industrial -20° C to +85° C

TYPE

Order Devices By Following Part Number — ICM7201IDR
Order Dice By Following Part Number - ICM7201/D

ABSOLUTE MAXIMUM RATINGS

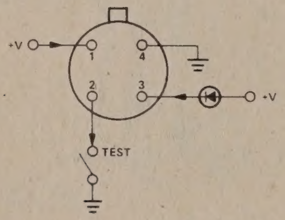
Power Dissipation	100 mW
Maximum Supply Voltage	5.5V
Maximum Output Current[1]	100 mA
Operating Temperature	—20°C to +85°C
Storage Temperature	—55°C to +125°C

TYPICAL OPERATING CHARACTERISTICS $T_A = 25°C$, Test Circuit unless otherwise stated

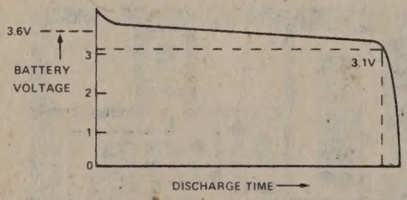
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I^+	LED off, $V^+ = +3.6$ V		1.2	2	mA
Trigger Voltage	V_{TRIG}		2.9	3.1	3.3	V
Temperature Coefficient of Trigger Voltage	$\Delta V_{TRIG}/\Delta T$			—12		mV/°C
Hysteresis Voltage	V_{th}			0.2		V
LED Current at Trigger Voltage	I_{LED}	V_F of LED approx. 1.7 V $V^+ = 3.1$ V		15		mA
Test Current	I_{TEST}	$V^+ = 3.6$ V		0.5	1.5	mA

Note:
1. At high supply voltages (approaching 5 volts) it is necessary to include a current limiting resistor in series with the LED to limit the output current to 100 mA maximum.

TEST CIRCUIT

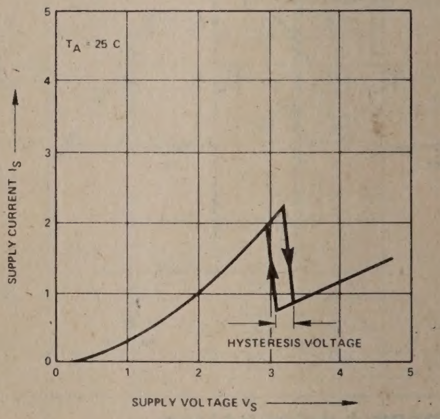


Ni-Cd 3-CELL DISCHARGE



TYPICAL OPERATING CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



OPTIONS

The ICM7201 can be supplied with maximum supply voltage options up to 15 volts and threshold voltage ranges starting from 1.8 volts. For further information contact the factory.

INTERSIL

ICM7207/A
CMOS Oscillator Controller

FEATURES

- **Stable HF oscillator**
- **Low power dissipation ≤ 5mW with 5 volt supply**
- **Counter chain has outputs at $\div 2^{12}$ and $\div 2^n$ or $\div(2^n \times 10)$; n = 17 for 7207, and 20 for 7207A**
- **Low impedance output drivers ≤100 ohms**
- **Count windows of 20/200ms (7207 with 6.5536MHz crystal) or 0.1/1 sec. (7207A with 5.24288MHz crystal)**

APPLICATIONS

- **System timebases**
- **Oscilloscope calibration generators**
- **Marker generator strobes**
- **Frequency counter controllers**

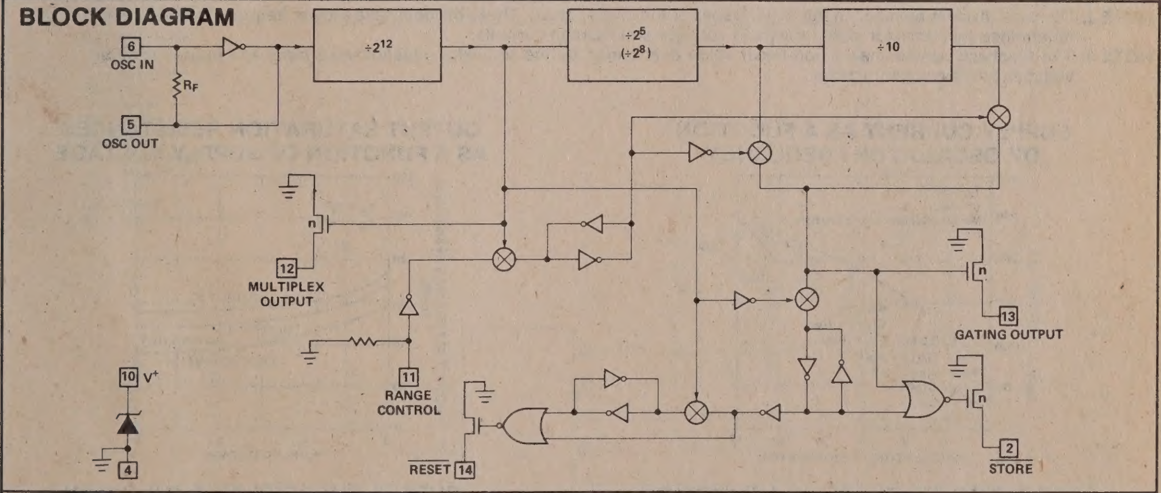
DESCRIPTION

The ICM7207/A consist of a high stability oscillator and frequency divider providing 4 control outputs suitable for frequency counter timebases. Specifically, when used as a frequency counter timebase in conjunction with the ICM7208 frequency counter, the four outputs provide the gating signals for the count window, store function, reset function and multiplex frequency reference. Additionally, the duration of the count window may be changed by a factor of 10 to provide a 2 decade range counting system.

The normal operating voltage of the ICM7207/A is 5 volts at which the typical dissipation is less than 2mW using an oscillator frequency of 6.5536MHz (5.24288MHz).

In the 7207/A the GATING output, $\overline{\text{RESET}}$, and the MULTIPLEX output provide both pull up and pull down, eliminating the need for 3 external resistors; although, buffering must be provided if interfacing with T²L is required. $\overline{\text{RESET}}$ occurs 391μs after $\overline{\text{STORE}}$, eliminating any potential problems of overlap between $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ when using the ICM7208.

BLOCK DIAGRAM

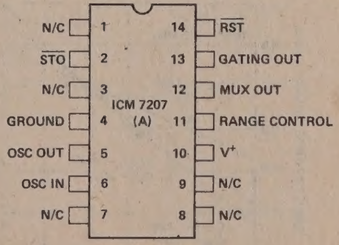

6
OSC IN
R_F
5
OSC OUT
÷2^12
÷2^5
(÷2^8)
÷10
n
12
MULTIPLEX OUTPUT
10
V+
4
11
RANGE CONTROL
RESET 14
n
13
GATING OUTPUT
n
2
STORE

ORDERING INFORMATION

ICM7207 A I PD
PD: PACKAGE
PD-14 PIN PLASTIC DIP
I: TEMPERATURE RANGE
-20°C to +85°C
A: ELECTRICAL OPTION
ICM7207: TYPE

ORDER DEVICES BY FOLLOWING PART NUMBER ICM7207 I PD, ICM7207AIPD
ORDER DICE BY FOLLOWING PART NUMBER ICM7207/D, ICM7207A/D

PIN CONFIGURATION (OUTLINE DRAWING PD)


N/C 1
STO 2
N/C 3
GROUND 4
OSC OUT 5
OSC IN 6
N/C 7
ICM 7207 (A)
14 RST
13 GATING OUT
12 MUX OUT
11 RANGE CONTROL
10 V+
9 N/C
8 N/C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.0V
Input Voltages	Equal to or less than supply voltage
Output Voltages	Not more positive than +6V with respect to GROUND
Output Currents	25mA
Power Dissipation @ 25°C Note 1	200mW
Operating Temperature Range	-20°C to +85°C
Storage Temperature Range	-55°C to +125°C

NOTE 1: Derate by 2mW/°C above 25°C.

Absolute maximum ratings refer to values which if exceeded may permanently change or destroy the device. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL OPERATING CHARACTERISTICS

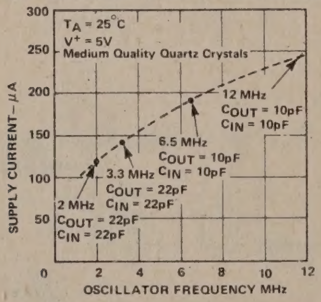
TEST CONDITIONS: f_{osc} = 6.5536MHz(7207), 5.24288MHz(7207A), V^+ = 5V, T_A = 25°C, test circuit unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	V^+	−20°C to +85°C	4		5.5	V
Supply Current	I^+	All outputs open circuit		260	1000	μA
Output on Resistances	$r_{ds}(on)$	Output current = 5mA All outputs		50	120	Ω
Output Leakage Currents	I_{OLK}	All outputs (STORE only)			50	μA
(Output Resistance Terminals 12,13,14)	(R_{OUT})	Output current = 50μA, 7207A only			33K	Ω
Input Pulldown Current	I_{pd}	Terminal 11 connected to V+		50	200	μA
Input Noise Immunity			25			% supply voltage
Oscillator Frequency Range	f_{osc}	Note 2	2		10	MHz
Oscillator Stability	f_{STAB}	$C_{IN} = C_{OUT}$ = 22pF		0.2	1.0	ppm/V
Oscillator Feedback Resistance	r_{OSC}	Quartz crystal open circuit Note 3	3			MΩ

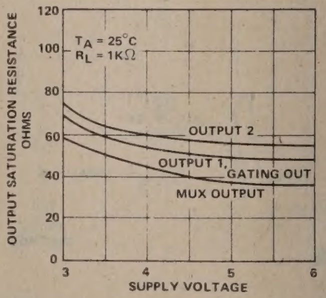
NOTE 2: Dynamic dividers are used in the initial stages of the divider chain. These dividers have a lower frequency of operation determined by transistor sizes, threshold voltages and leakage currents.

NOTE 3: The feedback resistor has a non-linear value determined by the oscillator instantaneous input and output voltage voltages and the supply voltage.

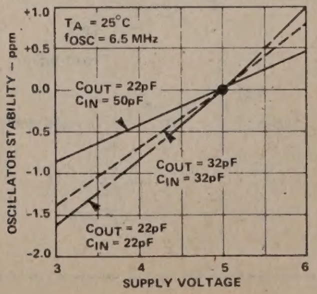
SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



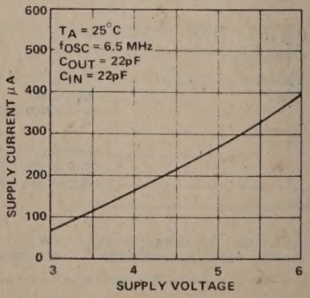
OUTPUT SATURATION RESISTANCES AS A FUNCTION OF SUPPLY VOLTAGE



OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE

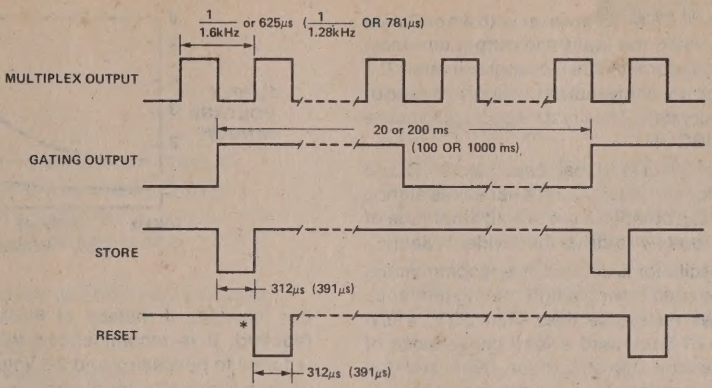


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT TIMING WAVEFORMS 7207/A

Crystal Frequency = 6.5536/5.24288MHz


$\frac{1}{1.6\text{kHz}}$ or 625μs ($\frac{1}{1.28\text{kHz}}$ OR 781μs)
MULTIPLEX OUTPUT
20 or 200 ms
(100 OR 1000 ms)
GATING OUTPUT
STORE
312μs (391μs)
RESET
*
312μs (391μs)

Referring to the test circuit, the crystal oscillator frequency is divided by 2^{12} to provide both the multiplex frequency and generate the output pulse widths. The GATING OUTPUT provides a 50% duty cycle signal whose period depends upon whether the RANGE CONTROL terminal is connected to V^+ or GROUND (open circuit).

*For ICM7207A this pulse is delayed 391μs.

TEST CIRCUIT

CRYSTAL PARAMETERS

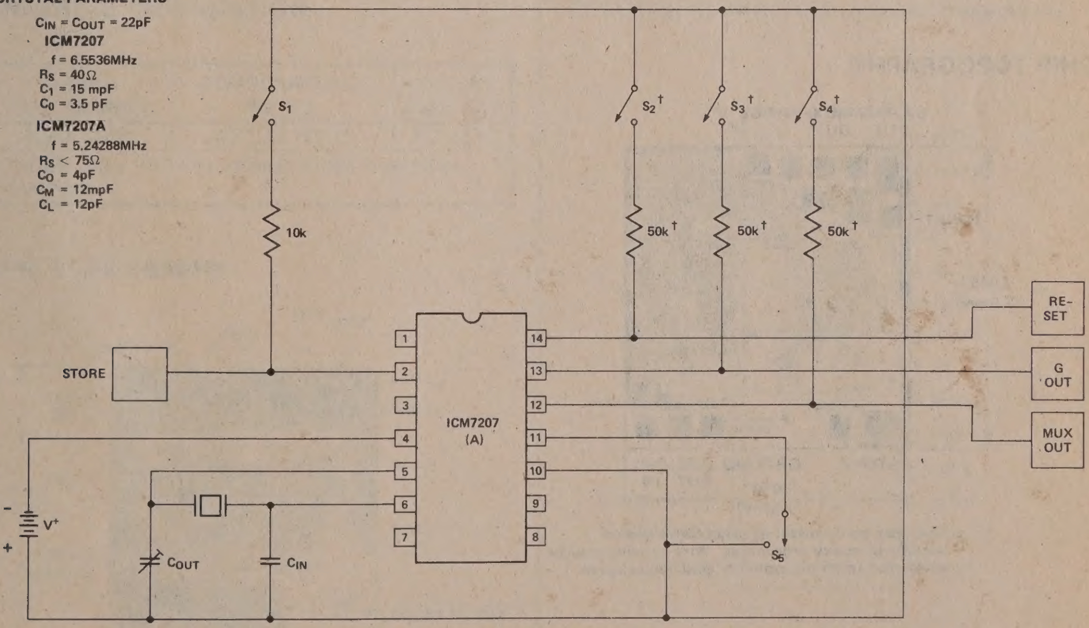
$C_{IN} = C_{OUT} = 22pF$

ICM7207

f = 6.5536MHz
$R_S = 40\Omega$
C_1 = 15 mpF
C_0 = 3.5 pF

ICM7207A

f = 5.24288MHz
$R_S < 75\Omega$
C_O = 4pF
C_M = 12mpF
C_L = 12pF


S1
S2 †
S3 †
S4 †
10k
50k †
50k †
50k †
STORE
1
2
3
4
5
6
7
14
13
12
11
10
9
8
ICM7207
(A)
RE-
SET
G
OUT
MUX
OUT
-
V+
+
COUT
CIN
S5

SWITCHES S_1, S_2, S_3, S_4 OPEN CIRCUIT FOR SUPPLY CURRENT MEASUREMENT.
SWITCH S_5 OPEN CIRCUIT FOR SLOW GATING PERIOD.

† SWITCHES S_2, S_3, S_4 and 50k RESISTORS ARE NOT NEEDED WHEN USING THE ICM7207A.

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a non-linear resistor connected between the input and output terminals to provide biasing. Oscillator stabilities of approximately 0.1 ppm per 0.1 volt change are achievable at a supply voltage of 5 volts, using low cost crystals. The crystal specifications are shown in the TEST CIRCUIT.

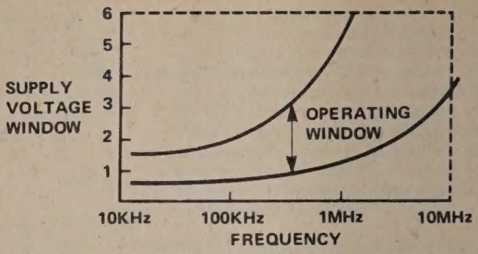
It is recommended that the crystal load capacitance (C_L) be no greater than 15pF for a crystal having a series resistance equal to or less than 75Ω, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10 ppm, a low series resistance (less than 25Ω), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C_{IN} should be 39pF and the oscillator tuning capacitor should range between approximately 8 and 60pF.

Use of a high quality crystal will result in typical oscillator stabilities of 0.05 ppm per 0.1 volt change of supply voltage.

FREQUENCY LIMITATIONS

The ICM7207/A uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but suffer from the disadvantage that there is a minimum operating frequency at a given supply voltage.

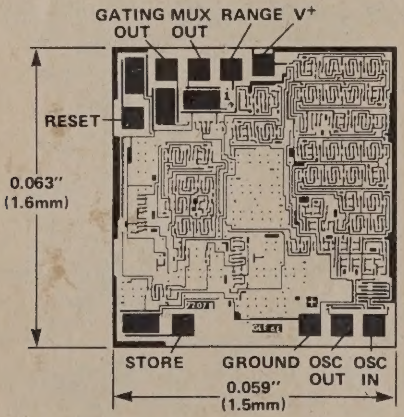


For example, if instead of 6.5MHz, a 1MHz oscillator is required, it is recommended that the supply voltage be reduced to between 2 and 2.5 volts. This may be realized by using a series resistor in series with the 5V positive supply line plus a decoupling capacitor. The quartz crystal parameters, etc., will determine the value of this resistor. NOTE: Except for the output open drain n-channel transistors no other terminal is permitted to exceed the supply voltage limits.

PRACTICAL FREQUENCY COUNTER

A complete frequency counter using the ICM7207/A together with the ICM7208 Frequency Counter is described in the ICM7208 data sheet.

CHIP TOPOGRAPHY



Chip may be die attached using conventional eutectic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.

INTERSIL

ICM7208
CMOS 7 Decade Counter

FEATURES

- Low operating power dissipation < 10mW
- Low quiescent power dissipation < 5mW
- Counts and displays 7 decades
- Wide operating supply voltage range $2V \leq V^+ \leq 6V$
- Drives directly 7 decade multiplexed common cathode LED display
- Internal store capability
- Internal inhibit to counter input
- Test speedup point
- All terminals protected against static discharge

DESCRIPTION

The ICM7208 is a fully integrated seven decade counter-decoder-driver and is manufactured using Intersil's low voltage metal gate C-MOS process.

Specifically the ICM7208 provides the following on chip functions: a 7 decade counter, multiplexer, 7 segment decoder, digit & segment driver, plus additional logic for display blanking, reset, input inhibit, and display on/off.

For unit counter applications the only additional components are a 7 digit common cathode display, 3 resistors and a capacitor to generate the multiplex frequency reference, and the control switches.

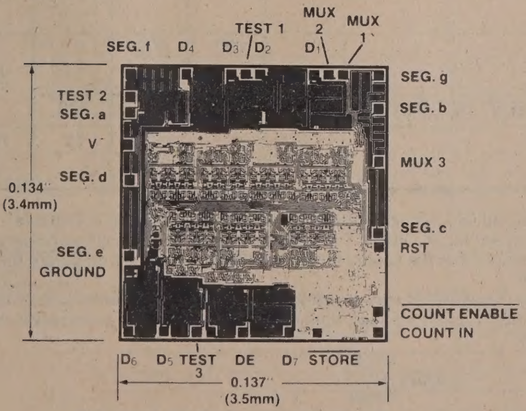
The ICM7208 is intended to operate over a supply voltage of 2 to 6 volts as a medium speed counter, or over a more restricted voltage range for high frequency applications.

As a frequency counter it is recommended that the ICM7208 be used in conjunction with the ICM7207 Oscillator Controller, which provides a stable HF oscillator, and output signal gating.

ORDERING INFORMATION

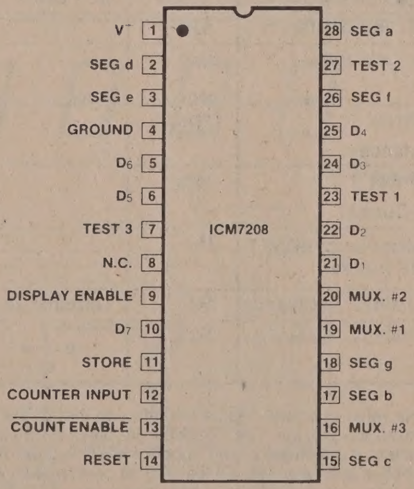
ORDER PART NUMBER	TEMPERATURE RANGE	28 LEAD PACKAGE
ICM7208IPI	-20°C to +85°C	PLASTIC
ORDER DICE BY FOLLOWING PART NUMBER: ICM7208D		

CHIP TOPOGRAPHY


SEG. f
D4
TEST 1
D3
D2
MUX 2
D1
MUX 1
SEG. g
SEG. b
MUX 3
SEG. c
RST
COUNT ENABLE
COUNT IN
TEST 2
SEG. a
V-
SEG. d
0.134" (3.4mm)
SEG. e
GROUND
D6
D5
TEST 3
DE
D7
STORE
0.137" (3.5mm)

Chip may be die attached using conventional eutectic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.

PIN CONFIGURATION (OUTLINE DRAWING PI)


V- 1
SEG d 2
SEG e 3
GROUND 4
D6 5
D5 6
TEST 3 7
N.C. 8
DISPLAY ENABLE 9
D7 10
STORE 11
COUNTER INPUT 12
COUNT ENABLE 13
RESET 14
ICM7208
28 SEG a
27 TEST 2
26 SEG f
25 D4
24 D3
23 TEST 1
22 D2
21 D1
20 MUX. #2
19 MUX. #1
18 SEG g
17 SEG b
16 MUX. #3
15 SEG c

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) .... 1 W
Supply voltage (Note 2) 6V
Output digit drive current (Note 3) 150mA
Output segment drive current .... 30 mA
Input voltage range (any input terminal) (Note 2) ... Not to exceed the supply voltage
Operating temperature range .... -20°C to +85°C
Storage temperature range .... –55°C to +125°C
Lead temperature (soldering, 10 seconds) .... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL OPERATION CHARACTERISTICS

TEST CONDITIONS: (V^+ = 5V, T_A = 25°C, TEST CIRCUIT, display off, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current	I_Q	All controls plus terminal 19 connected to V^+. No multiplex oscillator		30	100	µA
Quiescent Current	I_Q	All control inputs plus terminal 19 connected to V^+ except STORE which is connected to GROUND		70	150	
Operating Supply Current	I^+	All inputs connected to V^+, RC multiplexer osc operating $f_{in} < 25KHz$		210	500	
Operating Supply Current	I^+	$f_{in} = 2MHz$			700	
Supply Voltage Range	V^+	$f_{in} \leq 2MHz$	3.5		5.5	V
Digit Driver On Resistance	r_{DIG}			4	12	Ω
Digit Driver Leakage Current	I_{DIG}				500	µA
Segment Driver On Resistance	r_{SEG}			40		Ω
Segment Driver Leakage Current	I_{SLK}				500	µA
Pullup Resistance of RESET or STORE Inputs	R_P		100	400		kΩ
COUNTER INPUT Resistance	R_{IN}	Terminal 12 either at V^+ or GROUND			100	
COUNTER INPUT Hysteresis Voltage	V_{HIN}			25	50	mV

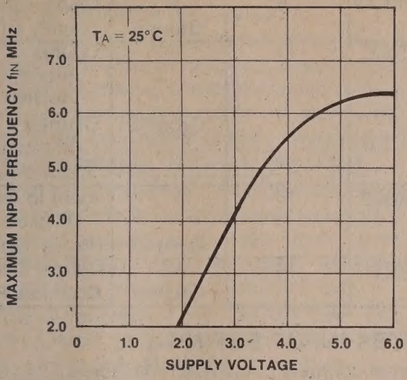
NOTE 1: This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

NOTE 2: The supply voltage must be applied before or at the same time as any input voltage. This poses no problems with a single power supply system. If a multiple power supply system is used, it is mandatory that the supply for the ICM7208 is switched on before the other supplies otherwise the device may be permanently damaged.

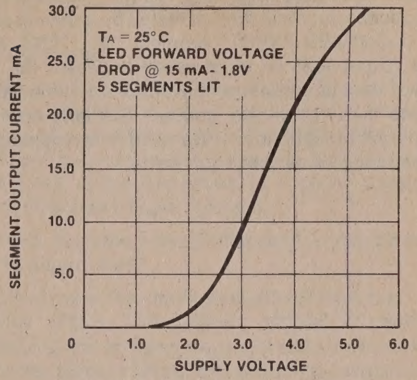
NOTE 3: The output digit drive current must be limited to 150mA or less under steady state conditions. (Short term transients up to 250mA will not damage the device.) Therefore, depending upon the LED display and the supply voltage to be used it may be necessary to include additional segment series resistors to limit the digit currents.

TYPICAL PERFORMANCE CHARACTERISTICS

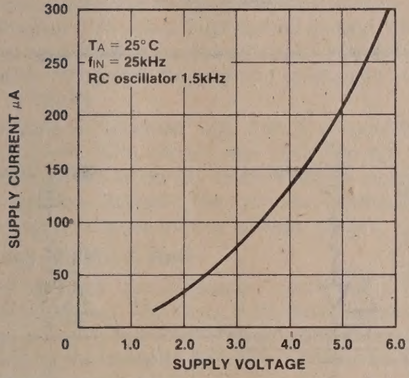
MAXIMUM COUNTER INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



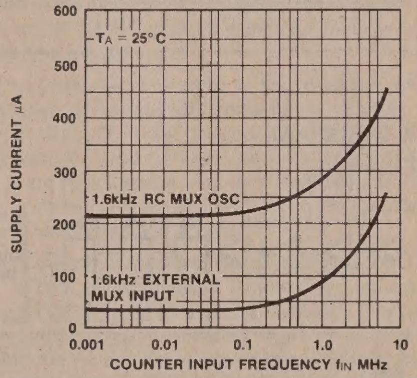
SEGMENT OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



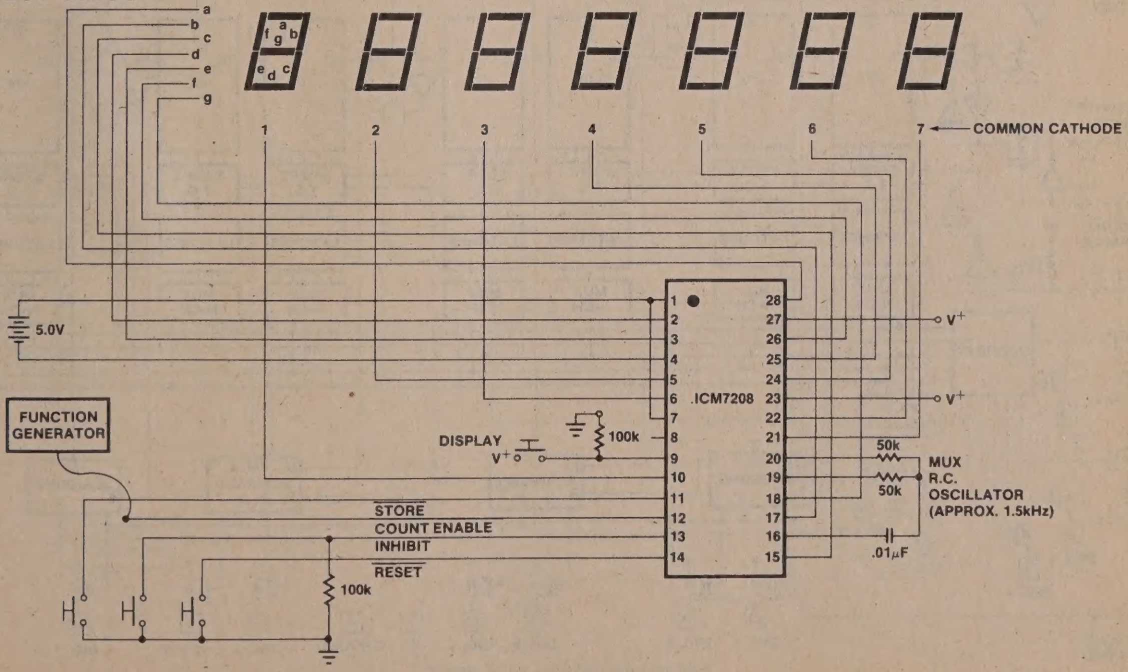
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



SUPPLY CURRENT AS A FUNCTION OF COUNTER INPUT FREQUENCY



TEST CIRCUIT


a
b
c
d
e
f
g
a
f g b
e d c
1
2
3
4
5
6
7
COMMON CATHODE
5.0V
FUNCTION GENERATOR
ICM7208
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
V+
V+
DISPLAY
V+
100k
50k
50k
MUX R.C. OSCILLATOR (APPROX. 1.5kHz)
.01μF
STORE
COUNT ENABLE
INHIBIT
RESET
100k

TEST PROCEDURES

The ICM7208 is provided with three input terminals 7, 23, 27 which may be used to accelerate testing. The least two significant decade counters may be tested by applying an input to the 'COUNTER INPUT' terminal 12. 'TEST POINT' terminal 23 provides an input which bypasses the 2 least significant decade counters and permits an injection of a signal into the third decade counter. Similarly terminals 7 and 27 permit rapid counter advancing at two points further along the string of decade counters.

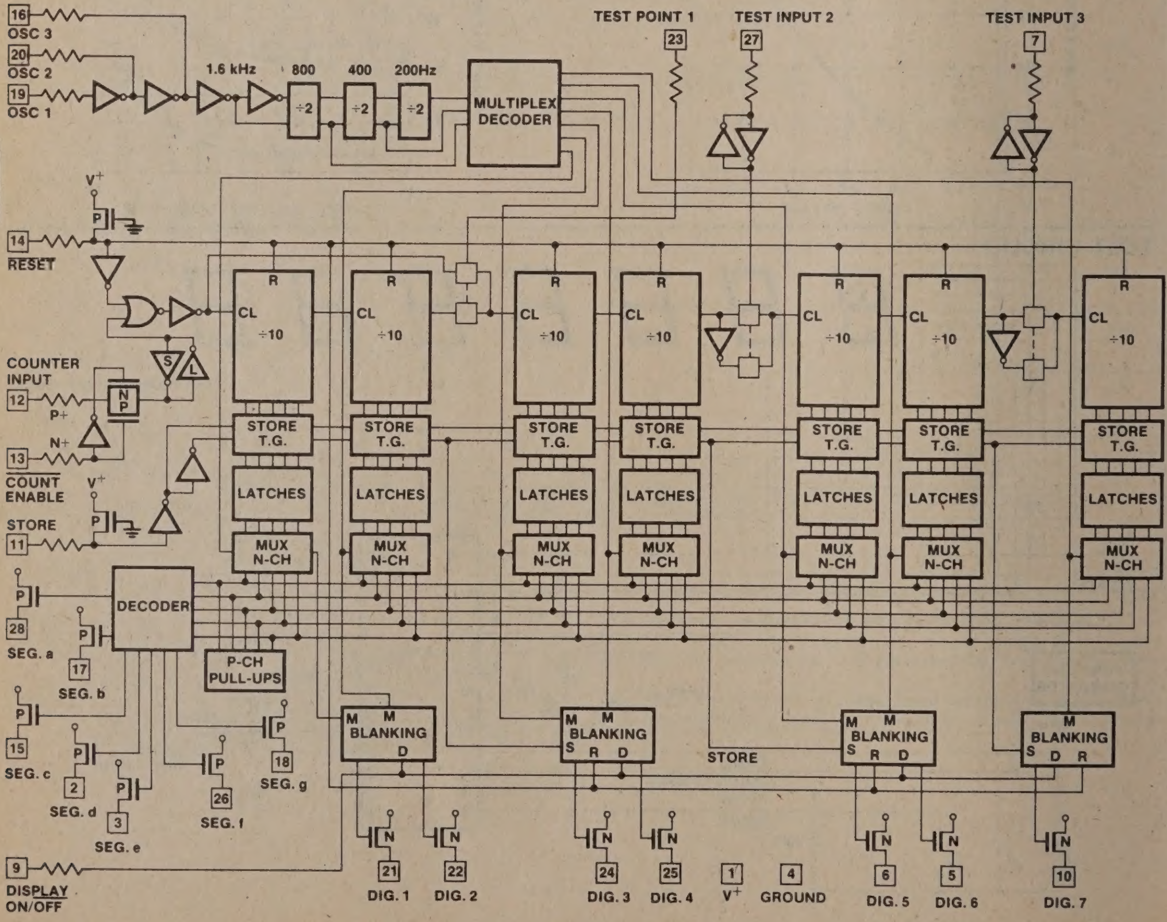
CONTROL INPUT DEFINITIONS

INPUT	TERMINAL	VOLTAGE	FUNCTION
1. DISPLAY	9	V⁺ Ground	Display On Display Off
2. $\overline{\text{STORE}}$	11	V⁺ Ground	Counter Information Latched Counter Information Transferring
3. $\overline{\text{ENABLE}}$	13	V⁺ Ground	Input to Counter Blocked Normal Operation
4. $\overline{\text{RESET}}$	14	V⁺ Ground	Normal Operation Counters Reset

COUNTER INPUT DEFINITION

The internal counters of the ICM7208 index on the negative edge of the input signal at terminal #12.

BLOCK DIAGRAM


16
OSC 3
20
OSC 2
19
OSC 1
1.6 kHz
800
400
200Hz
÷2
÷2
÷2
MULTIPLEX DECODER
TEST POINT 1
23
TEST INPUT 2
27
TEST INPUT 3
7
V⁺
P
14
RESET
COUNTER INPUT
12
N
P
P+
N+
S
L
13
COUNT ENABLE
V⁺
STORE
11
R
CL
÷10
STORE T.G.
LATCHES
MUX N-CH
DECODER
P-CH PULL-UPS
28
SEG. a
17
SEG. b
15
SEG. c
2
SEG. d
3
SEG. e
26
SEG. f
18
SEG. g
M
BLANKING
S
R
D
STORE
N
9
DISPLAY ON/OFF
21
DIG. 1
22
DIG. 2
24
DIG. 3
25
DIG. 4
1
V⁺
4
GROUND
6
DIG. 5
5
DIG. 6
10
DIG. 7

APPLICATION NOTES

1. Format of Signal to be Counted

The noise immunity of the COUNTER INPUT Terminal is approximately 1/3 the supply voltage. Consequently, the input signal should be at least 50% of the supply in peak to peak amplitude and preferably equal to the supply. **NOTE: The amplitude of the input signal should not exceed the supply; otherwise, damage may be done to the circuit.**

The optimum input signal is a 50% duty cycle square wave equal in amplitude to the supply. However, as long as the rate of change of voltage is not less than approximately 10^{-4}V/μsec at 50% of the power supply voltage, the input waveshape can be sinusoidal, triangular, etc.

When driving the input of the ICM7208 from TTL, a 1k-5k ohm pull-up resistor to the positive supply must be used to increase peak to peak input signal amplitude.

2. Display Considerations

Any common cathode multiplexable LED display may be used. However, if the peak digit current exceed 150 mA for any prolonged time, it is recommended that resistors be included in series with the segment outputs to limit digit current to 150mA.

The ICM7208 is specified with 500μA of possible digit leakage current. With certain new LED displays that are extremely efficient at low currents, it may be necessary to include resistors between the cathode outputs and the positive supply to bleed off this leakage current.

3. Display Multiplex Rate

The ICM7208 has approximately 0.5μs overlap between output drive signals. Therefore, if the multiplex rate is very fast, digit ghosting will occur. The ghosting determines the upper limit for the multiplex frequency. At very low multiplex rates flicker becomes visible.

It is recommended that the display multiplex rate be within the range of 50Hz to 200Hz, which corresponds to 400Hz to 1600Hz for the multiplex frequency input.

4. Unit Counter

The unit counter updates the display for each negative transition of the input signal. The information on the display will count, after reset, from 00 to 9,999,999 and then reset to 0000000 and begin to count up again. To blank leading zeros, actuate reset at the beginning of a count. Leading zero blanking affects two digits at a time.

For battery operated systems the display may be switched off to conserve power.

An external generator may be used to provide the multiplex frequency input. This signal, applied to terminal 19 (terminals 16 and 20 open circuit), should be approximately equal to the supply voltage, and should be a square wave for minimum of power dissipation.

For stand alone systems, two inverters are provided so that a simple but stable RC oscillator may be built using only 2 resistors and a capacitor.

Figure 1 shows the schematic of an extremely simple unit counter that can be used for remote traffic counting, to name one application. The power cell stack should consist of 3 or 4 nickel cadmium rechargeable cells (nominal 3.6 or 4.8 volts). If 4 x 1.5 volt cells are used it is recommended that a diode be placed in series with the stack to guarantee that the supply voltage does not exceed 6 volts.

The input switch is shown to be a single pole double throw switch (SPDT). A single pole single throw switch (SPST) could also be used (with a pullup resistor), however, anti-bounce circuitry must be included in series with the counter input. In order to avoid contact bounce problems due to the SPDT switch the ICM7208 contains an input latch on chip.

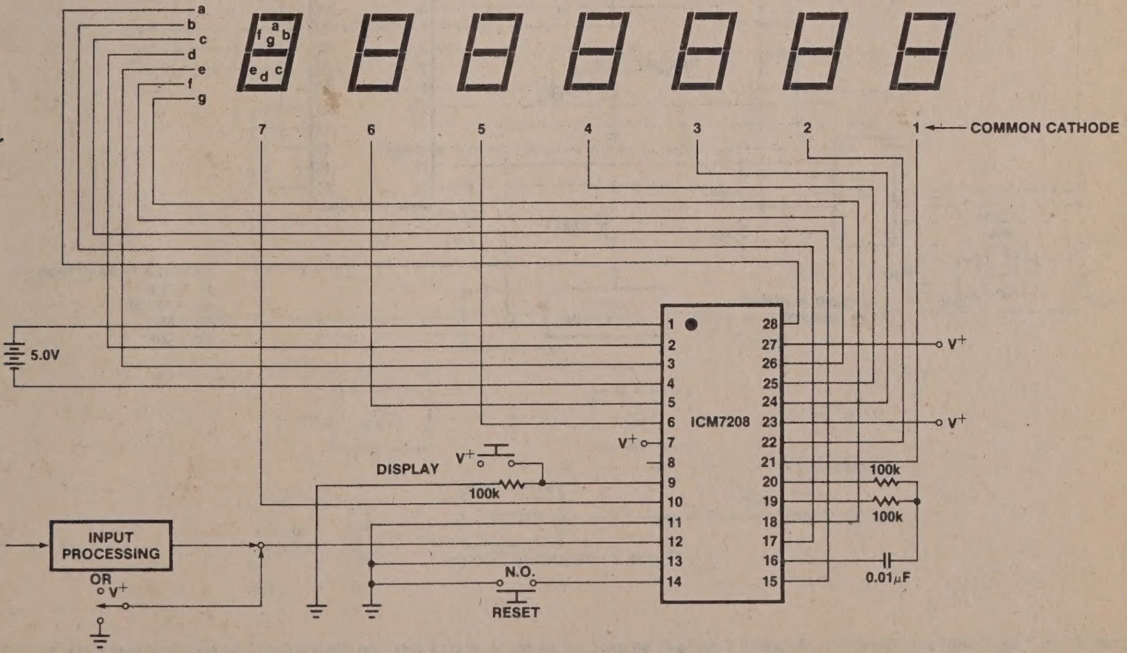


Figure 1: Schematic Unit Counter

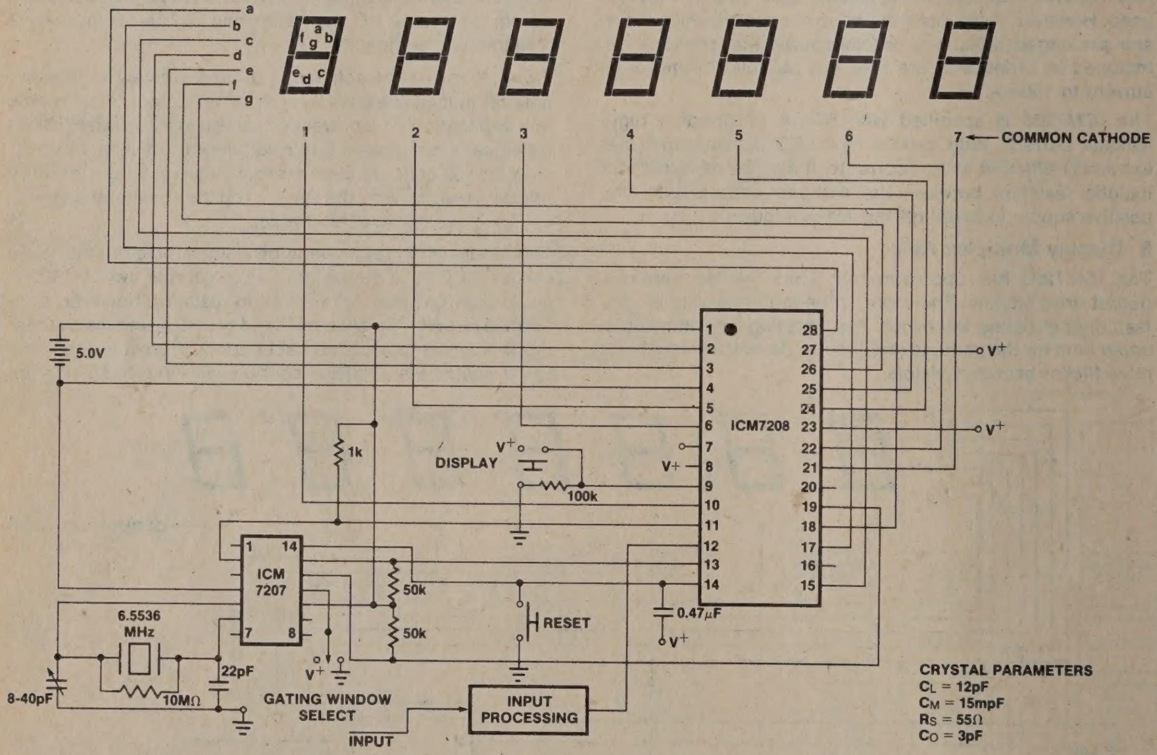
5. Frequency Counter

The ICM7208 may be used as a frequency counter when used with an external frequency reference and gating logic. This can be achieved using the ICM7207 Oscillator Controller (Figure 2). The ICM7207 uses a crystal controlled oscillator to provide the store and reset pulses together with the counting window. Figure 3 shows the recommended input gating waveforms to the ICM7208. At the end of a counting period (50% duty cycle) the counter input is inhibited. The counter information is then transferred and stored in latches, and can be displayed. Immediately after this information is stored, the counters are cleared and are ready to start a new count when the counter input is enabled.

Using a 6.5536mHz quartz crystal and the ICM7207 driving the ICM7208, two ranges of counting may be obtained, using either 0.01 sec or 0.1 sec counter enable windows.

Previous comments on leading zero blanking, etc., apply as per the unit counter.

The ICM7207 provides the multiplex frequency reference of 1.6kHz.


a
b
c
d
e
f
g
1
2
3
4
5
6
7 ← COMMON CATHODE
5.0V
ICM7208
V+
V+
1k
V+
DISPLAY
100k
V+
ICM 7207
1
14
7
8
50k
50k
RESET
0.47μF
V+
6.5536 MHz
22pF
8-40pF
10MΩ
V+
GATING WINDOW SELECT
INPUT PROCESSING
INPUT

CRYSTAL PARAMETERS
C_L = 12pF
C_M = 15mpF
R_S = 55Ω
C_O = 3pF

Figure 2: Frequency Counter

Note: For a 1 sec count window which allows all 7 digits to be used with a resolution of 1Hz, the ICM7207 can be replaced with the ICM7207A. Circuit details are given on the 7207A data sheet.

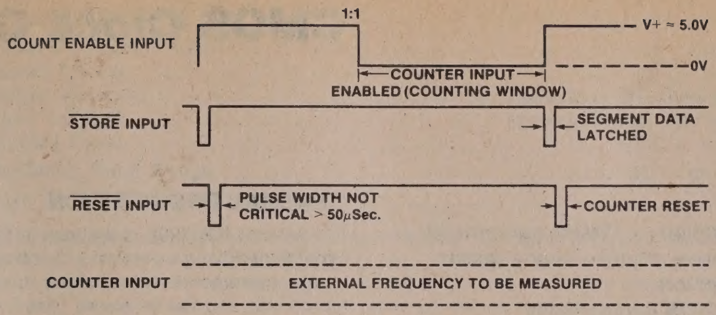

COUNT ENABLE INPUT
1:1
V+ ≈ 5.0V
0V
COUNTER INPUT ENABLED (COUNTING WINDOW)
STORE INPUT
SEGMENT DATA LATCHED
RESET INPUT
PULSE WIDTH NOT CRITICAL > 50μSec.
COUNTER RESET
COUNTER INPUT
EXTERNAL FREQUENCY TO BE MEASURED

Figure 3: Frequency Counter Input Waveforms

6. Period Counter

For this application, as opposed to the frequency counter, the gating and the input signal to be measured are reversed to the frequency counter. The input period is multiplied by two to produce a single polarity signal (50% duty cycle) equal to the input period, which is used to gate into the counter the frequency reference (1MHz in this case). Figure 5 shows a block schematic of the input waveform generator. The 1MHz frequency reference is generated by the ICM7209 Clock Generator using an 8MHz oscillator frequency and internally dividing this frequency by 8. Alternatively, a 1MHz signal could be applied directly to COUNTER INPUT. Waveforms are shown in Figure 4.

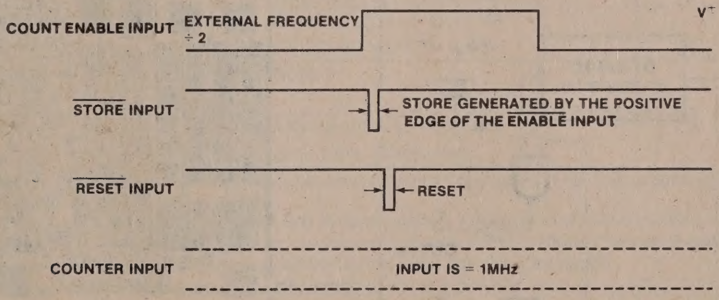

COUNT ENABLE INPUT
EXTERNAL FREQUENCY ÷ 2
V+
STORE INPUT
STORE GENERATED BY THE POSITIVE EDGE OF THE ENABLE INPUT
RESET INPUT
RESET
COUNTER INPUT
INPUT IS = 1MHz

Figure 4: Period Counter Input Waveforms

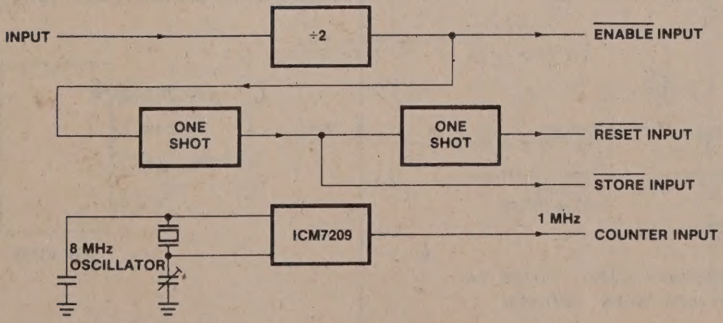

INPUT
÷2
ENABLE INPUT
ONE SHOT
ONE SHOT
RESET INPUT
STORE INPUT
ICM7209
1 MHz
COUNTER INPUT
8 MHz OSCILLATOR

Figure 5: Period Counter Input Generator

INTERSIL

ICM7209
CMOS Clock Generator

FEATURES

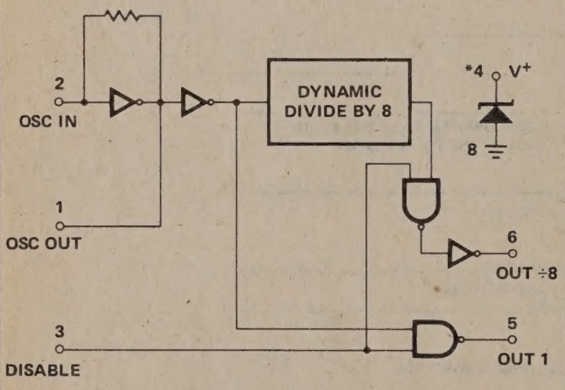
- High frequency operation — 10MHz guaranteed
- Easy to use oscillator — requires only a quartz crystal and two capacitors
- Bipolar, MOS and CMOS compatibility
- High output drive capability — 5 x TTL fanout with 10ns rise and fall times
- Low power — 50mW at 10MHz
- Choice of two output frequencies — osc., and osc. ÷8 frequencies
- Disable control for both outputs
- Wide industrial temperature range — −20°C to +85°C
- All inputs fully protected — circuits may be handled without any special precautions

GENERAL DESCRIPTION

The Intersil ICM7209 is a versatile CMOS clock generator capable of driving a number of 5 volt systems with a variety of input requirements. When used to drive up to 5 TTL gates, the typical rise and fall times are 10ns.

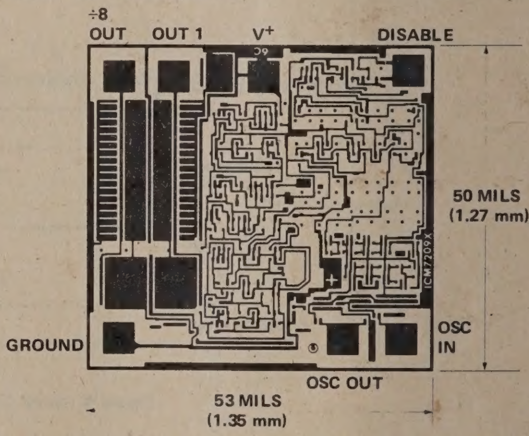
The ICM7209 consists of an oscillator, a buffered output equal to the oscillator frequency and a second buffered output having an output frequency one-eighth that of the oscillator. The guaranteed maximum oscillator frequency is 10MHz. Connecting the DISABLE terminal to the negative supply forces the ÷8 output into the '0' state and the output 1 into the '1' state.

SCHEMATIC DIAGRAM


2
OSC IN
1
OSC OUT
3
DISABLE
DYNAMIC DIVIDE BY 8
*4
V+
8
6
OUT ÷8
5
OUT 1

*ZENER VOLTAGE IS TYPICALLY 6.3 VOLTS

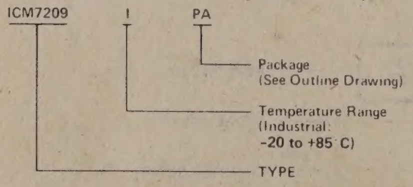
CHIP TOPOGRAPHY


÷8 OUT
OUT 1
V+
DISABLE
50 MILS (1.27 mm)
OSC IN
GROUND
OSC OUT
53 MILS (1.35 mm)

PADS 4.2 x 4.2 MILS^2 (.107 mm x .107 mm)

Chip may be die attached using conventional enteric or epoxy procedures. Wire bonding may be either Aluminum ultrasonic or Gold compression.

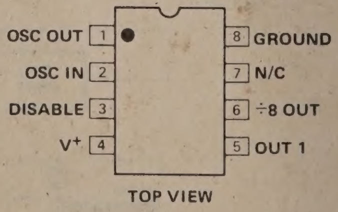
ORDERING INFORMATION


ICM7209
I
PA
Package (See Outline Drawing)
Temperature Range (Industrial: -20 to +85°C)
TYPE

Order Devices by Following Part Number ICM7209 I PA

Order Dice by Following Part Number · ICM7209 D

PIN CONFIGURATION (OUTLINE DRAWING PA)


OSC OUT 1
OSC IN 2
DISABLE 3
V+ 4
8 GROUND
7 N/C
6 ÷8 OUT
5 OUT 1
TOP VIEW

Pin 1 is designated by either a dot or a notch.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (25°C)	300mW
Supply Voltage	6 V
Output Voltages	Equal to or less than supply
Input Voltages	Equal to or less than supply
Storage Temp.	−55°C to +125°C
Operating Temp. Range	-20°C to +85°C
Lead Temp. (Soldering, 10 seconds)	300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5V \pm 10\%$, test circuit, $f_{osc} = 10MHz$, $T_A = 25°C$ unless otherwise specified.

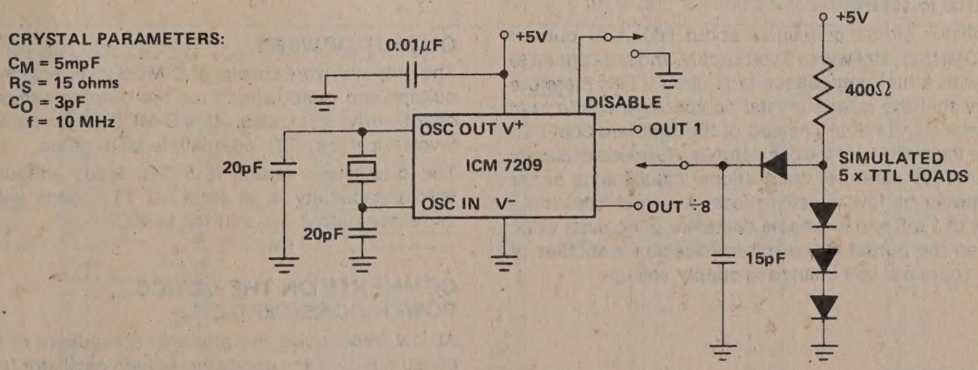
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNITS
Supply Current	I^+	Note 1 No Load		11	20	mA
Disable Input Capacitance	C_D				5	pF
Disable Input Leakage	I_{ILK}	Either '1' or '0' state			±10	μA
Output Low State	V_{OL}	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads			0.4	
Output High State	V_{OH}	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads	4.0	4.9		
Output Rise Time (Note 3)	t_r	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10	25	
Output Fall Time (Note 3)	t_f	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10	25	
Minimum OSC Frequency for ÷8 Output	f_{osc}	Note 2	2			
Output ÷8 duty cycle		Any operating frequency Low state : High state		7:9		

NOTE 1: The power dissipation is a function of the oscillator frequency (1st ORDER EFFECT see curve) but is also effected to a small extent by the oscillator tank components.

NOTE 2: The ÷8 circuitry uses a dynamic scheme. As with any dynamic system, information or data is stored on very small nodal capacitances instead of latches (static systems) and there is a lower cutoff frequency of operation. Dynamic dividers are used in the ICM7209 to significantly improve high frequency performance and to decrease power consumption.

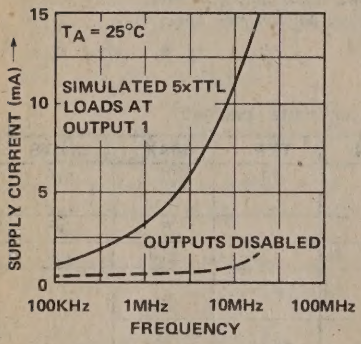
NOTE 3: Rise and fall times are defined between the output levels of 0.5 and 2.4 volts.

TEST CIRCUIT

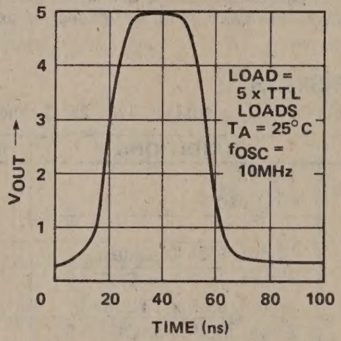


TYPICAL OPERATING CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY

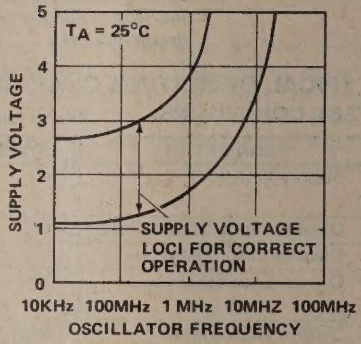


TYPICAL OUT 1 RISE AND FALL TIMES



Rise and fall times of OUT ÷8 are similar to those of OUT 1.

SUPPLY VOLTAGE RANGE FOR CORRECT OPERATION OF ÷8 COUNTER AS A FUNCTION OF OSCILLATOR FREQUENCY



APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator consists of a C-MOS inverter with a non-linear resistor connected between the oscillator input and output to provide D.C. biasing. Using commercially obtainable quartz crystals the oscillator will operate from low frequencies (10KHz) to 10MHz.

The oscillator circuit consumes about 500μA of current using a 10MHz crystal with a 5 volt supply, and is designed to operate with a high impedance tank circuit. It is therefore necessary that the quartz crystal be specified with a load capacitance (C_L) of 10pF instead of the standard 30pF. To maximize the stability of the oscillator as a function of supply voltage and temperature, the motional capacitance of the crystal should be low (5mpF or less). Using a fixed input capacitor of 18pF and a variable capacitor of nominal value of 18pF on the output will result in oscillator stabilities of typically 1ppm per volt change in supply voltage.

THE ÷8 OUTPUT

A dynamic divider is used to divide the oscillator frequency by 8. Dynamic dividers use small nodal capacitances to store voltage levels instead of latches (which are used in static dividers). The dynamic divider has advantages in high speed operation and low power but suffers from limited low frequency operation. This results in a window of operation for any oscillator frequency (see graph under TYPICAL OPERATING CHARACTERISTICS).

OUTPUT DRIVERS

The output drivers consist of C-MOS inverters having active pullups and pulldowns. Thus the outputs can be used to directly drive TTL gates, other C-MOS gates operating with a 5 volt supply, or TTL compatible MOS gates.

The guaranteed fanout is 5 TTL loads although typical fanout capability is at least 10 TTL loads with slightly increased output rise and fall times.

COMMENTS ON THE DEVICE POWER CONSUMPTION

At low frequencies the principal component of the power consumption is the oscillator. At high oscillator frequencies the major portion of the power is consumed by the output drivers, thus by disabling the outputs (activating the DISABLE INPUT) the device power consumption can be dramatically reduced.

ICM7211 (LCD)
ICM7212 (LED)
Four Digit CMOS Display Decoder/Drivers

ICM7211 (LCD) FEATURES

- **Four digit non-multiplexed 7 segment LCD display oututs with backplane driver**
- **Complete onboard RC oscillator to generate backplane frequency.**
- **Backplane input/output allows simple synchronization of slave-device segment outputs to a master backplane signal.**
- **ICM7211 devices provide separate digit select inputs to accept multiplexed BCD input (Pinout and functionally compatible with Siliconix DF411).**
- **ICM7211M devices provide data and digit select code input latches controlled by chip select inputs to provide a direct high speed processor interface.**
- **ICM7211 decodes binary to hexadecimal; ICM7211A decodes binary to Code B (0-9, dash, E, H, L, P, blank)**

ICM7212 (LED) FEATURES

- **28 current-limited segment outputs provide 4-digit non-multiplexed direct LED drive at > 5mA per segment.**
- **Brightness input allows direct control of LED segment current with a single potentiometer. Can function digitally as a display enable.**
- **ICM7212M and ICM7212A devices provide same input configuration and output decoding options as the ICM7211.**

DESCRIPTION

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs. These outputs provide the zero d.c. component signals necessary for long display life.

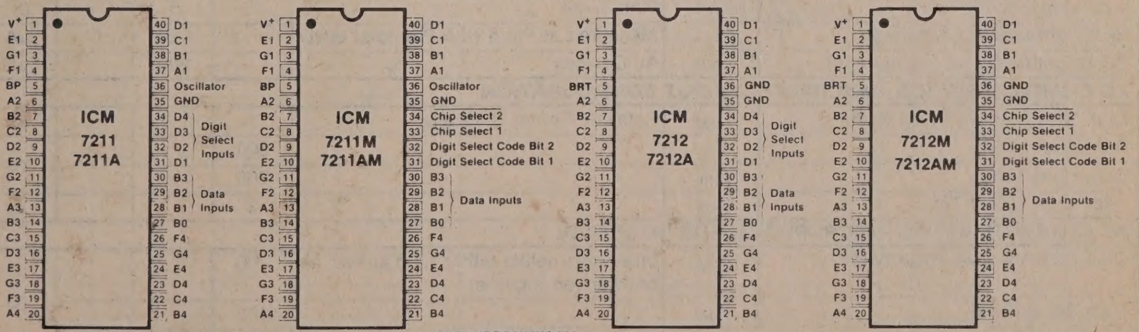
The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled low leakage open-drain n-channel outputs. These devices provide a BRIGHTNESS input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

Both the LCD and LED devices are available with two input configurations. The basic devices provide four data-bit inputs and four digit select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226 and ICL7103. The microprocessor interface (suffix M) devices provide data input latches and digit select code latches under control of high-speed chip select inputs. These devices simplify the task of implementing a cost-effective alphanumeric 7-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexa-decimal output. The "A" versions will provide the same output code as the ICM7218 "Code B", i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven segment decimal outputs.

Devices in the ICM7211/7212 family are packaged in a standard 40 pin plastic dual-in-line package and all inputs are fully protected against static discharge.

PIN CONFIGURATIONS (OUTLINE DRAWING PL)


ICM 7211 7211A
V+ 1
E1 2
G1 3
F1 4
BP 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
21 B4
22 C4
23 D4
24 E4
25 G4
26 F4
27 B0
28 B1
29 B2
30 B3
31 D1
32 D2
33 D3
34 D4
35 GND
36 Oscillator
37 A1
38 B1
39 C1
40 D1
Digit Select Inputs
Data Inputs
ICM 7211M 7211AM
V+ 1
E1 2
G1 3
F1 4
BP 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
21 B4
22 C4
23 D4
24 E4
25 G4
26 F4
27 B0
28 B1
29 B2
30 B3
31 Digit Select Code Bit 1
32 Digit Select Code Bit 2
33 Chip Select 1
34 Chip Select 2
35 GND
36 Oscillator
37 A1
38 B1
39 C1
40 D1
Data Inputs
ICM 7212 7212A
V+ 1
E1 2
G1 3
F1 4
BRT 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
21 B4
22 C4
23 D4
24 E4
25 G4
26 F4
27 B0
28 B1
29 B2
30 B3
31 D1
32 D2
33 D3
34 D4
35 GND
36 GND
37 A1
38 B1
39 C1
40 D1
Digit Select Inputs
Data Inputs
ICM 7212M 7212AM
V+ 1
E1 2
G1 3
F1 4
BRT 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
21 B4
22 C4
23 D4
24 E4
25 G4
26 F4
27 B0
28 B1
29 B2
30 B3
31 Digit Select Code Bit 1
32 Digit Select Code Bit 2
33 Chip Select 1
34 Chip Select 2
35 GND
36 GND
37 A1
38 B1
39 C1
40 D1
Data Inputs

(OUTLINE DRAWING PL)

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) .... 0.5 W @ 70°C
Supply Voltage 6.5V
Input Voltage (Any
Terminal) (Note 2) .... V^+ +0.3V, GROUND −0.3V
Operating Temperature Range .... −20°C to +85°C
Storage Temperature Range .... −55°C to +125°C
Lead Temperature (Soldering 10 sec.) .... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

TABLE I: OPERATING CHARACTERISTICS

TEST CONDITIONS: All parameters measured with $V^+ = 5V$

ICM7211 CHARACTERISTICS (LCD)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{op}	Test circuit, Display blank		10	50	μA
Oscillator Input Current	I_{OSCI}	Pin 36		±2	±10	
Segment Rise/Fall Time	t_{rfs}	$C_L = 200pF$		0.5		μs
Backplane Rise/Fall Time	t_{rfb}	$C_L = 5000pF$		1.5		
Oscillator Frequency	f_{osc}	Pin 36 Floating		16		kHz
Backplane Frequency	f_{bp}	Pin 36 Floating		125		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

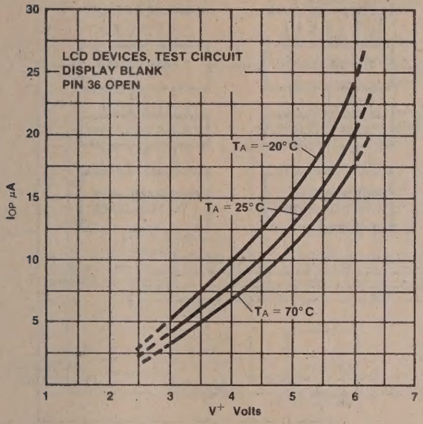
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pins 27-34 - GROUND		10	50	μA
Operating Current	I_{OP}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SLK}	Segment Off		±0.01	±1	μA
Segment On Current	I_{SEG}	Segment On, $V_O = +3V$	5	8		mA

INPUT CHARACTERISTICS

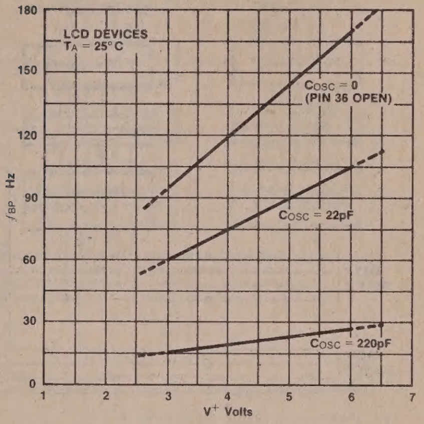
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" input voltage	V_{IH}		3			V
Logical "0" input voltage	V_{IL}				1	
Input leakage current	I_{ILK}	Pins 27-34		±.01	±1	μA
Input capacitance	C_{IN}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		±.01	±1	μA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1			μs
Data Setup Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		200			
Inter-Digit Select Time	t_{ids}		2			μs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{csa}	other chip select either held active, or both driven together	200			ns
Data Setup Time	t_{ds}		100			
Data Hold Time	t_{dh}		10	0		
Inter-Chip Select Time	t_{ics}		2			μs

TYPICAL CHARACTERISTICS

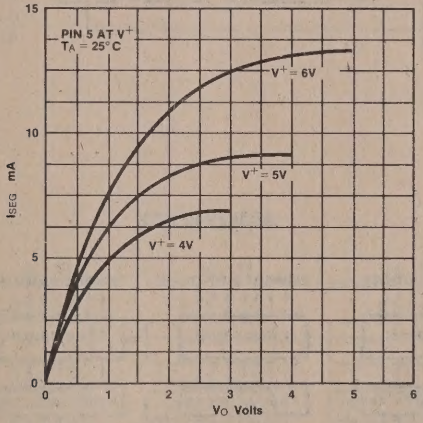
ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



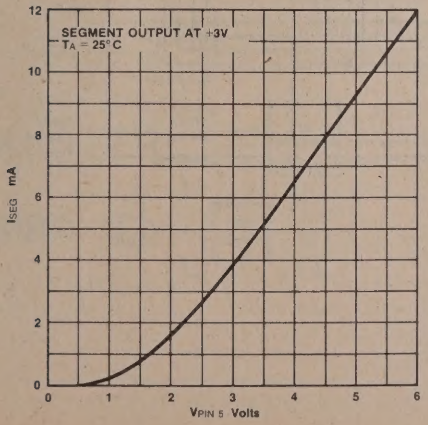
ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



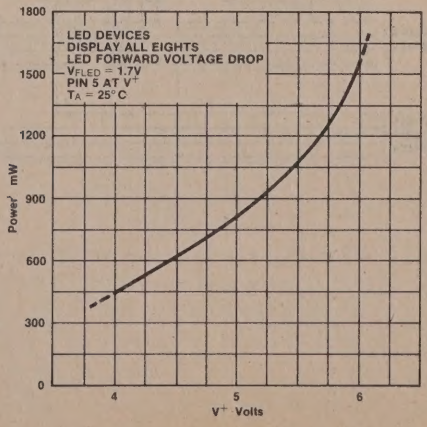
ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE

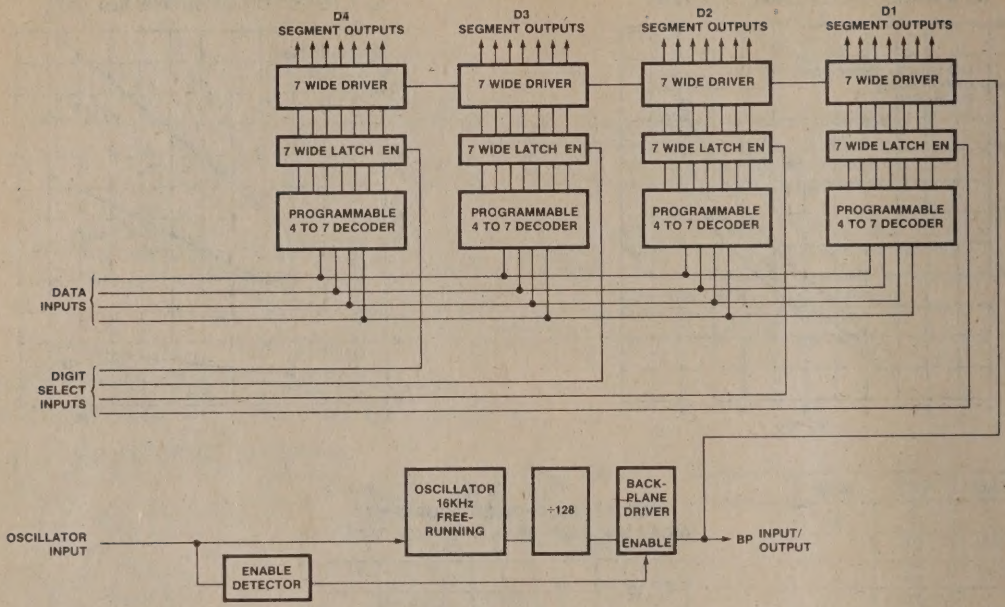


ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE

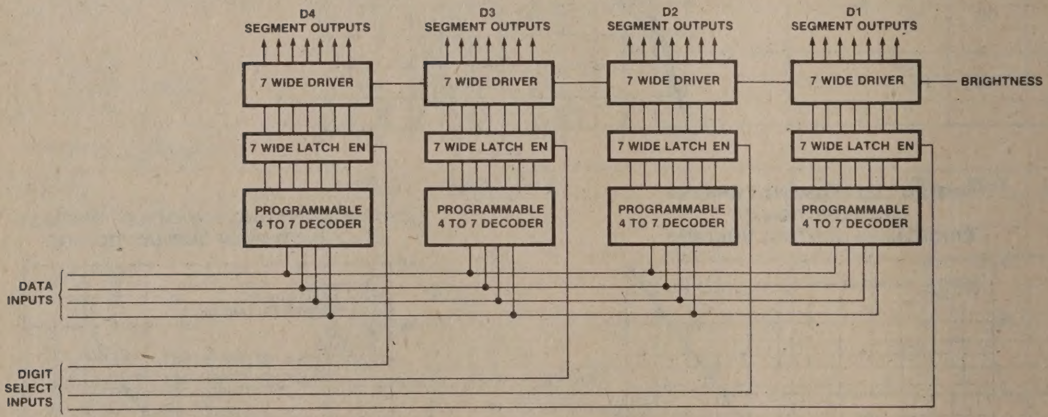


BLOCK DIAGRAMS

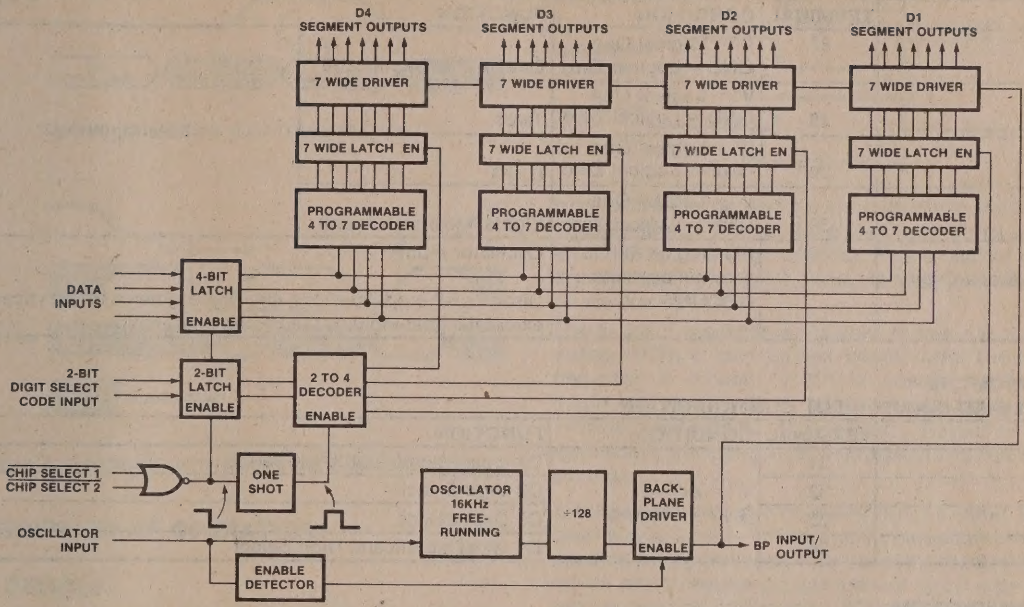
ICM7211 (A)


D4 SEGMENT OUTPUTS
D3 SEGMENT OUTPUTS
D2 SEGMENT OUTPUTS
D1 SEGMENT OUTPUTS
7 WIDE DRIVER
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUTS
DIGIT SELECT INPUTS
OSCILLATOR INPUT
OSCILLATOR 16KHz FREE-RUNNING
÷128
BACK-PLANE DRIVER
ENABLE
ENABLE DETECTOR
BP INPUT/ OUTPUT

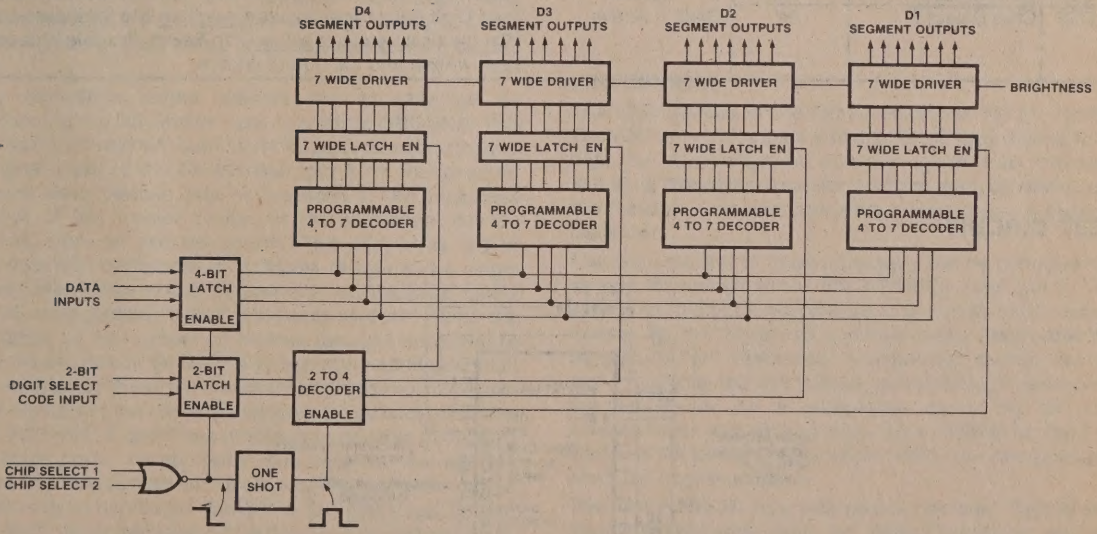
ICM7212 (A)


D4 SEGMENT OUTPUTS
D3 SEGMENT OUTPUTS
D2 SEGMENT OUTPUTS
D1 SEGMENT OUTPUTS
7 WIDE DRIVER
BRIGHTNESS
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUTS
DIGIT SELECT INPUTS

ICM7211(A)M


D4 SEGMENT OUTPUTS
D3 SEGMENT OUTPUTS
D2 SEGMENT OUTPUTS
D1 SEGMENT OUTPUTS
7 WIDE DRIVER
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUTS
4-BIT LATCH
ENABLE
2-BIT DIGIT SELECT CODE INPUT
2-BIT LATCH
ENABLE
2 TO 4 DECODER
ENABLE
CHIP SELECT 1
CHIP SELECT 2
ONE SHOT
OSCILLATOR INPUT
OSCILLATOR 16KHz FREE-RUNNING
÷128
BACK-PLANE DRIVER
ENABLE
BP INPUT/ OUTPUT
ENABLE DETECTOR

ICM7212(A)M


D4 SEGMENT OUTPUTS
D3 SEGMENT OUTPUTS
D2 SEGMENT OUTPUTS
D1 SEGMENT OUTPUTS
7 WIDE DRIVER
BRIGHTNESS
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUTS
4-BIT LATCH
ENABLE
2-BIT DIGIT SELECT CODE INPUT
2-BIT LATCH
ENABLE
2 TO 4 DECODER
ENABLE
CHIP SELECT 1
CHIP SELECT 2
ONE SHOT

INPUT DEFINITIONS

In this table, V+ and GROUND are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 1. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V^+ = Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logical One GND = Logical Zero	Twos	
B2	29	V^+ = Logical One GND = Logical Zero	Fours	
B3	30	V^+ = Logical One GND = Logical Zero	Eights (Most significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor GROUND	Oscillator input Disables BP output devices, allowing segments to be synced to an external signal input at the BP terminal (Pin 5)	

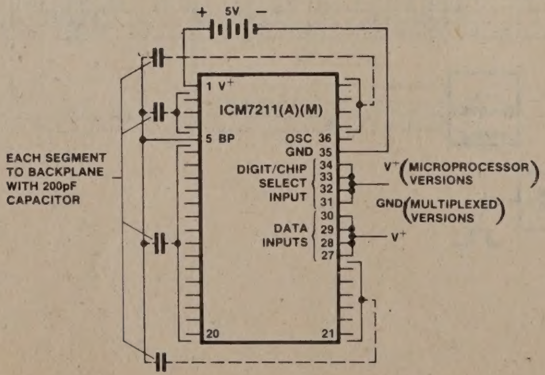
ICM7211/ICM7212
MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	CONDITION	FUNCTION
D1	31	V^+ = Active GND = Inactive	D1 (Least significant) Digit Select
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 (Most significant) Digit Select

ICM7211M/ICM7212M
MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	CONDITION	FUNCTION
DS1	Digit Select Code Bit 1 (LSB)	31	V^+ = Logical One GND = Logical Zero	DS1 & DS2 serve as a two bit Digit Select Code Input DS2, DS1 = 00 selects D4 DS2, DS1 = 01 selects D3 DS2, DS1 = 10 selects D2 DS2, DS1 = 11 selects D1
DS2	Digit Select Code bit 2 (MSB)	32		
$\overline{CS1}$	Chip Select 1	33	V = Inactive GND = Active	When both $\overline{CS1}$ and $\overline{CS2}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of either Chip Select, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34		

TEST CIRCUIT


+ 5V −
1 V+
ICM7211(A)(M)
5 BP
OSC 36
GND 35
DIGIT/CHIP SELECT INPUT
34
33
32
31
DATA INPUTS
30
29
28
27
20
21
EACH SEGMENT TO BACKPLANE WITH 200pF CAPACITOR
V+ (MICROPROCESSOR VERSIONS)
GND (MULTIPLEXED VERSIONS)
V+

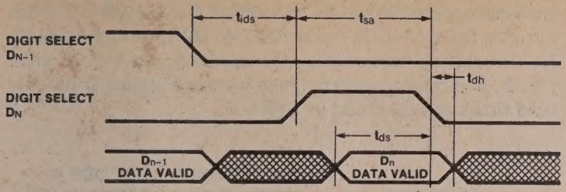


Figure 1: Multiplexed Input Timing Diagram

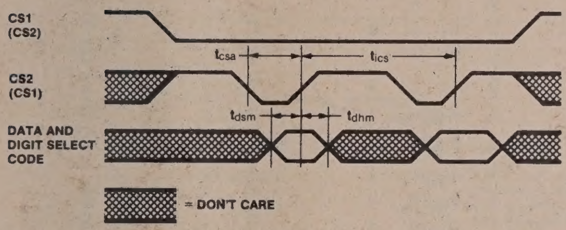
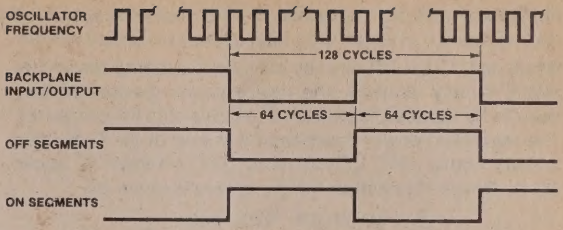


Figure 2: Microprocessor Interface Input Timing Diagram



Display Waveforms

DESCRIPTION OF OPERATION

LCD DEVICES

The LCD devices in the family (ICM7211, 7211A, 7211M, 7211AM) provide outputs suitable for driving conventional four-digit by seven-segment LCD displays, including 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to GROUND. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment), thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits; and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane output driver should handle the backplane to a display of 16 one-half-inch characters (rise and fall times not exceeding 5μs. ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7211 devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 16KHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor to the OSCillator terminal.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above GROUND). Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED DEVICES

The LED devices in the family (ICM7212, 7212A, 7212M, 7212AM) provide outputs suitable for directly driving four-digit by seven-segment common-anode LED displays, including 28 individual segment drivers, each consisting of a low-leakage, current-controlled, open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRIGHTNESS input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Fig (3). The potentiometer should be a high value (100KΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The BRIGHTNESS input may also be operated digitally as a display enable; when high, the display is fully on, and low fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two voltages at the Brightness input.

Note that the LED devices have two connections for GROUND; both of these pins should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (−15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^{+}-V_{FLED})\,(I_{SEG})\,(n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the Brightness input to keep power dissipation within the limits described above.

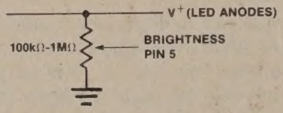


Figure 3: Brightness control

INPUT CONFIGURATIONS AND OUTPUT CODES

The standard devices in the ICM7211/12 family accept a four-bit true binary (ie, positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7211, ICM7211M, ICM7212, and ICM7212M devices decode this binary input into a seven-segment alphanumeric hexadecimal output, while the ICM7211A, ICM7211AM, ICM7212A, and ICM7212AM decode the binary input into the same seven-segment output as in the ICM7218 "Code B", ie 0-9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 2. Either decoder option will correctly decode true BCD to a seven-segment decimal output.

These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For larger quantity orders, (10K pcs. minimum) custom decoder options can be arranged. Contact the factory for details.

The ICM7211, ICM7211A, ICM7212, and ICM7212A devices are designed to accept multiplexed binary or BCD input. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30. More than one digit select may be activated simultaneously (which will write the same character into all selected digits), although the timing requirements shown in Fig (1) and Table 1 for data setup, hold, and inter-digit select times must be met to ensure correct output.

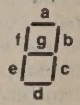
The ICM7211M, ICM7211AM, ICM7212M, and ICM7212AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the two-bit digit select code (DS1 pin 31, DS2 pin 32) are written into input buffer latches when both chip select inputs (CS1 pin 33, CS2 pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit select code latches. A select code of 00 writes into D4, SC2 = 0, SC1 = 1 writes into D3, SC2 = 1, SC1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Fig (2), and the chip select pulse widths and data setup and hold times are specified in Table 1.

BINARY				HEXADECIMAL ICM7211(M) ICM7212(M)	CODE B ICM7211A(M) ICM7212A(M)
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

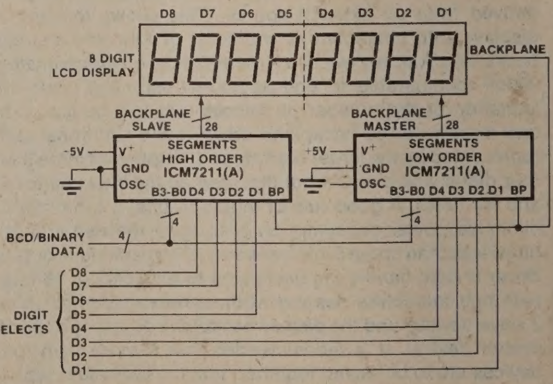
Table 2: Output Codes

SEGMENT ASSIGNMENT

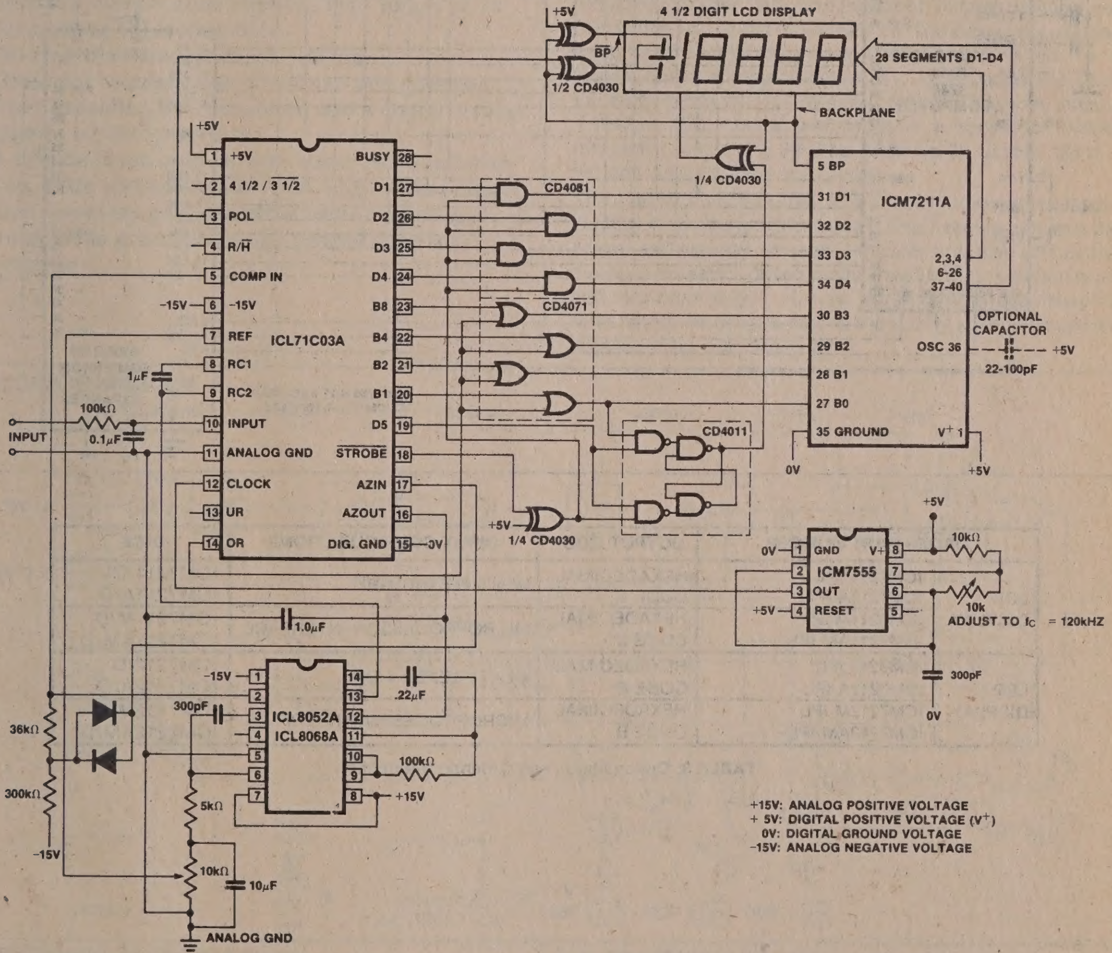


APPLICATIONS

1. Ganged ICM7211's Driving 8-Digit LCD Display.



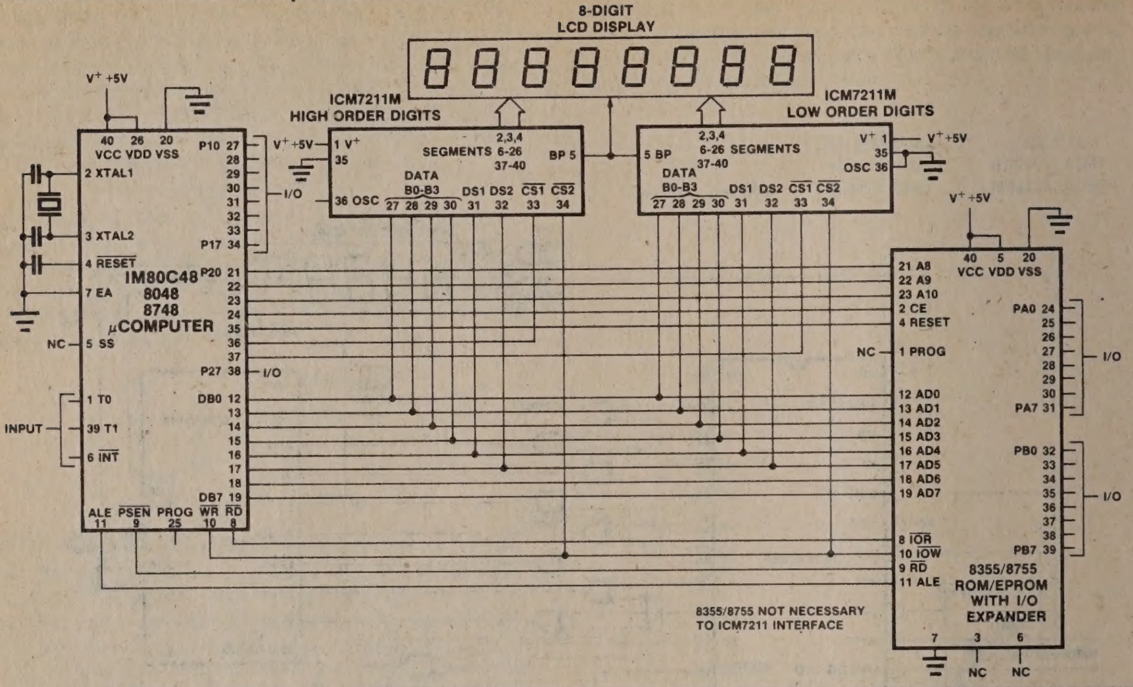
2. 4 1/2 Digit LCD DPM with Digit Blanking on Overrange.


+5V
4 1/2 DIGIT LCD DISPLAY
BP
1/2 CD4030
28 SEGMENTS D1-D4
BACKPLANE
1/4 CD4030
+5V
1 +5V
2 4 1/2 / 3 1/2
3 POL
4 R/H
5 COMP IN
-15V 6 -15V
7 REF
8 RC1
9 RC2
10 INPUT
11 ANALOG GND
12 CLOCK
13 UR
14 OR
ICL71C03A
BUSY 28
D1 27
D2 26
D3 25
D4 24
B8 23
B4 22
B2 21
B1 20
D5 19
STROBE 18
AZIN 17
AZOUT 16
DIG. GND 15 0V
CD4081
CD4071
CD4011
+5V
1/4 CD4030
5 BP
31 D1
32 D2
33 D3
34 D4
30 B3
29 B2
28 B1
27 B0
35 GROUND
ICM7211A
2,3,4
6-26
37-40
OSC 36
V+ 1
OPTIONAL CAPACITOR
22-100pF
+5V
0V
+5V
1μF
100kΩ
INPUT
0.1μF
1.0μF
+5V
0V 1 GND
2
3 OUT
+5V 4 RESET
ICM7555
V+ 8
7
6
5
10kΩ
10k
ADJUST TO fC = 120kHZ
300pF
0V
-15V 1
2
300pF 3
4
5
6
7
ICL8052A
ICL8068A
14
13
12
11
10
9
8 +15V
.22μF
100kΩ
36kΩ
300kΩ
-15V
5kΩ
10kΩ
10μF
ANALOG GND

+15V: ANALOG POSITIVE VOLTAGE
+ 5V: DIGITAL POSITIVE VOLTAGE (V+)
0V: DIGITAL GROUND VOLTAGE
-15V: ANALOG NEGATIVE VOLTAGE

NOTE: See also ICL8052/8068/ICL71C03 Data Sheet for a similar circuit with fewer features.

3. 8048/8748/IM87C48 Microprocessor Interface.


8-DIGIT
LCD DISPLAY
ICM7211M
HIGH ORDER DIGITS
ICM7211M
LOW ORDER DIGITS
V+ +5V
40 VCC
26 VDD
20 VSS
2 XTAL1
3 XTAL2
4 RESET
7 EA
NC 5 SS
IM80C48
8048
8748
μCOMPUTER
P10 27
P17 34
P20 21
P27 38
I/O
1 T0
39 T1
6 INT
INPUT
DB0 12
DB7 19
ALE 11
PSEN 9
PROG 25
WR 10
RD 8
1 V+
35
36 OSC
SEGMENTS 2,3,4 6-26 37-40
BP 5
DATA
B0-B3
27 28 29 30
DS1 31
DS2 32
CS1 33
CS2 34
5 BP
V+ 1
35
OSC 36
21 A8
22 A9
23 A10
2 CE
4 RESET
NC 1 PROG
12 AD0
13 AD1
14 AD2
15 AD3
16 AD4
17 AD5
18 AD6
19 AD7
8 IOR
10 IOW
9 RD
11 ALE
40 VCC
5 VDD
20 VSS
PA0 24
PA7 31
PB0 32
PB7 39
8355/8755
ROM/EPROM
WITH I/O
EXPANDER
7
3 NC
6 NC
8355/8755 NOT NECESSARY
TO ICM7211 INTERFACE

ORDER PART NUMBER		OUTPUT CODE	INPUT CONFIGURATIONS	DICE
LCD DISPLAY	ICM7211 IPL ICM7211A IPL	HEXADECIMAL CODE B	MULTIPLEXED 4-BIT	ICM7211/D ICM7211A/D
	ICM7211M IPL ICM7211AM IPL	HEXADECIMAL CODE B	MICROPROCESSOR INTERFACE	ICM7211M/D ICM7211AM/D
LED DISPLAY	ICM7212 IPL ICM7212A IPL	HEXADECIMAL CODE B	MULTIPLEXED 4-BIT	ICM7212/D ICM7212A/D
	ICM7212M IPL ICM7212AM IPL	HEXADECIMAL CODE B	MICROPROCESSOR INTERFACE	ICM7212M/D ICM7212AM/D

TABLE 3: Option Matrix and Ordering Information

INTERSIL

ICM7213
One Second/One Minute Precision Clock and Reference Generator

FEATURES

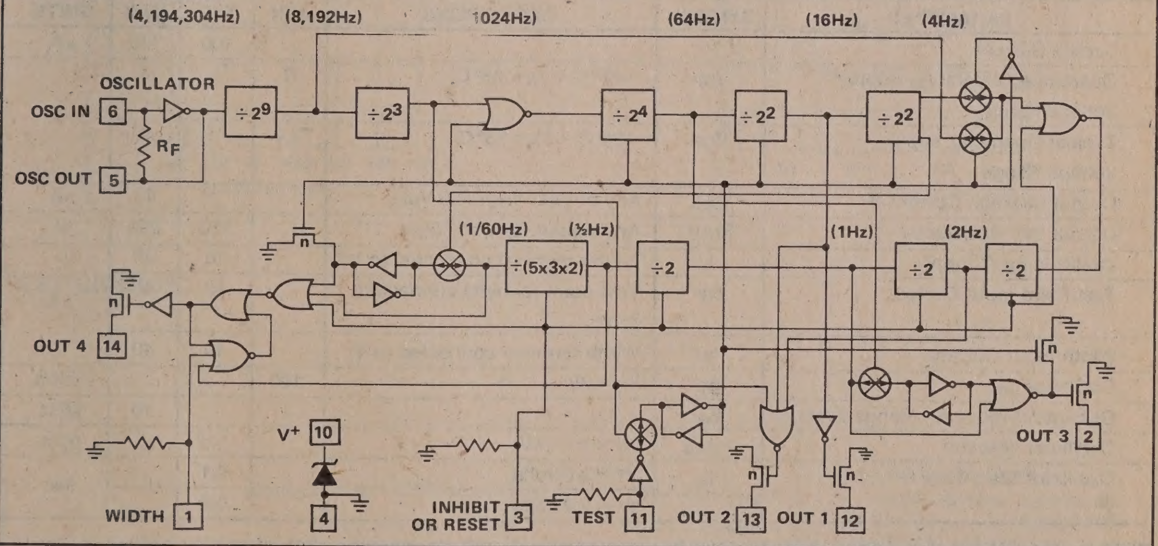
- **Guaranteed 2 volts operation**
- **Very low current consumption: Typ. 100μA @ 3V**
- **All outputs TTL compatible**
- **On chip oscillator feedback resistor**
- **Oscillator requires only 3 external components: fixed capacitor, trim capacitor, and a quartz crystal**
- **Output inhibit function**
- **4 simultaneous outputs: one pulse/sec, one pulse/min, 16Hz and composite 1024 + 16 + 2Hz outputs**
- **Test speed-up provides other frequency outputs**
- **Input static protection — no special handling required**

GENERAL DESCRIPTION

The ICM7213 is a fully integrated micropower oscillator and frequency divider with four buffered outputs suitable for interfacing with most logic families. The power supply may be either a two battery stack (Ni-cad, alkaline, etc.) or a regular power supply greater than 2 volts. Depending upon the state of the WIDTH, INHIBIT, and TEST inputs, using a 4.194304 MHz crystal will produce a variety of output frequencies including 2048 Hz, 1024 Hz, 34.133 Hz, 16 Hz, 1 Hz, and 1/60 Hz (plus composites).

The ICM7213 utilizes a very high speed low power metal gate C-MOS technology which uses 6.4 volt zeners between the drains and sources of each transistor and also across the supply terminals. Consequently, the ICM7213 is limited to a 6 volt maximum supply voltage, although a simple dropping network can be used to extend the supply voltage range well above 6 volts (see Figure 2).

BLOCK DIAGRAM


(4,194,304Hz)
(8,192Hz)
1024Hz)
(64Hz)
(16Hz)
(4Hz)
OSCILLATOR
OSC IN 6
R_F
OSC OUT 5
$\div 2^9$
$\div 2^3$
$\div 2^4$
$\div 2^2$
$\div 2^2$
n
(1/60Hz)
(½Hz)
÷(5x3x2)
÷2
(1Hz)
(2Hz)
÷2
÷2
OUT 4 14
V+ 10
4
WIDTH 1
INHIBIT OR RESET 3
TEST 11
OUT 2 13
OUT 1 12
OUT 3 2

ORDERING INFORMATION

ICM7213 I PD

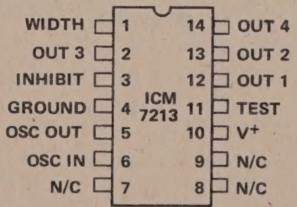
Package
PD = 14 Pin Plastic

Temperature Range
-20°C to +85°C

Type

Order Devices by Following Part Number
ICM7213IPD
Order Dice by Following Part Number
ICM7213D

PIN CONFIGURATION (OUTLINE DRAWING PD)


WIDTH 1
OUT 3 2
INHIBIT 3
GROUND 4
OSC OUT 5
OSC IN 6
N/C 7
14 OUT 4
13 OUT 2
12 OUT 1
11 TEST
10 V+
9 N/C
8 N/C
ICM 7213

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.0V
Output Current (Any output)	20mA
All Input and Oscillator Voltages (Note 1)	Equal to but not greater than the supply voltage
All Output Voltages (Note 1)	$0 \leq V_O \leq +6$
Operating Temperature Range	-20°C to +85°C
Storage Temperature Range	−40°C to +125°C
Power Dissipation (Note 2)	200mW
Lead Temperature (Soldering 10 sec.)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: The ICM7213 like most C-MOS devices, may enter a destructive latchup mode if an input or output voltage is applied in excess of those defined and there is no supply current limiting.

NOTE 2: Derate linearly power rating of 200mW at 25°C to 50mW at 70°C.

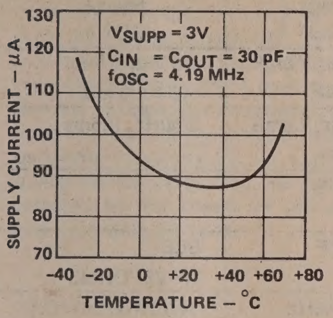
OPERATING CHARACTERISTICS

TEST CONDITIONS: $V+ = 3.0V$, $f_{osc} = 4.194304$ MHz, Test Circuit, $T_A = 25°C$ unless otherwise specified

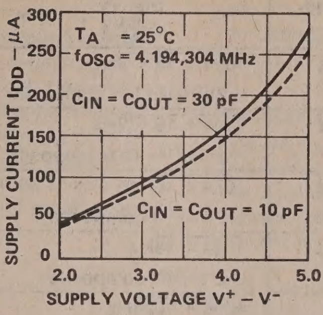
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I^+			100	140	µA
Guaranteed Operating Supply Voltage Range	V_{OP}	$-20°C < T_A < 85°C$	2		4	V
Typical Operating Supply Voltage Range	V_{OP}	$-20°C < T_A < 85°C$	1.4		5	
Output Leakage Current	I_{OLK}	Any output, $V_{OUT} = 6$ Volts			10	µA
Output Sat. Resistance	R_{OUT}	Any output, $I_{OLK} = 2.5mA$		120	200	Ω
Inhibit Input Current	I_I	Inhibit terminal connected to V^+		10	40	µA
Test Point Input Current	I_{TP}	Test point terminal connected to V^+		10	40	
Width Input Current	I_W	Width terminal connected to V^+		10	40	
Oscillator g_m	g_m	$V^+ = 2V$	100			umho
Oscillator Frequency Range (Note 3)	f_{osc}		1		10	MHz
Oscillator Stability	f_{STAB}	$2V < V^+ < 4V$		1.0		ppm
Oscillator Start Time	t_s	$V^+ = 3.0$ volts		0.1		sec
		$V^+ = 2.0$ volts		0.2		

NOTE 3: The ICM7213 uses dynamic dividers for high frequency division. As with any dynamic system, information is stored on very small nodal capacitances instead of latches (static system), therefore there is a lower frequency of operation. Dynamic dividers are used to improve the high frequency performance while at the same time significantly decreasing power consumption. At low supply voltages, operation at less than 1MHz is possible. See application notes.

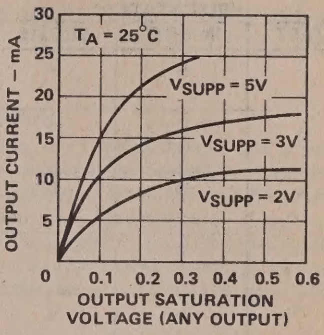
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



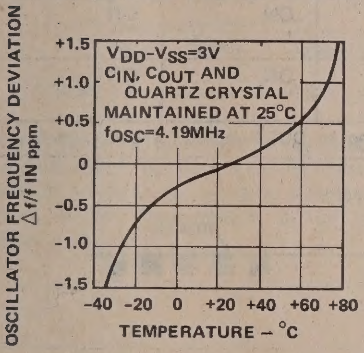
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



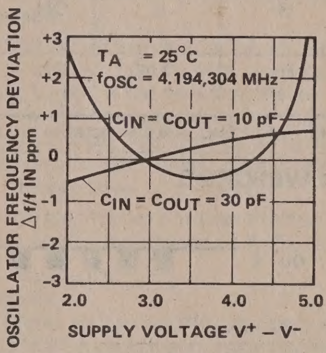
OUTPUT CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



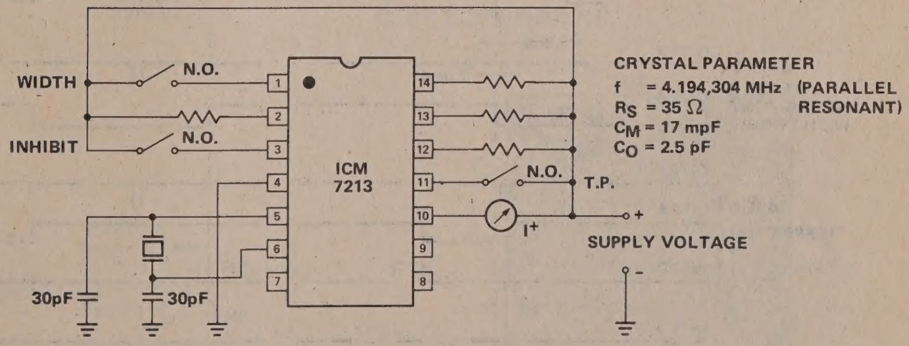
OSCILLATOR STABILITY AS A FUNCTION OF DEVICE TEMPERATURE



OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



TEST CIRCUIT


WIDTH
INHIBIT
N.O.
N.O.
N.O.
1
2
3
4
5
6
7
8
9
10
11
12
13
14
ICM 7213
T.P.
I+
+
SUPPLY VOLTAGE
-
30pF
30pF

CRYSTAL PARAMETER
f = 4.194,304 MHz (PARALLEL RESONANT)
R_S = 35 Ω
C_M = 17 mpF
C_O = 2.5 pF

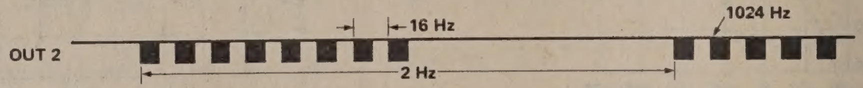
OUTPUT DEFINITIONS

TABLE I.

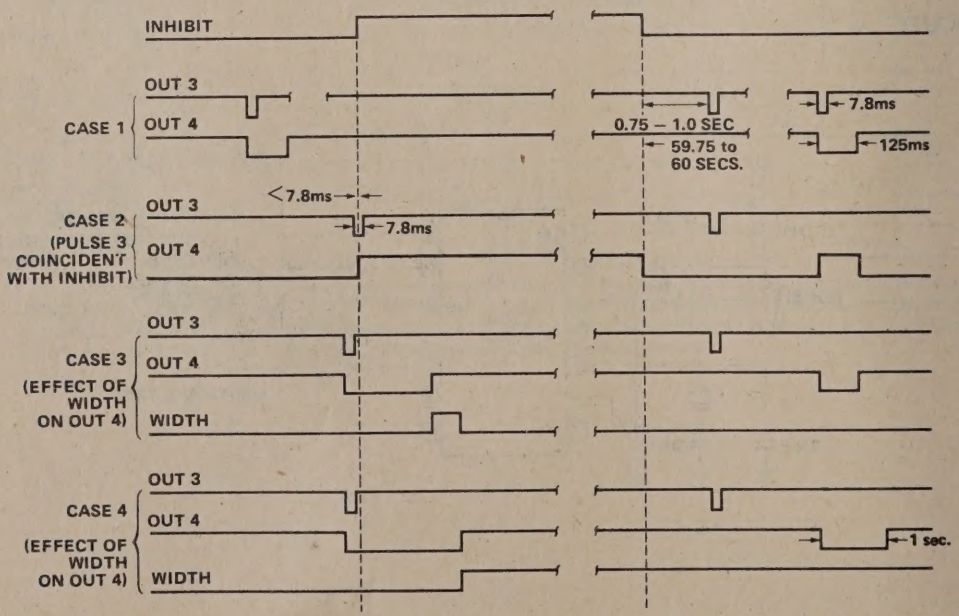
INPUT STATES*			PIN 12 OUT 1	PIN 13 OUT 2	PIN 2 OUT 3	PIN 14 OUT 4
TEST	INHIBIT	WIDTH				
L	L	L	16Hz ÷2^{18}	$\overline{1024 + 16 + 2}$Hz (÷2^{12}÷2^{18}÷2^{21}) composite	1Hz, 7.8mS ÷2^{22}	1/60Hz, 1 Sec. ÷(2^{26} x 3 x 5)
L	L	H	16Hz ÷2^{18}	$\overline{1024 + 16 + 2}$Hz (÷2^{12}÷2^{18}÷2^{21}) composite	1Hz, 7.8mS ÷2^{24}	1/60Hz, 125ms
L	H	L	16Hz ÷2^{18}	$\overline{1024 + 16}$Hz (÷2^{12}÷2^{18}) composite	OFF	OFF
L	H	H	16Hz ÷2^{18}	$\overline{1024 + 16}$Hz (÷2^{12}÷2^{18}) composite	OFF	SEE WAVEFORMS
H	L	L	ON	$\overline{4096 + 1024}$Hz (÷2^{10}÷2^{12}) composite	2048Hz ÷2^{11}	34.133Hz, 50% D.C. ÷(2^{13} x 5 x 3)
H	L	H	ON	$\overline{4096 + 1024}$Hz (÷2^{10}÷2^{12}) composite	2048Hz ÷2^{11}	34.133Hz, 50% D.C. ÷(2^{13} x 5 x 3)
H	H	L	ON	1024Hz ÷2^{12}	ON	ON
H	H	H	ON	1024Hz ÷2^{12}	ON	ON

NOTE: When TEST and RESET are connected to ground, or left open, all outputs except for OUT 3 and OUT 4 have a 50% duty cycle.

OUTPUT WAVEFORMS


OUT 2
16 Hz
1024 Hz
2 Hz

EFFECT OF INHIBIT INPUT TEST connected to ground or left open.


INHIBIT
OUT 3
CASE 1
OUT 4
0.75 – 1.0 SEC
59.75 to 60 SECS.
7.8ms
125ms
<7.8ms
OUT 3
CASE 2 (PULSE 3 COINCIDENT WITH INHIBIT)
OUT 4
7.8ms
OUT 3
CASE 3 (EFFECT OF WIDTH ON OUT 4)
OUT 4
WIDTH
OUT 3
CASE 4 (EFFECT OF WIDTH ON OUT 4)
OUT 4
WIDTH
1 sec.

All time scales are arbitrary, and in the case of OUT 3 only the pulses coinciding with the negative edge of OUT 4 are shown. Where time intervals are relevant they are clearly shown.

APPLICATIONS

1. Supply Voltage Considerations

The ICM7213 may be used to provide various precision outputs with frequencies from 2048Hz to 1/60Hz using a 4,194,304Hz quartz oscillator, and other output frequencies may be obtained using other quartz crystal frequencies. Since the ICM7213 uses dynamic high frequency dividers for the initial frequency division there are limitations on the supply voltage range depending on the oscillator frequency. If, for example, a low frequency quartz crystal is selected, the supply voltage should be selected in the center of the operating window, or approximately 1.7 volts.

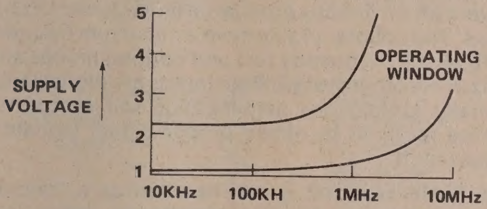
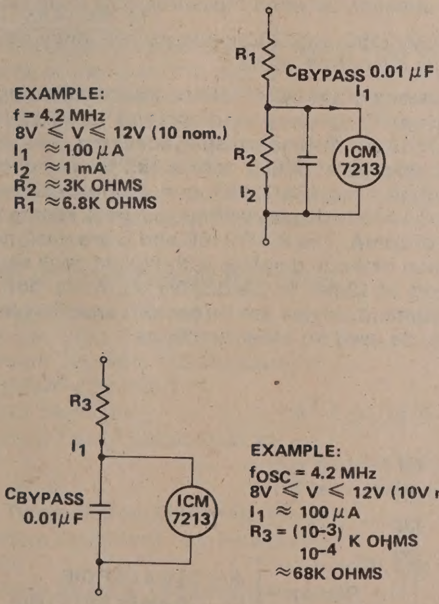


FIGURE 1: Window of Correct Operation

The supply voltage to the ICM7213 may be derived from a high voltage supply by using a simple resistor divider (if power is of no concern), by using a series resistor for minimum current consumption, or by means of a regulator.



EXAMPLE:
$f = 4.2$ MHz
$8V \leqslant V \leqslant 12V$ (10 nom.)
$I_1 \approx 100\,\mu A$
$I_2 \approx 1$ mA
$R_2 \approx 3K$ OHMS
$R_1 \approx 6.8K$ OHMS

EXAMPLE:
$f_{OSC} = 4.2$ MHz
$8V \leqslant V \leqslant 12V$ (10V nom)
$I_1 \approx 100\,\mu A$
$R_3 = \frac{(10-3)}{10^{-4}}$ K OHMS
$\approx 68K$ OHMS

FIGURE 2: Biasing Schemes with High Voltage Supplies

2. Logic Family Compatability

Pull up resistors will generally be required to interface with other logic families. These resistors must be connected between the various outputs and the positive power supply.

3. Oscillator Considerations

The oscillator consists of a C-MOS inverter and a feedback resistor whose value is dependent on the voltage at the oscillator input and output terminals and the supply voltage. Oscillator stabilities of approximately 0.1ppm per 0.1 volt variation are achievable with a nominal supply voltage of 5 volts and a single voltage dropping resistor. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (CL) be no greater than 22pF for a crystal having a series resistance equal to or less than 75 ohms, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10ppm, a low series resistance (less than 25 ohms), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C_{IN} should be 30pF and the oscillator tuning capacitor should range between approximately 16 and 60pF.

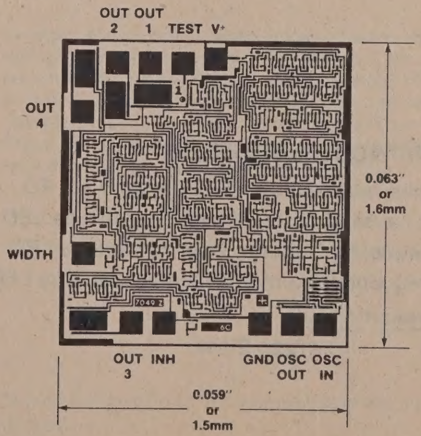
Use of a high quality crystal will result in typical stabilities of 0.05ppm per 0.1 volt change of supply voltage.

4. Control Inputs

The TEST input inhibits the 2^{18} output and applies the 2^9 output to the 2^{21} divider, thereby permitting a speedup of the testing of the ÷60 section by a factor of 2048 times. This also results in alternative output frequencies (see table).

The WIDTH input may be used to change the pulse width of OUT 4 from 125ms to 1 sec, or to change the state of OUT 4 from ON to OFF during INHIBIT.

CHIP TOPOGRAPHY



INTERSIL

ICM7216A/B/C/D 10 MHz Universal/ Frequency Counters

FEATURES

ALL VERSIONS:

- **Functions as a frequency counter. Measures frequencies from DC to 10 MHz**
- **Four internal gate times:**
  0.01 sec, 0.1 sec, 1 sec, 10 sec in frequency counter mode
- **Output directly drives digits and segments of large multiplexed LED displays. Common anode and common cathode versions**
- **Single nominal 5V supply required**
- **Stable high frequency oscillator, uses either 1 MHz or 10 MHz crystal**
- **Internally generated decimal points, interdigit blanking, leading zero blanking and overflow indication**
- **Display Off mode turns off display and puts chip into low power mode**
- **Hold and $\overline{\text{Reset}}$ inputs for additional flexibility**

ICM7216A AND B

- **Functions also as a period counter, unit counter, frequency ratio counter or time interval counter**
- **1 cycle, 10 cycles, 100 cycles, 1000 cycles in period, frequency ratio and time interval modes**
- **Measures period from 0.5μs to 10s**

ICM7216C AND D

- **Decimal point and leading zero blanking may be externally selected**

GENERAL DESCRIPTION

The ICM7216A and B are fully integrated Universal Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexers and 8 segment and 8 digit drivers which directly drive large multiplexed LED displays. The counter inputs have a maximum frequency of 10 MHz in frequency and unit counter modes and 2 MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10 MHz or 1 MHz quartz crystal timebase. For period and time interval, the 10MHz timebase gives a 0.1 μsec resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of 0.1 Hz in the least significant digit. There is 0.2 seconds between measurements in all ranges.

The ICM7216C and D function as frequency counters only, as described above.

All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in kHz. In the ICM7216A and B, time is displayed in μsec. The display is multiplexed at 500Hz with a 12.2% duty cycle for each digit. The ICM7216A and C are designed for common anode display with typical peak segment currents of 25mA. The ICM7216B and D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit and segment drivers are turned off, enabling the display to be used for other functions.

ORDERING INFORMATION

Universal Counter; Common Anode LED	**ICM 7216 A**	**IJI**
Universal Counter; Common Cathode LED	**ICM 7216 B**	**IPI**
Frequency Counter; Common Anode LED	**ICM 7216 C**	**IJI**
Frequency Counter; Common Cathode LED	**ICM 7216 D**	**IPI**

Type

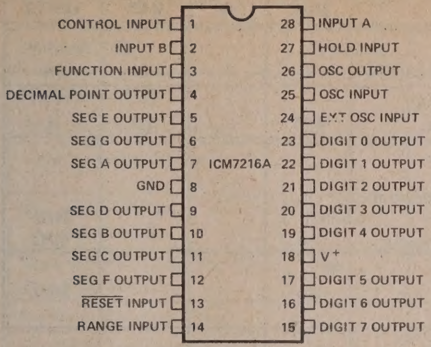
Package — JI — 28 pin CERDIP
PI — 28 pin PLASTIC DIP

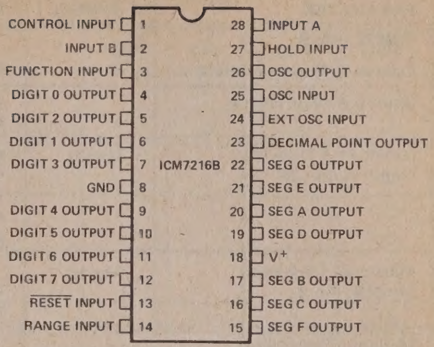
Temperature Range -20° C to +85° C

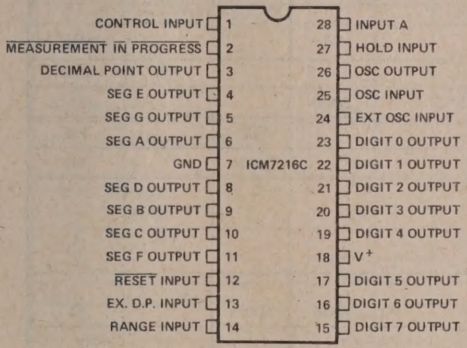
Evaluation Kit:

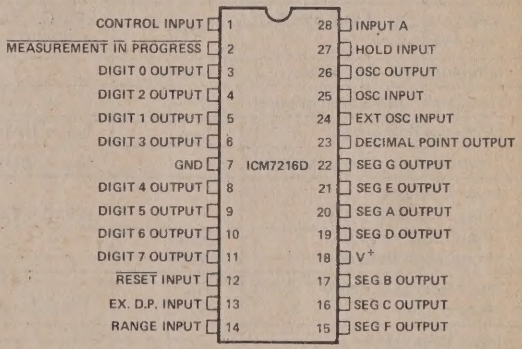
ICM7226 EV/Kit

PIN CONFIGURATIONS (OUTLINE DRAWINGS JI, PI)


ICM7216A
CONTROL INPUT 1
INPUT B 2
FUNCTION INPUT 3
DECIMAL POINT OUTPUT 4
SEG E OUTPUT 5
SEG G OUTPUT 6
SEG A OUTPUT 7
GND 8
SEG D OUTPUT 9
SEG B OUTPUT 10
SEG C OUTPUT 11
SEG F OUTPUT 12
RESET INPUT 13
RANGE INPUT 14
28 INPUT A
27 HOLD INPUT
26 OSC OUTPUT
25 OSC INPUT
24 EXT OSC INPUT
23 DIGIT 0 OUTPUT
22 DIGIT 1 OUTPUT
21 DIGIT 2 OUTPUT
20 DIGIT 3 OUTPUT
19 DIGIT 4 OUTPUT
18 V+
17 DIGIT 5 OUTPUT
16 DIGIT 6 OUTPUT
15 DIGIT 7 OUTPUT


ICM7216B
CONTROL INPUT 1
INPUT B 2
FUNCTION INPUT 3
DIGIT 0 OUTPUT 4
DIGIT 2 OUTPUT 5
DIGIT 1 OUTPUT 6
DIGIT 3 OUTPUT 7
GND 8
DIGIT 4 OUTPUT 9
DIGIT 5 OUTPUT 10
DIGIT 6 OUTPUT 11
DIGIT 7 OUTPUT 12
RESET INPUT 13
RANGE INPUT 14
28 INPUT A
27 HOLD INPUT
26 OSC OUTPUT
25 OSC INPUT
24 EXT OSC INPUT
23 DECIMAL POINT OUTPUT
22 SEG G OUTPUT
21 SEG E OUTPUT
20 SEG A OUTPUT
19 SEG D OUTPUT
18 V+
17 SEG B OUTPUT
16 SEG C OUTPUT
15 SEG F OUTPUT


ICM7216C
CONTROL INPUT 1
MEASUREMENT IN PROGRESS 2
DECIMAL POINT OUTPUT 3
SEG E OUTPUT 4
SEG G OUTPUT 5
SEG A OUTPUT 6
GND 7
SEG D OUTPUT 8
SEG B OUTPUT 9
SEG C OUTPUT 10
SEG F OUTPUT 11
RESET INPUT 12
EX. D.P. INPUT 13
RANGE INPUT 14
28 INPUT A
27 HOLD INPUT
26 OSC OUTPUT
25 OSC INPUT
24 EXT OSC INPUT
23 DIGIT 0 OUTPUT
22 DIGIT 1 OUTPUT
21 DIGIT 2 OUTPUT
20 DIGIT 3 OUTPUT
19 DIGIT 4 OUTPUT
18 V+
17 DIGIT 5 OUTPUT
16 DIGIT 6 OUTPUT
15 DIGIT 7 OUTPUT


ICM7216D
CONTROL INPUT 1
MEASUREMENT IN PROGRESS 2
DIGIT 0 OUTPUT 3
DIGIT 2 OUTPUT 4
DIGIT 1 OUTPUT 5
DIGIT 3 OUTPUT 6
GND 7
DIGIT 4 OUTPUT 8
DIGIT 5 OUTPUT 9
DIGIT 6 OUTPUT 10
DIGIT 7 OUTPUT 11
RESET INPUT 12
EX. D.P. INPUT 13
RANGE INPUT 14
28 INPUT A
27 HOLD INPUT
26 OSC OUTPUT
25 OSC INPUT
24 EXT OSC INPUT
23 DECIMAL POINT OUTPUT
22 SEG G OUTPUT
21 SEG E OUTPUT
20 SEG A OUTPUT
19 SEG D OUTPUT
18 V+
17 SEG B OUTPUT
16 SEG C OUTPUT
15 SEG F OUTPUT

EVALUATION KIT

The ICM7226 Universal Counter System has all of the features of the ICM7216 plus a number of additional features. The ICM7226 Evaluation Kit consists of the ICM7226AIDL (Common Anode LED Display), a 10 MHz quartz crystal, 8 each 7 segment .3" LED's, P.C. board, resistors, capacitors, diodes, switches, socket: everything needed to quickly assemble a functioning ICM7226 Universal Counter System.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage	6.5 Volts
Maximum Digit Output Current	400mA
Maximum Segment Output Current	60mA
Voltage On Any Input or Output Terminal(1)	$V^+ + .3V$ to $V^- - .3V$
Maximum Power Dissipation at 70°C	1.0 W (ICM7216A & C) 0.5 W (ICM7216B & D)
Lead Temperature (Soldering, 10 sec)	300°C
Maximum Operating Temperature Range	-20°C to +85°C
Maximum Storage Temperature Range	−55°C to +125°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. The ICM7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V^+ to V^- by more than 0.3 volts.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
ICM7216A/B						
Operating Supply Current	I^+	Display Off, Unused Inputs to GND		2	5	mA
Supply Voltage Range	V^+	$-20°C < T_A < +85°C$, Input A, Input B Frequency at F_{MAX}	4.75		6.0	V
Maximum Frequency Input A, Pin 28	$f_{A(max)}$	$-20°C < T_A < +85°C$ $4.75 < V^+ \leq 6.0V$, Figure 1, Function = Frequency, Ratio, Unit Counter	10			MHz
		Function = Period, Time Interval	2.5			MHz
Maximum Frequency Input B, Pin 2	$f_{B(max)}$	$-20°C < T_A < +85°C$ $4.75 < V^+ \leq 6.0V$, Figure 2	2.5			MHz
Minimum Separation Input A to Input B Time Interval Function		$-20°C < T_A < +85°C$ $4.75 < V^+ \leq 6.0V$, Figure 3	250			n
Maximum Osc. Freq. and Ext. Osc. Frequency	f_{osc}	$-20°C < T_A < +85°C$ $4.75 < V^+ \leq 6.0V$	10			MHz
Minimum Ext. Osc. Freq.	f_{osc}				100	kHz
Oscillator Transconductance	g_m	$V^+ - V^- = 4.75V$, $T_A = +85°C$	2000			μmhos
Multiplex Frequency	f_{mux}	$f_{osc} = 10MHz$		500		Hz
Time Between Measurements		$f_{osc} = 10MHz$		200		ms
Input Voltages: Pins 2,13,25,27,28		$-20°C < T_A < +85°C$				
Input Low Voltage	V_{INL}				1.0	V
Input High Voltage	V_{INH}		3.5			V
Input Resistance to V^+ Pins 13,24	R_{IN}	$V_{IN} = V^+ - 1.0V$	100K	400K		Ω
Input Leakage Pin 27,28,2	I_{ILK}				20	μA
Minimum Input Rate of Change	dV_{IN}/dt	Supplies Well Bypassed	25	15		mV/μs
ICM7216A						
Digit Driver: Pins 15,16,17,19,20,21,22,23						
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.0V$	-140	-180		mA
Low Output Current	I_{OL}	$V_{OUT} = +1.0V$		+0.3		mA
Segment Driver: Pins 4,5,6,7,9,10,11,12						
Low Output Current	I_{OL}	$V_{OUT} = +1.5V$	20	35		mA
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.5V$		-100		μA
Multiplex Inputs: Pins 1,3,14						
Input Low Voltage	V_{INL}				0.8	V
Input High Voltage	V_{INH}		2.0			V
Input Resistance to GROUND	R_{IN}	$V_{IN} = +1.0V$	50	100		kΩ
ICM7216B						
Digit Driver: Pins 4,5,6,7,9,10,11,12						
Low Output Current	I_{OL}	$V_{OUT} = +1.3V$	50	75		mA
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.5V$		-100		μA
Segment Driver: Pins 15,16,17,19,20,21,22,23						
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.0V$	-10			mA
Leakage Current	I_{SLK}	$V_{OUT} = V^+ - 2.5V$			10	μA
Multiplex Inputs: Pins 1,3,14						
Input Low Voltage	V_{INL}				$V^+ - 2.0$	V
Input High Voltage	V_{INH}		$V^+ - 0.8$			V
Input Resistance to V^+	R_{IN}	$V_{IN} = V^+ - 1.0V$	200	360		kΩ

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP	MAX.	UNITS
ICM7216C/D						
Operating Supply Current	I^+	Display Off, Unused Inputs to GND		2	5	mA
Supply Voltage Range		$-20°C < T_A < +85°C$, Input A Frequency at f_{max}	4.75		6.0	V
Maximum Frequency Input A, Pin 28	$f_{A(max)}$	$-20°C < T_A < +85°C$ $4.75 < V^+ < 6.0V$, Figure 1	10			MHz
Maximum Osc. Freq and Ext. Osc. Frequency	f_{osc}	$-20°C < T_A < +85°C$ $4.75 < V^+ < 6.0V$	10			MHz
Minimum Ext. Osc. Freq.	f_{osc}				100	kHz
Oscillator Transconductance	g_m	$V^+ = 4.75V$, $T_A = +85°C$	2000			μmhos
Multiplex Frequency	f_{mux}	$f_{osc} = 10MHz$		500		Hz
Time Between Measurements		$f_{osc} = 10MHz$		200		ms
Input Voltages: Pins 12,27,28						
Input Low Voltage	V_{INL}	$-20°C < T_A < +85°C$			1.0	V
Input High Voltage	V_{INH}		3.5			V
Input Resistance to V^+ Pins 12,24	R_{IN}	$V_{IN} = V^+ - 1.0V$	100	400		kΩ
Input Leakage Pin 27, Pin 28	I_{ILK}				20	μA
Output Current Pin 2	I_{OL}	$V_{OL} = +.4V$	0.36			mA
	I_{OH}	$V_{OH} = V^+ - .8V$	265			μA
Minimum Input Rate of Change	dV_{IN}/dt	Supplies Well Bypassed	25	15		mV/μs
ICM7216C						
Digit Driver: Pins 15,16,17,19,20,21,22,23						
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.0V$	-140	-180		mA
Low Output Current	I_{OL}	$V_{OUT} = 1.0V$		0.3		mA
Segment Driver: Pins 3,4,5,6,8,9,10,11						
Low Output Current	I_{OL}	$V_{OUT} = +1.5V$	20	30		mA
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.5V$		-100		μA
Multiplex Inputs: Pins 1,13,14						
Input Low Voltage	V_{INL}				0.8	V
Input High Voltage	V_{INH}		2.0			V
Input Resistance to GROUND	R_{IN}	$V_{IN} = +1.0V$	50	100		kΩ
ICM7216D						
Digit Driver: Pins 3,4,5,6,8,9,10,11						
Low Output Current	I_{OL}	$V_{OUT} = +1.3V$	50	75		mA
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.5V$		100		μA
Segment Driver: Pins 15,16,17,19,20,21,22,23						
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.0V$	10	15		mA
Leakage Current	I_{SLK}	$V_{OUT} = V^+ - 2.5V$			10	μA
Multiplex Inputs: Pins 1,13,14						
Input Low Voltage	V_{INL}				$V^+ - 2.0$	V
Input High Voltage	V_{INH}		$V^+ - 0.8$			V
Input Resistance to V^+	R_{IN}	$V_{IN} = V^+ - 1.0V$	200	360		kΩ

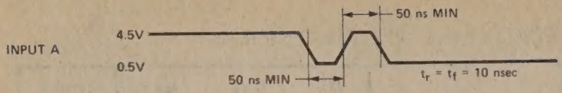

50 ns MIN
4.5V
INPUT A
0.5V
50 ns MIN
$t_r = t_f = 10$ nsec

FIGURE 1. Waveform for Guaranteed Minimum $f_{A(max)}$ Function = Frequency, Frequency Ratio, Unit Counter.

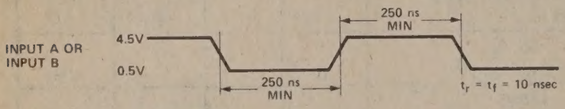

250 ns MIN
4.5V
INPUT A OR INPUT B
0.5V
250 ns MIN
$t_r = t_f = 10$ nsec

FIGURE 2. Waveform for Guaranteed Minimum $f_{B(max)}$ and $f_{A(max)}$ for Function = Period and Time Interval.

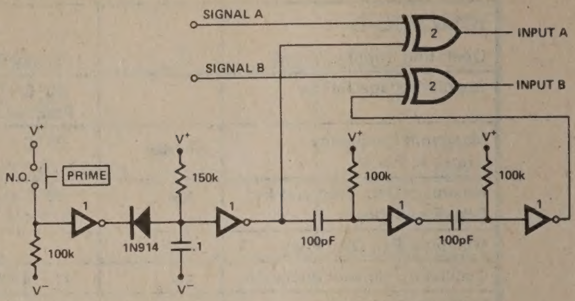
TIME INTERVAL MEASUREMENT

The ICM7216 can be used to accurately measure the time interval between two events. With a 10 MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the time interval mode and measuring a single event, the ICM7216 must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on channel A followed by a negative going edge on channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

This can be easily accomplished with the following circuit: (Figure 3b).


SIGNAL A
SIGNAL B
2
2
INPUT A
INPUT B
V+
N.O.
PRIME
100k
V−
1
1N914
V+
150k
.1
V−
1
100pF
V+
100k
1
100pF
V+
100k
1

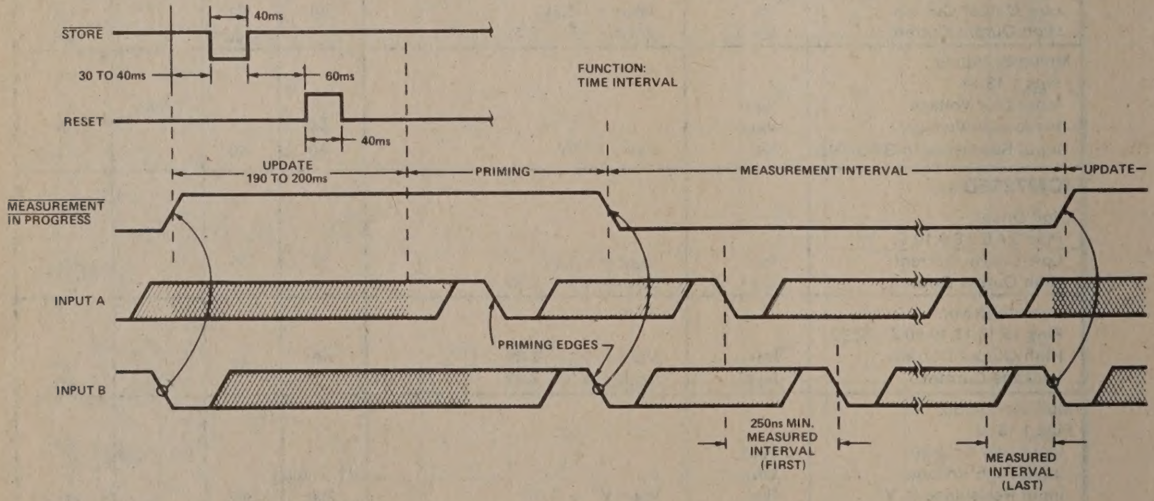
Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

FIGURE 3b. Priming Circuit, Signal A&B High or Low.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

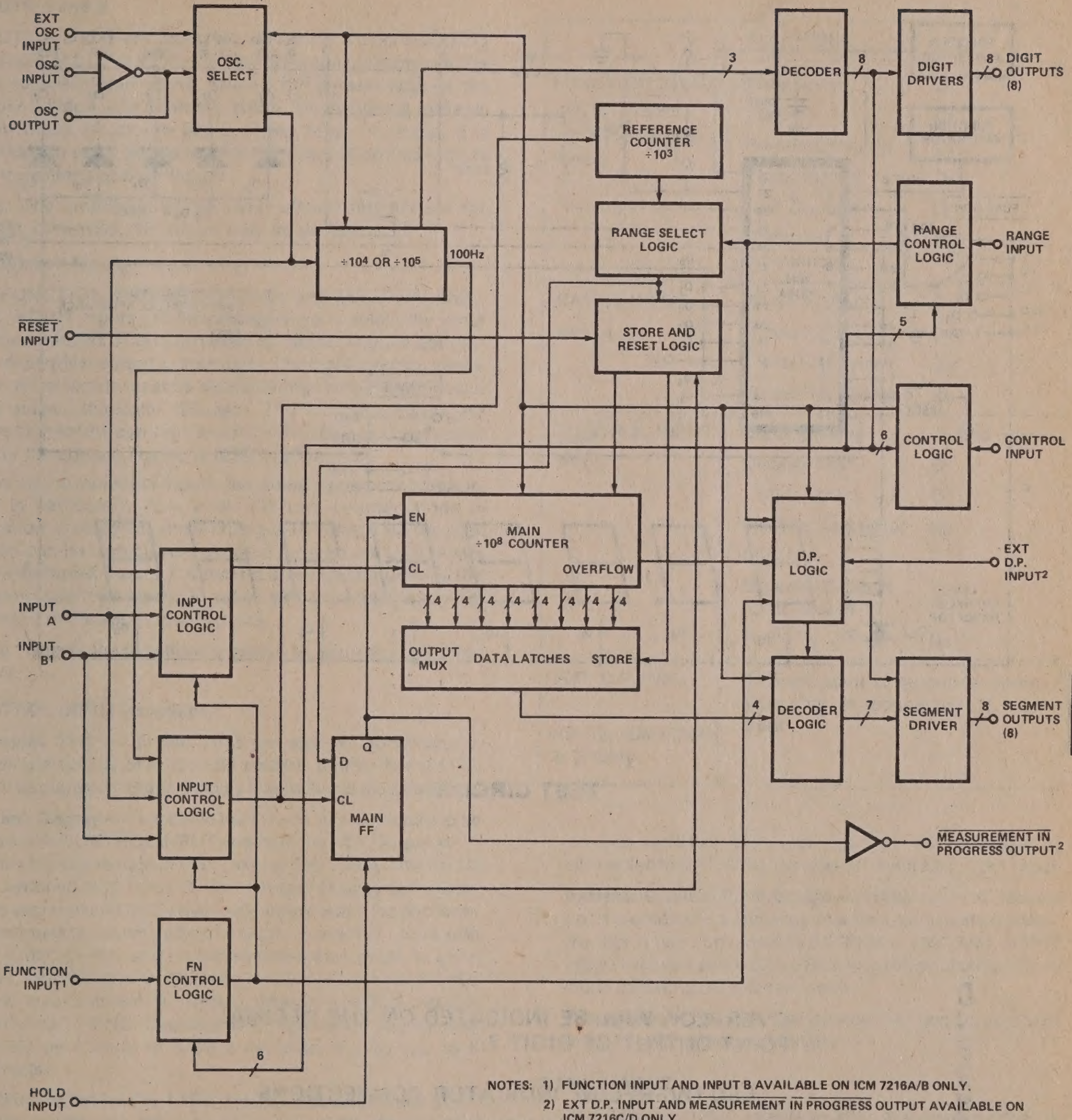
When timing repetitive signals, it is not necessary to "prime" the ICM7216 as the first alternating signal states automatically prime the device. See Figure 3b.

During any time interval measurement cycle, the ICM7216 requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.


40ms
STORE
30 TO 40ms
60ms
FUNCTION: TIME INTERVAL
RESET
40ms
UPDATE 190 TO 200ms
PRIMING
MEASUREMENT INTERVAL
UPDATE
MEASUREMENT IN PROGRESS
INPUT A
PRIMING EDGES
INPUT B
250ns MIN. MEASURED INTERVAL (FIRST)
MEASURED INTERVAL (LAST)

NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

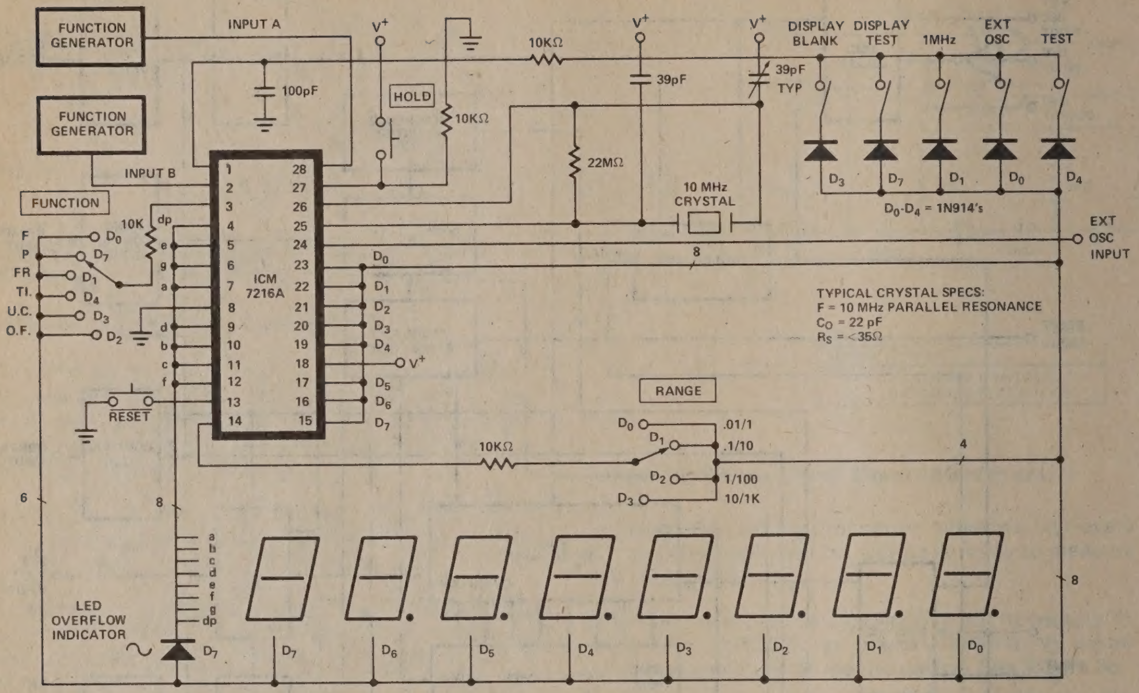
FIGURE 3a. Waveforms for Time Interval Measurement.


EXT OSC INPUT
OSC INPUT
OSC OUTPUT
OSC. SELECT
÷10⁴ OR ÷10⁵
100Hz
RESET INPUT
REFERENCE COUNTER ÷10³
RANGE SELECT LOGIC
STORE AND RESET LOGIC
DECODER
3
8
DIGIT DRIVERS
8
DIGIT OUTPUTS (8)
RANGE CONTROL LOGIC
RANGE INPUT
5
CONTROL LOGIC
6
CONTROL INPUT
MAIN ÷10⁸ COUNTER
EN
CL
OVERFLOW
4
OUTPUT MUX
DATA LATCHES
STORE
D.P. LOGIC
EXT D.P. INPUT²
DECODER LOGIC
4
7
SEGMENT DRIVER
8
SEGMENT OUTPUTS (8)
INPUT A
INPUT B¹
INPUT CONTROL LOGIC
INPUT CONTROL LOGIC
D
Q
CL
MAIN FF
MEASUREMENT IN PROGRESS OUTPUT²
FUNCTION INPUT¹
FN CONTROL LOGIC
6
HOLD INPUT

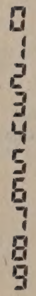
NOTES: 1) FUNCTION INPUT AND INPUT B AVAILABLE ON ICM 7216A/B ONLY.

2) EXT D.P. INPUT AND $\overline{\text{MEASUREMENT IN PROGRESS}}$ OUTPUT AVAILABLE ON ICM 7216C/D ONLY.

BLOCK DIAGRAM


FUNCTION GENERATOR
INPUT A
FUNCTION GENERATOR
INPUT B
FUNCTION
V+
V+
V+
100pF
HOLD
10KΩ
10KΩ
39pF
39pF TYP
22MΩ
10 MHz CRYSTAL
DISPLAY BLANK
DISPLAY TEST
1MHz
EXT OSC
TEST
D3
D7
D1
D0
D4
D0-D4 = 1N914's
EXT OSC INPUT
F
P
FR
TI.
U.C.
O.F.
10K
dp
e
g
a
d
b
c
f
D0
D7
D1
D4
D3
D2
RESET
ICM 7216A
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
D0
D1
D2
D3
D4
V+
D5
D6
D7
8
TYPICAL CRYSTAL SPECS:
F = 10 MHz PARALLEL RESONANCE
C0 = 22 pF
RS = <35Ω
RANGE
D0
D1
D2
D3
.01/1
.1/10
1/100
10/1K
10KΩ
4
6
8
8
a
b
c
d
e
f
g
dp
LED OVERFLOW INDICATOR
D7
D7
D6
D5
D4
D3
D2
D1
D0

TEST CIRCUIT



OUTPUT CODES

OVERFLOW WILL BE INDICATED ON THE DECIMAL POINT OUTPUT OF DIGIT 7.

LED OVERFLOW INDICATOR CONNECTIONS

	CATHODE	ANODE
ICM 7216A	DEC. PT.	D_7
ICM 7216B	D_7	DEC. PT.
ICM 7216C	DEC. PT.	D_7
ICM 7216D	D_7	DEC. PT.

APPLICATION NOTES

GENERAL

INPUTS A and B

INPUTS A and B are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from T^2L logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed Inputs

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μsec). The multiplex inputs are active high for the common anode ICM7216A and C and active low for the common cathode ICM7216B and D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10K resistor should be placed in series with the multiplex inputs as shown in the application circuits.

Table 1 shows the functions selected by each digit for these inputs.

CONTROL INPUT Functions

Display Test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Blank Display is selected at the same time.

Blank Display — To disable the drivers, it is necessary to tie D_3 to the CONTROL INPUT and have the HOLD input at V^+. The chip will remain in this "Display Off" mode until HOLD is switched back to GND. While in the "Display Off" mode, the segment and digit driver outputs are open, the oscillator continues to run with a typical supply current of 1.5mA with a 10 MHz crystal, and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to GND. Segment and Digit Drive outputs may thusly be bussed to drive a common display (up to 6 circuits).

1 MHz Select — The 1 MHz select mode allows use of a 1 MHz crystal with the same digit multiplex rate and time between measurements as with a 10 MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the lease significant digit will be in μsecond increments rather than 0.1 μsec increments.

External Oscillator Enable — In this mode the EXTERNAL OSCILLATOR INPUT is used instead of the on-chip oscillator for Timebase input and Main Counter input in Period and Time interval modes. The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100 KHz or the chip will reset itself to enable the on-chip oscillator. Oscillator input (pin 25) must also be connected to EXT. OSC. input when using EXT. OSC. input.

TABLE 1

	FUNCTION	DIGIT
FUNCTION INPUT Pin 3 (ICM7216A & B Only)	Frequency	D_0
	Period	D_7
	Frequency Ratio	D_1
	Time Interval	D_4
	Unit Counter	D_3
	Oscillator Frequency	D_2
RANGE INPUT Pin 14	.01 sec/1 Cycle	D_0
	.1 sec/10 Cycles	D_1
	1 sec/100 Cycles	D_2
	10 sec/1K Cycles	D_3
CONTROL INPUT Pin 1	Blank Display	D_3 and Hold
	Display Test	D_7
	1 MHz Select	D_1
	External Oscillator Enable	D_0
	External Decimal Point Enable	D_2
	(Test	D_4)
EXT. D.P. INPUT Pin 13, ICM7216C & D Only	Decimal point is output for same digit that is connected to this input	

External Decimal Point Enable — When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to EXTERNAL DECIMAL POINT input is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

Test Mode — This is a special mode for testing purposes only. Contact factory for details.

RANGE INPUT

The RANGE INPUT selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter. In all functional modes except **Unit Counter** a change in the RANGE INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

FUNCTION INPUT

The six functions that can be selected are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio** and **Oscillator Frequency.** This Input is available on the ICM7216A and B only.

These functions select which signal is counted into the Main Counter and which signal is counted by the Reference Counter, as shown in Table 2. In Time Interval, a flip flop is toggled first by a 1-0 transition of Input A and then by a 1-0 transition of Input B. The oscillator is gated into the Main Counter from the time Input A toggles the flip flop until Input B toggles it. A change in the FUNCTION INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed.

TABLE 2

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (f_A)	Input A	100 Hz (Oscillator ÷ 10^5 or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A → B)	Osc•(Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{osc})	Oscillator	100 Hz (Oscillator ÷ 10^5 or 10^4)

EXTernal DECimal Point Input — When the external decimal point is selected this input is active. Any of the digits, except D_7, can be connected to this point. D_7 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point. This input is available on the ICM7216C and D only.

HOLD Input — When the HOLD Input is at V^+, any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. When HOLD is changed to GND a new measurement is initiated.

$\overline{\text{RESET}}$ Input — The $\overline{\text{RESET}}$ Input is the same as an inverted HOLD Input, except the latches for the Main Counter are enabled, resulting in an output of all zeros, and the pin has a pull-up.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500 Hz rate with a digit time of 244 μsec. An interdigit blanking time of 6 μsec is used to prevent ghosting between digits. The decimal point and leading zero blanking assume right hand decimal point displays, and zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the Main Counter overflows. Overflow is indicated by the decimal point on digit 7 turning on.

The ICM7216A and C are designed to drive common anode LED displays at peak current of 25mA/segment, using displays with $V_F = 1.8$ V at 25mA. The average DC current will be over 3mA under these conditions. The ICM7216B and D are designed to drive common cathode displays at peak current of 15mA/segment using displays with $V_F = 1.8$V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 4,5,6 and 7 show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays, V^+ may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

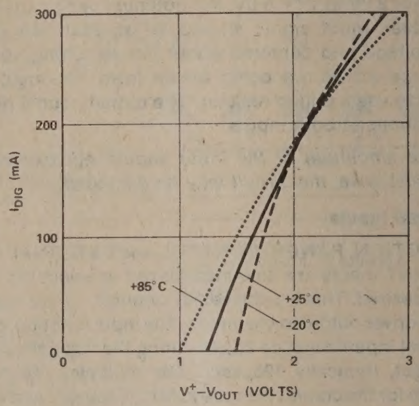
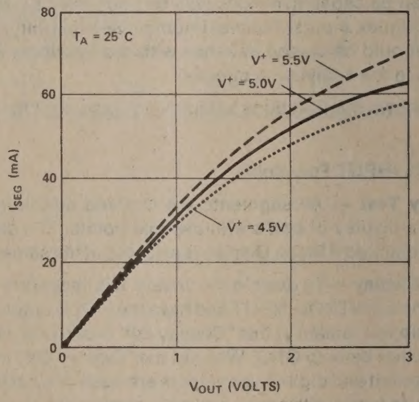


FIGURE 4. ICM7216A & C Typical I_{DIG} vs. $V^+ - V_{OUT}$, $4.5V \le V^+ \le 6.0V$



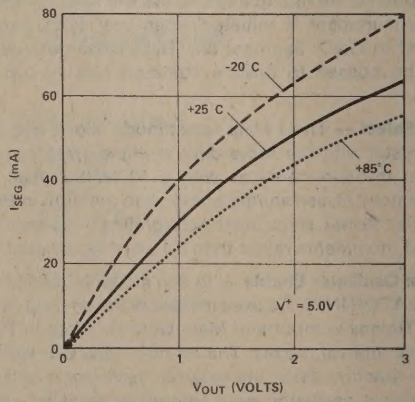


FIGURE 5. ICM7216A & C Typical I_{SEG} vs. V_{OUT}

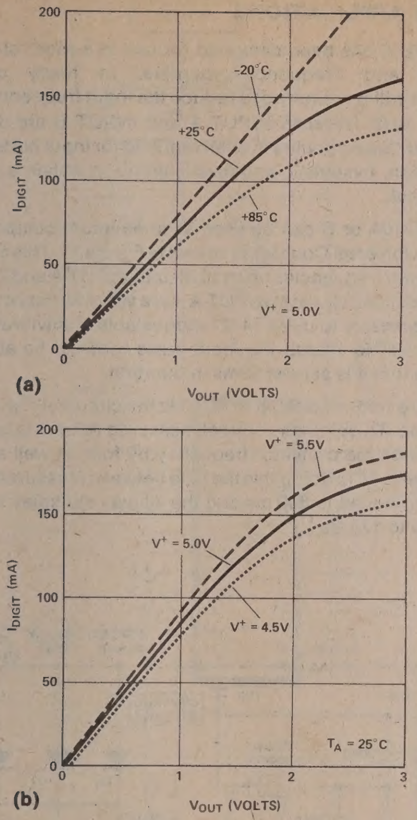


FIGURE 6. ICM7216B & D Typical I_{DIGIT} vs. V_{OUT}

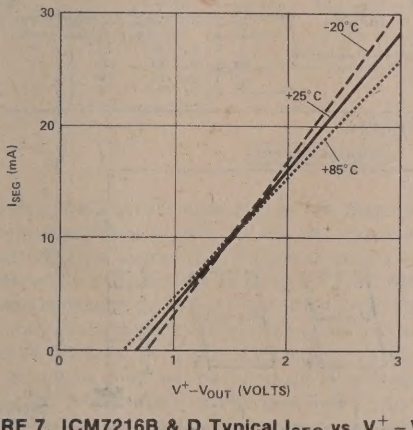
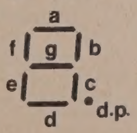


FIGURE 7. ICM7216B & D Typical I_{SEG} vs. $V^+ - V_{OUT}$, $4.5V \leq V^+ - V^- \leq 6.0V$

The segment and digit outputs in ICM7216's are not directly compatible with either TTL or CMOS logic when driving LEDs. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

Segment Identification:



ACCURACY

In a Universal Counter crystal drift and quantization errors cause errors. In Frequency, Period and Time Interval modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the Frequency mode the maximum accuracy is obtained with high frequency inputs and in Period mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 8, the least accuracy will be obtained at 10 KHz. In Time Interval measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 9. In Frequency Ratio measurement can be more accurately obtained by averaging over more cycles of INPUT B as shown in Figure 10.

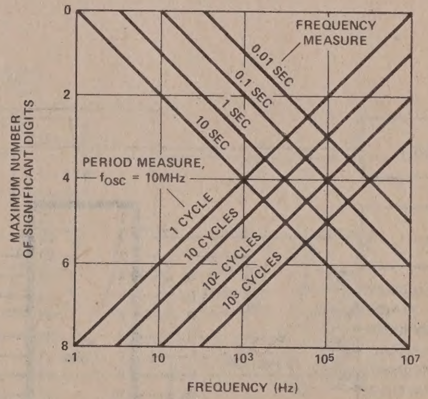


FIGURE 8. Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors

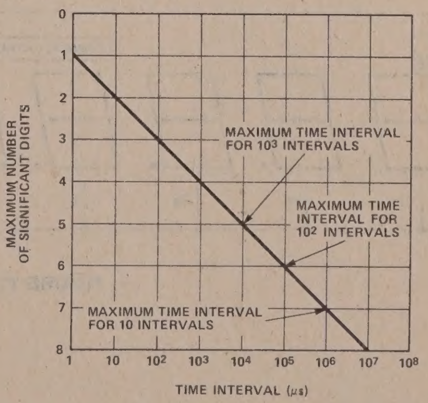


FIGURE 9. Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors

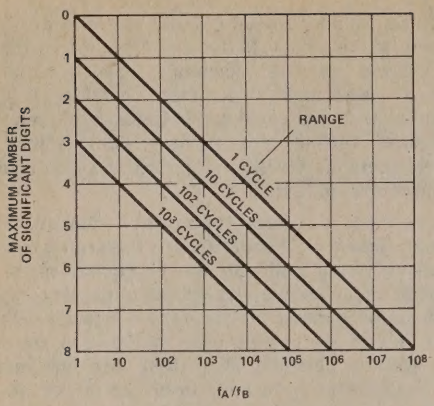


FIGURE 10. Maximum Accuracy for Frequency Ratio Measurement Due to Limitation of Quantization Errors

CIRCUIT APPLICATIONS

The ICM7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, prescalers will be required to reduce the input frequencies to under 10 MHz. Because INPUT A and INPUT B are digital inputs, additional circuitry is often required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal.

The ICM7216A or B can be used as a minimum component complete Universal Counter as shown in Figure 11. This circuit can use input frequencies up to 10 MHz at INPUT A and 2 MHz at INPUT B. If the signal at INPUT A has a very low duty cycle it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse width to be able to guarantee that it is at least 50ms in duration.

To measure frequencies up to 40 MHz the circuit of Figure 12 can be used. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well as the input frequency. In doing this the time between measurements is also lengthened to 800 ms and the display multiplex rate is decreased to 125 Hz.

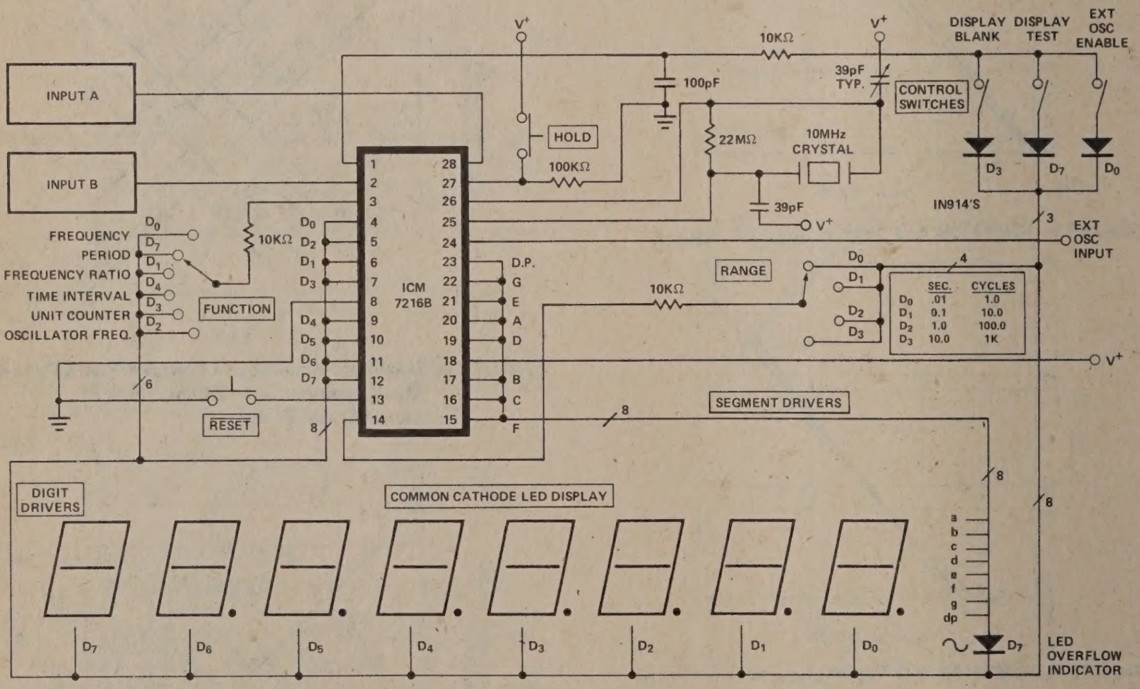

INPUT A
INPUT B
V+
HOLD
100KΩ
100pF
10KΩ
V+
39pF TYP.
22MΩ
10MHz CRYSTAL
39pF
V+
CONTROL SWITCHES
DISPLAY BLANK
DISPLAY TEST
EXT OSC ENABLE
D3
D7
D0
IN914'S
3
EXT OSC INPUT
4
FREQUENCY
PERIOD
FREQUENCY RATIO
TIME INTERVAL
UNIT COUNTER
OSCILLATOR FREQ.
D0
D7
D1
D4
D3
D2
10KΩ
FUNCTION
D0
D2
D1
D3
D4
D5
D6
D7
ICM 7216B
1 2 3 4 5 6 7 8 9 10 11 12 13 14
28 27 26 25 24 23 22 21 20 19 18 17 16 15
D.P.
G
E
A
D
B
C
F
RANGE
10KΩ
D0
D1
D2
D3
SEC. CYCLES
D0 .01 1.0
D1 0.1 10.0
D2 1.0 100.0
D3 10.0 1K
V+
6
RESET
8
SEGMENT DRIVERS
8
8
8
DIGIT DRIVERS
COMMON CATHODE LED DISPLAY
a
b
c
d
e
f
g
dp
D7
D6
D5
D4
D3
D2
D1
D0
D7
LED OVERFLOW INDICATOR

FIGURE 11. 10MHz Universal Counter

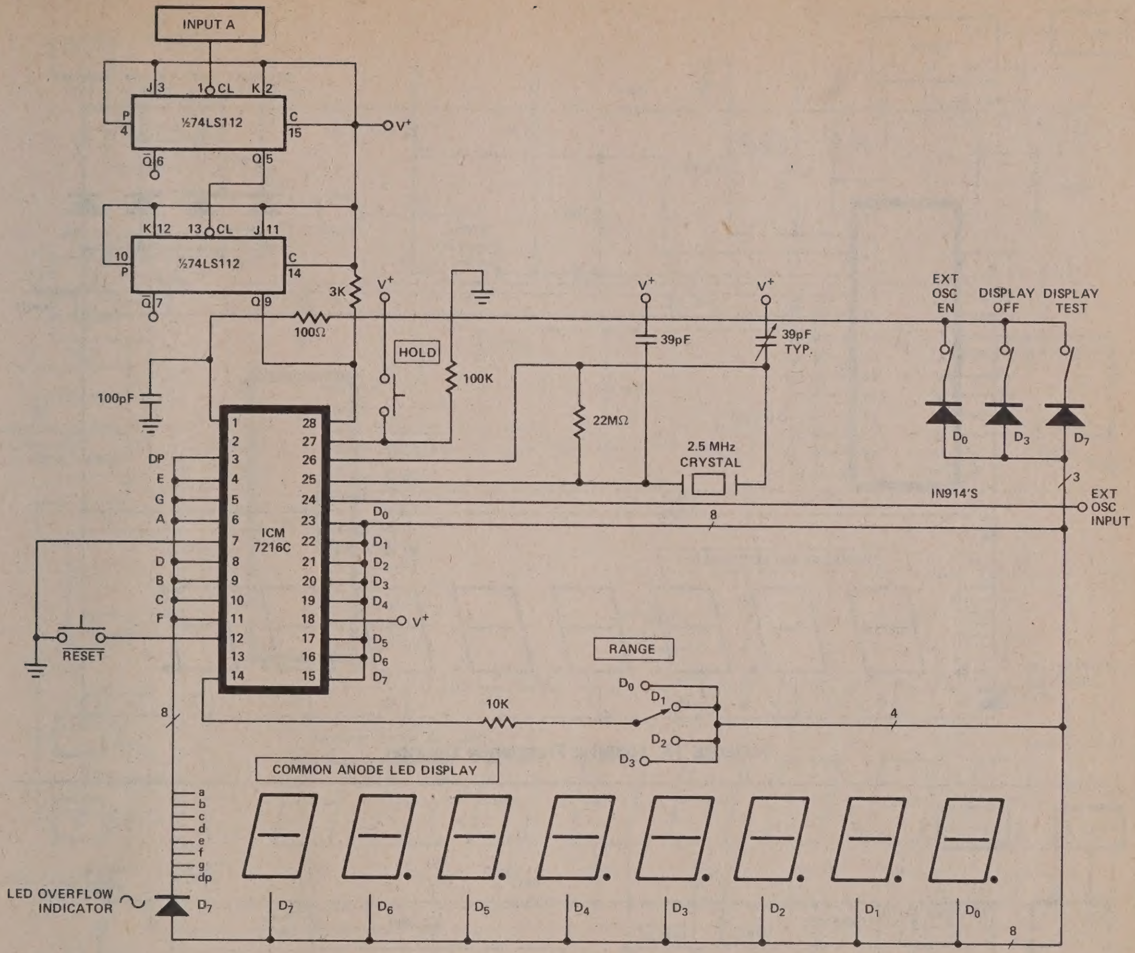

INPUT A
½74LS112
½74LS112
3K
100Ω
100pF
HOLD
100K
39pF
39pF TYP.
22MΩ
2.5 MHz CRYSTAL
EXT OSC EN
DISPLAY OFF
DISPLAY TEST
IN914'S
EXT OSC INPUT
ICM 7216C
RESET
RANGE
10K
COMMON ANODE LED DISPLAY
LED OVERFLOW INDICATOR
V+

FIGURE 12. 40MHz Frequency Counter

If the input frequency is prescaled by ten, then the oscillator can remain at 10 or 1 MHz, but the decimal point must be moved one digit to the right. Figure 13 shows a frequency counter with a ÷10 prescaler and an ICM7216C. Since there is no external decimal point with the ICM7216A or B, the decimal point may be controlled with additional drivers as shown in Figure 14. Alternatively, if separate anodes are available for the decimal points, they can be wired up to the adjacent digit anodes. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 15 additional logic has been added to count the input directly in period mode for maximum accuracy. In Figures 13 through 15, INPUT A comes from Q_C of the prescaler rather than Q_D to obtain an input duty cycle of 40%.

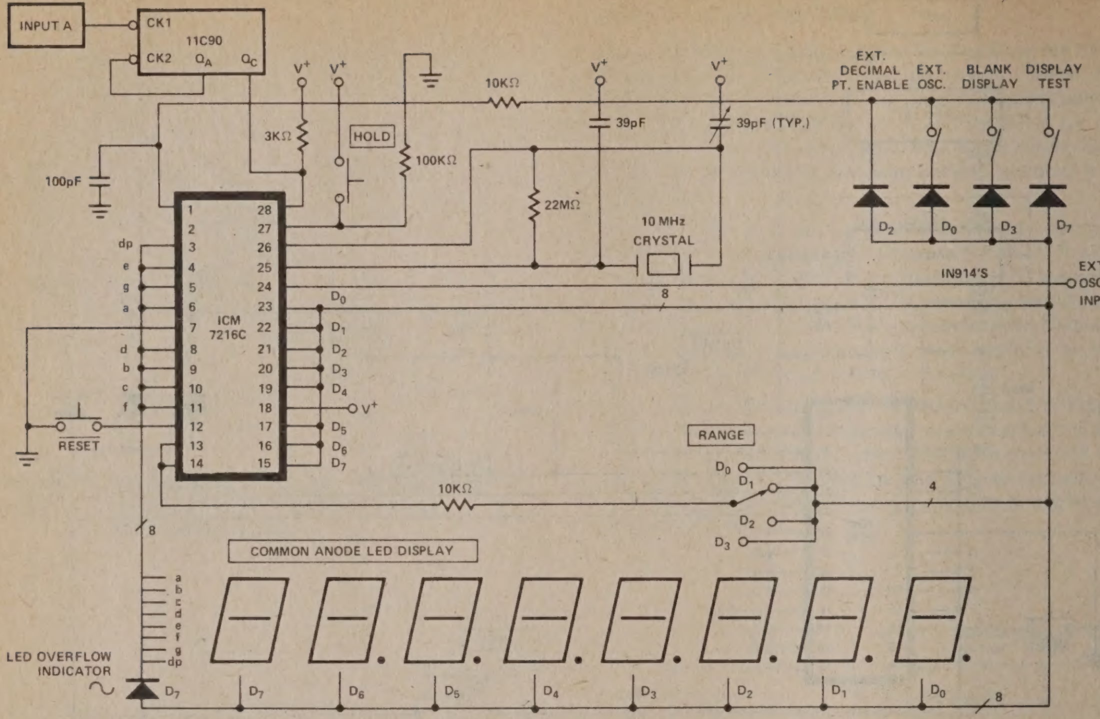

INPUT A
CK1
11C90
CK2
QA
QC
V+
3KΩ
HOLD
100KΩ
10KΩ
39pF
39pF (TYP.)
100pF
22MΩ
10 MHz
CRYSTAL
EXT. DECIMAL PT. ENABLE
EXT. OSC.
BLANK DISPLAY
DISPLAY TEST
D2
D0
D3
D7
IN914'S
EXT OSC INPUT
8
ICM 7216C
dp
e
g
a
d
b
c
f
RESET
D1
D4
D5
D6
RANGE
4
COMMON ANODE LED DISPLAY
LED OVERFLOW INDICATOR

FIGURE 13. 100MHz Frequency Counter

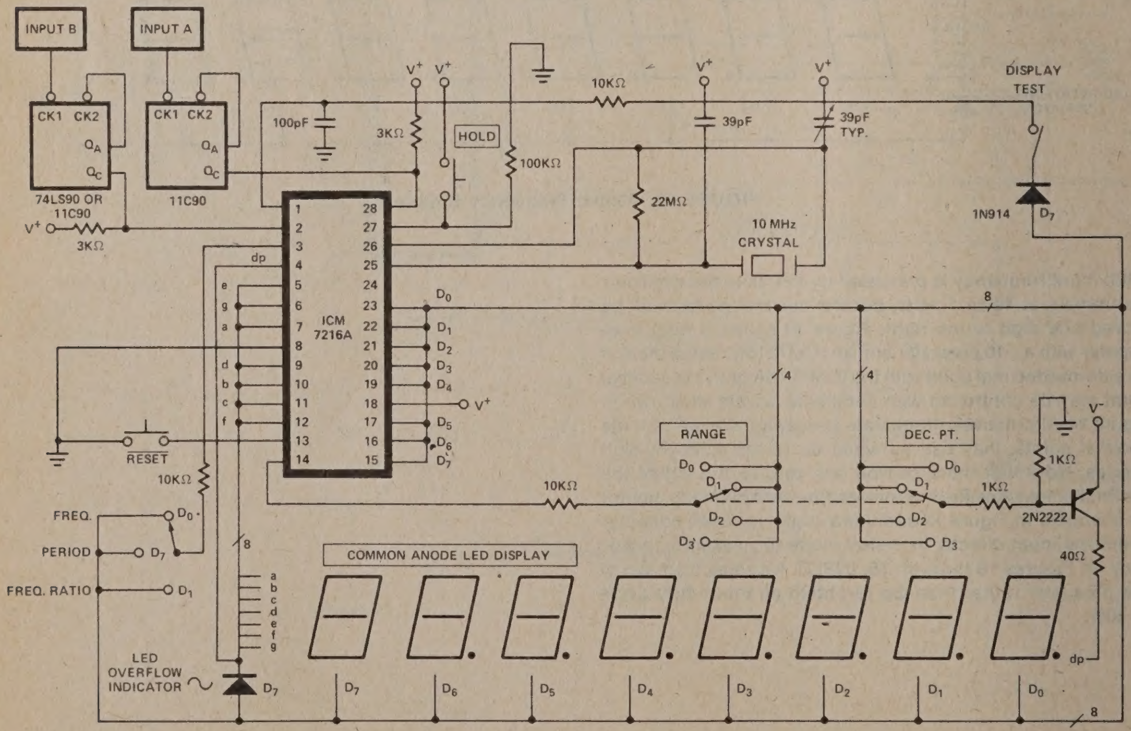
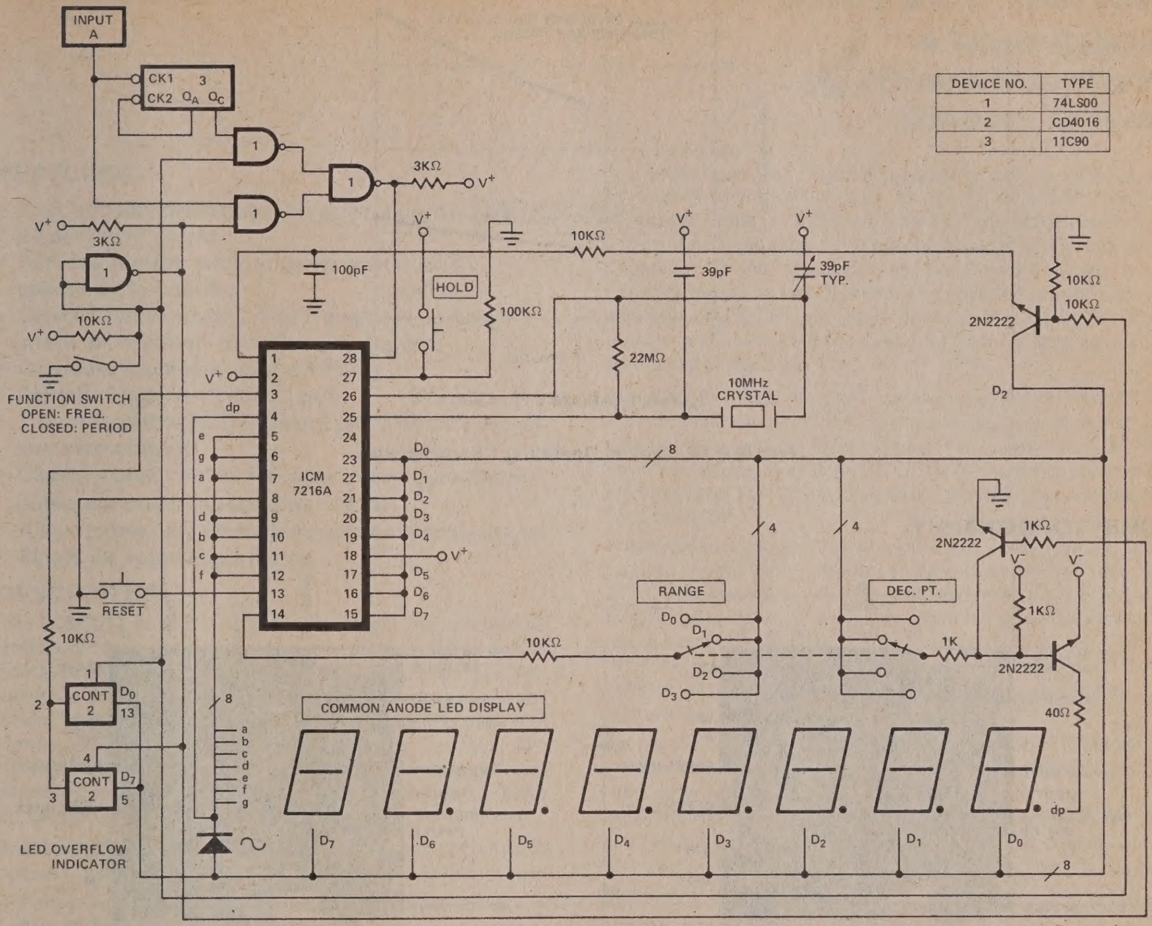

INPUT B
INPUT A
CK1 CK2
QA
QC
74LS90 OR 11C90
11C90
V+
3KΩ
100pF
HOLD
100KΩ
10KΩ
39pF
39pF TYP.
22MΩ
10 MHz
CRYSTAL
DISPLAY TEST
1N914
D7
ICM 7216A
dp
e
g
a
d
b
c
f
D0
D1
D2
D3
D4
D5
D6
RESET
10KΩ
FREQ.
PERIOD
FREQ. RATIO
RANGE
DEC. PT.
4
8
V-
1KΩ
2N2222
40Ω
COMMON ANODE LED DISPLAY
LED OVERFLOW INDICATOR

FIGURE 14. 100MHz Multifunction Counter


INPUT A
CK1 3
CK2 QA QC
1
3KΩ
V+
100pF
HOLD
100KΩ
10KΩ
39pF
39pF TYP.
22MΩ
10MHz CRYSTAL
2N2222
10KΩ
D2
FUNCTION SWITCH
OPEN: FREQ.
CLOSED: PERIOD
dp
e g a d b c f
ICM 7216A
D0 D1 D2 D3 D4 D5 D6 D7
RESET
8
4
RANGE
DEC. PT.
1KΩ
1K
V-
40Ω
CONT 2
LED OVERFLOW INDICATOR
COMMON ANODE LED DISPLAY
a b c d e f g

DEVICE NO.	TYPE
1	74LS00
2	CD4016
3	11C90

FIGURE 15. 100MHz Frequency, 2MHz Period Counter

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ to 22MΩ should be connected between the OSCillator INPUT and OUTPUT to provide biasing. The oscillator is designed to work with a parallel resonant 10 MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{in} C_{out} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

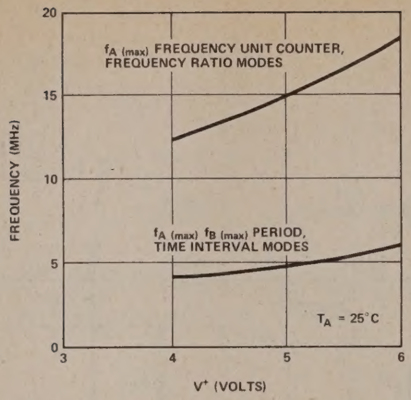
$$\text{where } C_L = \left(\frac{C_{in}C_{out}}{C_{in}+C_{out}}\right)$$

C_O = Crystal Static Capacitance
R_S = Crystal Series Resistance
C_{in} = Input Capacitance
C_{out} = Output Capacitance
$\omega = 2\pi f$

The required g_m should exceed the g_m specified for the ICM7216 by at least 50% to insure reliable startup. The OSCillator INPUT and OUTPUT pins each contribute about 5pF to C_{in} and C_{out}. For maximum stability of frequency, C_{in} and C_{out} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10 MHz or 1 MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is $f_{max} = \frac{f_{osc}}{2\times10^4}$ for 10 MHz mode and $f_{max} = \frac{f_{osc}}{2\times10^3}$ for the 1 MHz mode. The time between measurements is $\frac{2\times10^6}{f_{osc}}$ in the 10 MHz mode and $\frac{2\times10^5}{f_{osc}}$ in the 1 MHz mode.

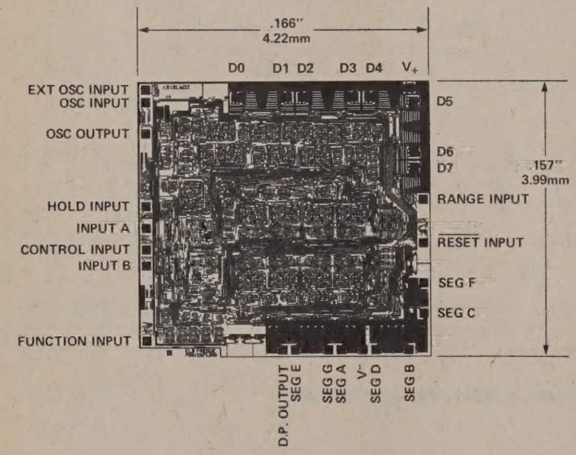
The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or INPUT can cause undesirable shifts in oscillator frequency.



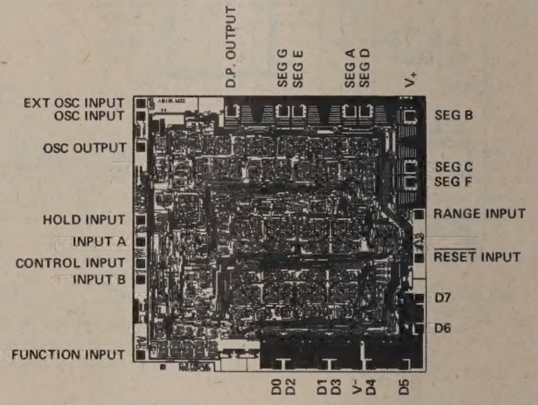
$f_{A(max)}$, $f_{B(max)}$ as a Function of V^+

FIGURE 16. Typical Operating Characteristics

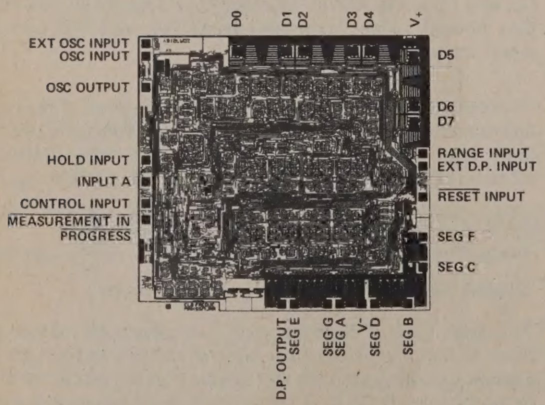
CHIP TOPOGRAPHY


.166"
4.22mm
.157"
3.99mm
D0
D1 D2
D3 D4
V+
EXT OSC INPUT
OSC INPUT
OSC OUTPUT
HOLD INPUT
INPUT A
CONTROL INPUT
INPUT B
FUNCTION INPUT
D5
D6
D7
RANGE INPUT
RESET INPUT
SEG F
SEG C
D.P. OUTPUT
SEG E
SEG G
SEG A
V-
SEG D
SEG B

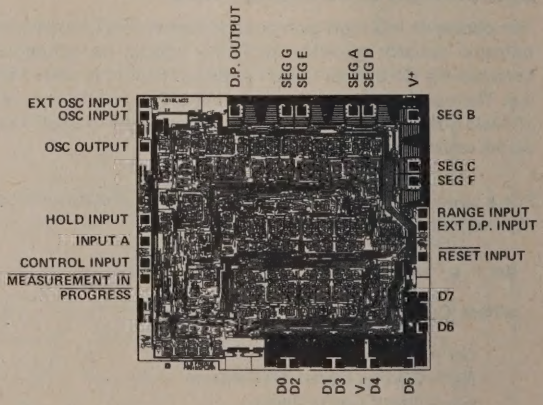
ICM7216A


D.P. OUTPUT
SEG G
SEG E
SEG A
SEG D
V+
EXT OSC INPUT
OSC INPUT
OSC OUTPUT
HOLD INPUT
INPUT A
CONTROL INPUT
INPUT B
FUNCTION INPUT
SEG B
SEG C
SEG F
RANGE INPUT
RESET INPUT
D7
D6
D0
D2
D1
D3
V-
D4
D5

ICM7216B


D0
D1
D2
D3
D4
V+
EXT OSC INPUT
OSC INPUT
OSC OUTPUT
HOLD INPUT
INPUT A
CONTROL INPUT
MEASUREMENT IN PROGRESS
D5
D6
D7
RANGE INPUT
EXT D.P. INPUT
RESET INPUT
SEG F
SEG C
D.P. OUTPUT
SEG E
SEG G
SEG A
V-
SEG D
SEG B

ICM7216C


D.P. OUTPUT
SEG G
SEG E
SEG A
SEG D
V+
EXT OSC INPUT
OSC INPUT
OSC OUTPUT
HOLD INPUT
INPUT A
CONTROL INPUT
MEASUREMENT IN PROGRESS
SEG B
SEG C
SEG F
RANGE INPUT
EXT D.P. INPUT
RESET INPUT
D7
D6
D0
D2
D1
D3
V-
D4
D5

ICM7216D

INTERSIL

ICM7217 Series
ICM7227 Series
4 Digit CMOS Up/Down Counter/ Display Driver

FEATURES

- **Four decade, presettable up-down counter with parallel zero detect**
- **Settable register with contents continuously compared to counter**
- **Directly drives multiplexed 7 segment common anode or common cathode LED displays**
- **On-board multiplex scan oscillator**
- **Schmitt trigger on count input**
- **TTL compatible BCD I/O port, carry/borrow, equal, and zero outputs**
- **Display blank control for lower power operation; quiescent power dissipation < 5mW**
- **All terminals fully protected against static discharge**
- **Single 5V supply operation**

DESCRIPTION

The ICM7217 and ICM7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The ICM7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The ICM7227 versions are for use in processor-based systems, where presetting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to .8" character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeroes can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

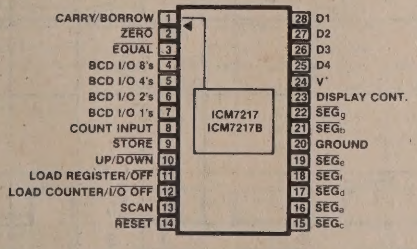
The ICM7217/7227 (common anode) and ICM7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B, 7227B (common anode) and ICM7217C/7227C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

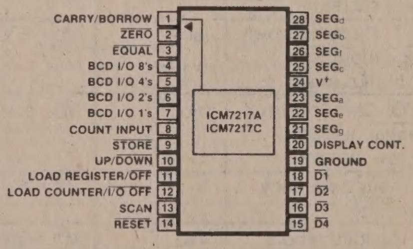
These circuits provide 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a $\overline{\text{ZERO}}$ output, which indicates when the count is zero, and an $\overline{\text{EQUAL}}$ output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a tri-state BCD I/O port. The CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$ outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2 MHz, although the device will typically run with f_{in} as high as 5 MHz. Counting and comparing (EQUAL output) will typically run 750 kHz maximum.

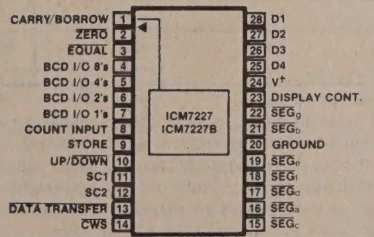
PIN CONFIGURATIONS (OUTLINE DRAWINGS JI, PI)

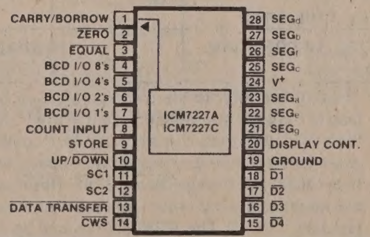

CARRY/BORROW 1
ZERO 2
EQUAL 3
BCD I/O 8's 4
BCD I/O 4's 5
BCD I/O 2's 6
BCD I/O 1's 7
COUNT INPUT 8
STORE 9
UP/DOWN 10
LOAD REGISTER/OFF 11
LOAD COUNTER/I/O OFF 12
SCAN 13
RESET 14
ICM7217
ICM7217B
28 D1
27 D2
26 D3
25 D4
24 V+
23 DISPLAY CONT.
22 SEGg
21 SEGb
20 GROUND
19 SEGe
18 SEGf
17 SEGd
16 SEGa
15 SEGc


CARRY/BORROW 1
ZERO 2
EQUAL 3
BCD I/O 8's 4
BCD I/O 4's 5
BCD I/O 2's 6
BCD I/O 1's 7
COUNT INPUT 8
STORE 9
UP/DOWN 10
LOAD REGISTER/OFF 11
LOAD COUNTER/I/O OFF 12
SCAN 13
RESET 14
ICM7217A
ICM7217C
28 SEGd
27 SEGb
26 SEGf
25 SEGc
24 V+
23 SEGa
22 SEGe
21 SEGg
20 DISPLAY CONT.
19 GROUND
18 D1
17 D2
16 D3
15 D4

COMMON ANODE

COMMON CATHODE


CARRY/BORROW 1
ZERO 2
EQUAL 3
BCD I/O 8's 4
BCD I/O 4's 5
BCD I/O 2's 6
BCD I/O 1's 7
COUNT INPUT 8
STORE 9
UP/DOWN 10
SC1 11
SC2 12
DATA TRANSFER 13
CWS 14
ICM7227
ICM7227B
28 D1
27 D2
26 D3
25 D4
24 V+
23 DISPLAY CONT.
22 SEGg
21 SEGb
20 GROUND
19 SEGe
18 SEGf
17 SEGd
16 SEGa
15 SEGc


CARRY/BORROW 1
ZERO 2
EQUAL 3
BCD I/O 8's 4
BCD I/O 4's 5
BCD I/O 2's 6
BCD I/O 1's 7
COUNT INPUT 8
STORE 9
UP/DOWN 10
SC1 11
SC2 12
DATA TRANSFER 13
CWS 14
ICM7227A
ICM7227C
28 SEGd
27 SEGb
26 SEGf
25 SEGc
24 V+
23 SEGa
22 SEGe
21 SEGg
20 DISPLAY CONT.
19 GROUND
18 D1
17 D2
16 D3
15 D4

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (common anode/Cerdip) .... 1 W } Note 1
Power Dissipation (common cathode/Plastic) .... 0.5 W } Note 1
Supply Voltage V^+-V^- 6V
Input voltage (any terminal) .... V^+ +0.3V, Ground −0.3V - Note 2
Operating temperature range .... -20°C to +85°C
Storage temperature range .... −55°C to +125°C

Absolute maximum ratings define stress limitations which if exceeded may permanently damage the device. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

OPERATING CHARACTERISTICS

$V^+ = 5V \pm 10\%$, $T_A = 25°C$, Test Circuit, Display Diode Drop 1.7V, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply current (Lowest power mode)	I^{+}_{MIN}, (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V^+ (Note 3)		350	500	μA
Supply current (Lowest power mode)	I^{+}_{MIN}, (7227)	Display off (Note 3)		300	500	μA
Supply current OPERATING	I^{+}_{OP}	Common Anode, Display On, all "8's"	175	200		mA
		Common Cathode, Display On, all "8's"	85	100		mA
Supply Voltage	V^+		4.5	5	5.5	V
Digit Driver output current	I_{DIG}	Common anode, $V_{OUT} = V^+ -2.2V$	175	200		mA peak
Segment driver output current	I_{SEG}	Common anode, $V_{OUT} = +1.3V$	−25	−40		mA peak
Digit Driver output current	I_{DIG}	Common cathode, $V_{OUT} = +1.3V$	−75	−100		mA peak
Segment Driver output current	I_{SEG}	Common cathode $V_{OUT} = V^+ -2V$	10	12.5		mA peak
$\overline{ST}$, $\overline{RS}$, UP/DN input pullup current	I_P	$V_{OUT} = V^+ -2V$ (See Note 3)	5	25		μA
3 level input impedance	Z_{IN}			100		kΩ
BCD I/O input high voltage	V_{BIH}	ICM7217 common anode (Note 4)	1.3			V
		ICM7217 common cathode (Note 4)	4.1			V
		ICM7227 with 50pF effective load	3			V
BCD I/O input low voltage	V_{BIL}	ICM7217 common anode (Note 4)			0.8	V
		ICM7217 common cathode (Note 4)			3.7	V
		ICM7227 with 50pF effective load			1.5	V
BCD I/O input pullup current	I_{BPU}	ICM7217 common anode $V_{IN} = V^+ -2V$ (Note 3)	5	25		μA
BCD I/O input pulldown current	I_{BPD}	ICM7217 common cathode $V_{IN} = +1.3V$ (Note 3)	5	25		μA
BCD I/O, Carry/borrow zero, equal outputs output high current	I_{BOH}	$V_{OH} = V^+ -1.5V$	100			μA
BCD I/O, Carry/borrow zero, equal outputs output low current	I_{BOL}	$V_{OL} = +0.4V$	−2			mA
Count input frequency (Guaranteed)	f_{in}	$V^+ = 5V \pm 10\%$, $-20°C < T_A < +70°C$	0	5	2	MHz
Count input threshold	V_{TC}	$V^+ = 5V$		2		V
Count input hysteresis	V_{HC}	$V^+ \doteq 5V$		0.5		V
Display scan oscillator frequency	f_{ds}	Free-running (SCAN terminal open circuit)		10		KHz
Operating Temperature Range	T_A	Industrial temperature range	−20		85	°C

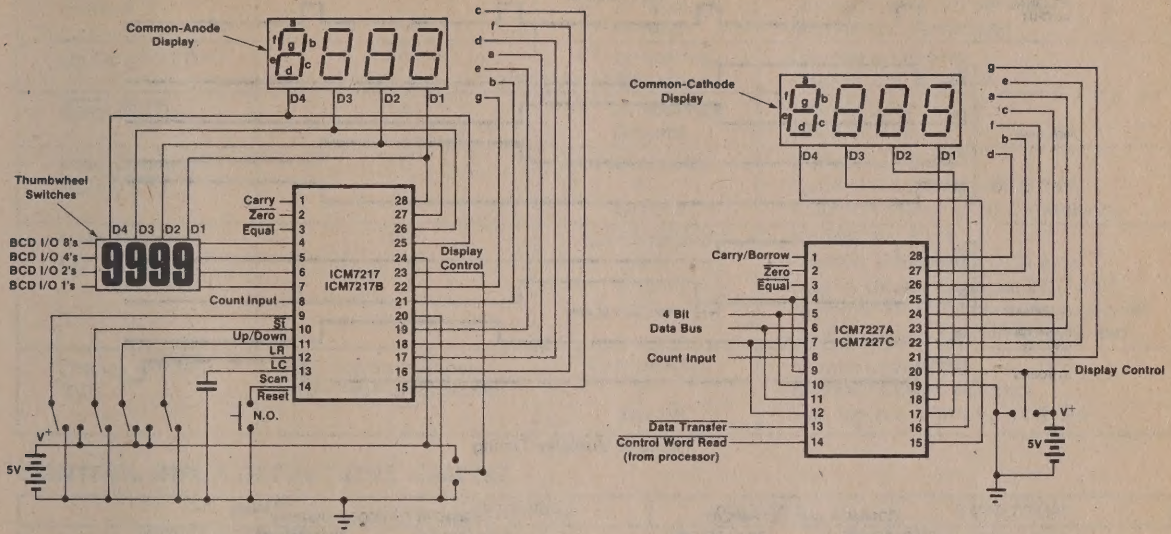
NOTE 1 These limits refer to the package and will not be obtained during normal operation.

NOTE 2 Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than V^- may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned on first.

NOTE 3 In the ICM7217 the Up/Down, Store, Reset and the BCD I/O as inputs have pullup devices which consume power when connected to the negative supply. When all these terminals are connected to the negative supply, with the display off, the device will consume typically 750 μA. The ICM7227 devices do not have these pullups and thus are not subject to this condition.

NOTE 4 These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as a logic zero for ICM7217 common-cathode versions only.

TEST CIRCUITS


Common-Anode Display
a
f
g
b
e
c
d
D4
D3
D2
D1
c
f
d
a
e
b
g
Thumbwheel Switches
D4
D3
D2
D1
BCD I/O 8's
BCD I/O 4's
BCD I/O 2's
BCD I/O 1's
9999
Carry
Zero
Equal
Count Input
ST
Up/Down
LR
LC
Scan
Reset
N.O.
ICM7217
ICM7217B
Display Control
V+
5V
Common-Cathode Display
g
e
a
c
f
b
d
Carry/Borrow
Zero
Equal
4 Bit Data Bus
Count Input
Data Transfer
Control Word Read (from processor)
ICM7227A
ICM7227C
Display Control
V+
5V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
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21
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17
16
15

Figure 1

Figure 1 shows the ICM7217 in the common-anode version and the ICM7227 in the common-cathode version.

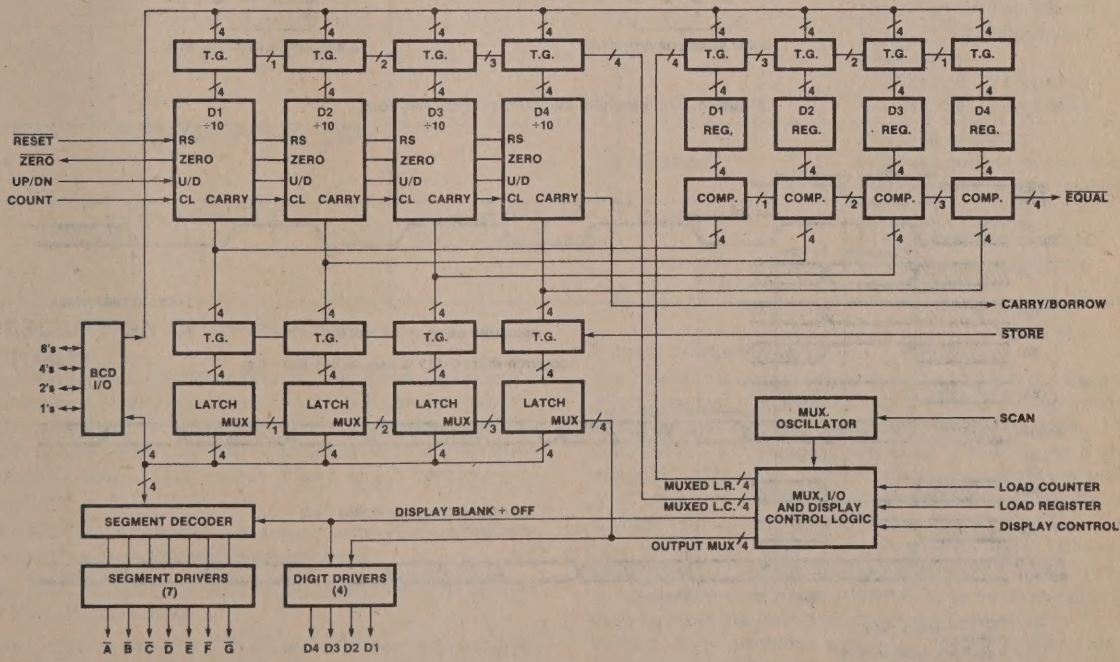

T.G.
D1 ÷10
D2 ÷10
D3 ÷10
D4 ÷10
RS
ZERO
U/D
CL
CARRY
RESET
ZERO
UP/DN
COUNT
D1 REG.
D2 REG.
D3 REG.
D4 REG.
COMP.
EQUAL
CARRY/BORROW
STORE
LATCH
MUX
BCD I/O
8's
4's
2's
1's
MUX. OSCILLATOR
SCAN
MUX, I/O AND DISPLAY CONTROL LOGIC
MUXED L.R.
MUXED L.C.
OUTPUT MUX
LOAD COUNTER
LOAD REGISTER
DISPLAY CONTROL
DISPLAY BLANK + OFF
SEGMENT DECODER
SEGMENT DRIVERS (7)
DIGIT DRIVERS (4)
A B C D E F G
D4 D3 D2 D1
4
1
2
3

Figure 2: ICM7217 Functional Block Diagram

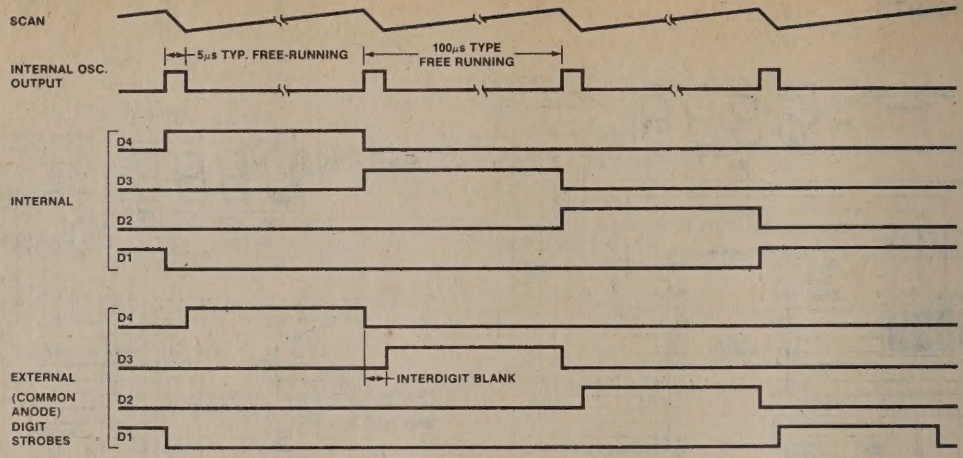

SCAN
5μs TYP. FREE-RUNNING
100μs TYPE FREE RUNNING
INTERNAL OSC. OUTPUT
INTERNAL
D4
D3
D2
D1
EXTERNAL (COMMON ANODE) DIGIT STROBES
D4
D3
INTERDIGIT BLANK
D2
D1

Figure 3: Multiplex Timing

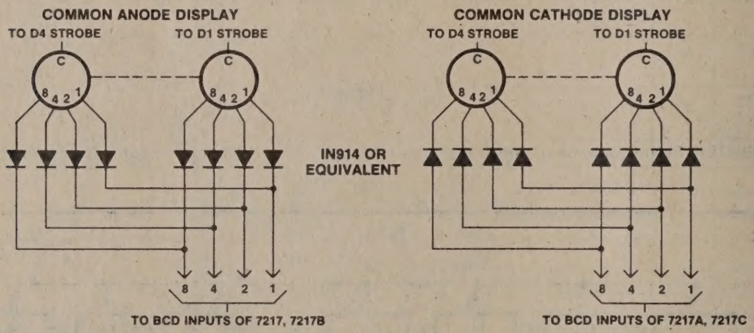

COMMON ANODE DISPLAY
TO D4 STROBE
TO D1 STROBE
C
8 4 2 1
C
8 4 2 1
IN914 OR EQUIVALENT
8 4 2 1
TO BCD INPUTS OF 7217, 7217B
COMMON CATHODE DISPLAY
TO D4 STROBE
TO D1 STROBE
C
8 4 2 1
C
8 4 2 1
8 4 2 1
TO BCD INPUTS OF 7217A, 7217C

Figure 4: Thumbwheel switch/diode connections

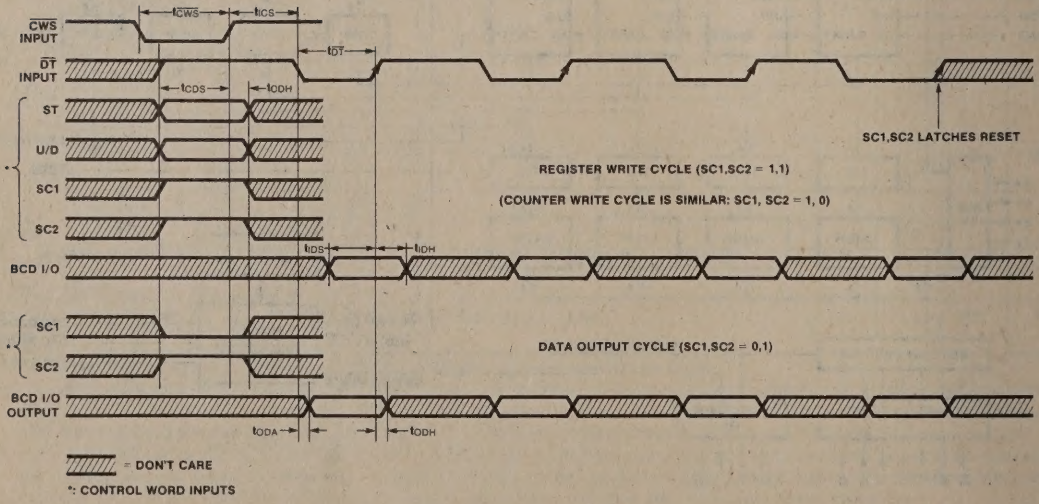

CWS INPUT
tCWS
tICS
DT INPUT
tDT
tCDS
tCDH
ST
U/D
SC1
SC2
SC1,SC2 LATCHES RESET
REGISTER WRITE CYCLE (SC1,SC2 = 1,1)
(COUNTER WRITE CYCLE IS SIMILAR: SC1, SC2 = 1, 0)
tIDS
tIDH
BCD I/O
SC1
SC2
DATA OUTPUT CYCLE (SC1,SC2 = 0,1)
BCD I/O OUTPUT
tODA
tODH
= DON'T CARE
*: CONTROL WORD INPUTS

Figure 5: ICM7227 I/O Timing (See Table 2)

CONTROL INPUT DEFINITIONS ICM7217

INPUT	TERMINAL	VOLTAGE	FUNCTION
Store ($\overline{\mathrm{ST}}$)	9	V^+ (or floating) Ground	Output latches not updated Output latches updated
Up/Down (U/$\overline{\mathrm{D}}$)	10	V^+ (or floating) Ground	Counter counts up Counter counts down
$\overline{\mathrm{Reset}}$ ($\overline{\mathrm{RST}}$)	14	V^+ (or floating) Ground	Normal Operation Counter Reset
Load Counter LC/$\overline{\mathrm{I/O\ OFF}}$	12	Unconnected V^+ Ground	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
Load Register LR/$\overline{\mathrm{OFF}}$	11	Unconnected V^+ Ground	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D4; mpx oscillator inhibited
Display Control (DC)	23 Common Anode 20 Common Cathode	Unconnected V^+ Ground	Normal operation Segment drivers disabled Leading zero blanking inhibited

CONTROL INPUT DEFINITIONS ICM7227

INPUT		TERMINAL	VOLTAGE	FUNCTION
	$\overline{\mathrm{Data\ Transfer}}$ ($\overline{\mathrm{DT}}$)	13	V^+ Ground	Normal Operation Causes transfer of data as directed by select code
Control Word Port	Store (ST)	9	V^+ (During $\overline{\mathrm{CWS}}$ Pulse) Ground	Output latches updated Output latches not updated
"	Up/$\overline{\mathrm{Down}}$ (U/$\overline{\mathrm{D}}$)	10	V^+ (During $\overline{\mathrm{CWS}}$ Pulse) Ground	Counter counts up Counter counts down
" "	Select Code Bit 1 (SC1) Select Code Bit 2 (SC2)	11 12	$V^+ = 1$ Ground	SC1, SC2 00 Change store and up/down latches. No data transfer. 01 Output latch data active 10 Counter to be preset 11 Register to be preset
	$\overline{\mathrm{Control\ Word\ Strobe}}$ ($\overline{\mathrm{CWS}}$)	14	V^+ Ground	Normal operation Causes control word to be written into control latches
	Display Control (DC)	23 Common Anode 20 Common Cathode	Unconnected V^+ Ground	Normal operation Display drivers disabled Leading zero blanking inhibited

DESCRIPTION OF OPERATION

OUTPUTS

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

The $\overline{\mathrm{EQUAL}}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{\mathrm{ZERO}}$ output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{\mathrm{EQUAL}}$ and $\overline{\mathrm{ZERO}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 2mA @ 0.4V (on resistance 200 ohms), and for a logic one, the outputs source >60μA.

The digit and segment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/seg. This corresponds to average currents of 10mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately 1/2 (V^+); this corresponds to normal operation. When this pin is connected to V^+, the segments are inhibited, and when connected to V^-, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch; see fig. 1.

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; in the ICM7227 versions, input/output control and timing must be provided externally. When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines.

The onboard multiplex scan oscillator has a nominal free-running frequency of 10kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply, or the oscillator may be directly overdriven to about 20kHz. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times (for ICM7217 versions) are shown in Table 1 below.

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Fig. 3 for the display digit multiplex timing.

Table 1

Scan Capacitor	Nominal Oscillator Frequency	Digit Repetition Date	Scan Cycle Time
None	10kHz	2.5kHz	400μs
20pF	5kHz	1.2kHz	800μs
90pF	1kHz	250Hz	4ms

CONTROL OF ICM7217

The counter is incremented by the rising edge of the count input signal when UP/DOWN is high. It is decremented when UP/DOWN is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments.

The STORE pin controls the internal latches and consequently the signals appearing at the 7-segment and BCD outputs. Bringing the STORE pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the RST pin low. The count input is inhibited during reset and load counter operations. The STO, RST and UP/DOWN pins are provided with pullup resistors of approximately 75 kΩ.

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately 1/2 V^+ for normal operation. With both LC and LR open, and thumbwheel switches (if used) set to "zero" (open), the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex. In this mode of operation, the BCD pins will drive one TTL load. When either or both of the LC or LR pins is connected to V^+, the TTL driver devices are turned off and the BCD pins become high-impedance inputs. When LC is connected to V^+, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V^+, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V^+, the count is inhibited and both register and counter are presettable. When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, EQUAL, ZERO, UP/DOWN, RESET and STORE functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" (pg. 5) for a cataloging of the pins that function as three-state self-biased inputs and their respective operations.

Note that the ICM7217 and 7217B have been designed to drive common anode displays. The BCD inputs are active high, as are the BCD outputs.

The ICM7217A and 7217C are used to drive common cathode displays, and the BCD inputs are active low. BCD outputs are active high.

NOTES ON THUMBWHEEL SWITCHES & MULTIPLEXING

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000.

Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. See fig. 4.

In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914).

During load counter and load register operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven, however the internal oscillator signal will be of the same duty cycle and phase as the overdriving signal, and the digits are blanked during the time the external signal is at a positive level. To insure proper leading zero blanking, the blanking time should not be less than about 2μs, and by varying the duty cycle, the display brightness may be altered. Overdriving the oscillator at less than 200Hz may cause display flickering. See fig. 6 for brightness control circuits.

These circuits are variable-duty-cycle oscillators suitable for overdriving the multiplex oscillator at the SCAN input of an ICM7217. The inverters should be CMOS CD4000 series, and the diodes may be any inexpensive device such as IN914.

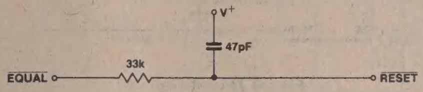
When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken high, the chip executes a sequence of operations that reads the thumbwheel switches. These inputs are edge-triggered, and pulsing them high for 500 ns at room temperature will initiate a full thumbwheel switch scan and data entry cycle.

When the circuit recognizes that a load input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4 digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4.

When using the digit outputs as strobes into the thumbwheel switches, the switched BCD data is inputted and automatically synchronized to the appropriate digit. When using the digit outputs to gate external logic, it must be remembered that input data must be valid at the trailing edge of the digit output.

The preset circuitry is used to perform the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the $\overline{\text{RESET}}$ input is low, the register will be set to zero, since the input lines are forced to zero.

When using the circuit as a programmable divider (÷ by N with equal outputs) a short time delay (about 1μs) is needed on the $\overline{\text{EQUAL}}$ output to allow the $\overline{\text{RESET}}$ input to establish a valid duration reset pulse.



When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching $\overline{\text{EQUAL}}$), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. $\overline{\text{RESET}}$ will not clear the register.

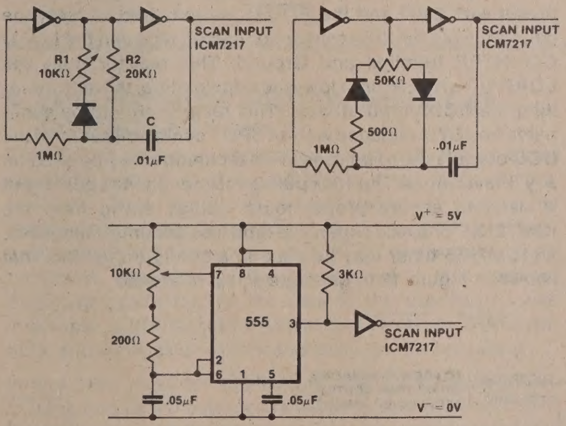


Figure 6: Brightness Circuits

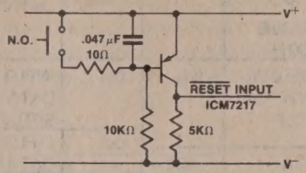
OUTPUT AND INPUT RESTRICTIONS

The CARRY/BORROW output is not valid during load counter and reset operations.

The $\overline{\text{EQUAL}}$ output is not valid during load counter or load register operations.

The $\overline{\text{ZERO}}$ output is not valid during a load counter operation.

The $\overline{\text{RESET}}$ input may be susceptible to noise if its input rise time (counting out of reset) is greater than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the RESET input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{RESET}}$ input is shown below.



CONTROL OF 7227 VERSIONS

The 7227 series has been designed to permit microprocessor control of the inputs. BCD inputs and outputs are active high.

In the IM7227 versions, the STORE, UP/$\overline{\text{DOWN}}$, SC1 and SC2 (select code bits 1 and 2) pins form a four-bit control word input. A negative-going pulse on the $\overline{\text{CWS}}$ (control word strobe) pin writes the data on these pins into four internal control latches, and resets the multiplex counter in preparation for sequencing a data transfer operation. The select code 00 is reserved for changing the state of the Store and/or Up/$\overline{\text{Down}}$ latches without initiating a data transfer. Writing a one into the Store latch sets the latch and causes the data in the counter to be transferred into the output latches, while writing a zero resets the latches causing them to retain data and not be updated. Similarly, writing a one into the Up/$\overline{\text{Down}}$ latch causes the counter to count up and writing a zero causes the counter to count down. The state of the Store and Up/$\overline{\text{Down}}$ latches may also be changed with a nonzero select code.

Writing a nonzero select code initiates a data transfer operation. Writing select code of 01 (SC1, SC2) indicates that the data in the output latches will be active and enables the BCD I/O port to output the data. Writing a select code of 11 indicates that the register will be preset, and a 10 indicates that the counter will be preset.

When a nonzero select code is read, the clock of the four-state multiplex counter is switched to the $\overline{\text{DT}}$ ($\overline{\text{DATA TRANSFER}}$) pin. Negative-going pulses at this pin then sequence a digit-by-digit data transfer, either outputting data or presetting the counter or register as determined by the select code. The output drivers of the BCD I/O port will be enabled only while $\overline{\text{DT}}$ is low during a data transfer initiated with a 01 select code.

The sequence of digits will be D4-D3-D2-D1, i.e. when outputting, the data from D4 will be valid during the first $\overline{\text{DT}}$ pulse, then D3 will be valid during the second pulse, etc. When presetting, the data for D4 must be valid at the positive-going transition (trailing edge) of the first $\overline{\text{DT}}$ pulse, the data for D3 must be valid during the second $\overline{\text{DT}}$ pulse, etc.

At the end of a data transfer operation, on the positive going transition of the fourth $\overline{\text{DT}}$ pulse, the SC1 and SC2 control latches will automatically reset, terminating the data transfer and reconnecting the multiplex counter clock to the oscillator. In the ICM7227 versions, the multiplex oscillator is always free-running, except during a data transfer operation when it is disabled.

Fig. 5 shows the timing of data transfers initiated with a 11 select code (writing into the register) and a 01 select code (reading out of the output latches). Typical times during which data must be valid at the control word and BCD I/O ports are indicated in Table 2.

Table 2

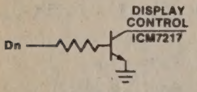
SYMBOL	DEFINITION	TIME, NS	SYMBOL	DEFINITION	TIME, NS
$t_{\overline{cws}}$	CONTROL WORD STROBE WIDTH	275	t_{cdh}	CONTROL DATA HOLD	300
t_{ics}	INTERNAL CONTROL SETUP	2-3μs	t_{ids}	INPUT DATA SETUP	-300
			t_{idh}	INPUT DATA HOLD	300
$t_{\overline{dt}}$	DATA TRANSFER PULSE WIDTH	300	t_{oda}	OUTPUT DATA ACCESS	300
t_{cds}	CONTROL DATA SETUP	300	t_{odh}	OUTPUT DATA HOLD	300

APPLICATIONS

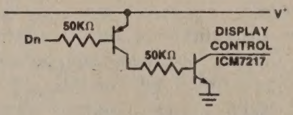
1. FIXED DECIMAL POINT

In the common anode versions, a fixed decimal point may be activated by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to Ground. With common cathode devices, the D.P. segment lead should be connected through a 75Ω series resistor to V$^+$.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown below with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display. See Figure 9 for a similarly operating multi-digit connection.


DISPLAY CONTROL ICM7217
Dn

COMMON ANODE


V+
50KΩ
Dn
DISPLAY CONTROL ICM7217
50KΩ

COMMON CATHODE

2. UNIT COUNTER WITH BCD OUTPUT (Figure 7)

The simplest application of the ICM7217 is a 4 digit unit counter. All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A and a common-cathode calculator-type display, results in the least expensive digital counter/display system available.

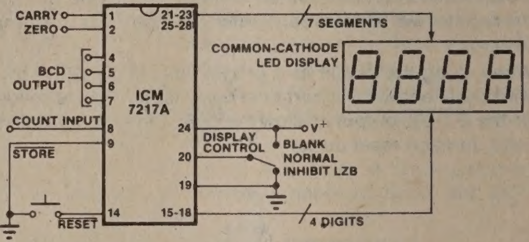

CARRY
ZERO
BCD OUTPUT
COUNT INPUT
STORE
RESET
1
2
4
5
6
7
8
9
14
21-23
25-28
ICM 7217A
24
20
19
15-18
7 SEGMENTS
COMMON-CATHODE LED DISPLAY
8888
DISPLAY CONTROL
V+
BLANK
NORMAL
INHIBIT LZB
4 DIGITS

Figure 7: Unit Counter

3. PRECISION ELAPSED TIME/COUNTDOWN TIMER (Figure 8)

This circuit uses an ICM7213 precision one minute/one second timebase generator using a 4.1943 MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{\text{EQUAL}}$ output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used. This technique may be used on any 3-level input. The 100k pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 12 to generate a 1Hz reference.

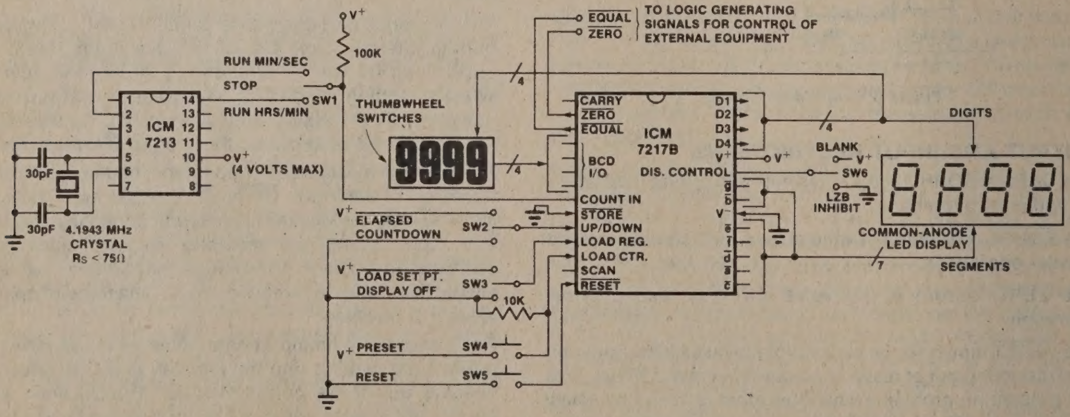

V+
100K
RUN MIN/SEC
STOP
SW1
RUN HRS/MIN
ICM 7213
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V+ (4 VOLTS MAX)
30pF
30pF
4.1943 MHz CRYSTAL Rs < 75Ω
THUMBWHEEL SWITCHES
9999
4
4
EQUAL
ZERO
TO LOGIC GENERATING SIGNALS FOR CONTROL OF EXTERNAL EQUIPMENT
CARRY
ZERO
EQUAL
ICM 7217B
BCD I/O
COUNT IN
STORE
UP/DOWN
LOAD REG.
LOAD CTR.
SCAN
RESET
D1
D2
D3
D4
V+
DIS. CONTROL
V-
g
b
e
f
d
a
c
V+
ELAPSED
COUNTDOWN
SW2
V+
LOAD SET PT.
DISPLAY OFF
SW3
10K
V+ PRESET
SW4
RESET
SW5
DIGITS
4
BLANK
V+
SW6
LZB INHIBIT
8888
COMMON-ANODE LED DISPLAY
7
SEGMENTS

Figure 8: Precision Timer

4. 8-DIGIT UP/DOWN COUNTER (Figure 9)

This circuit shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\overline{a}$ or $\overline{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize. This presents no problems with the ICM7227 devices, since the two devices are operated as peripherals to a processor.

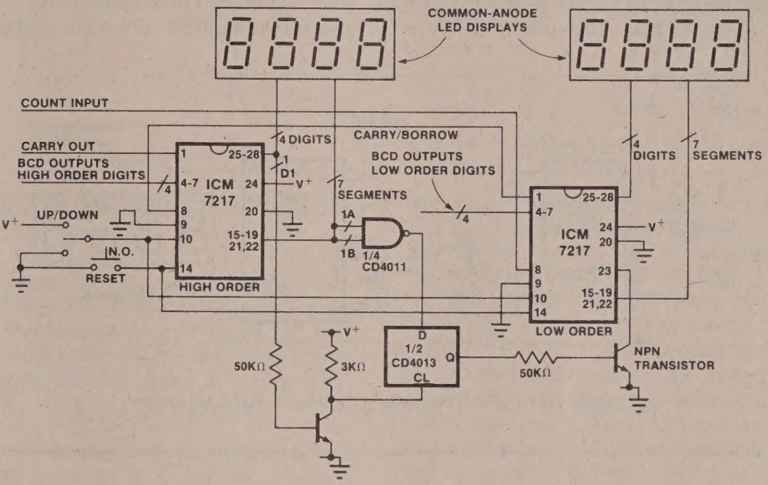

COMMON-ANODE LED DISPLAYS
COUNT INPUT
CARRY OUT
BCD OUTPUTS HIGH ORDER DIGITS
4
4-7
ICM 7217
1
25-28
24
20
8
9
10
14
15-19 21,22
HIGH ORDER
4 DIGITS
D1
V+
7 SEGMENTS
CARRY/BORROW
BCD OUTPUTS LOW ORDER DIGITS
1A
1B
1/4 CD4011
UP/DOWN
N.O.
RESET
4 DIGITS
7 SEGMENTS
23
LOW ORDER
D
1/2 CD4013
Q
CL
50KΩ
3KΩ
50KΩ
NPN TRANSISTOR

Figure 9: 8 Digit Up/Down Counter

5. TAPE RECORDER POSITION INDICATOR/ CONTROLLER (Figure 10)

This circuit shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an ICM7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs, and serve as a numerical display for the processor.

In the tape recorder application, the LOAD REGISTER, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{\text{EQUAL}}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the $\overline{\text{ZERO}}$ output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and .0047 µF capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

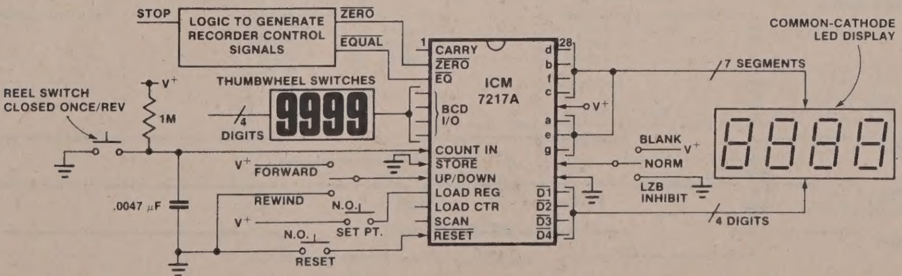

STOP
LOGIC TO GENERATE RECORDER CONTROL SIGNALS
ZERO
EQUAL
THUMBWHEEL SWITCHES
9999
4
DIGITS
REEL SWITCH CLOSED ONCE/REV
V+
1M
.0047 µF
FORWARD
REWIND
N.O.
SET PT.
RESET
1
28
CARRY
ZERO
EQ
ICM 7217A
BCD I/O
COUNT IN
STORE
UP/DOWN
LOAD REG
LOAD CTR
SCAN
RESET
d
b
f
c
a
e
g
D1
D2
D3
D4
7 SEGMENTS
COMMON-CATHODE LED DISPLAY
BLANK
NORM
LZB INHIBIT
4 DIGITS

Figure 10: Recorder Indicator

6. PRECISION FREQUENCY COUNTER/ TACHOMETER (Figure 11)

This circuit is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V^+, the gating time will be 0.1 second; this will display tens of hertz as the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536 MHz crystal), giving a 0.01 second gating with Pin 11 connected to V^+, and a 0.1 second gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

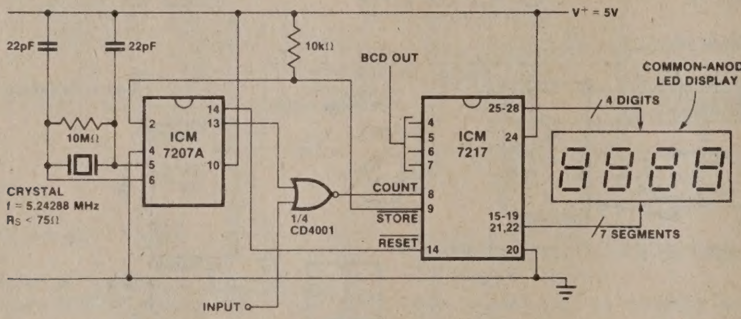

V+ = 5V
22pF
22pF
10kΩ
BCD OUT
COMMON-ANODE LED DISPLAY
4 DIGITS
10MΩ
ICM 7207A
ICM 7217
CRYSTAL f = 5.24288 MHz RS < 75Ω
1/4 CD4001
COUNT
STORE
RESET
7 SEGMENTS
INPUT

Figure 11: Precision Frequency Counter (~1MHz Maximum)

7. INEXPENSIVE FREQUENCY COUNTER/ TACHOMETER (Figure 12)

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals. To provide the gating signal, the timer is configured as an astable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately one second and negative for approximately 300-500μs. The positive waveform time is given by $t_{wp} = 0.693 (R_A + R_B) C$ while the negative waveform is given by $t_{wn} = 0.693 R_B C$. The system is calibrated by using a 5MΩ potentiometer for R_A as a "coarse" control and a 1k potentiometer for R_B as a "fine" control. CD40106B's are used as a monostable multivibrator and reset time delay.

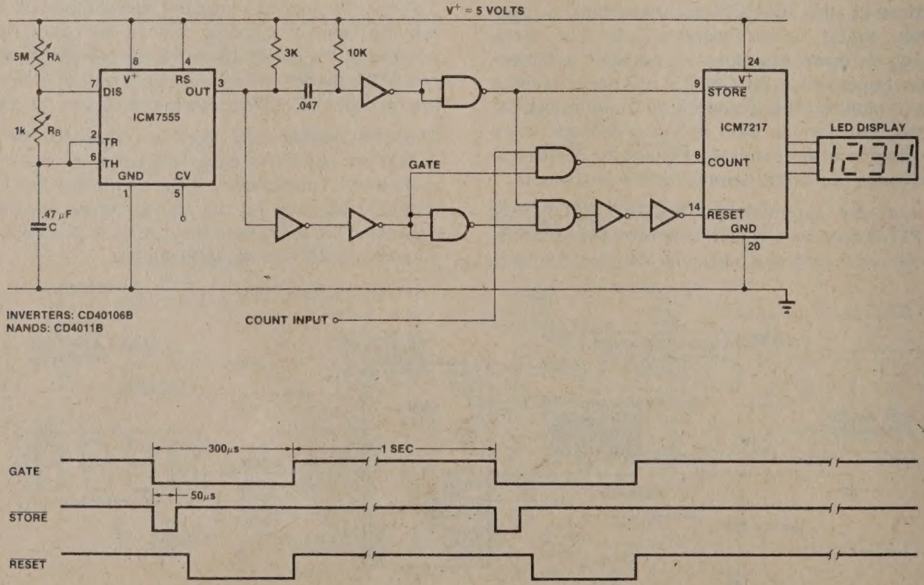

V+ = 5 VOLTS
5M RA
1k RB
.47μF C
ICM7555
3K
10K
.047
GATE
ICM7217
STORE
COUNT
RESET
GND
LED DISPLAY
1234
INVERTERS: CD40106B
NANDS: CD4011B
COUNT INPUT
300μs
1 SEC
50μs
GATE
STORE
RESET

Figure 12: Inexpensive Frequency Counter

8. LCD DISPLAY INTERFACE (Figure 13)

The low-power operation of the ICM7217 makes an LCD interface desirable. The Intersil ICM7211 4 digit BCD to LCD display driver easily interfaces to the ICM7217. Total system power consumption is less than 5mW.

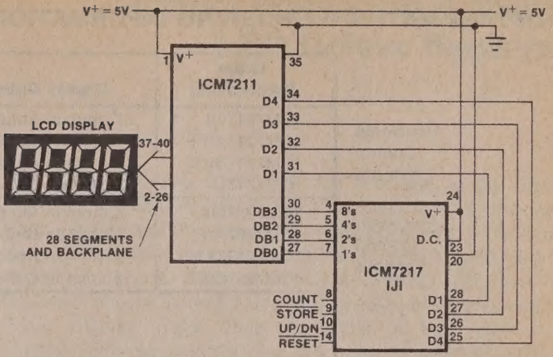

V+ = 5V
V+ = 5V
1
V+
ICM7211
35
34
D4
33
D3
32
D2
31
D1
LCD DISPLAY
37-40
2-26
28 SEGMENTS AND BACKPLANE
30
DB3
29
DB2
28
DB1
27
DB0
4
8's
5
4's
6
2's
7
1's
24
V+
D.C.
23
20
ICM7217 IJI
COUNT
8
STORE
9
UP/DN
10
RESET
14
D1
28
D2
27
D3
26
D4
25

Figure 13: LCD Display Interface

9. MICROPROCESSOR INTERFACE-ICM7227 (Figure 14)

This circuit shows the hardware necessary to interface the ICM7227 to an Intersil IM6100 CMOS microprocessor. Using an IM6101 Parallel Interface Element (PIE) allows the addition of one or more ICM7227 devices as generalized peripherals to any IM6100 system, using a minimum of external components.

A similar configuration may be used with the MC6800 using the corresponding PIE, while an 8223 can be used to interface 8080 based systems.

The ICM7227 can perform many "accessory" functions that are inefficient or impossible for the processor to perform. For simple systems, the ICM7227 can provide a cost-effective display latch/decoder/driver. By adding a timebase such as an ICM7213, and using an ICM7227C or D, an inexpensive real-time clock/display, directly accessible by the processor, can be constructed.

In the area of "intelligent" instrumentation, the ICM7227 can serve as a high speed (up to 750kHz) counter/comparator. This is the element often used for converting time, frequency, and positional and occurence data into digital form. For example, an ICM7207A can be used with two ICM7227's to provide an 8 digit, 2MHz frequency counter.

Since the ICM7207A gating output has a 50% duty cycle, there is 1 second for the processor to respond to an interrupt, generated by the negative going edge of this signal while it inhibits the count. The processor can respond to the interrupt using ROM based subroutines, to store the data, reset the counter, and read the data into main memory. To add simultaneous period display, the processor inverts the data and an ICM7218 Universal Display Driver stores and displays it. Capacitance can be measured by counting the frequency of an oscillator, thereby allowing the measurement of fluid levels, proximity detectors, etc.

Future Application Notes and Bulletins will address the ICM7227 more fully, and users are welcome to submit any circuits or unique uses for review and possible publication in application information.

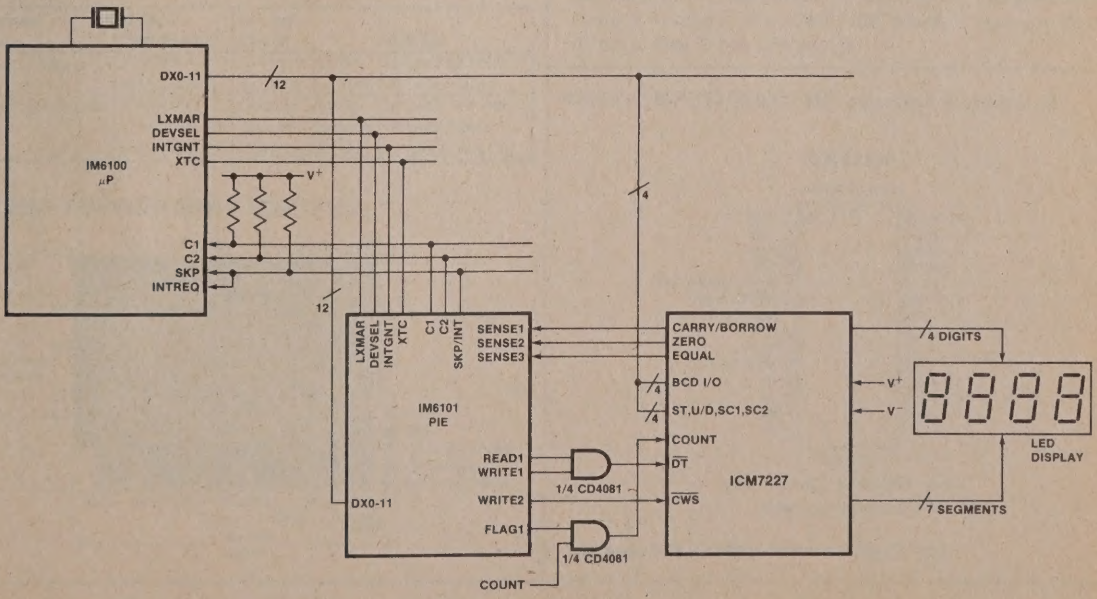

IM6100 μP
DX0-11
12
LXMAR
DEVSEL
INTGNT
XTC
V+
C1
C2
SKP
INTREQ
12
4
LXMAR
DEVSEL
INTGNT
XTC
C1
C2
SKP/INT
SENSE1
SENSE2
SENSE3
IM6101 PIE
READ1
WRITE1
DX0-11
WRITE2
FLAG1
1/4 CD4081
1/4 CD4081
COUNT
CARRY/BORROW
ZERO
EQUAL
BCD I/O
4
ST,U/D,SC1,SC2
4
COUNT
DT
CWS
ICM7227
4 DIGITS
V+
V−
LED DISPLAY
7 SEGMENTS

Figure 14: IM6100 Interface

OPTION MATRIX & ORDERING INFORMATION

	Order Part Number	Display Option	Count Option Max Count	28-LEAD Package
Hardwired Control Versions	ICM7217IJI	Common Anode	Decade/9999	CERDIP
	ICM7217AIPI	Common Cathode	Decade/9999	PLASTIC
	ICM7217BIJI	Common Anode	Timer/5959	CERDIP
	ICM7217C	Common Cathode	Timer/5959	PLASTIC
Processor Control Versions	ICM7227IJI	Common Anode	Decade/9999	CERDIP
	ICM7227AIPI	Common Cathode	Decade/9999	PLASTIC
	ICM7227BIJI	Common Anode	Timer/5959	CERDIP
	ICM7227CIPI	Common Cathode	Timer/5959	PLASTIC

INTERSIL

ICM7218 Series
CMOS Universal 8 Digit LED Driver System

FEATURES

- **Total circuit integration on chip includes:**
  - **a) Digit and segment drivers**
  - **b) All multiplex scan circuitry**
  - **c) 8X8 static memory**
  - **d) 7 segment Hexadecimal and Code B decoders**
- **Output drive suitable for large LED displays**
- **Both common anode and common cathode LED drive versions**
- **Single 5 volt supply required**
- **Data retention to 2 volts supply**
- **Shutdown feature - turns off display and puts chip into very low power dissipation mode**
- **Pin selectable choice of 2 seven segment decoders - Hexa or Code B - or no decode**
- **Microprocessor compatible**
- **Serial and random access versions**
- **Decimal point drive on each digit**

GENERAL DESCRIPTION

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems and an LED display. Included on chip is an 8x8 static memory array providing storage for the displayed information, 2 types of 7 segment decoders, all the multiplex scan circuitry and the high power digit and segment drivers.

The ICM7218A and ICM7218B are intended to be used primarily in microprocessor systems. Data is read directly from the I/O bus line from the microprocessor. 2 Control lines ($\overline{\text{Write}}$, and Mode) define chip select, which reads either 4 bits of control information (Data Coming, $\overline{\text{Shutdown}}$, Decode, Hexa or Code B Decoding) or 8 bits of Display Input Data. Display Input Data (8 words, 8 bits each) is automatically sequenced into the memory on successive positive going $\overline{\text{Write}}$ pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The ICM7218A drives a common anode display while the ICM7218B drives a common cathode display. (See Block Diagram 1)

The ICM7218C and ICM7218D feature 2 lines for control information ($\overline{\text{Write}}$, Three Level Input; Hexa, Code B, $\overline{\text{Shutdown}}$), 4 lines for Input Data and 3 lines for Data Addressing of each of eight data memory locations.

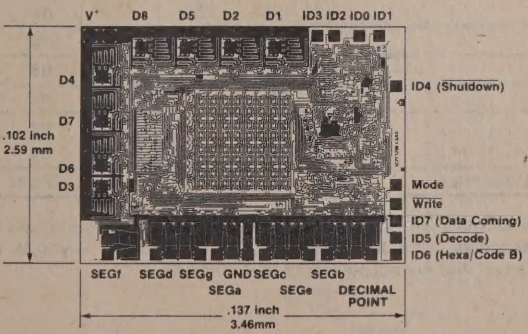
Data is written into memory by setting up a Data Address memory location, defining 4 lines of Input Data and then strobe the $\overline{\text{Write}}$ line low. The Three Level Control Input is independent of the $\overline{\text{Write}}$ instruction. Only Hexadecimal and Code B decoding are available for the Display Outputs. The ICM7218C drives a common anode display, the ICM7218D a common cathode display. (See Block Diagram 2)

The ICM7218E provides 4 separate lines for control information ($\overline{\text{Write}}$, Hexa-Code B, Decode, $\overline{\text{Shutdown}}$), 8 lines for input data, and 3 lines for digit address. Data is written into the memory by setting up a Data Address memory location, defining 8 lines of Input Data, and then strobe the $\overline{\text{Write}}$ line low. Control information is on separate lines and is independent of the $\overline{\text{Write}}$ instruction. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The ICM7218E drives a common anode display. (See Block Diagram 3)

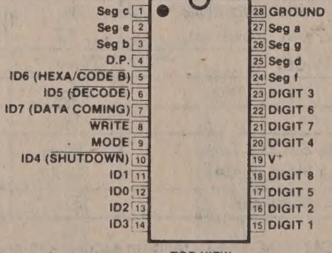
ORDERING INFORMATION

Typical App.	Order Part Number	Display Option	Package
Serial Access	ICM7218A IJI	Common Anode	28 Lead CERDIP
	ICM7218B IPI	Common Cathode	28 Lead Plastic
Random Access	ICM7218C IJI	Common Anode	28 Lead CERDIP
	ICM7218D IPI	Common Cathode	28 Lead Plastic
	ICM7218E IDL	Common Anode	40 Lead Ceramic

CHIP TOPOGRAPHY ICM7218A


V+
D8
D5
D2
D1
ID3 ID2 ID0 ID1
D4
D7
.102 inch
2.59 mm
D6
D3
ID4 (Shutdown)
Mode
Write
ID7 (Data Coming)
ID5 (Decode)
ID6 (Hexa/Code B)
SEGf
SEGd
SEGg
GND
SEGc
SEGb
SEGa
SEGe
DECIMAL POINT
.137 inch
3.46mm

PIN CONFIGURATION (OUTLINE DRAWING JI)


ICM7218A
COMMON ANODE
Seg c 1
Seg e 2
Seg b 3
D.P. 4
ID6 (HEXA/CODE B) 5
ID5 (DECODE) 6
ID7 (DATA COMING) 7
WRITE 8
MODE 9
ID4 (SHUTDOWN) 10
ID1 11
ID0 12
ID2 13
ID3 14
28 GROUND
27 Seg a
26 Seg g
25 Seg d
24 Seg f
23 DIGIT 3
22 DIGIT 6
21 DIGIT 7
20 DIGIT 4
19 V+
18 DIGIT 8
17 DIGIT 5
16 DIGIT 2
15 DIGIT 1
TOP VIEW

Note: Pins 5, 6, 7, 10 are under control of Mode pin 9. See page 6-72.

See page 6-69 for other device configurations.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Digit Output Current 300mA
Segment Output Current 50mA
Input Voltage (any terminal) .... V^+ +0.3V to V^- −0.3V
NOTE 1
Power Dissipation (28 Pin CERDIP) .... 1 W NOTE 2
Power Dissipation (28 Pin Plastic) .... 0.5 W NOTE 2
Power Dissipation (40 Pin Ceramic) .... 1 W NOTE 2
Operating Temperature Range .... −20°C to +85°C
Storage Temperature Range .... −55°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.

NOTE 2: These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C.

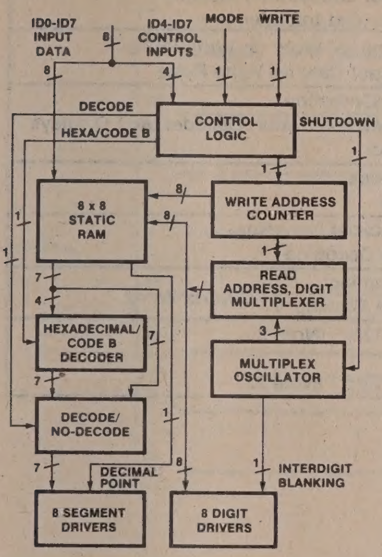
SYSTEM ELECTRICAL CHARACTERISTICS $V^+ = 5V \pm 10\%$; $T_A = 25°C$, Test Circuit, Display Diode Drop 1.7V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V^+	 Power Down Mode	4 2		6 6	V V
Quiescent Supply Current	I_Q	Shutdown (Note 3)	6	10	300	μA
Operating Supply Current	I_{OP}	Decoder On, Outputs Open Ckt No Decode, Outputs Open Ckt	250 200		950 450	μA μA
Digit Drive Current	I_{DIG}	Common Anode Vout = V^+ −2.0 Common Cathode Vout = V^- +1V	−170 50			mA mA
Digit Leakage Current	I_{DLK}				100	μA
Peak Segment Drive Current	I_{SEG}	Common Anode Vout = V^- +1.5V Common Cathode Vout = V^+ −2.0V	20 −10	25		mA mA
Segment Leakage Current	I_{SLK}				50	μA
Display Scan Rate	f_{MUX}	Per Digit		250		Hz
Three Level Input Logical "1" Input Voltage Floating Input Logical "0" Input Voltage	 V_{INH} V_{INF} V_{INL}	 Hexidecimal ICM7218C, D (Pin 9) Code B ICM7218C, D (Pin 9) Shutdown ICM7218C, D (Pin 9)	 4.0 2.0 		 3.0 1.75	 V V V
Three Level Input Impedance	Z_{IN}	Note 3		100		kΩ
Logical "1" Input Voltage Logical "0" Input Voltage	V_{IH} V_{IL}		3.5 		 .8	V V
Write Pulse Width (Negative) Write Pulse Width (Positive)	t_W $t_{\overline{W}}$	}7218A, B	550 550	400 400		ns ns
Write Pulse Width (Negative) Write Pulse Width (Positive)	t_W $t_{\overline{W}}$	}7218C, D, E	400 400	250 250		ns ns
Mode Pulse Width	t_m	7218A, B	500			ns
Data Set Up Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		25			ns
Digit Address Set Up Time Digit Address Hold Time	t_{das} t_{dah}	ICM7218C, D, E ICM7218C, D, E	500 100			ns ns
Data Input Impedance	Z_{IN}	5-10 pF Gate Capacitance		10^{10}		Ohms

NOTE 3: In the ICM7218C and D (random access versions) the Hexa/Code B/$\overline{\text{Shutdown}}$ Input (Pin 9) has internal biasing resistors to hold it at $V^+/2$ when Pin 9 is open circuited. These resistors consume power and result in a Quiescent Supply Current (I_Q) of typically 50μA. The ICM7218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.

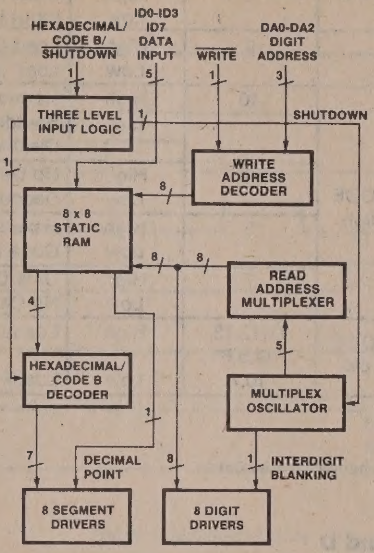
BLOCK DIAGRAMS

ICM7218A, ICM7218B


ID0-ID7 INPUT DATA
8
ID4-ID7 CONTROL INPUTS
MODE
WRITE
8
4
1
1
DECODE
HEXA/CODE B
CONTROL LOGIC
SHUTDOWN
1
1
1
1
8 x 8 STATIC RAM
8
8
WRITE ADDRESS COUNTER
1
READ ADDRESS, DIGIT MULTIPLEXER
7
4
HEXADECIMAL/ CODE B DECODER
7
3
MULTIPLEX OSCILLATOR
7
DECODE/ NO-DECODE
1
7
DECIMAL POINT
8
1
INTERDIGIT BLANKING
8 SEGMENT DRIVERS
8 DIGIT DRIVERS

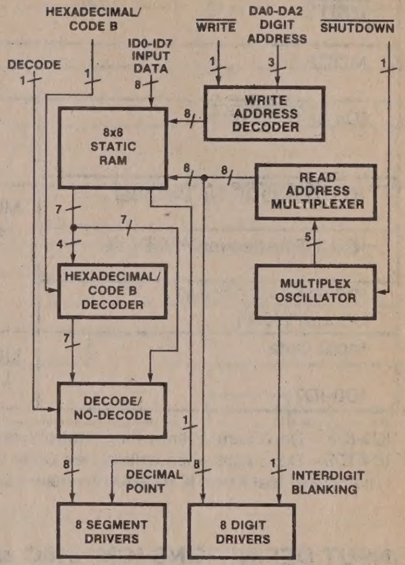
①

ICM7218C, ICM7218D


HEXADECIMAL/ CODE B/ SHUTDOWN
ID0-ID3 ID7 DATA INPUT
WRITE
DA0-DA2 DIGIT ADDRESS
1
5
1
3
THREE LEVEL INPUT LOGIC
1
SHUTDOWN
1
WRITE ADDRESS DECODER
8
8 x 8 STATIC RAM
8
8
READ ADDRESS MULTIPLEXER
4
5
HEXADECIMAL/ CODE B DECODER
MULTIPLEX OSCILLATOR
1
7
DECIMAL POINT
8
1
INTERDIGIT BLANKING
8 SEGMENT DRIVERS
8 DIGIT DRIVERS

②

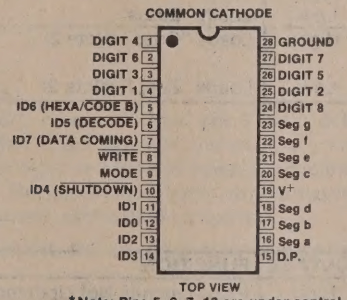
ICM7218E


HEXADECIMAL/ CODE B
WRITE
DA0-DA2 DIGIT ADDRESS
SHUTDOWN
DECODE
ID0-ID7 INPUT DATA
1
1
8
1
3
1
WRITE ADDRESS DECODER
8
8x8 STATIC RAM
8
8
READ ADDRESS MULTIPLEXER
7
7
4
5
HEXADECIMAL/ CODE B DECODER
MULTIPLEX OSCILLATOR
7
DECODE/ NO-DECODE
1
8
DECIMAL POINT
8
1
INTERDIGIT BLANKING
8 SEGMENT DRIVERS
8 DIGIT DRIVERS

③

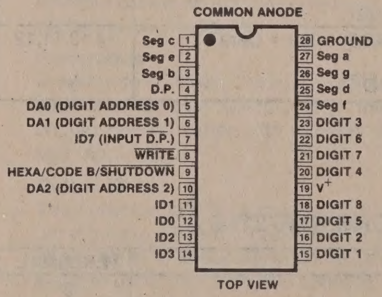
PIN CONFIGURATIONS (See page 6-67 for ICM7218A)

ICM7218B* (OUTLINE DRAWING PI)

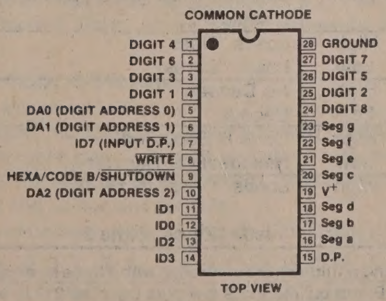

COMMON CATHODE
DIGIT 4 1
DIGIT 6 2
DIGIT 3 3
DIGIT 1 4
ID6 (HEXA/CODE B) 5
ID5 (DECODE) 6
ID7 (DATA COMING) 7
WRITE 8
MODE 9
ID4 (SHUTDOWN) 10
ID1 11
ID0 12
ID2 13
ID3 14
28 GROUND
27 DIGIT 7
26 DIGIT 5
25 DIGIT 2
24 DIGIT 8
23 Seg g
22 Seg f
21 Seg e
20 Seg c
19 V+
18 Seg d
17 Seg b
16 Seg a
15 D.P.
TOP VIEW

*Note: Pins 5, 6, 7, 10 are under control of Mode pin 9. See page 6.

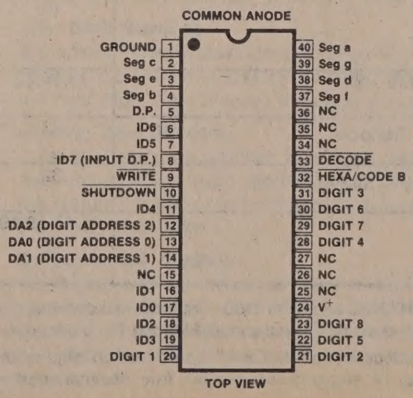
ICM7218C (OUTLINE DRAWING JI)


COMMON ANODE
Seg c 1
Seg e 2
Seg b 3
D.P. 4
DA0 (DIGIT ADDRESS 0) 5
DA1 (DIGIT ADDRESS 1) 6
ID7 (INPUT D.P.) 7
WRITE 8
HEXA/CODE B/SHUTDOWN 9
DA2 (DIGIT ADDRESS 2) 10
ID1 11
ID0 12
ID2 13
ID3 14
28 GROUND
27 Seg a
26 Seg g
25 Seg d
24 Seg f
23 DIGIT 3
22 DIGIT 6
21 DIGIT 7
20 DIGIT 4
19 V+
18 DIGIT 8
17 DIGIT 5
16 DIGIT 2
15 DIGIT 1
TOP VIEW

ICM7218D (OUTLINE DRAWING PI)


COMMON CATHODE
DIGIT 4 1
DIGIT 6 2
DIGIT 3 3
DIGIT 1 4
DA0 (DIGIT ADDRESS 0) 5
DA1 (DIGIT ADDRESS 1) 6
ID7 (INPUT D.P.) 7
WRITE 8
HEXA/CODE B/SHUTDOWN 9
DA2 (DIGIT ADDRESS 2) 10
ID1 11
ID0 12
ID2 13
ID3 14
28 GROUND
27 DIGIT 7
26 DIGIT 5
25 DIGIT 2
24 DIGIT 8
23 Seg g
22 Seg f
21 Seg e
20 Seg c
19 V+
18 Seg d
17 Seg b
16 Seg a
15 D.P.
TOP VIEW

ICM7218E (OUTLINE DRAWING DL)


COMMON ANODE
GROUND 1
Seg c 2
Seg e 3
Seg b 4
D.P. 5
ID6 6
ID5 7
ID7 (INPUT D.P.) 8
WRITE 9
SHUTDOWN 10
ID4 11
DA2 (DIGIT ADDRESS 2) 12
DA0 (DIGIT ADDRESS 0) 13
DA1 (DIGIT ADDRESS 1) 14
NC 15
ID1 16
ID0 17
ID2 18
ID3 19
DIGIT 1 20
40 Seg a
39 Seg g
38 Seg d
37 Seg f
36 NC
35 NC
34 NC
33 DECODE
32 HEXA/CODE B
31 DIGIT 3
30 DIGIT 6
29 DIGIT 7
28 DIGIT 4
27 NC
26 NC
25 NC
24 V+
23 DIGIT 8
22 DIGIT 5
21 DIGIT 2
TOP VIEW

INPUT DEFINITIONS ICM7218A and B

INPUT		TERMINAL	VOLTAGE	FUNCTION
WRITE		8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
MODE		9	High Low	Load Control Word on Write Pulse Load Input Data on Write Pulse
ID4 SHUTDOWN	MODE High	10	High Low	Normal Operation Shutdown (Oscillator, Decoder, and Displays Disabled)
ID5 (DECODE/No Decode)		6	High Low	No Decode Decode
ID6 (HEXAdecimal/CODE B)		5	High Low	Hexadecimal Decoding Code B Decoding
ID7 (DATA COMING - Control Word)		7	High Low	Data Coming } Control Word No Data Coming } Control Word
Input Data ID0-ID7*	MODE Low	11,12,13, 14,5,6 10,7	High Low	Loads "One" (Note 2) Loads "Zero" (Note 2)

*ID0-ID3 = Don't care when writing control word
ID4-ID7 = Don't care when writing Hex/Code B
(The display blanks on ICM7218A/B versions when writing in Data)

INPUT DEFINITIONS ICM7218C and D

INPUT	TERMINAL	VOLTAGE	FUNCTION
WRITE	8	High Low	Inputs Not Loaded Into Memory Inputs Loaded Into Memory
Three Level Input (Note 1)	9	High Floating Low	Hexadecimal Decode Code B Decode Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address DA2 (MSB)-DA0 (LSB)	10,6,5	High Low	Loads "Ones" Loads "Zeros"
Input Data ID3 (MSB) - ID0 = Data ID7 = D.P.	14,13,11,12 7	High Low	Loads "Ones" (Note 2) Loads "Zeros" (Note 2)

INPUT DEFINITIONS ICM7218E

INPUT	TERMINAL	VOLTAGE	FUNCTION
WRITE	9	High Low	Input Latches Not Updated Input Latches Updated
SHUTDOWN	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address (0,1,2) DA0-DA2	13,14,12	High Low	Loads "Ones" Loads "Zeros"
DECODE/No Decode	33	High Low	No Decode Decode
HEXAdecimal/CODE B	32	High Low	Code B Decoding Hexadecimal Decoding
Input Data ID0-ID7	16,17,18,19 6 7,11,8	High Low	Loads "Ones" (Note 2) Loads "Zeros" (Note 2)

NOTE 1 In the ICM7218C and ICM7218D versions, Hexadecimal, Code B and Shutdown are controlled with a three level input on Pin 9. Pulling Pin 9 high decodes Hexadecimal. Floating Pin 9 decodes Code B and pulling Pin 9 low puts the ICM7218 in a Shutdown mode.

NOTE 2 In the No Decode format, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents "on" segments, (i.e. segments are positive true, decimal point is negative true).

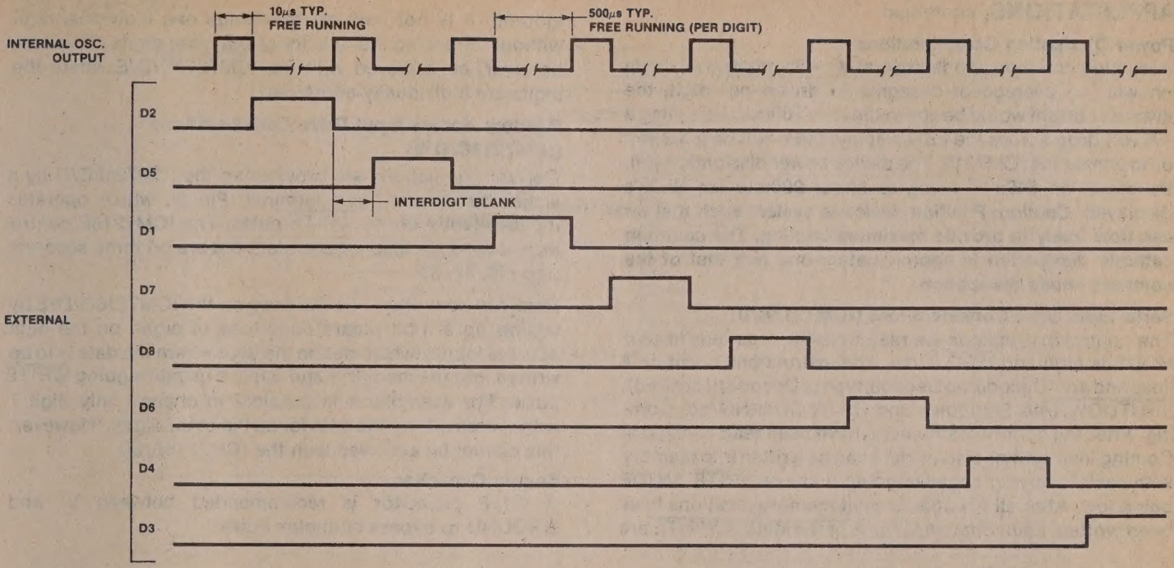


Figure 1: Multiplex Timing

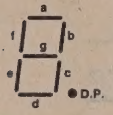


Figure 2: Segment Assignments

DECODE/No Decode

For the ICM7218A/B/E products, there are 3 input data formats possible; either direct segment and decimal point information (8 bits per digit) or 2 Binary codes plus decimal point (5 bits per digit). The 7 segment decoder on chip may be disabled if direct segment information is inputted.

In the No Decode format, the inputs directly control the outputs as follows:

Input Data:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Output Segments:	$\overline{\text{D.P.}}$	a	b	c	e	g	f	d

In this format, "Ones" represents on segments for all inputs except for the Decimal Point, where "zero' represents on segments.

HEXAdecimal or CODE B Decoding

For all products, a choice of either HEXA or Code B decoding may be made, HEXA decoding provides 7 segment numeric plus six alpha characters while Code B provides a negative sign (—), a blank (for leading zero blanking), certain useful alpha characters and all numeric formats.

The four bit binary code is set up on inputs ID3-ID0.

Binary Code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexa Code	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F
Code B	0	1	2	3	4	5	6	7	8	9	-	E	H	L	P	(Blank)

SHUTDOWN

SHUTDOWN performs several functions: it puts the device into a very low dissipation mode (typically 10μA at $V^+ = 5$), turns off both the digit and segment drivers, stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input data to the memory during shutdown - only the output and read sections of the device are disabled.

Powerdown

In a Shutdown Mode, the supply voltage may be reduced to 2 volts without data being lost in memory. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With 5 segments being driven, this is equal to about 40mA per segment peak drive or 5mA average drive. The common cathode drive is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately 10μs occurs between digit strobes to ensure that segment information is correct before the next digit drive thereby avoiding ghosting.

Leading Zero Blanking

This may be programmed into chip memory in the no-decode operation (each segment programmed for a zero for the blanked digits) or by using the 16th state (binary 15) with the Code B decoder.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to parallel connect digit drives together. For example, by paralleling pairs of digit drives together to drive a 4 digit display 10 mA average segment drive can be obtained.

APPLICATIONS, continued

Power Dissipation Considerations

Assuming common anode drive at $V^+ = 5$ volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming a 1.8 volt drop across the LED display, there will be a 3.2 volt drop across the ICM7218. The device power dissipation will, therefore, be 640mW rising to about 900mW for all '8''s displayed. **Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.**

Serial Input Drive Considerations (ICM7218A/B)

The control instructions are read from the input bus lines if MODE is high and $\overline{\text{WRITE}}$ low. The instructions occur on 4 lines and are - Decode/no Decode; type of Decode (if desired), $\overline{\text{SHUTDOWN}}$/no Shutdown and DATA COMING/not Coming. After the control instructions have been read (with Data Coming instruction) display data can be written into memory with each following negative going pulse of $\overline{\text{WRITE}}$, MODE being low. After all 8 words or digit memory locations have been written, additional transitions of the state of $\overline{\text{WRITE}}$ are ignored. It is not possible to change one individual digit without refreshing the data for all the other digits. (This can, however, be achieved with the ICM7218C/D/E where the digits are individually addressed.)

Random Access Input Drive Considerations (ICM7218C/D/E)

Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the $\overline{\text{WRITE}}$ pulse. The ICM7218E control instructions are also independent but are on three separate pins (10, 32, 33).

Data can be written into memory on the ICM7218C/D/E by setting up a 3 bit binary code (one of eight) on the digit address inputs (which define the digit where the data is to be written into the memory) and apply a negative going $\overline{\text{WRITE}}$ pulse. For example, it is possible to change only digit 7 without refreshing the data for all the other digits. (However, this cannot be achieved with the ICM7218A/B.)

Supply Capacitor

A 0.1μF capacitor is recommended between V^+ and GROUND to bypass multiplex noise.

SWITCHING WAVEFORMS ICM7218

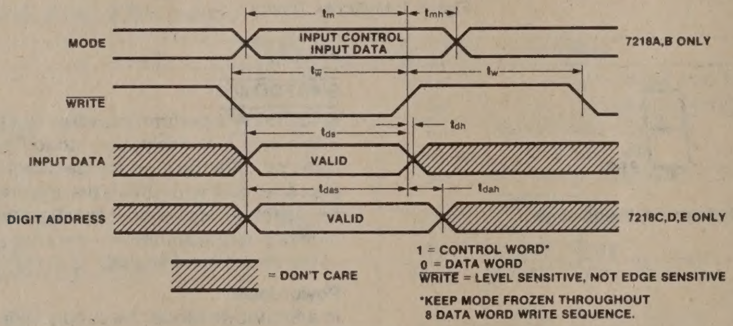

MODE
WRITE
INPUT DATA
DIGIT ADDRESS
tm
tmh
INPUT CONTROL
INPUT DATA
7218A,B ONLY
tw
tw
tds
tdh
VALID
tdas
tdah
VALID
7218C,D,E ONLY
= DON'T CARE
1 = CONTROL WORD*
0 = DATA WORD
WRITE = LEVEL SENSITIVE, NOT EDGE SENSITIVE
*KEEP MODE FROZEN THROUGHOUT
8 DATA WORD WRITE SEQUENCE.

Figure 3

CHIP ADDRESS SEQUENCE ICM7218A and B

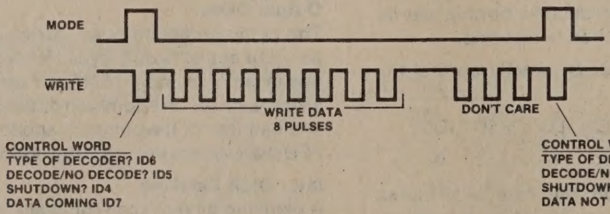

MODE
WRITE
WRITE DATA
8 PULSES
DON'T CARE
CONTROL WORD
TYPE OF DECODER? ID6
DECODE/NO DECODE? ID5
SHUTDOWN? ID4
DATA COMING ID7
CONTROL WORD
TYPE OF DECODER? ID6
DECODE/NO DECODE? ID5
SHUTDOWN? ID4
DATA NOT COMING ID7

Figure 4

CHIP ADDRESS SEQUENCE EXAMPLE ICM7218C/D/E

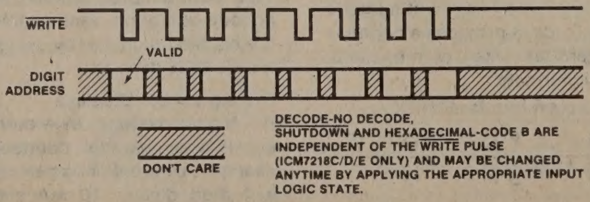
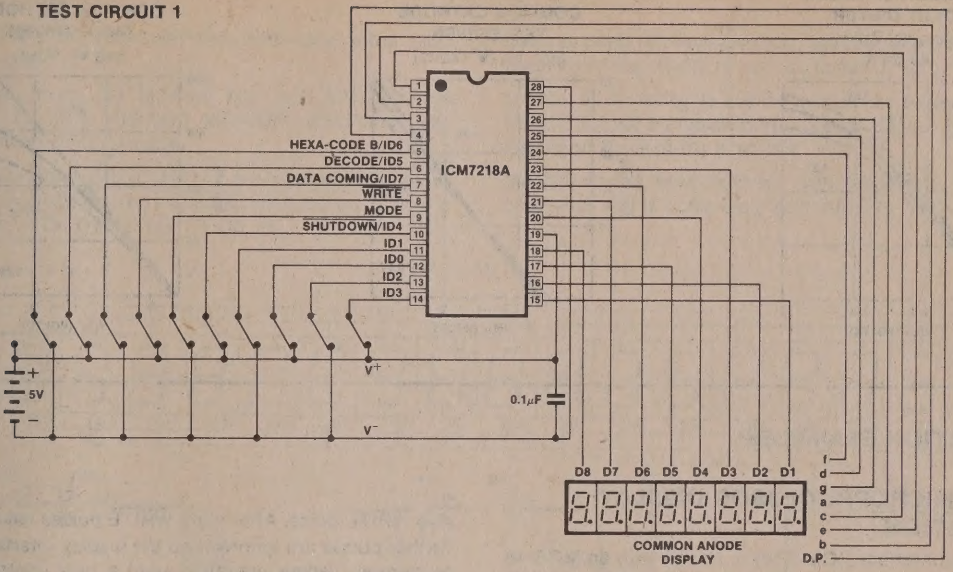

WRITE
VALID
DIGIT ADDRESS
DON'T CARE
DECODE-NO DECODE,
SHUTDOWN AND HEXADECIMAL-CODE B ARE
INDEPENDENT OF THE WRITE PULSE
(ICM7218C/D/E ONLY) AND MAY BE CHANGED
ANYTIME BY APPLYING THE APPROPRIATE INPUT
LOGIC STATE.

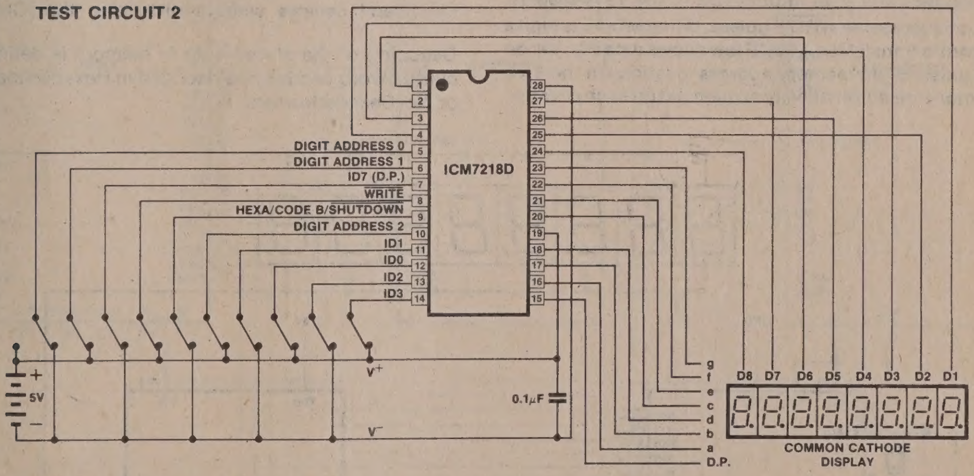
Figure 5

TEST CIRCUITS

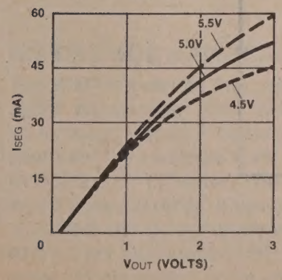
TEST CIRCUIT 1


ICM7218A
HEXA-CODE B/ID6
DECODE/ID5
DATA COMING/ID7
WRITE
MODE
SHUTDOWN/ID4
ID1
ID0
ID2
ID3
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
+
5V
−
V+
V−
0.1μF
D8 D7 D6 D5 D4 D3 D2 D1
f
d
g
a
c
e
b
D.P.
COMMON ANODE DISPLAY

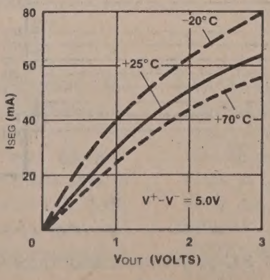
TEST CIRCUIT 2


ICM7218D
DIGIT ADDRESS 0
DIGIT ADDRESS 1
ID7 (D.P.)
WRITE
HEXA/CODE B/SHUTDOWN
DIGIT ADDRESS 2
ID1
ID0
ID2
ID3
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
+
5V
−
V+
V−
0.1μF
g
f
e
c
d
b
a
D.P.
D8 D7 D6 D5 D4 D3 D2 D1
COMMON CATHODE DISPLAY

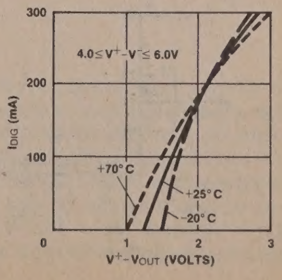
TYPICAL CHARACTERISTICS



COMMON ANODE SEG. DRIVER I_{SEG} vs. V_{OUT} AT 25°C



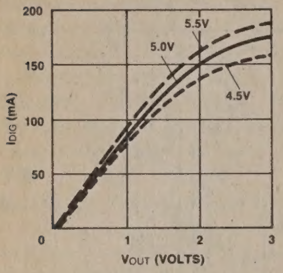
COMMON ANODE SEG. DRIVER I_{SEG} vs. V_{OUT}



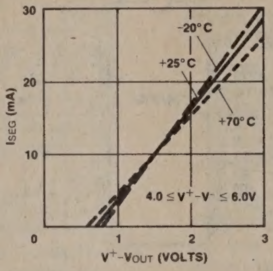
COMMON ANODE DIGIT DRIVER I_{DIG} vs. (V^+-V_{OUT})

TYPICAL CHARACTERISTICS, CONTINUED

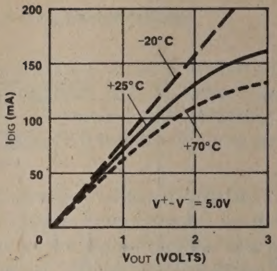
COMMON CATHODE
DIGIT DRIVER
I_{DIG} vs. V_{OUT}
AT 25°C



COMMON CATHODE
SEG. DRIVER
I_{SEG} vs. $(V^+ - V_{OUT})$



COMMON CATHODE
DIGIT DRIVER
I_{DIG} vs. V_{OUT}



APPLICATION EXAMPLES

8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

The display interface (ICM7218) is shown with an MCS-48 family microprocessor. The 8 bit data bus DB0/DB7-ID0/ID7 transfers control and data information to the 7218 display interface on successive $\overline{\text{WRITE}}$ pulses. When MODE is high a control word is transferred. MODE low allows data transfer on a $\overline{\text{WRITE}}$ pulse. Eight memory address locations in the 8 x 8 static memory are automatically sequenced on each successive $\overline{\text{WRITE}}$ pulse. After eight $\overline{\text{WRITE}}$ pulses have occurred, further pulses are ignored and the display interface returns to normal display operation until a new control word is transferred. See Figure 4. This also allows writing to other peripheral devices without disturbing the ICM7218 A/B.

Decoding of the stored data in memory is defined by the control word and may be decoded in Hexadecimal, Code B, or No-Decode formats.

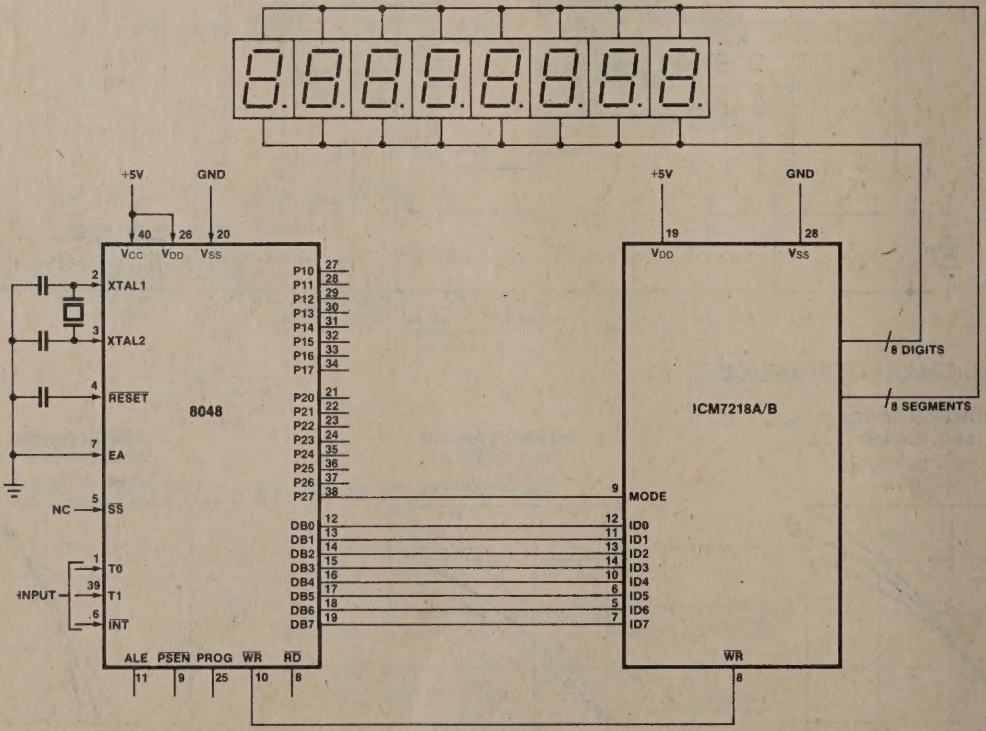

+5V
GND
40
26
20
VCC
VDD
VSS
2
XTAL1
3
XTAL2
4
RESET
7
EA
NC
5
SS
1
T0
INPUT
39
T1
6
INT
8048
P10
P11
P12
P13
P14
P15
P16
P17
P20
P21
P22
P23
P24
P25
P26
P27
27
28
29
30
31
32
33
34
21
22
23
24
35
36
37
38
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
12
13
14
15
16
17
18
19
ALE
PSEN
PROG
WR
RD
11
9
25
10
8
+5V
GND
19
28
VDD
VSS
8 DIGITS
8 SEGMENTS
ICM7218A/B
9
MODE
12
11
13
14
10
6
5
7
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7
WR
8

Figure 6: 8 Digit Microprocessor Display

16 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Both ICM7218's are addressed simultaneously with a 3 bit word, DA2-DA0.

Display data from the MCS-48 I/O bus (DB7-DB0) is transferred to both ICM7218 (ID3-ID0) simultaneously, 4 bits + 4 bits on WRITE enable.

Display digits from both ICM7218's are interleaved to allow adjacent pairs of digits to be loaded sequentially on a single 8 bit data bus, ie D0 D1, D2 D3, D4 D5, etc..

Decimal point information (from the processor, P26-P27) is supplied to the ICM7218 on bus lines ID7 to both devices.

Choice of decoding is available in either Hexadecimal or Code-B format by hardwiring or decoding to a Three Level format on Pin 9 of the ICM7218.

Multiplexing is asynchronous with respect to the microprocessor and is completely performed by the ICM7218.

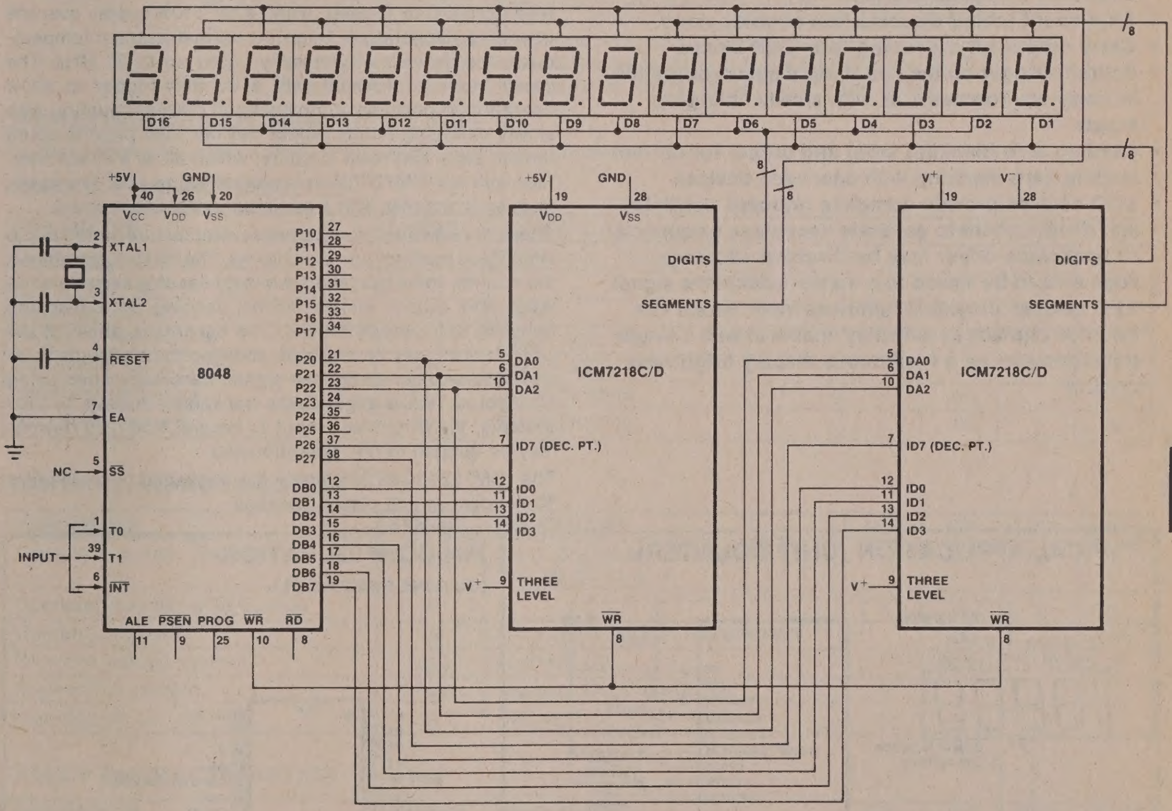

D16
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
8
8
8
8
+5V
GND
40
26
20
VCC
VDD
VSS
2
XTAL1
3
XTAL2
4
RESET
7
EA
5
NC
SS
1
T0
39
INPUT
T1
6
INT
8048
P10
P11
P12
P13
P14
P15
P16
P17
27
28
29
30
31
32
33
34
P20
P21
P22
P23
P24
P25
P26
P27
21
22
23
24
35
36
37
38
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
12
13
14
15
16
17
18
19
ALE
PSEN
PROG
WR
RD
11
9
25
10
8
+5V
GND
19
28
VDD
VSS
DIGITS
SEGMENTS
5
6
10
DA0
DA1
DA2
ICM7218C/D
7
ID7 (DEC. PT.)
12
11
13
14
ID0
ID1
ID2
ID3
V+
9
THREE LEVEL
WR
8
V+
V-
19
28
DIGITS
SEGMENTS
5
6
10
DA0
DA1
DA2
ICM7218C/D
7
ID7 (DEC. PT.)
12
11
13
14
ID0
ID1
ID2
ID3
V+
9
THREE LEVEL
WR
8

Figure 7: 16 Digit Display

NO DECODE APPLICATION

The ICM7218 can be used as a microprocessor based LED status panel driver. The microprocessor selected control word would include "No Decode" and "Data Coming". The computer then outputs word oriented "Ones" and "Zeroes" to indicate on-off states. This data is read into the ICM7218 which in turn directly drives appropriate discrete LEDs. LED indicators can be red or green (8 "segments" x 8 digits = 64 dots ÷ 2 per red or green = 32 channels). With red, yellow and green, 21 channels can be accommodated.

Additional ICM7218's may be bussed and addressed (see Figures 6 and 7) to expand the status panel capacity. Note per figure 4 that after the ICM7218A/B has been read in its data (8 WRITE pulses), it ignores additional information on the data lines. A new control word must be received before the next write sequence can be accommodated. Consequently, by address decoding and WRITE pulse enabling, numerous ICM7218's can be bussed together to allow a large number of indicator channels.

INTERSIL

ICM7224 (LCD)
ICM7225 (LED)
4½ Digit Counter/ Decoder/Drivers

FEATURES

- **High frequency counting - guaranteed 15MHz, typically 25MHz at 5V**
- **Low power operation - less than 100μW quiescent**
- **Store and Reset inputs permit operation as frequency or period counter**
- **True count inhibit disables first counter stage**
- **Carry output for cascading four-digit blocks**
- **Schmitt-trigger on the count input allows operation in noisy environments or with slowly changing inputs**
- **Leading zero blanking input and output for correct leading zero blanking with cascaded devices**
- **LCD devices provide complete onboard oscillator and divider chain to generate backplane frequency, or backplane driver may be disabled allowing segments to be slaved to a master backplane signal**
- **LED devices provide Brightness input which can function digitally as a display enable or with a single potentiometer as a continuous display brightness control**

GENERAL DESCRIPTION

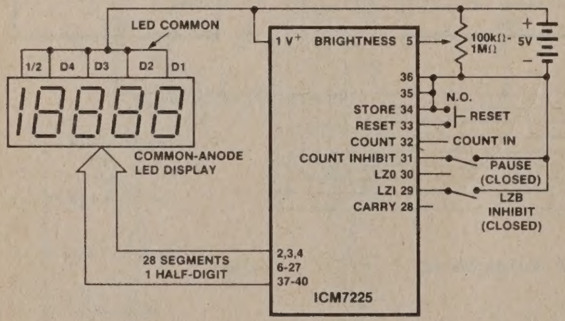
The ICM7224 and ICM7225 devices constitute a family of high-performance CMOS 4 1/2-digit counters, including decoders, output latches, display drivers, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15 MHz, using a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The count input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry, which allow a direct interface with the ICM7207/A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The carry output allows the counter to be cascaded, while the leading zero blanking input and output allows correct leading zero blanking between four-decade blocks. The backplane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display. In LED systems, the brightness input to several ICM7225 devices may be ganged to one potentiometer.

The ICM7224/ICM7225 family are packaged in a standard 40-pin dual-in-line plastic package.

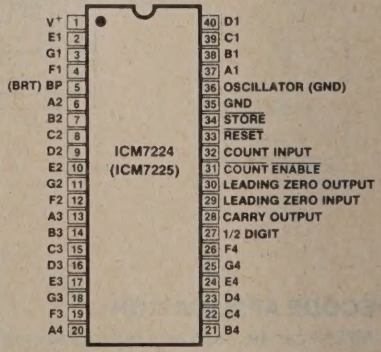
TYPICAL APPLICATION (UNIT COUNTER)


LED COMMON
1/2
D4
D3
D2
D1
COMMON-ANODE LED DISPLAY
28 SEGMENTS 1 HALF-DIGIT
2,3,4
6-27
37-40
ICM7225
1 V+
BRIGHTNESS 5
100kΩ- 1MΩ
5V
36
35
STORE 34
RESET 33
COUNT 32
COUNT INHIBIT 31
LZ0 30
LZI 29
CARRY 28
N.O.
RESET
COUNT IN
PAUSE (CLOSED)
LZB INHIBIT (CLOSED)

ORDERING INFORMATION

	ORDER PART NUMBER	COUNT OPTION
LCD DISPLAY	ICM7224 IPL ICM7224A IPL	19999 15959
LED DISPLAY	ICM7225 IPL ICM7225A IPL	19999 15959

PIN CONFIGURATION
(OUTLINE DRAWING PL)


ICM7224
(ICM7225)
V+ 1
E1 2
G1 3
F1 4
(BRT) BP 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
40 D1
39 C1
38 B1
37 A1
36 OSCILLATOR (GND)
35 GND
34 STORE
33 RESET
32 COUNT INPUT
31 COUNT ENABLE
30 LEADING ZERO OUTPUT
29 LEADING ZERO INPUT
28 CARRY OUTPUT
27 1/2 DIGIT
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	0.5 W @ 70°C
Supply Voltage (V^+)	6.5V
Input Voltage (Any Terminal) (Note 2)	V^+ +0.3V, −0.3V
Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−55°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/ICM7225 be turned on first.

OPERATING CHARACTERISTICS TABLE 2

(All Parameters measured with $V^+ = 5V$ unless otherwise indicated)

ICM7224 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current	I_{op}	Test circuit, Display blank		10	50	μA
Operating supply voltage range	V^+		3	5	6	V
Oscillator input current	I_{OSCI}	Pin 36		±2	±10	μA
Segment rise/fall time	t_{rfs}	C_{load} = 200pF		0.5		μs
Backplane rise/fall time	t_{rfb}	C_{load} = 5000pF		1.5		
Oscillator frequency	f_{osc}	Pin 36 Floating		16		KHz
Backplane frequency	f_{bp}	Pin 36 Floating		125		Hz

ICM7225 CHARACTERISTICS

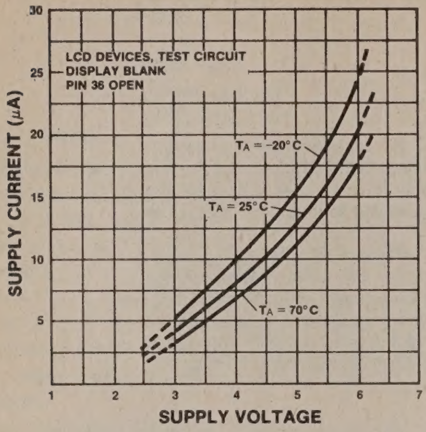
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current display off	I_{OPQ}	Pin 5 (Brightness) at GROUND Pins 29, 31-34 at V^+		10	50	μA
Operating supply voltage range	V^+		4	5	6	V
Operating current	I_{OP}	Pin 5 at V^+, Display 18888		200		mA
Segment leakage current	I_{SLK}	Segment Off		±0.01	±1	μA
Segment on current	I_{SEG}	Segment On, Vout = + 3V	5	8		mA
Half digit on current	I_H	Half digit on, Vout = + 3V	10	16		

FAMILY CHARACTERISTICS

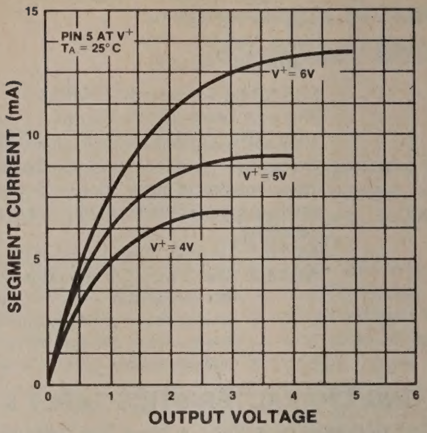
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Currents	I_P	Pins 29, 31, 33, 34 Vout = V^+- 3V		10		μA
Input High Voltage	V_{IH}	Pins 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pins 29, 31, 33, 34			1	
Count Input Threshold	V_{CT}			2		
Count Input Hysteresis	V_{CH}			0.5		
Output High Current	I_{OH}	Carry Pin 28 Leading Zero Out Pin 30 Vout = V^+ −3V	350	500		μA
Output Low Current	I_{OL}	Carry Pin 28 Leading Zero Out Pin 30 Vout = +3V	350	500		
Count Frequency	f_{count}	4.5V < V^+ < 6V	0	DC-25	15	MHz
Store, Reset Minimum Pulse Width	t_S,t_R		3			μs

TYPICAL CHARACTERISTICS

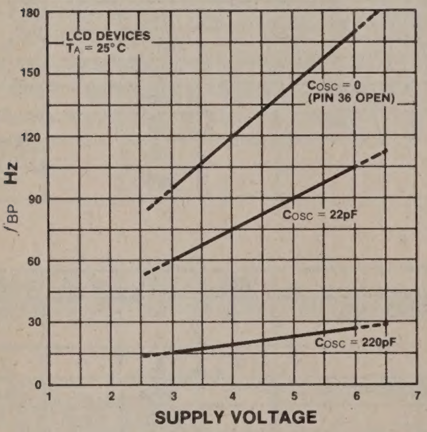
7224 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



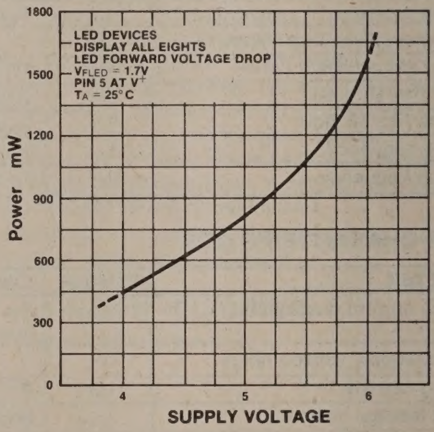
7225 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



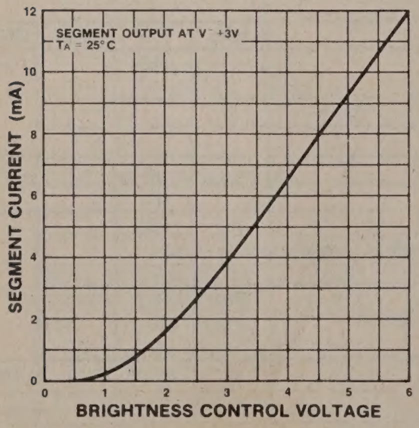
7224 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



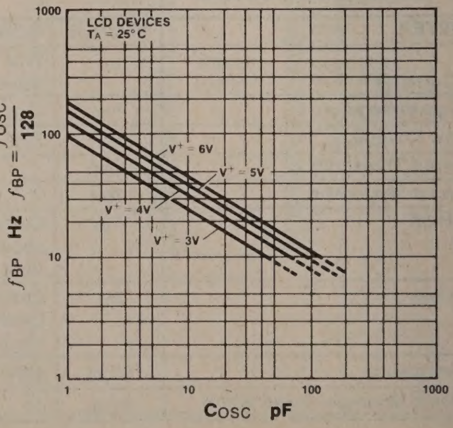
7225 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



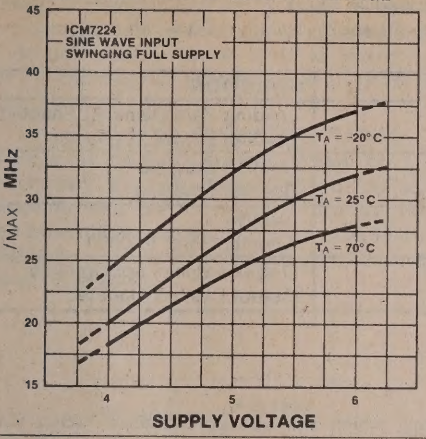
7225 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



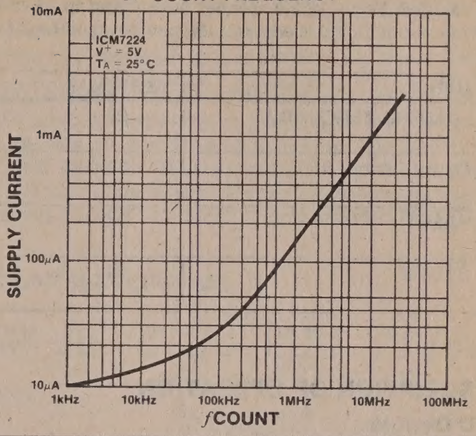
BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR C_{OSC}



MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE

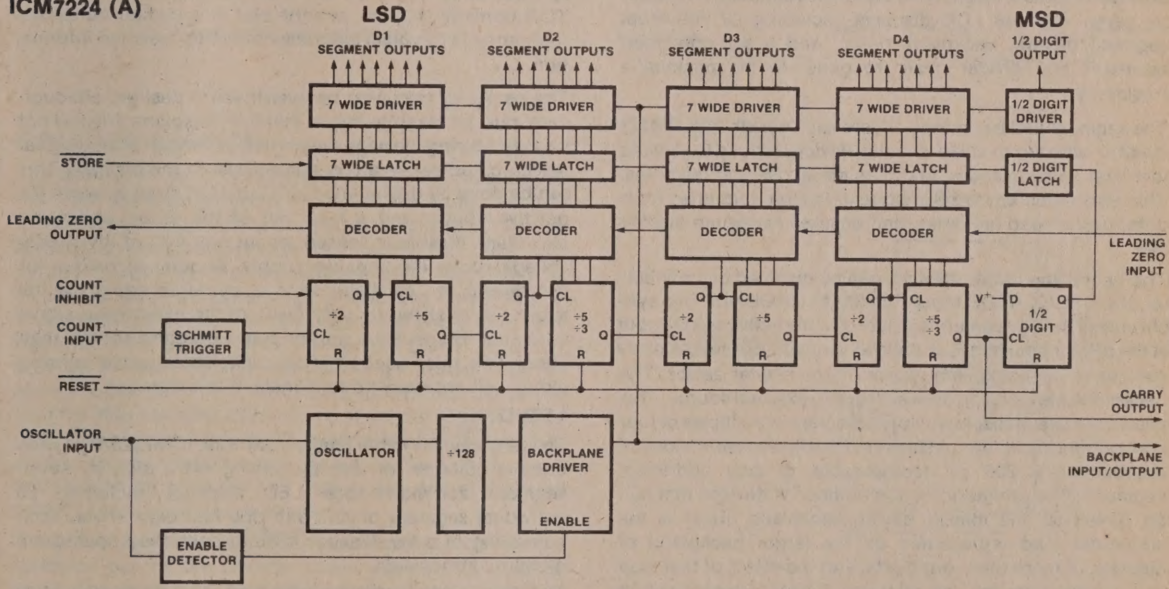


SUPPLY CURRENT AS A FUNCTION OF COUNT FREQUENCY

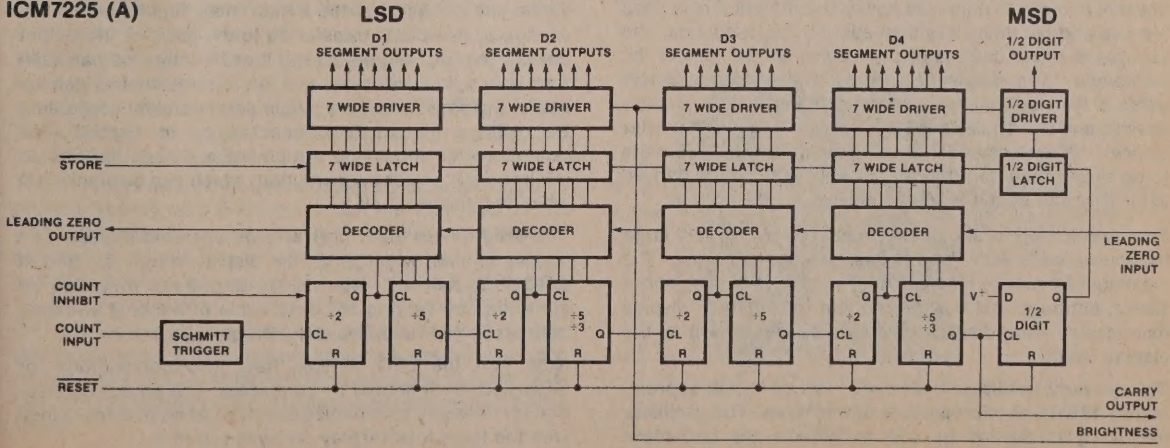


BLOCK DIAGRAMS

ICM7224 (A)


LSD
MSD
D1 SEGMENT OUTPUTS
D2 SEGMENT OUTPUTS
D3 SEGMENT OUTPUTS
D4 SEGMENT OUTPUTS
1/2 DIGIT OUTPUT
7 WIDE DRIVER
1/2 DIGIT DRIVER
STORE
7 WIDE LATCH
1/2 DIGIT LATCH
LEADING ZERO OUTPUT
DECODER
LEADING ZERO INPUT
COUNT INHIBIT
COUNT INPUT
SCHMITT TRIGGER
Q
CL
÷2
÷5
÷5 ÷3
R
V^+
D
1/2 DIGIT
RESET
CARRY OUTPUT
OSCILLATOR INPUT
OSCILLATOR
÷128
BACKPLANE DRIVER
ENABLE
BACKPLANE INPUT/OUTPUT
ENABLE DETECTOR

ICM7225 (A)


LSD
MSD
D1 SEGMENT OUTPUTS
D2 SEGMENT OUTPUTS
D3 SEGMENT OUTPUTS
D4 SEGMENT OUTPUTS
1/2 DIGIT OUTPUT
7 WIDE DRIVER
1/2 DIGIT DRIVER
STORE
7 WIDE LATCH
1/2 DIGIT LATCH
LEADING ZERO OUTPUT
DECODER
LEADING ZERO INPUT
COUNT INHIBIT
COUNT INPUT
SCHMITT TRIGGER
Q
CL
÷2
÷5
÷5 ÷3
R
V^+
D
1/2 DIGIT
RESET
CARRY OUTPUT
BRIGHTNESS

CONTROL INPUT DEFINITIONS

In this table, V and GROUND are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 2. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	VOLTAGE	FUNCTION
LEADING ZERO INPUT	29	V^+ or Floating GROUND	Leading Zero Blanking Enabled Leading Zeroes Displayed
Count Inhibit	31	V^+ or Floating GROUND	Counter Enabled Counter Disabled
$\overline{\text{RESET}}$	33	V^+ or Floating GROUND	Inactive Counter Reset to 0000
$\overline{\text{STORE}}$	34	V^+ or Floating GROUND	Output Latches not Updated Output Latches Updated

DESCRIPTION OF OPERATION

LCD Devices

The LCD devices in the family (ICM7224 and ICM7224A) provide outputs suitable for driving conventional 4-1/2 digit by seven segment LCD displays, including 29 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCILLATOR input (pin 36) to GROUND. This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200 pF (comparable to one additional segment). The limitation on the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 16KHz, at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor to the OSCILLATOR terminal (pin 36); see the plot of oscillator/backplane frequency in "Typical Characteristics" for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Devices

The LED devices in the family (ICM7225, ICM7225A) provide outputs suitable for directly driving 4-1/2 digit by seven segment common-anode LED displays, including 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Fig (3). The potentiometer should be a high value (100kΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

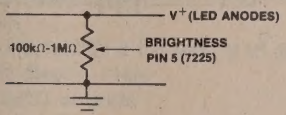
The BRighTness input may also be operated digitally as a display enable; when at V+, the display is fully on, and at GROUND, fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the BRighTness input.

Note that the LED devices have two connections for GROUND; both should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (−15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED}) \text{ x } (I_{SEG}) \text{ x } (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.



V+(LED ANODES)
100kΩ-1MΩ
BRIGHTNESS
PIN 5 (7225)

Figure 3: Brightness Control

COUNTER SECTION

The devices in the ICM7224/ICM7225 family implement a four digit ripple carry resetable counter, including a Schmitt trigger on the COUNT INPUT and a CARRY OUTPUT. Also included is an extra D-type flip-flop, clocked by the CARRY signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the COUNT INPUT, while the CARRY OUTPUT provides a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{\text{RESET}}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half digit is set, and subsequent CARRY outputs will not be affected.

A negative level at the $\overline{\text{COUNT ENABLE}}$ input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the count input, which prevents false counts that can result from using a normal logic gate to prevent counting.

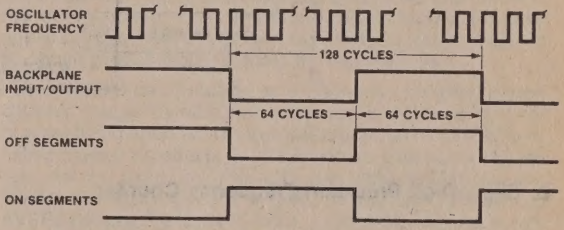
Each decade of counter drives directly into a four-to-seven decoder which develops the seven segment output code. The output data is latched at the driver; when the $\overline{\text{STORE}}$ pin is low, these latches are updated, and when high or floating, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the LEADING ZERO INPUT is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes; when low, or the half digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The LEADING ZERO OUTPUT is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the LEADING ZERO INPUT is at a positive level and the half digit is not set.

For example, in an eight-decade counter with overflow using two ICM7224/ICM7225 devices, the LEADING ZERO OUTPUT of the high order digit device would be connected to the LEADING ZERO INPUT of the low order digit device. This will assure correct leading zero blanking for all eight digits.

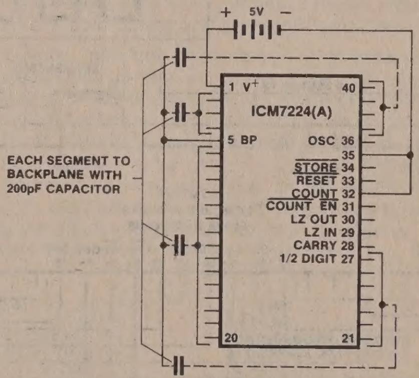
The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$, $\overline{\text{COUNT ENABLE}}$, and LEADING ZERO INPUTS are provided with pullup devices, so that they may be left open when a positive level is desired. The CARRY and LEADING ZERO OUTPUTS are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7224 or ICM7225 devices in four digit blocks.

DISPLAY WAVEFORMS



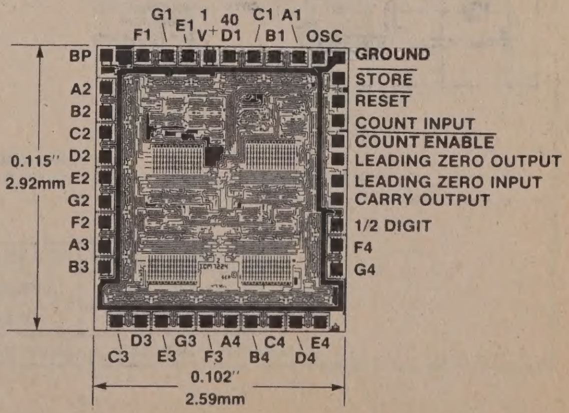
OSCILLATOR FREQUENCY
128 CYCLES
BACKPLANE INPUT/OUTPUT
64 CYCLES
64 CYCLES
OFF SEGMENTS
ON SEGMENTS

TEST CIRCUIT



+ 5V −
1 V+
40
ICM7224(A)
5 BP
OSC 36
35
STORE 34
RESET 33
COUNT 32
COUNT EN 31
LZ OUT 30
LZ IN 29
CARRY 28
1/2 DIGIT 27
20
21
EACH SEGMENT TO BACKPLANE WITH 200pF CAPACITOR

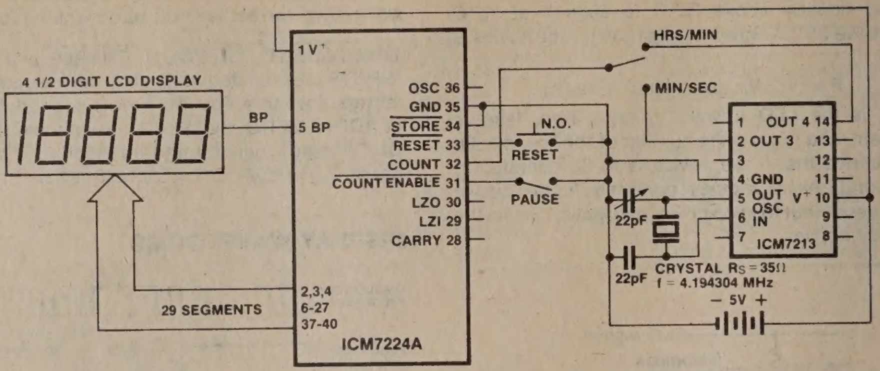
CHIP TOPOGRAPHY



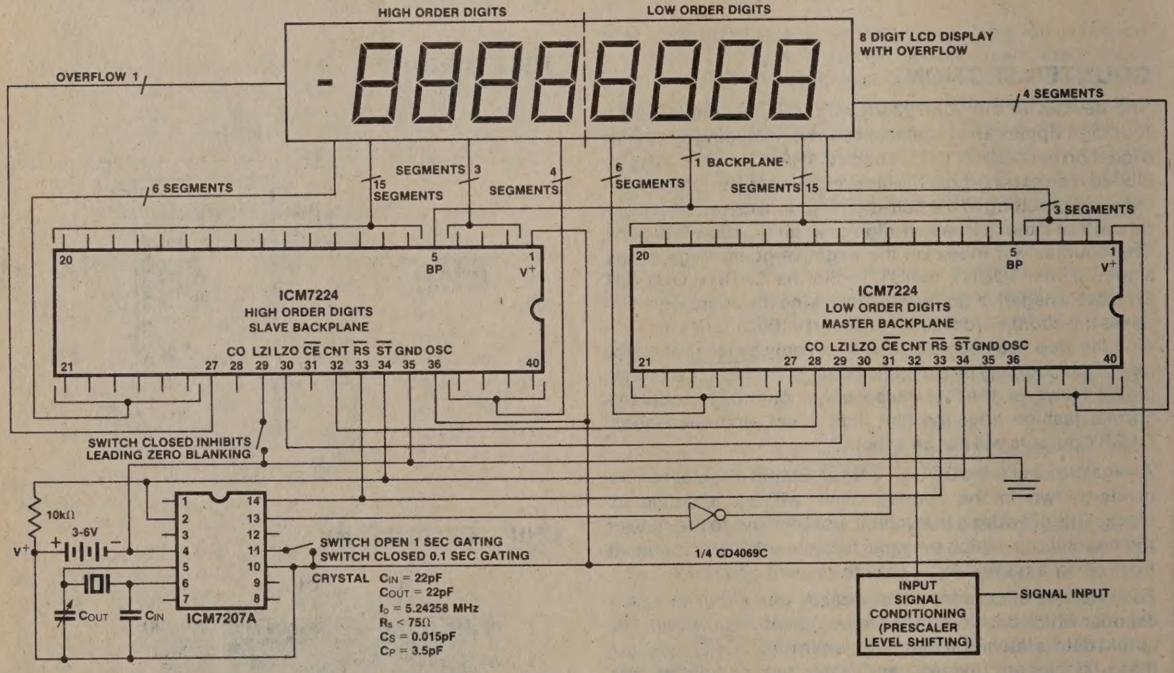
G1
E1
1
40
C1
A1
F1
V+
D1
B1
OSC
BP
A2
B2
C2
D2
E2
G2
F2
A3
B3
0.115″
2.92mm
GROUND
STORE
RESET
COUNT INPUT
COUNT ENABLE
LEADING ZERO OUTPUT
LEADING ZERO INPUT
CARRY OUTPUT
1/2 DIGIT
F4
G4
D3
G3
A4
C4
E4
C3
E3
F3
B4
D4
0.102″
2.59mm

APPLICATIONS

1. Two-Hour Precision Timer


4 1/2 DIGIT LCD DISPLAY
BP
1 V+
5 BP
OSC 36
GND 35
STORE 34
RESET 33
COUNT 32
COUNT ENABLE 31
LZO 30
LZI 29
CARRY 28
2,3,4
6-27
37-40
29 SEGMENTS
ICM7224A
HRS/MIN
MIN/SEC
N.O.
RESET
PAUSE
22pF
22pF
1 OUT 4 14
2 OUT 3 13
3 12
4 GND 11
5 OUT V+ 10
OSC
6 IN 9
7 8
ICM7213
CRYSTAL Rs = 35Ω
f = 4.194304 MHz
− 5V +

2. Eight-Digit Precision Frequency Counter


HIGH ORDER DIGITS
LOW ORDER DIGITS
8 DIGIT LCD DISPLAY
WITH OVERFLOW
OVERFLOW 1
4 SEGMENTS
6 SEGMENTS
SEGMENTS 3
15 SEGMENTS
4 SEGMENTS
6 SEGMENTS
1 BACKPLANE
SEGMENTS 15
3 SEGMENTS
20
5 BP
1 V+
ICM7224
HIGH ORDER DIGITS
SLAVE BACKPLANE
CO LZI LZO CE CNT RS ST GND OSC
21
27 28 29 30 31 32 33 34 35 36
40
20
5 BP
1 V+
ICM7224
LOW ORDER DIGITS
MASTER BACKPLANE
CO LZI LZO CE CNT RS ST GND OSC
21
27 28 29 30 31 32 33 34 35 36
40
SWITCH CLOSED INHIBITS
LEADING ZERO BLANKING
10kΩ
3-6V
V+
1 14
2 13
3 12
4 11
5 10
6 9
7 8
ICM7207A
COUT
CIN
SWITCH OPEN 1 SEC GATING
SWITCH CLOSED 0.1 SEC GATING
CRYSTAL CIN = 22pF
COUT = 22pF
fo = 5.24258 MHz
Rs < 75Ω
Cs = 0.015pF
CP = 3.5pF
1/4 CD4069C
INPUT SIGNAL CONDITIONING (PRESCALER LEVEL SHIFTING)
SIGNAL INPUT

ICM7226A/B
10MHz Universal Counter System
ICM7226A Drives Common Anode LED's
ICM7226B Drives Common Cathode LED's

FEATURES

- CMOS design for very low power
- Output drivers directly drive both digits and segments of large 8 digit LED displays. Both common anode and common cathode versions are available
- Measures frequencies from DC to 10 MHz; periods from 0.5μs to 10s
- Stable high frequency oscillator uses either 1MHz or 10MHz crystal
- Control signals available for gating of prescalers and prescaler display logic
- Multiplexed BCD outputs

APPLICATIONS

- Frequency Counter
- Period Counter
- Unit Counter
- Frequency Ratio Counter
- Time Interval Counter

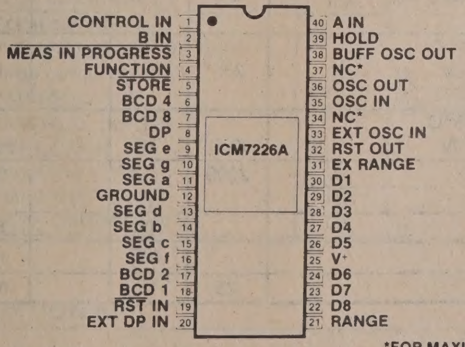
GENERAL DESCRIPTION

The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexer, and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in FREQUENCY and UNIT COUNTER modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

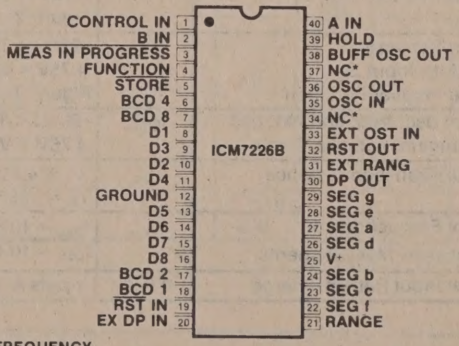
The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or a totalizing counter. The devices require either a 10MHz or 1MHz crystal timebase, or if desired an external timebase can also be used. For PERIOD and TIME INTERVAL, the 10MHz timebase gives a 0.1μsec resolution. In PERIOD AVERAGE and TIME INTERVAL AVERAGE, the resolution can be in the nanosecond range. In the FREQUENCY mode, the user can select accumulation time of 10ms, 100ms, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz. There is a 0.2s interval between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency display in kHz and time in μs. The display is multiplexed at a 500Hz rate with a 12.5% duty cycle for each digit. The ICM7226A is designed for common anode display with typical peak segment currents of 25mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the DISPLAY OFF mode, both digit drivers & segment drivers are turned off, allowing the display to be used for other functions.

PIN CONFIGURATION


CONTROL IN 1
B IN 2
MEAS IN PROGRESS 3
FUNCTION 4
STORE 5
BCD 4 6
BCD 8 7
DP 8
SEG e 9
SEG g 10
SEG a 11
GROUND 12
SEG d 13
SEG b 14
SEG c 15
SEG f 16
BCD 2 17
BCD 1 18
RST IN 19
EXT DP IN 20
ICM7226A
40 A IN
39 HOLD
38 BUFF OSC OUT
37 NC*
36 OSC OUT
35 OSC IN
34 NC*
33 EXT OSC IN
32 RST OUT
31 EX RANGE
30 D1
29 D2
28 D3
27 D4
26 D5
25 V+
24 D6
23 D7
22 D8
21 RANGE

(OUTLINE DRAWING DL)


CONTROL IN 1
B IN 2
MEAS IN PROGRESS 3
FUNCTION 4
STORE 5
BCD 4 6
BCD 8 7
D1 8
D3 9
D2 10
D4 11
GROUND 12
D5 13
D6 14
D7 15
D8 16
BCD 2 17
BCD 1 18
RST IN 19
EX DP IN 20
ICM7226B
40 A IN
39 HOLD
38 BUFF OSC OUT
37 NC*
36 OSC OUT
35 OSC IN
34 NC*
33 EXT OST IN
32 RST OUT
31 EXT RANG
30 DP OUT
29 SEG g
28 SEG e
27 SEG a
26 SEG d
25 V+
24 SEG b
23 SEG c
22 SEG f
21 RANGE

(OUTLINE DRAWING PL)

*FOR MAXIMUM FREQUENCY STABILITY, CONNECT TO V+ OR GROUND

ORDERING INFORMATION

DISPLAY	DEVICE	PACKAGE	ORDER NUMBER
Common Anode	ICM7226A	Ceramic	ICM7226A IDL
Common Cathode	ICM7226B	Plastic	ICM7226B IPL

NOTE: An evaluation kit is available for these devices — order ICM7226AEV/KIT.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage	6.5V
Maximum Digit Output Current	400mA
Maximum Segment Output Current	60mA
*Voltage on any Input or Output Terminal	Not to exceed V^+ or GND by more than +0.3 volts
Maximum Power Dissipation at 70°C (Note 1)	1.0W (ICM7226A) 0.5W (ICM7226B)
Maximum Operating Temperature Range	-20°C to +85°C
Maximum Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

***NOTE:** Destructive latchup may occur if input signals are applied before the power supply is established or if inputs or outputs are forced to voltages exceeding V^+ or ground by 0.3V.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Supply Current	I^+_{OP}	Display Off Unused inputs to GROUND		2	5	mA
Supply Voltage Range	V_{SUPP}	$-20°C < T_A < 85°C$ Input A, Input B Frequency at f_{MAX}	4.75		6.0	V
Maximum Guaranteed Frequency Input A, Pin 40	$f_{A(max)}$	$-20°C < T_A < 85°C$ $4.75V < V^+ < 6.0V$ Figure 1 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5	 14		MHz
Maximum Frequency Input B, Pin 2	$f_{B(max)}$	$-20°C < T_A < 85°C$ $4.75V < V^+ < 6.0V$ Figure 2	2.5			
Minimum Separation Input A to Input B Time Interval Function		$-20°C < T_A < 85°C$ $4.75V < V^+ < 6.0V$ Figure 3	250			ns
Maximum osc. freq. and ext. osc. freq. (minimum ext. osc. freq.)	f_{OSC}	$-20°C < T_A < 85°C$ $4.75V < V^+ < 6.0V$	(0.1)	10		MHz
Oscillator Transconductance	g_m	$V^+ = 4.75V$ $T_A = +85°C$	2000			μS
Multiplex Frequency	f_{mux}	$f_{osc} = 10$ MHz		500		Hz
Time Between Measurements		$f_{osc} = 10$ MHz		200		ms
Minimum Input Rate of Charge	dV_{in}/dt	Inputs A, B	25	15		mV/μs

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.0V$, test circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
INPUT VOLTAGES PINS 2,19,33,39,40 input low voltage	V_{IL}	$-20°C < T_A < +70°C$	1.0			V
input high voltage	V_{IH}				3.5	V
PIN 2, 39, 40 INPUT LEAKAGE, A, B	I_{ILK}				20	μA
PIN 33 input low voltage	V_{IL}	$-20°C < T_A < 70°C$	0.8			V
input high voltage	V_{IH}				2.0	V
Input resistance to V^+ PINS 19,33	R_{IN}	$V_{IN} = V^+ - 1.0V$.	100	400		kΩ
Input resistance to GROUND PIN 31	R_{IN}	$V_{IN} = +1.0V$	50	100		kΩ
Output Current PINS 3,5,6,7,17,18,32,38	I_{OL}	$V_{OL} = +0.4V$	400			μA
PINS 5,6,7,17,18,32	I_{OH}	$V_{OH} = +0.4V$	100			μA
PINS 3,38	I_{OH}	$V_{OH} = V^+ - 0.8V$	265			μA
ICM7226A PINS 22,23,24,26,27,28,29,30 DIGIT DRIVER high output current	I_{OH}	$V_O = V^+ - 2.0V$	150	180		mA
low output current	I_{OL}	$V_O = +1.0V$		−0.3		mA
SEGMENT DRIVER PINS 8,9,10,11,13,14,15,16 low output current	I_{OL}	$V_O = +1.5V$	25	35		mA
high output current	I_{OH}	$V_O = V^+ - 1.0V$		100		μA
MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage	V_{IL}				0.8	V
input high voltage	V_{IH}		2.0			V
input resistance to GROUND	R_{IN}	$V_{IN} = +1.0V$	50	100		kΩ
ICM7226B DIGIT DRIVER PINS 8,9,10,11,13,14,15,16 low output current	I_{OL}	$V_O = +1.0V$	50	75		mA
high output current	I_{OH}	$V_O = V^+ - 2.5V$		100		μA
SEGMENT DRIVER PINS 22,23,24,26,27,28,29,30 high output current	I_{OH}	$V_O = V^+ - 2.0V$	10	15		mA
leakage current	I_L	V_O = GROUND			10	μA
MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage	V_{IL}				$V^+ - 2.0$	V
input high voltage	V_{IH}		$V^+ - 0.8$			V
input resistance to V^+	R_{IN}	$V_{IN} = V^+ - 1.0V$	200	360		kΩ

EVALUATION KIT

An evaluation kit is available for the ICM7226. It includes all the components necessary to assemble and evaluate a universal frequency/period counter based on the ICM7226. With the help of this kit, an engineer or technician can have the ICM7226 "up-and-running" in less than an hour. Specifically, the kit contains an ICM7226AIDL, a 10MHz quartz crystal, eight each 7-segment .3" leds, PC board, resistors, capacitors, diodes, switches and IC socket. Order # ICM7226AEV/KIT.

TIME INTERVAL MEASUREMENT

The ICM7226 can be used to accurately measure the time interval between two events. With a 10MHz timebase crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

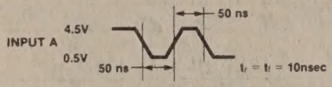

50 ns
4.5V
INPUT A
0.5V
50 ns
$t_r = t_f = 10nsec$

Figure 1: Waveform for Guaranteed Minimum F_{AMAX} Function = Frequency, Frequency Ratio, Unit Counter.

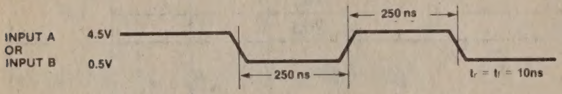
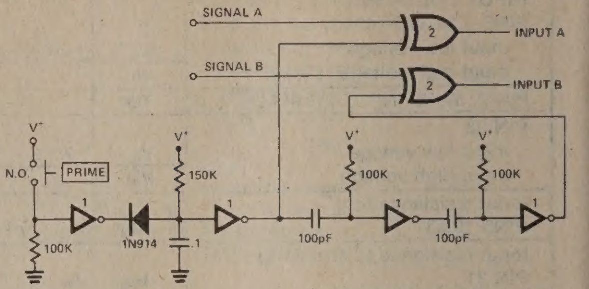

250 ns
INPUT A
OR
INPUT B
4.5V
0.5V
250 ns
$t_r = t_f = 10ns$

Figure 2: Waveform for Guaranteed Minimum f_{BMAX} and f_{AMAX} for Function = Period and Time Interval.

When in the time interval mode and measuring a single event, the ICM7226 must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A, followed by a negative going edge on Channel B to start the measurement interval. The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

This can easily be accomplished with the following circuit, Figure 3b:


SIGNAL A
2
INPUT A
SIGNAL B
2
INPUT B
V+
V+
V+
V+
N.O.
PRIME
150K
100K
100K
1
1
1
1
100K
1N914
.1
100pF
100pF

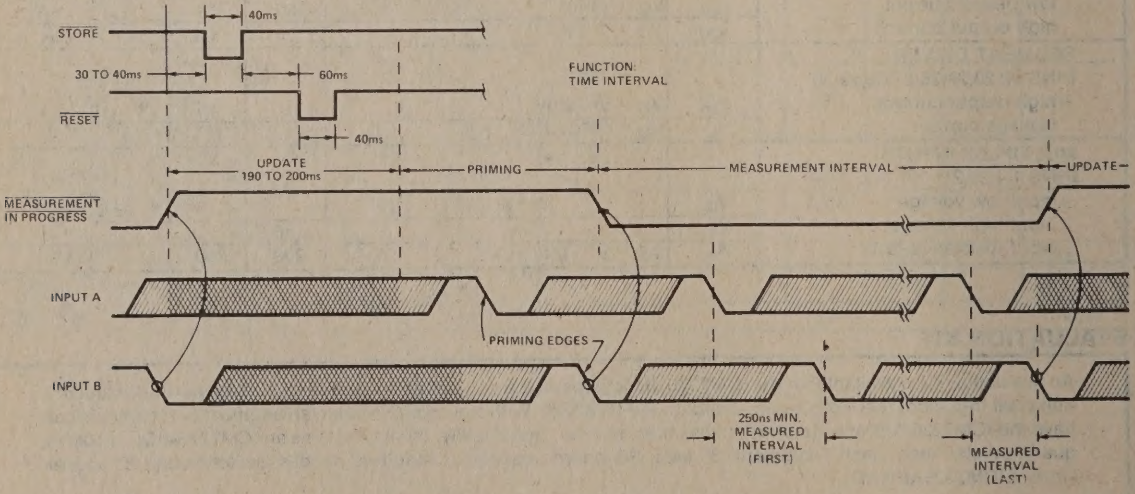
Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

Figure 3b: Priming Circuit, Signal A & B High or Low

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7226, as it is done automatically the first time the input signal changes states.

During any time interval measurement cycle, the ICM7226 requires 200ms following B going low to update the internal logic. A new measurement cycle will not take place until completion of this internal update time.


40ms
STORE
30 TO 40ms
60ms
FUNCTION:
TIME INTERVAL
RESET
40ms
UPDATE
190 TO 200ms
PRIMING
MEASUREMENT INTERVAL
UPDATE
MEASUREMENT
IN PROGRESS
INPUT A
PRIMING EDGES
INPUT B
250ns MIN.
MEASURED
INTERVAL
(FIRST)
MEASURED
INTERVAL
(LAST)

NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

Figure 3a: Waveforms in Time Interval Mode.

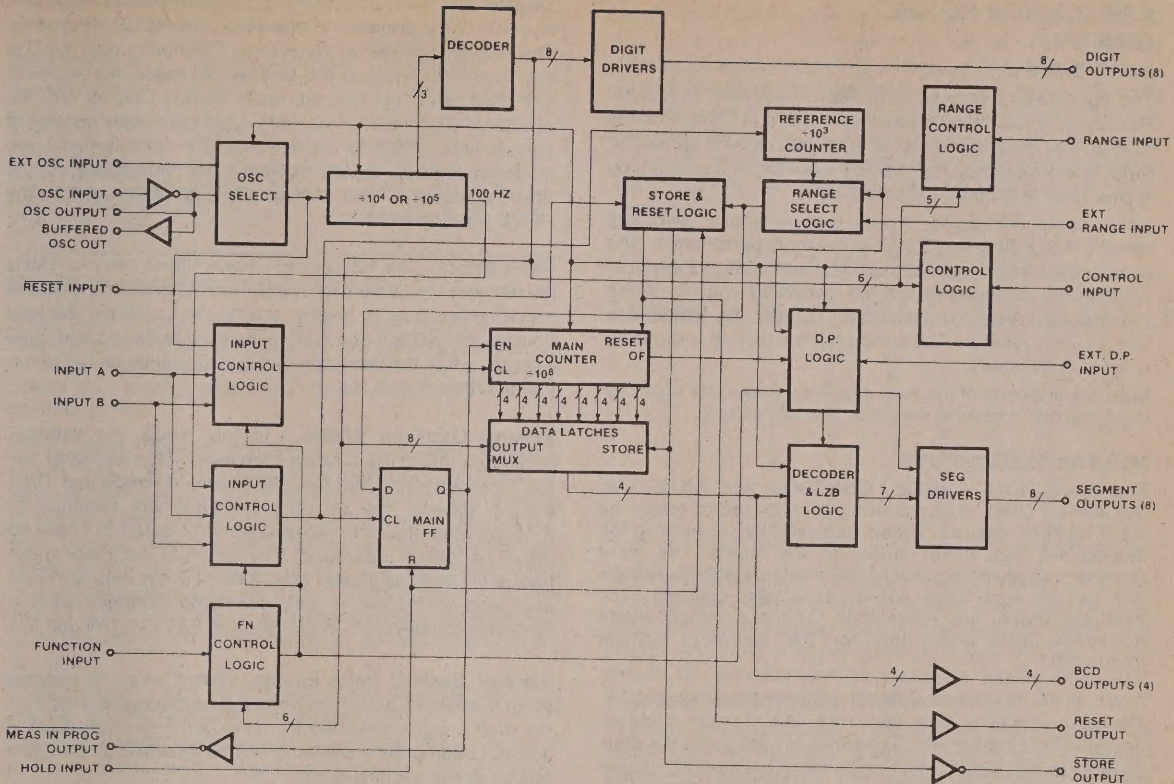

DECODER
DIGIT DRIVERS
8
3
DIGIT OUTPUTS (8)
REFERENCE ÷10³ COUNTER
RANGE CONTROL LOGIC
RANGE INPUT
EXT OSC INPUT
OSC INPUT
OSC OUTPUT
BUFFERED OSC OUT
OSC SELECT
÷10⁴ OR ÷10⁵
100 HZ
STORE & RESET LOGIC
RANGE SELECT LOGIC
5
EXT RANGE INPUT
RESET INPUT
6
CONTROL LOGIC
CONTROL INPUT
INPUT A
INPUT B
INPUT CONTROL LOGIC
EN
CL
MAIN COUNTER ÷10⁸
RESET
OF
D.P. LOGIC
EXT. D.P. INPUT
4
DATA LATCHES
OUTPUT MUX
STORE
D
Q
CL
MAIN FF
R
INPUT CONTROL LOGIC
DECODER & LZB LOGIC
7
SEG DRIVERS
SEGMENT OUTPUTS (8)
FN CONTROL LOGIC
FUNCTION INPUT
BCD OUTPUTS (4)
RESET OUTPUT
MEAS IN PROG OUTPUT
HOLD INPUT
STORE OUTPUT

Figure 4: Block Diagram

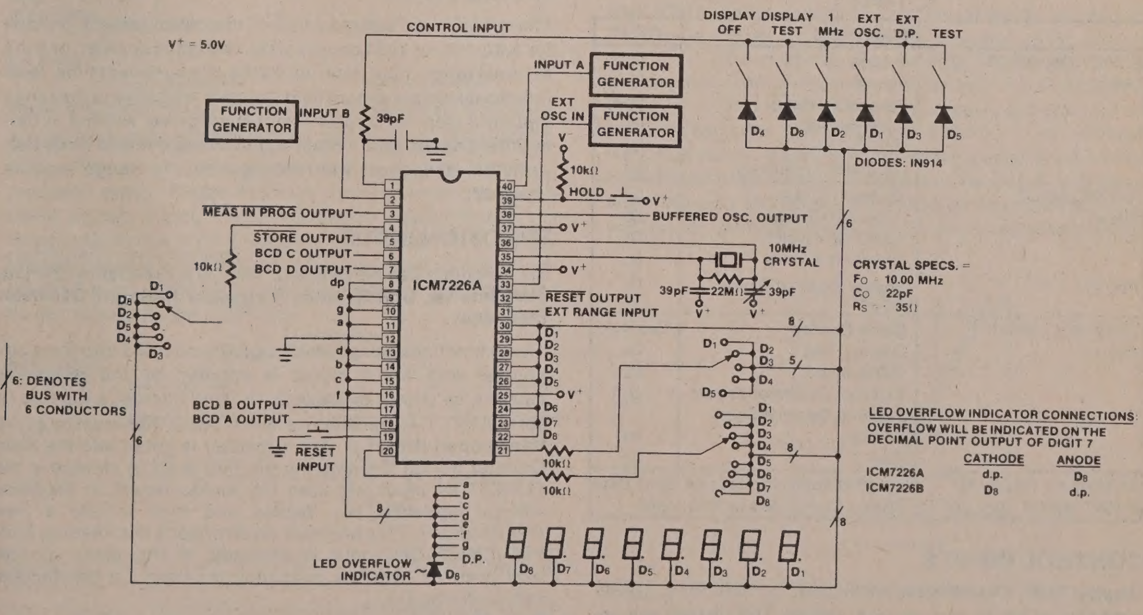

CONTROL INPUT
DISPLAY OFF
DISPLAY TEST
1 MHz
EXT OSC.
EXT D.P.
TEST
V⁺ = 5.0V
INPUT A
FUNCTION GENERATOR
FUNCTION GENERATOR
INPUT B
39pF
EXT OSC IN
FUNCTION GENERATOR
V⁺
10kΩ
HOLD
D₄ D₈ D₂ D₁ D₃ D₅
DIODES: IN914
MEAS IN PROG OUTPUT
BUFFERED OSC. OUTPUT
STORE OUTPUT
BCD C OUTPUT
BCD D OUTPUT
10kΩ
dp
e
g
a
d
b
c
f
ICM7226A
10MHz CRYSTAL
22MΩ
39pF
39pF
RESET OUTPUT
EXT RANGE INPUT
CRYSTAL SPECS. =
Fo = 10.00 MHz
Co = 22pF
Rs = 35Ω
6: DENOTES BUS WITH 6 CONDUCTORS
BCD B OUTPUT
BCD A OUTPUT
RESET INPUT
10kΩ
10kΩ
LED OVERFLOW INDICATOR CONNECTIONS:
OVERFLOW WILL BE INDICATED ON THE DECIMAL POINT OUTPUT OF DIGIT 7
CATHODE
ANODE
ICM7226A d.p. D₈
ICM7226B D₈ d.p.
LED OVERFLOW INDICATOR
D.P.
D₈ D₇ D₆ D₅ D₄ D₃ D₂ D₁

Figure 5: Test Circuit

APPLICATION NOTES

GENERAL

INPUTS A & B

The signal to be measured is applied to Input A in Frequency, Period, Unit Counter, Frequency Ratio and Time Interval modes. The other input signal to be measured is applied to Input B in Frequency Ratio and Time Interval. f_A should be higher than f_B during Frequency Ratio.

Both inputs are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$. For optimum performance, the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply by more than 0.3V otherwise, the circuit may be damaged.

MULTIPLEXED INPUTS

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μsec). The multiplex inputs are active high for the common anode ICM7226A, and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10k resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

TABLE 1

	FUNCTION	DIGIT
FUNCTION INPUT PIN 4	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT PIN 21	.01 Sec/1 Cycle	D_1
	.1 Sec/10 Cycles	D_2
	1 Sec/100 Cycles	D_3
	10 Sec/1k Cycles	D_4
PIN 31	Enable External Range Input	D_5
CONTROL INPUT PIN 1	Blank Display	D_4&Hold
	Display Test	D_8
	1MHz Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
	Test	D_5
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output for Same Digit That is Connected to This Input	

CONTROL INPUTS

Display Test - All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Display Off is selected at the same time.

Display Off - To enable the Display Off mode it is necessary to tie D_4 to the control input and have the HOLD input at V^+. The chip will remain in the Display Off mode until HOLD is switched low. While in the Display Off mode, the segment and digit driver outputs are open. During Display Off, the oscillator continues to run, with a typical supply current of 1.5mA with a 10MHz crystal, and no measurements are made. In addition, signals applied to the multiplexed inputs have no effect. A new measurement is initiated when the HOLD input goes low.

1MHz Select - The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as a 10MHz crystal. The internal decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in 1μs increments rather than 0.1μs.

External Oscillator Enable - In this mode, the external oscillator input is used, rather than the on chip oscillator, for the Timebase and Main Counter inputs in Period and Time interval modes. The on chip oscillator will continue to function when the external oscillator is selected, but have no effect on circuit operation. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself and enable the on chip oscillator. Connect external oscillator to **both** OSC IN (pin 35) and EXT OSC IN (pin 33).

External Decimal Point Enable - When external decimal point is enabled, a decimal point will be displayed whenever the digit driver connected to the external decimal point is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

Test Mode - This is a special mode used only in high speed production testing, and serves no other purpose.

RANGE INPUT

The range input selects whether the measurement is made for 1, 10, 100, or 1000 counts of the reference counter, or if the external range input determines the measurement time. In all functional modes except Unit Counter, a change in the range input will stop the measurement in progress, without updating the display, and initiate a new measurement. This prevents an erroneous first reading after the Range Input is changed.

FUNCTION INPUT

Six functions can be selected. They are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency.**

These functions select which signal is counted into the main counter and which signal is counted by the reference counter, as shown in Table 2. In Time Interval, a flip flop is set first by a 1→0 transition at INPUT A and then reset by a 1→0 transition at INPUT B. The oscillator is gated into the Main Counter during the time the flip flop is set. A change in the FUNCTION input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION Input is changed. If the main counter overflows, an overflow indication is output on the decimal output during D8.

TABLE 2

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (f_A)	Input A	100Hz (Oscillator ÷ 10^5 or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A→B)	Osc ON Gate	Osc OFF Gate
Unit Counter(Count A)	Input A	Not Applicable
Osc. Freq. (f_{OSC})	Oscillator	100Hz (Osc ÷ 10^5 or 10^4)

EXTERNAL DECIMAL POINT INPUT

When the EXTernal Decimal Point is selected, this input is active. Any of the digits, except D_8, can be connected to this point. D_8 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point.

HOLD Input - Except in the unit counter mode, when the HOLD Input is at V+, any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In unit counter mode when HOLD Input is at V+, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

RESET Input - The RESET Input also enables the main counter latches, resulting in an all zero output.

EXTernal RANGE Input - The EXTernal RANGE Input is used to select other ranges than those provided on the chip. Figure 4 shows the relationship between MEASurement IN PROGRESS and EXTernal RANGE Input.

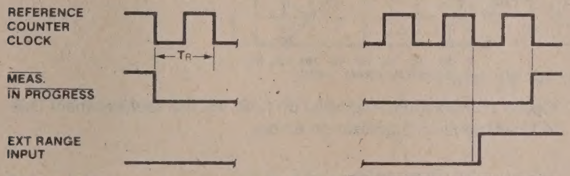


Figure 4: External Range Input to End of Measurement in Progress.

MEASUREMENT IN PROGRESS, STORE AND RESET Outputs - These outputs are provided to enable display of prescaler digits. Figure 5 shows the relationship between these signals during the time between measurements. All three outputs can drive a low power Schottky TTL load. The MEASUREMENT IN PROGRESS Output can directly drive one ECL load, if the ECL device is powered from the same power supply as the ICM7226.

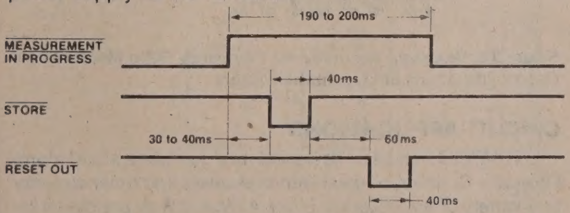


Figure 5: RESET OUT, STORE, and MEASUREMENT IN PROGRESS Outputs Between Measurements.

BCD Outputs - The BCD representation of each digit output is available at the BCD outputs; see Table 3 for Truth Table. The positive going (ICM7226A - Common Anode) or negative going (ICM7226B - Common Cathode) digit drivers lag the BCD data by 2 to 6 microseconds; the leading edge of the digit drive signal is used to externally latch the BCD data. Each BCD output will drive one low power Schottky TTL load and when interfacing low power Schottky TTL latches, it is necessary to use 1kΩ pull down resistors on the TTL inputs for optimum results. The display is multiplexed from MSD to LSD. Leading zero blanking has no effect on the BCD outputs.

TABLE 3 Truth Table BCD Outputs

NUMBER	BCD 8 PIN 7	BCD 4 PIN 6	BCD 2 PIN 17	BCD 1 PIN 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

BUFFered OSCillator OUTput - The BUFFered OSCillator OUTput has been provided to enable use of the on chip oscillator signal without loading the oscillator itself. This output will drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500Hz rate with a digit time of 244μs, and an interdigit blanking time of 6μs to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays; zeros following the decimal point will not be blanked. Leading zero blanking will also be disabled if the Main Counter overflows. The internal decimal point control displays frequency in kHz and time in μs.

The ICM7226A is designed to drive common anode LED displays at a peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be greater than 3mA under these conditions. The ICM7226B is designed to drive common cathode displays at a peak current of 15mA/segment, using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current, if required. Figures 6, 7, 8 and 9 show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

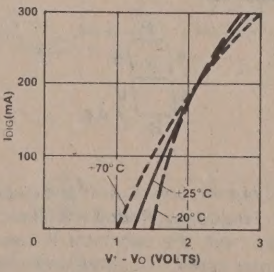
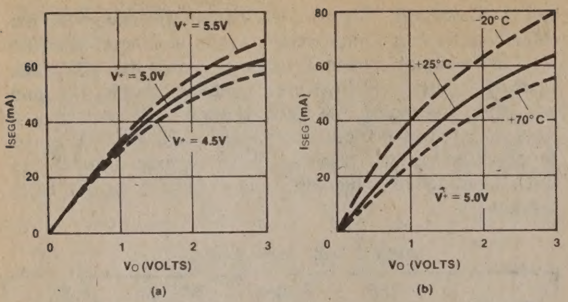


Figure 6: ICM7226A Typical I_{DIG} vs. $V^+ - V_O$
$4.5 \leq V^+ \leq 6.0V$



(a) (b)

Figure 7: ICM7226A Typical I_{SEG} vs. V_O

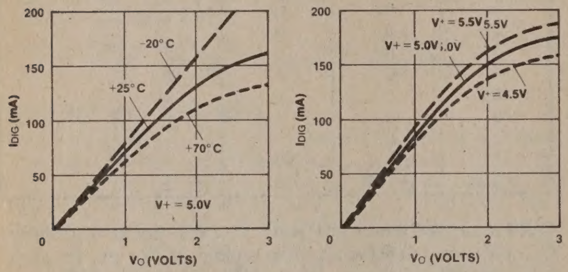


Figure 8: ICM7226B Typical I_{DIG} vs. V_O

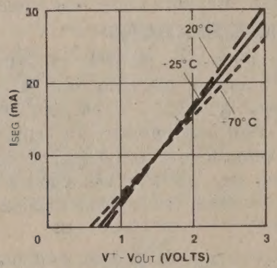
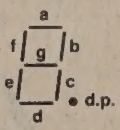


Figure 9: ICM7226B Typical I_{SEG} vs. $(V^+ - V_O)$
$4.5V \leq V^+ \leq 6.0V$

To increase the light output from the displays, V^+ may be increased to 6.0V, however care should be taken to see that maximum power and current ratings are not exceeded.

The segment and digit outputs in both the 7226A and B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

Segment Identification



ACCURACY

In a Universal Counter, crystal drift and quantization errors cause errors. In **Frequency, Period** and **Time Interval** Modes, a signal derived from the oscillator is used either in the Reference Counter or Main Counter, and in these modes, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **Frequency** Mode, maximum accuracy is obtained with high frequency inputs, and in **Period** Mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 10, the least accuracy will be obtained at 10kHz. In **Time Interval** measurements there is a maximum error of 1 count per interval. As a result there is the same inherent accuracy in all ranges, as shown in Figure 11. In **Frequency Ratio** measurement more accuracy can be obtained by averaging over more cycles of Input B as shown in Figure 12.

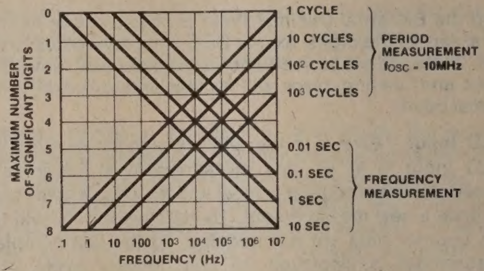


Figure 10: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors.

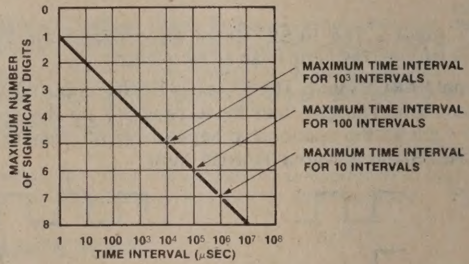


Figure 11: Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors.

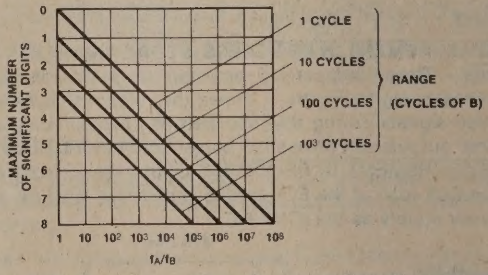


Figure 12: Maximum Accuracy for Frequency Ratio Measurement Due to Limitations of Quantization Errors.

CIRCUIT APPLICATIONS

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other circuitry in a variety of applications. Since A IN and B IN are digital inputs, additional circuitry will be required in many applications, for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications an FET source follower can be used for input buffering, and an ECL 10116 line receiver can be used for amplification and hysteresis to obtain high impedance input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely, depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, pull up resistors to V+ should be used to obtain optimal voltage swing at A IN and B IN.

If prescalers aren't required, the ICM7226 can be used to implement a minimum component Universal counter as shown in figure 13.

For input frequencies up to 40MHz, the circuit shown in figure 14 can be used to implement a **Frequency and Period Counter.** To obtain the correct value when measuring frequency and period, it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this the time between measurements is lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

If the input frequency is prescaled by ten, the oscillator frequency can remain at either 10MHz or 1MHz, but the decimal point must be moved. Figure 15 shows use of a ÷10 prescaler in **Frequency Counter** mode. Additional logic has been added to enable the 7226 to count the input directly in **Period** mode for maximum accuracy. Note that A IN comes from Q_C rather than Q_D, to obtain an input duty cycle of 40%. If an output with a duty cycle not near 50% must be used then it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse to guarantee a 50ns minimum pulse width.

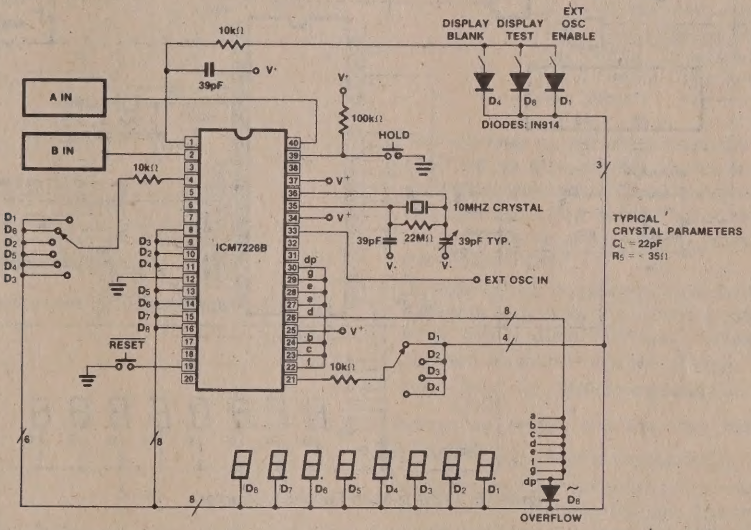
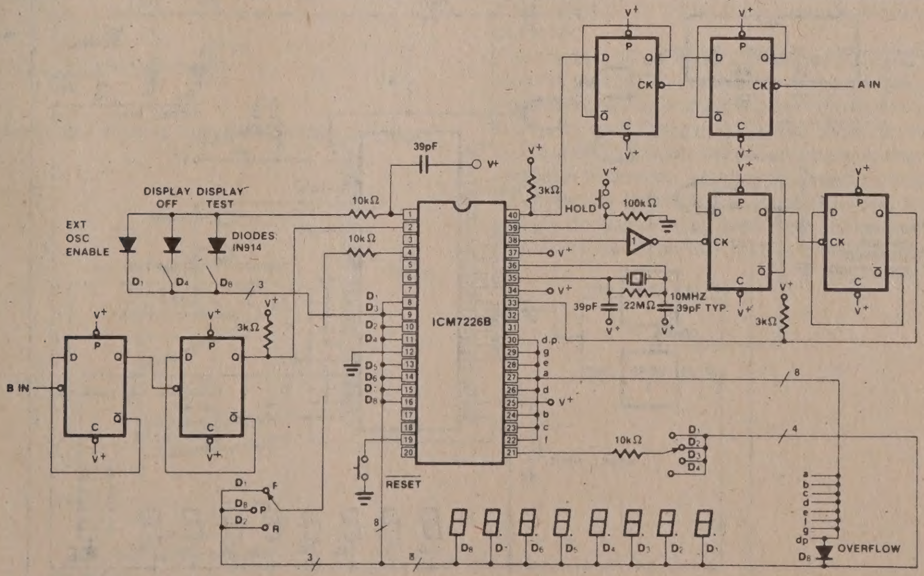

A IN
B IN
10kΩ
39pF
V+
100kΩ
HOLD
DISPLAY BLANK
DISPLAY TEST
EXT OSC ENABLE
D4
D8
D1
DIODES: IN914
ICM7226B
10MHZ CRYSTAL
22MΩ
39pF TYP.
TYPICAL CRYSTAL PARAMETERS
CL = 22pF
RS = < 35Ω
EXT OSC IN
RESET
OVERFLOW
dp
a
b
c
d
e
f
g

Figure 13: 10MHz Universal Counter


V+
P
D
Q
CK
Q̄
C
A IN
B IN
39pF
3kΩ
HOLD
100kΩ
10kΩ
DISPLAY OFF
DISPLAY TEST
EXT OSC ENABLE
DIODES IN914
D1
D4
D8
ICM7226B
10MHZ
22MΩ
39pF TYP.
RESET
F
P
R
OVERFLOW

Notes: 1) If a 2.5MHz crystal is used, diode D1 and I.C.'s 1 and 2 can be eliminated.

Figure 14: 40MHz Frequency, Period Counter

Figure 16 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the FUNCTION Input. Since the CD4016 is a digitally controlled analog transmission gate, no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2 or 3 bit digital inputs. These analog multiplexers may also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74153 or 74251 may also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

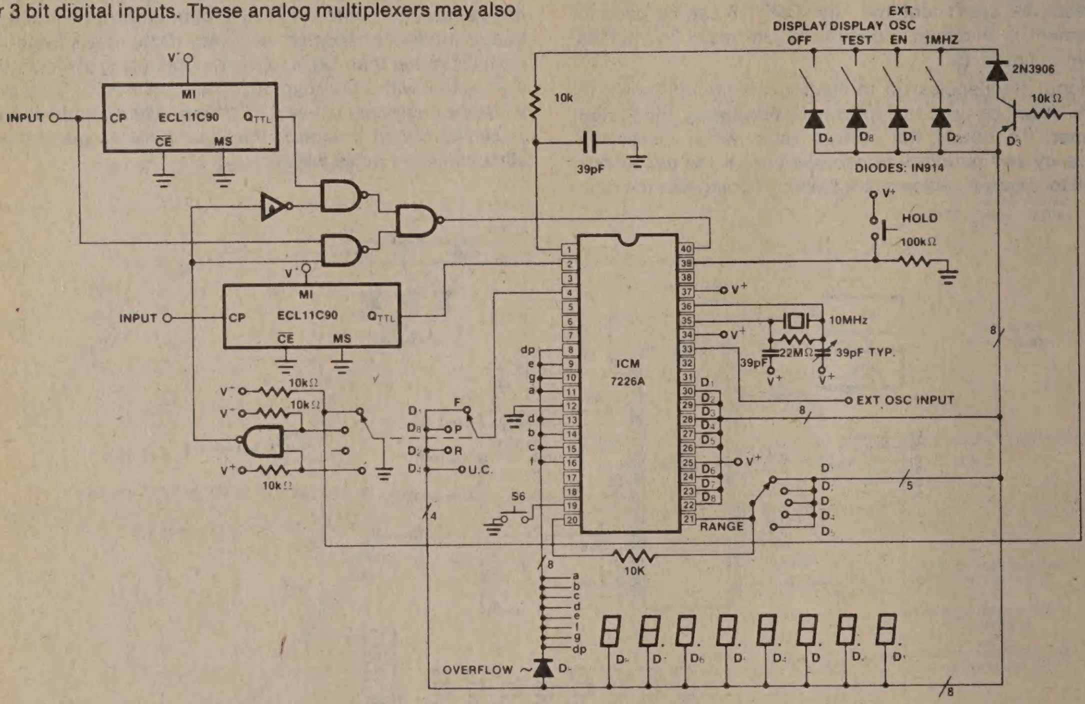

DISPLAY OFF
DISPLAY TEST
EXT. OSC EN
1MHZ
2N3906
10kΩ
10k
39pF
D4 D8 D1 D2 D3
DIODES: IN914
V+
HOLD
100kΩ
INPUT
MI
CP
ECL11C90
QTTL
CE
MS
ICM 7226A
10MHz
22MΩ
39pF TYP.
EXT OSC INPUT
RANGE
10K
dp e g a d b c f
P
R
U.C.
F
S6
OVERFLOW
a b c d e f g dp

Figure 15: 100MHz Multi Function Counter

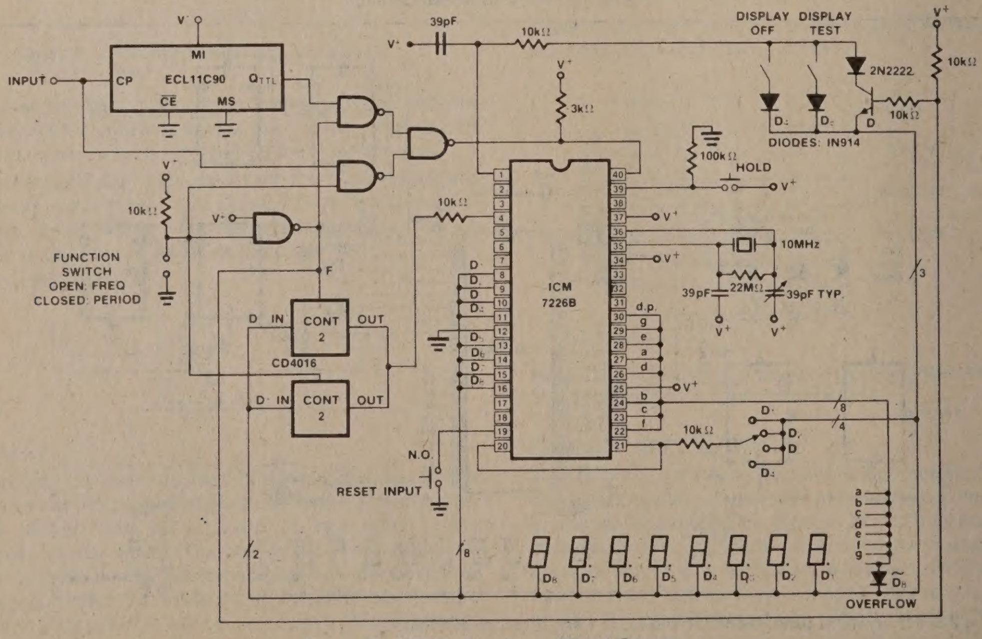
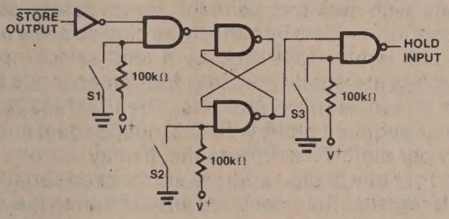

DISPLAY OFF
DISPLAY TEST
V+
39pF
10kΩ
2N2222
3kΩ
D
DIODES: IN914
100kΩ
HOLD
INPUT
MI
CP
ECL11C90
QTTL
CE
MS
FUNCTION SWITCH OPEN: FREQ CLOSED: PERIOD
F
D IN CONT 2 OUT
CD4016
ICM 7226B
10MHz
22MΩ
39pF TYP.
d.p. g e a d b c f
N.O.
RESET INPUT
a b c d e f g
OVERFLOW

Figure 16: 100MHz Frequency Period Counter

The circuit shown in figure 17 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the $\overline{\text{STORE}}$ output to put the ICM7226 into a hold mode. The HOLD input can also be used to reduce the time between measurements. The circuit shown in figure 18 puts a short pulse into the HOLD input a short time after STORE goes low. A new measurement will be initiated at the end of the pulse on the HOLD Input. This circuit reduces the time between measurements to less than 40ms from 200ms; use of the circuit shown in Figure 18 on the circuit shown in Figure 14 will reduce the time between measurements from 1600ms to 800ms.



SWITCH	FUNCTION
S1	OPEN = SINGLE MEAS MODE ENABLED
S2	CLOSED = INITIATE NEW MEASUREMENT
S3	CLOSED = HOLD INPUT

Figure 17: Single Measurement Circuit for Use With ICM7226

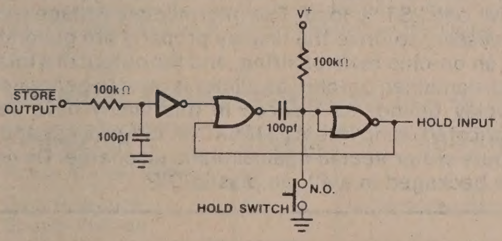
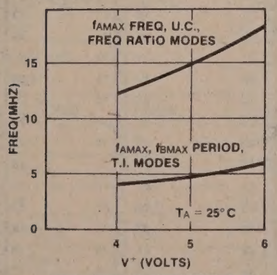


Figure 18: Circuit for Reducing Time Between Measurements



fAMAX, fBMAX AS FUNCTION OF V+

Figure 19: Typical Operating Characteristics

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35Ω.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{IN} C_{OUT} R_S \left(1+\frac{C_O}{C_L}\right)^2$$

$$\text{where } C_L = \left(\frac{CinCout}{Cin+Cout}\right)$$

C_O = Crystal static capacitance
R_S = Crystal Series Resistance
Cin = Input Capacitance
Cout = Output Capacitance
$\omega = 2\pi f$

The required g_m should exceed the g_m specified for the ICM7226 by at least 50% to insure reliable startup. The oscillator input and output pins each contribute about 4pF to C_{IN} and C_{OUT}. For maximum frequency stability, C_{IN} and C_{OUT} should be approximately twice the specified crystal static capacitance.

In cases where nondecade prescalers are used, it may be desirable to replace the 10MHz crystal with one of 1MHz. When this is done, both the multiplex rate and the time between measurements will change. The multiplex rate is $f_{max} = \frac{f_{osc}}{2 \times 10^4}$ for 10MHz mode and $f_{max} = \frac{f_{osc}}{2 \times 10^3}$ for a different frequency mode, and the time between measurements is $\frac{2 \times 10^6}{f_{osc}}$ in the 10MHz mode and f_{OSC} in the 1MHz mode. The buffered oscillator output should be used as an oscillator test point or to drive additional logic; this output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or the external oscillator input, a 10kΩ resistor should be added from buffered oscillator output to V+.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. In particular, coupling from the BUFfered OSCillator OUTput and EXTernal OSCillator INput to the OSCillator OUTput or OSCillator INput can cause undesirable shifts in oscillator frequency. To minimize this coupling, pins 34 and 37 should be connected to V+ or GROUND and these two signals should be kept away from the oscillator circuit. A typical crystal is the 10MHz CTS KNIGHTS ISI-002.

INTERSIL

PRELIMINARY
Specifications Subject To Change Without Notice

ICM7231/32/33/34 Display Decoder/Drivers for Triplexed Liquid Crystal Displays

FEATURES

- **ICM7231: Drives 8 digits of 7 segments with two independent annunciators per digit. Address and data input in parallel format.**
- **ICM7232: Drives 10 digits of 7 segments with two independent annunciators per digit. Address and data input in serial format.**
- **ICM7233: Drives 4 characters of 18 segments. Address and data input in parallel format.**
- **ICM7234: Drives 5 characters of 18 segments. Address and data input in serial format.**
- **Chips provide all signals required to drive rows and columns of triplexed LCD display.**
- **Display voltage independent of power supply, allows user control of display operating voltage and temperature compensation if desired.**
- **On-chip oscillator provides all display timing.**
- **Total power consumption typically 200μW, maximum 500μW at 5V.**
- **Low-power shutdown mode retains data with 5μW typical power consumption at 5V, 1μW at 2V.**
- **Direct interfacing to high-speed microprocessors and microcomputers.**

GENERAL DESCRIPTION

The ICM7231/7234 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry and contain a mask-programmed ROM allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

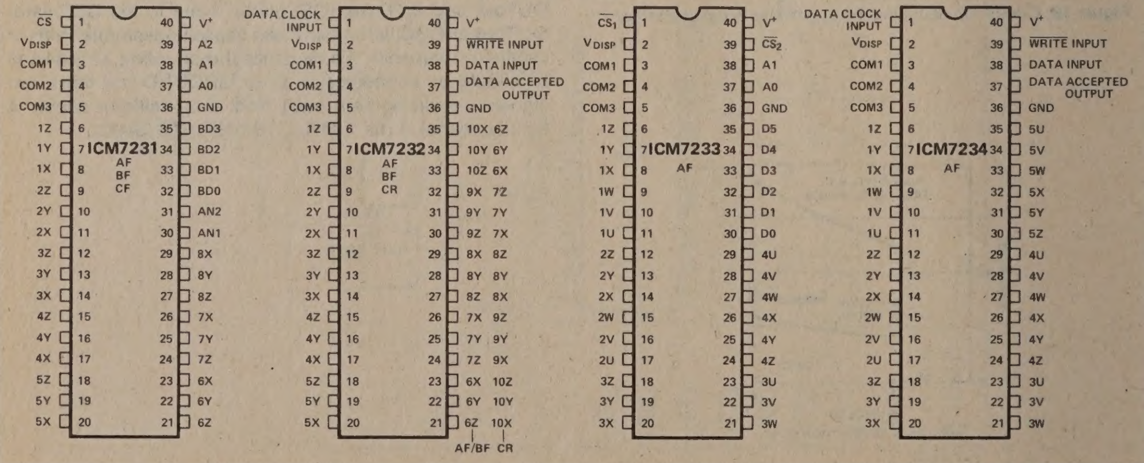
The ICM7231 drives displays with 8 seven-segment digits with two independent annunciators per digit, accepting six data bits and three digit address bits from parallel inputs controlled by a chip select input. The data bits are subdivided into four binary code bits and two annunciator control bits. The ICM7232 drives 10 seven-segment digits with two independent annunciators per digit. To write into the display, six bits of data and four bits of digit address are clocked serially into a shift register, then decoded and written to the display.

The ICM7233 has a parallel input structure similar to the ICM7231, but the decoding and the outputs are organized to drive four 18-segment alphanumeric characters. The six data bits represent a 6-bit ASCII code.

The ICM7234 uses a serial input structure like that of the ICM7232, and drives five 18-segment characters. Again, the input bits represent a 6-bit ASCII code.

Input levels are TTL compatible, and the DATA ACCEPTED output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string, and the output of a totally self-contained on-chip oscillator is used to generate all display timing. All devices in this family have been fabricated using Intersil's MAXCMOS® process and all inputs are protected against static discharge. Devices are packaged in a 40 pin plastic DIP.

PIN CONFIGURATIONS (OUTLINE DRAWING PL)


ICM7231
AF
BF
CF
CS 1 40 V+
VDISP 2 39 A2
COM1 3 38 A1
COM2 4 37 A0
COM3 5 36 GND
1Z 6 35 BD3
1Y 7 34 BD2
1X 8 33 BD1
2Z 9 32 BD0
2Y 10 31 AN2
2X 11 30 AN1
3Z 12 29 8X
3Y 13 28 8Y
3X 14 27 8Z
4Z 15 26 7X
4Y 16 25 7Y
4X 17 24 7Z
5Z 18 23 6X
5Y 19 22 6Y
5X 20 21 6Z
ICM7232
AF
BF
CR
DATA CLOCK INPUT 1 40 V+
VDISP 2 39 WRITE INPUT
COM1 3 38 DATA INPUT
COM2 4 37 DATA ACCEPTED OUTPUT
COM3 5 36 GND
1Z 6 35 10X 6Z
1Y 7 34 10Y 6Y
1X 8 33 10Z 6X
2Z 9 32 9X 7Z
2Y 10 31 9Y 7Y
2X 11 30 9Z 7X
3Z 12 29 8X 8Z
3Y 13 28 8Y 8Y
3X 14 27 8Z 8X
4Z 15 26 7X 9Z
4Y 16 25 7Y 9Y
4X 17 24 7Z 9X
5Z 18 23 6X 10Z
5Y 19 22 6Y 10Y
5X 20 21 6Z 10X
AF/BF CR
ICM7233
AF
CS1 1 40 V+
VDISP 2 39 CS2
COM1 3 38 A1
COM2 4 37 A0
COM3 5 36 GND
1Z 6 35 D5
1Y 7 34 D4
1X 8 33 D3
1W 9 32 D2
1V 10 31 D1
1U 11 30 D0
2Z 12 29 4U
2Y 13 28 4V
2X 14 27 4W
2W 15 26 4X
2V 16 25 4Y
2U 17 24 4Z
3Z 18 23 3U
3Y 19 22 3V
3X 20 21 3W
ICM7234
AF
DATA CLOCK INPUT 1 40 V+
VDISP 2 39 WRITE INPUT
COM1 3 38 DATA INPUT
COM2 4 37 DATA ACCEPTED OUTPUT
COM3 5 36 GND
1Z 6 35 5U
1Y 7 34 5V
1X 8 33 5W
1W 9 32 5X
1V 10 31 5Y
1U 11 30 5Z
2Z 12 29 4U
2Y 13 28 4V
2X 14 27 4W
2W 15 26 4X
2V 16 25 4Y
2U 17 24 4Z
3Z 18 23 3U
3Y 19 22 3V
3X 20 21 3W

OPTION TABLE AND ORDERING INFORMATION

ORDER PART NUMBER	OUTPUT CODE	ANNUNCIATOR LOCATIONS	INPUT	OUTPUT
ICM7231AFIPL	Hexadecimal	Both Annunciators on COM3	Parallel Entry 4 bit Data 2 bit Annunciators 3 bit Address	Eight Digits
ICM7231BFIPL	Code B			
ICM7231CFIPL	Code B	1 Annunciator COM1 1 Annunciator COM3		
ICM7232AFIPL	Hexadecimal	Both Annunciators on COM3	Serial Entry 4 bit Data 2 bit Annunciators 4 bit Address	Ten Digits
ICM7232BFIPL	Code B			
ICM7232CRIPL	Code B	1 Annunciator COM1 1 Annunciator COM3		
ICM7233AFIPL	64 Character (ASCII) 18 Segment	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
ICM7234AFIPL	64 Character (ASCII) 18 Segment	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters

Dice versions also available (ICM7231AF/D, ICM7233AF/D, etc.).

ABSOLUTE MAXIMUM RATINGS

Power Dissipation[1] .... 0.5 W @ 70°C
Supply Voltage (V^+) .... 6.5 V
Input Voltage[2] .... $-0.3 \leq V_{IN} \leq 6.5$
Display Voltage[2] .... $-0.3 \leq V_{DISP} \leq +0.3$
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. This limit refers to that of the package and will not be obtained during normal operation.
2. Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than -0.3 volts below ground, but may be connected to voltages above V^+ but not more than 6.5 volts above GND.

ELECTRICAL CHARACTERISTICS $V^+ = 5V$, $T_A = 25°C$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Power Supply Voltage	V^+		4	5	5.5	V
Data Retention Supply Voltage	V^+	Guaranteed Retention at 2V	2	1.6		V
Logic Supply Current	I^+	Current from V^+ to Ground excluding Display. $V_{DISP} = 2V$		40	100	μA
Shutdown Total Current	I_S	V_{DISP} Pin 2 Open		1	10	μA
Display Voltage Range	V_{DISP}	Ground $\leq V_{DISP} \leq V^+$	0		V^+	V
Display Voltage Setup Current	I_{DISP}	$V_{DISP} = 2V$ Current from V^+ to V_{DISP} On-Chip		15	25	μA
Display Voltage Setup Resistor Value	R_{DISP}	One of Three Identical Resistors in String		75		kΩ
DC Component of Display Signals				1/2	1	% ($V^+ - V_{DISP}$)
Display Frame Rate	f_{DISP}	See Figure 2	80	120		Hz
Input Low Level	V_{IL}	ICM7231, ICM7233 Pins 30-35, 37-39, 1			0.8	V
Input High Level	V_{IH}		2.0			V
Input Leakage	I_{ILK}	ICM7232, ICM7234 Pins 1, 38, 39		0.1	1	μA
Input Capacitance	C_{IN}			5		pF
Output Low Level	V_{OL}	Pin 37, ICM7232, ICM7234 $V^+ = 4.5V$, $I_{OUT} = \pm 400\mu A$			0.4	V
Output High Level	V_{OH}		4.1			V
Operating Temperature Range	T_{OP}	Industrial Range	-20		+85	°C

AC CHARACTERISTICS $V^+ = 5V \pm 10\%$, $-20°C \le T_A \le +85°C$

PARALLEL INPUT (ICM7231, ICM7233) See Figure 12

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Chip Select Pulse Width	t_{cs}		500			ns
Address/Data Setup Time	t_{ds}		200			ns
Address/Data Hold Time	t_{dh}		0	-20		ns
Inter-Chip Select Time	t_{ics}		2			µs

SERIAL INPUT (ICM7232, ICM7234) See Figures 15, 16, 17

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Data Clock Low Time	$t_{\overline{cl}}$		350			ns
Data Clock High Time	t_{cl}		350			ns
Data Setup Time	t_{ds}		200			ns
Data Hold Time	t_{dh}		0	-20		ns
$\overline{\text{Write}}$ Pulse Width	t_{wp}		350			ns
Write Pulse to Clock at Initialization	t_{wil}		1.5			µs
Data Accepted Low Output Delay	t_{odl}			10	100	ns
Data Accepted High Output Delay	t_{odh}			1.5	3	µs

TERMINAL DEFINITIONS

ICM7231 PARALLEL INPUT NUMERIC DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION	
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit	High = ON Low = OFF	See Table 3
BD0 BD1 BD2 BD3	32 33 34 35	Least Significant ⎤ 4 Bit Binary Data Inputs Most Significant ⎦	Input Data (See Table 1)	HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1 A2	37 38 39	Least Significant ⎤ 3 Bit Digit Address Inputs Most Significant ⎦	Input Address (See Table 2)	
$\overline{\text{CS}}$	1	Data Input Strobe/Chip Select	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit	

ICM7233 PARALLEL INPUT ALPHA DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION	
D0 D1 D2 D3 D4 D5	30 31 32 33 34 35	Least Significant Most Significant — 6 Bit (ASCII) Data Inputs	Input Data See Table 4	HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1	37 38	Least Significant Most Significant — Address Inputs	Input Add. See Table 5	
$\overline{\text{CS1}}$ $\overline{\text{CS2}}$	39 1	Chip Select Inputs	Both inputs LOW load data into input latches. Rising edge of either input causes data to be latched, decoded and sent out to addressed character.	

ICM7232 and ICM7234 SERIAL DATA AND ADDRESS INPUT

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Data Input	38	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
$\overline{\text{WRITE}}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of $\overline{\text{WRITE}}$ causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic to be reset. When DATA ACCEPTED Output is HIGH, positive going edge of $\overline{\text{WRITE}}$ triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. ICM7232: Eleventh edge resets shift register and control logic. ICM7234: Tenth edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register; ICM7232 8, 9 or 10 bits ICM7234 9 bits

ALL DEVICES

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V^+) chip is shutdown; oscillator stops, all display pins to V^+.
Common Line Driver Outputs	3,4,5		Drive display commons, or rows.
Segment Line Driver Outputs	6-29 6-35	(On ICM7231/33) (On ICM7232/34)	Drive display segments, or columns.
V^+	40	Chip Positive Supply	
GND	36	Chip Ground	

TRIPLEXING (1/3 MULTIPLEXING) LIQUID CRYSTAL DISPLAYS

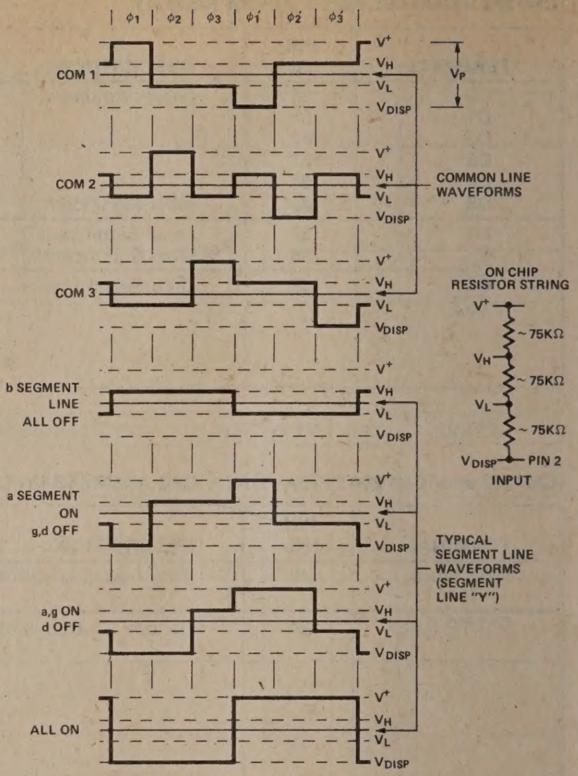
Figure 1 shows the connection diagram for a typical 7-segment display font with two annunciators such as would be used with an ICM7231 or ICM7232 numeric display driver. Figure 2 shows the voltage waveforms of the common lines and one segment line, chosen for this example to be the "Y" segment line. This line intersects with COM1 to form the "a" segment, COM2 to form the "g" segment and COM3 to form the "d" segment. Figure 2 also shows the waveform of the "Y" segment line for four different ON/OFF combinations of the "a", "g" and "d" segments. Each intersection (segment or annunicator) acts as a capacitance from segment line to common line, shown schematically in Figure 3. Figure 4 shows the voltage across the "g" segment for the same four combinations of ON/OFF segments in Figure 2.

The degree of polarization of the liquid crystal material and thus the contrast of any intersection depends on the RMS voltage across the intersection capacitance. Note from Figure 4 that the RMS OFF voltage is always $V_P/3$ and that the RMS ON voltage is always $1.92\ V_P/3$.

For a 1/3 multiplexed LCD, the ratio of RMS ON to OFF voltages is fixed at 1.92, achieving adequate display contrast with this ratio of applied RMS voltage makes some demands on the liquid crystal material used.

Figure 5 shows the curve of contrast versus applied RMS voltage for a liquid crystal material tailored for $V_P = 3.1V$, a typical value for 1/3-multiplexed displays in calculators. Note that the RMS OFF voltage $V_P/3 \approx 1V$ is just below the "threshold" voltage where contrast begins to increase. This places the RMS ON voltage at 2.1V, which provides about 85% contrast when viewed straight on.

All members of the ICM7231/ICM7234 family use an internal resistor string of three equal value resistors to generate the voltages used to drive the display. One end of the string is connected on the chip to V^+ and the other end (user input) is available at pin 2 (V_{DISP}) on each chip. This allows the display voltage input (V_{DISP}) to be optimized for the particular liquid crystal material used. Remember that $V_P = V^+ - V_{DISP}$ and should be three times the threshold voltage of the liquid crystal material used. Also it is very important that pin 2 never be driven below ground. This can cause device latchup and destruction of the chip.



NOTE: ϕ_1, ϕ_2, ϕ_3 – COMMON HIGH WITH RESPECT TO SEGMENT.

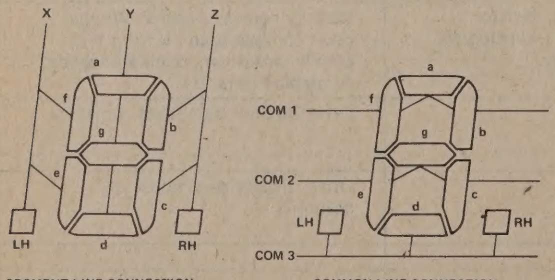
$\phi_1', \phi_2', \phi_3'$ – COMMON LOW WITH RESPECT TO SEGMENT.

COM 1 ACTIVE DURING ϕ_1 AND ϕ_1'

COM 2 ACTIVE DURING ϕ_2 AND ϕ_2'

COM 3 ACTIVE DURING ϕ_3 AND ϕ_3'

Figure 2. Display Voltage Waveforms



SEGMENT LINE CONNECTION

COMMON LINE CONNECTION

Figure 1. Connection Diagrams for Typical 7-Segment Displays

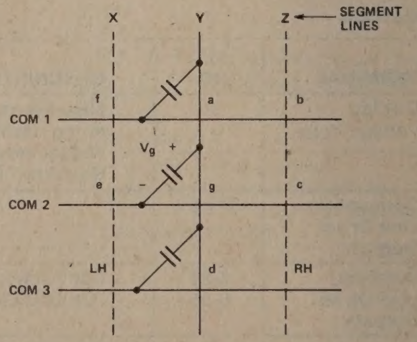
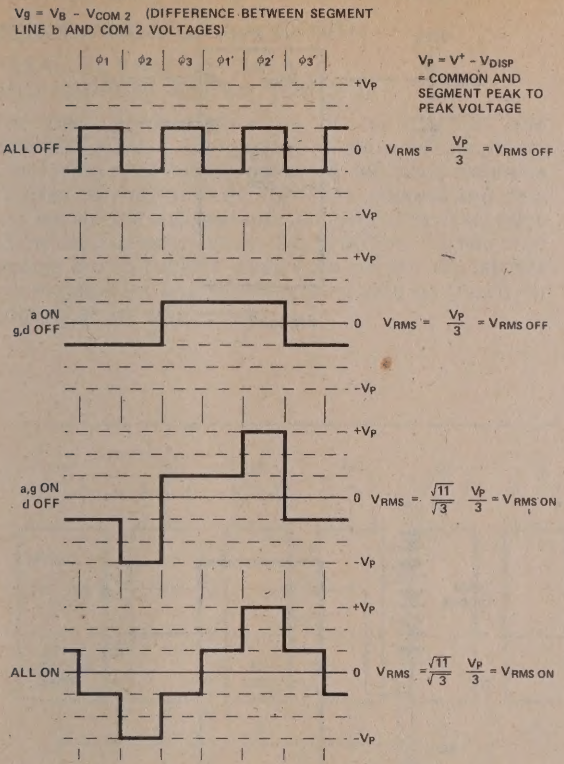


Figure 3. Display Schematic


$V_g = V_B - V_{COM\,2}$ (DIFFERENCE BETWEEN SEGMENT LINE b AND COM 2 VOLTAGES)
ϕ_1 ϕ_2 ϕ_3 ϕ_1' ϕ_2' ϕ_3'
$V_P = V^+ - V_{DISP}$ = COMMON AND SEGMENT PEAK TO PEAK VOLTAGE
+VP
0
-VP
ALL OFF
$V_{RMS} = \frac{V_P}{3} = V_{RMS\,OFF}$
a ON g,d OFF
$V_{RMS} = \frac{V_P}{3} = V_{RMS\,OFF}$
a,g ON d OFF
$V_{RMS} = \frac{\sqrt{11}}{\sqrt{3}} \frac{V_P}{3} = V_{RMS\,ON}$
ALL ON
$V_{RMS} = \frac{\sqrt{11}}{\sqrt{3}} \frac{V_P}{3} = V_{RMS\,ON}$

VOLTAGE CONTRAST RATIO = $\frac{V_{RMS\,ON}}{V_{RMS\,OFF}} = \frac{\sqrt{11}}{\sqrt{3}} = 1.92$

NOTE: ϕ_1, ϕ_2, ϕ_3 – COMMON HIGH WITH RESPECT TO SEGMENT.

$\phi_1', \phi_2', \phi_3'$ – COMMON LOW WITH RESPECT TO SEGMENT.

COM 1 ACTIVE DURING ϕ_1 AND ϕ_1'

COM 2 ACTIVE DURING ϕ_2 AND ϕ_2'

COM 3 ACTIVE DURING ϕ_3 AND ϕ_3'

Figure 4. Voltage Waveforms on Segment g (V_g)

TEMPERATURE EFFECTS AND TEMPERATURE COMPENSATION

The performance of the IC material is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures (-20°C) some displays may take several seconds to change to a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. One high temperature effect to consider deals with plastic materials used to make the polarizer. Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

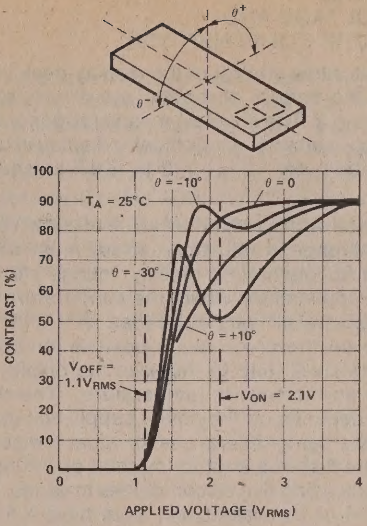


Figure 5. Contrast vs. Applied RMS Voltage

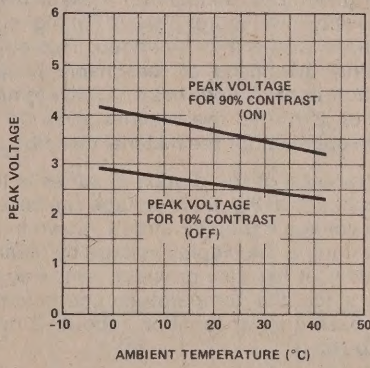


Figure 6. Temperature Dependence of LC Threshold

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of -7 to -14 mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_P, when the threshold voltage drops below $V_P/3$ OFF segments begin to be visible. Figure 6 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 5.

For applications where the display temperature does not vary widely, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_P) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

DISPLAY VOLTAGE AND TEMPERATURE COMPENSATION

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 2. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 2 to GND as shown in Figure 7.

A potentiometer with a maximum value of 200 kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient (this will tend to increase the display peak voltage with an increase in temperature). The display voltage also depends on the power supply voltage, and this will require tighter tolerances for wider temperature ranges. Figure 8 shows another method of setting up a display voltage using five silicon diodes in series. These diodes, 1N914 or equivalent, will each have a forward drop of approximately 0.65V, with approximately 20μA flowing through them at room temperature. Thus, 5 diodes will give 3.25V, suitable for a 3V display using materials as shown in Figures 5 and 6. For higher voltage displays, more diodes may be added. This circuit has the additional advantage of reasonable temperature compensation, as each diode has a negative temperature coefficient of -2 mV/°C; five in series gives -10 mV/°C, not far from optimum for the material described.

The disadvantage of the diodes in series is that only integral multiples of the diode voltage can be achieved. The diode voltage multiplier circuit shown in Figure 9 allows fine-tuning the display voltage by means of the potentiometer; it likewise provides temperature compensation since the temperature coefficient of the transistor base-emitter junction (about -2 mV/°C) is also multiplied.

The transistor used in the circuit of Figure 9 must have a beta of at least 100 with a collector current of 10 μA. The inexpensive 2N2222 shown in the figure is a suitable device, but any transistor with high beta at low current will function properly.

For battery operation, where the display voltage is generally the same as the battery voltage (usually 3-4.5V), the chip may be operated at the display voltage, with V_{DISP} connected to GND.

The inputs of the chip are designed such that they may be driven above V^+ without damaging the chip. This allows, for example, the chip and display to operate at a regulated 3V, and a microprocessor driving its inputs to operate with a less well controlled 5V supply. The inputs should not be driven more than 6.5V above GND under any circumstances.

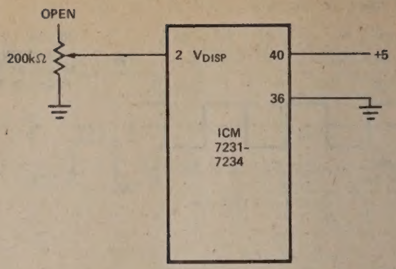


Figure 7

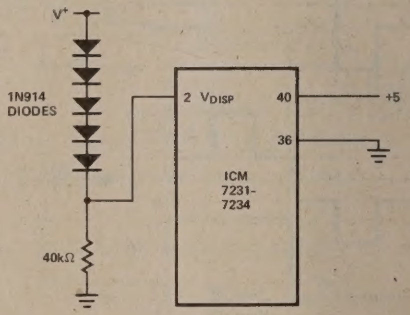


Figure 8

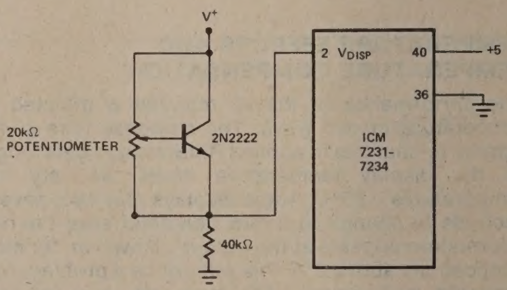


Figure 9

DESCRIPTION OF OPERATION

PARALLEL INPUT OF DATA AND ADDRESS ICM7231, ICM7233

The parallel input structure of the ICM7231 and ICM7233 devices is organized to allow simple, direct interfacing to all microprocessors, see block diagrams Figures 10 and 11. In the ICM7231, address and data bits are written into the input latches on the rising edge of the chip select input. In the ICM7233, the two chip selects are equivalent; when both are low, the latches are transparent and the data is latched on the rising edge of either chip select.

The rising edge of the chip select also triggers an on-chip pulse which enables the address decoder and latches the decoded data into the addressed digit outputs. The timing requirements for the parallel input devices are shown in Figure 12, with the values for setup, hold, and pulse width times shown in AC Characteristics on page 3. Note that there is a minimum time between chip select pulses; this is to allow sufficient time for the on-chip enable pulse to decay, and ensures that new data doesn't appear at the decoder inputs before the decoded data is written to the outputs.

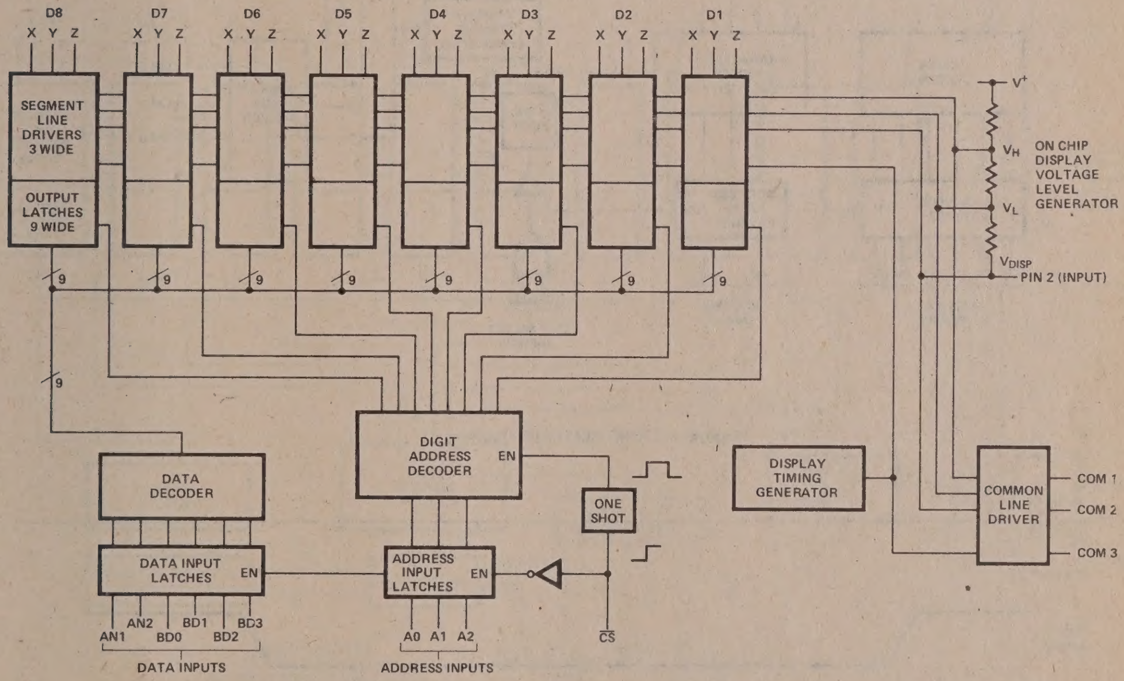

D8
D7
D6
D5
D4
D3
D2
D1
X Y Z
SEGMENT LINE DRIVERS 3 WIDE
OUTPUT LATCHES 9 WIDE
9
V+
VH
VL
VDISP
ON CHIP DISPLAY VOLTAGE LEVEL GENERATOR
PIN 2 (INPUT)
DIGIT ADDRESS DECODER
EN
ONE SHOT
DISPLAY TIMING GENERATOR
COMMON LINE DRIVER
COM 1
COM 2
COM 3
DATA DECODER
DATA INPUT LATCHES
ADDRESS INPUT LATCHES
AN1
AN2
BD0
BD1
BD2
BD3
DATA INPUTS
A0 A1 A2
ADDRESS INPUTS
CS

Figure 10. ICM7231 Block Diagram

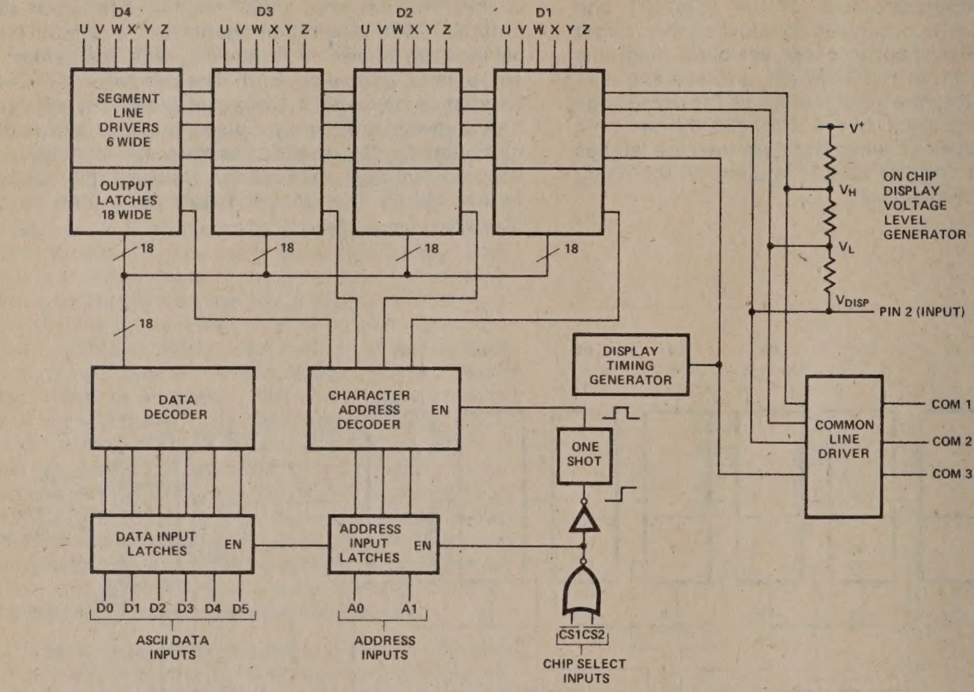
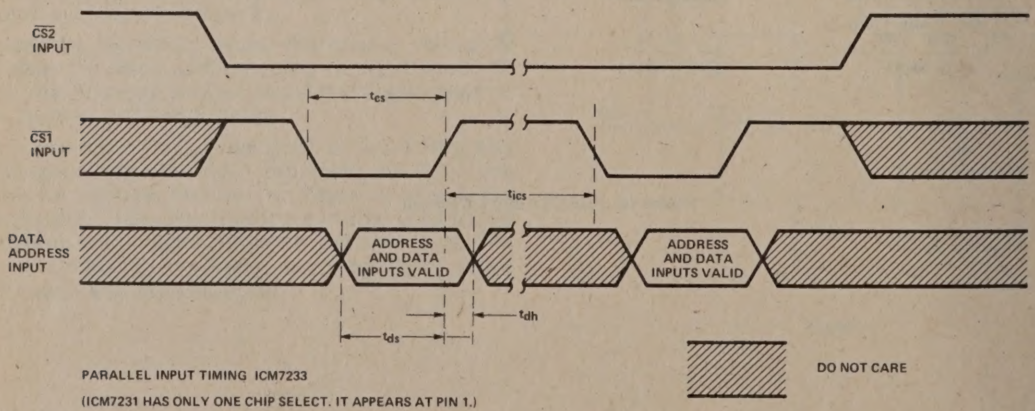

D4
D3
D2
D1
U V W X Y Z
SEGMENT LINE DRIVERS 6 WIDE
OUTPUT LATCHES 18 WIDE
18
V+
VH
VL
VDISP
PIN 2 (INPUT)
ON CHIP DISPLAY VOLTAGE LEVEL GENERATOR
DISPLAY TIMING GENERATOR
DATA DECODER
CHARACTER ADDRESS DECODER
EN
ONE SHOT
COMMON LINE DRIVER
COM 1
COM 2
COM 3
DATA INPUT LATCHES
ADDRESS INPUT LATCHES
D0 D1 D2 D3 D4 D5
ASCII DATA INPUTS
A0 A1
ADDRESS INPUTS
CS1 CS2
CHIP SELECT INPUTS

Figure 11. ICM7233 Block Diagram


CS2 INPUT
CS1 INPUT
DATA ADDRESS INPUT
tcs
tics
ADDRESS AND DATA INPUTS VALID
tds
tdh
DO NOT CARE

PARALLEL INPUT TIMING ICM7233

(ICM7231 HAS ONLY ONE CHIP SELECT. IT APPEARS AT PIN 1.)

Figure 12. Parallel Input Timing

SERIAL INPUT OF DATA AND ADDRESS ICM7232, ICM7234

The ICM7232 and ICM7234 trade six pins used as data inputs on the ICM7231 and ICM7233 for six more segment lines, allowing two more 9-segment digits (ICM7232) or one more 18-segment character (ICM7234). This is done at the cost of ease in interfacing, and requires that data and address information be entered serially. Refer to block diagrams, Figures 13 and 14 and timing diagrams, Figures 15, 16, and 17. The interface consists of four pins: DATA Input, DATA CLOCK Input, $\overline{\text{WRITE}}$ Input and DATA ACCEPTED Output. The data present at the DATA Input is clocked into a shift register on the rising edge of the DATA CLOCK Input signal, and when the correct number of bits has been shifted into the shift register (8 in the ICM7232, 9 in the ICM7234), the DATA ACCEPTED Output goes low. Following this, a low-going pulse at the $\overline{\text{WRITE}}$ input will trigger the chip to decode the data and store it in the output latches of the addressed digit. After the data is latched at the outputs, the shift register and the control logic are reset, returning the DATA ACCEPTED Output high. After this occurs, a pulse at the $\overline{\text{WRITE}}$ input will not change the outputs, but will reset the control logic and shift register, assuring that each data bit will be entered into the correct position in the shift register depending on subsequent DATA CLOCK inputs.

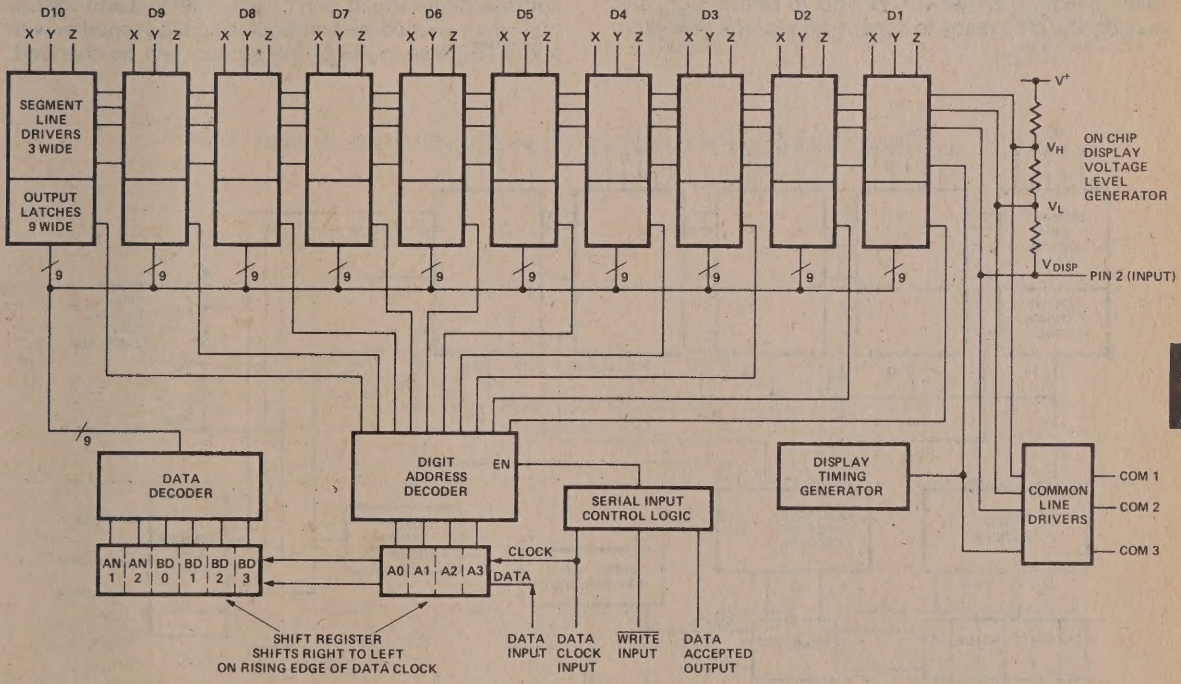

D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
X Y Z
SEGMENT LINE DRIVERS 3 WIDE
OUTPUT LATCHES 9 WIDE
9
V+
VH
VL
VDISP
ON CHIP DISPLAY VOLTAGE LEVEL GENERATOR
PIN 2 (INPUT)
DATA DECODER
DIGIT ADDRESS DECODER
EN
SERIAL INPUT CONTROL LOGIC
DISPLAY TIMING GENERATOR
COMMON LINE DRIVERS
COM 1
COM 2
COM 3
AN 1
AN 2
BD 0
BD 1
BD 2
BD 3
A0
A1
A2
A3
CLOCK
DATA
SHIFT REGISTER SHIFTS RIGHT TO LEFT ON RISING EDGE OF DATA CLOCK
DATA INPUT
DATA CLOCK INPUT
WRITE INPUT
DATA ACCEPTED OUTPUT

Figure 13. ICM7232 Block Diagram

The shift register and control logic will also be reset if too many data clock input edges are received; this also prevents incorrect data from being decoded. In the ICM7232, the eleventh clock resets the shift register and control logic, while in the ICM7234 it is the tenth.

The recommended procedure for entering data is shown in the serial input timing diagram, Figure 15. First, when DATA ACCEPTED is high, send a $\overline{\text{WRITE}}$ pulse. This resets the shift register and control logic and initializes the chip for the data input sequence. Next clock in the appropriate number of correct data and address bits. The DATA ACCEPTED Output may be monitored if desired, to determine when the chip is read to output the decoded data. When the correct number of bits has been entered, and the DATA ACCEPTED Output is low, a pulse at $\overline{\text{WRITE}}$ will cause the data to be decoded and stored in the outputs of the addressed digit. The shift register and control logic are reset, causing DATA ACCEPTED to return high, and leaving the chip ready to accept data for the next digit.

Note that for the ICM7232 the eleventh clock resets the shift register and control logic, but the DATA ACCEPTED Output goes low after the eighth clock. This allows the user to abbreviate the data to eight bits, which will write the correct character to the 7-segment display, but will leave the annunicators off, as shown in Figure 16.

If only AN2 is to be turned on, nine bits are clocked in; if AN1 is to be turned on, all ten bits are used.

In the ICM7234, nine bits are always required; the control logic is similar, but allows only a $\overline{\text{WRITE}}$ (DATA ACCEPTED Low) with nine bits entered in the shift register, as shown in Figure 17.

The DATA ACCEPTED Output will drive one low-power Schottky TTL input, and has equal current drive capability pulling high or low.

Note that in the serial input devices, it is possible to address digits which don't exist. Tables 2 and 5 show that when an incorrect address is applied together with a $\overline{\text{WRITE}}$ pulse, none of the outputs will be changed.

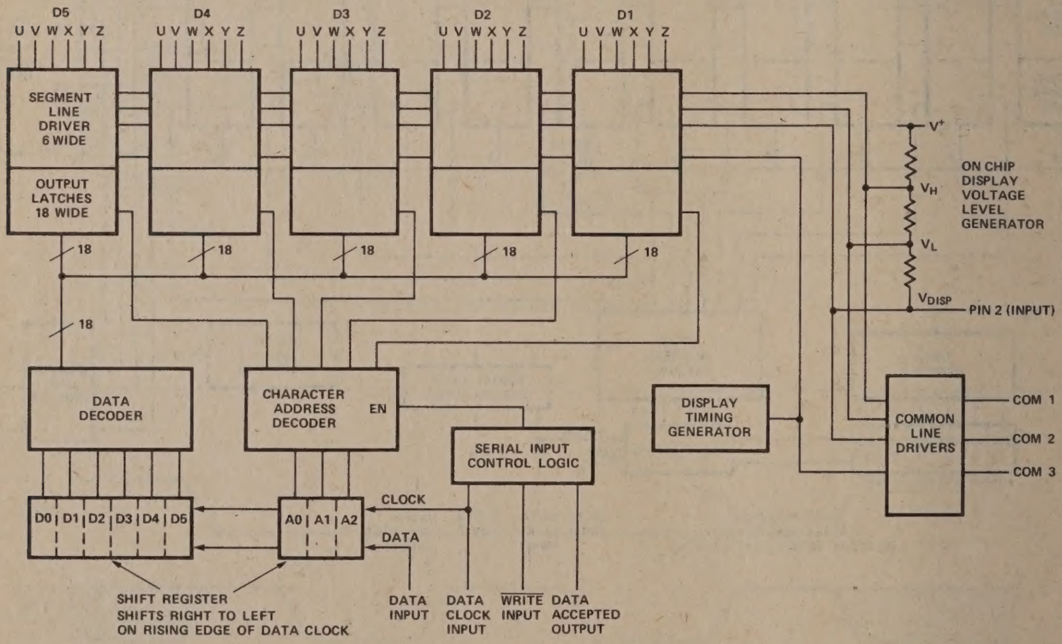

D5
D4
D3
D2
D1
U V W X Y Z
SEGMENT LINE DRIVER 6 WIDE
OUTPUT LATCHES 18 WIDE
18
V+
ON CHIP DISPLAY VOLTAGE LEVEL GENERATOR
VH
VL
VDISP
PIN 2 (INPUT)
DATA DECODER
CHARACTER ADDRESS DECODER
EN
SERIAL INPUT CONTROL LOGIC
DISPLAY TIMING GENERATOR
COMMON LINE DRIVERS
COM 1
COM 2
COM 3
D0 D1 D2 D3 D4 D5
A0 A1 A2
CLOCK
DATA
SHIFT REGISTER SHIFTS RIGHT TO LEFT ON RISING EDGE OF DATA CLOCK
DATA INPUT
DATA CLOCK INPUT
WRITE INPUT
DATA ACCEPTED OUTPUT

Figure 14. ICM7234 Block Diagram

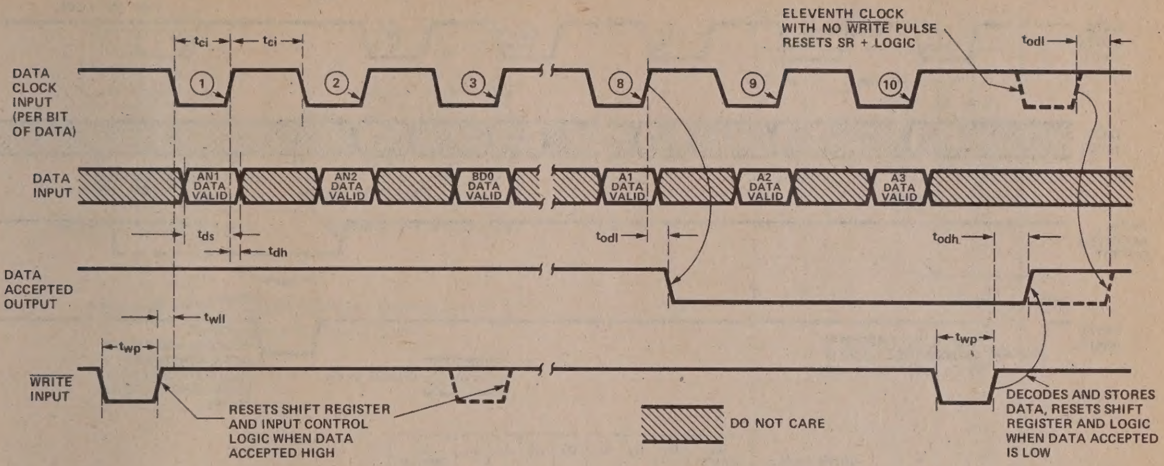

ELEVENTH CLOCK WITH NO WRITE PULSE RESETS SR + LOGIC
tci
tci
todl
DATA CLOCK INPUT (PER BIT OF DATA)
1
2
3
8
9
10
DATA INPUT
AN1 DATA VALID
AN2 DATA VALID
BD0 DATA VALID
A1 DATA VALID
A2 DATA VALID
A3 DATA VALID
tds
tdh
todl
todh
DATA ACCEPTED OUTPUT
twll
twp
twp
WRITE INPUT
RESETS SHIFT REGISTER AND INPUT CONTROL LOGIC WHEN DATA ACCEPTED HIGH
DO NOT CARE
DECODES AND STORES DATA, RESETS SHIFT REGISTER AND LOGIC WHEN DATA ACCEPTED IS LOW

Figure 15. ICM7232 One Digit Input Timing Diagram, Writing Both Annunicators

AN1 ENTER FIRST	AN2	BD0	BD1	BD2	BD3	A_0	A_1	A_2	A_3 ENTER LAST

ICM7232 WRITE ORDER

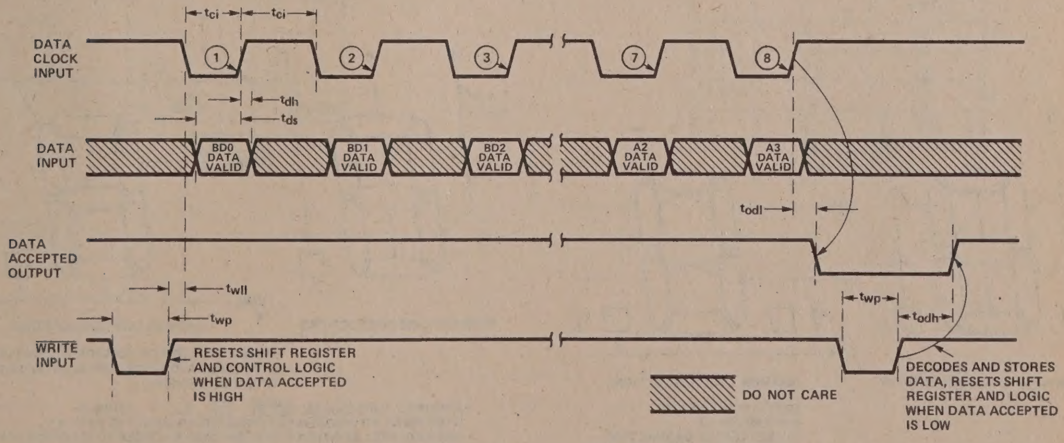
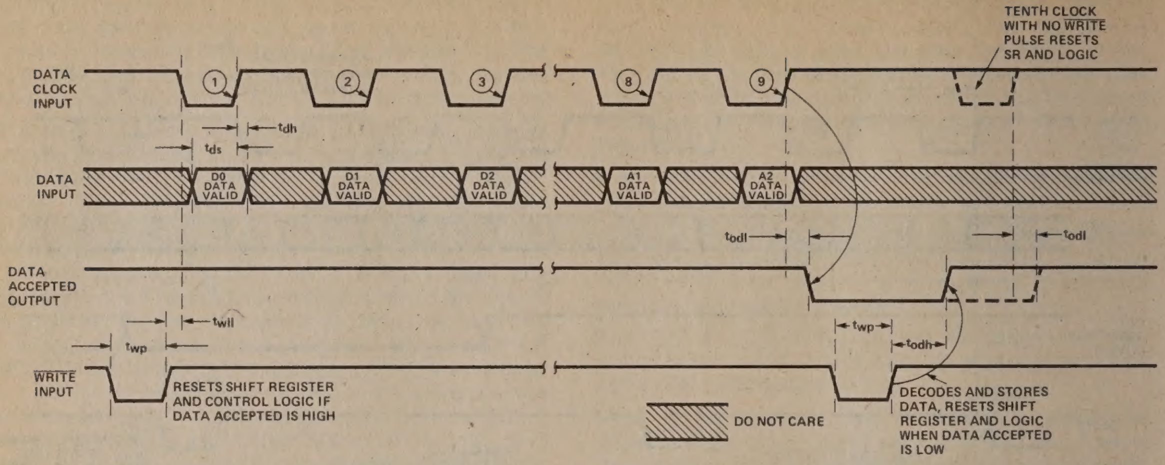

tci
tci
DATA CLOCK INPUT
1
2
3
7
8
tdh
tds
DATA INPUT
BD0 DATA VALID
BD1 DATA VALID
BD2 DATA VALID
A2 DATA VALID
A3 DATA VALID
todl
DATA ACCEPTED OUTPUT
twll
twp
twp
todh
WRITE INPUT
RESETS SHIFT REGISTER AND CONTROL LOGIC WHEN DATA ACCEPTED IS HIGH
DO NOT CARE
DECODES AND STORES DATA, RESETS SHIFT REGISTER AND LOGIC WHEN DATA ACCEPTED IS LOW

Figure 16. ICM7232 Input Timing Diagram, Leaving Both Annunciators OFF


TENTH CLOCK WITH NO WRITE PULSE RESETS SR AND LOGIC
DATA CLOCK INPUT
1
2
3
8
9
tdh
tds
DATA INPUT
D0 DATA VALID
D1 DATA VALID
D2 DATA VALID
A1 DATA VALID
A2 DATA VALID
todl
todl
DATA ACCEPTED OUTPUT
twll
twp
twp
todh
WRITE INPUT
RESETS SHIFT REGISTER AND CONTROL LOGIC IF DATA ACCEPTED IS HIGH
DO NOT CARE
DECODES AND STORES DATA, RESETS SHIFT REGISTER AND LOGIC WHEN DATA ACCEPTED IS LOW

WRITE ORDER	D_0 WRITE FIRST	D_1	D_2	D_3	D_4	D_5	A_0	A_1	A_2 WRITE LAST

Figure 17. ICM7234 One Character Input Timing Diagram

DISPLAY FONTS AND OUTPUT CODES

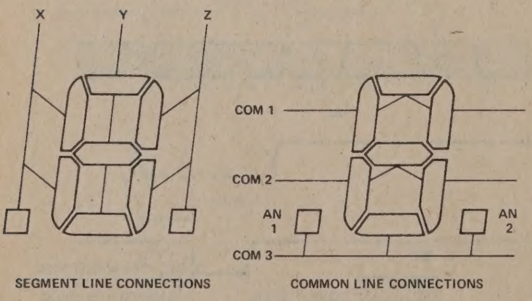
The standard versions of the ICM7231 and ICM7232 chips are programmed to drive a 7-segment display plus two annunciators per digit.

The "A" and "B" suffix chips place both annunciators on COM3. The display connections for one digit of this display are shown in Figure 18. The "A" devices decode the input data into a hexadecimal 7-segment output, while the "B" devices supply Code B outputs (see Table 1).

The "C" devices place the left hand annunciator on COM1 (AN2) and the right hand annunciator (usually a decimal point) on COM3 (AN1) (see Figure 19). The "C" devices provide only a "Code B" output for the 7-segments.

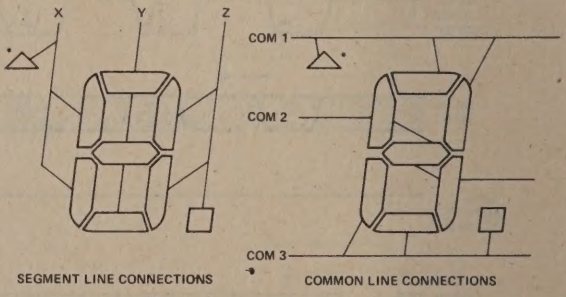
See Table 3 for annunicator input controls. The ICM7233 and ICM7234 are supplied in an "A" version only. The layout for a single character is shown in Figure 20 with output decoding shown in Table 4.

The data decoder is mask programmable. For larger quantity orders (10,000 and up) custom decoder programs can be arranged. Contact the factory for details.


X
Y
Z
COM 1
COM 2
AN 1
AN 2
COM 3
SEGMENT LINE CONNECTIONS
COMMON LINE CONNECTIONS

BOTH ANNUNCIATORS ON COMMON #3 (AT BOTTOM OF CHARACTER) ("A" AND "B" SUFFIX VERSIONS)

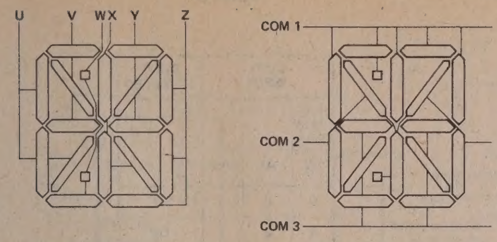
Figure 18. ICM7231 and ICM7232 Display Fonts ("A" and "B" Suffix Versions)


X
Y
Z
COM 1
COM 2
COM 3
*
SEGMENT LINE CONNECTIONS
COMMON LINE CONNECTIONS

LH ANNUNCIATOR ON COMMON #1 (TOP) (AN 2)
RH ANNUNCIATOR ON COMMON #3 (BOTTOM) (AN 1)
"C" SUFFIX DEVICES

*ANNUNCIATORS CAN BE: STOP , GO , △, ↑ - ARROWS THAT POINT TO INFORMATION PRINTED AROUND THE DISPLAY OPENING, ETC., WHATEVER THE DESIGNER CHOOSES TO INCORPORATE IN THE LIQUID CRYSTAL DISPLAY.

Figure 19. ICM7231 and ICM7232 Display Fonts ("C" Suffix Versions)



SEGMENT LINE CONNECTIONS

COMMON LINE CONNECTIONS

Figure 20. ICM7233 and ICM7234 Display Font (18-Segment Alphanumeric)

Table 1

CODE INPUT				DISPLAY OUTPUT	
BD 3	BD 2	BD 1	BD 0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

BINARY DATA DECODING (ICM7231/32)

Table 2

CODE INPUT				DISPLAY OUTPUT
ICM 7232 ONLY A3	A2	A1	A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

ADDRESS DECODING (ICM7231/32)

Table 3

CODE INPUT		DISPLAY OUTPUT	
AN 2	AN 1	ICM7231 A/B ICM7232 A/B BOTH ANNUNCIATORS ON COM 3	ICM7231C ICM7232C LH ANNUNCIATOR COM 1 RH ANNUNCIATOR COM 3
0	0	8	8
0	1	.8	8.
1	0	8.	˙8
1	1	.8.	˙8.

ANNUNCIATOR DECODING

Table 4

CODE INPUT				DISPLAY OUTPUT D5, D4			
D3	D2	D1	D0	0, 0	0, 1	1, 0	1, 1
0	0	0	0	@	P		0
0	0	0	1	A	Q	!	1
0	0	1	0	B	R	"	2
0	0	1	1	C	S	#	3
0	1	0	0	D	T	$	4
0	1	0	1	E	U	%	5
0	1	1	0	F	V	&	6
0	1	1	1	G	W	'	7
1	0	0	0	H	X	(	8
1	0	0	1	I	Y	)	9
1	0	1	0	J	Z	*	:
1	0	1	1	K	[	+	;
1	1	0	0	L	\	,	<
1	1	0	1	M	]	−	=
1	1	1	0	N	↑	.	>
1	1	1	1	O	←	/	?

DATA DECODING
6 - BIT ASCII → 18 SEGMENT
(ICM7233/34)

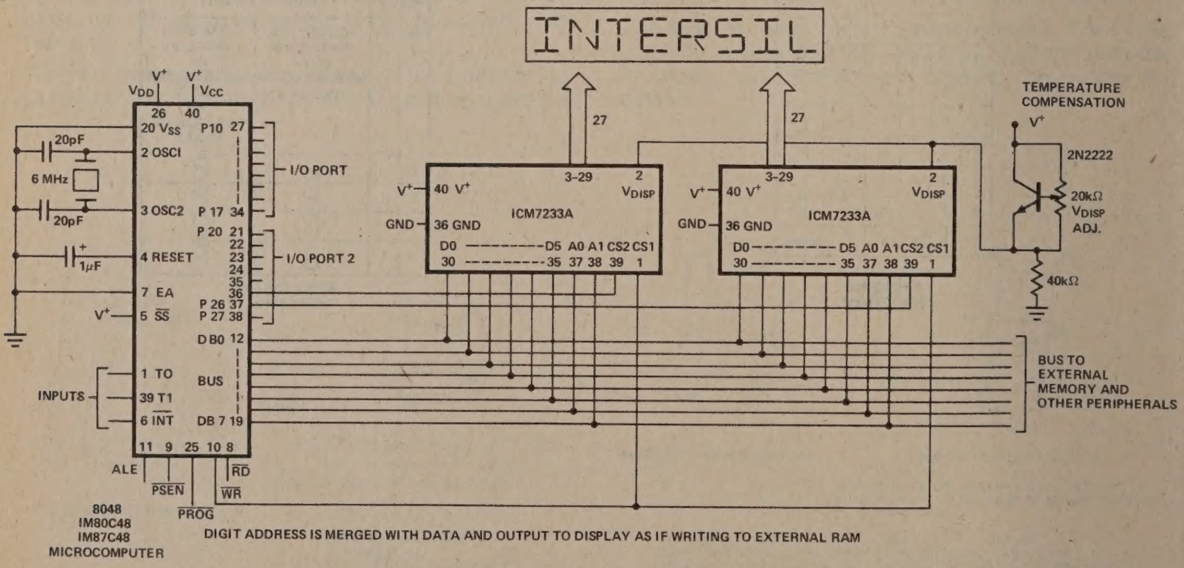
Table 5

CODE INPUT			DIGIT SELECTED
ICM 7234 ONLY			
A2	A1	A0	
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5
1	0	1	NONE
1	1	0	NONE
1	1	1	NONE

ADDRESS
DECODING
(ICM7233/34)

APPLICATIONS

Figures 21 and 22 show typical applications for the ICM7231-34 family.


INTERSIL
27
27
TEMPERATURE COMPENSATION
V+
2N2222
20kΩ VDISP ADJ.
40kΩ
V+ V+
VDD VCC
26 40
20 VSS
P10 27
2 OSC1
20pF
6 MHz
20pF
3 OSC2
P 17 34
I/O PORT
P 20 21
22
23
24
35
36
37
38
I/O PORT 2
4 RESET
1μF
7 EA
V+ 5 SS
P 26
P 27
DB0 12
BUS
DB 7 19
INPUTS
1 TO
39 T1
6 INT
11 9 25 10 8
ALE
PSEN
PROG
RD
WR
8048
IM80C48
IM87C48
MICROCOMPUTER
V+ 40 V+
GND 36 GND
3-29
2 VDISP
ICM7233A
D0 D5 A0 A1 CS2 CS1
30 35 37 38 39 1
BUS TO EXTERNAL MEMORY AND OTHER PERIPHERALS

DIGIT ADDRESS IS MERGED WITH DATA AND OUTPUT TO DISPLAY AS IF WRITING TO EXTERNAL RAM

Figure 21. 8048/IM80C48 Microcomputer with 8 Character 16 Segment Full ASCII Triplex Liquid Crystal Display

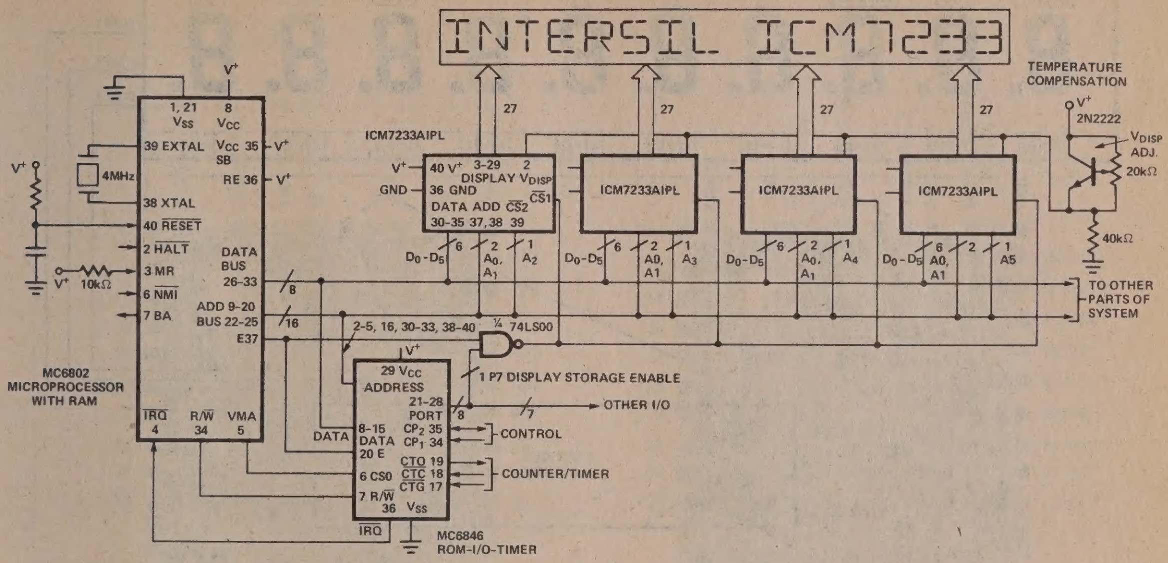

INTERSIL ICM7233
TEMPERATURE COMPENSATION
V+
2N2222
VDISP ADJ.
20kΩ
40kΩ
27
ICM7233AIPL
40 V+ 3-29 2
DISPLAY VDISP
36 GND
DATA ADD CS2 CS1
30-35 37,38 39
V+
GND
Do-D5 6
A0, A1 2
A2 1
A3
A4
A5
TO OTHER PARTS OF SYSTEM
1, 21 VSS
8 VCC
39 EXTAL
VCC SB 35
RE 36
4MHz
38 XTAL
40 RESET
2 HALT
3 MR
6 NMI
7 BA
10kΩ
DATA BUS 26-33
ADD BUS 9-20 22-25
E37
8
16
IRQ 4
R/W 34
VMA 5
MC6802 MICROPROCESSOR WITH RAM
2-5, 16, 30-33, 38-40
¼ 74LS00
29 VCC
ADDRESS
21-28 PORT
1 P7 DISPLAY STORAGE ENABLE
OTHER I/O
7
DATA
8-15 DATA
20 E
6 CS0
7 R/W
36 VSS
IRQ
CP2 35
CP1 34
CONTROL
CTO 19
CTC 18
CTG 17
COUNTER/TIMER
MC6846 ROM-I/O-TIMER

Figure 22. MC6802 Microprocessor with 16 Character 16 Segment Full ASCII Liquid Crystal Display

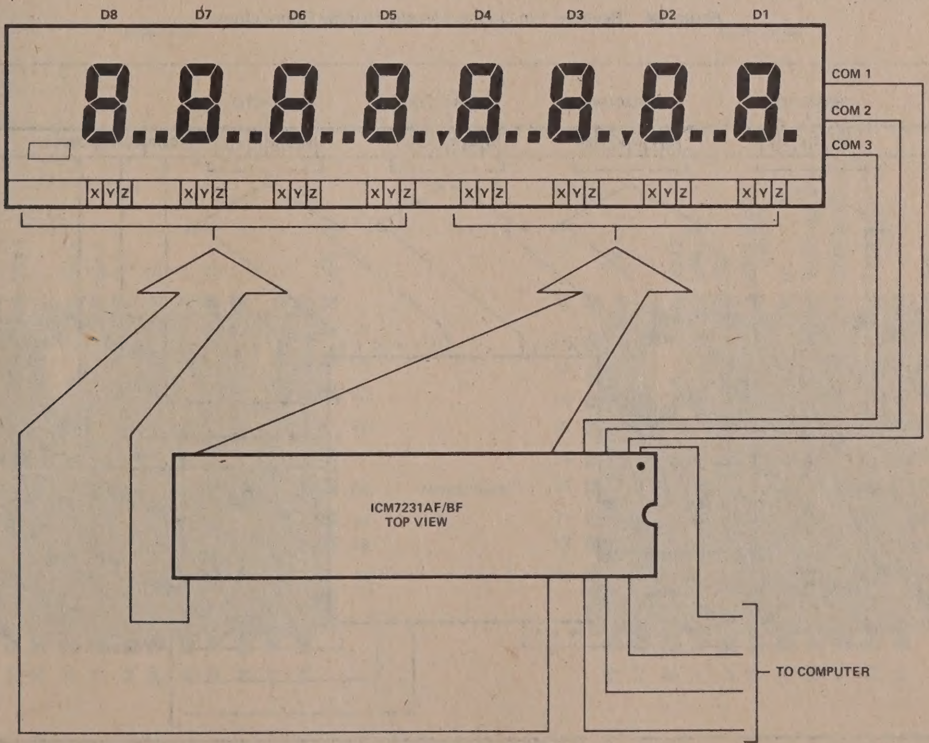

D8
D7
D6
D5
D4
D3
D2
D1
COM 1
COM 2
COM 3
X Y Z
ICM7231AF/BF TOP VIEW
TO COMPUTER

Figure 23. "Forward" Pin Orientation and Display Connections.

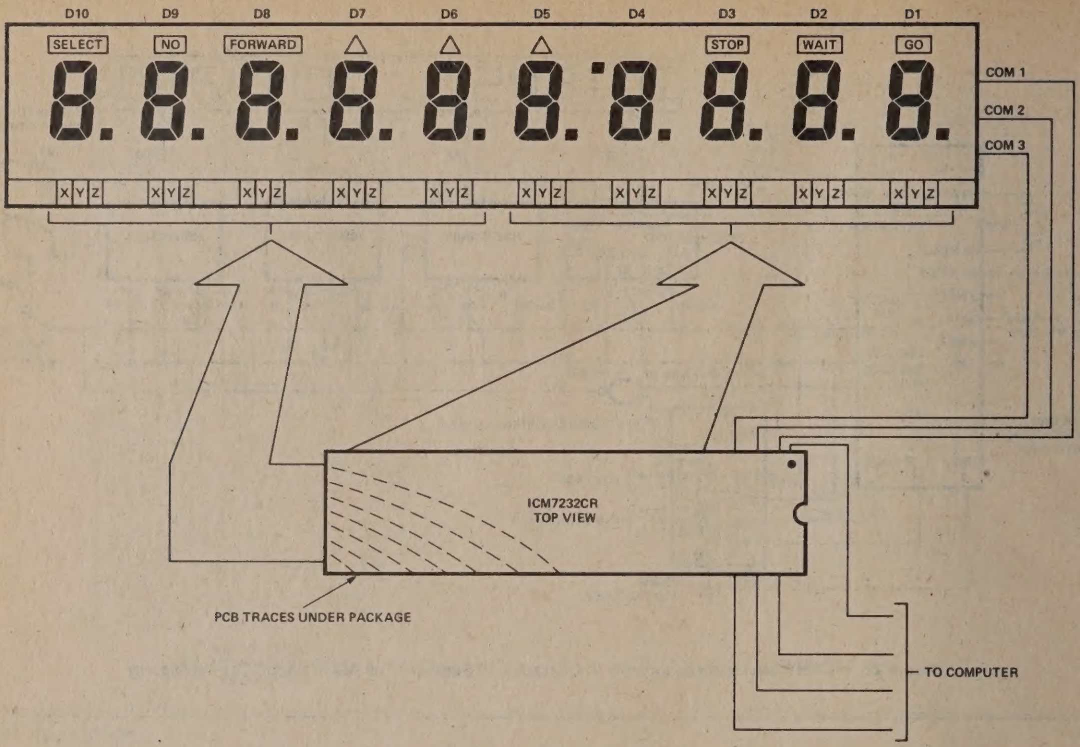

D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
SELECT
NO
FORWARD
STOP
WAIT
GO
COM 1
COM 2
COM 3
X Y Z
ICM7232CR
TOP VIEW
PCB TRACES UNDER PACKAGE
TO COMPUTER

Figure 24. "Reverse" Pin Orientation and Display Connections.

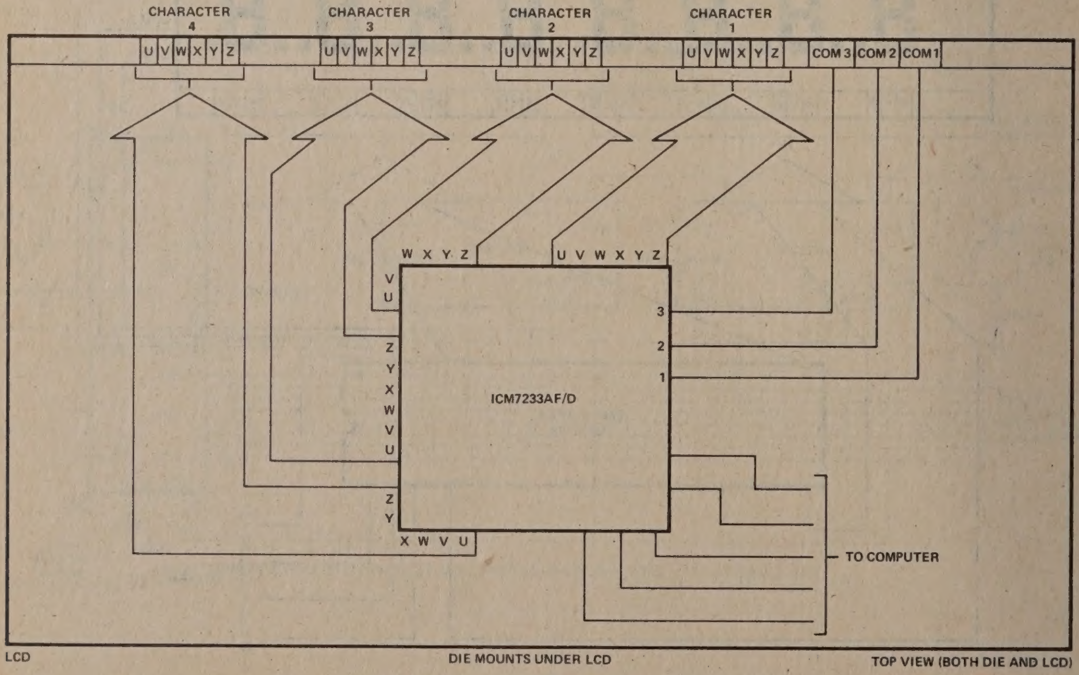
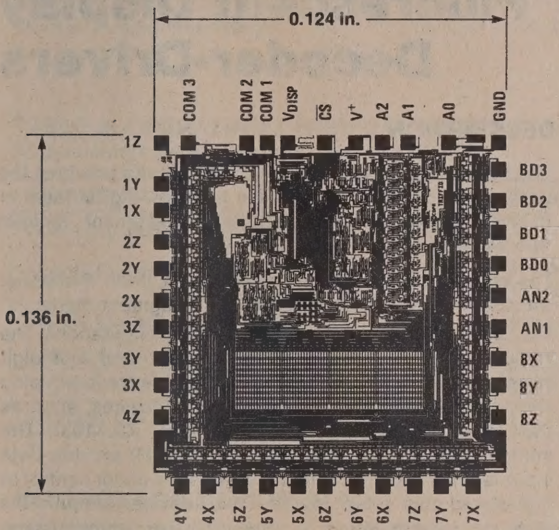
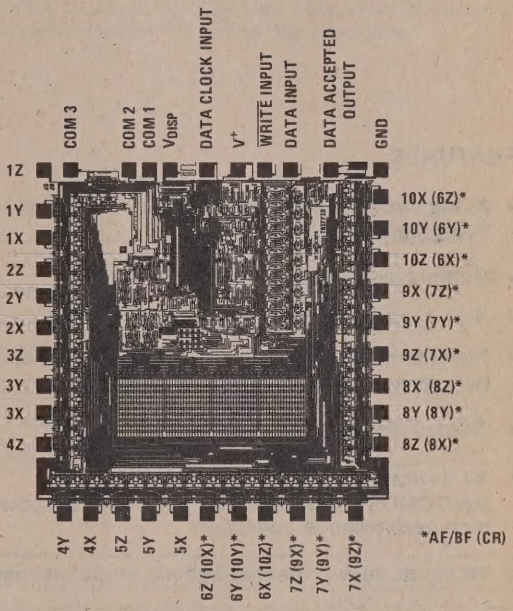

CHARACTER 4
CHARACTER 3
CHARACTER 2
CHARACTER 1
U V W X Y Z
COM 3
COM 2
COM 1
W X Y Z
U V W X Y Z
V
U
3
2
1
Z
Y
X
W
V
U
Z
Y
X W V U
ICM7233AF/D
TO COMPUTER
LCD
DIE MOUNTS UNDER LCD
TOP VIEW (BOTH DIE AND LCD)

Figure 25. "Forward" Die Pad Orientation and Typical Triplex Alphanumeric Display Connections.

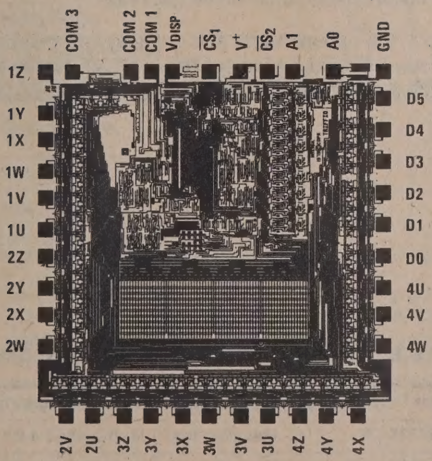
CHIP TOPOGRAPHY


0.124 in.
0.136 in.
COM 3
COM 2
COM 1
V_DISP
CS
V+
A2
A1
A0
GND
1Z
1Y
1X
2Z
2Y
2X
3Z
3Y
3X
4Z
BD3
BD2
BD1
BD0
AN2
AN1
8X
8Y
8Z
4Y
4X
5Z
5Y
5X
6Z
6Y
6X
7Z
7Y
7X

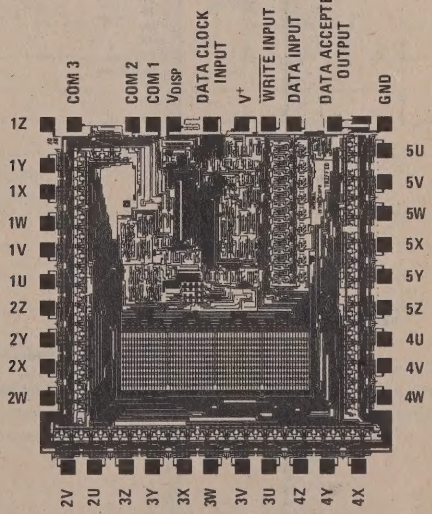
ICM7231


COM 3
COM 2
COM 1
V_DISP
DATA CLOCK INPUT
V+
WRITE INPUT
DATA INPUT
DATA ACCEPTED OUTPUT
GND
1Z
1Y
1X
2Z
2Y
2X
3Z
3Y
3X
4Z
10X (6Z)*
10Y (6Y)*
10Z (6X)*
9X (7Z)*
9Y (7Y)*
9Z (7X)*
8X (8Z)*
8Y (8Y)*
8Z (8X)*
4Y
4X
5Z
5Y
5X
6Z (10X)*
6Y (10Y)*
6X (10Z)*
7Z (9X)*
7Y (9Y)*
7X (9Z)*
*AF/BF (CR)

ICM7232


COM 3
COM 2
COM 1
V_DISP
CS1
V+
CS2
A1
A0
GND
1Z
1Y
1X
1W
1V
1U
2Z
2Y
2X
2W
D5
D4
D3
D2
D1
D0
4U
4V
4W
2V
2U
3Z
3Y
3X
3W
3V
3U
4Z
4Y
4X

ICM7233


COM 3
COM 2
COM 1
V_DISP
DATA CLOCK INPUT
V+
WRITE INPUT
DATA INPUT
DATA ACCEPTED OUTPUT
GND
1Z
1Y
1X
1W
1V
1U
2Z
2Y
2X
2W
5U
5V
5W
5X
5Y
5Z
4U
4V
4W
2V
2U
3Z
3Y
3X
3W
3V
3U
4Z
4Y
4X

ICM7234

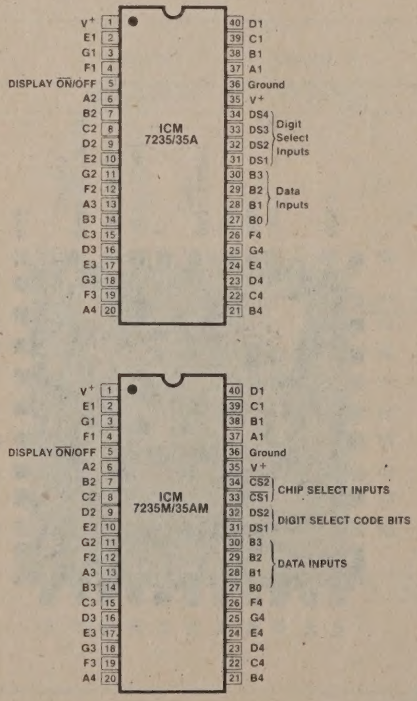
INTERSIL

ICM7235
Four Digit Non-Multiplexed Vacuum Fluorescent Display Decoder-Drivers

FEATURES

- **28 high voltage segment drivers provide four 7-segment digits**
- **Multiplexed BCD input (7235)**
- **High speed processor interface (7235M)**
- **7-segment hex (0-9, A-F) or Code-B (0-9, dash, E, H, L, P, blank) output versions available**
- **Display blanking input**
- **All devices fabricated using high density MAX-CMOS™ LSI technology for very low-power, high-performance operation**
- **All inputs fully protected against static discharge**

PIN CONFIGURATIONS (OUTLINE DRAWING PL)


V+ 1
E1 2
G1 3
F1 4
DISPLAY ON/OFF 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
ICM 7235/35A
40 D1
39 C1
38 B1
37 A1
36 Ground
35 V+
34 DS4
33 DS3
32 DS2
31 DS1
Digit Select Inputs
30 B3
29 B2
28 B1
27 B0
Data Inputs
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4
V+ 1
E1 2
G1 3
F1 4
DISPLAY ON/OFF 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
ICM 7235M/35AM
40 D1
39 C1
38 B1
37 A1
36 Ground
35 V+
34 CS2
33 CS1
CHIP SELECT INPUTS
32 DS2
31 DS1
DIGIT SELECT CODE BITS
30 B3
29 B2
28 B1
27 B0
DATA INPUTS
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4

DESCRIPTION

The ICM7235 family of display driver circuits provides the user with a single chip interface between digital logic or microprocessors to non-multiplexed 7-segment vacuum fluorescent displays.

The chips provide 28 high voltage open drain P-channel transistor outputs organized as four 7-segment digits.

The devices are available with two input configurations. The basic devices provide four data-bit inputs and four digit select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the Intersil ICM7217, ICM7226 and ICL7103. The microprocessor interface devices (suffix M) provide data input latches and digit select code latches under control of high-speed chip select inputs. These devices simplify the task of implementing a cost-effective alphanumeric 7-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices available will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexadecimal output (0-9, A-F). The "A" versions provide the same output code as the ICM7218 Code "B" (0-9, dash, E, H, L, P, blank). Either device will correctly decode true BCD to seven-segment decimal outputs.

All devices in the ICM7235 family are packaged in a standard 40-pin plastic dual-in-line package.

Table 1, the option matrix and ordering information, shows the four standard devices of the ICM7235 family and their markings, which serve as part numbers for ordering purposes.

TABLE 1: OPTION MATRIX AND ORDERING INFORMATION

Order Part Number	Output Code	Input Configuration
ICM7235 IPL	Hexadecimal	Multiplexed 4-Bit
ICM7235A IPL	Code B	Multiplexed 4-Bit
ICM7235M IPL	Hexadecimal	Microprocessor Interface
ICM7235AM IPL	Code B	Microprocessor Interface

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	0.5 W @ +70°C
Supply Voltage (V^+ -Ground)	6.5 Volts
Input Voltage (Note 2)	V^+ +0.3V, Ground −0.3V
Output Voltage (Note 3)	V^+ −35V
Operating Temperature Range	-20°C to +85°C
Storage Temperature Range	−55°C to +125°C

Absolute maximum ratings define stress limitations which, if exceeded, may permanently damage the device. These are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

TABLE 2: OPERATING CHARACTERISTICS

All parameters measured with $V^+ = 5V$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Supply Current	I^+	Measured V^+ to Ground Test circuit; display blank or OFF		10	50	µA
Supply Current	I^+	Measured V^+ to Display			100	mA
Segment OFF Output Voltage	V_{SEG}	$I_{SLK} = 10\mu A$	30			V
Segment OFF Leakage Current	I_{LS}	$V_{SEG} = V^+ - 30V$		0.1	10	µA
Segment ON Current	I_{SEG}	$V_{SEG} = V^+ - 2V$	1.5	2.5		mA

INPUT CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	V_{IH}	Referred to Ground	3			V
Logical "0" Input Voltage	V_{IL}	Referred to Ground			1.5	V
Input Leakage Current	I_{ILK}	Pins 27-34		±0.1	±1	µA
Input Capacitance	C_{IN}	Pins 27-34		5		pF
ON/OFF Input Leakage	$I_{ILK(ON/OFF)}$	All Devices		±0.1	±1	µA
ON/OFF Input Capacitance	$C_{IN(ON/OFF)}$	All Devices		200		pF
AC CHARACTERISTICS — MULTIPLEXERD INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1			µs
Data Setup Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		200			ns
Inter-Digit Select Time	t_{ids}		2			µs
AC CHARACTERISTICS — MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{csa}	Other chip select either held active, or both driven together	200			ns
Data Setup Time	t_{dsm}		100			ns
Data Hold Time	t_{dhm}		10	0		ns
Inter-Chip Select Time	t_{ics}		2			µs

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any input terminal to a voltage in excess of V^+ or ground may cause destructive device latch-up. For this reason, it is recommended that inputs from external sources operating on a different power supply be applied only after the device's own power supply has been established, and that on multiple supply systems the supply to the ICM7235 be turned on first.

NOTE 3: This value refers to the display outputs only.

INPUT DEFINITIONS

In this table, V^+ and ground are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 2. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V^+ = Logical One Ground = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logical One Ground = Logical Zero	Twos	
B2	29	V^+ = Logical One Ground = Logical Zero	Fours	
B3	30	V^+ = Logical One Ground = Logical Zero	Eights (Most Significant)	
$\overline{\text{ON}}$/OFF	5	V^+ = OFF, Ground = ON		Display ON/OFF Input

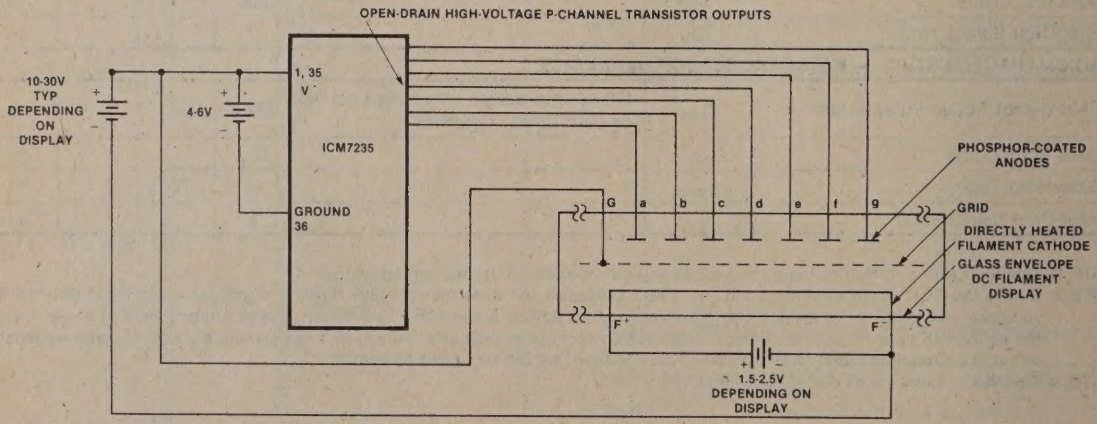
ICM7235, ICM7235A
MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	CONDITION	FUNCTION
D1	31	V^+ = Active Ground = Inactive	D1 (Least Significant) Digit Select
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 (Most Significant) Digit Select

ICM7235M, ICM7235AM
MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	CONDITION	FUNCTION
DS1	Digit Select Code Bit 1 (LSB)	31	V^+ = Logical One Ground = Logical Zero	DS2 & DS1 serve as a two-bit Digit Select Code Input DS2, DS1 = 00 selects D4 DS2, DS1 = 01 selects D3 DS2, DS1 = 10 selects D2 DS2, DS1 = 11 selects D1
DS2	Digit Select Code Bit 2 (MSB)	32		
$\overline{\text{CS1}}$	Chip Select 1	33	V^+ = Inactive Ground = Active	When **both** $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ are taken to ground, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of **either** Chip Select, the data is decoded and written into the output latches.
$\overline{\text{CS2}}$	Chip Select 2	34		

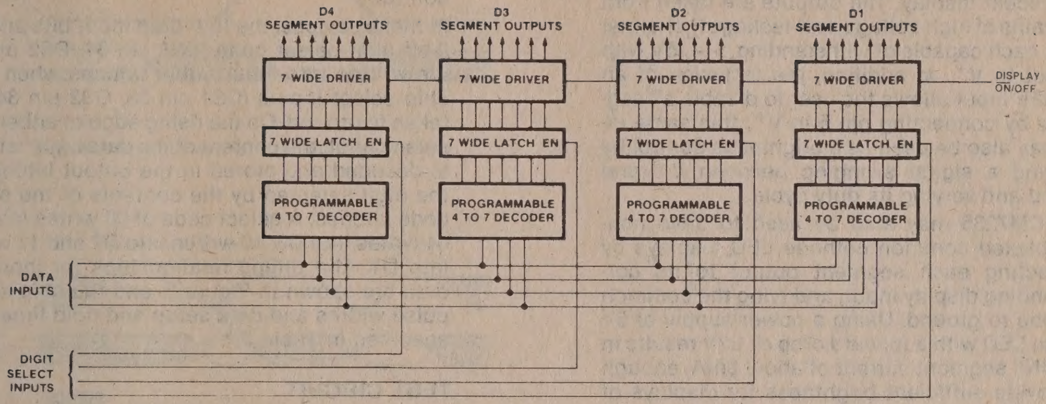
ICM 7235 TYPICAL DC VACUUM FLUORESCENT DISPLAY CONNECTION


OPEN-DRAIN HIGH-VOLTAGE P-CHANNEL TRANSISTOR OUTPUTS
10-30V TYP DEPENDING ON DISPLAY
+
−
4-6V
+
−
1, 35
V+
ICM7235
GROUND
36
G
a
b
c
d
e
f
g
PHOSPHOR-COATED ANODES
GRID
DIRECTLY HEATED FILAMENT CATHODE
GLASS ENVELOPE
DC FILAMENT DISPLAY
F+
F−
+
−
1.5-2.5V DEPENDING ON DISPLAY

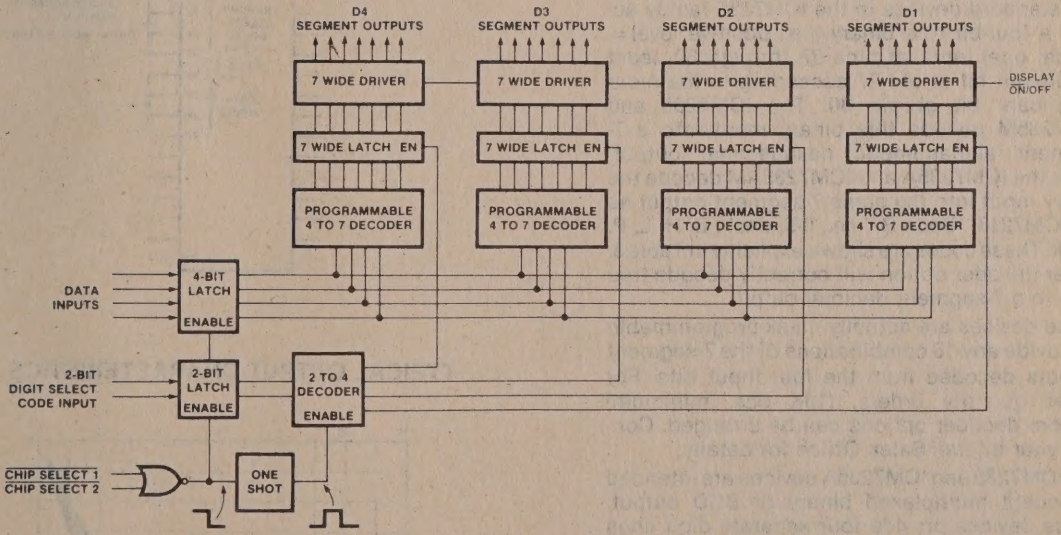
VACUUM FLUORESCENT DISPLAYS (4 DIGIT):

1. NEC Electron, Inc.
   3120 Central Expressway
   Santa Clara, CA 95051
   Tel. (408) 241-8222
   Model FIP 4F8S

ICM7235/35A


D4
SEGMENT OUTPUTS
D3
SEGMENT OUTPUTS
D2
SEGMENT OUTPUTS
D1
SEGMENT OUTPUTS
7 WIDE DRIVER
DISPLAY ON/OFF
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUTS
DIGIT SELECT INPUTS

ICM7235M/35AM


D4
SEGMENT OUTPUTS
D3
SEGMENT OUTPUTS
D2
SEGMENT OUTPUTS
D1
SEGMENT OUTPUTS
7 WIDE DRIVER
DISPLAY ON/OFF
7 WIDE LATCH EN
PROGRAMMABLE 4 TO 7 DECODER
DATA INPUTS
4-BIT LATCH
ENABLE
2-BIT DIGIT SELECT CODE INPUT
2-BIT LATCH
ENABLE
2 TO 4 DECODER
ENABLE
CHIP SELECT 1
CHIP SELECT 2
ONE SHOT

CIRCUIT DESCRIPTION

Each device in the ICM7235 family provides signals for directly driving the anode-terminals of a four-digit, 7-segment non-multiplexed vacuum fluorescent display. The outputs are taken from the drains of high-voltage, low-leakage P-channel FETs, each capable of withstanding > −35V with respect to V⁺. In addition, the inclusion of an ON/OFF input allows the user to disable all segments by connecting pin 5 to V⁺; this same input may also be used as a brightness control by applying a signal swinging between V⁺ and ground and varying its duty cycle.

The ICM7235 may also be used to drive non-multiplexed common cathode LED displays by connecting each segment output to its corresponding display input, and tying the common cathode to ground. Using a power supply of 5V and an LED with a forward drop of 1.7V results in an "ON" segment current of about 3mA, enough to provide sufficient brightness for displays of up to 0.3" character height.

Note that these devices have two V⁺ terminals; each should be connected to the positive supply voltage. This double connection is necessary to minimize the effects of bond wire resistance, which could be a problem due to the high display currents.

Input Configurations and Output Codes

The standard devices in the ICM7235 family accept a four-bit true binary (i.e., positive level = logical one) input at pins 27 through 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7235 and ICM7235M decode this binary input into a 7-segment alphanumeric hexadecimal output, while the ICM7235A and ICM7235AM decode the binary input into the same 7-segment output as the ICM7218 "Code B," i.e., 0-9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 3. Either decoder option will correctly decode true BCD to a 7-segment decimal output.

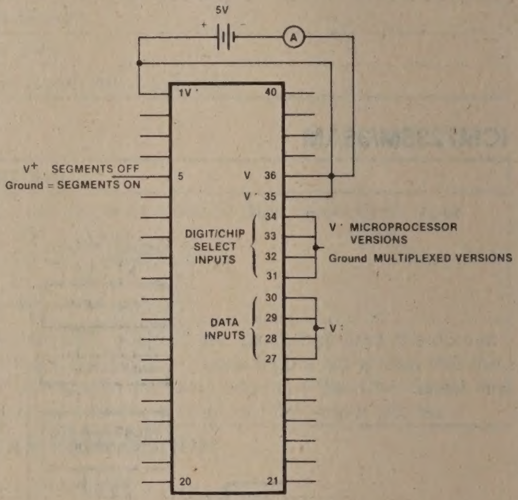
These devices are actually mask-programmable to provide any 16 combinations of the 7-segment outputs decoded from the four input bits. For larger quantity orders, (10K pcs. minimum) custom decoder options can be arranged. Contact your Intersil Sales Office for details.

The ICM7235 and ICM7235A devices are intended to accept multiplexed binary or BCD output. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30. More than one digit select may be activated simultaneously (which will write the same character into all selected digits), although the timing requirements shown in Figure 2 and Table 2 for data setup, hold, and inter-digit select times must be met to ensure correct output.

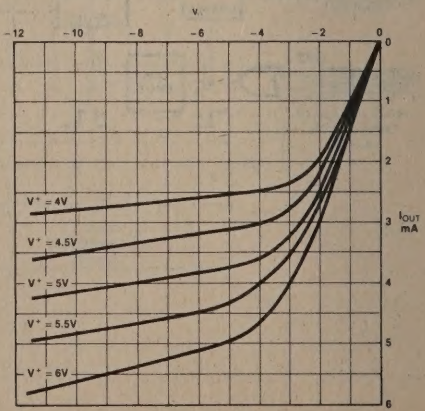
The ICM7235M and AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the 2-bit digit select code (DS1 pin 31, DS2 pin 32) are written into input buffer latches when both chip select inputs (CS1 pin 33, CS2 pin 34) are taken to ground. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the select code latches. A select code of 00 writes into D4, 01 writes into D3, 10 writes into D2 and 11 writes into D1. The timing relationships for inputting data are shown in Figure 3, and the chip select pulse widths and data setup and hold times are specified in Table 2.

TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS



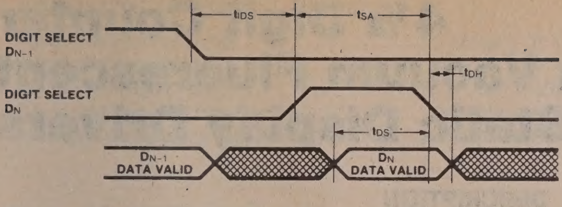

tIDS
tSA
DIGIT SELECT
DN-1
tDH
DIGIT SELECT
DN
tDS
DN-1
DATA VALID
DN
DATA VALID

Figure 2. Multiplexed Input Timing Diagram

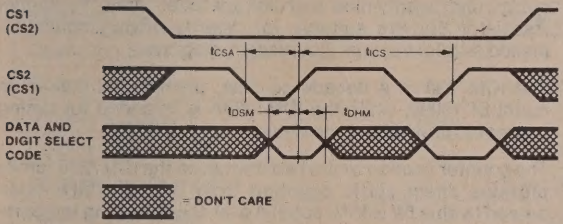

CS1
(CS2)
tCSA
tICS
CS2
(CS1)
tDSM
tDHM
DATA AND
DIGIT SELECT
CODE
= DON'T CARE

Figure 3. Microprocessor Interface Input Timing Diagram

SEGMENT ASSIGNMENT

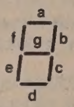


Table 3 Output Codes

BINARY				HEXADECIMAL	CODE B
B3	B2	B1	B0	ICM7235 ICM7235M	ICM7235A ICM7235AM
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

INTERSIL

ICM7236
4½ Digit Counter With Vacuum Fluorescent Static Display Drivers

FEATURES

- **High frequency counting — guaranteed 15MHz, typically 25MHz at 5V**
- **Low power operation — less than 100μW quiescent**
- **Direct 4½ digit seven-segment display drive for non-multiplexed vacuum fluorescent displays**
- **Store and Reset inputs permit operation as frequency or period counter**
- **True count inhibit disables first counter stage**
- **Carry output for cascading four-digit blocks**
- **Schmitt-trigger on count input allows operation in noisy environments or with slowly changing inputs**
- **Leading zero blanking input and output for correct leading zero blanking with cascaded devices**
- **All inputs fully protected against static discharge — no special handling precautions necessary**
- **Devices fabricated using MAXCMOS™ process for high-performance, low power operation**

DESCRIPTION

The ICM7236 and ICM7236A devices are high-performance CMOS 4½ digit counters, including decoders, output latches, count inhibit, reset, and leading zero blanking circuitry, and twenty-nine high-voltage open drain P-channel transistor outputs suitable for directly driving non-multiplexed (static) vacuum fluorescent displays.

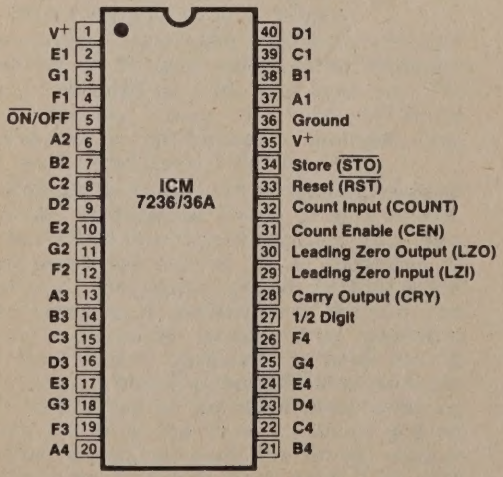
The ICM7236 is a decade counter, providing a maximum count of 19999, while the ICM7236A is intended for timing purposes, providing a maximum count of 15959.

The counter section of the two devices in the ICM7236 family provides direct static counting from DC to 15MHz guaranteed (with a 5V ±10% supply) over the operating temperature range. At normal room temperatures, the device will typically count up to 25MHz. The count input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry which allows a direct interface with the ICM7207 devices to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate features intended to simplify cascading in four-digit blocks. The carry output allows the counter to be cascaded, while the leading zero blanking input and output allow correct leading zero blanking between four-decade blocks.

The ICM7236 and ICM7236A are packaged in a standard 40-pin dual-in-line plastic package.

PIN CONFIGURATION (OUTLINE DRAWING PL)



V+ 1
E1 2
G1 3
F1 4
$\overline{\text{ON}}$/OFF 5
A2 6
B2 7
C2 8
D2 9
E2 10
G2 11
F2 12
A3 13
B3 14
C3 15
D3 16
E3 17
G3 18
F3 19
A4 20
ICM 7236/36A
40 D1
39 C1
38 B1
37 A1
36 Ground
35 V+
34 Store ($\overline{\text{STO}}$)
33 Reset ($\overline{\text{RST}}$)
32 Count Input (COUNT)
31 Count Enable (CEN)
30 Leading Zero Output (LZO)
29 Leading Zero Input (LZI)
28 Carry Output (CRY)
27 1/2 Digit
26 F4
25 G4
24 E4
23 D4
22 C4
21 B4

TABLE 1: ORDERING INFORMATION

ORDER PART NUMBER	COUNT OPTION
ICM7236IPL	19999
ICM7236AIPL	15959

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	0.5 W @ +70°C
Supply Voltage (V^+)	6.5 V
Display Voltage (Note 3)	V^+ −35V
Operating Temperature Range	-20°C to +85°C
Storage Temperature Range	−55°C to +125°C

Absolute maximum ratings define stress limitations which, if exceeded, may permanently damage the device. These are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

TABLE 2: OPERATING CHARACTERISTICS

(All parameters measured with $V^+ = 5V$ unless otherwise indicated.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}	V^+	3	5	6	V
Operating Current	I_{OP}	Test circuit, Display blank		10	50	μA
Display Voltage	V_{DISP}				30	V
Display Output Leakage	I_{DLK}	Output OFF, $V = V^+ - 30V$		0.1	10	μA
Input Pullup Currents	I_P	Pins 29, 31, 33, 34 $V = V^+ - 3V$		10		μA
Input High Voltage	V_{IH}	Pins 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pins 29, 31, 33, 34			2	V
Count Input Threshold	V_{CT}			2		V
Count Input Hysteresis	V_{CH}			0.5		V
Output High Current	I_{OH}	Carry Pin 28, leading zero out Pin 30 $V_{OUT} = V^+ - 3V$.	350	500		μA
Output Low Current	I_{OL}	Carry Pin 28, leading zero out Pin 30 $V_{OUT} = +3V$.	350	500		μA
Count Frequency	f_{count}	$4.5V < V^+ < 6V$	0	25	15	MHz
Store, Reset Minimum Pulse Width	t_S, t_W		3			μs

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than V^+ or less than ground may cause destructive device latch-up. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7236/7236A be turned on first.

NOTE 3: This limit refers to the display output terminals only.

DESCRIPTION OF OPERATION

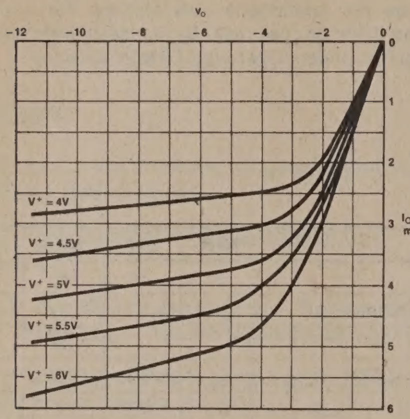
All of the chips in the ICM7236 family provide twenty-nine outputs suitable for directly driving the anode terminals of 4½ digit seven-segment non-multiplexed (static) vacuum-fluorescent displays. Each display output is the drain of a high-voltage low-leakage P-channel transistor, capable of withstanding typically greater than −35 volts with respect to V^+. The output characteristics are shown graphically under "Typical Characteristics."

These chips also provide a dislay $\overline{ON}$/OFF input which may be used to disable all the segment outputs and thus blank the display. This input may also be used to control the display brightness by varying the duty cycle of a signal at the input swinging between V^+ and ground.

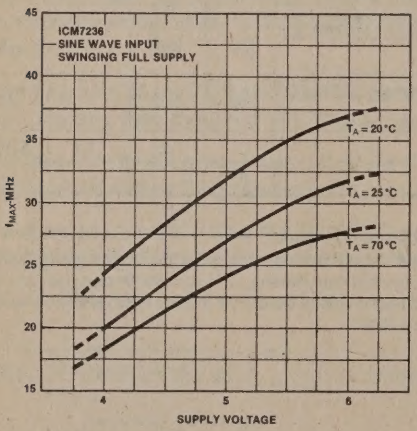
NOTE that these circuits have two terminals for V^+; both of these pins should be connected to the power supply positive terminal. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

These chips may also be used to directly drive non-multiplexed common-cathode LED displays, where each segment of the display is driven by one ICM7236 output, and the common cathode is connected to ground. With a 5V power supply and a 1.7V LED diode forward voltage drop, the current in an "ON" segment will be typically 3mA. This should provide sufficient brightness in displays up to about 0.3" character height.

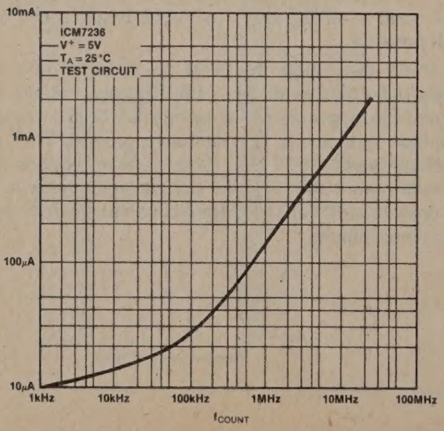
TYPICAL OUTPUT CHARACTERISTICS



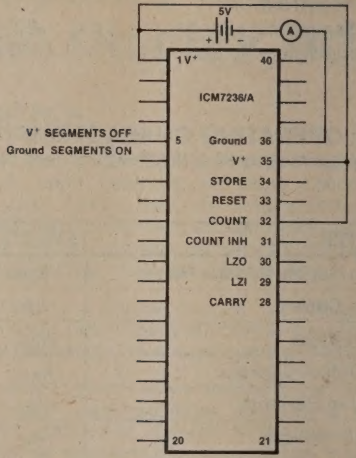
MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE



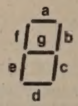
SUPPLY CURRENT AS A FUNCTION OF COUNT FREQUENCY



TEST CIRCUIT


5V
+
−
A
1 V⁺
40
ICM7236/A
V⁺ SEGMENTS OFF
Ground SEGMENTS ON
5
Ground 36
V⁺ 35
STORE 34
RESET 33
COUNT 32
COUNT INH 31
LZO 30
LZI 29
CARRY 28
20
21

SEGMENT ASSIGNMENT



COUNTER SECTION

The devices in the ICM7236 family implement a four-digit ripple-carry resetable counter, including a Schmitt trigger on the COUNT input and a CaRrY output. Also included is an extra D-type flip-flop, clocked by the carry signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the COUNT input, and the CaRrY output will provide a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the ReSet terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent CaRrY outputs will not be affected.

A negative level at the COUNT ENABLE disables the first divide-by-two in the counter chain without affecting its clock. This provides a true **count** inhibit which is not sensitive to the state of the count input, preventing false counts which can result from using a normal logic gate forcing the state of the clock to prevent counting.

Each decade drives directly into a four-to-seven decoder which derives the seven-segment output code. Each decoder output corresponds to the one-segment terminal of the device. The output data is latched at the driver; when the STOre pin is at a negative level, these latches are updated, and when the STO pin is left open or at a poistive level, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Input is floating, or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When the Leading Zero Input is at a negative level, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Output is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked, which can only occur when the Leading Zero Input is at a positive level and the half-digit is not set.

For example, on an eight-decade counter with overflow using two ICM7236 devices, the Leading Zero Output of the high-order digit device would be connected to the Leading Zero Input of the low-order digit device. This will assure correct leading zero blanking for all eight digits.

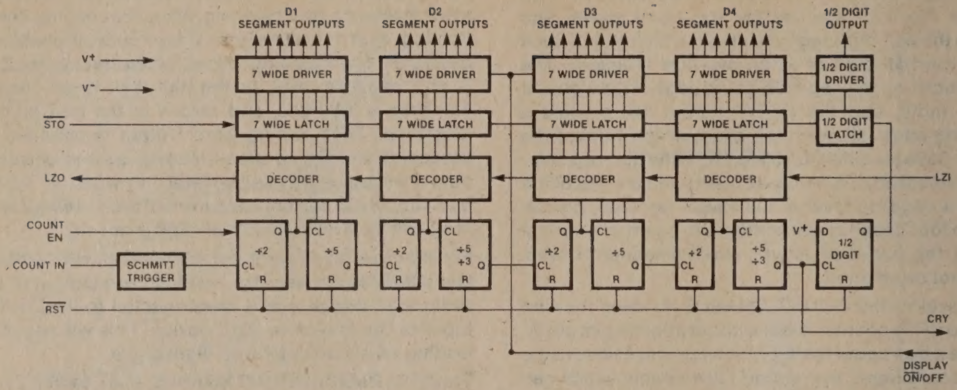
The STO, ReSeT, COUNT ENABLE, and Leading Zero Inputs are provided with pullup devices, so that they may be left open when a positive level is desired. The CaRrY and Leading Zero Outputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7236 devices in four-digit blocks.

CONTROL INPUT DEFINITIONS

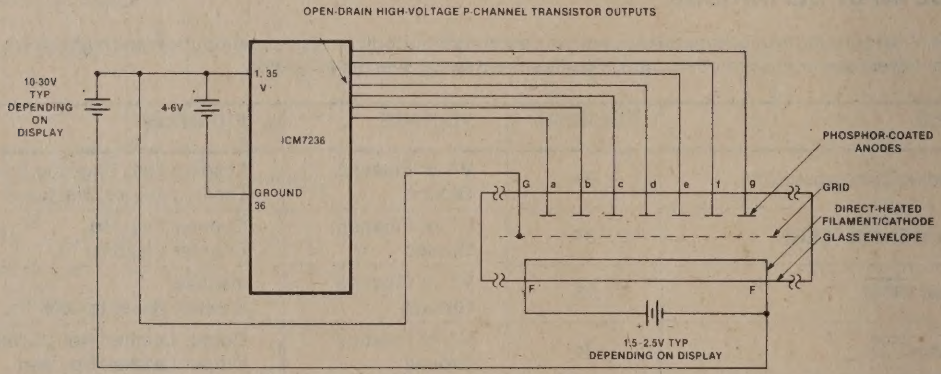
In this table, V+ and ground are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 2. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Input (LZI)	29	V^+ or Floating Ground	Leading Zero Blanking Enabled Leading Zeroes Displayed
Count Enable (CEN)	31	V^+ or Floating Ground	Counter Enabled Counter Disabled
Reset ($\overline{\text{RST}}$)	33	V^+ or Floating Ground	Inactive Counter Reset to 0000
Store ($\overline{\text{STO}}$)	34	V^+ or Floating Ground	Output Latches Not Updated Output Latches Updated
Display $\overline{\text{ON}}$/OFF	5	V^+ Ground	Display Outputs Disabled Display Outputs Enabled

BLOCK DIAGRAM


D1
SEGMENT OUTPUTS
D2
SEGMENT OUTPUTS
D3
SEGMENT OUTPUTS
D4
SEGMENT OUTPUTS
1/2 DIGIT
OUTPUT
V+
V−
STO
LZO
COUNT
EN
COUNT IN
SCHMITT
TRIGGER
RST
7 WIDE DRIVER
7 WIDE LATCH
DECODER
1/2 DIGIT
DRIVER
1/2 DIGIT
LATCH
LZI
÷2
÷5
÷5
÷3
CL
Q
R
V+
D
1/2
DIGIT
CRY
DISPLAY
ON/OFF

TYPICAL DC VACUUM FLUORESCENT DISPLAY CONNECTION


OPEN-DRAIN HIGH-VOLTAGE P-CHANNEL TRANSISTOR OUTPUTS
10-30V
TYP
DEPENDING
ON
DISPLAY
4-6V
1, 35
V-
ICM7236
GROUND
36
G
a
b
c
d
e
f
g
PHOSPHOR-COATED
ANODES
GRID
DIRECT-HEATED
FILAMENT/CATHODE
GLASS ENVELOPE
F
F
1.5-2.5V TYP
DEPENDING ON DISPLAY

VACUUM FLUORESCENT DISPLAYS (4 1/2 DIGIT):

1. NEC Electron, Inc.
   3120 Central Expressway
   Santa Clara, CA 95051
   Tel. (408) 241-8222
   Model FIP 5F8S

ICM7240/50/60 CMOS Programmable Timers/Counters

FEATURES

- **Replaces 8240/50/60, 2240 in most applications**
- **Timing from microseconds to days**
- **May be used as fixed or programmable counter**
- **Programmable with standard thumbwheel switches**
- **Select output count from**
  1RC to 255RC (ICM7240)
  1RC to 99RC (ICM7250)
  1RC to 59RC (ICM7260)
- **Monostable or astable operation**
- **Low supply current: 115μA @ 5 volts**
- **Wide supply voltage range: 2-16 volts**
- **Cascadeable**

GENERAL DESCRIPTION

The ICM7240/50/60 is a family of CMOS Timer/Counter circuits intended to replace Intersil's ICL 8240/50/60 and the 2240 in most applications. Together with the ICM7555/56 (CMOS versions of the SE/NE 555/6), they provide a complete line of RC oscillators/timers/counters offering lower supply currents, wider supply voltage ranges, higher operating frequencies, lower component counts and a wider range of timing components. They are intended to simplify the selection of various time delays or frequency outputs from a fixed RC oscillator circuit.

Each device consists of a counter section, control circuitry, and an RC oscillator requiring an external resistor and capacitor. For counter/divider applications, the oscillator may be inhibited and an input clock applied to the TB terminal. The ICM7240 is intended for straight binary counting or timing, whereas the ICM7250 is optimized for decimal counting or timing. The ICM7260 is specifically designed for time delays in seconds, minutes and hours. All three devices use open drain output transistors, thereby allowing wire AND-ing. Manual programming is easily accomplished by the use of standard thumbwheel switches or hardwired connections. The ICM7240/50/60 are packaged in 16 pin CERDIP packages.

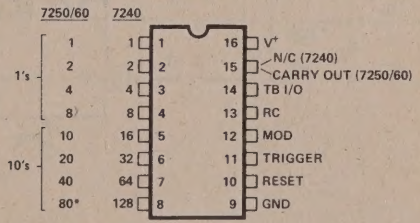
Applications include programmable timing, long delay generation, cascadeable counters, programmable counters, low frequency oscillators, and sequence timing.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7240IJE	-20°C to +85°C	16 Lead CERDIP
ICM7250IJE	-20°C to +85°C	16 Lead CERDIP
ICM7260IJE	-20°C to +85°C	16 Lead CERDIP
ICM7240/D		Dice Only
ICM7250/D		Dice Only
ICM7260/D		Dice Only

PIN CONFIGURATION (OUTLINE DRAWING JE)

ICM7240, 7250, 7260



*7260 OPEN CIRCUIT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Input Voltage[1] Terminals 10,11,12,13,14	GND -0.3V to V+ + 0.3V
Maximum continuous output current (each output)	50 mA
Power Dissipation[2]	200 mW
Operating Temperature Range	-20° C to +85° C
Storage Temperature Range	-55° C to +125° C

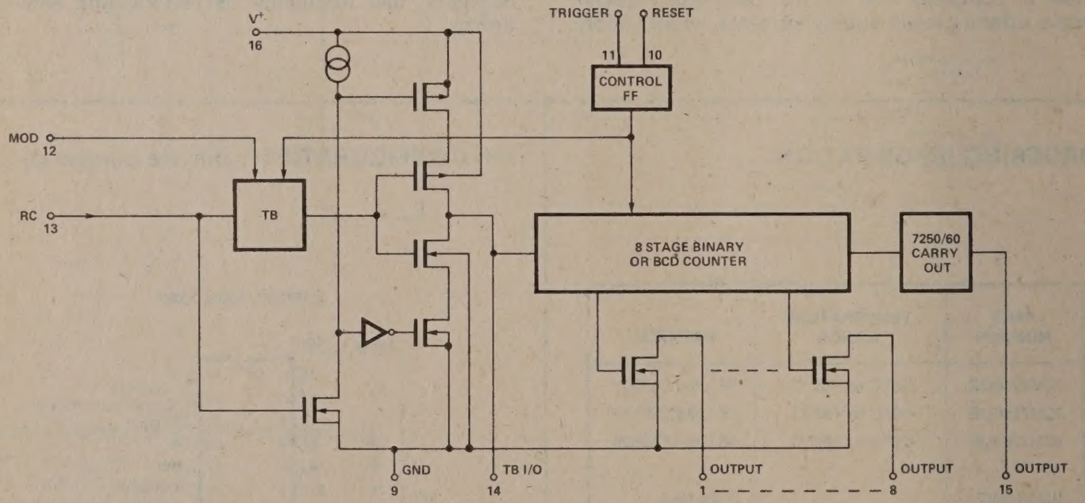
NOTES:

1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7240/50/60 be turned on first.
2. Derate at -2 mW/° C above 25° C.

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM

ICM7240/50/60


V+
16
TRIGGER
RESET
11
10
CONTROL FF
MOD
12
RC
13
TB
8 STAGE BINARY OR BCD COUNTER
7250/60 CARRY OUT
GND
9
TB I/O
14
OUTPUT
1
OUTPUT
8
OUTPUT
15

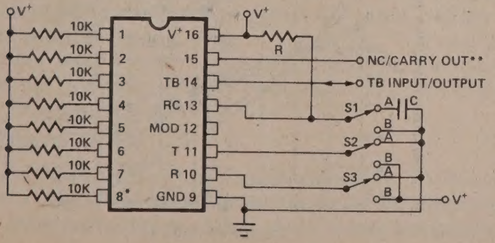
ELECTRICAL CHARACTERISTICS

Each of the three devices utilizes an identical timebase, control flip-flops, and basic counters, with the outputs consisting of open drain n-channel transistors. Only the ICM7250/60 have CARRY outputs.

Test Conditions: Test circuit, $V^+ = 5V$, $T_A = +25°C$, $R = 10K\Omega$, $C = 0.1\mu F$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current	I^+	Reset		125		μA
		Operating, $R = 10K\Omega$, $C = 0.1\mu F$		300	700	μA
		Operating, $R = 1M\Omega$, $C = 0.1\mu F$		120	500	μA
		TB Inhibited, RC Connected to GND		125		μA
Timing Accuracy				5		%
RC Oscillator Frequency Temperature Drift	$\Delta f/\Delta T$	(Exclusive of RC Drift)		250		ppm/° C
Time Base Output Voltage	V_{OTB}	$I_{SOURCE} = 1$ mA	3.5	4.2		V
		$I_{SINK} = 3.2$ mA		0.25	0.6	V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground			25	μA
Mod Voltage Level	V_{MOD}	$V^+ = 5V$		3.5		V
		$V^+ = 15V$		11.0		V
Trigger Input Voltage	V_{TRIG}	$V^+ = 5V$		1.6	2.0	V
		$V^+ = 15V$		3.5	4.5	V
Reset Input Voltage	V_{RST}	$V^+ = 5V$		1.3	2.0	V
		$V^+ = 15V$		2.7	4.0	V
Max Count Toggle Rate 7240	f_t	$V^+ = 2V$ Counter/Divider Mode		1		MHz
		$V^+ = 5V$ Counter/Divider Mode	2	6		MHz
		$V^+ = 15V$ Counter/Divider Mode		13		MHz
		50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND				
Max Counter Toggle Rate 7250, 7260	f_t	$V^+ = 5V$ (Counter/Divider Mode)	1.5	5		MHz
Max Count Toggle Rate 7240, 7250, 7260	f_t	Programmed Timer — Divider Mode			100	KHz
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output $V^+ = 5V$, $I_{OUT} = 3.2$ mA		0.22	0.4	V
Output Leakage Current	I_{OLK}	$V^+ = 5V$, per Output			1	μA
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	$V^+ \leq 5.5V$	1K		22M	Ω
		$V^+ \leq 16V$	1K		22M	Ω

TEST CIRCUIT



S1–A = RC RUN
B = T. B. INPUT RUN

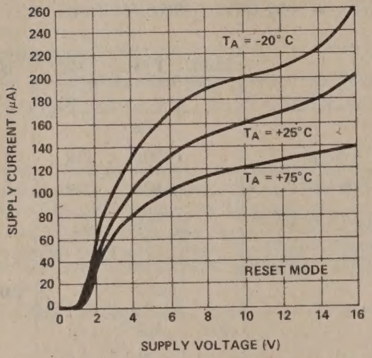
S2–A = INACTIVE
B = TRIGGER

S3–A = INACTIVE
B = RESET

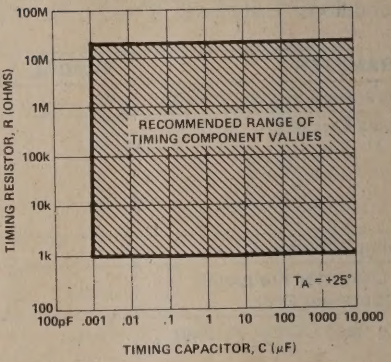
NOTE: S1-B INHIBITS THE TIMEBASE SECTION, ALLOWING TERMINAL 14 TO BECOME THE COUNTER INPUT.
** TERMINAL 15 IS CARRY OUTPUT FOR 7250/60 DEVICES.
* TERMINAL 8 IS OPEN CIRCUIT FOR 7260.

TYPICAL PERFORMANCE CHARACTERISTICS

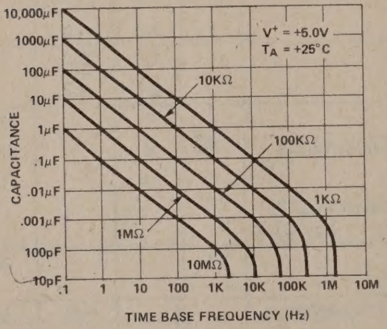
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



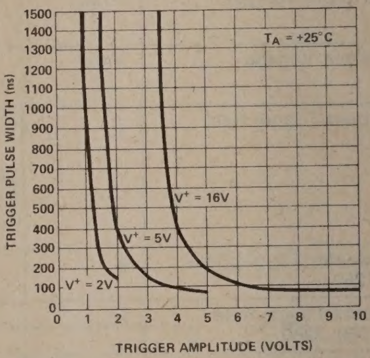
RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



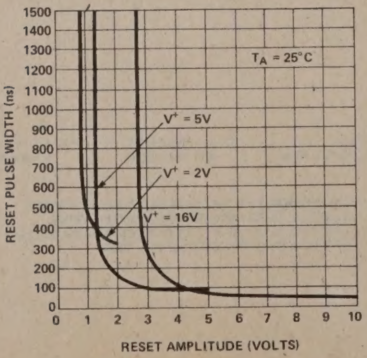
TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



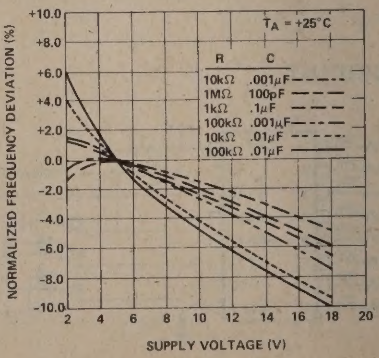
MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



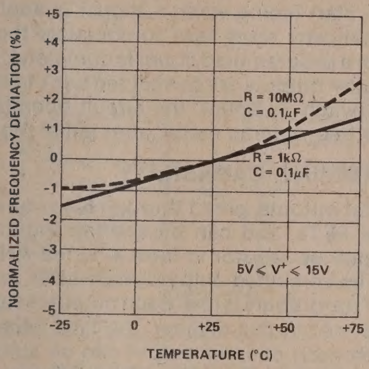
MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



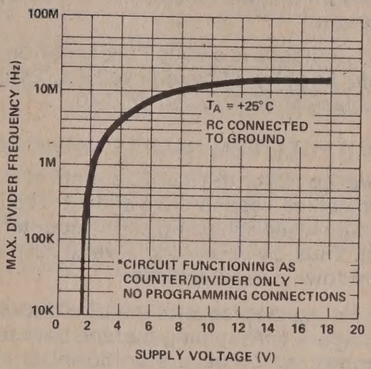
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



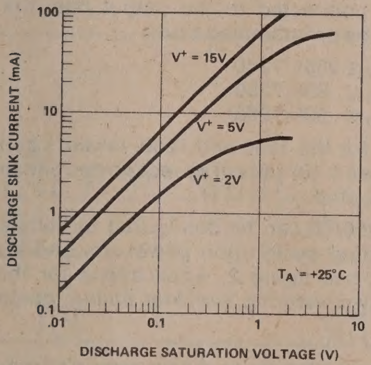
TYPICAL PERFORMANCE CHARACTERISTICS



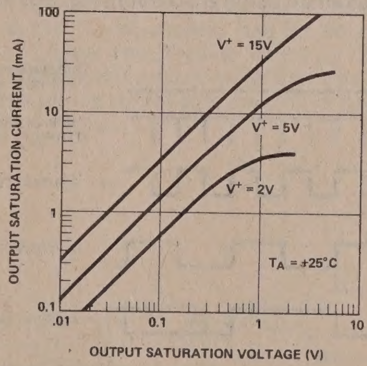
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE*



DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE

DESCRIPTION OF PIN FUNCTIONS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

Each binary counter output is a buffered "open-drain" type. At reset condition, all the counter outputs are at a high, or non-conducting state. After a trigger input or when using the internal timebase, the outputs change state (see timing diagram, Figure 1). If an external clock input is used, the trigger input must overlap at least the first falling edge of the clock. The counter outputs can be used individually, or can be connected together in a wired-AND configuration, as described in the Programming section.

GROUND (PIN 9)

This is the return or most negative supply pin. It should have a very low impedance as the capacitor discharge and other switched currents could create transients.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuits are reset or triggered by positive going control pulses applied to pins 10 and 11, and once triggered they ignore additional trigger inputs until either the timing cycle is completed or a reset signal is applied. If both reset and trigger are applied simultaneously trigger overrides reset. Minimum input pulse widths are shown in the typical performance characteristics. Note that all devices feature power ON reset.

MODULATION AND SYNC INPUT (PIN 12)

The period t of the time base oscillator can be modulated by applying a DC voltage to this terminal. The time base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12.

TIMEBASE INPUT/OUTPUT PIN (TERMINAL 14)

While this pin can be used as either a time base input or output terminal, it should only be used as an input terminal if terminal 13 (RC) is connected to GND.

If the counter is to be externally driven, care should be taken to ensure that fall times are fast (see Operating Limits section).

Under no conditions is a 300pF capacitor on this terminal useful and should be removed if a 7240/50/60 is used to replace an 8240/50/60 or 2240.

CARRY OUTPUT (TERMINAL 15, ICM7250/60 ONLY)

This pin will go HI for the last 10 counts of a 59 or 99 count, and can be used to drive another 7250 or 7260 counter stage while still using all the counter outputs of the first. Thus, by cascading several 7250's a large BCD countdown can be achieved.

The basic timing diagrams for the ICM7240/50/60 are shown in Figure 1. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states.

Note that for straight binary counting the outputs are symmetrical; that is, a 50% duty cycle HI-LO. This is not the case when using BCD counting. See Figure 3.

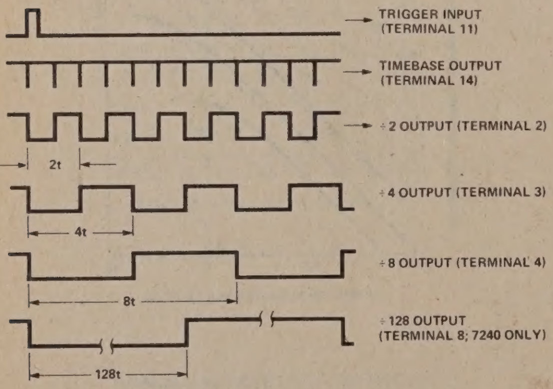

TRIGGER INPUT (TERMINAL 11)
TIMEBASE OUTPUT (TERMINAL 14)
÷2 OUTPUT (TERMINAL 2)
2t
÷4 OUTPUT (TERMINAL 3)
4t
÷8 OUTPUT (TERMINAL 4)
8t
÷128 OUTPUT (TERMINAL 8; 7240 ONLY)
128t

Figure 1. Timing Diagram for ICM7240/50/60

CIRCUIT DESCRIPTION

The timing cycle is initiated by applying a positive-going trigger pulse to pin 11. This pulse enables the counter section, sets all counter outputs to the LOW or ON state, and starts the time base oscillator. Then, external C is charged through external R from 20% to 70% of V^+, generating a timing waveform with period t, equal to 1_{RC}. A short negative clock or time base pulse occurs during the capacitor discharge portion of the waveform. These clock pulses are counted by the binary counter of the 7240 or by two cascaded Binary Coded Decimal (BCD) Counters in the 7250/60. The timing cycle terminates when a positive-going reset pulse is applied to pin 10. When the circuit is at reset, both the time base and the counter sections are disabled and all the counter outputs are at a HIGH or OFF state. The carrry-out is also HIGH.

In most timing applications, one or more of the counter outputs are connected back to the reset terminal; the circuit will start timing when a trigger is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S_1 open), the circuit operates in its astable, or free-running mode, after initial triggering.

PROGRAMMING CAPABILITY

The counter outputs, pins 1 through 8, are open-drain N-channel FETs, and can be shorted together to a common pull-up resistor to form a "wired-AND" connection. The combined output will be LOW as long as **any one** of the outputs is low. Each output is capable of sinking ≈5 mA. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle (monostable mode) t_o would be 32t for a 7240 and 20t for a 7250/60. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $t_o = (1 + 16 + 32)t$ for the 7240 or $(1 + 10 + 20)t$ for the 7250/60. Thus, by selecting the number of counter terminals connected to the output bus, the timing cycle can be programmed from:

$1t \le t_o \le 255t$ (7240)
$1t \le t_o \le 99t$ (7250)
$1t \le t_o \le 59t$ (7260)

Note that for the 7250 and 7260, invalid count states (BCD values ≥ 10) will not be recognized and the counter will not stop.

The 7240/50/60 can be configured to initiate a controlled timing cycle upon power up, and also reset internally; see figure 2. Applications for this could include lawn watering sprinkler timing, pump operation, etc.

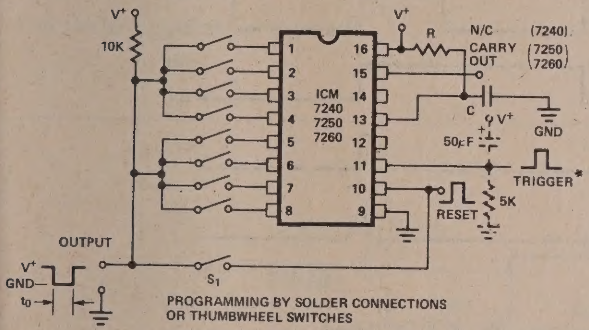
BINARY OR DECIMAL PATTERN GENERATION

In astable operation, as shown in Figure 2, the output of the 7240/50 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 1, which shows the phase relations between the counter outputs. Figure 3 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

THUMBWHEEL SWITCHES

While the ICM7240 is frequently hard wired for a particular function, the ICM7250 and ICM7260 can easily be programmed using thumbwheel switches. Standard BCD thumbwheel switches have one common and four inputs (1,2,4 and 8) which are connected according to the binary equivalent to the digits 0 through 9.

For a single ICM7250 two such switches would select a time of 1RC to 99RC. Cascading two ICM7250's (using the carry out gate) would expand selection to 9999RC. For a ICM7260, there are standard BCD thumbwheel switches for the 0 through 5 digit (twelve position 0 to 5 repeated).


V+
10K
V+
R
N/C
CARRY OUT
(7240)
(7250)
(7260)
ICM 7240 7250 7260
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
C
V+
50μF
GND
TRIGGER*
5K
RESET
OUTPUT
V+
GND
t0
S1

PROGRAMMING BY SOLDER CONNECTIONS
OR THUMBWHEEL SWITCHES

* FOR POWER UP TRIGGERING (t_W=185ms) USE CIRCUIT SHOWN AND OMIT EXTERNAL PULSE.

Figure 2. Generalized Circuit for Timing Applications (Switch S_1 open for astable operation, closed for monostable operation)

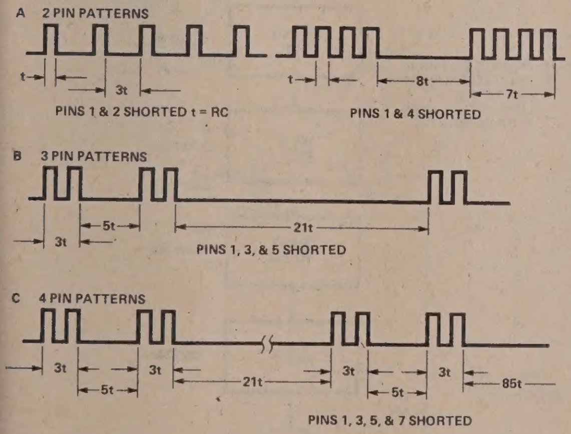

A 2 PIN PATTERNS
t
3t
PINS 1 & 2 SHORTED t = RC
t
8t
7t
PINS 1 & 4 SHORTED
B 3 PIN PATTERNS
3t
5t
21t
PINS 1, 3, & 5 SHORTED
C 4 PIN PATTERNS
3t
5t
3t
21t
3t
5t
3t
85t
PINS 1, 3, 5, & 7 SHORTED

Figure 3. Pulse Patterns Obtained by Shorting Various Counter Outputs

NOTES ON THE COUNTER SECTION

Used as a straight binary counter (ICM7240), as a ÷100 (ICM7250), or ÷60 (ICM7260) all devices are significantly faster than their bipolar equivalents. However, when using these devices as *programmable* counters the maximum frequency of operation is reduced by more than an order of magnitude. For any division ratio other than 256 (ICM7240), 100 (ICM7250), or 60 (ICM7260) the maximum input frequency must be limited to approximately 100 KHz or less (with V+equal to +5 volts). The reason for this is two-fold:

a. Since Ripple counters are used, there is a propagation delay between each individual ÷2 counter (8 counters for the ICM7240/50 and 7 for the ICM7260). Outputs from the individual ÷2 counters are AND'ed together to provide the output signal and the Reset/Trigger signal.

b. There must be a delay of the positive going output to the Reset terminal, (pin 10) and the Trigger terminal (pin 11). The Reset signal must therefore be generated first, and from this signal another signal is obtained through a delay network. The trigger overrides Reset.

The delay between Trigger and Reset is generated by the signal RC network consisting of the 56kΩ resistor and the 330pF capacitor.

The delay caused by the counter Ripple delays can be as long as 2μs (5 volt supply), and the delay between Reset and Trigger should be at least 2 μs. The sum of these two delays cannot be greater than one-half of the input clock period for reliable operation. See Figure 4 and 5.

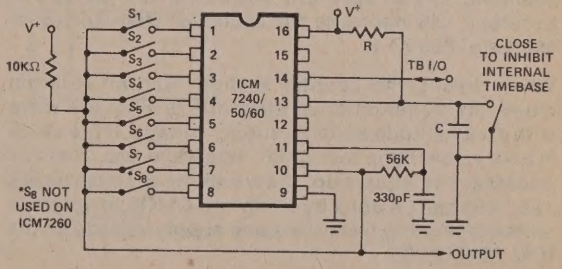

S1
S2
S3
S4
S5
S6
S7
*S8
V+
10KΩ
ICM 7240/ 50/60
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
V+
R
TB I/O
CLOSE TO INHIBIT INTERNAL TIMEBASE
C
56K
330pF
OUTPUT
*S8 NOT USED ON ICM7260

Figure 4. Programming the Counter Section of the ICM7240/50/60

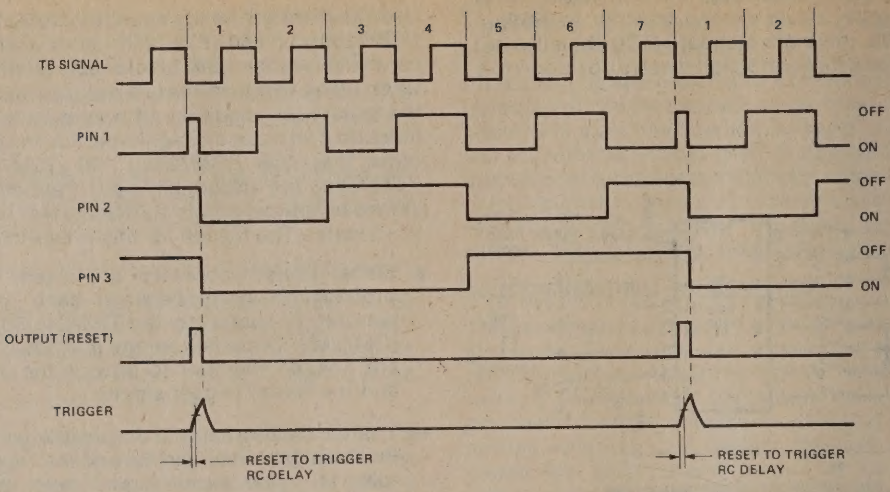

1
2
3
4
5
6
7
1
2
TB SIGNAL
PIN 1
PIN 2
PIN 3
OUTPUT (RESET)
TRIGGER
OFF
ON
OFF
ON
OFF
ON
RESET TO TRIGGER
RC DELAY
RESET TO TRIGGER
RC DELAY

Figure 5. Waveforms for Programming the Counter Section for a Division Ratio of 7 (S$_1$, S$_2$, S$_3$ Closed)

APPLICATIONS

GENERAL CONSIDERATIONS

Shorting the RC terminal or output terminals to V$^+$ may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limit of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under Typical Performance Characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200 KHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform (rise/fall time ≤ 1μs); this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM 7240/50/60.

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

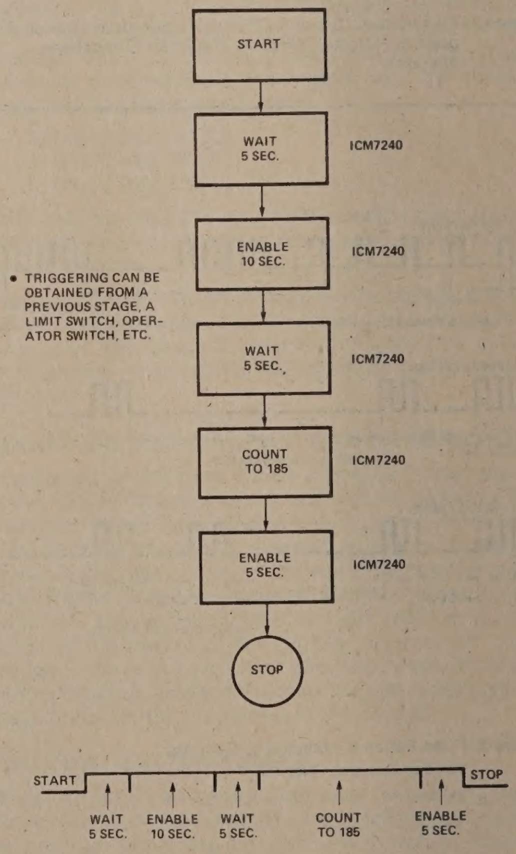

START
WAIT
5 SEC.
ICM7240
ENABLE
10 SEC.
ICM7240
• TRIGGERING CAN BE OBTAINED FROM A PREVIOUS STAGE, A LIMIT SWITCH, OPERATOR SWITCH, ETC.
WAIT
5 SEC.
ICM7240
COUNT
TO 185
ICM7240
ENABLE
5 SEC.
ICM7240
STOP
START
WAIT
5 SEC.
ENABLE
10 SEC.
WAIT
5 SEC.
COUNT
TO 185
ENABLE
5 SEC.
STOP

Figure 6.

CMOS PRECISION PROGRAMMABLE 0-99 SECONDS/MINUTES LABORATORY TIMER

The ICM7250 is well suited as a laboratory timer to alert personnel of the expiration of a preselected interval of time.

When connected as shown, the timer can accurately measure preselected time intervals of 0-99 seconds or 0-99 minutes. A 5 volt buzzer alerts the operator when the preselected time interval is over.

The circuit operates as follows:

The time base is first selected with S1 (seconds or minutes), then units 0-99 are selected on the two thumbwheel switches S4 and S5. Finally, switch S2 is depressed to start the timer. Simultaneously the quartz crystal controlled divider circuits are reset, the ICM7250 is triggered and counting begins. The ICM7250 counts until the pre-programmed value is reached, whereupon it is reset, pin 10 of the CD4082B is enabled and the buzzer is turned on. Pressing S3 turns the buzzer off.

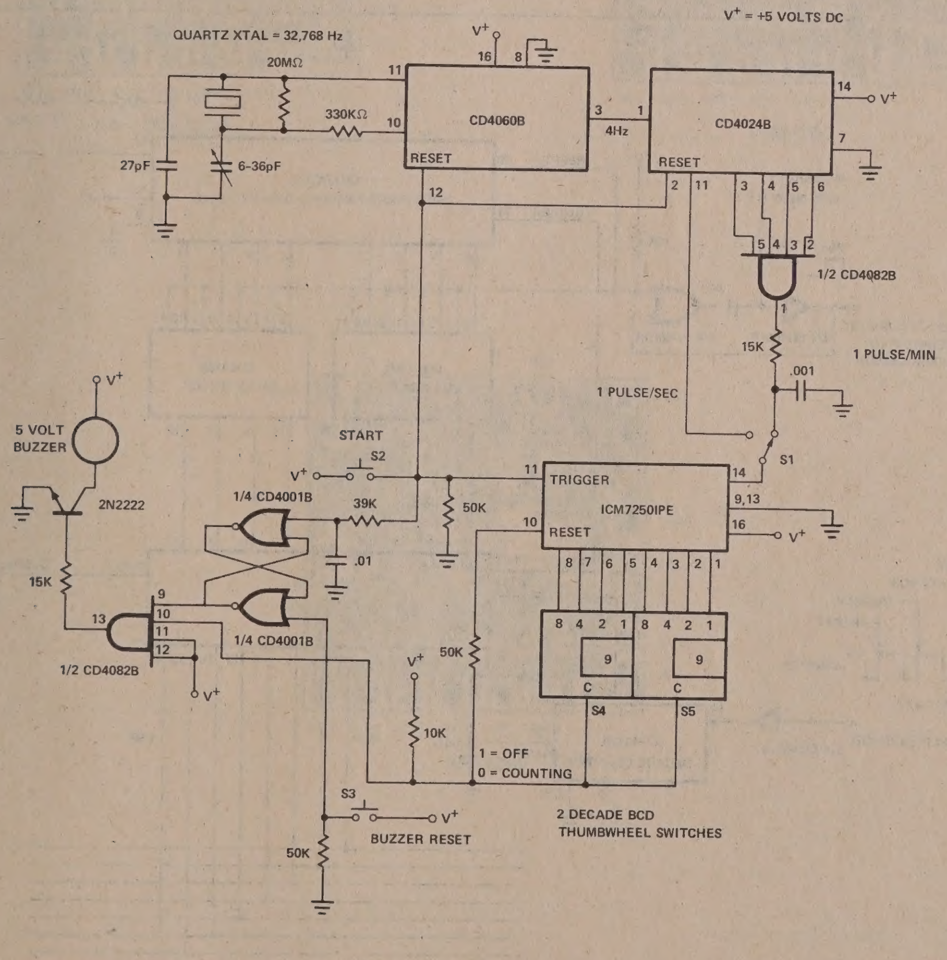

V+ = +5 VOLTS DC
QUARTZ XTAL = 32,768 Hz
V+
16
8
20MΩ
11
330KΩ
10
CD4060B
RESET
12
27pF
6-36pF
3
1
4Hz
CD4024B
RESET
14
V+
7
2
11
3
4
5
6
5
4
3
2
1/2 CD4082B
1
15K
1 PULSE/MIN
.001
1 PULSE/SEC
S1
V+
5 VOLT
BUZZER
2N2222
START
S2
V+
11
TRIGGER
14
ICM7250IPE
9,13
10
RESET
16
V+
1/4 CD4001B
39K
50K
.01
15K
9
13
10
11
12
1/4 CD4001B
1/2 CD4082B
V+
8
7
6
5
4
3
2
1
8 4 2 1
8 4 2 1
9
9
C
C
S4
S5
V+
50K
10K
1 = OFF
0 = COUNTING
S3
V+
BUZZER RESET
50K
2 DECADE BCD
THUMBWHEEL SWITCHES

Figure 7.

LOW POWER MICROPROCESSOR PROGRAMMABLE INTERVAL TIMER

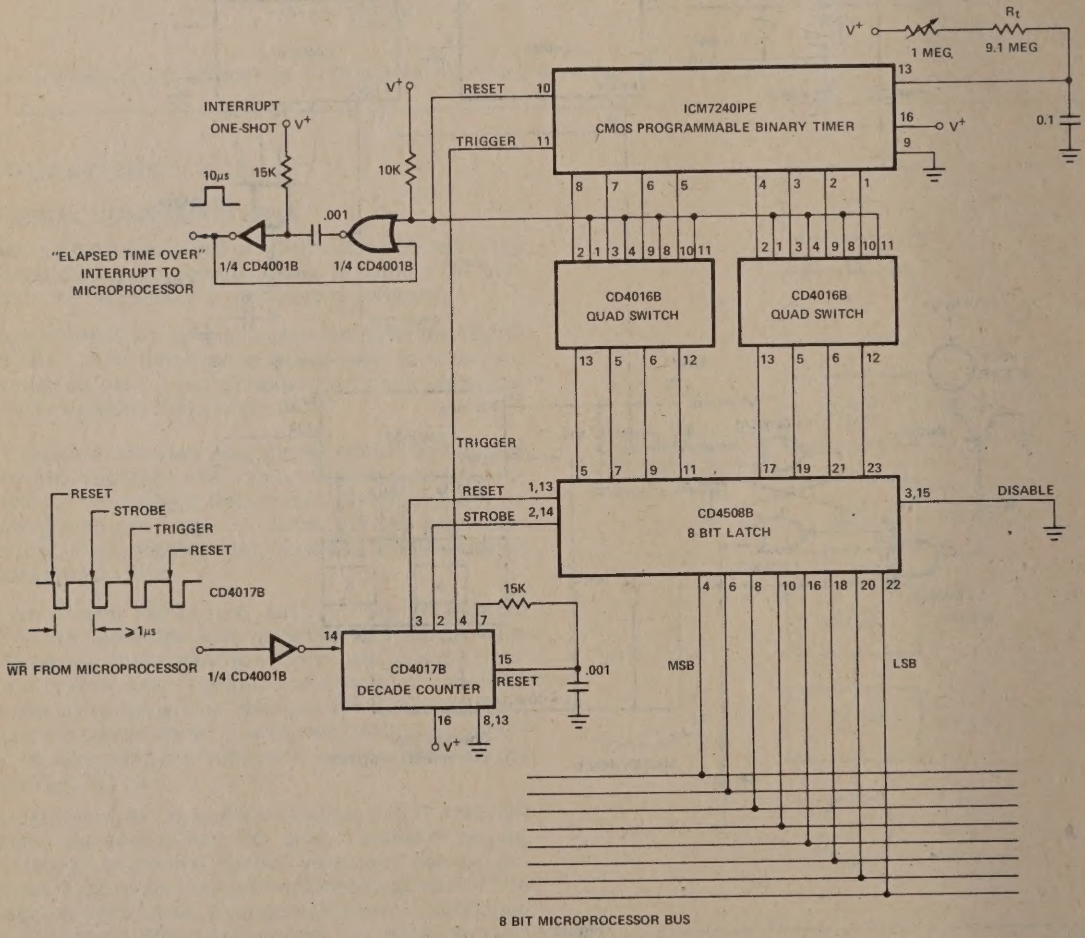
The ICM7240 CMOS programmable binary timer can be configured as a low cost microprocessor controlled interval timer with the addition of a few inexpensive CD4000 series devices.

With the devices connected as shown, the sequence of operation is as follows:

The microprocessor sends out an 8 bit binary code on its 8 bit I/O bus (the binary value needed to program the ICM7240), followed by four $\overline{\text{WRITE}}$ pulses into the CD4017B decade counter. The first pulse resets the 8 bit latch, the second strobes the binary value into the 8 bit latch, the third triggers the ICM7240 to begin its timing cycle and the fourth resets the decade counter.

The ICM7240 then counts the interval of time determined by the R-C value on pin 13, and the programmed binary count on pins 1 through 8. At the end of the programmed time interval, the interrupt one-shot is triggered, informing the microprocessor that the programmed time interval is over.

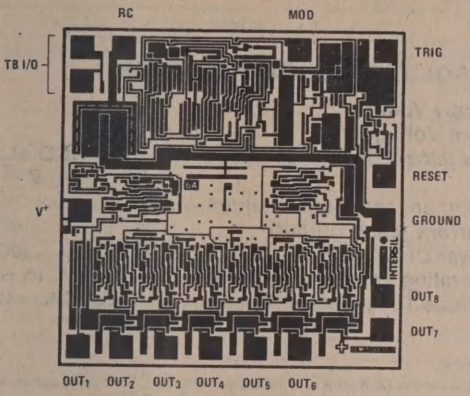
With a resistor of approximately 10 MΩ and capacitor of 0.1 μF, the time base of the ICM7240 is one second. Thus, a time of 1-255 seconds can be programmed by the microprocessor, and by varying R or C, longer or shorter time bases can be selected.



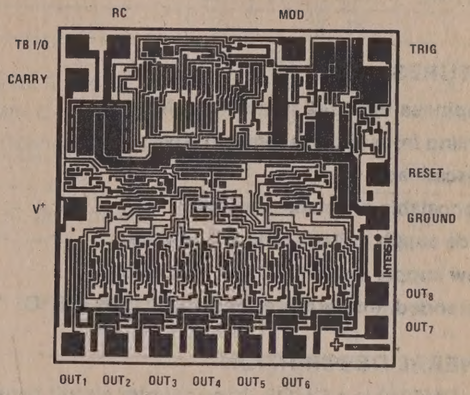
V+
1 MEG.
Rt
9.1 MEG
13
ICM7240IPE
CMOS PROGRAMMABLE BINARY TIMER
16
V+
9
0.1
Ct
RESET 10
TRIGGER 11
INTERRUPT
ONE-SHOT
V+
15K
10K
10μs
.001
"ELAPSED TIME OVER" INTERRUPT TO MICROPROCESSOR
1/4 CD4001B
1/4 CD4001B
CD4016B
QUAD SWITCH
CD4016B
QUAD SWITCH
TRIGGER
RESET 1,13
STROBE 2,14
CD4508B
8 BIT LATCH
3,15
DISABLE
RESET
STROBE
TRIGGER
RESET
CD4017B
≥1μs
WR FROM MICROPROCESSOR
1/4 CD4001B
14
15K
CD4017B
DECADE COUNTER
15
RESET
.001
16
V+
8,13
MSB
LSB
8 BIT MICROPROCESSOR BUS

Figure 8.

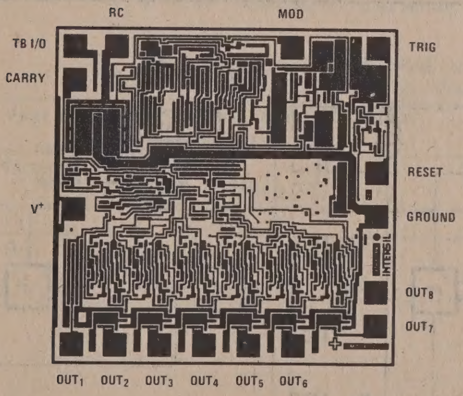
CHIP TOPOGRAPHY


RC
MOD
TB I/O
TRIG
RESET
V$^+$
GROUND
OUT$_8$
OUT$_7$
OUT$_1$
OUT$_2$
OUT$_3$
OUT$_4$
OUT$_5$
OUT$_6$
INTERSIL

ICM7240


RC
MOD
TB I/O
CARRY
TRIG
RESET
V$^+$
GROUND
OUT$_8$
OUT$_7$
OUT$_1$
OUT$_2$
OUT$_3$
OUT$_4$
OUT$_5$
OUT$_6$
INTERSIL

ICM7250


RC
MOD
TB I/O
CARRY
TRIG
RESET
V$^+$
GROUND
OUT$_8$
OUT$_7$
OUT$_1$
OUT$_2$
OUT$_3$
OUT$_4$
OUT$_5$
OUT$_6$
INTERSIL

ICM7260

ALL CHIPS 68 x 69 mils

INTERSIL

ICM7242
Long Range Fixed Timer/Counter

FEATURES

- **Replaces the 2242 in most applications**
- **Timing from microseconds to days**
- **Cascadeable**
- **Monostable or astable operation**
- **Wide supply voltage range: 2-16 volts**
- **Low supply current: 115μA @ 5 volts**
- **Extended temperature range: -20° C to +85° C**

GENERAL DESCRIPTION

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in 95% of the applications, with a significant reduction in the number of external components.

Three outputs are provided. They are, the oscillator output, and buffered outputs from the first and eighth counters.

The ICM7242 is packaged in an 8-pin CERDIP.

ABSOLUTE MAXIMUM RATINGS

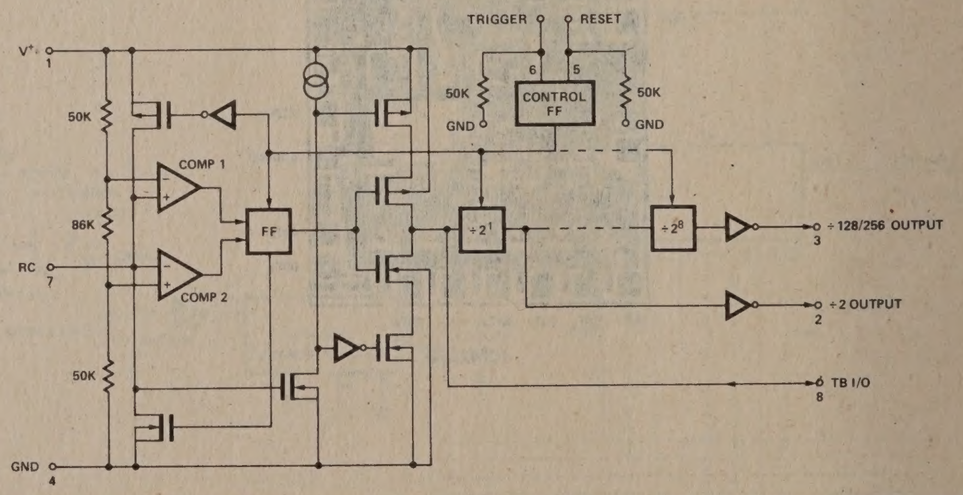
Supply Voltage	18V
Input Voltage[1] Terminals (Pins 5, 6, 7, 8)	GND -0.3V to V⁺+ 0.3V
Maximum continuous output current (each output)	50 mA
Power Dissipation[2]	200 mW
Operating Temperature Range	-20° C to +85° C
Storage Temperature Range	-55° C to +125° C

NOTES:

1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V⁺or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply by applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.
2. Derate at -2 mW/°C above 25°C.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

BLOCK DIAGRAM

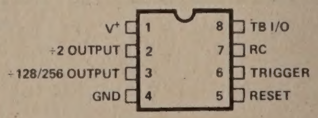


ORDERING INFORMATION

Device: ICM7242IJA

Dice: ICM7242/D

PIN CONFIGURATION (OUTLINE DRAWING JA)

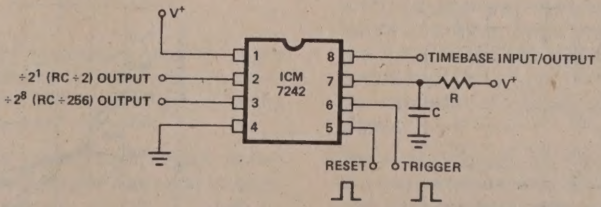


ELECTRICAL CHARACTERISTICS

Test Conditions: Test circuit, $V^+ = 5V$, $T_A = +25°C$, $R = 10K\Omega$, $C = 0.1\mu F$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current	I^+	Reset		125		μA
		Operating, R = 10KΩ, C = 0.1μF		300	700	μA
		Operating, R = 1MΩ, C = 0.1μF		120	500	μA
		TB Inhibited, RC Connected to GND		125		μA
Timing Accuracy				5		%
RC Oscillator Frequency Temperature Drift	$\Delta f/\Delta T$	(Independent of RC Components)		250		ppm/°C
Time Base Output Voltage	V_{OTB}	$I_{SOURCE} = 1$ mA	3.5	4.2		V
		$I_{SINK} = 3.2$ mA		0.25	0.6	V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground			25	μA
Mod Voltage Level	V_{MOD}	$V^+ = 5V$		3.5		V
		$V^+ = 15V$		11.0		V
Trigger Input Voltage	V_{TRIG}	$V^+ = 5V$		1.6	2.0	V
		$V^+ = 15V$		3.5	4.5	V
Reset Input Voltage	V_{RST}	$V^+ = 5V$		1.3	2.0	V
		$V^+ = 15V$		2.7	4.0	V
Trigger/Reset Input Resistors	R_{TRIG}, R_{RST}	(Pull Downs)		50		kΩ
Max Count Toggle Rate	f_t	$V^+ = 2V$		1		MHz
		$V^+ = 5V$ Counter/Divider Mode	2	6		MHz
		$V^+ = 15V$		13		MHz
		50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND				
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output $V^+ = 5V$, $I_{OUT} = 3.2$ mA		0.22	0.4	V
Output Sourcing Current 7242	I_{SOURCE}	$V^+ = 5V$ Terminals 2 & 3, $V_{OUT} = 1V$		300		μA
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	$V^+ \leq 5.5V$	100		22M	Ω
		$V^+ \leq 16V$	300		22M	Ω

TEST CIRCUIT

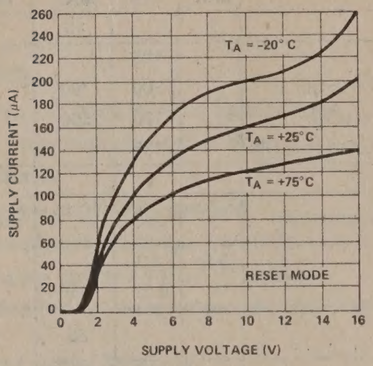


• TIMEBASE PERIOD = 1.0RC;
1 SEC. = 1MΩ x 1μF

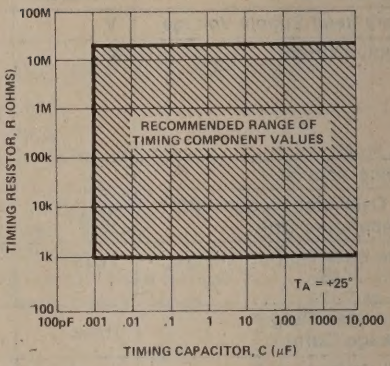
NOTE: OUTPUTS ÷2^1 AND ÷2^8 ARE INVERTERS AND HAVE ACTIVE PULLUPS.

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

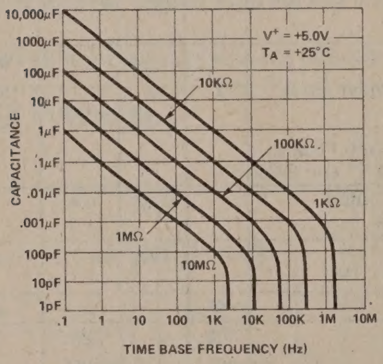


RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING

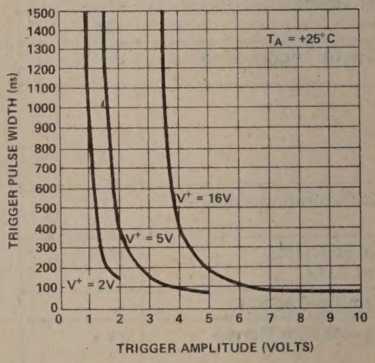


DIMENSIONS IN INCHES AND MILLIMETERS

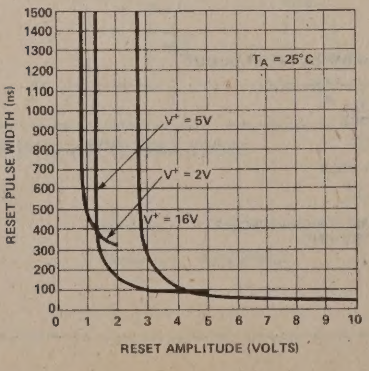
TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



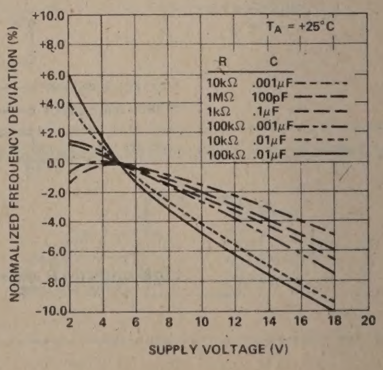
MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE

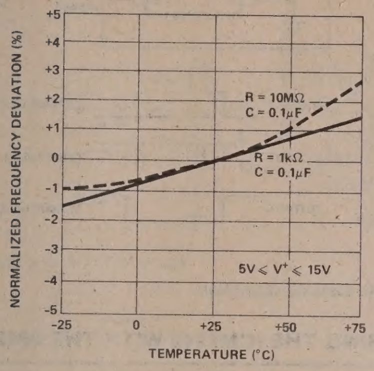


NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE

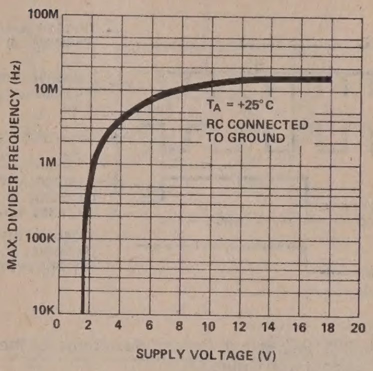


TYPICAL PERFORMANCE CHARACTERISTICS

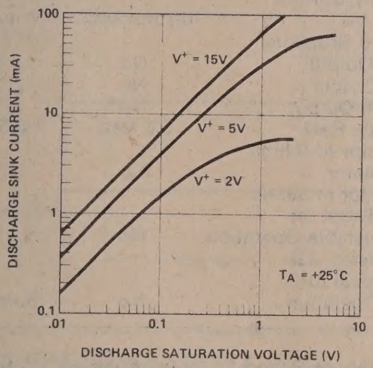
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



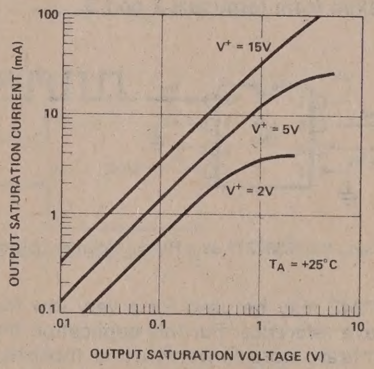
MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE



DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



APPLICATIONS

GENERAL CONSIDERATIONS

Shorting the RC terminal or output terminals to V$^+$ may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

OPERATING LIMITS

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under typical performance characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200 KHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscillator/timer than a 555 or ICM7555, because of the on-chip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

Because outputs will not be AND'd, output inverters are used instead of open drain N-channel transistors, and the external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

The timing diagram for the ICM7242 is shown in Figure 1. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the $\div 2^8$ output returns to the high state.

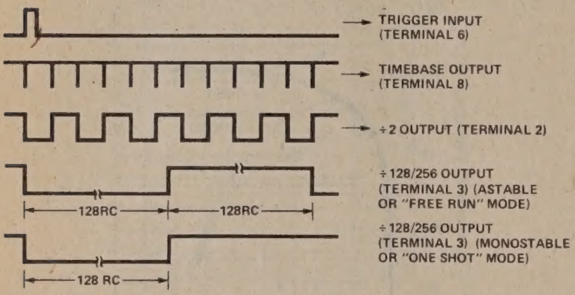

TRIGGER INPUT (TERMINAL 6)
TIMEBASE OUTPUT (TERMINAL 8)
÷2 OUTPUT (TERMINAL 2)
÷128/256 OUTPUT (TERMINAL 3) (ASTABLE OR "FREE RUN" MODE)
128RC
128RC
÷128/256 OUTPUT (TERMINAL 3) (MONOSTABLE OR "ONE SHOT" MODE)
128 RC

Figure 1. Timing Diagrams of Output Waveforms for the ICM7242. (Compare with Figure 5)

To use the 8-bit counter without the timebase, terminal 7 (TB I/O) should be connected to ground and the outputs taken from terminals 2 and 3.

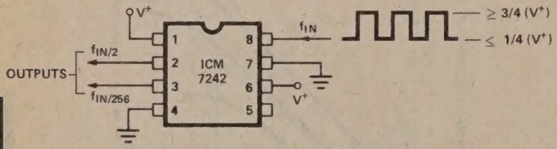

V+
fIN/2
OUTPUTS
fIN/256
ICM 7242
1
2
3
4
8
7
6
5
fIN
V+
≥ 3/4 (V+)
≤ 1/4 (V+)

Figure 2. Using the ICM7242 as a Ripple Counter (Divider)

The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 3).

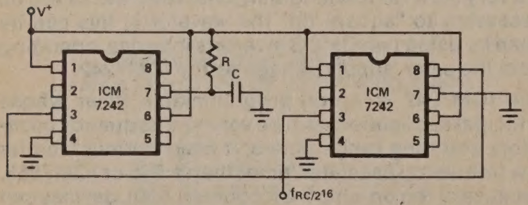

V+
R
C
ICM 7242
ICM 7242
1
2
3
4
8
7
6
5
fRC/216

Figure 3. Low Frequency Reference (Oscillator)

For monostable operation the $\div 2^8$ output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

The ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value p^-resistors have been used on the ICM7242 to provide the comparator timing points.

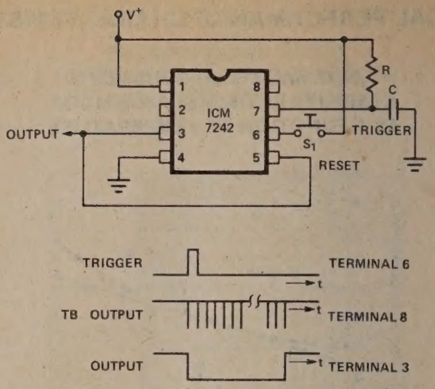

V+
R
C
ICM 7242
1
2
3
4
8
7
6
5
OUTPUT
S1
TRIGGER
RESET
TRIGGER
TERMINAL 6
t
TB OUTPUT
TERMINAL 8
t
OUTPUT
TERMINAL 3
t

Figure 4. Monostable Operation

COMPARING THE ICM7242 WITH THE 2242

		ICM7242	2242
a.	Operating Voltage	2-16V	4-15V
b.	Commercial Temp. Range	-20° C to +75° C	0° C to +75° C
c.	Supply Current V+ = 5V	0.7 mA Max.	7 mA Max.
d.	Pullup Resistors		
	TB Output	No	Yes
	÷2 Output	No	Yes
	÷256 Output	No	Yes
e.	Toggle Rate	3.0 MHz	0.5 MHz
f.	Resistor to Inhibit Oscillator	No	Yes
g.	Resistor in Series with Reset for Monostable Operation	No	Yes
h.	Capacitor TB Terminal for HF Operation	No	Sometimes

By selection of R and C , a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

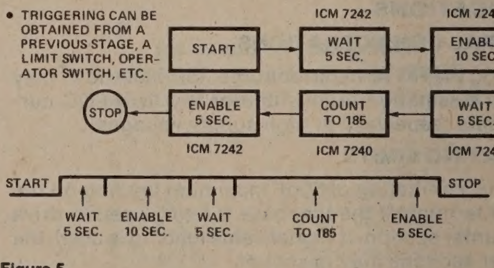

• TRIGGERING CAN BE OBTAINED FROM A PREVIOUS STAGE, A LIMIT SWITCH, OPERATOR SWITCH, ETC.
START
ICM 7242
WAIT 5 SEC.
ICM 7242
ENABLE 10 SEC.
STOP
ENABLE 5 SEC.
ICM 7242
COUNT TO 185
ICM 7240
WAIT 5 SEC.
ICM 7242
START
STOP
WAIT 5 SEC.
ENABLE 10 SEC.
WAIT 5 SEC.
COUNT TO 185
ENABLE 5 SEC.

Figure 5.

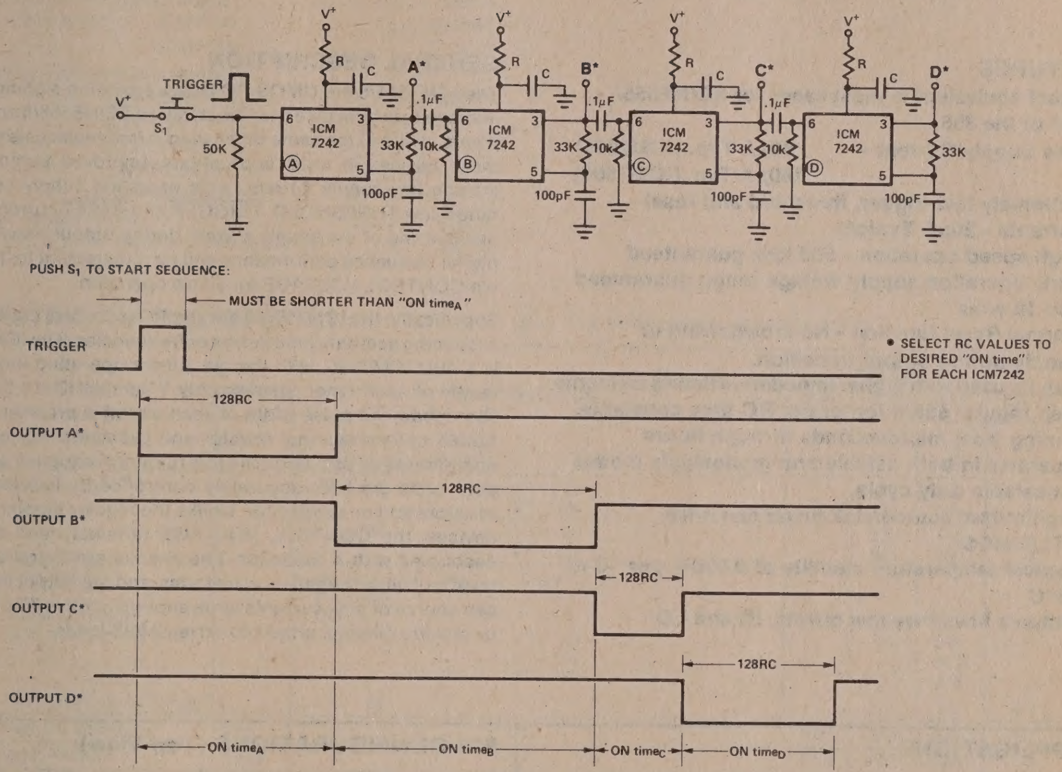
By cascading devices, use of low cost CMOS AND/ OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, autoatic lubrication systems, etc.

ICM7242

SEQUENCE TIMING

- Process Control
- Machine Automation
- Electro-pneumatic Drivers
- Multi-operation (Serial or Parallel controlling)

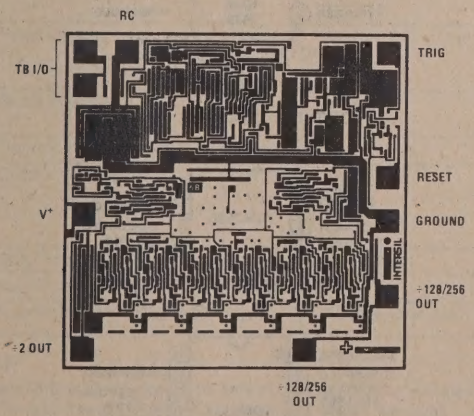
SEQUENCE TIMER:



V+
R
C
A*
B*
C*
D*
TRIGGER
S1
50K
ICM 7242
6
3
5
Ⓐ
Ⓑ
Ⓒ
Ⓓ
.1μF
33K
10k
100pF
PUSH S1 TO START SEQUENCE:
MUST BE SHORTER THAN "ON timeA"
TRIGGER
128RC
OUTPUT A*
OUTPUT B*
OUTPUT C*
OUTPUT D*
ON timeA
ON timeB
ON timeC
ON timeD
• SELECT RC VALUES TO DESIRED "ON time" FOR EACH ICM7242

Figure 6.

CHIP TOPOGRAPHY (.068" × .069")



RC
TB I/O
V+
÷2 OUT
TRIG
RESET
GROUND
÷128/256 OUT
÷128/256 OUT
INTERSIL

ICM7555/7556
CMOS
General Purpose Timers

FEATURES

- **Exact equivalent in most cases for SE/NE555/ • 556 or the 355.**
- **Low Supply Current — 80μA Typ. (ICM7555)**
  160μA Typ. (ICM7556)
- **Extremely low trigger, threshold and reset currents - 20pA Typical**
- **High speed operation - 500 kHz guaranteed**
- **Wide operation supply voltage range guaranteed 2 to 18 volts**
- **Normal Reset function - No crowbarring of supply during output transition.**
- **Can be used with higher impedance timing elements than regular 555/6 for longer RC time constants.**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **High output source/sink driver can drive TTL/CMOS**
- **Typical temperature stability of 0.005% per °C at 25°C**
- **Outputs have very low offsets, HI and LO**

GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V^+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

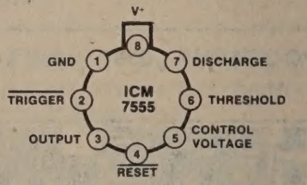
APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

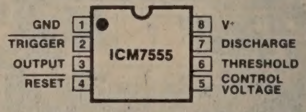
ORDERING INFORMATION

ORDER PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7555IPA	−20 to +85°C	8 Lead MiniDip
ICM7555ITY	−20 to +85°C	TO-99 Can
ICM7555MTY	−55 to +125°C	TO-99 Can
ICM7556IPD	−20 to +85°C	14 Lead Plastic DIP
ICM7556MJD	−55 to +125°C	14 Lead CERDIP
ICM7555/D		DICE
ICM7556/D		DICE

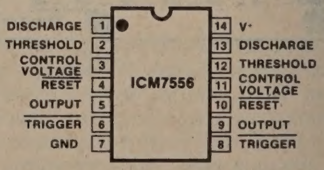
PIN CONFIGURATIONS (Top View)


V+
8
GND 1
7 DISCHARGE
TRIGGER 2
ICM 7555
6 THRESHOLD
OUTPUT 3
5 CONTROL VOLTAGE
4
RESET

(OUTLINE DRAWING TO-99)


GND 1
TRIGGER 2
OUTPUT 3
RESET 4
ICM7555
8 V+
7 DISCHARGE
6 THRESHOLD
5 CONTROL VOLTAGE

(OUTLINE DRAWING PA)


DISCHARGE 1
THRESHOLD 2
CONTROL VOLTAGE 3
RESET 4
OUTPUT 5
TRIGGER 6
GND 7
ICM7556
14 V+
13 DISCHARGE
12 THRESHOLD
11 CONTROL VOLTAGE
10 RESET
9 OUTPUT
8 TRIGGER

(OUTLINE DRAWING JD, PD)

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage .... +18 Volts
Input Voltage Trigger, Threshold, $\overline{\text{Reset}}$ ..... $\leq V^+ + 0.3V$ to $\geq V^- - 0.3V$
Output Current Control Voltage 100mA
Power Dissipation[2] ICM7556 .... 300mW
ICM7555 .... 200mW
Operating Temperature Range [2]
ICM7555IPA .... −20° C to +85° C
ICM7555ITY .... −20° C to +85° C
ICM7556IPD .... −20° C to +85° C
ICM7555MTY .... −55° C to +125° C
ICM7556MJD .... −55° C to +125° C
Storage Temperature .... −65° C to +150° C
Lead Temperature (Soldering 60 Seconds) .... +300° C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS (T_A = 25° C, V^+ = +2 to +15 Volts unless other specified)

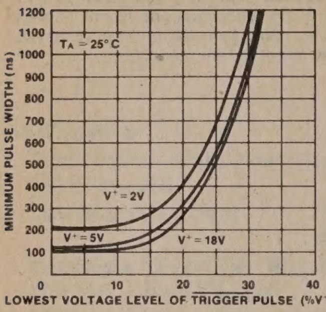
PARAMETER	SYMBOL	TEST CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
Supply Voltage	V^+	$-20° C \leq T_A \leq +70° C$	2		18	V
		$-55° C \leq T_A \leq +125° C$	3		16	V
Supply Current[3]	I^+	ICM7555 $V^+ = 2V$		60	200	μA
		$V^+ = 18V$		120	300	μA
		ICM7556 $V^+ = 2V$		120	400	μA
		$V^+ = 18V$		240	600	μA
Timing Error		R_A, R_B = 1k to 100k, $5V \leq V^+ \leq 15V$ C = 0.1μF				
Initial Accuracy		Note 4		2.0	5.0	%
Drift with Temperature		Note 4 $V^+ = 5V$		50	200	ppm/° C
		$V^+ = 10V$			300	
		$V^+ = 15V$			600	
Drift with Supply Voltage		$V^+ = 5V$		1.0	3.0	%/V
Threshold Voltage	V_{TH}	V^+	0.63	0.66	0.67	V^+
Trigger Voltage	V_{TRIG}	V^+	0.29	0.33	0.34	V^+
Trigger Current	I_{TRIG}	$V^+ = 18V$		50		pA
		$V^+ = 5V$		10		pA
		$V^+ = 2V$		1		pA
Threshold Current	I_{TH}	$V^+ = 18V$		50		pA
		$V^+ = 5V$		10		pA
		$V^+ = 2V$		1		pA
Reset Current	I_{RST}	V_{RESET} = Ground $V^+ = 18V$		100		pA
		$V^+ = 5V$		20		pA
		$V^+ = 2V$		2		pA
Reset Voltage	V_{RST}	$V^+ = 18V$	0.4	0.7	1.0	V
		$V^+ = 2V$	0.4	0.7	1.0	V
Control Voltage Lead	V_{CV}	V^+	0.62	0.66	0.67	V^+
Output Voltage Drop	V_O	Output Lo $V^+ = 18V$ $I_{SINK} = 3.2mA$		0.1	0.4	V
		$V^+ = 5V$ $I_{SINK} = 3.2mA$		0.15	0.4	V
		Output Hi $V^+ = 18V$ $I_{SOURCE} = 1.0mA$	17.25	17.8		V
		$V^+ = 5V$ $I_{SOURCE} = 1.0mA$	4.0	4.5		V
Rise Time of Output	t_r	$R_L = 10M\Omega$ $C_L = 10pF$ $V^+ = 5V$	35	40	75	ns
Fall Time of Output	t_f	$R_L = 10M\Omega$ $C_L = 10pF$ $V^+ = 5V$	35	40	75	ns
Guaranteed Max Osc Freq	f_{max}	Astable Operation	500			kHz

NOTES:

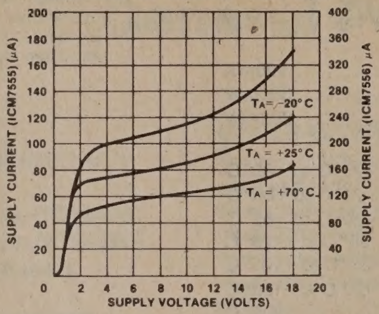
1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ +0.3V or less than V^- −0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.
2. Junction temperatures should not exceed 135° C and the power dissipation must be limited to 20mW at 125° C. Below 125° C power dissipation may be increased to 300mW at 25° C. Derating factor is approximately 3mW/° C (7556) or 2mW/° C (7555).
3. The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD and $\overline{\text{RESET}}$ voltages.
4. Parameter is not 100% tested, Majority of all units meet this specification.

TYPICAL CHARACTERISTICS

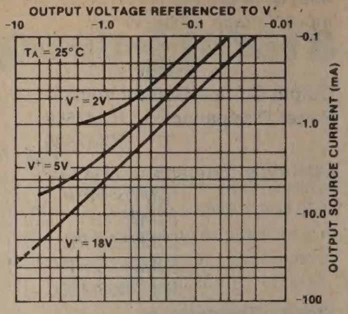
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



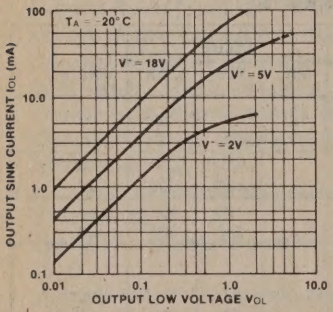
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



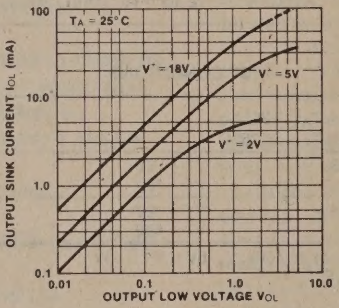
OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



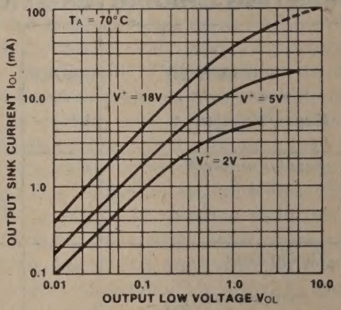
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



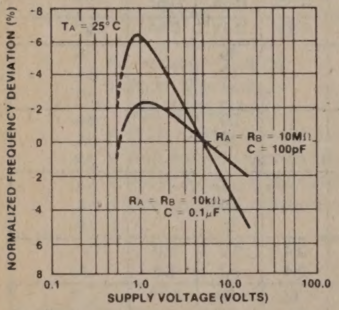
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



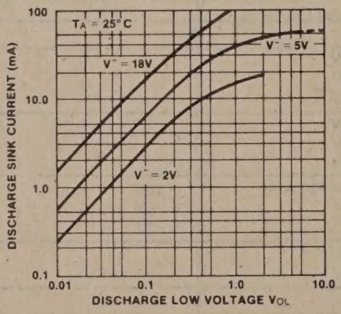
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



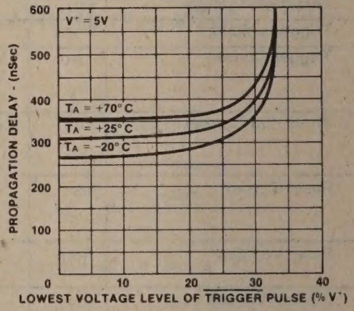
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



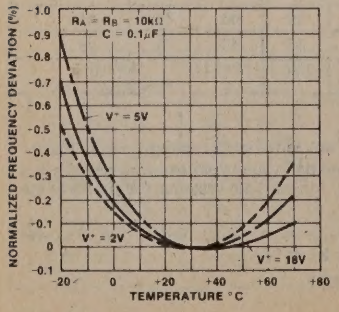
DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



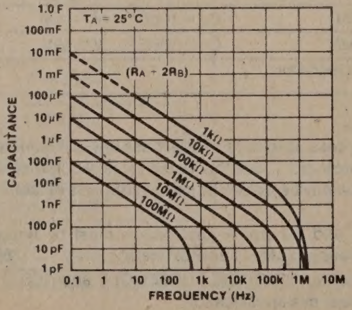
PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



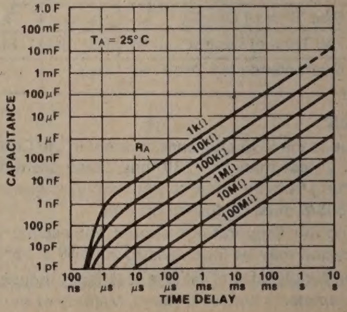
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



FREE RUNNING FREQUENCY AS A FUNCTION OF RA, RB and C



TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF RA AND C



APPLICATION NOTES

GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 2.

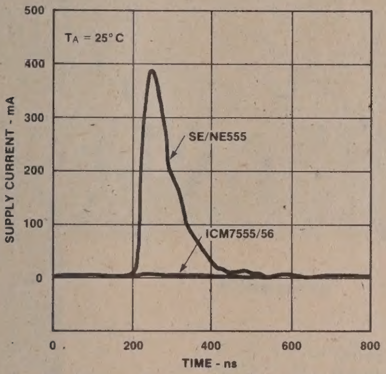


Figure 2. Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition

The ICM7555/6 produces supply current spikes of only 2-3 mA instead of 300-400 mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 3 and 4.

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 3. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

$$f = \frac{1}{1.4\,RC}$$

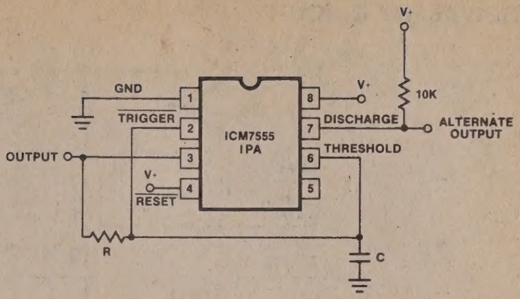


Figure 3: Astable Operation

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

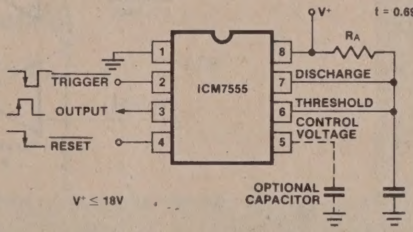


Figure 4: Monostable Operation

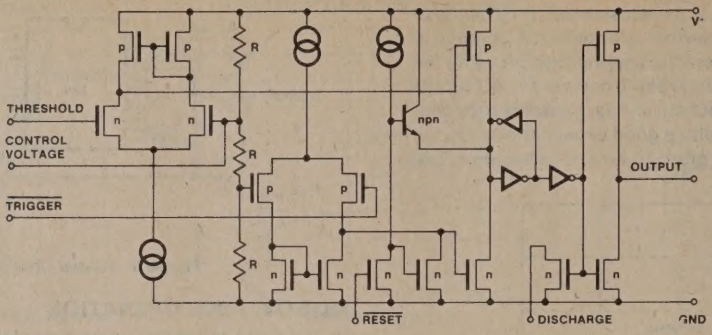
CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and TRIGGER internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

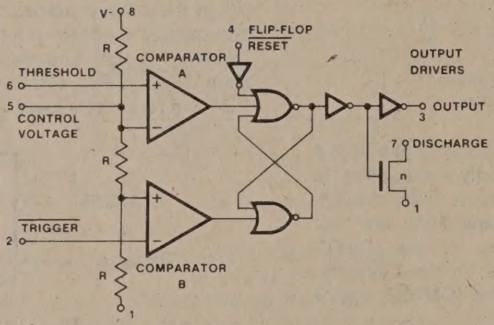
$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

EQUIVALENT CIRCUIT


V+
p
R
THRESHOLD
n
CONTROL VOLTAGE
TRIGGER
npn
OUTPUT
RESET
DISCHARGE
GND

BLOCK DIAGRAM


V+ 8
R
COMPARATOR A
4 FLIP-FLOP RESET
OUTPUT DRIVERS
THRESHOLD 6
5 CONTROL VOLTAGE
OUTPUT 3
7 DISCHARGE
n
1
TRIGGER 2
COMPARATOR B
1

This block diagram reduces the circuitry down to its simplest equivalent components.
Tie down unused inputs.
R = 100kΩ, ± 20% typ.

TRUTH TABLE

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
$>2/3(V^+)$	$>1/3(V^+)$	HIGH	LOW	ON
$1/3<V_{TH}<2/3$	$1/3<V_{TH}<2/3$	HIGH	STABLE	STABLE
DON'T CARE	$<1/3(V^+)$	HIGH	HIGH	OFF

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

Consumer Circuits

Watches

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ICM7045A 7-15
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Touch Tone Encoders

ICM7206 7-28

Watches

Part Number	Circuit Description	Typical Current at 1.55 VDC
ICM1424C	3½-Digit 5-Function LCD watch circuit. Features Hours:Minutes, Month-Date, Seconds. Rapid advance setting. Mounts on top of the watch substrate.	1.5μA
ICM1424MC	Same as ICM1424C above, except mounts on backside of the substrate.	1.5μA
ICM7210 ICM7210C	4-Digit 6-Function LCD watch circuit. Features Hours:Minutes, Month-Date, Alpha Day, Seconds. ICM7210 mounts on top of substrate, has AM/PM flags.	1.5μA
ICM7210M ICM7210MC	Same as ICM7210 and ICM7210C above, except backside mount.	1.5μA
ICM7214A	4-Digit 6-Function LED watch circuit. Features Hours:Minutes, Alpha Day, Month-Date, Seconds. Direct drive of LED digits and segments.	4.0μA @3.1 V
ICM7220A ICM7220FA	6-Digit 6-Function LCD watch circuit with direct drive Cricket alarm. Features Hours:Minutes, Month-Date, Alpha Day (ICM7220A) or Day-of-Week flags (ICM7220FA), Seconds. Backside mount.	2.5μA
ICM7220MA ICM7220MA	Same as ICM7220A and ICM7220FA above, except top mount.	2.5μA
ICM7245B/D/E/F ICM7245U	Analog quartz watch/clock circuit. ICM7245B/D/E/F for bipolar stepper motors, ICM7245U for unipolar stepper motors. Ultra high accuracy: 0.1 ppm.	0.4μA
ICM7270	4-Digit 6-Function Duplex LCD watch circuit. Features Hours:Minutes, Day-of-Week flags, Month-Date, Seconds. Bond option for 24 hour, date-month reversal. Top mount. Ultra high accuracy 0.1 ppm	0.9μA
ICM7271	4-Digit 6-Function Duplex LCD watch circuit with direct Cricket alarm and Snooze. Features Hours:Minutes, Day-of-Week flags, Month-Date, Seconds. Bond option for 24 hour, date-month reversal. 5 minute repeatable snooze. Top mount. Ultra high accuracy 0.1 ppm	0.9μA
ICM7272	4-Digit 6-Function Duplex LCD watch circuit with Chronograph. Features Hours:Minutes, Day-of-Week flags, Month-Date, Seconds. Bond option for 24 hour, date-month reversal. 30 minute Chronograph with auto rollover, bargraph for tenths of seconds resolution. Top mount. Ultra high accuracy 0.1 ppm	0.9μA
ICM7273	4-Digit 6-Function LCD watch circuit with direct drive Cricket alarm. Features Hours:Minutes, Day-of-Week flags, Month-Date, Seconds. Bond option for 24 hour, date-month reversal. Top mount.	2.5μA

Notes: All Intersil watch circuits are designed for use with a 32,768Hz quartz crystal. All provide a rapid advance setting.

Watch circuits are normally sold in die form. The ICM1424C is also available in a 40 pin plastic DIP, and the ICM7245B/D/E/F and ICM7245U are available in either an 8 pin plastic DIP or mini-flatpack as well as dice.

All Intersil watch circuits have a fixed on-chip oscillator capacitor. The above circuits show typical current at 1.55 Volts (3.1 for the ICM7214A) LCD units in doubler mode.

Clocks

Part Number	Circuit Description	Typical Operating Voltage	Package
ICM1115 ICM1115A ICM1115B	Analog quartz clock circuit with simple alarm. For bipolar stepper motors; 1 Hz square wave output. Analog quartz clock circuit with simple alarm. For bipolar stepper motors; 1 Hz square wave output. Analog quartz clock circuit with simple alarm. For bipolar stepper, motors; 1 Hz square wave output.	1.5V	8 pin DIP
ITS9064-1	Analog quartz clock with complex alarm. For bipolar stepper motors. 1Hz square wave output.		
ICM7038A ICM7038C ICM7038F	Analog quartz clock circuit with simple alarm. For synchronous motors. ICM7038A is a 16 stage divider, 7038C is a 17 stage divider, and 7038F is an 18 stage divider. All have a square wave output.	3.0V	8 pin DIP
ICM7038B ICM7038D ICM7038E ICM7038G	Analog quartz clock circuit with simple alarm. For synchronous motors. ICM7038B is a 16 stage divider, 7038D is a 17 stage, 7038E is an 18 stage, and 7038G is a 19 stage. All have a square wave output.	1.5V	8 pin DIP
ICM7049A	Analog quartz clock circuit with complex alarm. For unipolar stepper motors. 31 ms pulse width, 1Hz rate.	1.5V	8 pin DIP
ICM7050	Analog quartz clock circuit with complex alarm. For bipolar stepper motors. 47 ms pulse width, 1Hz rate	1.5V	8 pin DIP
ITS9063	Analog quartz clock circuit with complex alarm. For bipolar stepper motors. 31 ms pulse width, 1Hz rate		
ICM7051A ICM7051B	Analog quartz clock circuit for automotive applications—synchronous motors, 64 Hz square wave. Analog quartz clock circuit for automotive applications—bipolar stepper motors. 31 ms pulse width, 1Hz rate	12.0V	8 pin DIP
ICM7052	Analog quartz clock circuit with complex alarm and Snooze. For bipolar stepper motors. 31 ms pulse width, 1Hz rate.	1.5V	14 pin DIP
ICM7223 ICM7223D	4 Digit LCD Alarm Clock with Snooze. Direct drive Cricket alarm. 24 hour format by bond option. For 32.768 kHz quartz crystal.	1.5V	40 pin DIP
ICM7223A	4 Digit LCD Clock Radio circuit with Sleep Timer, Snooze and Alarm. Low battery indicator, Radio Enable. For 32.768 kHz quartz crystal.	9.0V	40 pin DIP
ICM7223VF	4 Digit Vacuum Fluorescent Clock Radio/Auto Clock circuit with Sleep Timer, Alarm, Snooze, and Radio Enable. For 32.768 kHz quartz crystal.	12.0V	40 pin DIP

Notes: All Analog clock circuits are designed for use with a 4.19 MHz quartz crystal, with the exception of the ICM7223 series which uses a 32.768 kHz crystal.
Clock circuits are normally purchased in package form; each is also available as dice.
All Analog clock circuits are mask programmable for oscillator frequency, output frequency and pulse width, and alarm frequency. Consult the factory for details.

Stopwatches

Part Number	Circuit Description	Crystal Frequency	Package
ICM7045	8 Digit 4 Function LED stopwatch circuit. Features Hours:Minutes:Seconds:100ths. Provides Time Out, Taylor, Split and Rally modes. Direct drive for LEDs. May be used as 24-hour clock.	6.55 MHz	28 pin DIP
ICM7045A	8 Digit 4 Function LED industrial stopwatch circuit, precision decade timer. Counts seconds, minutes or hours by selection of suitable quartz crystal.	Seconds: 1.31MHz Minutes: 2.18 MHz Hours: 3.64 MHz	28 pin DIP
ICM7205	6 Digit 2 Function LED stopwatch circuit. Features Minutes:Seconds:100ths. Provides Taylor and Split modes. Direct drive for LEDs.	3.28 MHz	24 pin DIP
ICM7215	6 Digit 4 Function LED stopwatch circuit. Features Minutes:Seconds:100ths. Provides Time out, Taylor and Split modes. Direct drive for LEDs.	3.28 MHz	24 pin DIP

Notes: All stopwatches may be purchased as an Evaluation Kit (EV KIT) which includes the IC and the appropriate quartz crystal. All operate at 2.5 to 4.5 volts, and source 15 mA current to the segments of the LEDs.

CMOS
ANALOG QUARTZ CLOCK(1)
SELECTION GUIDE

PRODUCT NUMBER	INTERSIL MASK VARIANT	CRYSTAL FREQUENCY (MHz)	MOTOR DRIVE OUTPUT	OUTPUT PULSE CHARACTERISTICS		ALARM FREQUENCY (Hz)	NOMINAL VOLTAGE (V)	TYPICAL CURRENT (I^+) (μA)	PACKAGE(4)
				Width (ms)	Freq. (pulses per sec)				
ICM7038A	—	4.19	Synchronous	7.8 (1)	64	512	3.0	90	8-pin DIP
ICM7038B	—	4.19	Synchronous	7.8 (1)	64	512	1.5	40	8-pin DIP
ICM7038C	—	4.19	Synchronous	15.6 (1)	32	512	3.0	90	8-pin DIP
ICM7038D	—	4.19	Synchronous	15.6 (1)	32	512	1.5	40	8-pin DIP
ICM7038E	—	4.19	Synchronous	31.2 (1)	16	512	1.5	40	8-pin DIP
ICM7038F	—	4.19	Synchronous	31.2 (1)	16	512	3.0	90	8-pin DIP
ICM7038G	—	4.19	Synchronous	62.5 (1)	8	512	1.5	40	8-pin DIP
ICM7049	ITS9026	4.19	Unipolar	7.8	1	1024+16+2	1.5	40	14-pin DIP
ICM7049	ITS9026	4.19	Unipolar	31.2 (1)	16				
ICM7049	ITS9026	4.19	Unipolar	125	1 per min				
ICM7049A	—	4.19	Unipolar	31.2	1	2048+8+1	1.5	40	8-pin DIP
ICM7049A	ITS9044-1	4.19	Unipolar	15.6	1	1024	1.5	40	8-pin DIP
ICM7049A	ITS9068	4.19	Unipolar	7.8	1	2048+8+1	1.5	40	8-pin DIP
ICM7050	—	4.19	Bipolar	46.9	1	2048+8+1	1.5	40	8-pin DIP
ICM7050	ITS9063	4.19	Bipolar	31.2	1	2048+8+1	1.5	40	8-pin DIP
ICM7050	ITS9064-1	4.19	Bipolar	500 (1)	1	2048+8+1	1.5	40	8-pin DIP
ICM7051A	ITS9042-1	4.19	Bipolar	7.8(1)	64	—	13.5(2)	500	8-pin DIP
ICM7051B	—	4.19	Bipolar	31.2	1	—	13.5(2)	500	8-pin DIP
ICM7052	—	4.19	Bipolar	31.2 or 500	1	4096+32+2+1 (3)	1.5	40	14-pin DIP
ICM1115A	—	4.19	Bipolar	500 (1)	1	64	1.5	80	8-pin DIP
ICM1115B	—	4.19	Bipolar	500 (1)	1	64	1.5	40	8-pin DIP
ICM7307	ITS9088	4.19	Unipolar	7.8	1	0.25	1.5	35	8-pin DIP
ICM7307	ITS9090	4.19	Unipolar	7.8	1	0.25(3)	1.5	35	8-pin DIP

All Intersil analog quartz products are mask programmable. Options include:

- Crystal frequency (32 kHz, 1 MHz, etc.)
- Pulse width (500 msec to 3.9 msec)
- Pulse frequency (64 Hz to 0.5 Hz)
- Alarm frequency (64 Hz to 4096 Hz, including complex)
- Motor drive characteristics
- Oscillator characteristics, including fixed capacitors (ICM7049A, ICM7050)

Notes: (1) Square wave
(2) For automotive service
(3) Includes snooze
(4) All Intersil analog quartz products may be ordered in die form.

ICM1424C/MC 5-Function LCD Watch Circuit

FEATURES

- **One chip system**
- **Very low current consumption: 1.5μA at 1.55 volt typical**
- **Drives standard 3-1/2 digit display with time, month, date, and seconds**
- **Voltage doubler requires only two external capacitors**
- **4-year perpetual calendar**
- **32 kHz oscillator requires only quartz crystal and trimming capacitor**
- **Fully protected against short circuits on all inputs and outputs**
- **Display button calls up all functions:**

NORMAL operation:

Run 1 (time only)

Press:		To:
DISPLAY	once	Display month/date
	again	Display seconds
	again	Return to RUN 1

RUN 2 (time alternating with month/date)

Press:		To:
SET	once	Enter RUN 2 from RUN 1
DISPLAY	once	Display seconds
	again	Return to RUN 2

SET operation: (begin with RUN 1 mode)

Press:		To:
SET	once	Switch to RUN 2
	again	Set month*
	again	Set date*
	again	Set hours*
	again	Set minutes*
	again	Return to RUN 1

*Selected counter advances once with each push of the DISPLAY button or at a 1Hz rate if it is held down.

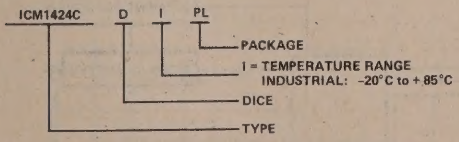
GENERAL DESCRIPTION

The ICM1424C is a fully integrated 5-function 3-1/2 digit liquid crystal watch circuit, fabricated using Intersil's low threshold metal gate CMOS process, and designed to interface easily with readily available LCD watch displays. The oscillator, frequency divider, counters, decoder, voltage multiplier and 32Hz display drivers are all included on chip. The only components required for a complete LCD watch in addition to the circuit are a battery, a 3 volt liquid crystal display, two 0.5μF capacitors, a 32768Hz quartz crystal, a trimming capacitor and two switches.

The circuit divides the oscillator frequency in 15 binary stages to a frequency of 1Hz. Some of the divider signals are used to drive the voltage multiplier (512Hz) and the liquid crystal outputs (32Hz). The 1Hz signal is counted down in the seconds, minutes, hours, date, day and month counters, which are selectively connected to the decoders based on the control logic. The decoder outputs determine the phase of the 32Hz signal on the segment outputs, in order to turn the segments on and off. The SPST switches (60 ms maximum switch bounce) control normal operation and setting of the watch. The seconds in both RUN 1 and RUN 2 stay on until commanded off, while all other demand functions automatically revert to the normal display.

The ICM1424MC is identical to the ICM1424C with the exception that the ICM1424C is designed to mount on the top of the watch substrate, while the mirror image MC device mounts on the bottom.

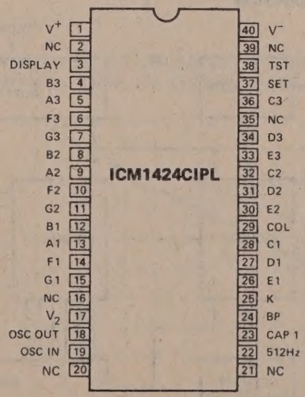
ORDERING INFORMATION



ORDER DICE BY FOLLOWING PART NUMBER: ICM1424C/D
ICM1424MC/D

ORDER DEVICES BY FOLLOWING PART NUMBERS: ICM1424CIPL

PIN CONFIGURATION (OUTLINE DRAWING PL)



Signal	Pin	Pin	Signal
V^+	1	40	V^-
NC	2	39	NC
DISPLAY	3	38	TST
B3	4	37	SET
A3	5	36	C3
F3	6	35	NC
G3	7	34	D3
B2	8	33	E3
A2	9	32	C2
F2	10	31	D2
G2	11	30	E2
B1	12	29	COL
A1	13	28	C1
F1	14	27	D1
G1	15	26	E1
NC	16	25	K
V_2	17	24	BP
OSC OUT	18	23	CAP 1
OSC IN	19	22	512Hz
NC	20	21	NC

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... -55°C to +125°C
Operating Temperature .... -10°C to +60°C
Power Dissipation[1] (Dice Only) .... 100 mW
Supply Voltage[2]
$V^+ - V^-$ 2.0V
$V^+ - V_2^-$ 5.5V
Input Voltage (Osc. In, Test, Set, Display) .... $V^- \leq V_{IN} \leq V^+$
Output Voltage (Osc. Out, 512) . $V^- \leq V_{OUT} \leq V^+$
(All Other Pins) .... $V_2^- \leq V_{OUT} \leq V^+$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

Notes:

1. The ICM1424/MC is fully short circuit protected on all inputs and outputs. However, if by forward biasing an input or output the device is put into a latchup condition, power dissipation must be limited to 100mW to prevent destruction of the device.
2. The ICM1424C/MC is intended for use with two power supplies, one of which is derived from an external battery (V^-) and the other is generated internally by the voltage multiplier (V_2^-). The common point of the two supplies is the most positive, V^+. If desired the circuit can be supplied with an external V_H by disconnecting the multiplier capacitors.

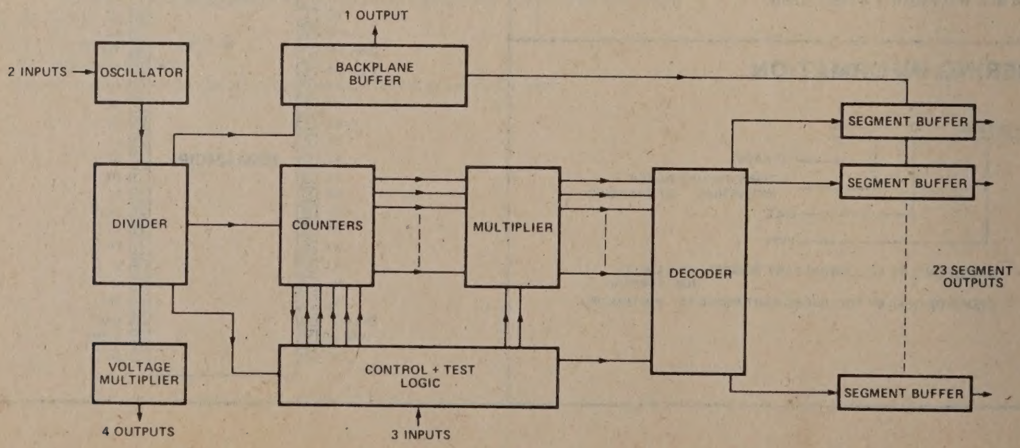
OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ = 1.55V$, voltage doubler connected, $T_A = 25°C$, watch circuit, unless otherwise specified. All voltages are expressed in absolute value.

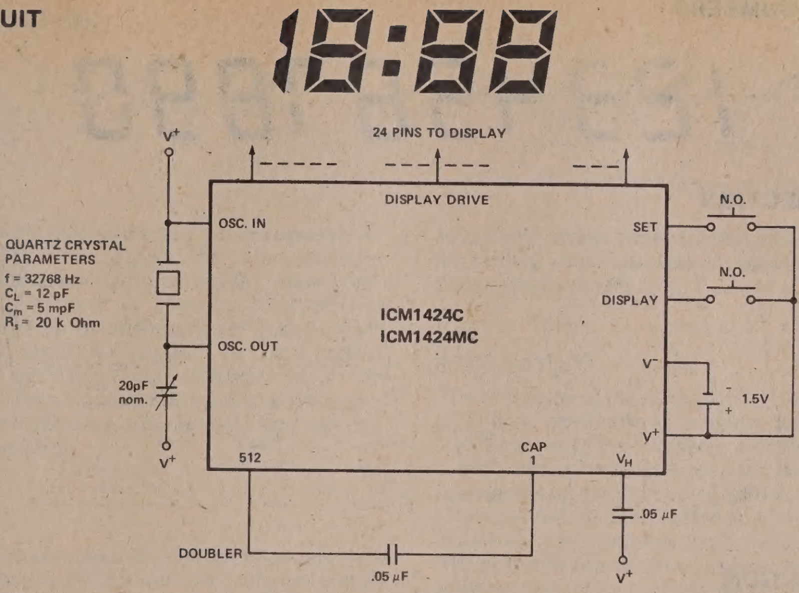
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V^+	$V^+ = 0V$ $-10°C < T_A < 60°C$	1.2		1.8	V
Supply Current	I^+	Display Disconnected		1.5	3.0	μA
Doubler Output Voltage	V_2^-	$V^- = 0V$ $I_H = 0.0\ \mu A$		3.1	2.9	V
		$I_H = 1.0\ \mu A$		3.0	2.8	V
512 Hz Drive Current	I_{512}	$V_{SAT} = 0.2V$ (Both Directions)	20			μA
Segment Drive Current	I_{SEG}	$V_{SAT} = 0.2V$ (Both Directions)	10			μA
Backplane Drive Current	I_{BP}	$V_{SAT} = 0.1V$ (Both Directions)	20			μA
Switch Actuation Current	I_{SW}	$V_{SW} = V_{DD}$		15		μA
Oscillator Stability	Δf	$V_{DD} = 0V$ $-1.55V \leq V_{SS} \leq -1.20V$ $C_{IN} = C_{OUT} = 25\ pF$		1.5		PPM
Oscillator Input Current[3]	$I_{OSC\ IN}$	'OSC IN' Connected to V_{DD} 'OSC OUT' Open Circuit		0.2		μA
Oscillator Input Capacitance	C_{IN}		20	25	30	pF
Oscillator Transconductance	g_m		10	15		μmho

3. The integrated oscillator biasing component has a nonlinear characteristic depending on the instantaneous values of the input and output voltages of the oscillator and the supply. Under oscillator startup conditions this component has a maximum value. See Application Notes, page 7-9.

BLOCK DIAGRAM

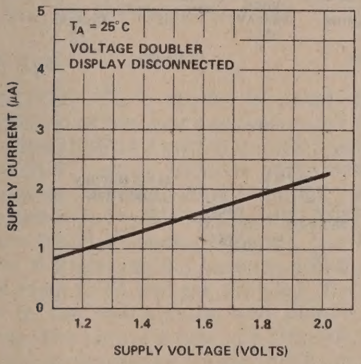


WATCH CIRCUIT

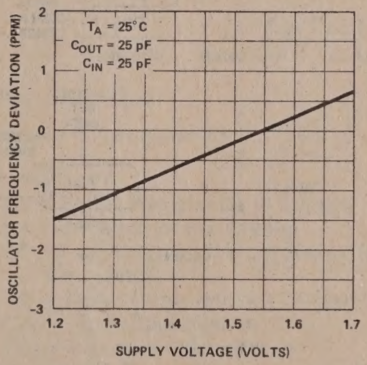

18:88
24 PINS TO DISPLAY
V+
DISPLAY DRIVE
OSC. IN
QUARTZ CRYSTAL PARAMETERS
f = 32768 Hz
C_L = 12 pF
C_m = 5 mpF
R_s = 20 k Ohm
ICM1424C
ICM1424MC
OSC. OUT
20pF nom.
V+
SET
N.O.
DISPLAY
N.O.
V−
1.5V
V+
512
CAP 1
V_H
.05 μF
V+
DOUBLER
.05 μF

TYPICAL PERFORMANCE CHARACTERISTICS

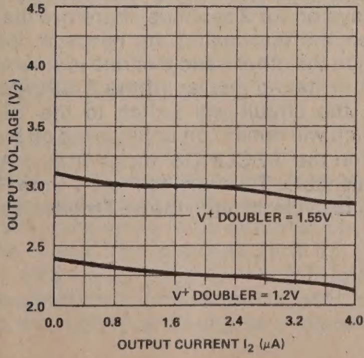
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



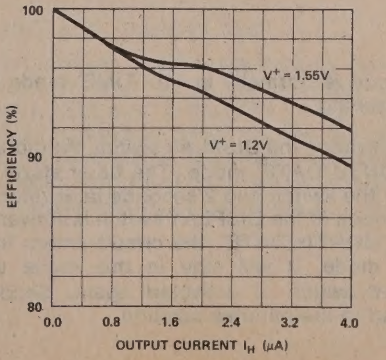
OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



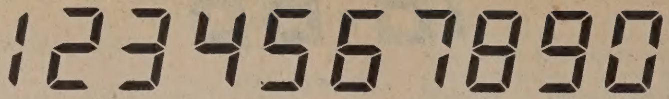
VOLTAGE DOUBLER OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



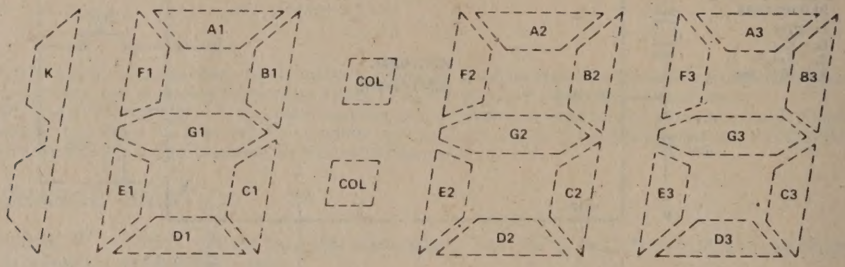
VOLTAGE DOUBLER EFFICIENCY AS A FUNCTION OF OUTPUT CURRENT



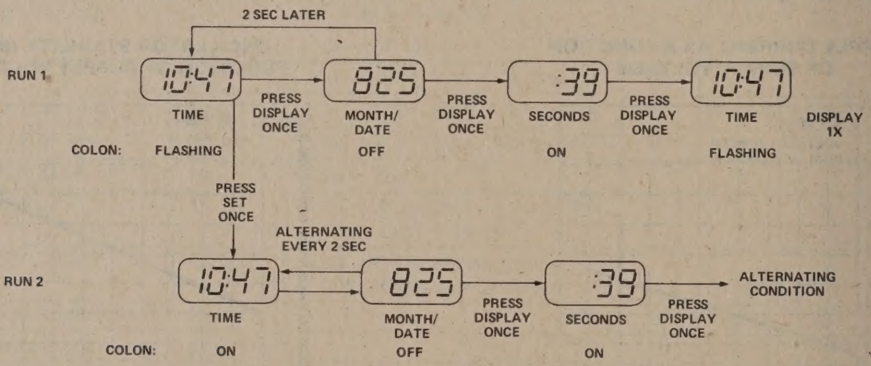
DISPLAY FONT NUMBERS



DISPLAY CONNECTION


K
A1
F1
B1
G1
E1
C1
D1
COL
COL
A2
F2
B2
G2
E2
C2
D2
A3
F3
B3
G3
E3
C3
D3

NORMAL OPERATION


2 SEC LATER
RUN 1
10:47
825
:39
10:47
PRESS DISPLAY ONCE
PRESS DISPLAY ONCE
PRESS DISPLAY ONCE
TIME
MONTH/ DATE
SECONDS
TIME
DISPLAY 1X
COLON:
FLASHING
OFF
ON
FLASHING
PRESS SET ONCE
ALTERNATING EVERY 2 SEC
RUN 2
10:47
825
:39
ALTERNATING CONDITION
TIME
MONTH/ DATE
PRESS DISPLAY ONCE
SECONDS
PRESS DISPLAY ONCE
COLON:
ON
OFF
ON

Two modes are provided for normal operation, the RUN 1 and RUN 2 mode, selectable by the user using the SET switch. In either mode only the DISPLAY switch is used to address the watch.

RUN 1

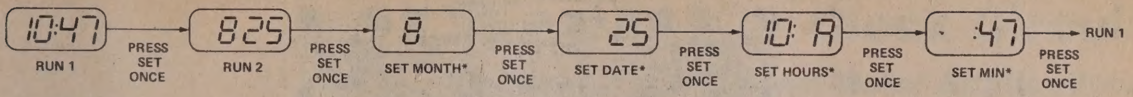
The circuit is normally in the 'TIME' mode with the colon flashing.

Upon activating the DISPLAY switch, the circuit enters the 'MONTH/DATE' mode. The timer starts after release of the switch and 2 seconds later returns to the 'TIME' mode. If the DISPLAY switch is activated again during 'MONTH/DATE', the circuit enters the 'SECONDS' mode. It will stay in this mode until the DISPLAY switch is activated again. Seconds are displayed in the minutes position.

RUN 2

This mode allows 'hands off' viewing of both time and month/date by cycling every 2 seconds between the 'TIME' mode (colon on) and 'MONTH/DATE'. Each display stays on for 2 seconds, therefore the user can always see the information he needs in less than 2 seconds. On the other hand this rate is slow enough to give a non-irritating display. If the DISPLAY switch is activated, the circuit will switch to the 'SECONDS' mode, which will remain on until turned off by the user. Note that in the 'SECONDS' mode RUN 1 AND 2 are indistinguishable. To return to RUN 1 from RUN 2 it is necessary to cycle through the SET modes. Press SET 5 times.

SETTING OPERATION



*Selected counter advances one with each push of the DISPLAY button or at a 1 Hz rate if DISPLAY held down.

Setting the ICM1424C/MC is carried out in a sequential manner. The SET input allows the user to cycle through two run modes and four set modes. In each set mode the DISPLAY input is used to advance the counter being set either by one count per push or at a 1 Hz rate if the DISPLAY switch is held down continuously. All set operations are independent, i.e. the counters following the one being set are inhibited; this allows convenient time zone adjustment without affecting date or month.

DATE SET

The perpetual calendar uses 28 days for February. In a leap year, on February 29, the watch will display March 1. To display February 29, change date to 29 first, then March to February.

HOURS SET

The ICM1424C/MC is intended for use with a display without AM/PM flags and shows an A in the minutes units position for AM and a P for PM.

MINUTES SET

The 'MINUTES SET' mode is used for exact synchronization of the watch as well as for setting the minutes. If the DISPLAY switch is not activated during 'MINUTES SET', neither seconds nor minutes will be affected and the next activation of the SET switch will return the circuit to the RUN 1 time mode with flashing colon. If the DISPLAY switch is used in the 'MINUTES SET' mode, the minutes will advance and the seconds counter is reset to 00 and put on hold. The user now advances to the next minute and pushes the SET switch once. The circuit is now in a TIME HOLD mode, showing hours, minutes and colon (not flashing), while the seconds are still held to 00. At the tone of the time signal push the DISPLAY switch. This will cause the watch to display month/date and back to time, while the seconds will start running at the time the switch is activated. Time setting accuracy is approximately 0.1 seconds.

APPLICATION NOTES

SYSTEM CONSIDERATIONS

The ICM1424C is designed to be mounted on the same side of the board substrate as the display; the ICM1424MC is designed to be mounted on the back-side of the board. The switches used for the watch should be SPST connected to V^+. The total system power consumption is sufficiently low that it is possible to replace the battery without loss of timekeeping. A 100μF low voltage capacitor should be connected across the battery terminals; this allows about 20 seconds for battery replacement.

OSCILLATOR

The oscillator of the ICM1424C/MC is designed for low frequency operation at very low currents from a 1.3 to 1.8 volt supply. The oscillator is of the inverter type with a non-linear feedback resistor having a maximum resistance under startup conditions included on chip. The nominal load capacitance of the crystal should be less than 15pF, typically 12pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance must be compatible with the characteristics of the circuit to insure startup and operation over a wide voltage range under worst case conditions. On chip oscillator capacitor ≈ 25pF.

The following expressions can be used to arrive at a crystal specification: Tuning range

$$\frac{\Delta f}{f} = \frac{C_m}{2\,(C_O + C_L)}\ ;\ C_L = \frac{C_{IN}\,C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for startup

$$g_m = 4\pi^2 f^2\, C_{IN}\, C_{OUT}\, R_S \left[1 + \frac{C_O}{C_L}\right]^2$$

here

R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance
C_m = Motional Capacitance of Crystal

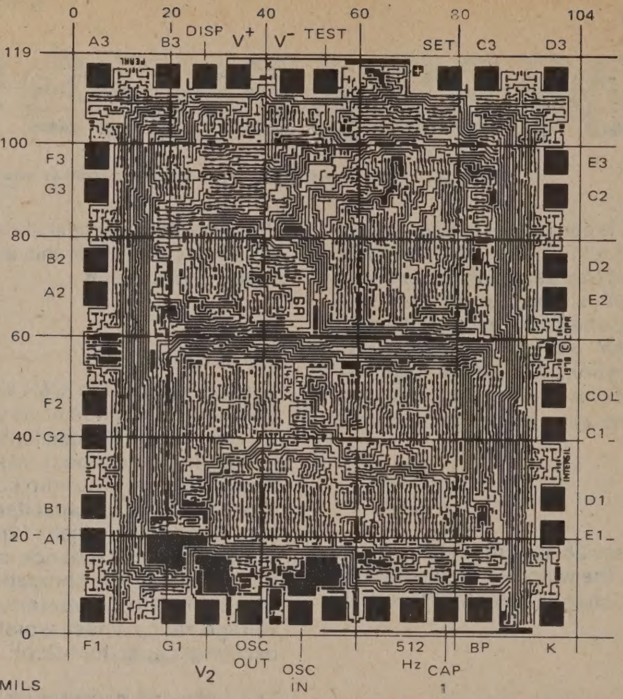
The g_m required for startup calculated should not exceed 50% of the g_m guaranteed for the device.

TEST POINT AND DISPLAY TEST

The circuit is reset to a known state by connecting SET, DISPLAY and TEST to V^+. This state is December 1, 12:00 a.m., in the RUN 1 mode. The TEST input, when connected to V^+ causes the circuit to speed up the seconds by 128 times, while inputs can then be applied at a rate of up to 500 Hz. The test point allows automatic testing of the device in a very short time.

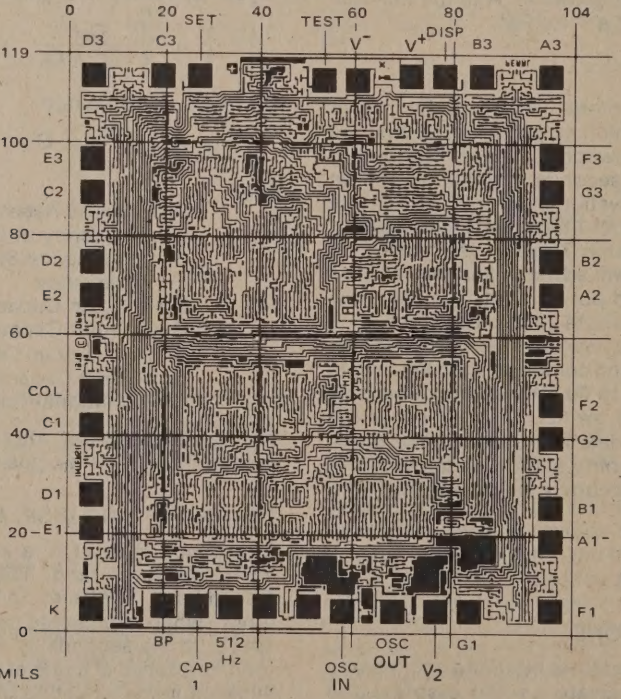
CHIP TOPOGRAPHY

ICM1424C


0
20
40
60
80
104
119
100
80
60
40
20
0
A3
B3
DISP
V+
V-
TEST
SET
C3
D3
F3
G3
B2
A2
F2
G2
B1
A1
E3
C2
D2
E2
COL
C1
D1
E1
F1
G1
V2
OSC OUT
OSC IN
512 Hz
CAP 1
BP
K

BOND PAD SIZE = 5x5 MILS

ICM1424MC


0
20
40
60
80
104
119
100
80
60
40
20
0
D3
C3
SET
TEST
V-
V+
DISP
B3
A3
E3
C2
D2
E2
COL
C1
D1
E1
K
F3
G3
B2
A2
F2
G2
B1
A1
F1
BP
CAP 1
512 Hz
OSC IN
OSC OUT
V2
G1

BOND PAD SIZE = 5x5 MILS

INTERSIL

ICM7038B/D/E/G CMOS Analog Quartz Clock Circuit

Synchronous Motor Applications

FEATURES

- **Single battery operation: 1.2 to 1.8 volt operation**
- **Very low power: 30μA typical**
- **High output current drive: 1 mA minimum**
- **Zero output bridge DC component (50% duty cycle square wave)**
- **All inputs fully protected — no special handling precautions required**
- **Wide temperature range: -20° C to +70° C**

GENERAL DESCRIPTION

The ICM7038 family of synchronous motor drivers is designed to operate from a 1.5V battery, and performs the functions of oscillator, frequency divider and output driver. In addition a power driver is tapped off from the thirteenth divider for use as an alarm driver.

Specifically the ICM7038 family uses an inverter oscillator having all biasing components on chip. Binary dividers permit frequency division from 4 MHz down to 64 Hz (ICM7038B). The output from the divider network drives a bridge output circuit which provides a 50% duty cycle AC square wave having virtually zero DC component for driving a synchronous single phase motor. The total output driver saturation is typically 200 ohms providing efficient operation of synchronous motors. The alarm output will drive a transducer (piezoelectric or speaker).

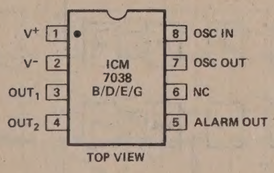
TABLE OF OPTIONS

The ICM7038 may be modified with alternative metal masks to provide any number of binary divider stages up to a maximum of 19 together with various output options. Consult your Intersil representative or the factory for further information. The alarm output can be tapped off from any of the latter divider stages.

(See table for standard options).

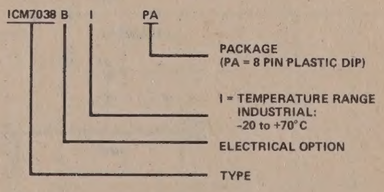
Part Number	Binary Dividers	Output Frequency (50% Duty Cycle Square Wave)
ICM7038B	16	64 Hz
ICM7038D	17	32 Hz
ICM7038E	18	16 Hz
ICM7038G	19	8 Hz

PIN CONFIGURATION (OUTLINE DRAWING PA)



PIN 1 IS DESIGNATED BY EITHER A DOT OR A NOTCH.

ORDERING INFORMATION


ICM7038 B I PA
PACKAGE (PA = 8 PIN PLASTIC DIP)
I = TEMPERATURE RANGE INDUSTRIAL: -20 to +70°C
ELECTRICAL OPTION
TYPE

ORDER DEVICES BY FOLLOWING PART NUMBER—
ICM7038B I PA

ORDER DICE BY FOLLOWING PART NUMBER—
ICM7038C/D

ABSOLUTE MAXIMUM RATINGS

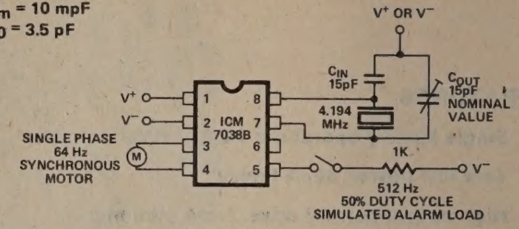
Power Dissipation Output Short Circuit[1]	300mW
Supply Voltage	3V
Output Voltage[2]	3V
Input Voltage[2]	3V
Storage Temperature	-30°C to +125°C
Operating Temperature	-20°C to +70°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

TEST CIRCUIT

QUARTZ CRYSTAL PARAMETERS

f = 4,194,304 Hz
R_S = 35Ω
C_m = 10 mpF
C_0 = 3.5 pF


V+ OR V−
V+
V−
1
2
3
4
8
7
6
5
ICM 7038B
SINGLE PHASE 64 Hz SYNCHRONOUS MOTOR
M
CIN 15pF
COUT 15pF NOMINAL VALUE
4.194 MHz
1K
V−
512 Hz 50% DUTY CYCLE SIMULATED ALARM LOAD

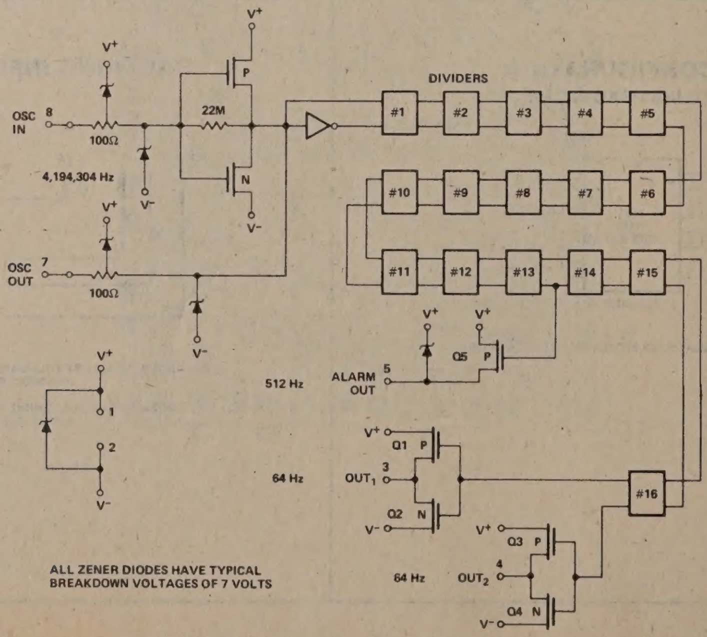
NOTES:
1. This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.
2. Except for instantaneous static discharges all terminals may exceed the supply voltage (2.0V max) by ±0.5 volt provided that the currents in these terminals are limited to 2 mA each.

TYPICAL OPERATING CHARACTERISTICS

(V^+ = 1.5V, f_{osc} = 4,194,304 Hz test circuit 1, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current	I^+			30	60	μA
Guaranteed Operating Voltage Range	V^+	-20°C ≤ to ≤ 70°C	1.2		1.8	V
Total Output Saturation Resistance	R_{SAT}	p+n Output Transistors, I_{OUT} = 0.5mA		200	700	Ω
Alarm Output Saturation Resistance	R_{AL}	I_{OUT} = 1mA		300	800	Ω
Oscillator Stability	f_{STAB}	1.2V < V^+ < 1.6V C_{IN} = C_{OUT} = 15pF		1		ppm
Oscillator Start-Up Time	t_{start}	V^+ = 1.2V			1.0	sec

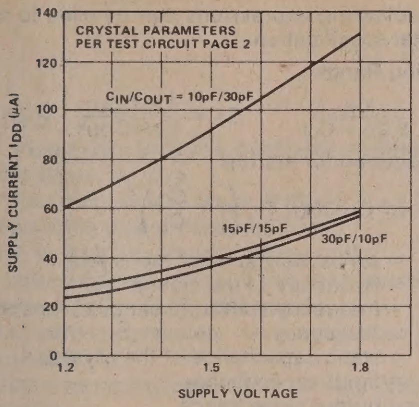
SCHEMATIC DIAGRAM (ICM7038B)


V+
V+
P
N
22M
V−
OSC IN 8
100Ω
4,194,304 Hz
V+
V−
OSC OUT 7
100Ω
V−
DIVIDERS
#1
#2
#3
#4
#5
#10
#9
#8
#7
#6
#11
#12
#13
#14
#15
V+
V+
Q5
P
ALARM OUT 5
512 Hz
V+
1
2
V−
64 Hz
V+
Q1 P
OUT1 3
Q2 N
V−
#16
V+
Q3 P
OUT2 4
64 Hz
Q4 N
V−

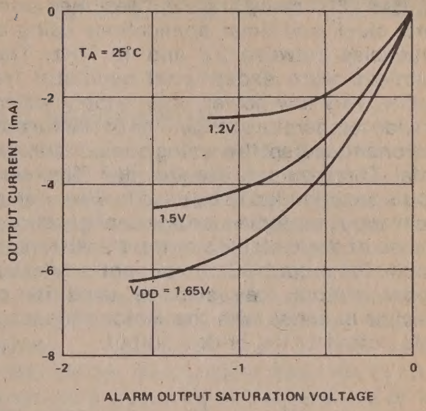
ALL ZENER DIODES HAVE TYPICAL BREAKDOWN VOLTAGES OF 7 VOLTS

TYPICAL OPERATING CHARACTERISTICS

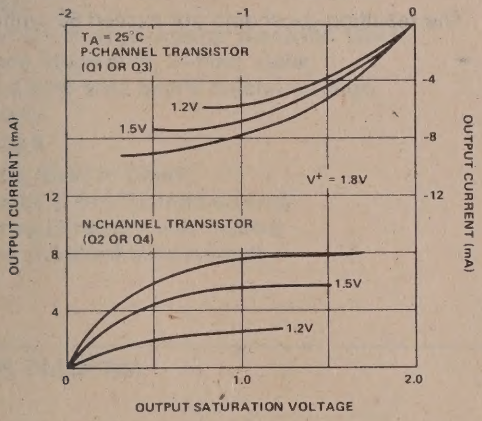
SUPPLY CURRENT VS. SUPPLY VOLTAGE



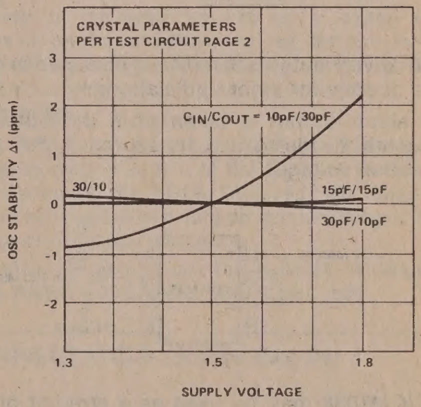
ALARM OUTPUT CURRENT (SOURCE) VS. OUTPUT SATURATION VOLTAGE



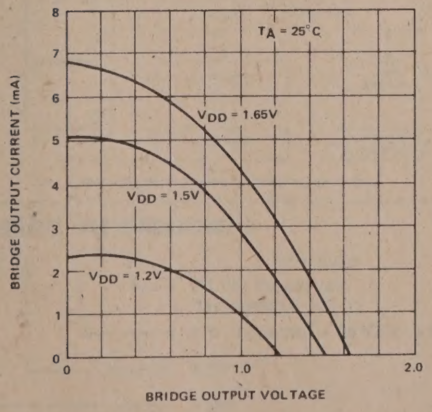
OUTPUT CURRENT (SOURCE) VS. OUTPUT SATURATION VOLTAGE



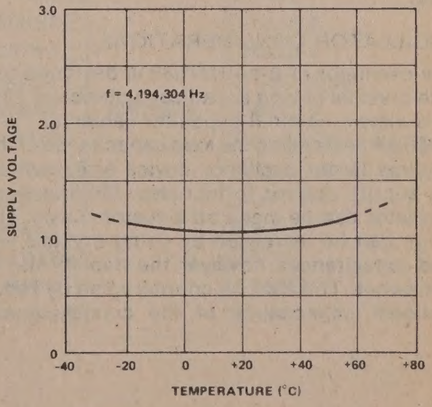
OSCILLATOR STABILITY VS. SUPPLY VOLTAGE



BRIDGE OUTPUT CURRENT VS. BRIDGE OUTPUT VOLTAGE



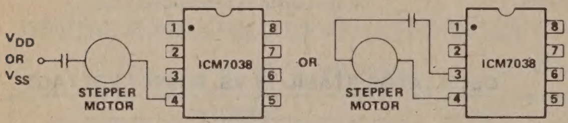
MINIMUM OPERATING SUPPLY VOLTAGE VS. TEMPERATURE



APPLICATION NOTES

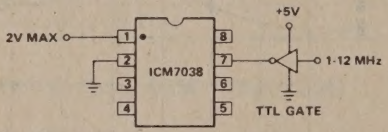
GENERAL DESCRIPTION

The ICM7038 Family has been designed primarily for quartz clock and timer applications using oscillator frequencies between 2.0 and 10 MHz. The design objectives were exceptional oscillator frequency stability, very low power, wide supply voltage range and wide temperature range. The oscillator contains all components except the tuning components and quartz crystal. Three outputs are provided. The two principal outputs are intended to be used to drive a single phase synchronous motor in a bridge configuration. As such, because of the matching of the transistors in the two outputs, the output DC component is extremely small. Stepper motors may also be used by placing a capacitor in series with the motor and using either a single output or the bridge output.



Alternatively outputs 3 and 4 may be used to drive TTL logic directly for timer applications.

The alarm output is taken from the output of the thirteenth divider and can source 1 mA at a low saturation voltage.



The ICM7038 may be used as a straight divider by driving directly into the oscillator output (pin no. 7) with a low impedance square wave drive. As such it may be used over the frequency range 1 MHz to 10 MHz.

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7038 is designed to operate with crystals having a load capacitance of 10 to 12 pF. This allows nominal capacitor values of 15/15 pF or 20/20 pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however, the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor is provided on chip, which has a maximum value at start up. Oscillator tuning should be done at the oscillator output.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)} \qquad C_L = \frac{C_{IN}C_{OUT}}{C_{IN}+C_{OUT}}$$

g_m required for startup

$$g_m = \omega^2 C_{IN}C_{OUT} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

R_S = series resistance of the crystal
f = frequency of the crystal
Δf = frequency shift from series resonance frequency
C_O = static capacitance of the crystal
C_{IN} = input capacitance
C_{OUT} = output capacitance
C_L = load capacitance
C_m = motional capacitance
ω = $2\pi f$

The resulting g_m should not exceed 50 μmhos

ICM7045/A CMOS Precision Decade Timers

FEATURES

- **Total integration: includes oscillator, divider, decoder driver on chip**
- **Wide operating supply range: $2.5V \le V^+ \le 4.5V$**
- **Low operating power consumption: 0.9 mW @ 3.6V supply with display off**
- **High output current drive: 18 mA peak current per segment with 12.5% duty cycle.**
- **Leading zero suppression: timer stopwatch applications**
- **Fractional second suppression: 24-hour clock application**
- **Short duration short circuit protection on all inputs and outputs at 3.6V supply**

ICM7045

- **Versatility of applications: precision timer, 4 mode stopwatch, 24-hour clock**
- **Uses 6.5536 MHz quartz crystal for high accuracy**

ICM7045/A

- **May Be Used to Count**
  - **–Seconds (1.310772 MHz crystal)**
  - **–Minutes (2.184533 MHz crystal)**
  - **–Hours (3.640889 MHz crystal)**

GENERAL DESCRIPTION

The ICM7045/A are fully integrated precision decade timers fabricated using Intersil's low voltage metal gate C-MOS technology. The oscillator, frequency divider, multiplexer, decoder, segment and digit output buffers are all included on-chip. The circuits are designed to interface directly with fully multiplexed 8-digit 7-segment common cathode LED displays. The normal supply voltage is 3.6V, equivalent to a stack of three nickel cadmium batteries.

The ICM7045

The ICM7045 divides the oscillator frequency in sixteen binary stages to a frequency of 100 Hz; some of these intermediate outputs are used to generate the multiplex waveforms at a 12.5% duty cycle/800 Hz rate. The 100 Hz signal is then processed in the counters and multiplexed in the decoders.

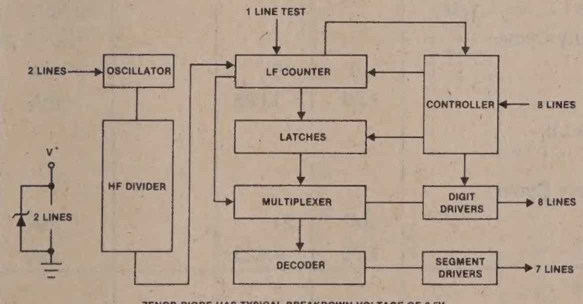
This circuit is designed for use as a digital timer, 4-function stopwatch and 24 hour clock; the only external components required are the display, batteries, 6.5536 MHz crystal, turning capacitor and 4 switches.

The ICM7045A

The main difference between the 7045 and 7045A is that the divide by sixty counters of the 7045 are replaced by decade counters in the 7045A. Thus seconds, minutes or hours may be counted in a decade fashion, depending on the choice of oscillator frequency.

The two other differences are: the oscillator is divided by 2^{17} in the 7045A, and CATH 8 (LSD) is not used.

BLOCK DIAGRAM


1 LINE TEST
2 LINES
OSCILLATOR
LF COUNTER
CONTROLLER
8 LINES
LATCHES
V+
HF DIVIDER
2 LINES
MULTIPLEXER
DIGIT DRIVERS
8 LINES
DECODER
SEGMENT DRIVERS
7 LINES

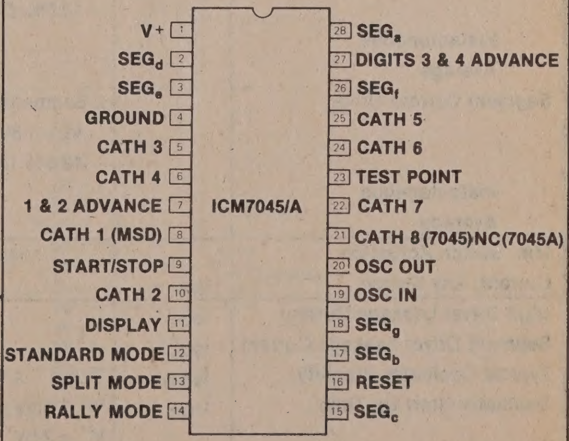
ZENOR DIODE HAS TYPICAL BREAKDOWN VOLTAGE OF 6.5V.

ORDERING INFORMATION

ICM7045 A I DI
Package
28 Pin Plastic DIP
Temperature Range
I = Industrial −20°C to +85°C
Option
Type

Order Dice by Following Part Number — ICM7045/D, ICM7045A/D

PIN CONFIGURATION (outline dwg DI)


V+ 1
SEGd 2
SEGe 3
GROUND 4
CATH 3 5
CATH 4 6
1 & 2 ADVANCE 7
CATH 1 (MSD) 8
START/STOP 9
CATH 2 10
DISPLAY 11
STANDARD MODE 12
SPLIT MODE 13
RALLY MODE 14
ICM7045/A
28 SEGa
27 DIGITS 3 & 4 ADVANCE
26 SEGf
25 CATH 5
24 CATH 6
23 TEST POINT
22 CATH 7
21 CATH 8 (7045) NC (7045A)
20 OSC OUT
19 OSC IN
18 SEGg
17 SEGb
16 RESET
15 SEGc

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (1)	1W
Supply Voltage	+5.5V
Input Voltage	Equal to, but never in excess of the supply voltages
Output Voltage	Equal to, but never in excess of the supply voltages
Digit Drive Output Current	150mA/digit
Storage Temperatures	−55°C to +125°C
Operating Temperatures	−20°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

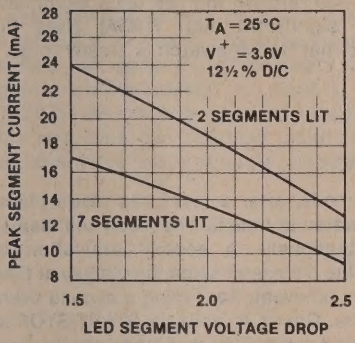
TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V+ = 3.6V$, $T_A = 25°C$ Parameters listed are absolute value

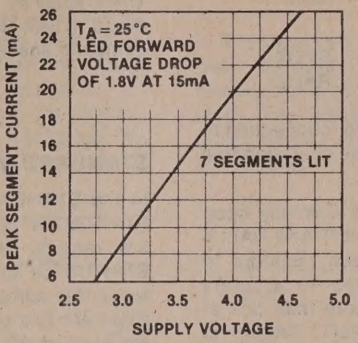
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I+	Display Off		180	2000	μA
		7 Segments Lit $V_F = 1.8V$	70	105		mA
		2 Segments Lit $V_F = 1.8V$	28	42		mA
Operating Voltage	V^+	$-20°C < T_A < 85°C$	2.5		4.5	V
Segment Current Drive	I_{SEG}	7 Segments I.T., $V_F = 1.8V$, 12.5% Duty Cycle				
Instantaneous			10	15		mA
Average			1.25	1.825		mA
Segment Current Drive		2 Segments Lit, $V_F = 1.8V$ 12.5% Duty Cycle				
Instantaneous			14	21		mA
Average			1.75	2.625		mA
Min. Switch Actuation Current, Any Switch	I_{SW}		50			μA
Digit Driver Leakage Current	I_{DLK}				200	μA
Segment Driver Leakage Current	I_{SLK}				200	μA
Typical Oscillator Stability	f_{STAB}	$3V \leq V^+ \leq 4V$, $C_{TUNING} = 15pF$		1.0		ppm
Oscillator Start Up Time	t_{start}	$V^+ = 3.6V$			0.1	sec
		$V^+ = 2.5V$			1.0	sec
Oscillator Input Capacitance	C_{IN}			17		pF

TYPICAL PERFORMANCE CURVES

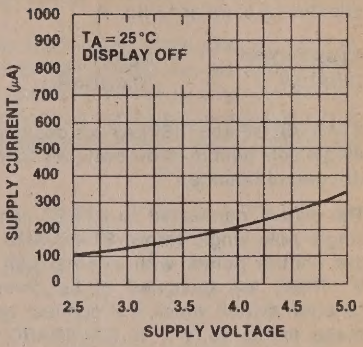
PEAK SEGMENT CURRENT DRIVE
VS.
LED SEGMENT VOLTAGE DROP



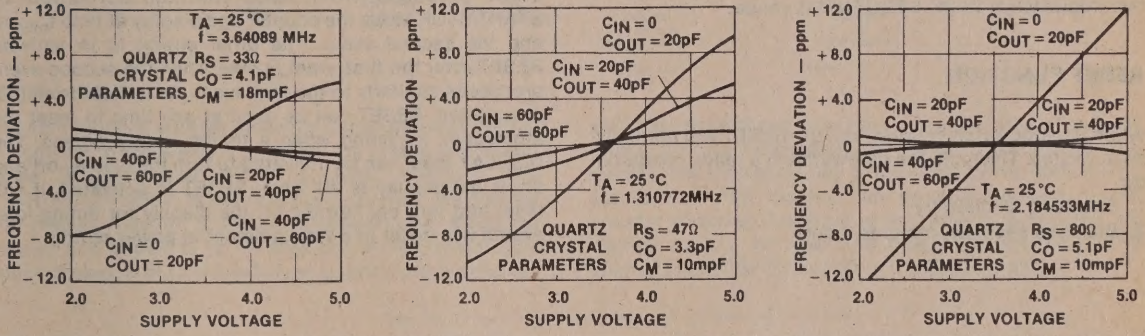
PEAK SEGMENT CURRENT
VS.
SUPPLY VOLTAGE



SUPPLY CURRENT
VS.
SUPPLY VOLTAGE

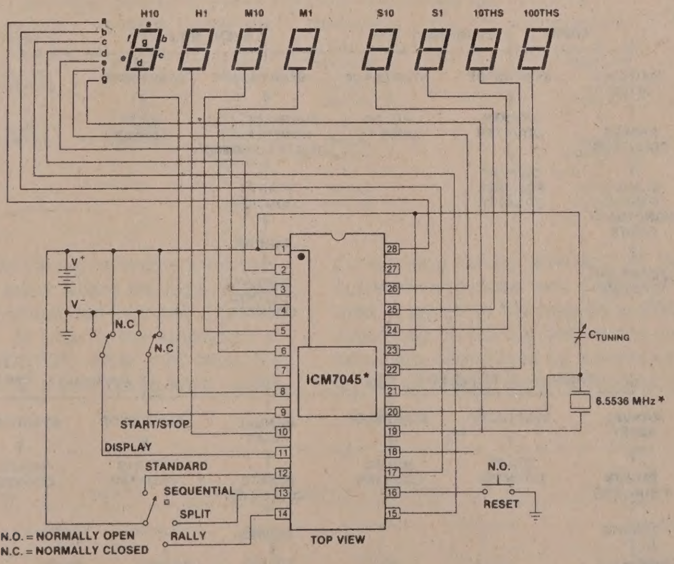


OSCILLATOR STABILITY VS. SUPPLY VOLTAGE FOR 3 DIFFERENT QUARTZ CRYSTALS (ICM7045A)



ICM7045

Quartz Crystal Parameters
f = 6.5536 MHz
$R_s = 40Ω$
$C_1 = 15mpF$
$C_O = 3.5pF$


H10
H1
M10
M1
S10
S1
10THS
100THS
a
b
c
d
e
f
g
V^+
V^-
N.C
N.C
START/STOP
DISPLAY
STANDARD
SEQUENTIAL
SPLIT
RALLY
N.O. = NORMALLY OPEN
N.C. = NORMALLY CLOSED
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
ICM7045*
TOP VIEW
C_{TUNING}
6.5536 MHz*
N.O.
RESET

*Shown for ICM7045. The same circuit may be used with the 7045A if a different crystal frequency is chosen.

NOTE: Specify quartz crystal to have nominal frequency value when tuned by a total parallel capacitance value of 12 pF or less.

Figure 1: Four Stopwatch Modes

FUNCTIONAL OPERATION

STOPWATCH/TIMER OPERATION

The control inputs used in the complete stopwatch application are: (refer to fig. 1)

START/STOP
RESET
SPLIT
DISPLAY
STANDARD
RALLY

START/STOP and DISPLAY are designed for connection to single pole double throw switches to insure operation free of contact bounce.

The switch connected to RESET can be normally open single pole single throw. STANDARD, SPLIT and RALLY are control points with internal pull down resistors to V^-.These are designed to be connected to a rotary function switch which will connect no more than one of these points to V^+. If STANDARD (SPLIT, RALLY) is connected to $V+$ the stopwatch is said to be in the STANDARD (SPLIT, RALLY) mode. If all three are left open, the stopwatch is in the SEQUENTIAL mode.

RESET FUNCTION

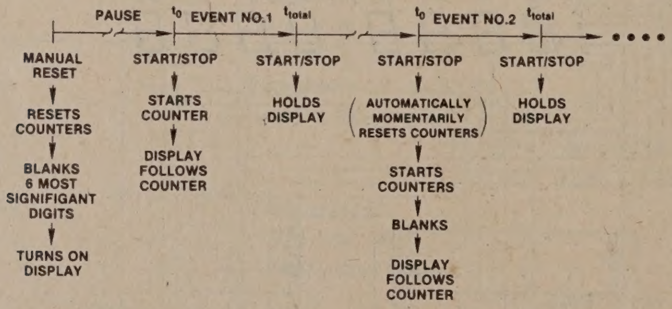
When the stopwatch is turned on, the RESET will normally be activated. This puts the stopwatch in a ready condition by:

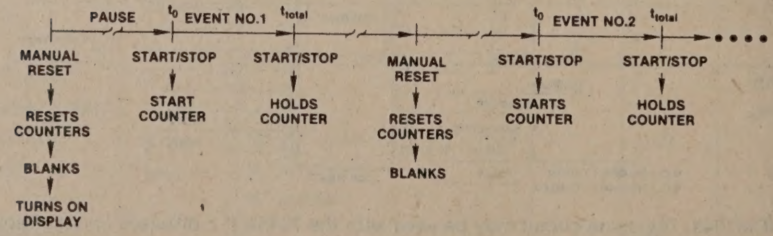
1. Resetting all circuitry
2. Blanking seconds, minutes, hours
3. Showing 00 in the two least significant digits. (7045; least significant digit 7045A)
4. Turning on the display if it was previously turned off

The display of just two zeros in the two least significant digits (7045; least significant digit 7045A) gives the complete assurance that the stopwatch is "ready to go."

STANDARD MODE

In the STANDARD mode, after a reset has taken place, START/STOP is activated at time t_0. The clock and display are moving simultaneously. A second activation of START/STOP stops the clock and holds the display at time t_{total}. This completes an event. For timing a second event there are two options. One is to activate START/STOP at the start of the second event. This will momentarily reset the counter and display so that the timing of the second event proceeds from zero. Another activation of START/STOP stops the counter and display at time t_{total} to end the second event. The other option is to activate RESET after the first event is over. Then the second event proceeeds similarly to the first event. As is clear from this description, RESET can be used at any time to reset the stopwatch, including when a timing is in progress. The DISPLAY input can be activated to turn the display off and on. If the display is off when RESET is activated, it will reset and turn on. Turning off the display for timing long events will result in a very substantial power saving.


PAUSE
t0 EVENT NO.1 ttotal
t0 EVENT NO.2 ttotal
MANUAL RESET
RESETS COUNTERS
BLANKS 6 MOST SIGNIFIGANT DIGITS
TURNS ON DISPLAY
START/STOP
STARTS COUNTER
DISPLAY FOLLOWS COUNTER
START/STOP
HOLDS DISPLAY
START/STOP
(AUTOMATICALLY MOMENTARILY RESETS COUNTERS)
STARTS COUNTERS
BLANKS
DISPLAY FOLLOWS COUNTER
START/STOP
HOLDS DISPLAY

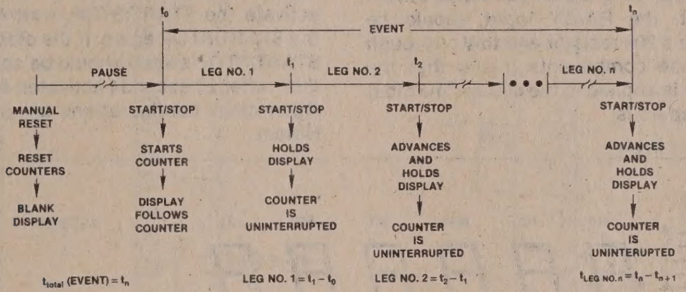

PAUSE
t0 EVENT NO.1 ttotal
t0 EVENT NO.2 ttotal
MANUAL RESET
RESETS COUNTERS
BLANKS
TURNS ON DISPLAY
START/STOP
START COUNTER
START/STOP
HOLDS COUNTER
MANUAL RESET
RESETS COUNTERS
BLANKS
START/STOP
STARTS COUNTER
START/STOP
HOLDS COUNTER

SEQUENTIAL MODE

The sequential mode of the stopwatch is designed for timing events consisting of more than one leg (such as relays, multilap races, etc.). After the initial reset the START/STOP is activated at t_0 to start the event. A second activation of START/STOP at time t_1 stops the display and allows t_1 to be read out, while the clock resets and starts counting again instantaneously. At time t_2 an activation of START/STOP enters t_2 (the time of leg 2) into the display. This sequence can continue indefinitely. Assuming the total event has n legs, the total elapsed time is then equal to the sum of the n times read out:

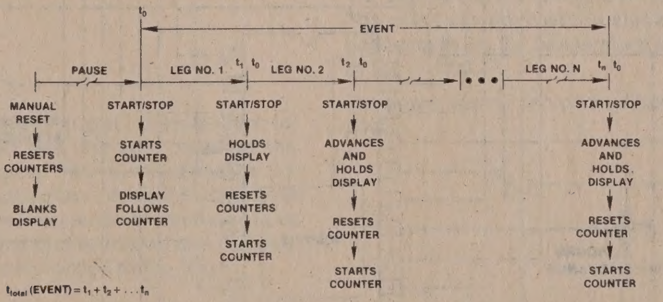
$$t_{total} = t_1 + t_2 . . . + t_n$$

If it is desired to see the moving clock after a time has been recorded, the DISPLAY switch can be activated to release the display hold and catch up with the moving clock. The display cannot be turned off in the sequential mode. RESET can be activated at any time to reset clock and display.


t_0
EVENT
t_n
PAUSE
LEG NO. 1
t_1
LEG NO. 2
t_2
LEG NO. n
MANUAL RESET
RESET COUNTERS
BLANK DISPLAY
START/STOP
STARTS COUNTER
DISPLAY FOLLOWS COUNTER
START/STOP
HOLDS DISPLAY
COUNTER IS UNINTERRUPTED
START/STOP
ADVANCES AND HOLDS DISPLAY
COUNTER IS UNINTERRUPTED
START/STOP
ADVANCES AND HOLDS DISPLAY
COUNTER IS UNINTERUPTED
t_{total} (EVENT) = t_n
LEG NO. 1 = $t_1 - t_0$
LEG NO. 2 = $t_2 - t_1$
$t_{LEG\ NO.\ n} = t_n - t_{n+1}$

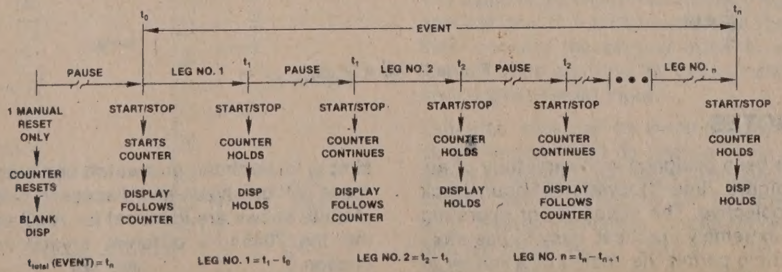
SPLIT MODE

The split mode is another mode for timing multileg events. In contrast to the sequential mode, the timing in the split mode is cumulative. From a reset condition, the START/STOP switch is activated at t_0 to start the counter and display running. A second activation at t_1 stops the display and allows t_1 to be read out while counter continues timing. A third activation at t_2 advances the display with the total elapsed time from t_0 to t_2 showing. Finally, at time t_n the total elapsed time of the event is entered in the display. The time of one leg of the event can be obtained by subtraction. The display can be synchronized to the counter (catch-up function) at any time by activating the display switch. To reset the timer, activate reset. The display cannot be turned off in the SPLIT mode.


t_0
EVENT
PAUSE
LEG NO. 1
t_1 t_0
LEG NO. 2
t_2 t_0
LEG NO. N
t_n t_0
MANUAL RESET
RESETS COUNTERS
BLANKS DISPLAY
START/STOP
STARTS COUNTER
DISPLAY FOLLOWS COUNTER
START/STOP
HOLDS DISPLAY
RESETS COUNTERS
STARTS COUNTER
START/STOP
ADVANCES AND HOLDS DISPLAY
RESETS COUNTER
STARTS COUNTER
START/STOP
ADVANCES AND HOLDS DISPLAY
RESETS COUNTER
STARTS COUNTER
t_{total} (EVENT) = $t_1 + t_2 + . . . t_n$

RALLY MODE

The rally mode is designed for timing of events with interruptions. Consider an n leg event where the legs may be separated by intervals which should not be timed. The rally mode starts with a RESET. At time t_0 the stopwatch is started by activating START/STOP. After this point the RESET function is disabled to prevent accidental resets during long timing intervals. At time t_1 a START/STOP pulse stops counter and display. From here on each leg time is added to the total by a START/STOP pulse at the beginning of the leg and at the end. The individual leg times are determined by subtraction. The display can be turned on and off with the display switch.


t_0
EVENT
t_n
PAUSE
LEG NO. 1
t_1
PAUSE
t_1
LEG NO. 2
t_2
PAUSE
t_2
LEG NO. n
1 MANUAL RESET ONLY
COUNTER RESETS
BLANK DISP
START/STOP
STARTS COUNTER
DISPLAY FOLLOWS COUNTER
START/STOP
COUNTER HOLDS
DISP HOLDS
START/STOP
COUNTER CONTINUES
DISPLAY FOLLOWS COUNTER
START/STOP
COUNTER HOLDS
DISPLAY HOLDS
START/STOP
COUNTER CONTINUES
DISPLAY FOLLOWS COUNTER
START/STOP
COUNTER HOLDS
DISP HOLDS
t_{total} (EVENT) = t_n
LEG NO. 1 = $t_1 - t_0$
LEG NO. 2 = $t_2 - t_1$
LEG NO. n = $t_n - t_{n+1}$

CLOCK OPERATION

The control inputs used in a possible 24-hour clock configuration are (refer to fig. 2):

START/STOP
MINUTES ADVANCE
HOURS ADVANCE
RALLY

START/STOP, MINUTES ADVANCE and HOURS ADVANCE are designed for connection to single pole double throw switches; this assures contact bounce elimination on these inputs. To avoid an additional switch for the DISPLAY input, the RALLY input should be connected to V+ through a 20k resistor and to V− through a 0.01μF capacitor. These components insure that the display is on when power is applied to the circuit. The most convenient setting procedure is:

1. If clock is not running when power is applied activate START/STOP switch.
2. Depress MINUTES ADVANCE switch to obtain correct minutes setting, one minute count per activation.
3. Depress HOURS ADVANCE switch to obtain correct HOURS setting, one hour count per activation.

It is possible to set the clock more accurately or to correct small time errors by using START/STOP in combination with MINUTES ADVANCE. If the clock is, for instance, 20 seconds slow, activate the MINUTES ADVANCE once, then activate the START/STOP, wait 40 seconds and activate the START/STOP again. If the clock is 20 seconds fast, the START/STOP switch should be activated to stop the clock, then after 20 seconds activated again to restart the clock. Other clock configurations are possible (see Application Notes).

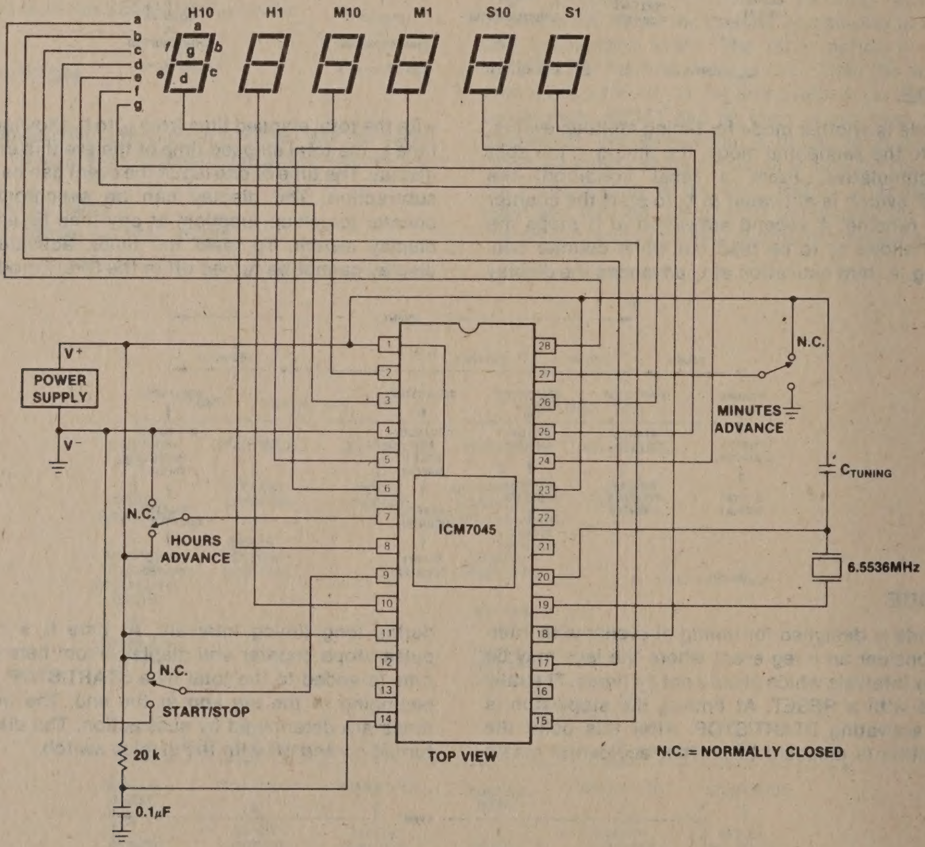


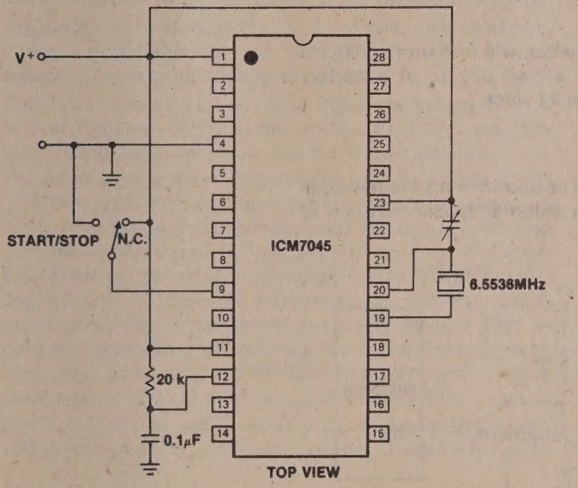
Figure 2: Clock Mode

APPLICATION NOTES

The ICM7045/A have been designed with versatility of applications in the digital timer/stopwatch/24-hour clock field as the major objective. The simplicity of operating modes allow for an extremely practical, easy to use stopwatch, at the same time permit the design of a variety of simple lapse timer, stopwatch and clock circuits; a few of these will be shown and discussed briefly here. Note that circuits shown are identical for 7045 and 7045A. When using the 7045A, a different crystal frequency must be chosen.

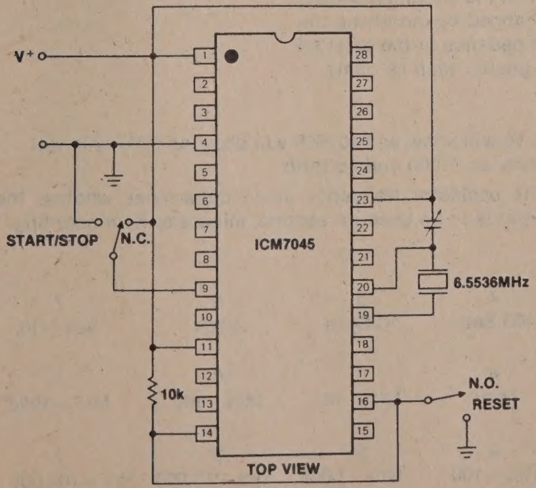
TIMER CIRCUIT I

This simple circuit (display connections not shown) allows interval timing up to 24 hours with a resolution of 0.01 second. Each interval is timed by one start and one stop pulse on the start/stop line. The start pulse for the next interval to be timed automatically resets the timer. Leading zero suppression is automatic.


V+
START/STOP
N.C.
ICM7045
6.5536MHz
20 k
0.1μF
1 2 3 4 5 6 7 8 9 10 11 12 13 14
28 27 26 25 24 23 22 21 20 19 18 17 16 15
TOP VIEW

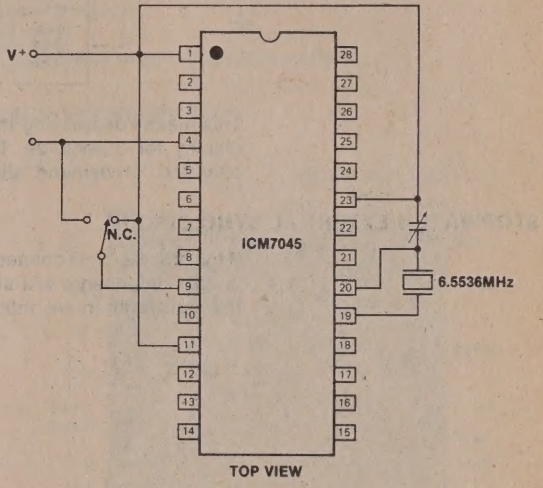
TIMER CIRCUIT II

This circuit allows cumulative timing of intervals. Each interval is timed by one start and one stop pulse on the start/stop line. Each subsequent interval timed adds to the total line displayed. The reset switch allows the timer to be reset to zero to start another sequence of intervals. Note that the time between the end of one interval and the start of the reset is not recorded nor added to the total.


V+
START/STOP
N.C.
ICM7045
6.5536MHz
10k
N.O.
RESET
1 2 3 4 5 6 7 8 9 10 11 12 13 14
28 27 26 25 24 23 22 21 20 19 18 17 16 15
TOP VIEW

TIMER CIRCUIT III

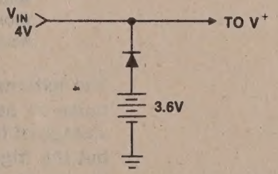
This circuit allows interval timing with a single pulse on the start/stop line. Each pulse enters the time elapsed since the previous pulse into the display, resets the timer and starts the timer for the next interval.


V+
N.C.
ICM7045
6.5536MHz
1 2 3 4 5 6 7 8 9 10 11 12 13 14
28 27 26 25 24 23 22 21 20 19 18 17 16 15
TOP VIEW

CLOCK CIRCUIT I

The standard clock circuit is shown and described in fig. 2. The clock accuracy with a stable voltage supply will depend mostly on the temperature and aging characteristics of the crystal.

The power supply can be modified to give battery standby power.

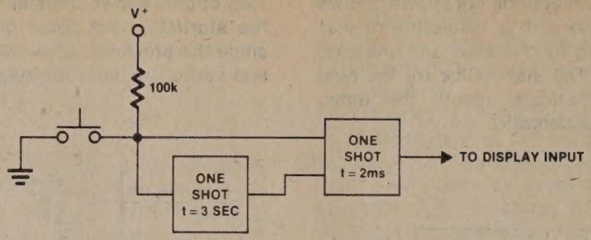

V_{IN}
4V
TO V+
3.6V

The standby circuit should be designed to provide the specified minimum voltage to the ICM7045.

OTHER CLOCK CIRCUITS

The basic clock circuit can be modified for various special applications. If it is desired to turn the display on and off, then connect the display input to an additional SPDT switch, while omitting the capacitor/resistor combination on the STANDARD Input.

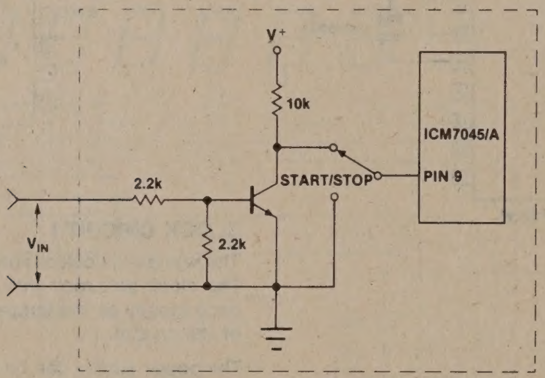
This input can then be wired directly to V^+. This 24-hour clock version might be applicable to vehicles, boats, etc. where a battery is available to supply the display off clock current, while the display can be turned on with the ignition. Another possible configuration would connect a special circuit to the DISPLAY input which generates a double pulse about 3 seconds apart:



This means depressing the switch will turn on the clock's display for 3 seconds. This allows design of a battery operated "on demand" digital 24-clock.

STOPWATCH EXTERNAL SYNC CIRCUIT

If the stopwatch is connected as shown in fig.1, a few additional components will allow external synchronization of the stopwatch in any mode:



NOTE: Be sure to minimize the distance between the transistor and the ICM7045 to prevent noise from being generated along this connection. *Noise spikes absolutely must not exceed the supply voltages.*

The external sync signal source must supply a positive pulse to activate the START/STOP input. The minimum voltage of this pulse is about 1.2V in the circuit as shown, but the triggering level can be changed by modifying the input resistor ratio. The output impedance of the external sync signal source should be no greater than 4k ohms.

THE ICM7045A

The ICM7045A will count to a total of 2399999. The next count will show 0000000. On appliction of RESET the display will show 0 on the least significant digit; all other digits will be blanked. Leading zero suppression blanking is performed on pairs of digits. For example, 9 will show as 9, 10 will show as 010, 999 will show as 999, 1000 will show as 01000 and so forth.

The oscillator frequency alone determines whether the timer is to be used for second, minute or hour counting.

'SECONDS' TIMER Use a 1.31072MHz quartz crystal

DIGIT #	1	2	3	4	5	6	7
	100K Secs	10K Secs	1K Secs	100 Secs	10 Secs	Secs	Sec ÷ 10

'MINUTES' TIMER Use a 2.184533MHz quartz crystal

DIGIT #	1	2	3	4	5	6	7
	1K Mins	100 Mins	10 Mins	Mins	Min ÷ 10	Min ÷ 100	Min ÷ 1000

'HOURS' TIMER Use a 3.640889MHz quartz crystal

DIGIT #	1	2	3	4	5	6	7
	10 Hrs	Hrs	Hrs ÷ 10	Hrs ÷ 100	Hrs ÷ 1,000	Hrs ÷ 10,000	Hrs ÷ 100,000

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary MOS inverter with on-chip feedback resistors and an on-chip fixed input capacitor of 22pF. For the 6.5536 MHz crystal needed for normal timing, it is suggested that the nominal load capacitance be kept under 12pF to keep total loading on the oscillator to a reasonable level. The actual trimmer range and the nominal load capacitance needed will have to be determined from the total stray capacitance of the particular circuit (including ICM7045 with package, PC board, etc.) and the tuning tolerance of the chosen crystal.

The series resistance of the crystal should also be kept to a low value (typically less than 50 ohms) to achieve adequate low voltage operation.

Oscillator tune up can be most easily performed using a pull-up resistor of 10k ohms on the fractional seconds digit, using period average tune for 1.25ms (800Hz).

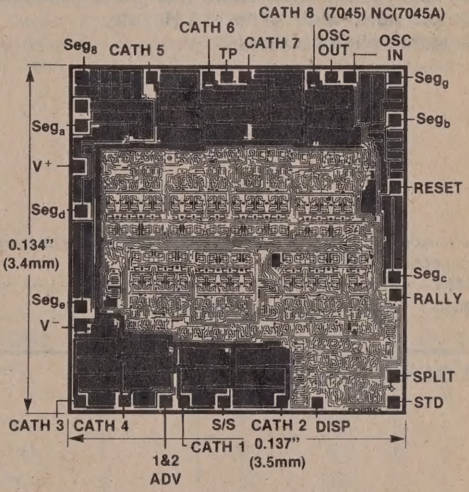
The oscillator of the ICM7045A is identical to that of the ICM7045, with the exception of the crystal frequency and load capacitance. Using similar value tuning capacitances with the lower frequency crystals (1.31077HHz, 2.184MHz 3.64089MHz) the stability of the oscillator is significantly degraded. It is therefore recommended that the tuning capacitances be increased to a nominal total of 40pF at both the oscillator input and output. Since there is an on chip input capacitance of 20-22pF the additional external input capacitance should be approximately 20pF.

The ICM7045A is guaranteed to operate over the supply voltage range of 2.5 to 4.5V using nominal input and output tuning capacitances of 40pF and with crystals having the following characteristics:

$f = 1.310772$MHz
2.184533MHz
3.64089MHz

$R_S \leq 100\Omega$ (150Ω for 1.310772MHz)
$C_M \rightarrow 10\text{-}20$mpF
$C_O \leq 6$pF
$C_L = 20$pF (parallel resonance mode)

CHIP TOPOGRAPHY



ICM7050
CMOS Quartz Clock Circuit
Bipolar Stepper Motor Applications

FEATURES

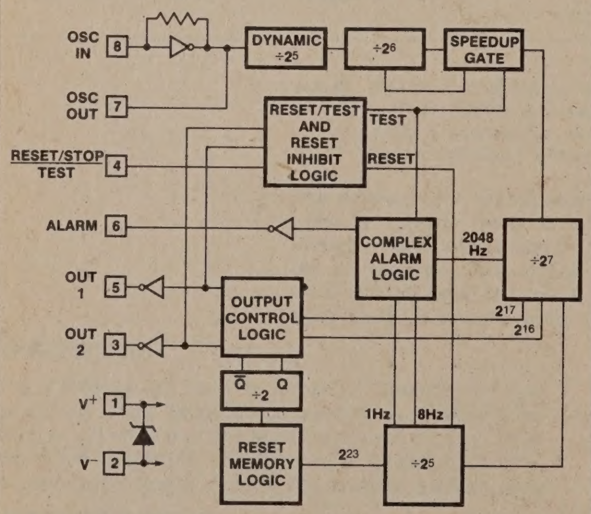
- **Single battery operation**
- **Very low current - typically 30μA at 4.19MHz**
- **Reset or stop function, inhibited during output**
- **Excellent drive with extremely low output saturation resistance: less than 100 ohms**
- **Complex direct drive alarm: 1Hz + 8Hz + 2048Hz**
- **Output pulse width 47ms at 1 Hz rate**
- **Custom options available***

*Two customized versions of the ICM7050 are available as standard factory options. They are:
ITS9063 — Output pulse width is 31 ms at 1Hz rate.
ITS9064-1 — Output pulse is a 1Hz square wave.

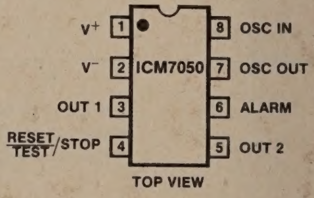
GENERAL DESCRIPTION

The ICM7050 is a single battery analog quartz clock circuit intended for use with bipolar stepper motors, and fabricated using Intersil's low voltage metal gate C-MOS process. The circuit consists of an oscillator, a divider chain, an output oneshot, and output buffers. The oscillator, when using the specified 4.19MHz crystal and capacitors, provides excellent stability. The high frequency portion of the divider chain consists of dynamic dividers, while the remainder are static. The dynamic dividers provide for low power consumption and low operating voltage, but limit low frequency operation. The 2^{23} divider chain is tapped at the 2^{11}, 2^{19}, and 2^{22} points to provide a complex alarm of 1Hz, 8Hz, and 2048Hz driving an output inverter. The oneshot generates the 46.875 millisecond pulse width and the large output inverters provide the low impedance necessary to drive the motor. A reset inhibit function is provided so that if the RESET occurs during an output pulse resetting will not take place until the pulse is completed. RESET may also be used as a stop for synchronization to a time signal or tester.

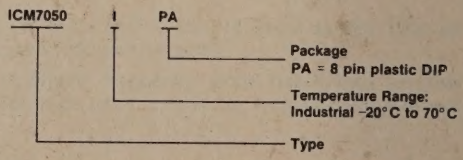
BLOCK DIAGRAM


OSC IN 8
OSC OUT 7
RESET/STOP TEST 4
ALARM 6
OUT 1 5
OUT 2 3
V+ 1
V− 2
DYNAMIC ÷2^5
÷2^6
SPEEDUP GATE
RESET/TEST AND RESET INHIBIT LOGIC
TEST
RESET
COMPLEX ALARM LOGIC
2048 Hz
÷2^7
2^17
2^16
OUTPUT CONTROL LOGIC
Q̄ Q ÷2
1Hz
8Hz
RESET MEMORY LOGIC
2^23
÷2^5

PIN CONFIGURATION (OUTLINE DRAWING PA)


V+ 1
V− 2
OUT 1 3
RESET/TEST/STOP 4
ICM7050
8 OSC IN
7 OSC OUT
6 ALARM
5 OUT 2
TOP VIEW

ORDERING INFORMATION


ICM7050
I
PA
Package
PA = 8 pin plastic DIP
Temperature Range:
Industrial −20°C to 70°C
Type

Order Devices by Following Part Number — ICM7050IPA
Order Dice by Following Part Number — ICM7050/D
Order Options by Following Part Numbers —
ICM7050 IPA/ITS 9063
ICM7050 IPA/ITS 9064-1

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit (Note 1) 300mW
Supply Voltage 3V
Output Voltage (Note 2) .... Equal to but never
Input Voltage (Note 2) .... exceeding the supply voltage
Storage Temperature .... −30°C to +125°C
Operating Temperature .... −20°C to +70°C
Lead Temperature (soldering, 10s) .... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This value of power dissipation refers to thet of the package and will not normally be obtained under normal operating conditions.

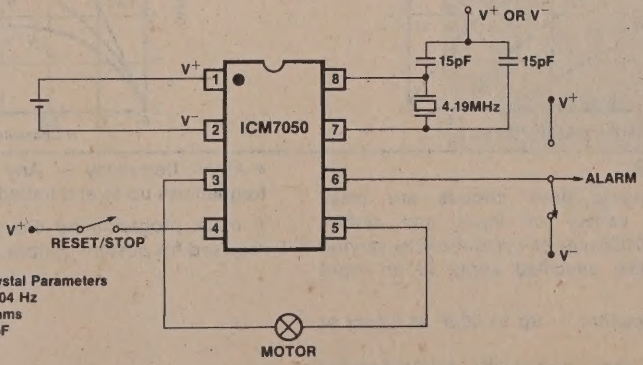
NOTE 2: Due to the inherent SCR structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

ELECTRICAL CHARACTERISTICS

(V+ = 1.5V, f_{osc} = 4,194,304Hz test circuit, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I^+	No Load		30	60	μA
Operating Voltage	V^+	$-20°C < T_A < 70°C$	1.2		1.8	V
Total Output Saturation Resistance	R_{OUT}	$I_L = 3mA$		70	100	Ω
Alarm Saturation Resistance	$R_{AL(on)}$	P, $I_L = 1mA$		400	700	Ω
		N, $I_L = 2mA$		100	400	Ω
Oscillator Stability	f_{stab}	$1.2 \le V^+ \le 1.6$		1		ppm
Oscillator Start-up Time	t_{start}	$V^+ = 1.2V$			1.0	sec

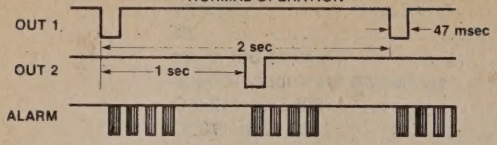
CLOCK CIRCUIT



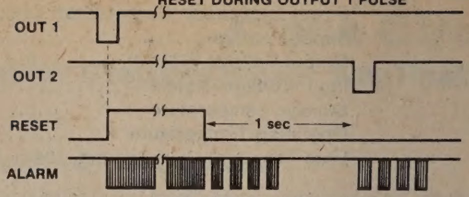
Quartz Crystal Parameters
f = 4,194,304 Hz
R_S = 45 ohms
C_1 = 10mpF
C_0 = 4pF

OUTPUT WAVEFORMS

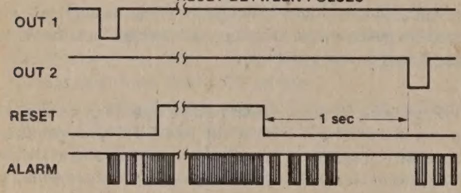
NORMAL OPERATION


OUT 1
47 msec
2 sec
OUT 2
1 sec
ALARM

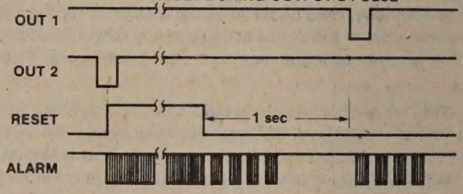
RESET DURING OUTPUT 1 PULSE


OUT 1
OUT 2
RESET
1 sec
ALARM

RESET BETWEEN PULSES

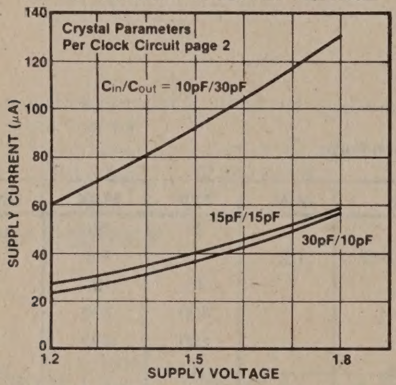

OUT 1
OUT 2
RESET
1 sec
ALARM

RESET DURING OUTPUT 2 PULSE

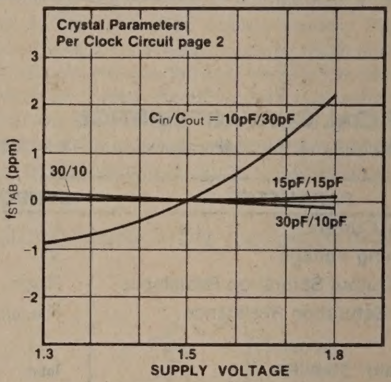

OUT 1
OUT 2
RESET
1 sec
ALARM

TYPICAL OPERATION CHARACTERISTICS

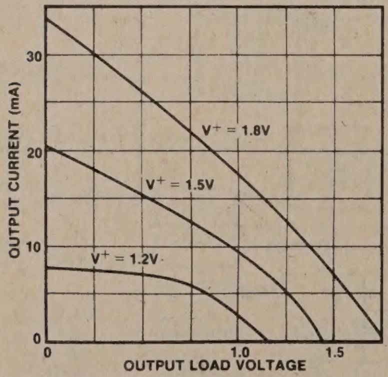
SUPPLY CURRENT vs SUPPLY VOLTAGE



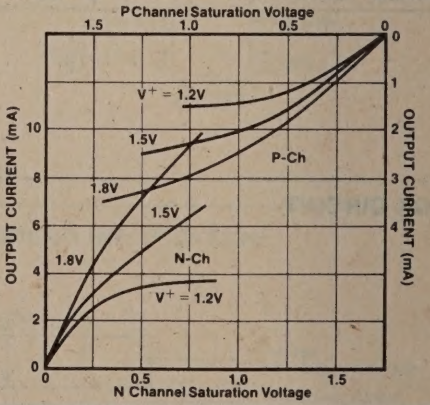
OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



OUTPUT CURRENT vs OUTPUT LOAD VOLTAGE



ALARM OUTPUT CURRENT vs SATURATION VOLTAGE



CUSTOM OPTIONS

All Intersil analog quartz clock circuits are mask programmable for a variety of input and output configurations. The ICM7050 may be customized by varying the following. Parameters specified apply to an input frequency of 32kHz.

- On chip oscillator capacitor — up to 50pF at C_{OSCI} or C_{OSCO}
- Output pulse width — from 7.8ms to 50% of output period
- Output pulse frequency — from 0.5Hz to 64Hz
- Alarm frequency — Any combination of three binary frequencies up to and including 2048Hz.

A mask programming charge and a minimum order are required for custom options. Consult factory for details.

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7050 has been designed to operate with crystals having a load capacitance of 10 to 12pF. This allows nominal capacitor values of 15/15pF or 20/20pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor having a maximum value at start up is provided on chip. Oscillator tuning should be done at the oscillator output.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_o + C_L)} \qquad C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}}$$

g_m required for startup

$$g_m = \omega^2 C_{in}C_{out}R_S \left(1 + \frac{C_o}{C_L}\right)^2$$

R_S = series resistance of the crystal
f = frequency of the crystal
Δf = frequency shift from series resonance frequency
C_o = static capacitance of the crystal
C_{in} = input capacitance.
C_{out} = output capacitance
C_L = motional capacitance
$\omega = 2\pi f$

The resulting g_m should not exceed 50μmhos.

OSCILLATOR TUNING METHODS

When tuning the oscillator two methods can be used. The first method would be to monitor the output pulse at either OUT 1 or OUT 2 with a counter set to measure the period. The oscillator trimmer would then be adjusted for a reading of 2.000000 secs. A second method would be to put the device in the reset mode by pulling the reset pin to V^+ and then monitor the ALARM output with a counter set to measure average period. The ALARM output is a continuous 2048Hz when in the reset mode, which gives a period of 488.2815μs.

The trimmer capacitor used for tuning should be connected to the oscillator output. Otherwise, if tuned at the input, the stability will vary with tuning, and the current drain may become excessive when the input capacitance is much less than the output capacitance. Refer to the I^+ vs V^+ and OSCILLATOR STABILITY vs V^+ characteristic curves on the preceding page.

TEST MODE OPERATION

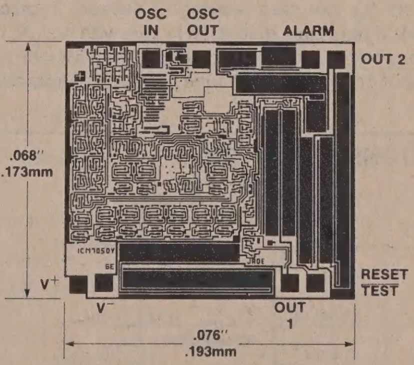
Pulling the RESET/TEST input to −7V switches the device into the test mode to speedup automatic testing. When in the test mode the output rate is increased 16 times, from 1Hz to 16Hz, with a corresponding reduction in pulse width. The ALARM output changes to a composite waveform of 16Hz and 128Hz. The circuit can be reset while in the test mode by shorting the ALARM output to V^-.

ALARM CONSIDERATIONS

The ALARM output inverter is large enough to directly drive transducers requiring up to 2mA of current. If more current is needed than a buffer should be used*. A slight fluctuation in the supply current of 0.5μA to 1.0μA will be seen; this is a result of 2048Hz driving the relatively large gate capacitance of the alarm output transistors.

*See Intersil Application Bulletin A031 for details.

CHIP TOPOGRAPHY



INTERSIL

ICM7206 CMOS Touch Tone™ Encoder

FEATURES

- **Low cost system with minimum component count**
- **Fully integrated oscillator uses 3.58 MHz color TV crystal**
- **High current bipolar output driver**
- **Low output harmonic distortion**
- **Wide operating supply voltage range: 3 to 6 volts**
- **Uses inexpensive single contact per key calculator type keyboard (ICM7206/C/D)**
- **Extremely low power ≤ 5.5mW with a 5.5V supply**
- **Single and dual tone capabilities**
- **Multiple key lockout**
- **Disable output: provides output switch function whenever a key is pressed**
- **Custom options available**

GENERAL DESCRIPTION

The Intersil ICM7206/A/B/C/D are 2-of-8 sine wave tone encoders for use in telephone dialing systems. Each circuit contains a high frequency oscillator, two separate programmable dividers, a D/A converter, and a high level output driver.

The reference frequency is generated from a fully integrated oscillator requiring only a 3.58 MHz color TV crystal. This frequency is divided by 8 and is then gated into two divide by N counters (possible division ratios 1 through 128) which provide the correct division ratios for the upper and lower band of frequencies. The outputs from these two divide by N counters are further divided by 3 to provide the time sequencing for a 4 voltage level synthesis of each sinewave. Both sinewaves are added and buffered to a high current output driver, with provisions made for up to two external capacitors for low pass filtering, if desired. Typically, the total output harmonic distortion is 20% with no L.P. filtering and it may be reduced to typically less than 5% with filtering. The output drive level of the tone pairs will be approximately −3dBV into a 900 ohm termination. The skew between the high and low groups is typically 2.5 dB without low pass filtering.

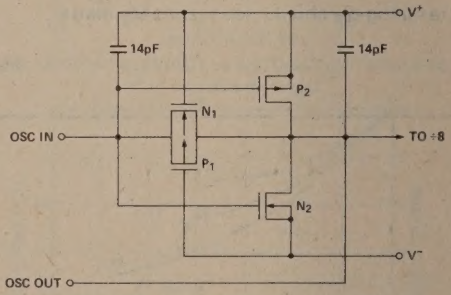
The 7206 uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will run whenever the power is applied, and the DISABLE output consists of a p-channel open drain FET whose source is connected to V^+.

The 7206A can also use a 3 x 4 or 4 x 4 keyboard, but requires a double contact type with the common line tied to V^+. The oscillator will be on whenever power is applied; the DISABLE output consists of a p-channel open drain FET; its' source is connected to V^+.

The 7206B requires a 4 x 4 double contact keyboard with the common line tied to V^-. The oscillator will be on only during the time that a ROW is enabled, and the DISABLE output consists of an n-channel open drain FET with its' source tied to V^-.

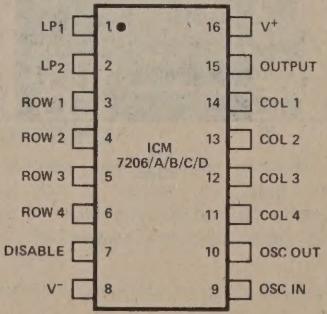
The 7206C uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will be on only during the time that a key is depressed. The DISABLE output consists of an n-channel open drain FET with its source tied to V^-.

The 7206D uses a single contact 3 x 4 or 4 x 4 keyboard. The oscillator will be on only during the time that a key is depressed. DISABLE output consists of a p-channel open drain FET with its source tied to V^+.



ICM7206 Oscillator

PIN CONFIGURATION (OUTLINE DRAWING PE)



Pin 1 is designated either by a dot or a notch.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7206 JPE	-40° C to +85° C	Plastic
ICM7206A JPE	-40° C to +85° C	Plastic
ICM7206B JPE	-40° C to +85° C	Plastic
ICM7206C JPE	-40° C to +85° C	Plastic
ICM7206D JPE	-40° C to +85° C	Plastic
ICM7206/D	-40° C to +85° C	DICE
ICM7206A/D	-40° C to +85° C	DICE
ICM7206B/D	-40° C to +85° C	DICE
ICM7206C/D	-40° C to +85° C	DICE
ICM7206D/D	-40° C to +85° C	DICE

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2)	6.0V
Supply Current V^- (terminal 8)	25mA
Supply Current V^+ (terminal 16)	40mA
Disable Output Volt. (term. 7)	Not more pos. than V^+ nor more neg. than −6V with respect to V^+
Output Volt. (term. 15)	Not more pos. than +5V with respect to V^+, nor more neg. than −1.0 with respect to V^-
Output Current (terminal 15)	25mA
Power Dissipation	300mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C

NOTE 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 2. The ICM7206 family has a zener diode connected between V^+ and V^- having a breakdown voltage between 6.2 and 7.0 volts. If the currents into terminals 8 and 16 are limited to 25 and 40mA maximum respectively, the supply voltage may be increased above 6 volts to zener voltage. With no such current limiting, the supply voltage must not exceed 6 volts.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.5V$, Test Circuit, $T_A = 25°C$ unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Current	I^+	R_L disconnected			450	1000	µA
Guaranteed Operating Supply Voltage Range (Note 3)	V_{OP}	$-40°C \leq T_A \leq +85°C$		3.0		6.0	V
Peak to Peak Output Voltage	V_{OUT}	C_1, C_2 disconnected — Low Band		0.90	1.15	1.45	
		$R_L = 1k\Omega$, no filtering — High Band		1.10	1.40	1.70	
RMS Output Voltage		$R_L = 1k\Omega$, $f_{OUT} = 697Hz$	C_2 Only		480		mV
			C_1 to C_2		480		
			No filtering		490		
		$R_L = 1k\Omega$, $f_{OUT} = 1633Hz$	C_1		490		
			C_1 to C_2		580		
			No filtering		655		
Skew Between High and Low Band Output Voltages		$R_L = 1k\Omega$, C_1, C_2 disconnected			2.5	3.0	dB
Output Impedance	Z_O	$R_L = 1k\Omega$	Operating		90	200	Ω
			Quiescent		25		KΩ
Total Output Harmonic Distortion	THD1	Either Hi or Low Bands No Low Pass Filtering			20	25	%
Total Output Harmonic Distortion	THD2	$R_L = 1k\Omega$, $C_1 = .002\mu F$	$f_{OUT} = 697Hz$		2.3	10	
		$C_2 = 0.02\mu F$	$f_{OUT} = 1633Hz$		1.0	10	
Maximum Output Voltage Level	V_{OH}	$R_L = 1k\Omega$				4.6	V
Minimum Output Voltage Level	V_{OL}	$R_L = 1k\Omega$		0.5			
Keyboard Input Pullup Resistors	R_{IN}	Terminals 3,4,5,6,11,12,13,14		35	100	150	KΩ
Keyboard Input Capacitance	C_{IN}	Terminals 3,4,5,6,11,12,13,14				5	pF
Guaranteed Oscillator Frequency Range (Note 4)	f_{OSC}	$3 \leq (V^+ - V^-) \leq 6V$		2.0		4.5	MHz
Guaranteed Oscillator Frequency Range		$4V \leq (V^+ - V^-) \leq 6V$		2.0		7	
System Startup Time on Application of Power	t_{on}	ICM7206, ICM7206A			10		ms
System Startup Time on Application of Power and Key Depressed Simultaneously		ICM7206B, ICM7206C, ICM7206D				7	
DISABLE Output Saturation Resistance (ON STATE)	R_D	See Logic Table for Input Conditions Current = 4mA			330	700	Ω
DISABLE Output Leakage (OFF STATE)	I_{OLK}	See Logic Table for Input Conditions				10	µA
Oscillator Load Capacitance	C_{OSC}	Measured between terminals 9 & 10, no supply voltage applied to circuit $-40°C \leq T_A \leq 85°C$			7		pF
Guaranteed Output Frequency Tolerance	f_O	Any output frequency Crystal tolerance ±60ppm Crystal load capacitance CL = 30pF				±0.75	%
Oscillator Startup Time ICM7206B, C, D	t_{start}	$V^+ = 3V$ (Note 5)				7	ms

NOTE 3: Operation above 6 volts must employ supply current limiting. Refer to 'ABSOLUTE MAXIMUM RATINGS' and the Application Notes for further information.

NOTE 4: The ICM7206 family uses dynamic high frequency circuitry in the initial 2^3 divider resulting in low power dissipation and excellent performance over a restricted frequency range. Thus, for reliable operation with a 6 volt supply an oscillator frequency of not less than 2MHz must be used.

NOTE 5: After row input is enabled.

TRUTH TABLE

LINE	ROWS (1) ACTIVATED	COLS (2) ACTIVATED	OUTPUT (TERMINAL #15)	DISABLE (TERMINAL #7)	COMMENTS
1	0	0	Off	Off	Quiescent State
2	1	1	$f_{row} + f_{col}$	On	Dual Tone
3	1	2 or 3 (incl. col #4)	f_{row}	On	Single Tone
4	2 or 3	1	f_{col}	On	Single Tone
5	2 or 3	2 or 3 (excl. col #3)	D.C. Level	On	No Tone
6	1	4 or 3 (must excl. col #4)	f_{row}, 50% Duty Cycle	f_{row}, 50% Duty Cycle	f_{row} Test
7	4	1	f_{col}, 50% Duty Cycle	f_{col}, 50% Duty Cycle	f_{col} Test
8	0	1 or 2 or 3 or 4	Off	Off	n/a*
9	1	0	902Hz + f_{row}	On	n/a*
10	2 or 3	0	902Hz	On	n/a*
11	4	0	902Hz, 50% Duty Cycle	902Hz, 50% Duty Cycle	n/a*
12	2 or 3 or 4	4	D.C. Level	Indeterminate	Multiple Key Lockout
13	4	2 or 3 or 4	D.C. Level	Indeterminate	Multiple Key Lockout

*n/a — not applicable to telephone calling.

Note 1: Rows are activated for the ICM7206/C by connecting to a negative supply voltage with respect to V^+ (terminal 16) at least 33% of the value of the supply voltage (V^+–V^-). For the ICM7206A rows (and columns) are activated by connecting to a positive supply voltage with respect to V^- (terminal 8) at least 33% of the value of the supply voltage (V^+–V^-). The rows and columns of the ICM7206B are activated by connecting to a negative supply voltage.

Note 2: Columns (ICM7206) are activated by being connected to a positive supply voltage with respect to V^- (terminal 8) at least 33% of the value of the supply voltage (V^+–V^-).

COMMENTS

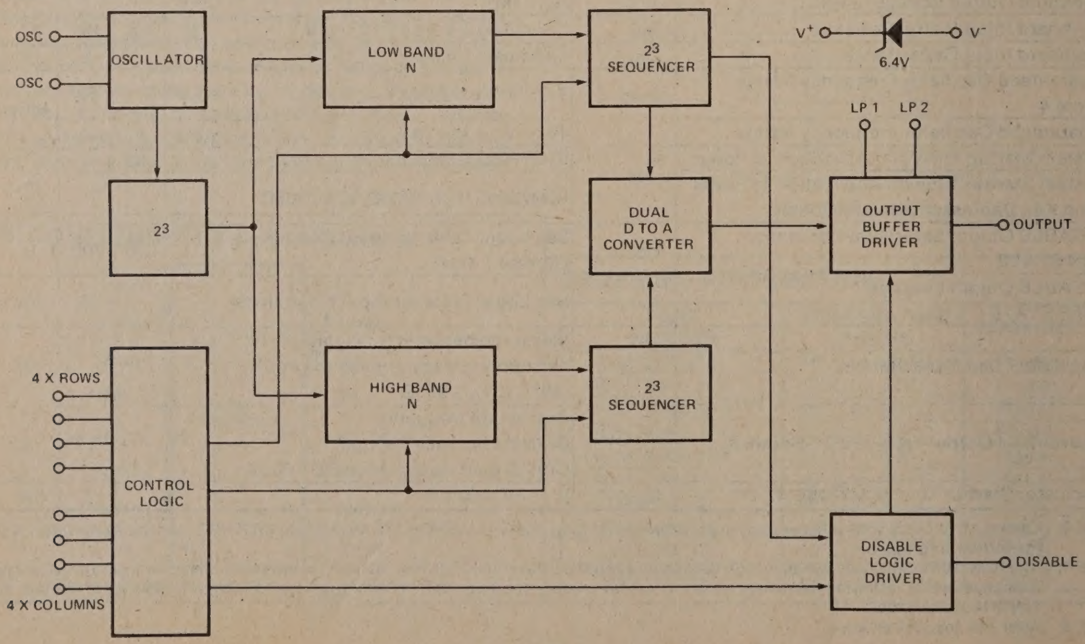
All combinations of row and column activations are given in the truth table. Lines 1 thru 7 and 12, 13 represent conditions obtainable with a matrix keyboard. Lines 8 thru 11 are given only for completeness and are not pertinent to telephone dialing.

Lines 6 and 7 show conditions for generating 50% duty cycle full amplitude signals useful for rapid testing of the row and column frequencies on automatic test equipment. In all other cases, output frequencies on terminal 15 are single or dual 4 level synthesized sine waves.

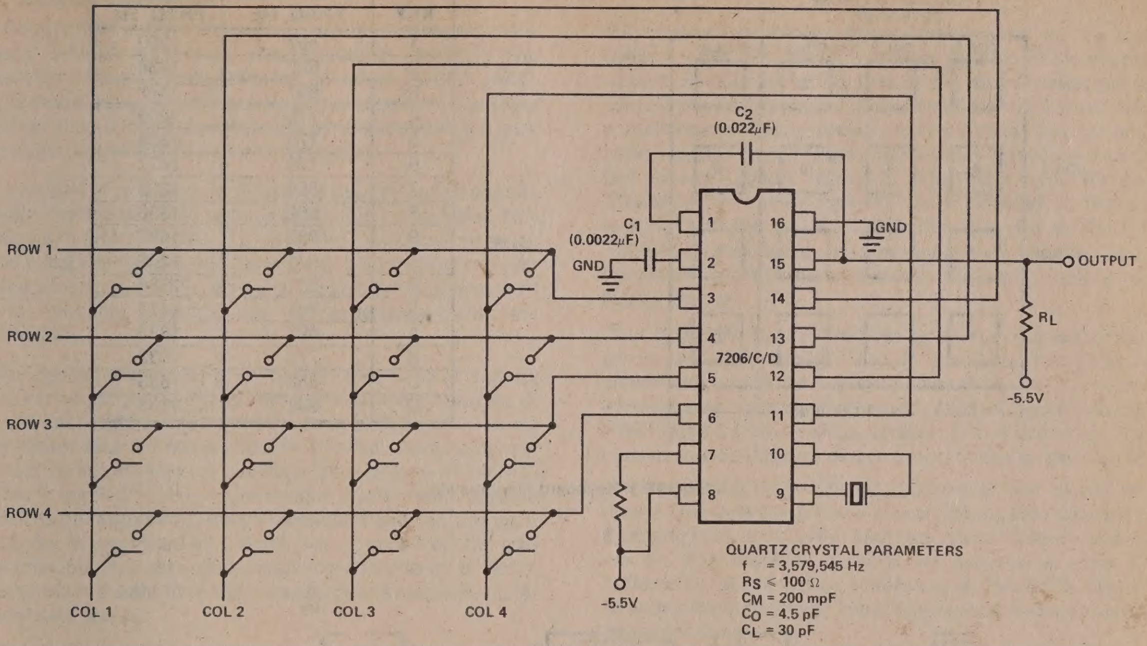
A 'DC LEVEL' on terminal 15 may be any voltage level between approximately 1.2 and 4.3 volts with respect to V^- (terminal 8) for a 5.5 volt supply voltage.

The impedance of the OUTPUT (terminal 15) is approximately 20K ohms in the OFF state. The 'DISABLE OUT-OUT' ON and OFF conditions are defined in the TYPICAL OPERATING CHARACTERISTICS.

SCHEMATIC DIAGRAM



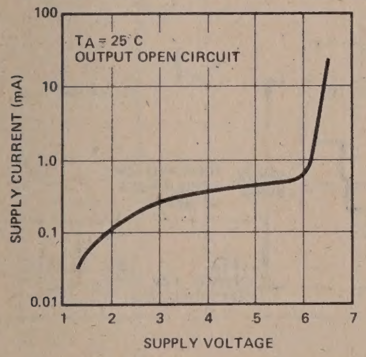
TEST CIRCUIT (single contact keyboard devices shown)


C2
(0.022μF)
C1
(0.0022μF)
GND
GND
ROW 1
ROW 2
ROW 3
ROW 4
COL 1
COL 2
COL 3
COL 4
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
7206/C/D
OUTPUT
RL
-5.5V
-5.5V

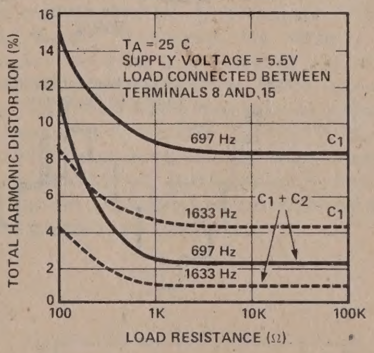
QUARTZ CRYSTAL PARAMETERS
f = 3,579,545 Hz
$R_S \leq 100\ \Omega$
C_M = 200 mpF
C_O = 4.5 pF
C_L = 30 pF

TYPICAL OPERATING CHARACTERISTICS

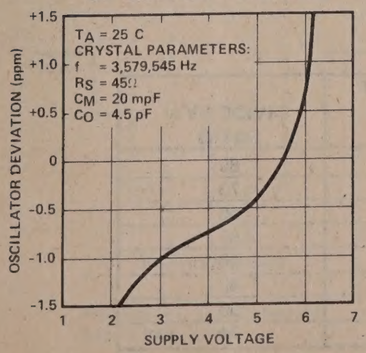
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



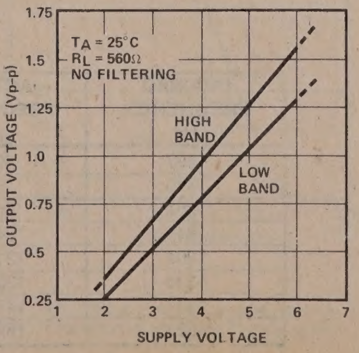
TOTAL HARMONIC DISTORTION AS A FUNCTION OF LOAD RESISTANCE

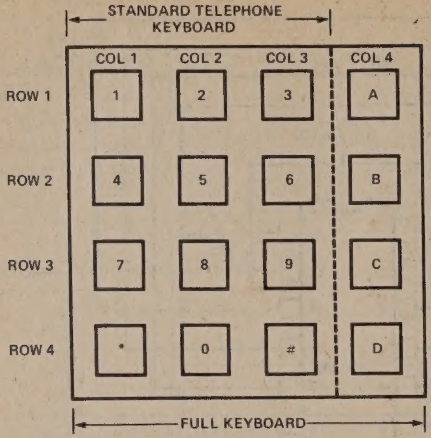


OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF SUPPLY VOLTAGE



PEAK TO PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE




STANDARD TELEPHONE KEYBOARD
COL 1
COL 2
COL 3
COL 4
ROW 1
ROW 2
ROW 3
ROW 4
1
2
3
A
4
5
6
B
7
8
9
C
*
0
#
D
FULL KEYBOARD

KEY	LOW BAND FREQ. Hz	HI BAND FREQ. Hz
1	697	1209
2	697	1336
3	697	1477
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
*	941	1209
0	941	1336
#	941	1477
A	697	1633
B	770	1633
C	852	1633
D	941	1633

FIGURE 1: Keyboard Frequencies

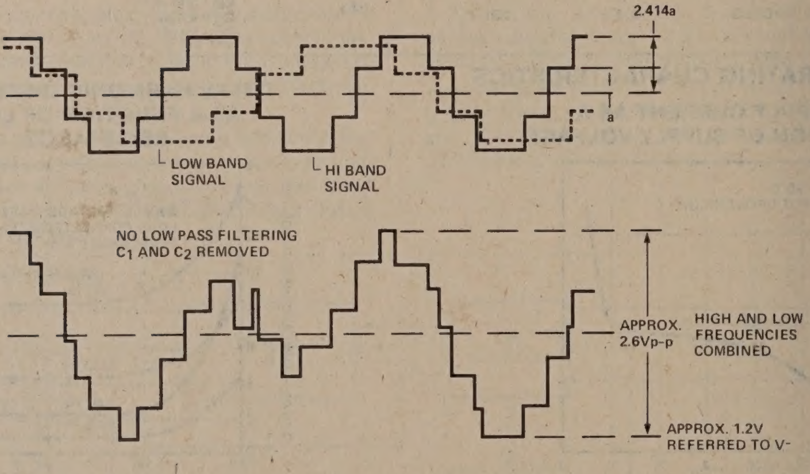

2.414a
a
LOW BAND SIGNAL
HI BAND SIGNAL
NO LOW PASS FILTERING
C1 AND C2 REMOVED
APPROX. 2.6Vp-p
HIGH AND LOW FREQUENCIES COMBINED
APPROX. 1.2V REFERRED TO V-

FIGURE 2

Figure 2 shows individual currents of a low band and high band frequency pair into the summing node A (see Figure 3) and the resultant voltage waveform.

DESIRED FREQUENCY Hz	ACTUAL FREQUENCY Hz	FREQUENCY DEVIATION %	DIVIDE BY N RATIO
697	699.13	+0.30	80
770	766.17	−0.50	73
852	847.43	−0.54	66
941	947.97	+0.74	59
1209	1215.88	+0.57	46
1336	1331.68	−0.32	42
1477	1471.85	−0.35	38
1633	1645.01	+0.74	34

APPLICATION NOTES

1. Device Description

The ICM7206 family is manufactured with a standard metal gate C-MOS technology having proven reliability and excellent reproducability resulting in extremely high yields. The techniques used in the design have been developed over many years and are characterized by wide operating supply voltage ranges and low power dissipation.

To minimize chip size, all diffusions used to define source-drain regions and field regions are butted up together. This results in approximately 6.3 volt zener breakdown between the supply terminals, and between all components on chip. As a consequence, the usual C-MOS static charge problems and handling problems are not experienced with the ICM7206.

The oscillator consists of a medium size C-MOS inverter having on chip a feedback resistor and two capacitors of 14pF each, one at the oscillator input and the other at the oscillator output. The oscillator is followed by a dynamic ÷23 circuit which divides the oscillator frequency to 447,443Hz. This is applied to two programmable dividers each capable of division ratios of any integer between 1 and 128, and each counter is controlled by a ROM. The outputs from the programmable counters drive sequencers (divide by 8) which generate the eight time slots necessary to synthesize the 4-level sine waves.

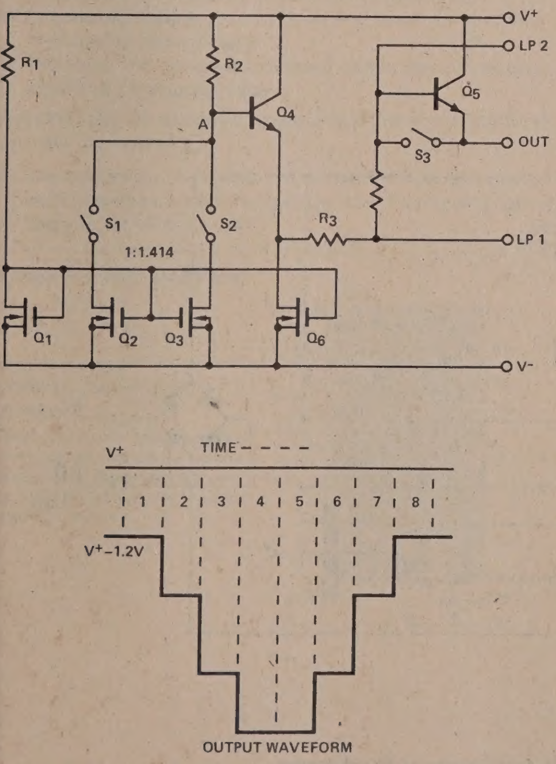


FIGURE 3: D to A Converter and Output Buffer

The control logic block recognizes signals on the row and column inputs that are only a small fraction of the supply voltage, thereby permitting the use of a simple matrix single contact per key keyboard, rather than the more usual two contacts per key type having a common line. The row and column pullup resistors are equal in value and connected to the opposite supply terminals (ICM7206/C only; for the ICM7206A all pullup resistors are connected to the V^- terminal and for the ICM7206B they are tied to the V^+. Therefore, connecting a row input to a column input generates a voltage on those inputs which is one half of the supply voltage.

The ICM7206 family employs a unique but extremely simple digital to analog (D to A) converter. This D to A converter produces a 4 level synthesized sine wave having an intrinsic total harmonic distortion level of approximately 20%. Figure 3 shows a single channel D to A converter. The current sources Q_2 and Q_3 are proportioned in the ratio of 1:1.414. During time slots 1 and 8 both S_1 and S_2 are off, during time slots 2 and 7 only S_1 is on, during time slots 3 and 6 only S_2 is on, and during time slots 4 and 5 both S_1 and S_2 are on. The resultant currents are summed at node A, buffered by Q_4 and further buffered by R_3, R_4 and Q_5. Switch S_3 allows the output to go into a high impedance mode under quiescent conditions.

Node A is the common summing point for both the high and low band frequencies although this is not shown in Figure 3.

The synthesized sine wave has negligible even harmonic distortion and very low values of third and fifth harmonic distortion thereby minimizing the filtering problems necessary to reduce the total harmonic distortion to well below the 10% level required for touch tone telephone encoding. Figure 4 shows the low pass filter characteristic of the output buffer for $C_1 = 0.0022\mu F$ and $C_2 = 0.022\mu F$. A small peak of 0.4dB occurs at 1100Hz with sharp attention (12dB per octave) above 2500Hz. This type of active filter produces a sharper and more desirable knee characteristic than would two simple cascaded RC networks.

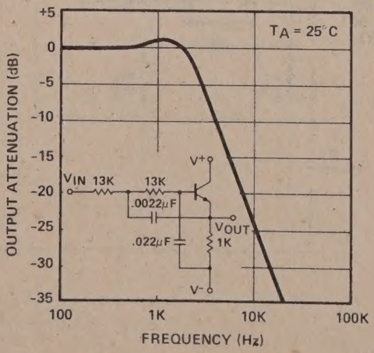


FIGURE 4: Frequency Attentuation Characteristics of the Output Buffer

2. Latchup Considerations

Most junction isolated C-MOS integrated circuits, especially those of moderate or high complexity, exhibit latchup phenomena whereby they can be triggered into an uncontrollable low impedance mode between the supply terminals. This can be due to gross forward biasing of inputs or outputs (with respect to the supply terminals), high voltage supply transients, or more rarely by exceptional fast rate of rise of supply voltages.

The ICM7206 family is no exception, and precautions must be taken to limit the supply current to those values shown in the ABSOLUTE MAXIMUM RATINGS. For an example, do not use a 6 volt very low impedance supply source in an **electrically extremely noisy** environment unless a 500 ohm current limiting resistor is included in series with the V^- terminal. For normal telephone encoding applications no problems are envisioned, even with low impedance transients of 100 volts or more, if circuitry similar to that shown in the next section is used.

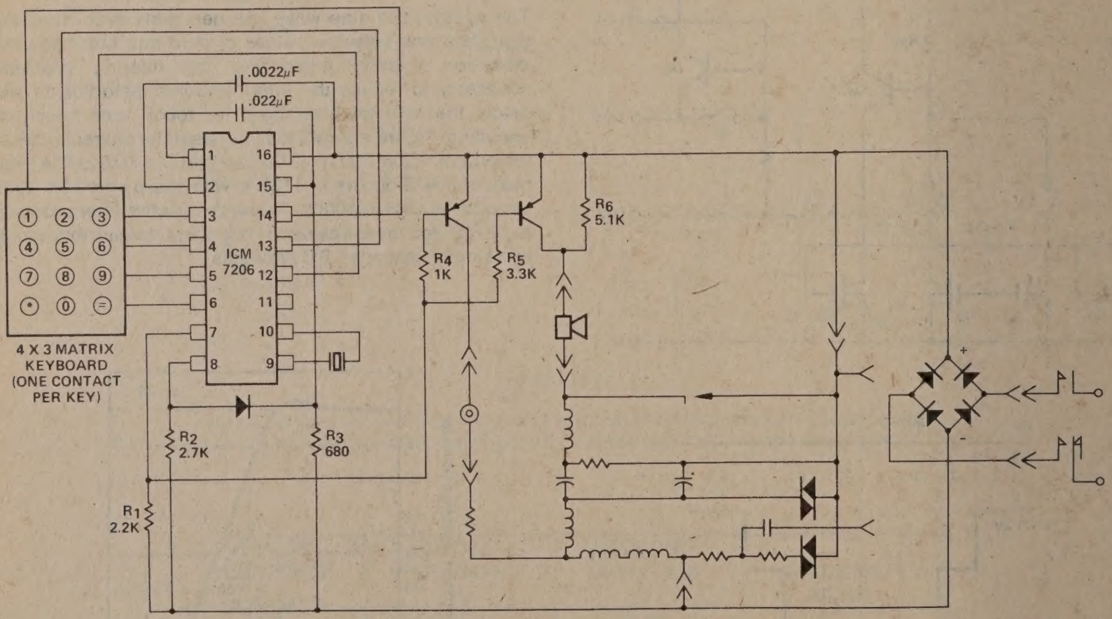
3. Typical Application (Telephone Handset)

A typical encoder for telephone handsets is shown in Figure 5. This encoder uses a single contact per key keyboard and provides all other switching functions electronically. The diode connected between terminals 8 and 15 prevents the output going more than 1 volt negative with respect to the negative supply V^- and the circuit operates over the supply voltage range from 3.5 volts to 15 volts on the device side of the bridge rectifier. Transients as high as 100 volts will not cause system failure, although the encoder will not operate correctly under these conditions. Correct operation will resume immediately after the transient is removed.

The output voltage of the synthesized sine wave is almost directly proportional to the supply voltage (V^+–V^-) and will increase with increase of supply voltage until zener breakdown occurs (approximately 6.3 volts between terminals 8 and 16) after which the output voltage remains constant.

4. Portable Tone Generator

The ICM7206A/B require a two contact key keyboard with the common line connected to the positive supply (neg for ICM7206B) (terminal 16). A simple diode matrix may be used with this keyboard to provide power to the system whenever a key is depressed, thus negating the need for an on/off switch. In Figure 6 the tone generator is shown using a 9 volt battery. However, if instead, a 6 volt battery is used, the diode D_4 is not required. It is recommended that a 470 ohm resistor still be included in series with a negative (positive) supply to prevent accidental triggering of latchup.



NOTE: If dual contact keyboard is used, common should be left floating.

FIGURE 5: Telephone Handset Touch Tone Encoder

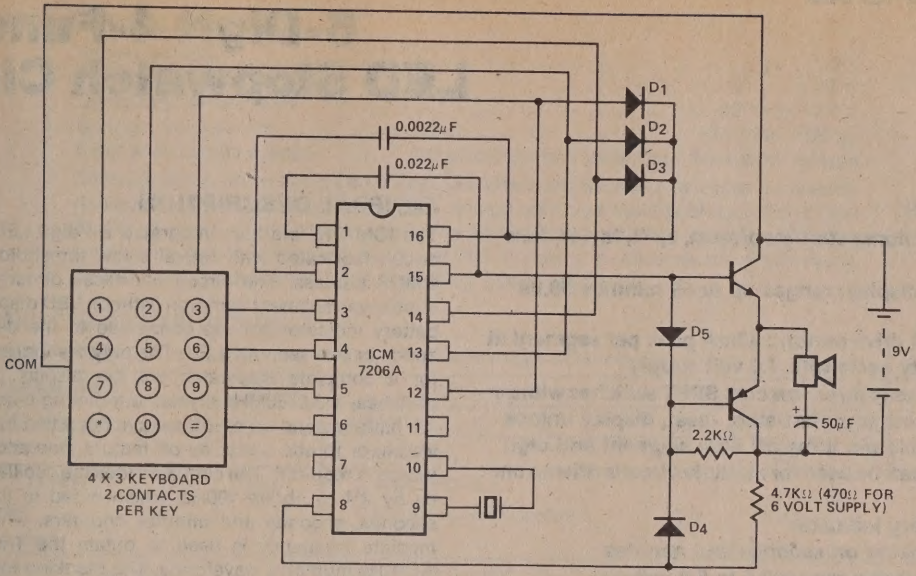

D1
D2
D3
0.0022μF
0.022μF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
ICM
7206A
1
2
3
4
5
6
7
8
9
*
0
=
COM
4 X 3 KEYBOARD
2 CONTACTS
PER KEY
D5
9V
50μF
2.2KΩ
4.7KΩ (470Ω FOR
6 VOLT SUPPLY)
D4

FIGURE 6: Portable Tone Generator

OPTIONS

(For additional information consult the factory)

a) Selecting the least expensive and most reliable keyboard

b) Selecting the lowest cost and most available quartz crystal

c) Minimizing the number of external components

d) Minimizing supply current drain and maximizing operating supply voltage range

e) Providing the smallest and least expensive circuit possible in a 16 lead package

Options can be achieved using metal mask additions to provide the following.

1) The sequence or position of either the row or column terminals can be interchanged i.e., row 1 terminal 3 could become terminal 11, etc.

2) Any frequency oscillator from approximately 0.5MHz to 7MHz can be chosen. Note that the accuracy of the output frequencies will depend on the exact oscillator frequency. For instance, a 1 MHz crystal could be used with worst case output frequency error of 0.8%. Or, if high accuracy is required, ±0.25%, oscillator frequencies of 5,117,376Hz or 2,558,688Hz could be selected. ROM's are used to program the dividers.

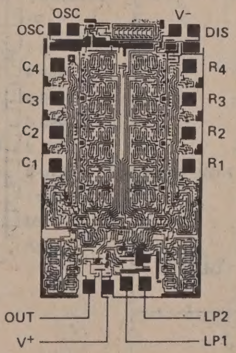
3) The 'DISABLE' output may be changed to an inverter or an uncommitted drain n-channel transistor.

4) The oscillator may be disabled until a key is depressed.

CHIP TOPOGRAPHY

Chip Dimensions
0.060" (1.524mm) x0.101"
(2.565mm)

Chip may be die attached using conventional eutectic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.


OSC
V-
OSC
DIS
C4
R4
C3
R3
C2
R2
C1
R1
OUT
LP2
V+
LP1

ICM7215
6-Digit 4-Function LED Stopwatch Circuit

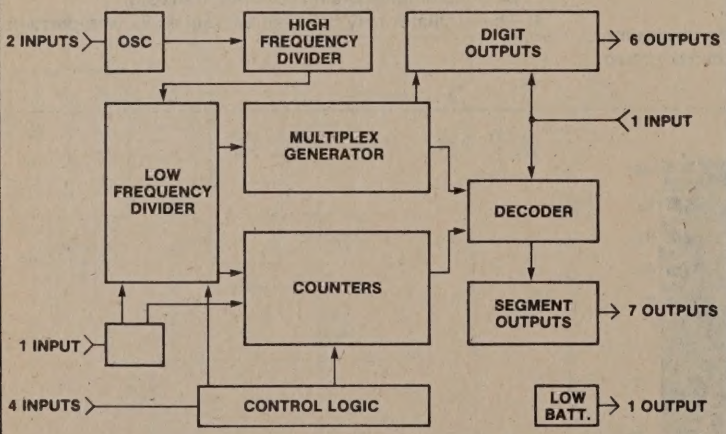
FEATURES

- **Four functions: start/stop/reset, split, taylor, time out**
- **Six digit display: ranges up to 59 minutes 59.99 seconds**
- **High LED drive current: 13mA peak per segment at 16.7% duty cycle with 4.0 volt supply**
- **Requires only three low cost SPST switches without loss of accuracy: start/stop, reset, display unlock**
- **Chip enable pin turns off both segment and digit outputs; can be used for multiple circuits driving one display**
- **Low battery indicator**
- **Digit blanking on seconds and minutes**
- **Wide operating range: 2.0 to 5.0 volts**
- **1KHz multiplex rate prevents flickering display**
- **Can be used easily in four different single function stopwatches or two two-function stopwatches: start/stop/reset with time-out, split with taylor. The component count for a three- or four-function stopwatch will be slightly greater.**
- **Retrofit to ICM7205 for split and/or taylor applications**

GENERAL DESCRIPTION

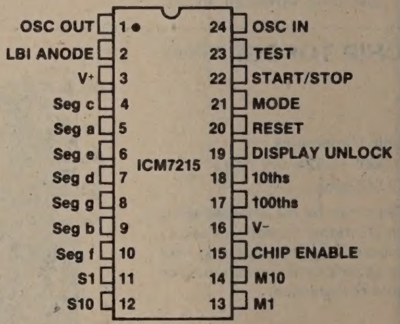
The ICM7215 is a fully integrated six digit LED stopwatch circuit fabricated with Intersil's low threshold metal gate CMOS process. The circuit interfaces directly with a six digit/seven segment common cathode LED display. The low battery indicator can be connected to the decimal point anode or to a separate LED. The only components required for a complete stopwatch are the display, three SPST switches, a 3.2768MHz crystal, a trimming capacitor, three AA batteries and an on-off switch. For a two function stopwatch, or to add a display off feature, one additional slide switch is required. The circuit divides the oscillator frequency by 2^{15} to obtain 100Hz, which is fed to the fractional seconds, seconds and minutes counters, while an intermediate frequency is used to obtain the 1/6 duty cycle 1.07KHz multiplex waveforms. The blanking logic provides leading zero blanking for seconds and minutes independently of the clock. The ICM7215 is packaged in a 24-lead plastic DIP.

BLOCK DIAGRAM


2 INPUTS
OSC
HIGH FREQUENCY DIVIDER
DIGIT OUTPUTS
6 OUTPUTS
1 INPUT
LOW FREQUENCY DIVIDER
MULTIPLEX GENERATOR
DECODER
COUNTERS
SEGMENT OUTPUTS
7 OUTPUTS
1 INPUT
4 INPUTS
CONTROL LOGIC
LOW BATT.
1 OUTPUT

PIN CONFIGURATION

(OUTLINE DRAWING PG)


OSC OUT 1
LBI ANODE 2
V+ 3
Seg c 4
Seg a 5
Seg e 6
Seg d 7
Seg g 8
Seg b 9
Seg f 10
S1 11
S10 12
ICM7215
24 OSC IN
23 TEST
22 START/STOP
21 MODE
20 RESET
19 DISPLAY UNLOCK
18 10ths
17 100ths
16 V-
15 CHIP ENABLE
14 M10
13 M1

ORDERING INFORMATION

Order devices by following part number ICM7215 I PG
Order dice by following part number ICM7215/D

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... 5.5 V
Power Dissipation (Note 1) .... 0.75 W
Operating Temperature .... −20°C to +70°C
Storage Temperature .... −55°C to +125°C
Input and Output Voltage .... equal to but never exceeding the supply voltage

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

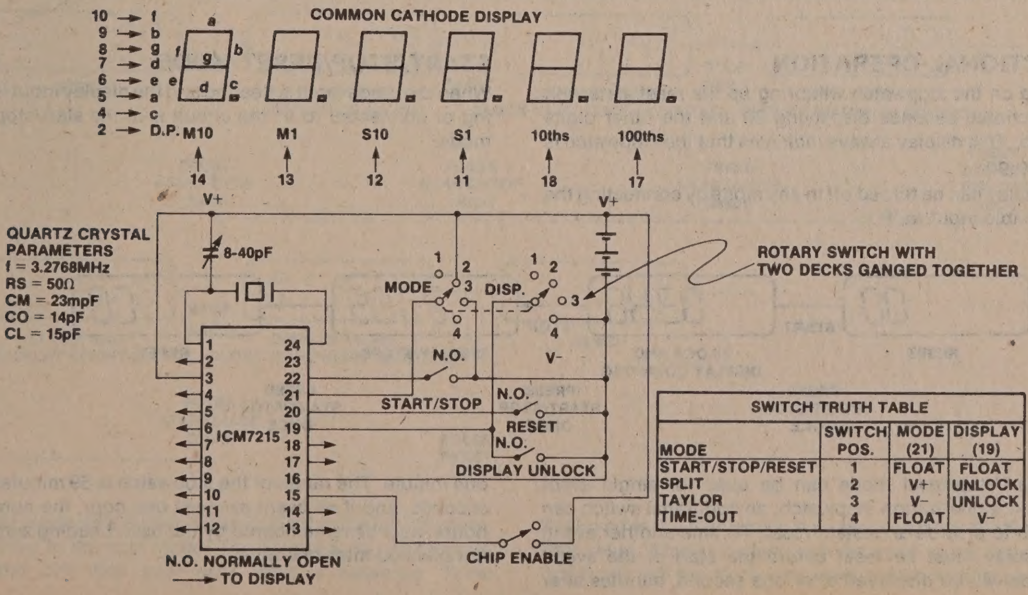
OPERATING CHARACTERISTICS:

TEST CONDITIONS: $T_A = +25°C$, stopwatch circuit, $V^+ = 4.0V$ unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V^+	$-20°C \leq T_A \leq +70°C$	2.0		5.0	V
Supply Current	I^+	Display off		0.6	1.5	mA
Segment Current	I_{SEG}	5 segments lit				
Peak		1.8 Volts across display	9.0	13.2		
Average				2.2		
Switch Actuation Current	I_{SW}	All inputs except chip enable		20	50	μA
Switch Actuation Current		Chip enable		50	200	
Digit Leakage Current	I_{DLK}	$V_{DIG} = 2.0V$			50	
Segment Leakage Current	I_{SLK}	$V_{SEG} = 2.0V$			100	
Low Battery Indicator Trigger Voltage	V_{LBI}		2.2		2.8	V
LBI Output Current	I_{LBI}	$V^+ = 2.0V$, $V_{LBI} = 1.6V$		2.0		mA
Oscillator Stability	f_{STAB}	$V^+ = 2.0V$ to $V^+ = 5.0V$		6		PPM
Oscillator Transconductance	g_m	$V^+ = 2.0V$	120			μmho
Oscillator Input Capacitance	C_{OSCI}		24	30	36	pF

NOTE 1: The output devices on the ICM7215 have very low impedance characteristics, especially the digit cathode drivers. If these devices are shorted to a low impedance power supply, the current could be as high as 300mA. This will not damage the device momentarily, but if the short circuit condition is not removed immediately probable device failure will occur.

STOPWATCH CIRCUIT



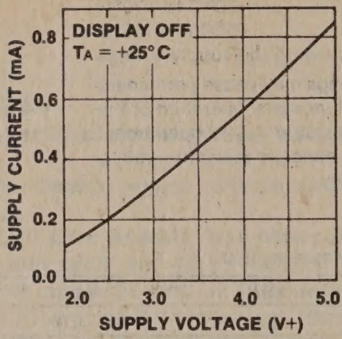
COMMON CATHODE DISPLAY
10 → f
9 → b
8 → g
7 → d
6 → e
5 → a
4 → c
2 → D.P.
a
b
c
d
e
f
g
M10
M1
S10
S1
10ths
100ths
14
13
12
11
18
17
V+
V+
QUARTZ CRYSTAL PARAMETERS
f = 3.2768MHz
RS = 50Ω
CM = 23mpF
CO = 14pF
CL = 15pF
8-40pF
MODE
DISP.
1
2
3
4
ROTARY SWITCH WITH TWO DECKS GANGED TOGETHER
V−
N.O.
START/STOP
RESET
DISPLAY UNLOCK
CHIP ENABLE
ICM7215
1 2 3 4 5 6 7 8 9 10 11 12
24 23 22 21 20 19 18 17 16 15 14 13
N.O. NORMALLY OPEN
→ TO DISPLAY

SWITCH TRUTH TABLE

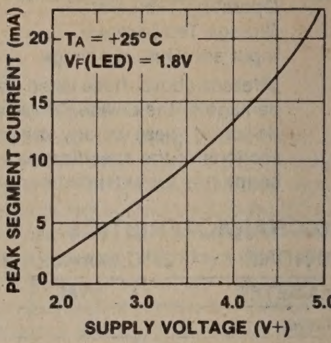
MODE	SWITCH POS.	MODE (21)	DISPLAY (19)
START/STOP/RESET	1	FLOAT	FLOAT
SPLIT	2	V+	UNLOCK
TAYLOR	3	V−	UNLOCK
TIME-OUT	4	FLOAT	V−

TYPICAL PERFORMANCE CHARACTERISTICS

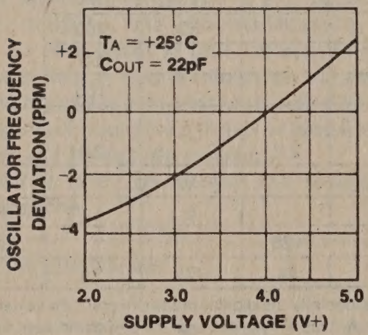
SUPPLY CURRENT VS VOLTAGE



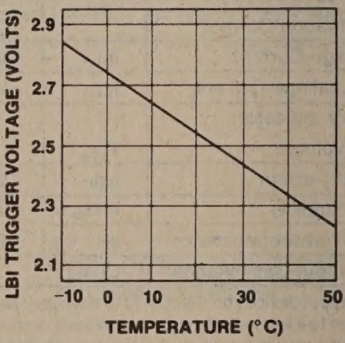
SEGMENT CURRENT VS SUPPLY VOLTAGE



OSC. STABILITY VS SUPPLY VOLTAGE



LOW BATTERY INDICATOR (LBI) TRIGGER VOLTAGE VS TEMPERATURE



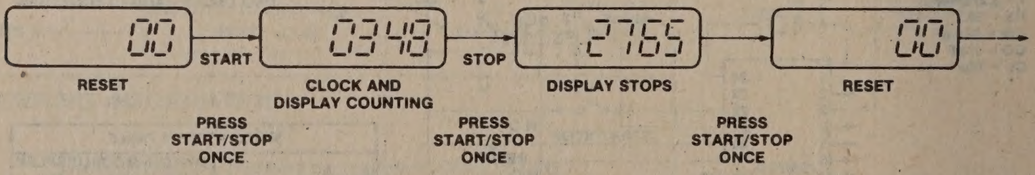
FUNCTIONAL OPERATION

Turning on the stopwatch will bring up the reset state with the fractional seconds displaying 00 and the other digits blanked. This display always indicates that the stopwatch is ready to go.

The display can be turned off in any mode by connecting the chip enable input to V+.

START/STOP/RESET MODE

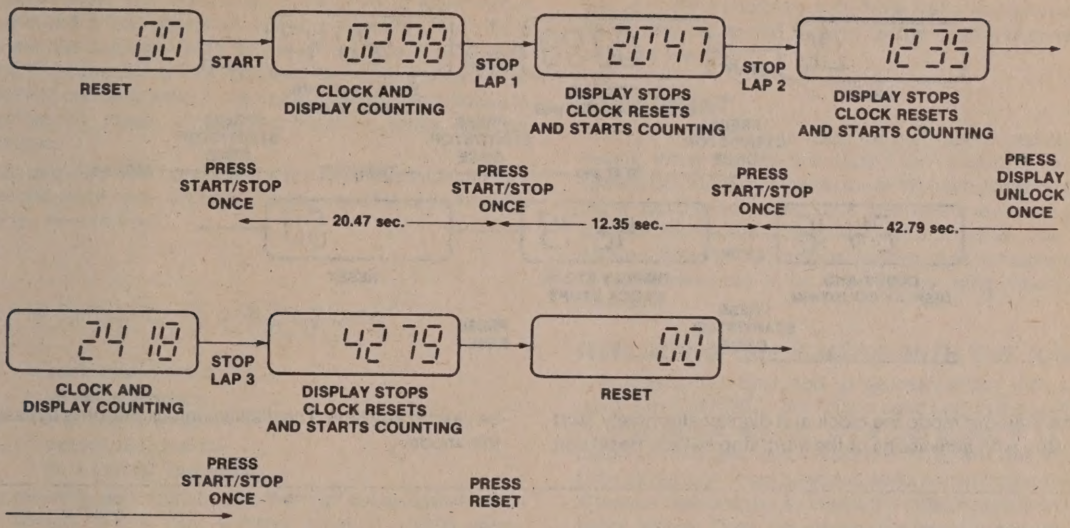
When the mode input is floating and the display input is floating or connected to V+ the circuit is in the start/stop/reset mode.


00
START
0348
STOP
2765
00
RESET
CLOCK AND DISPLAY COUNTING
DISPLAY STOPS
RESET
PRESS START/STOP ONCE
PRESS START/STOP ONCE
PRESS START/STOP ONCE

The start/stop/reset mode can be used for single event timing in a one-button stopwatch; an additional switch can be used to provide an instant reset. To time another event, the display must be reset before the start of the event. Seconds will be displayed after one second, minutes after one minute. The range of the stopwatch is 59 minutes 59.99 seconds, and if an event exceeds one hour, the number of hours must be remembered by the user. Leading zeroes are not blanked after one hour.

TAYLOR OR SEQUENTIAL MODE

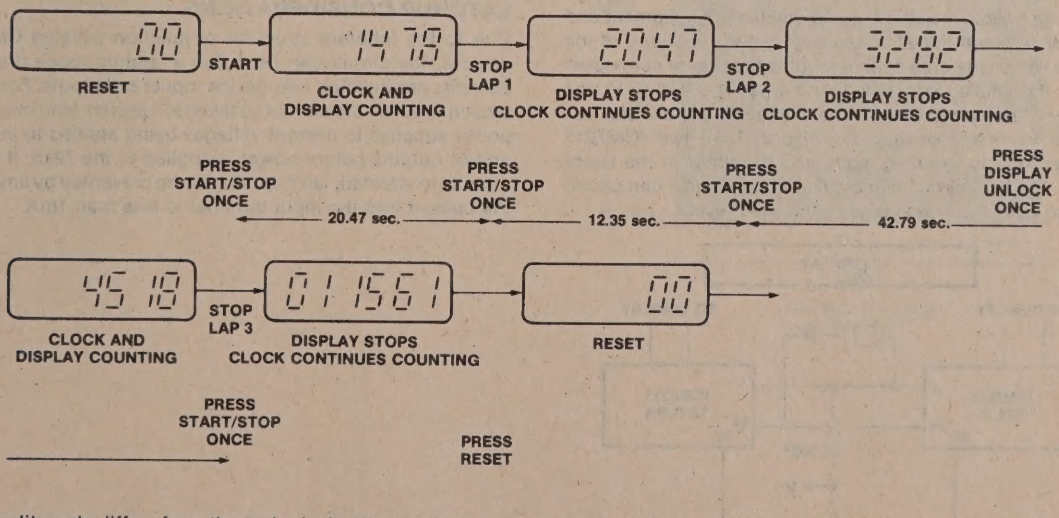
When the mode input is connected to V−, the stopwatch is in the taylor or sequential mode.


00
START
02 98
STOP
LAP 1
20 47
STOP
LAP 2
12 35
RESET
CLOCK AND
DISPLAY COUNTING
DISPLAY STOPS
CLOCK RESETS
AND STARTS COUNTING
DISPLAY STOPS
CLOCK RESETS
AND STARTS COUNTING
PRESS
START/STOP
ONCE
PRESS
START/STOP
ONCE
PRESS
START/STOP
ONCE
PRESS
DISPLAY
UNLOCK
ONCE
20.47 sec.
12.35 sec.
42.79 sec.
24 18
STOP
LAP 3
42 79
00
CLOCK AND
DISPLAY COUNTING
DISPLAY STOPS
CLOCK RESETS
AND STARTS COUNTING
RESET
PRESS
START/STOP
ONCE
PRESS
RESET

Each split time is measured from zero in the taylor mode; i.e., after stopping the watch, the counters reset momentarily and start counting the next interval. The time displayed is that elapsed since the last activation of start/stop. The display is stationary after the first interval unless the display unlock is used to show the running clock. Reset can be used at any time.

SPLIT MODE

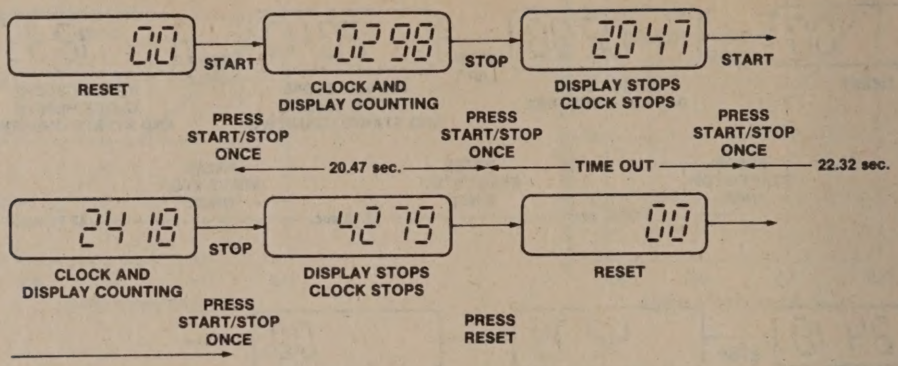
When the mode input is connected to V+ the stopwatch is in the split mode.


00
START
14 78
STOP
LAP 1
20 47
STOP
LAP 2
32 82
RESET
CLOCK AND
DISPLAY COUNTING
DISPLAY STOPS
CLOCK CONTINUES COUNTING
DISPLAY STOPS
CLOCK CONTINUES COUNTING
PRESS
START/STOP
ONCE
PRESS
START/STOP
ONCE
PRESS
START/STOP
ONCE
PRESS
DISPLAY
UNLOCK
ONCE
20.47 sec.
12.35 sec.
42.79 sec.
45 18
STOP
LAP 3
01 15 61
00
CLOCK AND
DISPLAY COUNTING
DISPLAY STOPS
CLOCK CONTINUES COUNTING
RESET
PRESS
START/STOP
ONCE
PRESS
RESET

The split mode differs from the taylor in that the lap times are cumulative in the split mode. The counters do not reset or stop after the first start until reset is activated. Time displayed is the cumulative time elapsed since the first start after reset. Display unlock can be used to let the display 'catch up' with the clock, and reset can be used at any time.

TIME OUT MODE

When the mode input is floating and the display input is tied to V-, the stopwatch is in the time-out mode.


00
START
02 98
STOP
20 47
START
RESET
CLOCK AND DISPLAY COUNTING
DISPLAY STOPS CLOCK STOPS
PRESS START/STOP ONCE
PRESS START/STOP ONCE
PRESS START/STOP ONCE
20.47 sec.
TIME OUT
22.32 sec.
24 18
STOP
42 79
00
CLOCK AND DISPLAY COUNTING
DISPLAY STOPS CLOCK STOPS
RESET
PRESS START/STOP ONCE
PRESS RESET

In the time-out mode the clock and display alternately start and stop with activations of the start/stop switch. Reset can be used at any time. The display unlock button is bypassed in this mode.

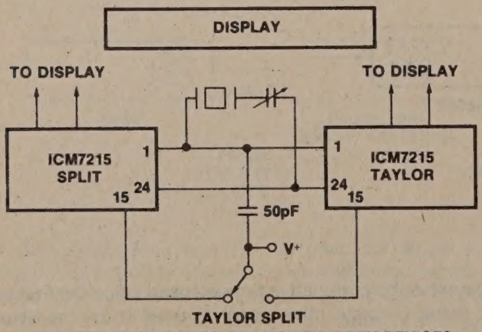
APPLICATION NOTES

LOW BATTERY INDICATOR

The on-chip low battery indicator is intended for use with a small LED or the decimal points on a standard LED display. The output is the drain of a p-channel transistor two-thirds the size of the segment drivers, and designed to provide a trigger voltage of approximately 2.5 volts at room temperature. Normal AA type batteries will provide many hours of accurate timekeeping after the indicator comes on, however the wide voltage spread between the LBI voltage and minimum operating voltage is required to guarantee low battery indication under worst case conditions.

CHIP ENABLE

The chip enable input is used to disable both segment and digit drivers without affecting any of the functions of the device. When the chip enable input is floating or connected to V-, the display is enabled, and when the tied to V+ the display is turned off. One example of the many possible uses of this feature is driving one display from two ICM7215 devices, one in the split mode and the other in the taylor mode. The circuit below indicates how the user can obtain lap and cumulative readings of the same event.


DISPLAY
TO DISPLAY
TO DISPLAY
ICM7215 SPLIT
1
24
15
ICM7215 TAYLOR
1
24
15
50pF
V+
TAYLOR SPLIT

ALL OTHER SWITCHES COMMON TO BOTH DEVICES

SWITCH CHARACTERISTICS

The ICM7215 is designed for use with SPST switches throughout. On the display unlock and reset inputs the characteristics of the switches are unimportant, since the circuit responds to a logic level held for any length of time however short. Switch bounce on these inputs does not need to be specified. The start/stop input, however, responds to an edge and so requires a switch with less than 15ms of switch bounce. The bounce protection circuitry has been specifically designed to let the circuit respond to the first edge of the signal, so as to preserve the full accuracy of the system.

LATCHUP CONSIDERATIONS

Due to the inherent structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied to the 7215. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

OSCILLATOR DESIGN

The oscillator of the ICM7215 includes all components on chip except the 3.2768 MHz crystal and the trimming capacitor. The oscillator input capacitance has a nominal value of 30pF, and the circuit is designed to work with a crystal with a load capacitance of approximately 15pF. If the crystal has characteristics as shown on page 3, an 8-40pF trimming capacitor will be adequate for a tuning tolerance of ±30PPM on the crystal. If the crystal's static capacitance is significantly lower, a narrower trimming range may be selected.

After deciding on a crystal and a nominal load capacitance, take the worst case values of C_{in}, C_{out} and R_S and calculate the g_m required by:

$$g_m = \omega^2 C_{in} C_{out} R_S \left\{1 + \frac{C_o (C_{in} + C_{out})}{C_{in} C_{out}}\right\}^2$$

C_o = static capacitance
R_S = series resistance
C_{in} = input capacitance
C_{out} = output capacitance
ω = 2π x crystal frequency

The resulting g_m should be less than half the g_m specified for the device. If it is not, a lower value of crystal series resistance and/or load capacitance should be specified.

OSCILLATOR TUNING

Tuning can be accomplished by using the 10th or 100th seconds with the device reset. The frequency on the cathode should be tuned to 1066.667 Hz, which is equivalent to a period of 937.5 microseconds. Note that a frequency counter cannot be connected directly to the oscillator because of possible loading.

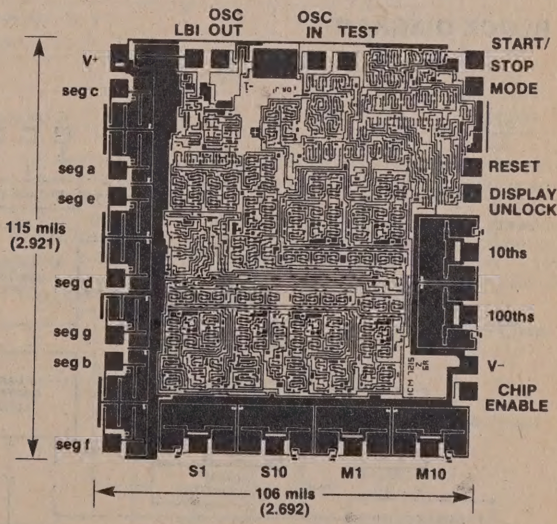
TEST POINT

The test point input is used for high speed testing of the device. When the input is pulsed low, a latch is set which speeds up counting by a factor of 32; each pulse on the test point rapidly advances both minutes and seconds in a parallel mode. To accurately rapid advance the signal applied to the test point must be free of switch bounce. The circuit is taken out of the test mode by using either reset or start/stop.

REPLACING THE ICM7205 WITH THE ICM7215

The ICM7215 is designed to be compatible with circuits using the ICM7205. If the 7205 is used only in the split mode no changes are required. If the 7205 is used in the taylor mode and the split taylor input (pin 21) is left open, a jumper from pin 21 to V− must be added when converting to the 7215. A jumper may also be needed if the 7205 is used with a split/taylor switch. Once the jumper has been added the board can be used with either device.

CHIP TOPOGRAPHY



PAD SIZE 5 x 5 mils
(0.127 x 0.127)

INTERSIL

ICM7223
4-Digit LCD Clock Circuit with Snooze Alarm

FEATURES

- **3-1/2 or 4 digit display with AM/PM and alarm flags**
- **12/24 hour user selectable formats**
- **Direct alarm drive @ 3V p-p, with complex (cricket) alarm tone**
- **8 minute snooze (Dice programmable from 2 to 14 minutes in two minute increments)**
- **Single battery operation (1.5V)**
- **Low current — 6 μA maximum**
- **On-chip fixed oscillator input capacitor**
- **32 kHz oscillator requires only quartz crystal and trimming capacitor**
- **Voltage tripler for large displays**

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7223IPL	-20°C to +70°C	40 Pin Plastic DIP
ICM7223D/D	-20°C to +70°C	DICE

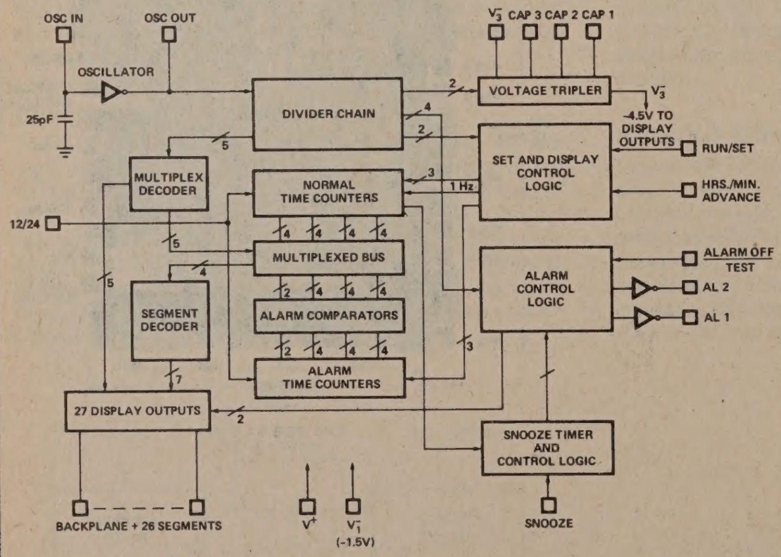
GENERAL DESCRIPTION

The ICM7223 is a fully integrated 4-digit LCD clock circuit with 24 hour alarm and 8 minute snooze timer. For high accuracy and low power consumption a 32.768 KHz quartz watch crystal is used as the time base, and the number of external components has been reduced to a minimum.

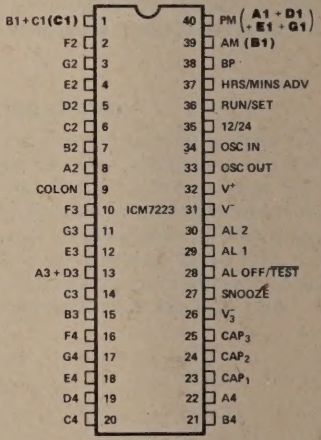
The time keeping and alarm time counters are split during setting, allowing hours and minutes to be set independently, each at a 2 Hz rate. A 'time hold' mode is entered when setting minutes; seconds are automatically reset to zero. The clock starts when the RUN mode is entered, thereby permitting synchronization of the clock to the nearest second. Seconds are not displayed.

The ICM7223 is fabricated using Intersil's low threshold metal gate CMOS process for minimum cost and long battery life.

BLOCK DIAGRAM


OSC IN
OSC OUT
OSCILLATOR
25pF
DIVIDER CHAIN
MULTIPLEX DECODER
NORMAL TIME COUNTERS
MULTIPLEXED BUS
SEGMENT DECODER
ALARM COMPARATORS
ALARM TIME COUNTERS
27 DISPLAY OUTPUTS
12/24
V3̄ CAP 3 CAP 2 CAP 1
VOLTAGE TRIPLER
V3̄
-4.5V TO DISPLAY OUTPUTS
SET AND DISPLAY CONTROL LOGIC
RUN/SET
HRS./MIN. ADVANCE
1 Hz
ALARM CONTROL LOGIC
ALARM OFF/TEST
AL 2
AL 1
SNOOZE TIMER AND CONTROL LOGIC
SNOOZE
BACKPLANE + 26 SEGMENTS
V+
V1̄ (-1.5V)

PIN CONFIGURATION
(OUTLINE DRAWING PL)


B1+C1(C1) 1
F2 2
G2 3
E2 4
D2 5
C2 6
B2 7
A2 8
COLON 9
F3 10
G3 11
E3 12
A3+D3 13
C3 14
B3 15
F4 16
G4 17
E4 18
D4 19
C4 20
ICM7223
40 PM (A1+D1 +E1+G1)
39 AM (B1)
38 BP
37 HRS/MINS ADV
36 RUN/SET
35 12/24
34 OSC IN
33 OSC OUT
32 V+
31 V-
30 AL 2
29 AL 1
28 AL OFF/TEST
27 SNOOZE
26 V3̄
25 CAP3
24 CAP2
23 CAP1
22 A4
21 B4

PARENTHESES AND **BOLD TYPE** INDICATE 24 HOUR OPERATION

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... -55°C to +125°C
Operating Temperature .... -10°C to +60°C
Power Dissipation[1] .... 100 mW
Supply Voltage[2]
$V^+ - V_{\bar{1}}$ 2.0V
$V^+ - V_{\bar{3}}$ 5.5V
Input Voltage (Osc. In, Test,
Set, Display) .... $V^- \leq V_{IN} \leq V^+$
Output Voltage (Osc. Out, 512) ..... $V_{\bar{1}} \leq V_{OUT} \leq V^+$
(All Other Pins) .... $V_{\bar{3}} \leq V_{OUT} \leq V^+$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

OPERATING CHARACTERISTICS

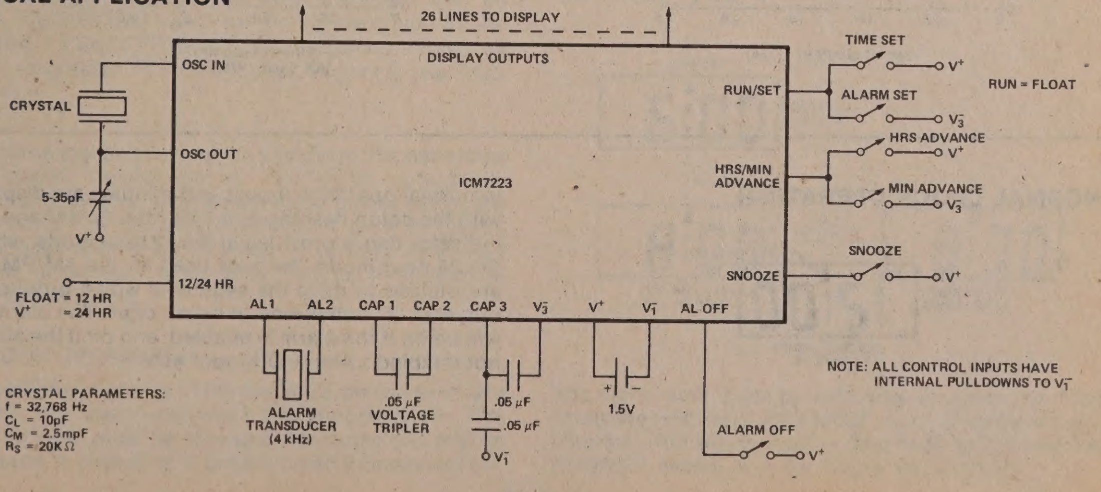
TEST CONDITIONS: $V^+ - V^- = 1.55V$, voltage tripler connected, $T_A = 25°C$, Test Circuit, unless otherwise specified, voltages and currents are shown as absolute values.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V^+	$V^- = 0V$ $-10°C < T_A < 60°C$	1.2		1.8	Volts
Supply Current	I^+	Display Disconnected		4	6	µA
Tripler Output Voltage	$V_{\bar{3}}$	$I_3 = 0.0\ \mu A$ $I_3 = 1.0\ \mu A$	4.2 4.1			V
Segment Drive Current	I_{SEG}	$V_{SAT} = 0.2V$ (Both Directions)	5			µA
Backplane Drive Current	I_{BP}	$V_{SAT} = 0.1V$ (Both Directions)	20			µA
Switch Actuation Current	I_{SW}	$V_{SW} = V^+$ or $V_{SW} = V_{\bar{3}}$		3	5	µA
Alarm Saturation Resistance	$R_{AL(ON)}$	P-CH at 1 mA P-CH		350	500	Ω
		N-CH at 0.5 mA N-CH		1500	1800	
Oscillator Stability	f_{STAB}	$V^- = 0V$, $1.20V \leq V^+ \leq 1.55V$, $C_{OUT} = 25$ pF		2		PPM
Oscillator Input Current[3]	I_{OSCI}	'OSC IN' Connected to V^+ 'OSC OUT' Open Circuit		0.2		µA
Oscillator Input Capacitance	C_{IN}		20	25	30	pF
Oscillator Transconductance	g_m		10	15		µmho

Notes:

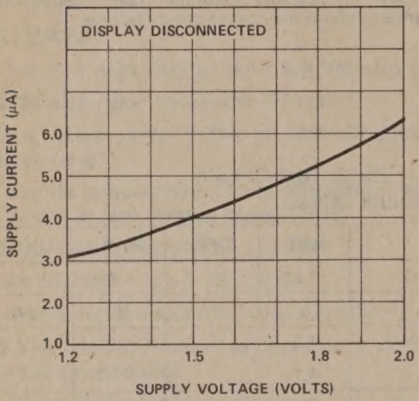
1. The ICM7223 is fully short circuit protected on all inputs and outputs. However, if by forward biasing an input or output the device is put into a latchup condition, power dissipation must be limited to 100 mW to prevent destruction of the device.
2. The ICM7223 is intended for use with two power supplies, one of which is derived from an external battery $V_{\bar{1}}$ and the other is generated internally by the voltage multiplier ($V_{\bar{3}}$ The common point of the two supplies is the most positive, V+. If desired the circuit can be supplied with an external $V_{\bar{3}}$ by disconnecting the multiplier capacitors, or $V_{\bar{3}}$ and $V_{\bar{1}}$ can be tied together (for a 1.5 volt display for instance).
3. The integrated oscillator biasing components have a nonlinear characteristic depending on the instantaneous values of the input and output voltages of the oscillator and the supply. Under oscillator startup conditions this component has a maximum value.

TYPICAL APPLICATION

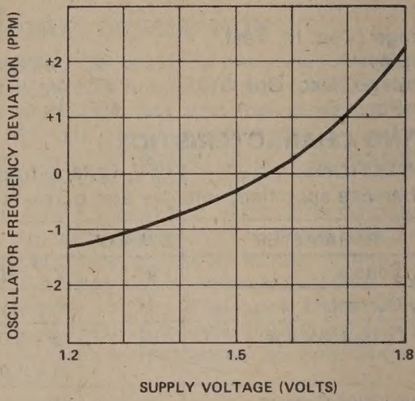

26 LINES TO DISPLAY
DISPLAY OUTPUTS
OSC IN
CRYSTAL
OSC OUT
5-35pF
V+
ICM7223
12/24 HR
FLOAT = 12 HR
V+ = 24 HR
AL1
AL2
CAP 1
CAP 2
CAP 3
V3̄
V+
V1̄
AL OFF
RUN/SET
TIME SET
V+
ALARM SET
V3̄
RUN = FLOAT
HRS/MIN ADVANCE
HRS ADVANCE
V+
MIN ADVANCE
V3̄
SNOOZE
SNOOZE
V+
ALARM TRANSDUCER (4 kHz)
.05 µF VOLTAGE TRIPLER
.05 µF
.05 µF
V1̄
+
1.5V
ALARM OFF
V+
NOTE: ALL CONTROL INPUTS HAVE INTERNAL PULLDOWNS TO V1̄
CRYSTAL PARAMETERS:
f = 32,768 Hz
CL = 10pF
CM = 2.5mpF
RS = 20KΩ

TYPICAL PERFORMANCE CHARACTERISTICS

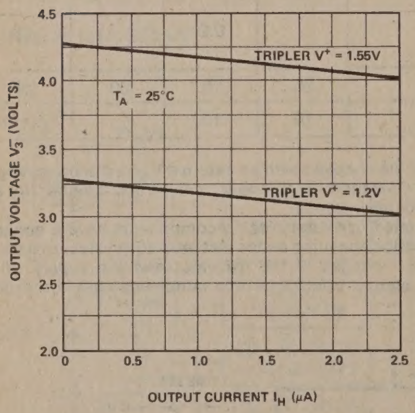
SUPPLY CURRENT VS. SUPPLY VOLTAGE



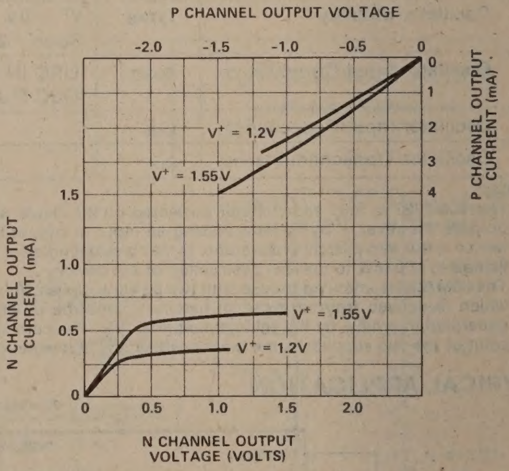
OSCILLATOR STABILITY VS. SUPPLY VOLTAGE



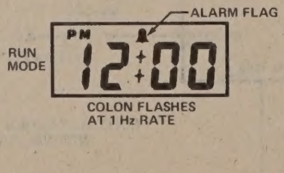
VOLTAGE MULTIPLIER OUTPUT VOLTAGE VS. OUTPUT CURRENT



ALARM DRIVER OUTPUT CURRENT VS. OUTPUT VOLTAGE

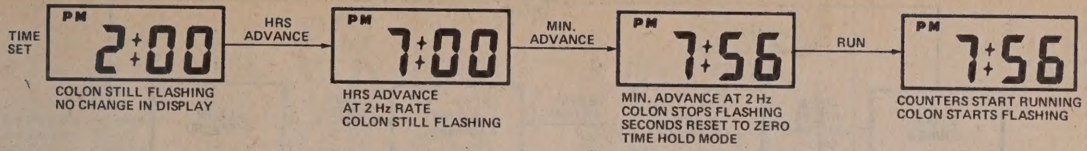


NORMAL CLOCK OPERATION



In normal operation, hours and minutes are displayed with the colon flashing at a 1 Hz rate. An AM and a PM indicator flag is provided in the 12 hour mode, while in the 24 hour mode, the pads used for the AM/PM flags are utilized to drive the segments which produce the numeral "2" in the tens of hours digit. The alarm flag will be on if the alarm is enabled, and off if the alarm is not enabled; (Alarm Off input at V+).

TIME SETTING

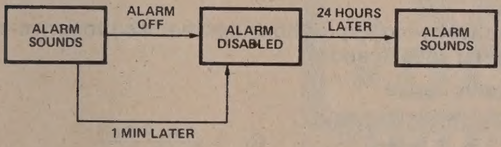

TIME SET
PM 2:00
COLON STILL FLASHING
NO CHANGE IN DISPLAY
HRS ADVANCE
PM 7:00
HRS ADVANCE
AT 2 Hz RATE
COLON STILL FLASHING
MIN. ADVANCE
PM 7:56
MIN. ADVANCE AT 2 Hz
COLON STOPS FLASHING
SECONDS RESET TO ZERO
TIME HOLD MODE
RUN
PM 7:56
COUNTERS START RUNNING
COLON STARTS FLASHING

NOTE: When the HRS/MIN Advance input is activated there will be a pause of less than one second before the counters start advancing at a 2 Hz rate.

TIME SETTING

To set the time, the RUN/SET switch is placed in the Time Set position, and the HRS/MIN advance input is used to advance the hours or minutes. The seconds are reset to zero and counting is stopped whenever the minutes are set. The clock will start when the RUN/SET switch is put back into the RUN position, and while in the RUN position, inputs from the HRS/MIN advance switch are disabled to prevent accidental setting.

ALARM OPERATION


ALARM SOUNDS
ALARM OFF
ALARM DISABLED
24 HOURS LATER
ALARM SOUNDS
1 MIN LATER

The alarm comparator provides a 24 hour alarm in both 12 and 24 hour modes. When the time of day and alarm times are equal, the alarm outputs are enabled, providing that the ALARM OFF input is at V^-. If the ALARM OFF input is at V^+, the alarm outputs will not be enabled. The alarm outputs provide a push-pull, or bridge, configuration for direct drive of a piezoelectric transducer, and if increased drive (loudness) is desired, a coil and external NPN transistor may be used. The external transistor should be driven by the ALARM 1 output. The coil DC resistance should be 100Ω or greater, to limit the peak current to less than 13 mA.

The alarm signal is a complex waveform that generates the Intersil Cricket sound. The alarm output will automatically stop after one minute unless either the ALARM OFF or the SNOOZE input is used. The alarm transducer should be selected to provide maximum output (loudness) at 4 kHz, that is, it should be resonant at 4 kHz.

SNOOZE OPERATION

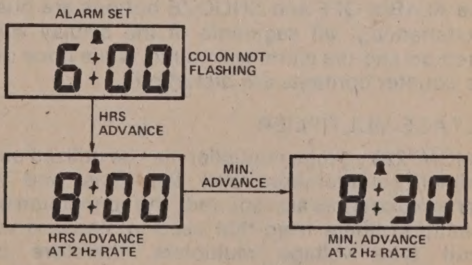
A momentary closure of the SNOOZE switch to V^+ will silence the alarm and start the snooze timer. The Snooze input must be activated during the one minute the alarm is sounding in order to start a Snooze cycle.

After 8 minutes the alarm will again sound, and will continue for 2 minutes and stop unless ALARM OFF is used or another Snooze cycle is activated. The Snooze may be repeated as many times as desired.

NOTE: In die form, all the SNOOZE input pads are available, allowing the manufacturer or user to select snooze times from 2 to 14 minutes in 2 minute steps. These pads are identified as SN1, SN2 and SN3. See the following table for the selection of Snooze times:

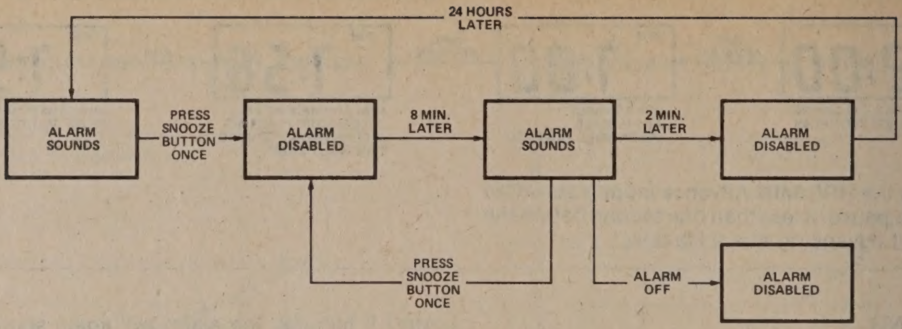
INPUT CODE (1 = V^+)			SNOOZE TIME
SN3	SN2	SN1	
0	0	0	None
0	0	1	2 minutes
0	1	0	4 minutes
0	1	1	6 minutes
1	0	0	8 minutes
1	0	1	10 minutes
1	1	0	12 minutes
1	1	1	14 minutes

ALARM SETTING


ALARM SET
6:00
COLON NOT FLASHING
HRS ADVANCE
8:00
HRS ADVANCE
AT 2 Hz RATE
MIN. ADVANCE
8:30
MIN. ADVANCE
AT 2 Hz RATE

The alarm time is set by switching to Alarm Set, then using the HRS/MIN ADVANCE input to set hours and minutes. The alarm time is displayed only when the RUN/SET switch is in the Alarm Set position.

SNOOZE OPERATION



NOTE: IF ALARM OFF IS LEFT AT V^+ THE ALARM WILL NOT SOUND 24 HOURS LATER.

APPLICATION NOTES

ALARM DRIVE

The ICM7223 alarm output transistors are capable of directly driving a piezoelectric ceramic transducer at 3 volts peak-to-peak. Any transducer that does not require more than 1 mA of peak current may also be used. The transducer should generate maximum output at 4 kHz. If a louder sound is desired, buffering (using an NPN transistor and 5 mho coil) or sound enhancement techniques such as a resonant cavity or diaphragm will be required. See Application Bulletin A031 for details.

TEST MODE

The high speed test mode for automatic testing is entered by pulling the ALARM OFF/TEST Input to -7 volts referenced to V_1^-. In this state the HRS/MIN ADVANCE input will advance the appropriate counters at the rate that the input is toggled. The colon will appear to stop flashing as it is changing state more rapidly than the display can respond. In the run mode the minutes will change at a 4.27 Hz rate, as the clock has been speeded up by a factor of 256 Hz. The backplane frequency will be 512 Hz. The voltage tripler drive frequencies remain the same as in normal modes.

ALARM AND DISPLAY TEST

If the ALARM OFF and SNOOZE buttons are pushed simultaneously, all segments of the display will be turned on and the alarm will sound, while none of the time counter contents are disturbed.

VOLTAGE MULTIPLIER

The ICM7223 voltage multiplier may be utilized only in a tripler configuration; only four pins, and three external capacitors are required. The connection of the capacitors differs from that used in standard watch circuit type voltage multiplers, therefore close attention should be paid to substrate design to ensure the proper connection of the capacitors.

OSCILLATOR

The oscillator of the ICM7223 is designed for low frequency operation at very low currents from a 1.55 volt supply. The oscillator is of the inverter type with a nonlinear feedback resistor included on chip, which has a maximum resistance under startup conditions. The nominal load capacitance of the crystal should be less than 15 pF, typically 12 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance have to be compatible with the characteristics of the circuit to insure startup and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning range

$$\frac{\Delta f}{f} = \frac{C_m}{2\,(C_O + C_L)} ; \quad C_L = \frac{C_{IN}\,C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for startup

$$g_m = 4\pi^2 f^2\, C_{IN}\, C_{OUT}\, R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

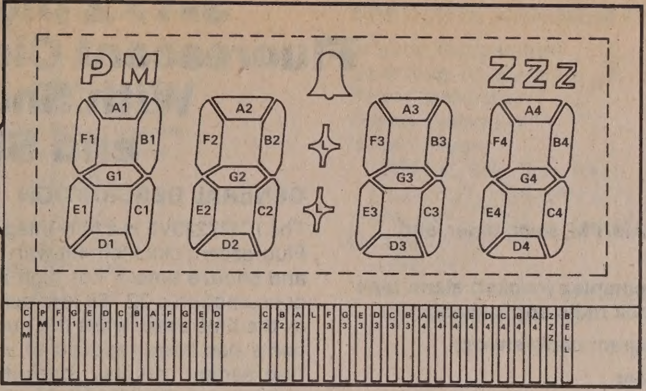
R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance of Crystal
C_m = Motional Capacitance of Crystal

The g_m required for startup calculated should not exceed 50% of the g_m guaranteed for the device.

POWER UP RESET

An on chip circuit is provided that will reset all counters and flip-flops to a known state when power is first applied. The alarm and timekeeping counters will be reset to 1:00 am in the 12 hr. mode and 0:00 in the 24 hr. mode. This function is not tested during automatic testing, as it does not affect normal circuit operation.

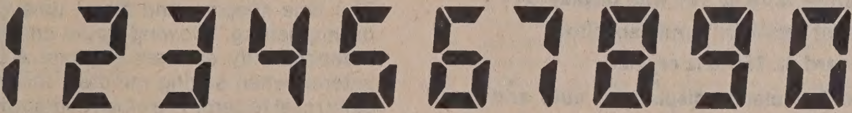
DISPLAY


PM
ZZZ
A1
F1
B1
G1
E1
C1
D1
A2
F2
B2
G2
E2
C2
D2
A3
F3
B3
G3
E3
C3
D3
A4
F4
B4
G4
E4
C4
D4
COM
PM
F1
G1
E1
D1
C1
B1
A1
F2
G2
E2
D2
C2
B2
A2
L
F3
G3
E3
D3
C3
B3
A3
F4
G4
E4
D4
C4
B4
A4
ZZZ
BELL

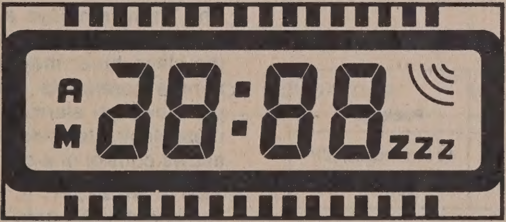
MOTOROLA	MLC406
BECKMAN	737-01
LADCOR	LAD-001
HAMLIN	3411
TIMEX	T1001
COCKROFT	CII202

DISPLAY FONT

NUMBERS

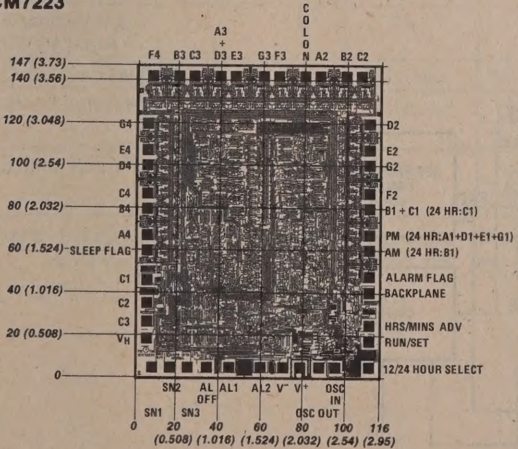


COCKROFT CII201



CHIP TOPOGRAPHY

ICM7223


F4
B3
C3
A3 + D3
E3
G3
F3
COLON
A2
B2
C2
147 (3.73)
140 (3.56)
120 (3.048)
100 (2.54)
80 (2.032)
60 (1.524)
40 (1.016)
20 (0.508)
0
G4
E4
D4
C4
B4
A4
SLEEP FLAG
C1
C2
C3
V_H
D2
E2
G2
F2
B1 + C1 (24 HR:C1)
PM (24 HR:A1+D1+E1+G1)
AM (24 HR:B1)
ALARM FLAG
BACKPLANE
HRS/MINS ADV
RUN/SET
12/24 HOUR SELECT
SN1
SN2
SN3
AL OFF
AL1
AL2
V⁻
V⁺
OSC IN
OSC OUT
0
20 (0.508)
40 (1.016)
60 (1.524)
80 (2.032)
100 (2.54)
116 (2.95)

CHIP DIMENSIONS: 116 x 147 mils (2.95 x 3.73 mm)

INTERSIL

ICM7223VF
3-1/2 Digit Vacuum Fluorescent Clock Circuit With Snooze Timer and Sleep Timer

FEATURES

- **3-1/2 digit display with AM/PM, sleep timer, and alarm flags**
- **Direct alarm drive with complex (cricket) alarm tone plus radio enable for clock radio applications**
- **8 minute repeatable programmable snooze**
- **Programmable sleep timer**
- **Wide operating voltage range — 4 to 15 volts**
- **Low current — 12μA @ 12V with display off**
- **On-chip fixed oscillator input capacitor**
- **Uses standard 32.768 kHz crystal**
- **Display control blanks display for auto and travel clock applications**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7223VFIPL	-20°C to +85°C	40 Pin Plastic DIP
ICM7223VF/D	-20°C to +85°C	Dice

GENERAL DESCRIPTION

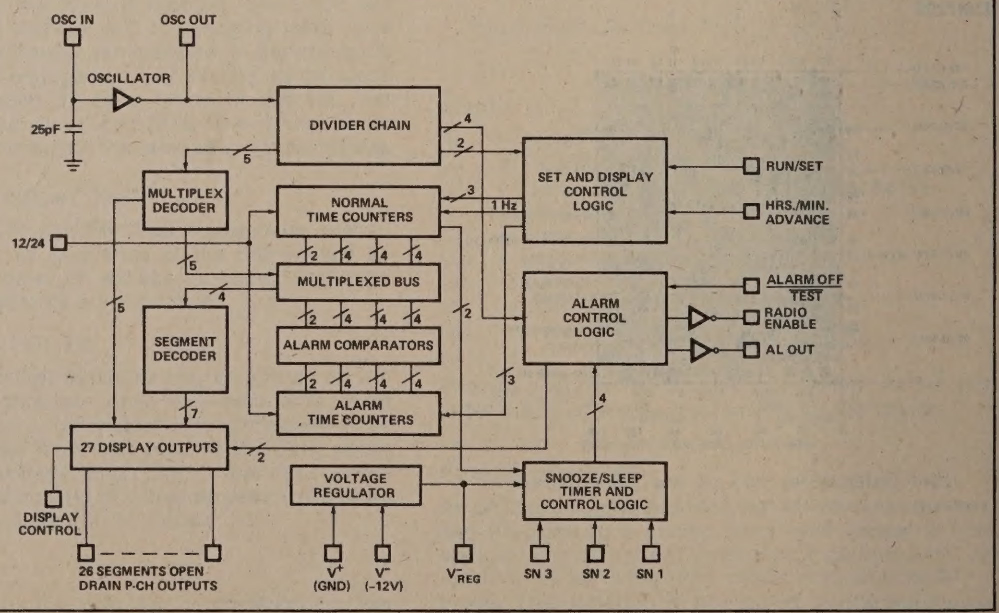
The ICM7223VF is a fully integrated 3-1/2 digit Vacuum Fluorescent clock circuit with 24 hour alarm, and sleep and snooze timers. For high accuracy and low power consumption a 32.768 kHz quartz watch crystal is used as the time base, while the number of external components has been reduced to a minimum. The vacuum fluorescent display outputs are static, or non-multiplexed, thereby eliminating radio frequency interference (RFI).

The time keeping and alarm time counters are split during setting, allowing hours and minutes to be set independently, each at a 2 Hz rate. A 'time hold' mode is entered when setting minutes; seconds are automatically reset to zero. The clock starts when the RUN mode is entered; this permits synchronization of the clock to the nearest second. Seconds are not displayed.

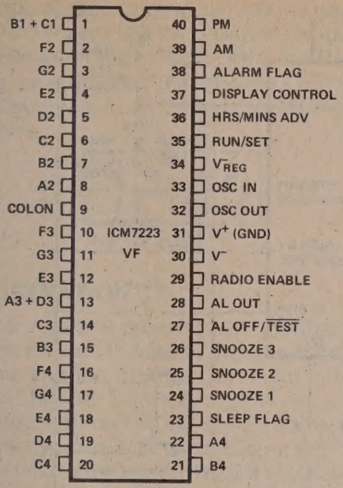
The alarm employs a snooze timer that may be programmed from 2 to 14 minutes in two minute increments; the sleep timer may be set from 8 to 56 minutes in 8 minute increments. The alarm outputs consist of a complex (cricket) alarm tone to directly drive a speaker or piezoelectric transducer and a radio enable output which allows control of a clock radio.

The ICM7223VF is fabricated using Intersil's low threshold metal gate CMOS process for minimum cost and long battery life. Current drain at 12 volts is typically 12μA with a maximum of 25μA (display off).

BLOCK DIAGRAM


OSC IN
OSC OUT
OSCILLATOR
25pF
DIVIDER CHAIN
4
2
5
SET AND DISPLAY CONTROL LOGIC
RUN/SET
HRS./MIN. ADVANCE
MULTIPLEX DECODER
NORMAL TIME COUNTERS
3
1 Hz
12/24
2
4
4
4
5
MULTIPLEXED BUS
4
5
ALARM OFF
TEST
ALARM CONTROL LOGIC
RADIO ENABLE
AL OUT
SEGMENT DECODER
ALARM COMPARATORS
2
3
ALARM TIME COUNTERS
7
4
27 DISPLAY OUTPUTS
2
VOLTAGE REGULATOR
SNOOZE/SLEEP TIMER AND CONTROL LOGIC
DISPLAY CONTROL
26 SEGMENTS OPEN DRAIN P-CH OUTPUTS
V+ (GND)
V- (-12V)
V-REG
SN 3
SN 2
SN 1

PIN CONFIGURATION (OUTLINE DRAWING PL)


B1 + C1 1
F2 2
G2 3
E2 4
D2 5
C2 6
B2 7
A2 8
COLON 9
F3 10
G3 11
E3 12
A3 + D3 13
C3 14
B3 15
F4 16
G4 17
E4 18
D4 19
C4 20
ICM7223
VF
40 PM
39 AM
38 ALARM FLAG
37 DISPLAY CONTROL
36 HRS/MINS ADV
35 RUN/SET
34 VREG
33 OSC IN
32 OSC OUT
31 V+ (GND)
30 V−
29 RADIO ENABLE
28 AL OUT
27 AL OFF/TEST
26 SNOOZE 3
25 SNOOZE 2
24 SNOOZE 1
23 SLEEP FLAG
22 A4
21 B4

NOTE: CONSULT FACTORY IF 24 HOUR TIME DISPLAY IS DESIRED.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... -55°C to +125°C
Operating Temperature .... -20°C to +85°C
Power Dissipation[1] .... 500 mW
Supply Voltage ($V^+ - V^-$) 18V
Input Voltage
(OSC IN, SN_1, SN_2, SN_3) ..... $-2V \le V_{IN} \le V^+ + 0.3V$
(RUN/SET, HRS/MIN ADV, AL OFF/$\overline{TEST}$) ...... $V^- - 0.3V \le V_{IN} \le V^+ + 0.3V$
Output Voltage
(OSC OUT) .... $-2V \le V_{OUT} \le V^+$
(AL OUT, RADIO ENABLE, All Segment Drivers) .... $V^- \le V_{OUT} \le V^+$

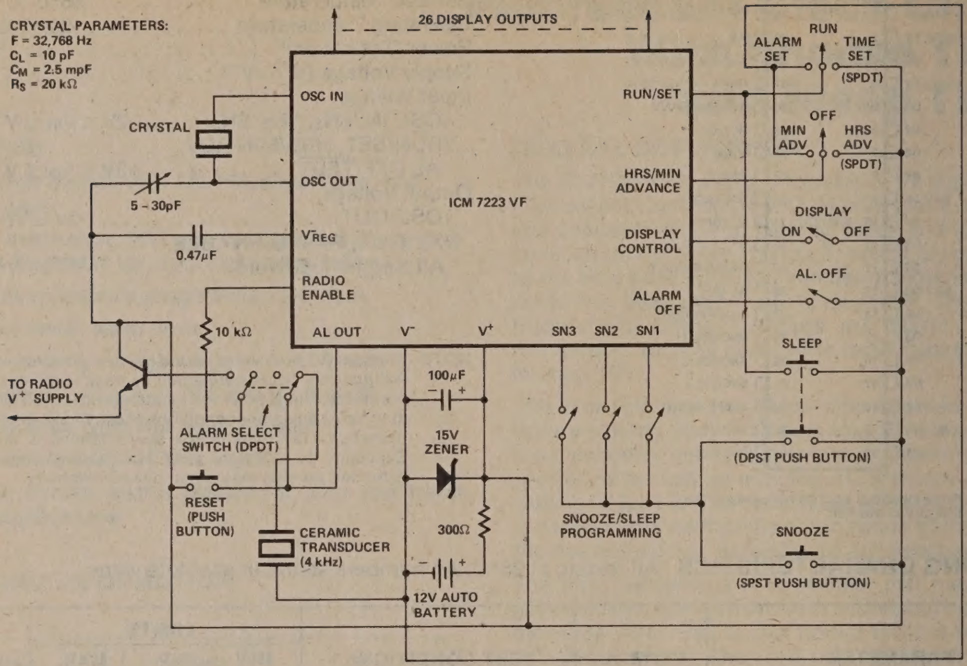
NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS All testing at 25°C; All numbers stated in absolute value

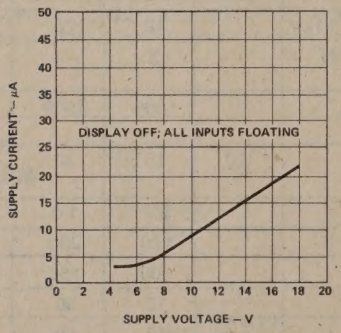
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Supply Voltage Range Timekeeping Accurate	V^+		4		15	V
Supply Current	I^+	Display OFF $V^+ - V^- = 12V$		12	25	μA
Supply Current Display ON[2]		$V^+ - V^- = 12V$, Display Test, NEC LD8164		3		mA
Segment Output Saturation Resistance	R_{SEG}	$I_{DS} = 1mA$ P-ch		1000	1500	Ω
Oscillator Input Capacitance	C_{IN}		20	25	30	pF
Oscillator Stability	f_{STAB}	$5V \le V_{SUPPLY} \le 15V$		0.7	1.0	ppm
Alarm Saturation Resistance	$R_{AL(on)}$	P-ch at 10mA		220	300	Ω
		N-ch at 10mA		100	150	Ω
Switch Actuation Current	I_{SW}	$V_{SW} = V^+$		10	30	μA
		$V_{SW} = V^-$		10	30	μA

NOTES: 1. This value of power dissipation is that of the package and will not be obtained under normal operating conditions.
2. Chip current plus display anode current only; does not include display filament or grid currents.

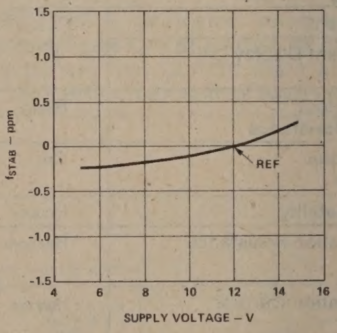
TYPICAL CLOCK RADIO APPLICATION


CRYSTAL PARAMETERS:
F = 32,768 Hz
C_L = 10 pF
C_M = 2.5 mpF
R_S = 20 kΩ
26 DISPLAY OUTPUTS
CRYSTAL
5 – 30pF
0.47µF
OSC IN
OSC OUT
V_{REG}
RADIO ENABLE
AL OUT
V⁻
V⁺
SN3
SN2
SN1
ICM 7223 VF
RUN/SET
HRS/MIN ADVANCE
DISPLAY CONTROL
ALARM OFF
RUN
ALARM SET
TIME SET
(SPDT)
OFF
MIN ADV
HRS ADV
(SPDT)
DISPLAY
ON
OFF
AL. OFF
SLEEP
(DPST PUSH BUTTON)
SNOOZE
(SPST PUSH BUTTON)
SNOOZE/SLEEP PROGRAMMING
10 kΩ
TO RADIO V⁺ SUPPLY
ALARM SELECT SWITCH (DPDT)
RESET (PUSH BUTTON)
CERAMIC TRANSDUCER (4 kHz)
100µF
15V ZENER
300Ω
12V AUTO BATTERY

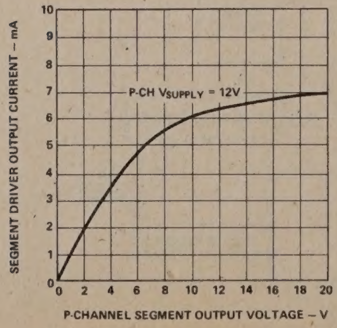
SUPPLY CURRENT vs. SUPPLY VOLTAGE



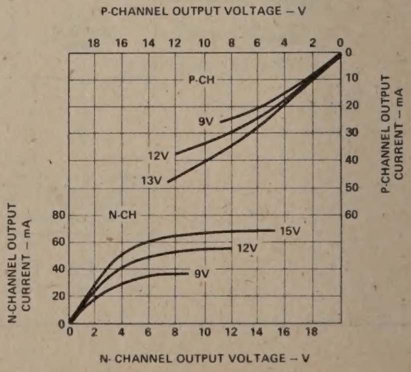
OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



SEGMENT DRIVER OUTPUT CURRENT vs. DRAIN VOLTAGE

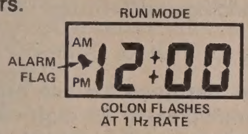


ALARM DRIVER OUTPUT CURRENT vs. OUTPUT VOLTAGE



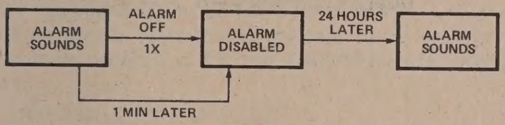
NORMAL CLOCK OPERATION

In normal operation hours and minutes are displayed with the colon flashing at a 1 Hz rate. AM and PM indicators are provided. The alarm flag will be on if the ALARM OFF input is floating, and off with the ALARM OFF input at V$^+$. Time is displayed in a 12 hour format with AM/PM annunciators.

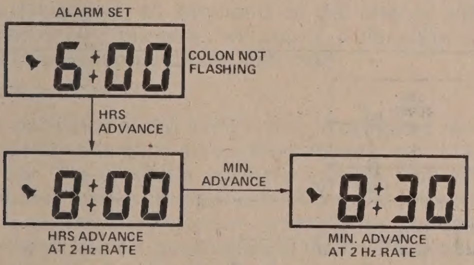

RUN MODE
AM
ALARM FLAG
PM
12:00
COLON FLASHES AT 1 Hz RATE

ALARM OPERATION

The alarm comparator provides a 24 hour alarm by taking into account AM and PM. When the time of day and alarm times agree, and the ALARM OFF input is floating, the ALARM and RADIO ENABLE outputs are activated; the alarm sounds and the RADIO ENABLE line goes to V$^+$. Momentarily tying the ALARM OFF input to V$^+$ will silence both the alarm and the radio. The alarm will automatically shut off after one minute if the ALARM OFF is not used; the RADIO ENABLE will stay HIGH until either the ALARM OFF or SNOOZE inputs are used. The SNOOZE input must be applied within one minute in order to begin a snooze cycle.


ALARM SOUNDS
ALARM OFF
1X
ALARM DISABLED
24 HOURS LATER
ALARM SOUNDS
1 MIN LATER

ALARM SETTING


ALARM SET
6:00
COLON NOT FLASHING
HRS ADVANCE
8:00
MIN. ADVANCE
8:30
HRS ADVANCE AT 2 Hz RATE
MIN. ADVANCE AT 2 Hz RATE

The alarm time is set by switching to Alarm Set, then using the HRS/MIN ADVANCE input to set hours and minutes. The alarm time is displayed only when the RUN/SET switch is in the Alarm Set position.

SNOOZE OPERATION

To begin a snooze cycle, the SNOOZE input must be momentarily shorted to V$^+$ during the one minute that the alarm is sounding or the RADIO ENABLE line is high. When this is done the alarm will be silenced and the snooze timer started; the alarm will sound again after the selected snooze time. Unless the ALARM OFF input is used, the alarm will automatically shut off after two minutes. The RADIO ENABLE will remain on until the ALARM OFF line is activated, however, a second snooze cycle can be initiated with the SNOOZE switch. This can only be done if the SNOOZE is activated while the alarm is sounding.

The snooze times are programmable in 7 steps from 2 to 14 minutes. Programming is accomplished with binary coding on the three SNOOZE inputs, as shown in the following table:

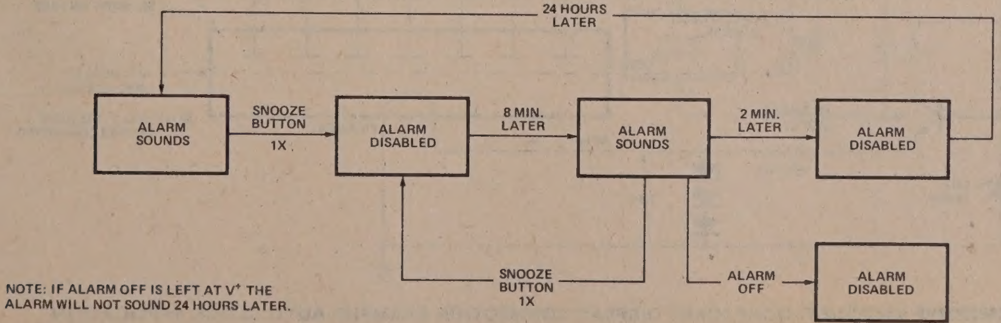
INPUT CODE (1 = V$^+$)			SNOOZE TIME	SLEEP TIME
SN3	SN2	SN1		
0	0	0	None	None
0	0	1	2 minutes	8 minutes
0	1	0	4 minutes	16 minutes
0	1	1	6 minutes	24 minutes
1	0	0	8 minutes	32 minutes
1	0	1	10 minutes	40 minutes
1	1	0	12 minutes	48 minutes
1	1	1	14 minutes	56 minutes

SLEEP OPERATION

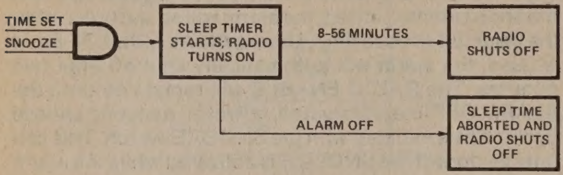
The sleep timer may be activated at any time except during a snooze cycle or when the alarm is sounding. The sleep timer is started by setting the RUN/SET switch in the SET position and momentarily activating the SNOOZE switch. Sleep times are programmed with the snooze inputs; see table on previous page.

Another method for sleep timer activation is to use a single DPST pushbutton switch, with one pole connected to the RUN/SET switch and the other to the common side of the SNOOZE programming switch. The other side of the switches is tied to V$^+$. (See typical application, page 3). This method allows the use of a "dedicated" sleep button, which may be recessed to prevent accidental activation.

SNOOZE OPERATION

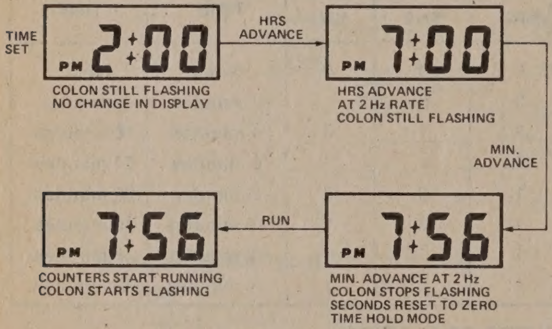

24 HOURS LATER
ALARM SOUNDS
SNOOZE BUTTON
1X
ALARM DISABLED
8 MIN. LATER
ALARM SOUNDS
2 MIN. LATER
ALARM DISABLED
SNOOZE BUTTON
1X
ALARM OFF
ALARM DISABLED
NOTE: IF ALARM OFF IS LEFT AT V+ THE ALARM WILL NOT SOUND 24 HOURS LATER.

When the sleep timer is activated the RADIO ENABLE output is set high to turn on a radio. At end of the programmed sleep time the RADIO ENABLE output is returned to V$^-$.


TIME SET
SNOOZE
SLEEP TIMER STARTS; RADIO TURNS ON
8-56 MINUTES
RADIO SHUTS OFF
ALARM OFF
SLEEP TIME ABORTED AND RADIO SHUTS OFF

TIME SETTING

To set the time, the RUN/SET switch is placed in the Time Set position, and the HRS/MIN advance input is used to advance the hours or minutes. The seconds are reset to zero and counting is stopped whenever the minutes are set. The clock will start when the RUN/SET switch is put back into the RUN position, and while in the RUN position, inputs from the HRS/MIN advance switch are disabled to prevent accidental setting.


TIME SET
PM 2:00
COLON STILL FLASHING
NO CHANGE IN DISPLAY
HRS ADVANCE
PM 7:00
HRS ADVANCE
AT 2 Hz RATE
COLON STILL FLASHING
MIN. ADVANCE
PM 7:56
MIN. ADVANCE AT 2 Hz
COLON STOPS FLASHING
SECONDS RESET TO ZERO
TIME HOLD MODE
RUN
PM 7:56
COUNTERS START RUNNING
COLON STARTS FLASHING

NOTE: When the HRS/MIN Advance input is activated there will be a pause of less than one second before the counters start advancing at a 2 Hz rate.

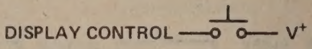
DISPLAY

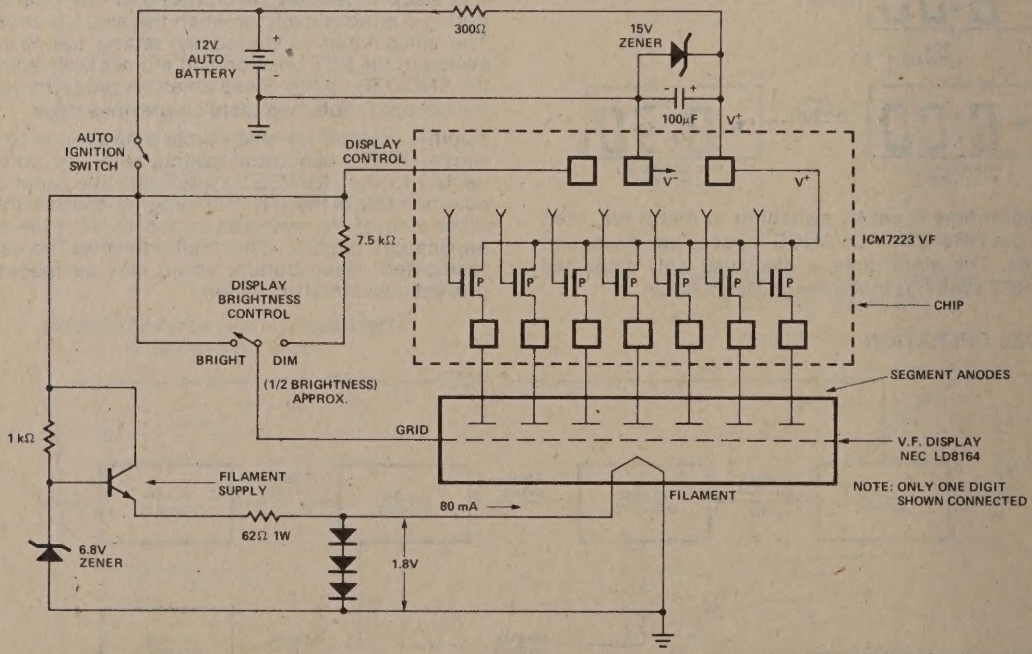
The ICM7223VF is designed for use only with 12V direct drive (non-multiplexed) 3½ digit vacuum fluorescent displays such as the NEC LD8164 or equivalent. (But see "LED Display Driving" under DESIGN CONSIDERATIONS.)

DESIGN CONSIDERATIONS

DISPLAY CONTROL

This input allows the display to be blanked (turned off) when low current operation is desirable, such as when an auto clock is being used with the engine turned off. For normal operation connect DISPLAY CONTROL to V$^+$; to turn off display allow the input to float. A SPST switch can be used for those times when it is desired to turn on the display with the engine off.


DISPLAY CONTROL
V+


300Ω
12V AUTO BATTERY
15V ZENER
100μF
V+
AUTO IGNITION SWITCH
DISPLAY CONTROL
V−
V+
7.5 kΩ
ICM7223 VF
P
CHIP
DISPLAY BRIGHTNESS CONTROL
BRIGHT
DIM
(1/2 BRIGHTNESS) APPROX.
SEGMENT ANODES
GRID
V.F. DISPLAY NEC LD8164
1 kΩ
FILAMENT SUPPLY
FILAMENT
NOTE: ONLY ONE DIGIT SHOWN CONNECTED
80 mA
62Ω 1W
1.8V
6.8V ZENER

ICM7223VF VACUUM FLUORESCENT DISPLAY CONNECTION EXAMPLE; AUTO CLOCK APPLICATION

LED DISPLAY DRIVE

It is possible to drive high efficiency common cathode LED displays with the 7223VF as long as the total display current does not exceed 100mA (or 4mA per segment), as excessive on-chip heating may occur. Operation is not guaranteed for extended periods, since the package power dissipation limits are likely to be exceeded. When driving LED displays with the 7223VF, use of the DISPLAY CONTROL as a "time demand" is highly recommended.

CHIP RESET

Power up reset is not provided on the 7223VF, as interaction between the V^+ and V^- inputs and the voltage regulator in noisy environments could cause spurious resetting. Resetting the circuit to a known state, 1:00 AM, can be accomplished by momentarily connecting the ALARM OUT output to V+; this can be done with a NO SPST switch. This same method may be employed to clear the 7223VF in the event that it powers up in an illegal state.

TEST MODE OPERATION

This mode, provided for high speed automatic testing, is entered by shorting ALARM OFF to V^-. The minutes will then advance at a 4.27 Hz rate and setting can be accomplished by the application of a digital input to the hrs — mins advance input. The counter will then advance once per pulse. Note that in the test mode there is no debounce protection on the HRS/MINS ADVANCE input.

ALARM AND DISPLAY TEST

If the ALARM OFF and SNOOZE buttons are pushed simultaneously, all segments of the display will be turned on and the alarm will sound, while none of the time counter contents are disturbed.

OSCILLATOR

The oscillator of the ICM7223VF is designed for low frequency operation at very low currents from a 12 volt supply. The oscillator is of the inverter type with a nonlinear feedback resistor included on chip, which has a maximum resistance under startup conditions. The nominal load capacitance of the crystal should be less than 15 pF, typically 12 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance have to be compatible with the characteristics of the circuit to insure startup and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)} \; ; \; C_L = \frac{C_{IN} C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for startup

$$g_m = 4\pi^2 f^2 C_{IN} C_{OUT} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance of Crystal
C_m = Motional Capacitance of Crystal

The (calculated) g_m required for startup should not exceed 50% of the g_m guaranteed for the device.

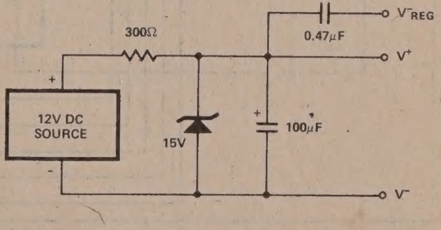
ALARM DRIVE

The ICM7223VF will directly drive any suitable audio transducer (piezoelectric ceramic, or magnetic speaker) with a peak frequency response of 4 kHz with $V^+ = 12V$ and a peak current of 10 mA. The volume should be more than adequate; no buffering should be required.

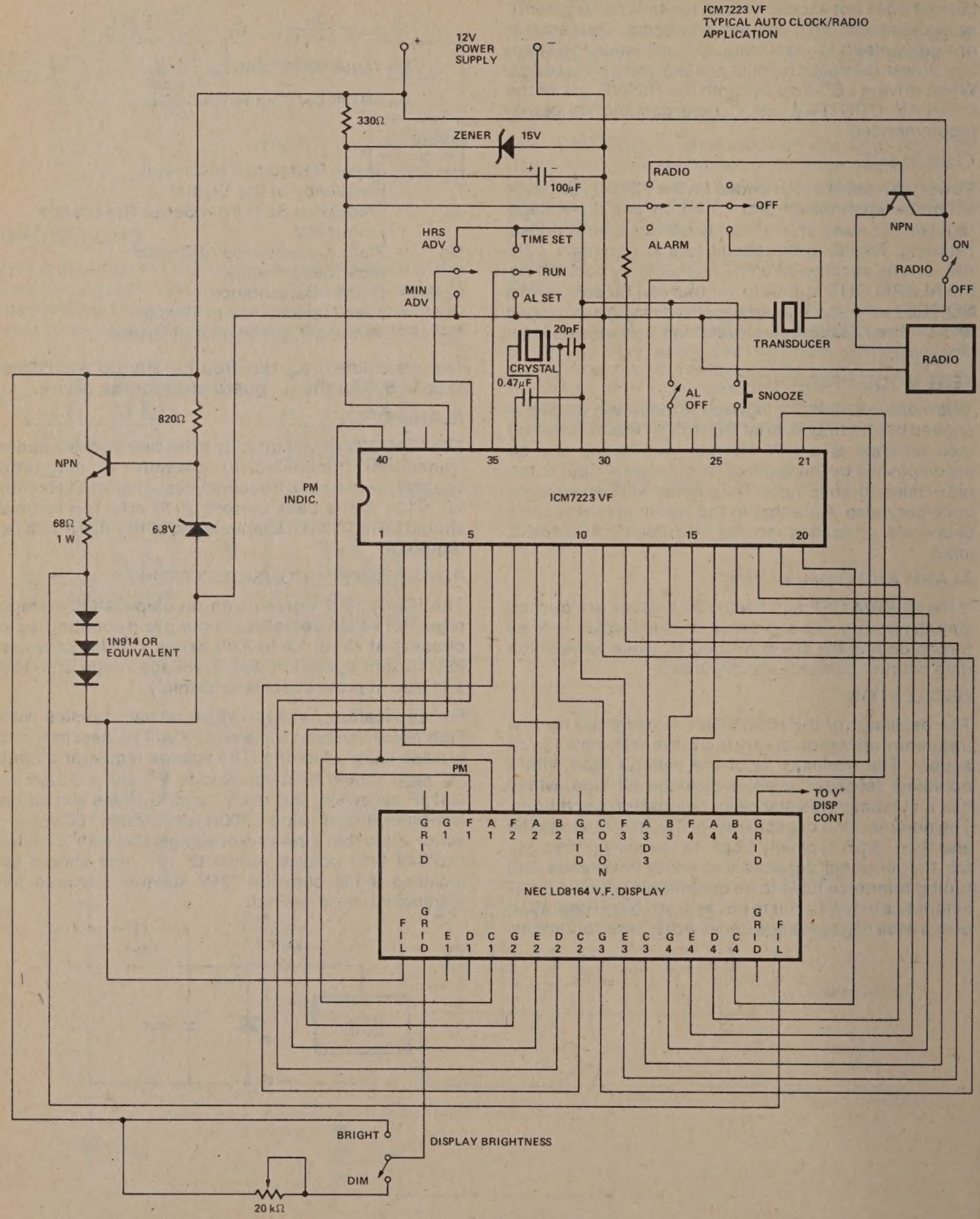
POWER SUPPLY CONSIDERATIONS

The ICM7223VF contains an on-chip CMOS voltage regulator which operates all timing and counting logic circuitry at about 1.8 to 2.0V below V^+. This provides low current operation over a voltage range of 4-15V and also improves oscillator stability.

For applications which involve power supplies with high noise levels or transients, it will be necessary to provide supply filtering. The voltage regulator output (V^-_{REG}) should be decoupled to V^+ with a 0.22μF to 0.47μF capacitor, and the V^+ and V^- lines should be low-pass-filtered using a 300Ω resistor and 100μF capacitor. Note that a zener diode in parallel with the filter cap will limit voltage spikes to 15V, and should be included if the common "24V survival" required for automotive use is desired.



TYPICAL CLOCK RADIO APPLICATION

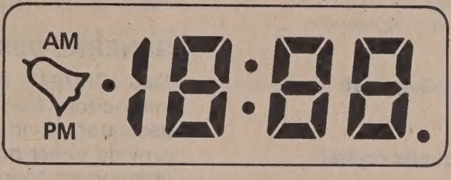


ICM7223 VF
TYPICAL AUTO CLOCK/RADIO
APPLICATION

+
12V POWER SUPPLY
−
330Ω
ZENER
15V
100μF
HRS ADV
TIME SET
MIN ADV
RUN
AL SET
20pF
CRYSTAL
0.47μF
RADIO
OFF
ALARM
NPN
ON
RADIO
OFF
TRANSDUCER
RADIO
AL OFF
SNOOZE
820Ω
NPN
PM INDIC.
68Ω 1 W
6.8V
1N914 OR EQUIVALENT
40
35
30
25
21
ICM7223 VF
1
5
10
15
20
PM
TO V+ DISP CONT
GRID
G1
F1
A1
F2
A2
B2
GRID
COLON
F3
A3 D3
B3
F4
A4
B4
GRID
NEC LD8164 V.F. DISPLAY
FIL
GRID
E1
D1
C1
G2
E2
D2
C2
G3
E3
C3
G4
E4
D4
C4
GRID
FIL
BRIGHT
DISPLAY BRIGHTNESS
DIM
20 kΩ

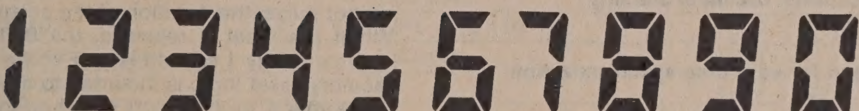
TYPICAL DISPLAY (FIP5E15S)

Other displays (by NEC):
- FIP 5B8S
- LD 8196
- LD 8164

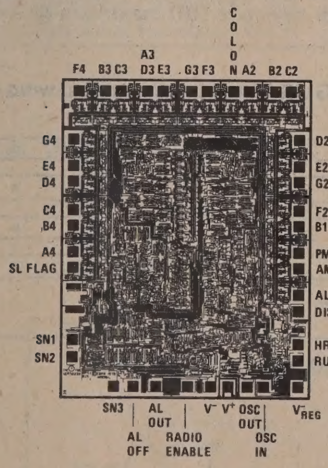


DISPLAY FONT

NUMBERS


1234567890

CHIP TOPOGRAPHY


F4
B3 C3
A3
D3 E3
. G3 F3
COLON
A2
B2 C2
G4
E4
D4
C4
B4
A4
SL FLAG
SN1
SN2
D2
E2
G2
F2
B1 + C1
PM
AM
ALARM FLAG
DISP CONT
HRS/MIN ADV
RUN/SET
SN3
AL OUT
AL OFF
RADIO ENABLE
V⁻
V⁺
OSC OUT
OSC IN
V REG

CHIP DIMENSIONS: 116 x 147 mils (2.95 x 3.73 mm)

INTERSIL

ICM7245
Quartz Analog Watch Circuit

FEATURES

- **Very low current consumption: 0.4μA at 1.55 volt typical**
- **32 kHz oscillator requires only quartz crystal and trimming capacitor**
- **Bipolar stepper drive with low output ON resistance: 200 ohms maximum (7245 A/B/D/E/F)**
- **Unipolar stepper drive with very low output ON resistance: 50 ohms maximum (7245U)**
- **Extremely accurate: oscillator stability typically 0.1 ppm**
- **STOP function for easy time synchronization**
- **TEST input for highspeed testing**
- **Wide temperature range: -20° C to +70° C**
- **On chip fixed oscillator capacitor: 20pF ±20%**

TABLE OF OPTIONS

Device Number	Bipolar/ Unipolar	Pulse Width (ms)	Pulse Frequency	Oscillator Capacitor
ICM7245A	B	9.7	1Hz	C_{OUT}
ICM7245B	B	7.8	1Hz	C_{IN}
ICM7245D	B	7.8	0.1Hz (1 pulse/ 10 seconds)	C_{OUT}
ICM7245E	B	7.8	0.0833Hz (1 pulse/ 12 seconds)	C_{IN}
ICM7245F	B	7.8	0.05Hz (1 pulse/ 20 seconds)	C_{IN}
ICM7245U	U	3.9	1Hz	C_{IN}

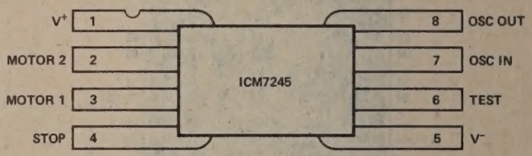
GENERAL DESCRIPTION

The ICM7245 is a very low current, low voltage microcircuit for use in analog watches. It consists of an oscillator, dividers, logic and drivers necessary to provide either bipolar or unipolar drive for minimum-component count watches. The oscillator is extremely stable over wide ranges of voltage and temperature, and thus combines high accuracy with low system power. The ICM7245 is fabricated using Intersil's low threshold metal-gate CMOS process.

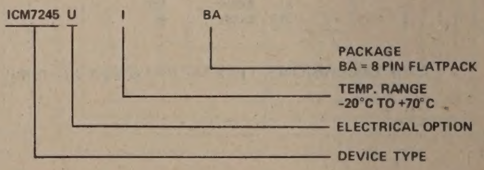
The inverter oscillator contains all components on-chip except for the tuning capacitor and quartz crystal. The binary divider consists of 15 stages, the last 5 of which may be reset. If a reset (stop) occurs during an output pulse, the duration of the pulse is not affected. When the reset is released, the first output occurs approximately 1 second later. For the bipolar version, memory reset logic is included to make sure the first pulse after a "stop" occurs on the opposite output from the one just before the "stop".

The bipolar bridge output consists of two large inverters, normally high. The output ON resistance of the P and N channel devices in series is 200Ω maximum @ 1 mA. In unipolar operation, the output is made up of a single normally high inverter. The ON resistance of the N-channel device is 50Ω maximum @ 3 mA.

PIN CONFIGURATION (OUTLINE DRAWING BA)



ORDERING INFORMATION



ORDER DICE BY FOLLOWING PART NUMBER:
ICM7245A/D
└SELECT OPTION

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... -40°C to +125°C
Operating Temperature .... -20°C to +70°C
Power Dissipation (Note 1) .... 25 mW
Supply Voltage ($V^+ - V^-$) .... 3.0 volts
Lead Temperature (Soldering, 10 sec) ..... 300°C
Input Voltages .... $V^- -0.3 < V_{IN} < V^+ +0.3$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

Note 1.: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.

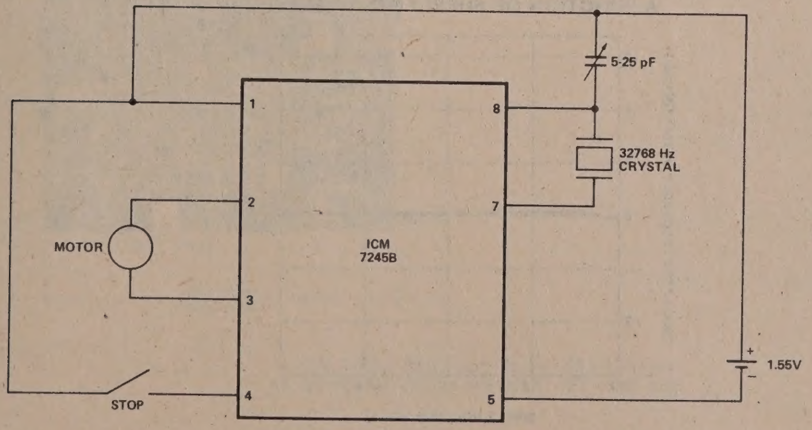
TYPICAL OPERATING CHARACTERISTICS

$V^+ - V^- = 1.55V$, $f_{osc} = 32{,}768$ Hz, circuit in Figure 1, $T_A = 25°C$, unless otherwise stated. Numbers are in absolute values.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	I^+	No Load		0.4	0.8	μA
Operating Voltage	$V^+ - V^-$	0°C < T_A < 50°C	1.2		1.8	V
Oscillator Transconductance	g_m	Start-up	15			μmho
Oscillator Capacitance	C_{OSC}		16	20	24	pF
STOP Input Current	I_{STOP}				0.3	μA
TEST Input Current	I_{TEST}				10	μA
Oscillator Stability	f_{STAB}	$\Delta(V^+ - V^-) = 0.6V$		0.1		ppm
Supply Current During Stop	I^+	'STOP' Connected to V^+			1.0	μA
Output Saturation Resistance	R_O	Bipolar (N-CH. + P-CH) $I_L = 1$ mA			200	Ω
Output Saturation Resistance P-CH	R_{O-P}	Unipolar $I_L = 3$ mA			200	Ω
Output Saturation Resistance N-CH	R_{O-N}	Unipolar $I_L = 3$ mA			50	Ω

7

TYPICAL WATCH CIRCUIT

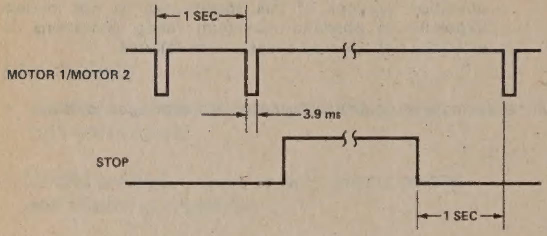


CRYSTAL PARAMETERS
f = 32768 Hz
C_L = 10 pF
C_M = 2.5 mpF
R_S = 20KΩ

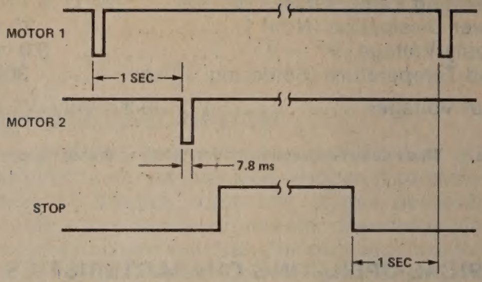
Figure 1.

WAVEFORMS

(ICM7245U)

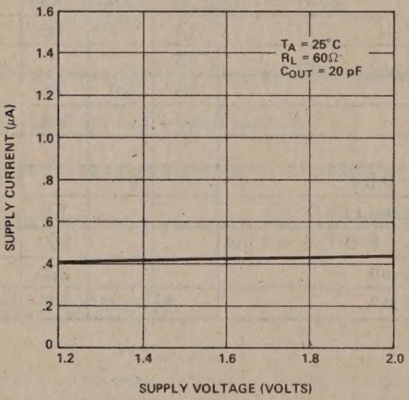

1 SEC
MOTOR 1/MOTOR 2
3.9 ms
STOP
1 SEC

(ICM7245B)

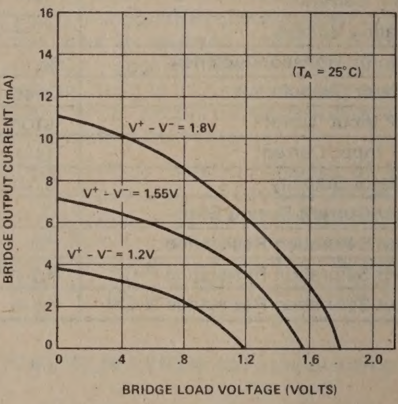

MOTOR 1
1 SEC
MOTOR 2
7.8 ms
STOP
1 SEC

TYPICAL OPERATING CHARACTERISTICS

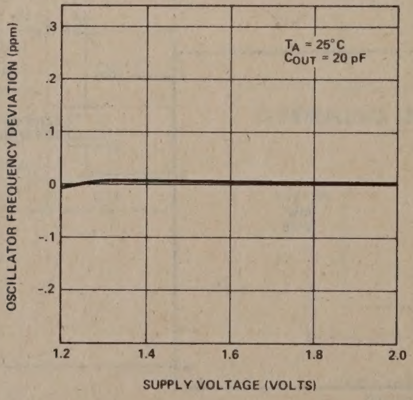
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



BRIDGE OUTPUT CURRENT AS A FUNCTION OF LOAD VOLTAGE



OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



APPLICATION NOTES

OSCILLATOR

The oscillator of the ICM7245 is designed for low frequency operation at very low current from a 1.55 volt supply. The oscillator is of the inverter type, using a non-linear feedback resistor having maximum resistance under start-up conditions. The nominal load capacitance of the crystal should be less than 12 pF, with a preferred range of 7-10 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance must be compatible with the characteristics of the circuit to insure start-up and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)}\ ; \ C_L = \frac{C_{IN}\,C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for start-up

$$g_m = 4\pi^2 f^2 C_{IN}\,C_{OUT}\,R_S\left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance
C_m = Motional Capacitance of Crystal

The g_m required for start-up calculated should not exceed 50% of the g_m guaranteed for the device.

TEST POINT

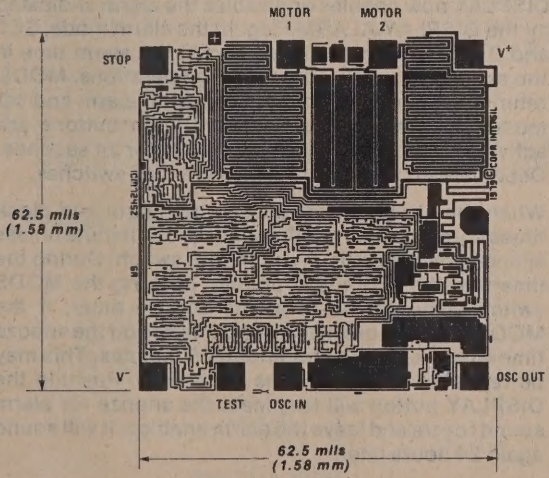
The TEST input, when connected to V⁻, causes the ICM7245B/U to speed-up the outputs by 16 times. On long period output versions (12, 20, 60 sec) the speed-up factor will be larger. This allows easy testing of the finished watch module. The pulse width is not affected by the speed-up of the pulse frequency.

CUSTOM VERSIONS

The ICM7245 may be modified with alternative metal masks to provide different number of dividers, various pulse widths, and different output configurations.

In addition, MOS capacitors on-chip up to a total of 50 pF may be connected to either the input and/or the output of the oscillator. Consult your Intersil representative or the factory for further information.

CHIP TOPOGRAPHY



DIE SIZE = 62.5 x 62.5 MILS (1.58 x 1.58 mm)
BOND PAD SIZE = 5x5 MILS (.127 x .127 mm)

PRELIMINARY
Specifications Subject To Change Without Notice

ICM7271
4-Digit Duplexed LCD Watch Circuit with Snooze Alarm

FEATURES

- **4-digit duplexed display with time, day of week, and alarm flags**
- **4-digit alarm**
- **Direct alarm drive @ 3 volts peak-to-peak with complex alarm tone. Alarm lasts for 1 minute unless silenced with DISPLAY button**
- **Repeatable 5 minute snooze**
- **12/24 hr, month/date reversal bond option**
- **Power ON reset**
- **Display test: All segments ON when DISPLAY and SET are pushed at the same time**
- For NORMAL operation: (All operations begin with RUN display — hours: minutes, day)

Press:		To:
DISPLAY	once	Display month — date day
	again	Display seconds day
	again	Return to hours: minutes day display

- For ALARM operation:

Press:		To:
MODE	once	Display alarm time
SET	once	Set alarm hours*
	again	Set alarm 10 mins.*
	again	Set alarm minutes*
DISPLAY	once	Enable alarm
	again	Disable alarm

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- For SET operation:

Press:		To:
SET	once	Set month*
	again	Set date*
	again	Set day*
	again	Set hours, AM/PM*
	again	Set minutes*
	again	RUN or HOLD (see page 7-64)

*Selected counter advances once with each push of the DISPLAY button or at a 1 Hz rate if it is held down.

ORDERING INFORMATION (Dice Only)

ICM7271/ D
DICE
TYPE

GENERAL DESCRIPTION

The ICM7271 is a fully integrated 4-digit 6 function LCD watch circuit with 24 hour snooze alarm. It is fabricated using Intersil's low threshold metal gate CMOS process and designed to interface with a readily available 4-digit duplexed LCD display. The oscillator, frequency dividers, alarm register, segment decoders, voltage multiplier, alarm and segment drivers are all incorporated on chip. The only additional components required for a complete watch are a 32 KHz quartz crystal, a trimming capacitor, 2 multiplier capacitors, a 3 Volt, 2:1 Multiplexed Liquid Crystal Display, an alarm transducer, 3 SPST switches and a 1.5V battery.

The circuit divides the oscillator frequency in 15 binary stages to 1 Hz. The intermediate frequencies are used to drive the voltage multiplier (512 Hz) and to provide AC drive to the display (32 Hz). The 1 Hz signal is divided down further in the seconds, minutes, hours, day, date and month counters. A four year perpetual calendar is provided.

In the SET modes, the counter being set is displayed and flashed at a 1 Hz rate. Advancing the counters occurs with each push of DISPLAY or at 1 Hz if DISPLAY is held down.

Alarm operation is very convenient. Activating the MODE button puts the circuit in the alarm mode. DISPLAY now enables or disables the alarm, indicated by the DISPLAY ALARM Flag. In the alarm mode, SET and DISPLAY control the setting of the alarm time in the same way as the other setting operations, MODE returns the circuit to normal time. Both alarm and set modes have a time-out function; if no buttons are activated, the circuit returns to Run after 24 seconds. Debounce up to 60 ms is provided on all switches.

When the alarm is enabled and the alarm and clock times agree, the alarm will sound for one minute unless silenced by the DISPLAY or MODE switch. During the time that the alarm is sounding, pushing the MODE switch activates the 5 minute snooze timer; if the MODE switch is pressed during this period the snooze time will be extended for another 5 minutes. This may be repeated as many times as desired. Pushing the DISPLAY button will terminate the snooze (or alarm sound) cycle and leave the alarm enabled; it will sound again 24 hours later.

The ICM7271 is designed to be mounted on the top of the substrate (same side as the DISPLAY).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... -55°C to +125°C
Operating Temperature .... -10°C to +60°C
Power Dissipation[1] (Dice Only) .... 100 mW
Supply Voltage[2]
$V^+ - V^-$ 2.7V
$V^+ - V_H$ 5.5V
Input Voltage (Osc. In, Test,
Set, Display) .... $V^- \leq V_{IN} \leq V^+$
Output Voltage (Osc Out) ...... $V^- \leq V_{OUT} \leq V^+$
(All Other Pins) .... $V_2^- \leq V_{OUT} \leq V^+$

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. The ICM7271 is fully short circuit protected on all inputs and outputs. However, if by biasing an input or output the device is put into a latchup condition, power dissipation must be limited to 100 mW to prevent destruction of the device.
2. The ICM7271 is intended for use with two power supplies, one of which is derived from an external battery (V^-) and the other is generated internally by the voltage multiplier (V_2^-). The common point of the two supplies is the most positive, V^+. If desired the circuit can be supplied with an external V_2^- by disconnecting the multiplier capacitors.

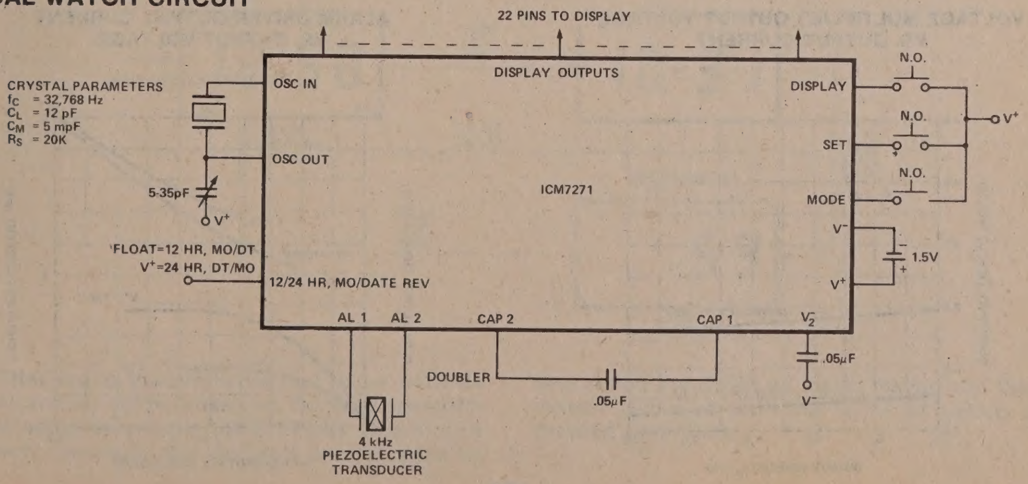
OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ - V^- = 1.55V$, Voltage Doubler Connected, $T_A = 25°C$ Unless Otherwise Specified. Voltages Specified in Absolute Value.

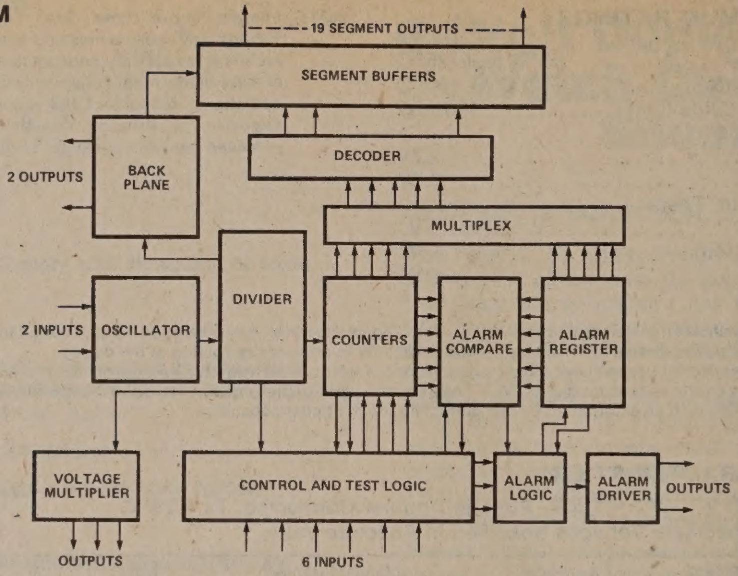
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V^+	$V^- = 0V$ $-10°C < T_A < 60°C$	1.2		1.8	Volts
Supply Current	I^+	Display Disconnected		1.5	3.0	μA
Doubler Output Voltage	V_2^-	$I_H = 0.0\ \mu A$	3.0	3.1		Volts
		$I_H = 1.0\ \mu A$	2.9	3.0		
Segment Drive Current	I_{SEG}	$V_{SAT} = 0.2V$ (Both Directions)	5			μA
Backplane Drive Current	I_{BP}	$V_{SAT} = 0.1V$ (Both Directions)	10			μA
Switch Actuation Current	I_{SW}	$V_{SW} = V^+$		10		μA
Alarm Saturation Resistance	$R_{AL(ON)}$	N-ch and P-ch (Series) at 1mA			600	ohms
Oscillator Stability	f_{STAB}	$V^- = 0V$, $1.20V \leq V^+ \leq 1.55V$, $C_{OUT} = 25\ pF$		2		PPM
Oscillator Input Current[3]	I_{OSCI}	'OSC IN' Connected to V^+ 'OSC OUT' Open Circuit		0.2		μA
Oscillator Input Capacitance	C_{IN}		20	25	30	pF
Oscillator Transconductance	g_m		10	15		μmho

3. The integrated oscillator biasing component has a nonlinear characteristic depending on the instantaneous values of the input and output voltages of the oscillator and the supply. Under oscillator startup conditions this component has a maximum value.

TYPICAL WATCH CIRCUIT

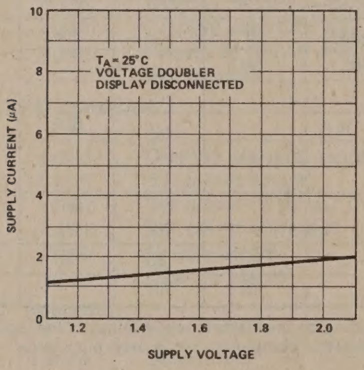

22 PINS TO DISPLAY
DISPLAY OUTPUTS
CRYSTAL PARAMETERS
f_C = 32,768 Hz
C_L = 12 pF
C_M = 5 mpF
R_S = 20K
OSC IN
OSC OUT
5-35pF
V+
'FLOAT=12 HR, MO/DT
V+=24 HR, DT/MO
12/24 HR, MO/DATE REV
ICM7271
DISPLAY
SET
MODE
N.O.
N.O.
N.O.
V+
V-
V+
1.5V
AL 1
AL 2
CAP 2
CAP 1
V_2^-
.05μF
V-
DOUBLER
.05μF
4 kHz
PIEZOELECTRIC
TRANSDUCER

BLOCK DIAGRAM

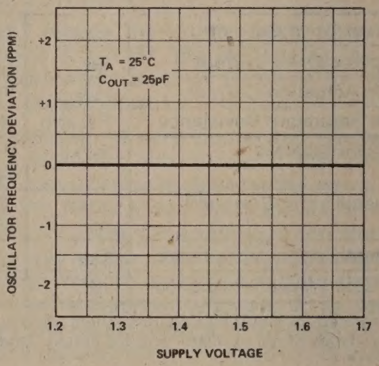

19 SEGMENT OUTPUTS
SEGMENT BUFFERS
BACK PLANE
2 OUTPUTS
DECODER
MULTIPLEX
2 INPUTS
OSCILLATOR
DIVIDER
COUNTERS
ALARM COMPARE
ALARM REGISTER
VOLTAGE MULTIPLIER
CONTROL AND TEST LOGIC
ALARM LOGIC
ALARM DRIVER
OUTPUTS
OUTPUTS
6 INPUTS

TYPICAL PERFORMANCE CHARACTERISTICS

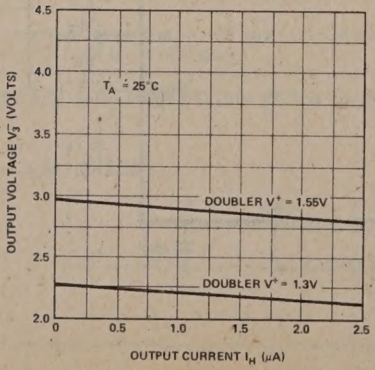
SUPPLY CURRENT VS. SUPPLY VOLTAGE



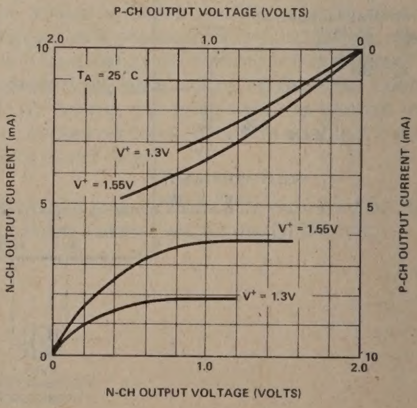
OSCILLATOR STABILITY VS. SUPPLY VOLTAGE



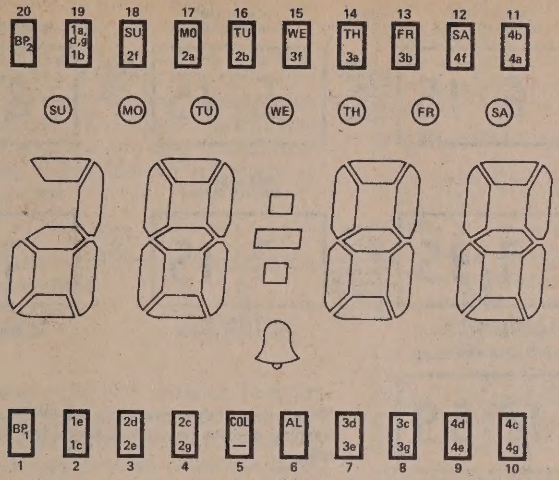
VOLTAGE MULTIPLIER OUTPUT VOLTAGE VS. OUTPUT CURRENT



ALARM DRIVER OUTPUT CURRENT VS. OUTPUT VOLTAGE



DUPLEXED 4 DIGIT LCD DISPLAY *


20
19
18
17
16
15
14
13
12
11
BP2
1a, d,g 1b
SU 2f
MO 2a
TU 2b
WE 3f
TH 3a
FR 3b
SA 4f
4b 4a
SU
MO
TU
WE
TH
FR
SA
BP1
1e 1c
2d 2e
2c 2g
COL —
AL
3d 3e
3c 3g
4d 4e
4c 4g
1
2
3
4
5
6
7
8
9
10

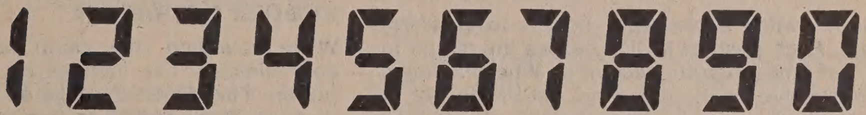
*Typical displays include

LADCOR	LAD-122
Fairchild	FLM-4005-01
BBC	LC1612XX LC2013XX

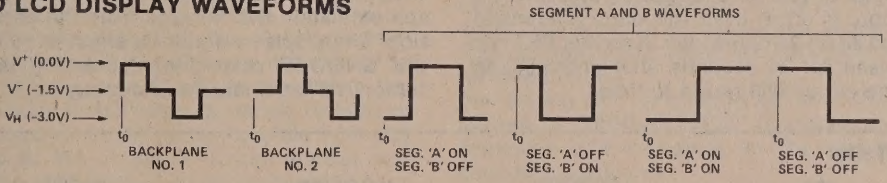
NOTE: UPPER SEGMENTS CONTROLLED BY BP_2.
LOWER SEGMENTS CONTROLLED BY BP_1.

DISPLAY FONT

NUMBERS

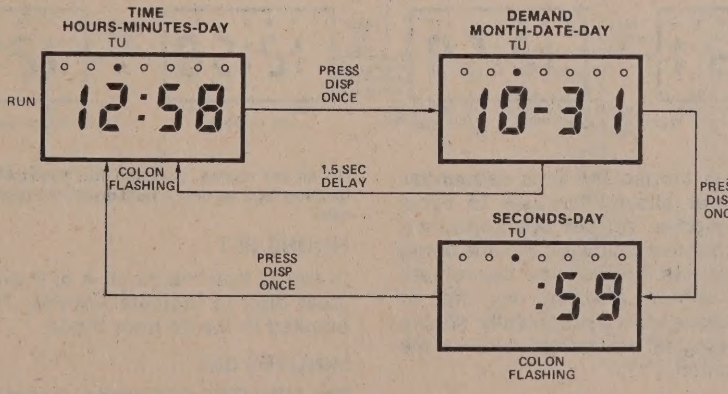


DUPLEXED LCD DISPLAY WAVEFORMS


SEGMENT A AND B WAVEFORMS
V+ (0.0V)
V− (-1.5V)
VH (-3.0V)
t0
BACKPLANE NO. 1
BACKPLANE NO. 2
SEG. 'A' ON SEG. 'B' OFF
SEG. 'A' OFF SEG. 'B' ON
SEG. 'A' ON SEG. 'B' ON
SEG. 'A' OFF SEG. 'B' OFF

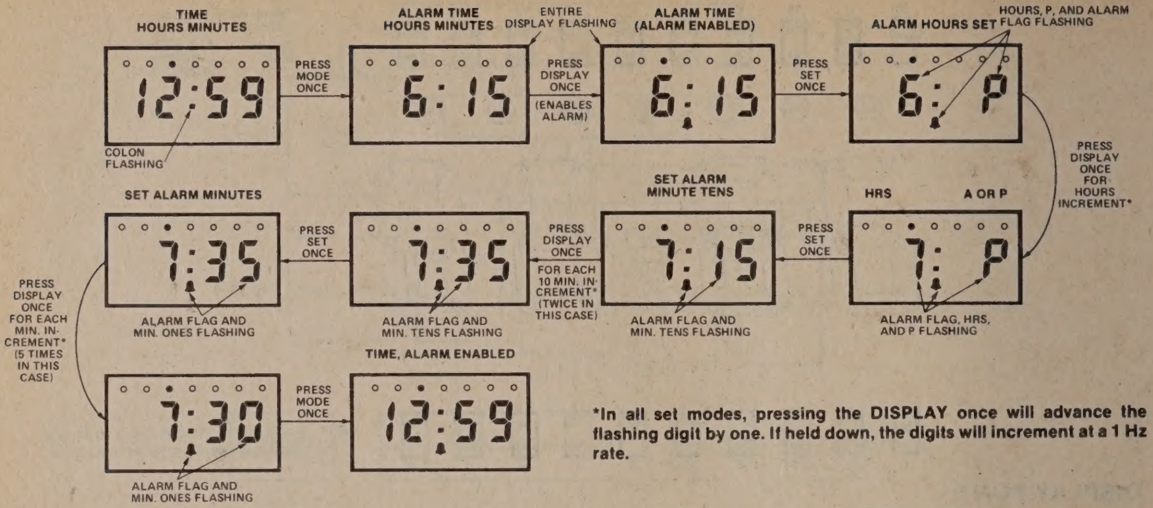
$$V_{rms}\text{ ON (ON SEG. VOLTS)} = \frac{1}{\sqrt{2}}\sqrt{(V^+)^2 + \left(\frac{V^+}{2}\right)^2} = \frac{\sqrt{5}V^+}{2\sqrt{2}};\quad V_{rms}\text{ OFF (OFF SEG. VOLTS)} = \frac{1}{\sqrt{2}}\sqrt{0 + \left(\frac{V^+}{2}\right)^2} = \frac{V^+}{2\sqrt{2}};\quad \text{ON : OFF} = \sqrt{5} : 1 \cong 2.3 : 1$$

NORMAL WATCH OPERATION


TIME
HOURS-MINUTES-DAY
TU
RUN
12:58
COLON FLASHING
PRESS DISP ONCE
DEMAND
MONTH-DATE-DAY
TU
10-31
1.5 SEC DELAY
PRESS DISP ONCE
SECONDS-DAY
TU
:59
PRESS DISP ONCE
COLON FLASHING

In the TIME mode, the circuit displays hours, minutes and day, and the colon is flashing. Demand operation is actuated by depressing the DISPLAY switch once for month, date, and day. Seconds are displayed by depressing the DISPLAY switch twice, and they will remain displayed until the DISPLAY switch is depressed a third time.

ALARM OPERATION


TIME
HOURS MINUTES
12:59
COLON FLASHING
PRESS MODE ONCE
ALARM TIME
HOURS MINUTES
6:15
ENTIRE DISPLAY FLASHING
PRESS DISPLAY ONCE (ENABLES ALARM)
ALARM TIME (ALARM ENABLED)
6:15
PRESS SET ONCE
ALARM HOURS SET
HOURS, P, AND ALARM FLAG FLASHING
6: P
PRESS DISPLAY ONCE FOR HOURS INCREMENT*
HRS
A OR P
7: P
ALARM FLAG, HRS, AND P FLASHING
PRESS SET ONCE
SET ALARM MINUTE TENS
7:15
ALARM FLAG AND MIN. TENS FLASHING
PRESS DISPLAY ONCE FOR EACH 10 MIN. INCREMENT* (TWICE IN THIS CASE)
7:35
ALARM FLAG AND MIN. TENS FLASHING
PRESS SET ONCE
SET ALARM MINUTES
7:35
ALARM FLAG AND MIN. ONES FLASHING
PRESS DISPLAY ONCE FOR EACH MIN. INCREMENT* (5 TIMES IN THIS CASE)
7:30
ALARM FLAG AND MIN. ONES FLASHING
PRESS MODE ONCE
TIME, ALARM ENABLED
12:59

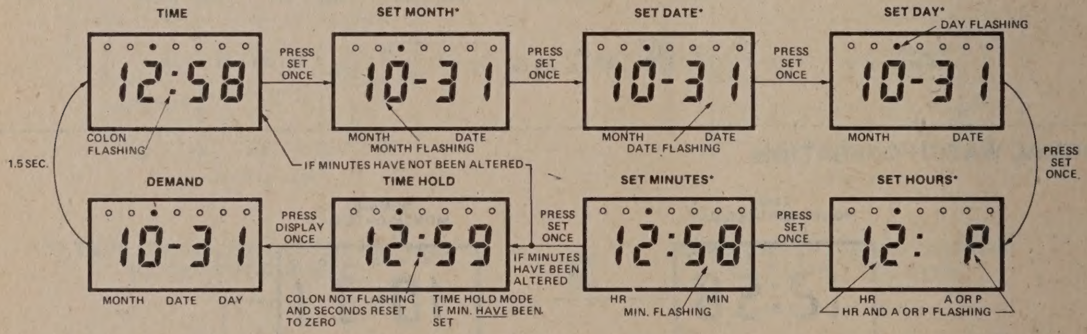
*In all set modes, pressing the DISPLAY once will advance the flashing digit by one. If held down, the digits will increment at a 1 Hz rate.

The mode switch allows easy access to all alarm functions. Each push of MODE causes the circuit to switch from time to alarm or vice versa. When the watch time equals the alarm (including AM/PM for 12 hr mode) the alarm will sound. The alarm will silence itself after one minute, or can be silenced by pressing the DISPLAY button. In either case, the alarm will remain armed to sound again 24 hours later. If neither SET nor DISPLAY is used for 24 seconds after entering the alarm mode the circuit will return to time.

SNOOZE OPERATION

While sounding, the alarm may be silenced for approximately five minutes by pressing the MODE button. This 'SNOOZE' may be repeated as often as desired. If the MODE button is pressed during the 'SNOOZE' time the alarm will be silenced for approximately five minutes from the second depression. The display will not be affected by activation of the 'SNOOZE' operation; depressing the DISPLAY button will terminate the snooze cycle.

SET OPERATION


TIME
12:58
COLON FLASHING
PRESS SET ONCE
SET MONTH*
10-31
MONTH
DATE
MONTH FLASHING
PRESS SET ONCE
SET DATE*
10-31
MONTH
DATE
DATE FLASHING
PRESS SET ONCE
SET DAY*
DAY FLASHING
10-31
MONTH
DATE
PRESS SET ONCE
SET HOURS*
12: P
HR
A OR P
HR AND A OR P FLASHING
PRESS SET ONCE
SET MINUTES*
12:58
HR
MIN
MIN. FLASHING
PRESS SET ONCE
IF MINUTES HAVE BEEN ALTERED
IF MINUTES HAVE NOT BEEN ALTERED
TIME HOLD
12:59
TIME HOLD MODE IF MIN. HAVE BEEN SET
COLON NOT FLASHING AND SECONDS RESET TO ZERO
PRESS DISPLAY ONCE
DEMAND
10-31
MONTH
DATE
DAY
1.5 SEC.

Setting the ICM7271 is carried out in a sequential manner. The SET input allows the user to cycle through the five set modes. All set operations are independent, i.e. the counters following the one being set are inhibited; this allows, for instance, convenient time zone adjustment without affecting day, date or month. The setting sequence is graphically shown above. The counters being set are flashed at a 1 Hz rate for easy user identification.

DATE SET

The perpetual calendar uses 28 days for February. In a leap year, on February 29, the watch will display March 1. To display February 29, change date to 29 first, then March to February.

*In all set modes, pressing the DISPLAY once will advance the flashing digit by one. If held down, the digits will increment at a 1 Hz rate.

HOURS SET

In the 12 hour mode an A or P will appear in the right most digit to indicate AM/PM. These characters are blanked in the 24 hour mode.

MINUTES SET

The MINUTES SET mode is used for exact synchronization of the watch as well as for setting the minutes. If the DISPLAY switch is not activated during MINUTES SET, neither seconds nor minutes will be affected and the next activation of the SET switch will return the circuit to normal time. If DISPLAY is used in the

MINUTES SET mode the minutes will advance and the seconds will reset to 00 and be put on hold. The user now advances to the next minute and pushes SET once. The circuit is now in TIME HOLD. The DISPLAY will show hours, minutes, day, and the colon will be on (not flashing). At the tone of the time signal, push DISPLAY. This will cause the watch to display month/date/day for 1.5 seconds and return to normal (running) (time) display. Time setting accuracy is approximately 0.1 seconds.

SET MODE TIME-OUT

If neither SET nor DISPLAY is used for 24 seconds the circuit will return to normal time.

APPLICATION NOTES

ALARM DRIVE

The ICM7271/M provides sufficient drive current for normal use with a 4 KHz piezoelectric transducer, provided the transducer is properly mounted. For increased drive, a 5 mH coil and an external NPN transistor are required. Refer to the Application Note A031, "ICM7220A Coil Driven Alarm Design," for details.

OSCILLATOR

The oscillator of the ICM7271/M is designed for low frequency operation from a 1.55 volt supply at very low currents. The oscillator is of the inverter type with a non-linear feedback resistor which has a maximum resistance under startup conditions included on chip. The nominal load capacitance of the crystal should be less than 15 pF, typically 12 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance must be compatible with the characteristics of the circuit to insure startup and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)};\quad C_L = \frac{C_{IN}\,C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for startup

$$g_m = 4\pi^2 f^2\, C_{IN}\, C_{OUT}\, R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

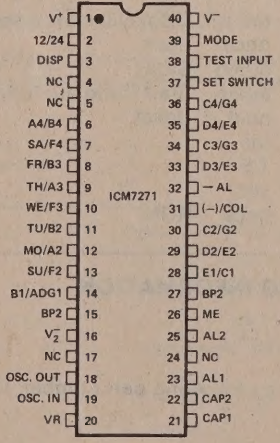
R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance
C_m = Motional Capacitance of Crystal

The g_m required for startup calculated should not exceed 50% of the g_m guaranteed for the device.

TEST POINT AND DISPLAY TEST

The circuit is reset to a known state by connecting SET, DISPLAY, and TEST to V^+. This state is Saturday December 1, 12:00 am (or 00:00), with alarm at 12:00 am (or 00:00) and disabled. When powering up the device, it will also reset to this state. The TEST input, when connected to V^+ causes the circuit to speed up the seconds by 512 times. The date-month carry is not inhibited during connecting SET and DISPLAY to V^+ the circuit will provide a DISPLAY TEST function, turning on all segments and indicators on the display as well as sounding the alarm.

PIN CONFIGURATION



ICM7272
4-Digit Duplexed LCD Chronograph Watch Circuit

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

- **4-digit duplexed display with time, day of week, date and chrono flags**
- **Full 30 minute chronograph: minutes, seconds, tenths. Tenths of seconds are displayed in dynamic bargraph**
- **MODE button allows switching between watch and chronograph without affecting chrono function**
- **12/24 hour, month/date reversal bond option**
- **Display test: All segments and flags ON when DISP and SET are pushed at the same time**
- **Power ON reset**
- For NORMAL operation: (All operations begin with RUN display — hours: minutes, day)

Press:		To:
DISPLAY	once	Display month — date day

- For SET operation:

Press:		To:
SET	once	Set month*
	again	Set date*
	again	Set day*
	again	Set hours*
	again	Set minutes*
	again	RUN or HOLD

*Selected counter advances once with each push of the DISPLAY button or at a 1Hz rate if it is held down.

- For chronograph operation

Press:		To:
MODE	once	Display minutes: seconds, tenths
DISPLAY	once	Start
	again	Stop
	again	Start (time out function)
DISPLAY	hold for 1.5 sec.	Reset
MODE	once	RUN

ORDERING INFORMATION

Order dice by following part number: ICM7272D

Note: For evaluation only the ICM7272 is available in a 40 pin ceramic DIP with 0.1" pin-to-pin and 0.6" row-to-row spacing. Order part number: ICM7272IDL

GENERAL DESCRIPTION

The ICM7272 is a fully integrated 4-digit 6-function LCD watch circuit with a 30 minute, tenth second chronograph, and designed to interface with readily available 4-digit duplexed displays. The oscillator, frequency dividers, voltage multiplier, and segment drivers are all incorporated on chip. The only additional components required for a complete watch are a 32 kHz crystal, one trimming capacitor, two multiplier capacitors, a duplexed LCD display, three SPST switches and a 1.5V battery.

Chronograph operation has been optimized for short as well as long interval timing. Tenths of seconds are displayed in a dynamic bargraph across the top of the display, while seconds and minutes are displayed in the 4-seven segment digits. 30 minutes is automatically converted to 00:00.0.

The MODE button allows alternating between watch and chrono at any time; in the CHRONO mode, the DISPLAY switch acts as the START/STOP/RESET. In TIME SET mode, if no buttons are pushed for 24 seconds the circuit returns to RUN. 60 ms of switch debounce is provided on all switch inputs.

The ICM7272 is fabricated using Intersil's low threshold metal gate CMOS process, and is designed for mounting on the same side of the substrate as the display.

PIN CONFIGURATION

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-55°C to +125°C
Operating Temperature	-20°C to +85°C
Power Dissipation[1] (Dice Only)	100 mW
Supply Voltage[2]	
$V^+ - V^-$	2.0V
$V^+ - V_2^-$	5.5V
Input Voltage (Osc. In, Test, Set, Display)	$V^- \leq V_{IN} \leq V^+$
Output Voltage (Osc Out)	$V^- \leq V_{OUT} \leq V^+$
(All Other Pins)	$V_2^- \leq V_{OUT} \leq V^+$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. The ICM7272 is fully short circuit protected on all inputs and outputs. However, if by biasing an input or output the device is put into a latchup condition, power dissipation must be limited to 100 mW to prevent destruction of the device.
2. The ICM7272 is intended for use with two power supplies, one of which is derived from an external battery (V^-) and the other is generated internally by the voltage multiplier(V_2^-). The common point of the two supplies is the most positive, V^+. If desired the circuit can be supplied with an external V_2^- by disconnecting the multiplier capacitors.

OPERATING CHARACTERISTICS

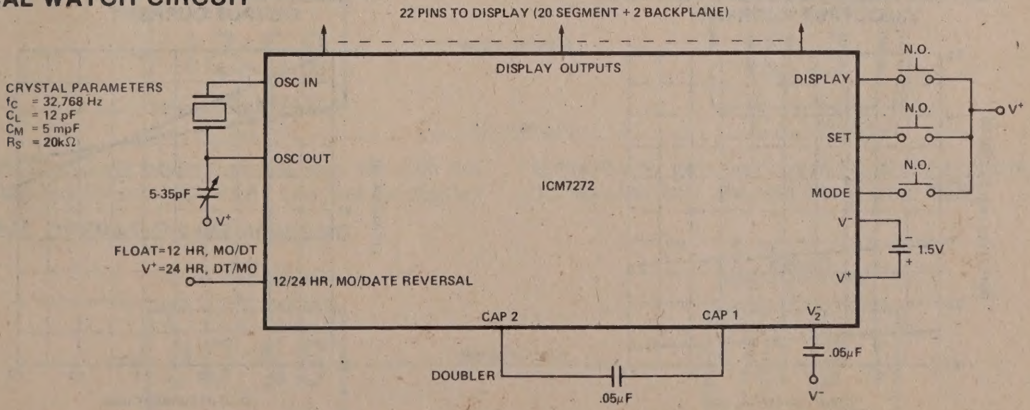
TEST CONDITIONS: $V^+ - V^- = 1.55V$, Voltage Doubler Connected, $T_A = 25°C$, unless otherwise stated. Voltages Specified in Absolute Value.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V^+	$V^- = 0V$ $-10°C < T_A < 60°C$	1.2		1.8	Volts
Supply Current	I^+	Display Disconnected		1.5	3.0	μA
Doubler Output Voltage	V_2^-	$I_H = 0.0\ \mu A$	3.0	3.1		Volts
		$I_H = 1.0\ \mu A$	2.9	3.0		
Segment Drive Current	I_{SEG}	$V_{SAT} = 0.2V$ (Both Directions)	5			μA
Backplane Drive Current	I_{BP}	$V_{SAT} = 0.1V$ (Both Directions)	10			μA
Switch Actuation Current	I_{SW}	$V_{SW} = V^+$		10		μA
Alarm Saturation Resistance	$R_{AL(ON)}$	N-ch and P-ch (Series) at 1mA			600	ohms
Oscillator Stability	f_{STAB}	$V^- = 0V$, $1.3V \leq V^+ \leq 1.55V$, $C_{OUT} = 25\ pF$		0.1		PPM
Oscillator Input Current[3]	I_{OSCI}	'OSC IN' Connected to V^+ 'OSC OUT' Open Circuit		0.2		μA
Oscillator Input Capacitance	C_{IN}		20	25	30	pF
Oscillator Transconductance	g_m		10	15		μmho

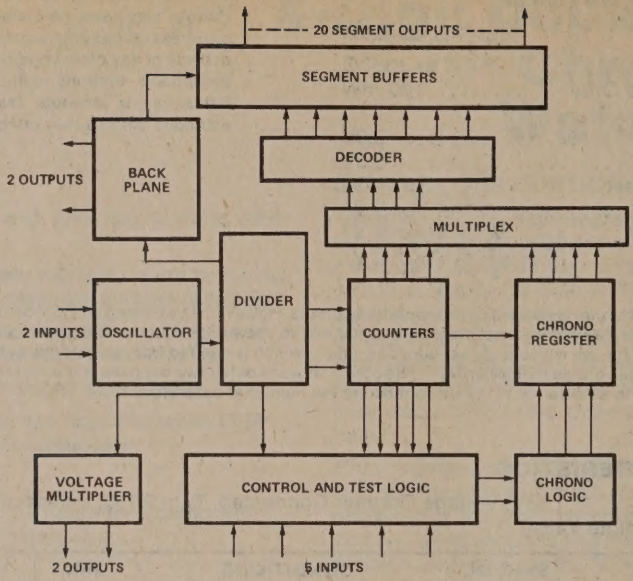
Notes:

3. The integrated oscillator biasing component has a nonlinear characteristic depending on the instantaneous values of the input and output voltages of the oscillator and the supply. Under oscillator startup conditions this component has a maximum value.

TYPICAL WATCH CIRCUIT

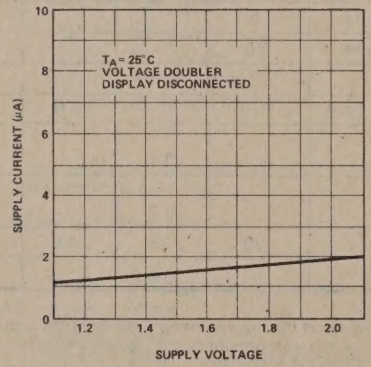


BLOCK DIAGRAM

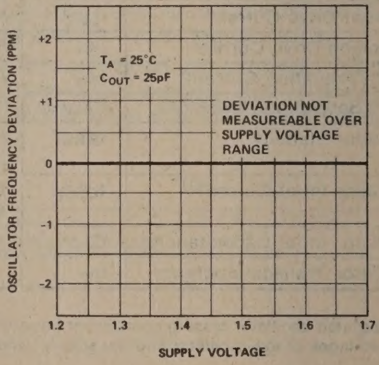

20 SEGMENT OUTPUTS
SEGMENT BUFFERS
DECODER
2 OUTPUTS
BACK PLANE
MULTIPLEX
DIVIDER
2 INPUTS
OSCILLATOR
COUNTERS
CHRONO REGISTER
VOLTAGE MULTIPLIER
CONTROL AND TEST LOGIC
CHRONO LOGIC
2 OUTPUTS
5 INPUTS

TYPICAL PERFORMANCE CHARACTERISTICS

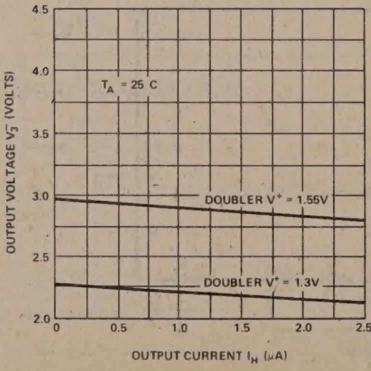
SUPPLY CURRENT VS. SUPPLY VOLTAGE



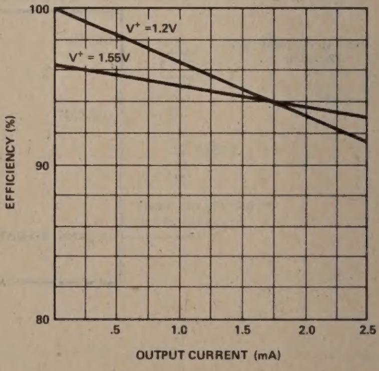
OSCILLATOR STABILITY VS. SUPPLY VOLTAGE



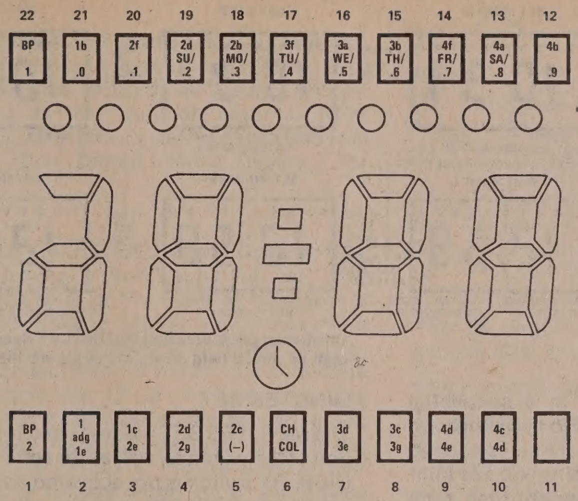
VOLTAGE DOUBLER OUTPUT VOLTAGE VS. OUTPUT CURRENT



VOLTAGE DOUBLER EFFICIENCY VS. OUTPUT CURRENT



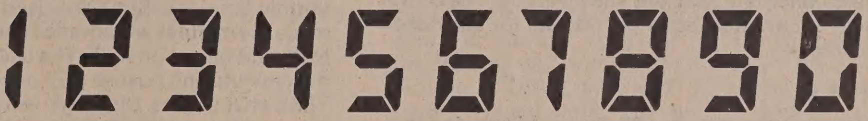
DUPLEXED CHRONO WATCH DISPLAY


22
BP 1
21
1b .0
20
2f .1
19
2d SU/ .2
18
2b MO/ .3
17
3f TU/ .4
16
3a WE/ .5
15
3b TH/ .6
14
4f FR/ .7
13
4a SA/ .8
12
4b .9
BP 2
1
1 adg 1e
2
1c 2e
3
2d 2g
4
2c (–)
5
CH COL
6
3d 3e
7
3c 3g
8
4d 4e
9
4c 4d
10
11

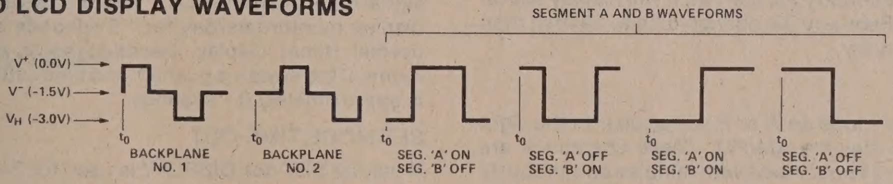
NOTE: UPPER SEGMENTS CONTROLLED BY BP_2.
LOWER SEGMENTS CONTROLLED BY BP_1.

DISPLAY FONT

NUMBERS

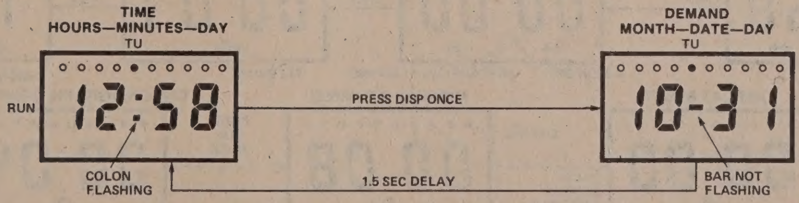


DUPLEXED LCD DISPLAY WAVEFORMS



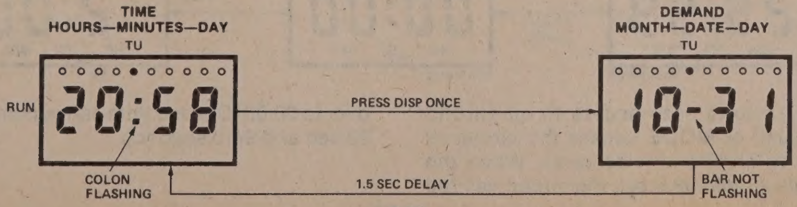
$$V_{rms}\ \text{ON (ON SEG. VOLTS)} = \frac{1}{\sqrt{2}}\sqrt{(V^+)^2+\left(\frac{V^+}{2}\right)^2} = \frac{\sqrt{5}V^+}{2\sqrt{2}};\quad V_{rms}\ \text{OFF (OFF SEG. VOLTS)} = \frac{1}{\sqrt{2}}\sqrt{0+\left(\frac{V^+}{2}\right)^2} = \frac{V^+}{2\sqrt{2}};\quad \text{ON : OFF} = \sqrt{5} : 1 \simeq 2.3 : 1$$

NORMAL WATCH OPERATION (12 Hr option)

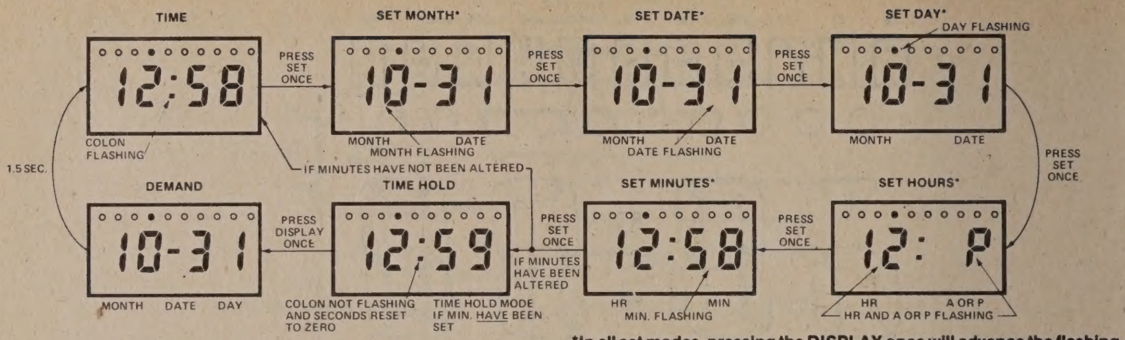

TIME
HOURS—MINUTES—DAY
TU
RUN
12:58
COLON FLASHING
PRESS DISP ONCE
1.5 SEC DELAY
DEMAND
MONTH—DATE—DAY
TU
10-31
BAR NOT FLASHING

The circuit displays hours, minutes and day with the colon flashing. Pressing DISPLAY switches the display to the month, date, and day mode with the date flag on. 1.5 seconds later, the circuit returns to TIME.

NORMAL OPERATION (24 Hr option)


TIME
HOURS—MINUTES—DAY
TU
RUN
20:58
COLON FLASHING
PRESS DISP ONCE
1.5 SEC DELAY
DEMAND
MONTH—DATE—DAY
TU
10-31
BAR NOT FLASHING

SET OPERATION


TIME
12:58
COLON FLASHING
PRESS SET ONCE
SET MONTH*
10-31
MONTH
DATE
MONTH FLASHING
PRESS SET ONCE
SET DATE*
10-31
MONTH
DATE
DATE FLASHING
PRESS SET ONCE
SET DAY*
DAY FLASHING
10-31
MONTH
DATE
PRESS SET ONCE
SET HOURS*
12: P
HR
A OR P
HR AND A OR P FLASHING
PRESS SET ONCE
SET MINUTES*
12:58
HR
MIN
MIN. FLASHING
PRESS SET ONCE
IF MINUTES HAVE BEEN ALTERED
IF MINUTES HAVE NOT BEEN ALTERED
TIME HOLD
12:59
COLON NOT FLASHING AND SECONDS RESET TO ZERO
TIME HOLD MODE IF MIN. HAVE BEEN SET
PRESS DISPLAY ONCE
DEMAND
10-31
MONTH
DATE
DAY
1.5 SEC.

***In all set modes, pressing the DISPLAY once will advance the flashing digit by one. If held down, the digits will increment at a 1 Hz rate.**

Setting the ICM7272 is carried out in a sequential manner. The SET input allows the user to cycle through the five set modes. All set operations are independent, i.e. the counters following the one being set are inhibited; this allows, for instance, convenient time zone adjustment without affecting day, date or month. The setting sequence is graphically shown above. The counters being set are flashed at a 1 Hz rate for easy user identification.

DATE SET

The perpetual calendar uses 28 days for February. In a leap year, on February 29, the watch will display March 1. To display February 29, change date to 29 first, then March to February.

HOURS SET

In the 12 hour mode an A or P will appear in the right most digit to indicate AM/PM. These characters are blanked in the 24 hour mode, with minutes continuously displayed.

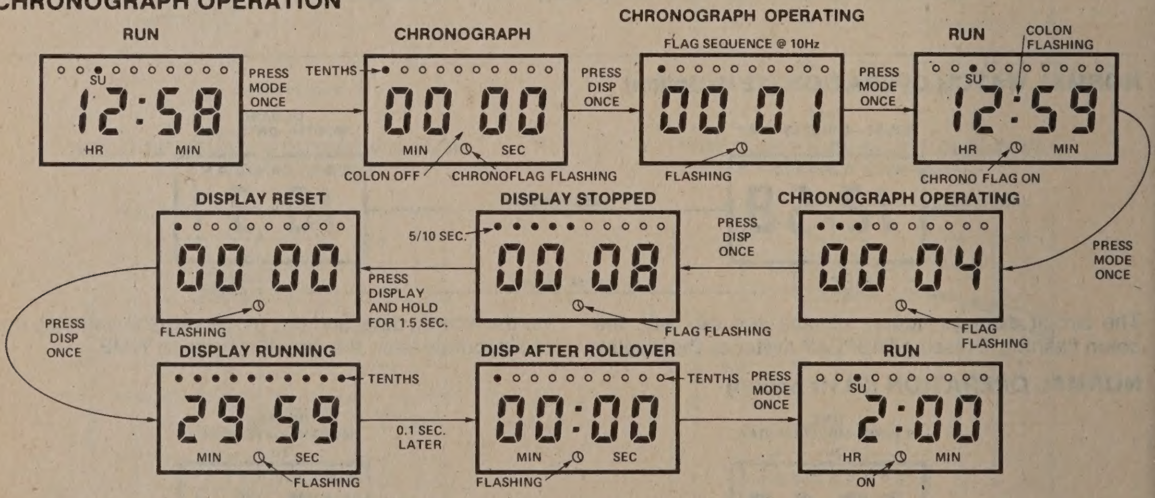
MINUTES SET

The MINUTES SET mode is used for exact synchronization of the watch as well as for setting the minutes. If the DISPLAY switch is not activated during MINUTES SET, neither seconds nor minutes will be affected and the next activation of the SET switch will return the circuit to normal time. If DISPLAY is used in the MINUTES SET mode the minutes will advance and the seconds will reset to 00 and be put on hold. The user now advances to the next minute and pushes SET once. The circuit is now in TIME HOLD. The DISPLAY will show hours, minutes, day, and the colon will be on (not flashing). At the time signal tone, push DISPLAY. This will cause the watch to display month/date/day for 1.5 seconds and return to normal (time) display. Seconds begin counting the moment the switch is pushed, and time setting accuracy is approximately 0.1 seconds.

SET MODE TIME-OUT

If neither SET nor DISPLAY is used for 24 seconds the circuit will return to normal time.

CHRONOGRAPH OPERATION


RUN
SU
12:58
HR
MIN
PRESS MODE ONCE
CHRONOGRAPH
TENTHS
00 00
MIN
SEC
COLON OFF
CHRONOFLAG FLASHING
PRESS DISP ONCE
CHRONOGRAPH OPERATING
FLAG SEQUENCE @ 10Hz
00 01
FLASHING
PRESS MODE ONCE
RUN
COLON FLASHING
SU
12:59
HR
MIN
CHRONO FLAG ON
PRESS MODE ONCE
CHRONOGRAPH OPERATING
00 04
FLAG FLASHING
PRESS DISP ONCE
DISPLAY STOPPED
5/10 SEC.
00 08
FLAG FLASHING
PRESS DISPLAY AND HOLD FOR 1.5 SEC.
DISPLAY RESET
00 00
FLASHING
PRESS DISP ONCE
DISPLAY RUNNING
TENTHS
29 59
MIN
SEC
FLASHING
0.1 SEC. LATER
DISP AFTER ROLLOVER
TENTHS
00:00
MIN
SEC
FLASHING
PRESS MODE ONCE
RUN
SU
2:00
HR
MIN
ON

The MODE switch allows easy access to all chrono functions. Each push of MODE causes the circuit to switch from time to chrono or vice versa. When the chrono time equals 29 min 59.9 sec the circuit will roll over to 00:00. Chrono time can accumulate up to 29 min 59 sec and 9/10 seconds.

APPLICATION NOTES

ALARM DRIVE

The ICM7272 provides sufficient drive current for normal use with a 4 KHz piezoelectric transducer, provided the transducer is properly mounted. For increased drive, a 5 mH coil and an external NPN transistor are required. Refer to the Application Note A031, "ICM7220A Coil Driven Alarm Design," for details.

OSCILLATOR

The oscillator of the ICM7272 is designed for low frequency operation from a 1.55 volt supply at very low currents. The oscillator is of the inverter type with a non-linear feedback resistor which has a maximum resistance under startup conditions included on chip. The nominal load capacitance of the crystal should be less than 15 pF, typically 12 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance must be compatible with the characteristics of the circuit to insure startup and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)}; \quad C_L = \frac{C_{IN} C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for startup

$$g_m = 4\pi^2 f^2 C_{IN} C_{OUT} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance
C_m = Motional Capacitance of Crystal

The g_m required for startup calculated should not exceed 50% of the g_m guaranteed for the device.

TEST POINT AND DISPLAY TEST

The circuit is reset to a known state by connecting SET, DISPLAY, and TEST to V^+. This state is Saturday December 1, 12:00 am (or 00:00), with alarm at 12:00 am (or 00:00) and disabled. When powering up the device, it will also reset to this state. The TEST input, when connected to V^+ causes the circuit to speed up the seconds by 512 times. The date-month carry is not inhibited during date set in the test mode. By connecting SET and DISPLAY to V^+ the circuit will provide a DISPLAY TEST function, turning on all segments and indicators on the display as well as sounding the alarm.

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NMOS

Static RAMs

Organization	Max Access Time (ns)	I_{CC} Max(mA)	No. Pins	Package*	Temp Range*
1024 x 4					
2114/2114L	450	100/70	18	J,P	C,M
2114/3/2114L-3	300	100/70	18	J,P	C,M
2114/2/2114L-2	200	100/70	18	J,P	C,M
2148	70	140	18	J,P	C
2148-3	55	140	18	J	M
M2148	85	180	18	J	M
4096 x 1					
7141/7141L	450	70/50	18	J,P	C,M
7141-3/7141L-3	300	70/50	18	J,P	C,M
7141-2/7141L-2	200	70/50	18	J,P	C,M
2147/2147L	70	160/140	18	J,P	C
2147-3	55	180	18	J,P	C
M2147	85	180	18	J	M

Dynamic RAMs

Organization	Max Access Time (ns)	I_{DD} Max(mA)	No. Pins	Package*	Temp Range*
4096 x 1					
7027-1	120	35	16	J	C
4027-2	150	35	16	J	C
4027-3	200	35	16	J	C
4027-4	250	35	16	J	C

ROMs

Organization	Max Access Time (ns)	I_{DD} Max(mA)	No. Pins	Package*	Temp Range*
1024 x 4					
82HM137	60	120	18	J,P	C
82HM137	80	130	18	J	M
2048 x 4					
82HM185	60	120	18	J,P	C
82HM185	60	130	18	J	M
512 x 8					
82HM141	70	175	24	J,P	C
82HM141	90	185	24	J	M
1024 x 8					
82HM181	70	175	24	J,P	C
82HM181	90	185	24	J	M
2048 x 8					
82HM191	80	175	24	J,P	C
82HM191	100	185	24	J	M
4096 x 8					
IM7332	300	80	24	J,P	C
8192 x 8					
IM7364	350	150	24	J,P	C

*Package and Temperature Key

F—Flatpack
J—Ceramic Dual In-Line
P—Plastic Dual In-Line
D-Ceramic Side Braized (Not Recommended for High Volume),

C—Commercial, 0°C to +70°C
I—Industrial, -40°C to +85°C
M—Military, -55°C to +125°C

CMOS

Static RAMS

Organization	Max Access Time (ns)	Vcc (V)	Icc Max (mA) Operating	Icc Max (μA) Standby	No. Pins	Package*	Temp Range
64 x 12							
IM6512	460	5	—	100	18	J,F	C,I,M
IM6512A	150	10	—	500	18	J,F	I,M
1024 x 1							
IM65X08	250	5	2	10	16	J,F,P	C,I,M
IM65X08A	200	10	10	500	16	J,F,P	I,M
IM65X18	250	5	2	10	18	J,F,P	C,I,M
IM65X18A	200	10	10	500	18	J,F,P	I,M
4096 x 1							
IM6504	300	5	7	50	18	J,P	C,I,M
256 x 4							
IM65X51	300	5	2	10	18	J,P	C,I,M
IM65X51A	235	10	10	500	22	J,P	I,M
IM65X61	300	5	2	10	18	J,P	C,I,M
IM65X61A	235	10	10	500	22	J,P	I,M
1024 x 4							
IM6514	300	5	7	50	18	J,P	C,I,M

ROMS

Organization	Max Access Time (ns)	Vcc (V)	Icc Max (mA) Operating	Icc Max (μA) Standby	No. Pins	Package*	Temp Range
1024 x 12							
IM6312-1	510	5	1.8	100	18	J,F	I,M
IM6312A	250	10	2	500	18	J,F	I,M
2048 x 8							
IM6316	550	5	20	200	18	J	I,M

EPROMs

Organization	Max Access Time (ns)	Vcc (V)	Icc Max (mA) Operating	Icc Max (μA) Standby	No. Pins	Package*	Temp Range
1024 x 4							
IM6653	550	5	6	140	24	J	I,M
IM6653A	300	10	12	140	24	J	I,M
512 x 8							
IM6654	550	5	6	140	24	J	I,M
IM6654A	300	10	12	140	24	J	I,M

Bipolar PROMS

Organization	Max Access Time (ns)	Icc Max (mA)	No. Pins	Output Type	Package*	Temp
FPLA						
IM5200	100		24	OC	J	C
32 x 8						
IM5600	65	100	16	OC	J,F,P	C,M
IM5610	65	100	16	TS	J,F,P	C,M
256 x 4						
IM5603A	70	130	16	OC	J,F,P	C,M
IM5623	70	130	16	TS	J,F,P	C,M
512 x 4						
IM5604	80	140	16	OC	J,F,P	C,M
IM5624	80	140	16	TS	J,F,P	C,M

*See package and temperature key, p 8-2

MICROPROCESSOR

IM6100 Microprocessor Family

IM6100	— CMOS Microprocessor
IM6101	— CMOS Programmable Interface Element (PIE)
IM6102	— CMOS Memory Extension/DMA/Interval Timer/Controller (MEDIC)
IM6103	— CMOS 20 bit Parallel Input-Output Port (PIO)

UARTS

IM6402/IM6403

Development Support

6801	— IM6100 CMOS Family Sampler
6950	— Intercept Junior Tutorial System
6910	— Intercept II Microcomputer Prototype Development System
6940	— Intercept III Microcomputer Prototyping Development System
6975	— Intercept Dual Floppy Disk drive

IM8048 Peripheral

Development Support

6942	— Concept 48—Single Board Development Tool

SYSTEMS

LSI-8	— LSI Based PDP8® Computer System - see 6912, 6914, 6915.
6920	— CMOS EPROM Programmer

INTERSIL

2114
4096 Bit (1024 x 4) NMOS Static RAM

FEATURES

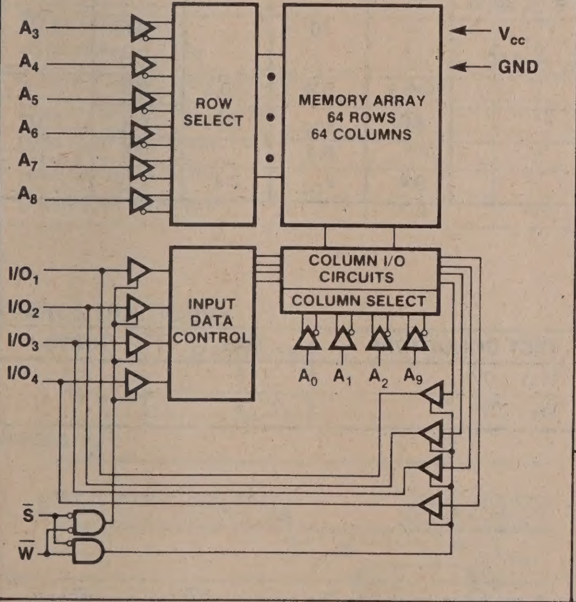
- **Cycle Time Equal to Access Time**
- **Completely Static - No Clock Required**
- **Common Data Input and Output**
- **TTL Compatible Inputs and Outputs**
- **883A Class B Processing Available**
- **Single +5 Volt Power Supply**
- **Pin Compatible with industry standard 2114**
- **Maximum Access Time:**
  - **-200 ns (–2)**
  - **-300 ns (–3)**
- **Maximum Power Dissipation:**
  - **–370 mW (2114L)**
  - **–525 mW (2114)**

DESCRIPTION

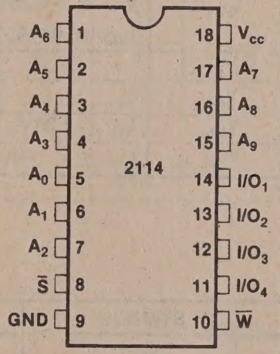
The 2114 is a 4096-bit static Random Access Memory organized 1024 words x 4 bits. The storage cells and decode and control circuitry are completely static, therefore no clocks or refresh operations are required. Memory access occurs within the specified access time after all address inputs are stable. A Chip Select input is provided for simple memory array expansion.

The 2114 is pin and performance compatible with the industry standard 2114 series, and the device is assembled in a standard 18-pin DIP for maximum system packing density.

BLOCK DIAGRAM

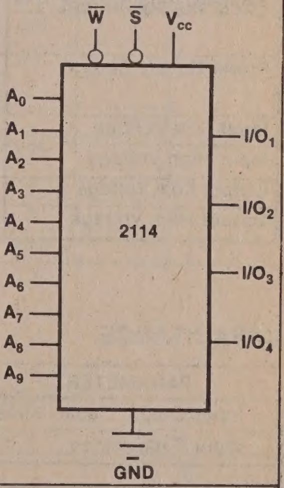

A_3
A_4
A_5
A_6
A_7
A_8
ROW SELECT
MEMORY ARRAY 64 ROWS 64 COLUMNS
V_{cc}
GND
I/O_1
I/O_2
I/O_3
I/O_4
INPUT DATA CONTROL
COLUMN I/O CIRCUITS
COLUMN SELECT
A_0
A_1
A_2
A_9
$\overline{S}$
$\overline{W}$

PIN CONFIGURATION


A_6 1
A_5 2
A_4 3
A_3 4
A_0 5
A_1 6
A_2 7
$\overline{S}$ 8
GND 9
18 V_{cc}
17 A_7
16 A_8
15 A_9
14 I/O_1
13 I/O_2
12 I/O_3
11 I/O_4
10 $\overline{W}$
2114

(outline dwgs JN,PN)

LOGIC SYMBOL


$\overline{W}$
$\overline{S}$
V_{cc}
A_0
A_1
A_2
A_3
A_4
A_5
A_6
A_7
A_8
A_9
2114
I/O_1
I/O_2
I/O_3
I/O_4
GND

PIN NAMES

A_0-A_9	ADDRESS INPUTS
I/O_1-I/O_4	DATA INPUT/OUTPUT
$\overline{W}$	WRITE ENABLE
$\overline{S}$	CHIP SELECT

ORDERING INFORMATION

POWER	ACCESS TIME			PACKAGE
	200ns	300ns	450ns	
370mW	D2114L2	D2114L3	D2114L	CERDIP
	P2114L2	P2114L3	P2114L	PLASTIC
525mW	D2114-2	D2114-3	D2114	CERDIP
	P2114-2	P2114-3	P2114	PLASTIC

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin to Ground	−0.5V to +7V
Power Dissipation	1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = +5V \pm 5\%$, $T_A = 0°C$ to $+70°C$

PARAMETER	SYMBOL	TEST CONDITIONS	2114L		2114		UNITS
			MIN	MAX	MIN	MAX	
Input Load Current	I_{INLD}	V_{IN} = 0V to 5.25V		10		10	μA
Output Leakage Current	I_{OLK}	$\overline{S}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}		10		10	
Power Supply Current	I_{CC2}	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = +25°C		65		90	mA
Power Supply Current	I_{CC1}	V_{IN} = +5.25V $I_{I/O}$ = 0mA, T_A = 0°C		70		100	
Input Low Voltage	V_{IL}		−0.5	0.8	−0.5	0.8	V
Input High Voltage	V_{IH}		2.0	V_{CC}	2.0	V_{CC}	
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA		0.4		0.4	
Output High Voltage	V_{OH}	I_{OH} = −1mA	2.4	V_{CC}	2.4	V_{CC}	

CAPACITANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	5	

NOTE: These parameters are periodically sampled, not 100% tested.

DEVICE OPERATION

When $\overline{W}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{W}$ remains high, the data stored cannot be changed by the addresses Chip Select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be changed by $\overline{W}$, the addresses, or the input data as long as $\overline{S}$ is high. Either $\overline{S}$ or $\overline{W}$ by itself, or in conjunction with the other, can prevent the extraneous writing due to signal transitions.

A read occurs during the overlap of $\overline{S}$ low and $\overline{W}$ high.

Data within the array can only be changed during a Write time, defined as the overlap of $\overline{S}$ low and $\overline{W}$ low. To prevent the loss of data, the addresses must to properly established during the entire Write time plus t_{wr}.

AC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = +5V \pm 5\%$, $T_A = 0°C$ to $+70°C$
$t_r = t_f = 10ns$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, Output Load = 1 TTL Gate and 100pF
Input and Output Timing Reference Level = 1.5V

READ CYCLE

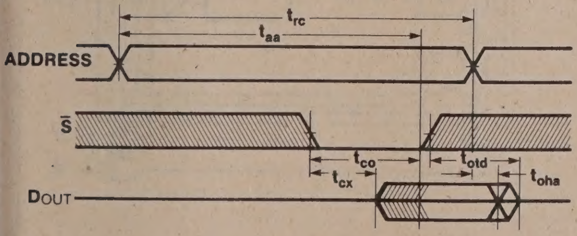
PARAMETER	SYMBOL	2114-2 2114L2		2114-3 2114L3		2114 21114L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{rc}	200		300		450		ns
Access Time	t_{aa}		200		300		450	
$\overline{S}$ to Output Valid	t_{co}		70		100		100	
$\overline{S}$ to Output Active	t_{cx}	20		20		20		
Output Three-State from Deselect	t_{otd}	0	60	0	80	0	100	
Output Hold from Address Change	t_{oha}	50		50		50		

WRITE CYCLE

PARAMETER	SYMBOL	2114-2 2114L2		2114-3 2114L3		2114 2114L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{wc}	200		300		450		ns
Write Time	t_w	120		150		200		
Write Release Time	t_{wr}	0		0		0		
Output Three-State from Write	t_{otw}	0	60	0	80	0	100	
Data to Write Time Overlap	t_{dw}	120		150		200		
Data Hold from Write Time	t_{dh}	0		0		0		
Address Setup Time	t_{aw}	0		0		0		
$\overline{S}$ Select Pulse Width	t_{cw}	120		150		200		

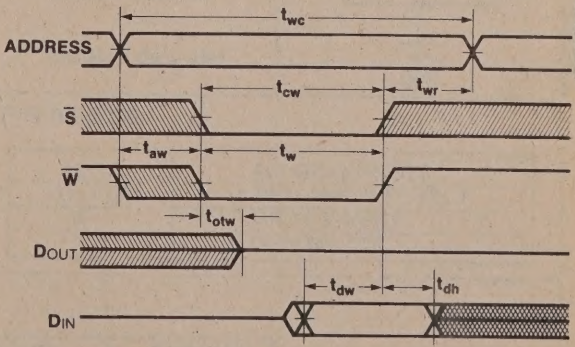
TIMING DIAGRAMS

READ CYCLE



t_{rc}
t_{aa}
ADDRESS
$\overline{S}$
t_{co}
t_{otd}
t_{cx}
t_{oha}
DOUT

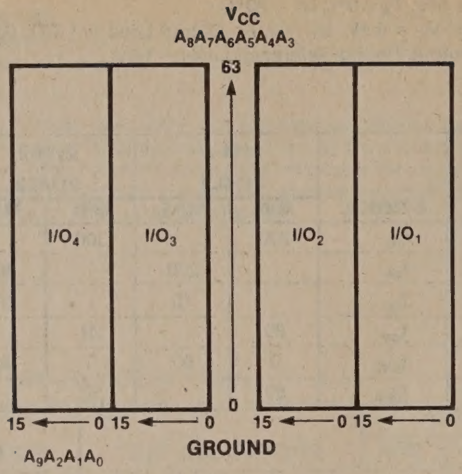
WRITE CYCLE



t_{wc}
ADDRESS
t_{cw}
t_{wr}
$\overline{S}$
t_{aw}
t_w
$\overline{W}$
t_{otw}
DOUT
t_{dw}
t_{dh}
DIN

Note: $\overline{W}$ is high for a READ cycle.

2114 BIT MAP DIAGRAM


V_{CC}
$A_8A_7A_6A_5A_4A_3$
63
0
I/O$_4$
I/O$_3$
I/O$_2$
I/O$_1$
15 ← 0 15 ← 0
15 ← 0 15 ← 0
$A_9A_2A_1A_0$
GROUND

INTERSIL

M2114L
4096 Bit (1024x4) NMOS Static RAM

FEATURES

- Cycle Time Equal to Access Time
- Completely Static-No Clock Required
- Common Data Input and Output
- TTL Compatible Inputs and Outputs
- 883A Class B Processing Available
- Single +5 Volt Power Supply
- Maximum Access Time:
  - –200 ns (–2)
  - –300 ns (–3)
- Maximum Power Dissipation: –495mW
- Pin Compatible with Intel M2114
- Military Temperature Operation: –55°C to +125°C

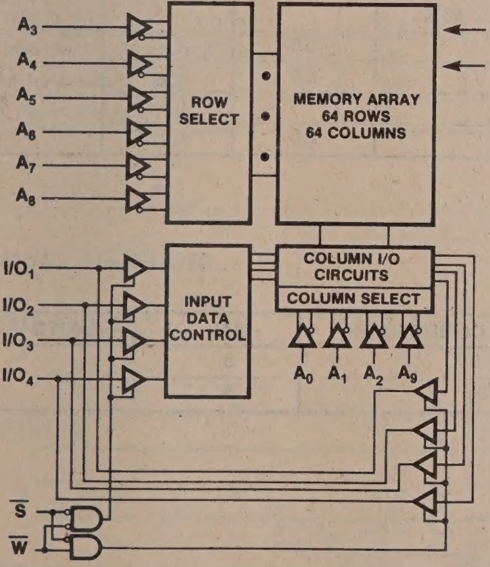
DESCRIPTION

The M2114L is a 4096-bit static Random Access Memory organized 1024 words x 4 bits. The storage cells and decode and control circuitry are completely static therefore, no clocks or refresh operations are required. Memory access occurs within the specified access time after all address inputs are stable. A Chip Select input is provided for simple memory array expansion.

The M2114L is pin and functionally compatible with the Intel M2114 series, and operations at 90mA over a 5V ± 10% range. The worst-case access time is 450ns with speeds of 300 ns (–3) and 200ns (–2) available.

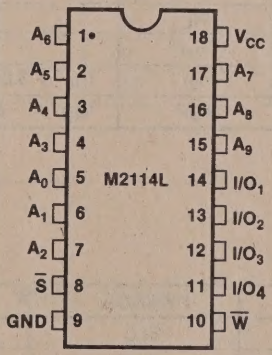
The device is assembled in a standard 18-pin DIP for maximum system packing density.

BLOCK DIAGRAM



A_3
A_4
A_5
A_6
A_7
A_8
ROW SELECT
MEMORY ARRAY 64 ROWS 64 COLUMNS
V_{CC}
GND
I/O_1
I/O_2
I/O_3
I/O_4
INPUT DATA CONTROL
COLUMN I/O CIRCUITS
COLUMN SELECT
A_0
A_1
A_2
A_9
$\overline{S}$
$\overline{W}$

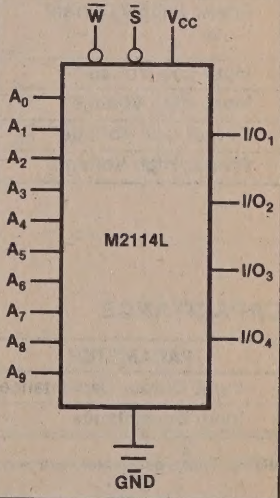
PIN CONFIGURATION



A_6 1
A_5 2
A_4 3
A_3 4
A_0 5
A_1 6
A_2 7
$\overline{S}$ 8
GND 9
18 V_{CC}
17 A_7
16 A_8
15 A_9
14 I/O_1
13 I/O_2
12 I/O_3
11 I/O_4
10 $\overline{W}$
M2114L

(outline dwg JN)

LOGIC SYMBOL



$\overline{W}$
$\overline{S}$
V_{CC}
A_0
A_1
A_2
A_3
A_4
A_5
A_6
A_7
A_8
A_9
M2114L
I/O_1
I/O_2
I/O_3
I/O_4
GND

PIN NAMES

A_0-A_9	ADDRESS INPUTS
I/O_1-I/O_4	DATA INPUT/OUTPUT
$\overline{W}$	WRITE ENABLE
$\overline{S}$	CHIP SELECT

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE
MD2114L2	200ns	CERDIP
MD2114L3	300ns	CERDIP
MD2114L	450ns	CERDIP

ABSOLUTE MAXIMUM RATINGS

Operating Temperature .... −55°C to +125°C
Storage Temperature .... −65°C to +150°C
Voltage on Any Pin to Ground .... −0.5V to +7V
Power Dissipation 1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input Load Current	I_{INLD}	V_{IN} = 0V to 5.5V		10	µA
Output Leakage Current	$\lvert I_{OLK} \rvert$	$\overline{S}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}		10	
Power Supply Current	I_{CC1}	V_{IN} = 5.5V, $I_{I/O}$ = 0mA, T_A = +25°C		65	mA
Power Supply Current	I_{CC2}	V_{IN} = 5.5V, $I_{I/O}$ = 0mA, T_A = −55°C		90	
Input Low Voltage	V_{IL}		−0.5	0.8	V
Input High Voltage	V_{IH}		2.0	V_{CC}	
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA		0.4	
Output High Voltage	V_{OH}	I_{OH} = −200µA	2.4	V_{CC}	

CAPACITANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	5	

NOTE: These parameters are periodically sampled, not 100% tested.

DEVICE OPERATION

When $\overline{W}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{W}$ remains high, the data stored cannot be changed by the addresses, Chip Select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be changed by $\overline{W}$, the addresses, or the input data as long as $\overline{S}$ is high. Either $\overline{S}$ or $\overline{W}$ by itself, or in conjuction with the other, can prevent the extraneous writing due to signal transitions.

A read occurs during the overlap of $\overline{S}$ low and $\overline{W}$ high. Data within the array can only be changed during a Write time, defined as the overlap of $\overline{S}$ low and $\overline{W}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{wr}.

AC CHARACTERISTICS

TEST CONDITIONS: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$
$t_r = t_f = 10ns$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, Output Load = 1 TTL Gate and 100pF
Input and Output Timing Reference Level = 1.5V

READ CYCLE

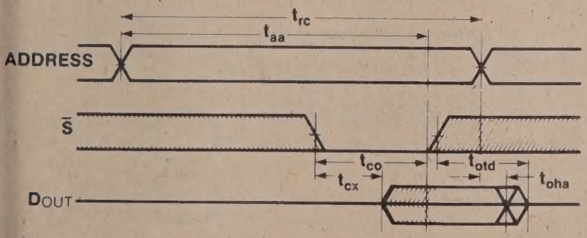
PARAMETER	SYMBOL	M2114L2		M2114L3		M2114L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{rc}	200		300		450		ns
Access Time	t_{aa}		200		300		450	
$\overline{S}$ to Output Valid	t_{co}		70		100		100	
$\overline{S}$ to Output Active	t_{cx}	20		20		20		
Output Three-State from Deselect	t_{otd}	0	60	0	80	0	100	
Output Hold from Address Change	t_{oha}	50		50		50		

WRITE CYCLE

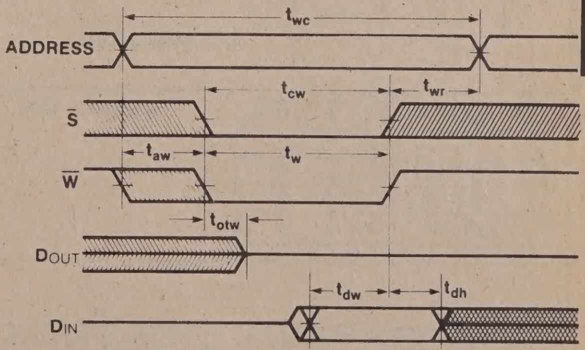
PARAMETER	SYMBOL	M2114L2		M2114L3		M2114L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{wc}	200		300		450		ns
Write Time	t_w	120		150		200		
Write Release Time	t_{wr}	0		0		0		
Output Three-State from Write	t_{otw}	0	60	0	80	0	100	
Data to Write Time Overlap	t_{dw}	120		150		200		
Data Hold from Write Time	t_{dh}	0		0		0		
Address Setup Time	t_{aw}	0		0		0		
$\overline{S}$ Select Pulse Width	t_{cw}	120		150		200		

TIMING DIAGRAMS

READ CYCLE (1)

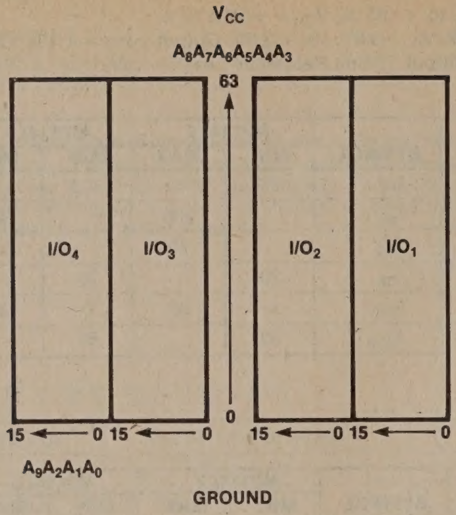

t_{rc}
t_{aa}
ADDRESS
$\overline{S}$
t_{co}
t_{otd}
t_{cx}
t_{oha}
DOUT

WRITE CYCLE


t_{wc}
ADDRESS
t_{cw}
t_{wr}
$\overline{S}$
t_{aw}
t_w
$\overline{W}$
t_{otw}
DOUT
t_{dw}
t_{dh}
DIN

Note: 1. $\overline{W}$ is high for a READ cycle.

2114 BIT MAP DIAGRAM


V_CC
A8A7A6A5A4A3
63
0
I/O4
I/O3
I/O2
I/O1
15 ← 0 15 ← 0 15 ← 0 15 ← 0
A9A2A1A0
GROUND

2147
4096 Bit (4096 x 1) HMOS Static RAM

FEATURES

- **High speed — 55ns maximum access time**
- **Automatic low-power standby — 550mW (2147L)**
- **Completely static — no clock required**
- **Single +5V supply**
- **TTL compatible inputs and outputs**
- **Three-state output**
- **HMOS Process technology**
- **Industry standard 2147 pin compatible**

GENERAL DESCRIPTION

The Intersil 2147 is a low power, high-speed 4096-bit static RAM organized 4096 words by 1 bit. It is an advanced version of the industry standard 2147, fabricated using Intersil's HMOS single-layer poly selective-oxidation process. Innovative design techniques result in minimum cell area and optimum circuit performance.

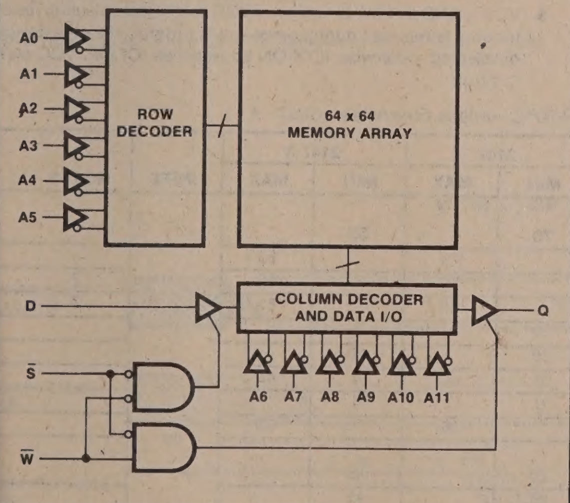
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

An automatic low-power standby mode is controlled by chip select ($\overline{S}$); less than one cycle time after $\overline{S}$ goes high, power dissipation drops from a maximum of 160mA to 20mA (2147).

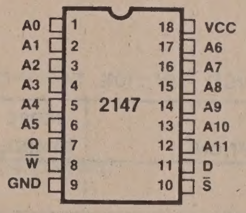
The basic device operates over the 5V ± 10% range with a worst-case access time of 70ns. A "−3" device is available with a worst-case access time of 55ns.

The Intersil 2147 is supplied in an 18-pin package with industry standard pin configuration.

BLOCK DIAGRAM

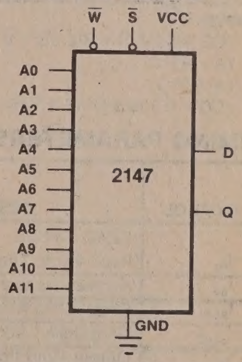

A0
A1
A2
A3
A4
A5
ROW DECODER
64 x 64 MEMORY ARRAY
COLUMN DECODER AND DATA I/O
D
Q
$\overline{S}$
$\overline{W}$
A6
A7
A8
A9
A10
A11

PIN CONFIGURATION


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
Q 7
$\overline{W}$ 8
GND 9
2147
18 VCC
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 D
10 $\overline{S}$

(outline dwg JN)

LOGIC SYMBOL


$\overline{W}$
$\overline{S}$
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
2147
D
Q
GND

PIN NAMES

A0-A11	ADDRESS INPUTS
D	DATA INPUT
Q	DATA OUTPUT
$\overline{S}$	CHIP SELECT
$\overline{W}$	WRITE ENABLE

ORDERING INFORMATION

PART NO.	ACCESS TIME	ACTIVE CURRENT	STANDBY CURRENT	PACKAGE	TEMP. RANGE
D2147-3	55ns	180mA	30mA	18 Pin CERDIP	0°C to +70°C
D2147L	70ns	140mA	10mA	18 Pin CERDIP	0°C to +70°C
D2147	70ns	160mA	20mA	18 Pin CERDIP	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
V_{IN}	Voltage on any Pin Relative to GND	–1.5	+7	V	2
I_{OS}	D.C. Output Current		20	mA	
t_{STORE}	Storage Temperature	–65	+150	°C	
t_{BIAS}	Ambient Temperature Under Bias	–10	+85	°C	
P_D	Power Dissipation		1	W	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
2. This device contains internal circuitry to protect against damage due to static charge. Conventional precautions should be observed, however, during storage, handling, and use to avoid exposure to excessive voltages.

ELECTRICAL PARAMETERS VCC = 5V ± 10%, TA = 0°C to +70°C, unless otherwise noted

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	TEST CONDITONS
V_{IH}	Input HIGH Voltage	2.0	6.0	V	
V_{IL}	Input LOW Voltage	– 1.0	0.8	V	
V_{OH}	Output HIGH Voltage	2.4		V	IOH = + 4.0mA
V_{OL}	Output LOW Voltage		0.4	V	IOL = 8mA
I_{IL}	Input Leakage Current		10	μA	V_{CC} = 5.5V, GND ≤ VIN ≤ VCC
I_{OLK}	Output Leakage Current		50	μA	V_{CC} = 5.5V, $\overline{S}$ = VIH, GND ≤ VO ≤ 4.5V
I_{OS}	Output Short Circuit Current	– 200	200	mA	V_{OUT} = GND to V_{CC}

SYMBOL	DESCRIPTION	MAXIMUM VALUES			UNITS	NOTES
		2147-3	2147L	2147		
ICCOP1	Operating Supply Current	170	135	150	mA	1, 2
ICCOP2	Operating Supply Current	180	140	160	mA	2, 3
ICCSB	Standby Supply Current	30	10	20	mA	4
ICCPON	Peak Power-On Supply Current	70	30	50	mA	5

NOTES:

1. VCC = 5.5V, $\overline{S}$ = VIL, IO = 0
2. TA = 25°C
3. TA = 0°C
4. VCC = 4.5 to 5.5V, $\overline{S}$ = VIH
5. VCC = GND to 4.5V, $\overline{S}$ = lower of VCC or VIH min. A pullup resistor on $\overline{S}$ is required during power-on in order to keep the device deselected; otherwise ICCPON approaches ICCOP. VCC slew ≥ 1V/μs.

TIMING PARAMETERS VCC = 5V ±10%, TA = 0°C to +70°C, unless otherwise noted[1, 4]

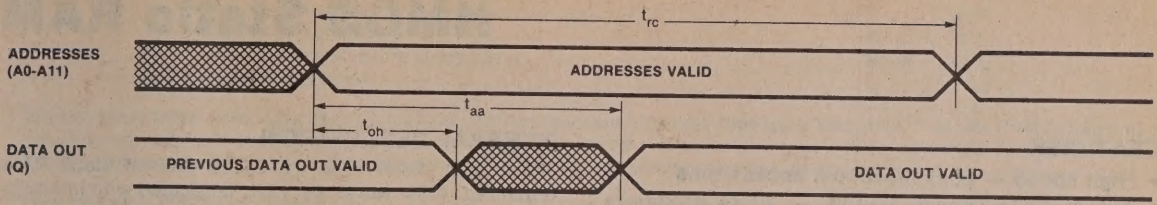
SYMBOL	DESCRIPTION	JEDEC SYMBOL	2147		2147-3		UNITS	NOTES
			MIN	MAX	MIN	MAX		
	READ CYCLE							
t_{rc}	Read Cycle Time		70		55		ns	
t_{aa}	Address Access Time	TAVQV		70		55		
t_{acs1}	Chip Select Access Time	TSLQV		70		55		2
t_{acs2}	Chip Select Access Time	TSLQV		80		65		3
t_{oh}	Output Hold from Address Change	TAXQX	5		5			
t_{lz}	Chip Selection to Output Enabled	TSLQX	10		10			
t_{hz}	Chip Deselection to Output Disabled	TSHQZ	0	40	0	40		
t_{pu}	Chip Selection to Power Up Time		0		0			
t_{pd}	Chip Deselection to Power Down Time			30		30		
	WRITE CYCLE							
t_{wc}	Write Cycle Time		70		55			
t_{cw}	Chip Selection to End of Write	TSLWH	55		45			
t_{aw}	Address Valid to End of Write	TAVWH	55		45			
t_{as}	Address Setup Time	TAVWL	0		0			
t_{wp}	Write Pulse Width	TWLWH	40		35			
t_{wr}	Write Recovery Time	TWHAX	15		10			
t_{dw}	Data Valid to End of Write	TDVWH	30		25			
t_{dh}	Data Hold Time	TWHDX	10		10			
t_{wz}	Write Enabled to Output Disabled	TWLQZ	0	35	0	30		
t_{ow}	Output Active from End of Write	TWHQX	0		0			

NOTES:

1. t_r = t_f = 10ns. Input and output timing reference level = 1.5V.
2. Device deselected for 55ns or more prior to selection.
3. Device deselected for a finite time less than 55ns prior to selection.
4. Operating temperature range is guaranteed with transverse ai flow exceeding 400 linear feet per minute.

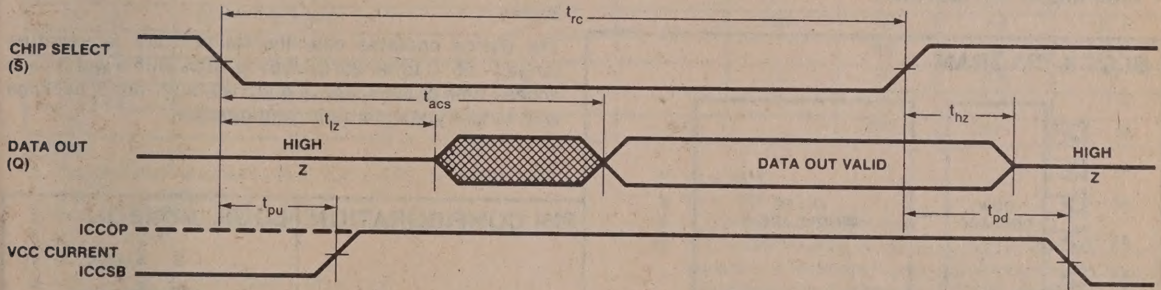
TIMING DIAGRAMS

Read Cycle (Address)


ADDRESSES (A0-A11)
ADDRESSES VALID
DATA OUT (Q)
PREVIOUS DATA OUT VALID
DATA OUT VALID
t_{rc}
t_{aa}
t_{oh}

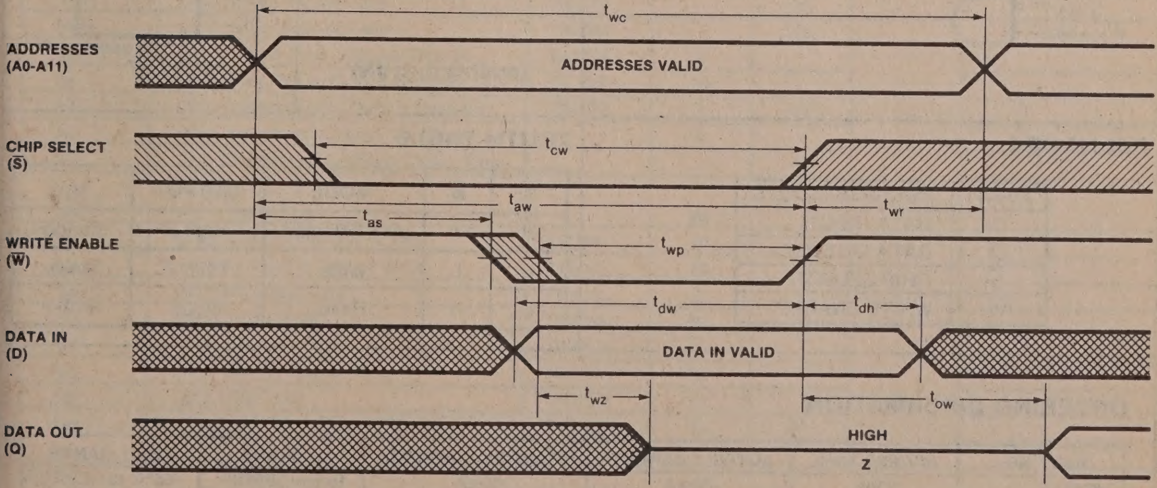
Notes: 1. Device is continuously selected, $\overline{S} = V_{IL}$.
2. Write Enable is high for read cycle, $\overline{W} = V_{IN}$.

Read Cycle (Chip Select)


CHIP SELECT ($\overline{S}$)
DATA OUT (Q)
HIGH
Z
DATA OUT VALID
HIGH
Z
ICCOP
VCC CURRENT
ICCSB
t_{rc}
t_{acs}
t_{lz}
t_{hz}
t_{pu}
t_{pd}

Note: Address is valid prior to or coincident with $\overline{S}$ transition low.

Write Cycle ($\overline{W}$ Controlled)


ADDRESSES (A0-A11)
ADDRESSES VALID
CHIP SELECT ($\overline{S}$)
WRITE ENABLE ($\overline{W}$)
DATA IN (D)
DATA IN VALID
DATA OUT (Q)
HIGH
Z
t_{wc}
t_{cw}
t_{aw}
t_{wr}
t_{as}
t_{wp}
t_{dw}
t_{dh}
t_{wz}
t_{ow}

INTERSIL

M2147
4096 Bit (4096 x 1) HMOS Static RAM

FEATURES

- **High speed — 85ns maximum access time**
- **Automatic low-power standby — 30mA maximum**
- **Full military temperature range**
- **883A Class B processing available**
- **Completely static — no clock required**
- **Single +5V supply**
- **TTL compatible inputs and outputs**
- **Three-state outputs**
- **HMOS process technology**
- **Intel M2147 compatible**

GENERAL DESCRIPTION

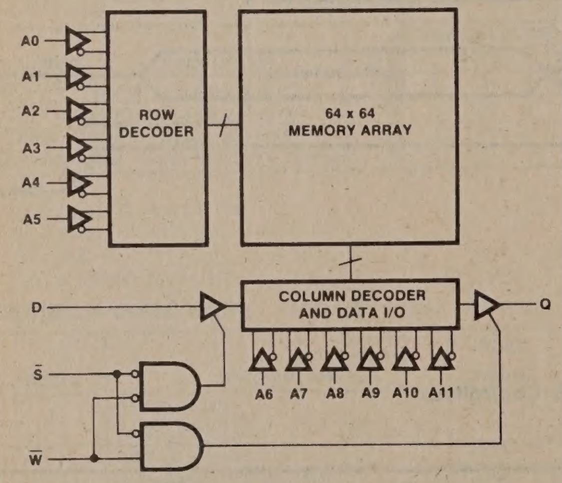
The Intersil M2147 is a high-speed 4096-bit static RAM organized 4096 words by 1 bit, fabricated with Intersil's HMOS single-layer poly selective-oxidation process. Innovative design techniques result in minimum cell area and optimum circuit performance.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

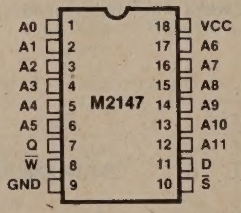
An automatic low-power standby mode is controlled by chip select ($\overline{S}$); less than one cycle time after $\overline{S}$ goes high, power dissipation drops from a maximum of 180mA to 30mA.

The device operates over the full military temperature range (−55°C to +125°C) at 5V ± 10% with a worst-case access time of 85ns, and is supplied in an 18-pin package with industry standard pin configuration.

BLOCK DIAGRAM

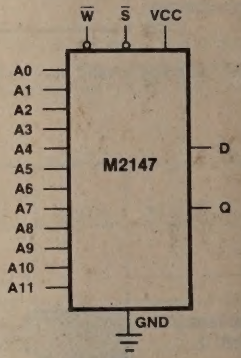

A0
A1
A2
A3
A4
A5
ROW DECODER
64 x 64 MEMORY ARRAY
D
COLUMN DECODER AND DATA I/O
Q
$\overline{S}$
A6
A7
A8
A9
A10
A11
$\overline{W}$

PIN CONFIGURATION


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
Q 7
$\overline{W}$ 8
GND 9
M2147
18 VCC
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 D
10 $\overline{S}$

(outline dwg JN)

LOGIC SYMBOL


$\overline{W}$
$\overline{S}$
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
M2147
D
Q
GND

PIN NAMES

A0-A11	ADDRESS INPUTS
D	DATA INPUT
Q	DATA OUTPUT
$\overline{S}$	CHIP SELECT
$\overline{W}$	WRITE ENABLE

TRUTH TABLE

$\overline{S}$	$\overline{W}$	MODE	OUTPUT	ICC
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	DOUT	Active

ORDERING INFORMATION

PART NO.	ACCESS TIME	ACTIVE CURRENT	STANDBY CURRENT	PACKAGE	TEMP. RANGE
MD2147	85ns	180mA	30mA	18-pin CERDIP	−55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Voltage on any Pin Relative to GND .... −1.5 to +7 Volts
D.C. Output Current 20mA
Storage Temperature .... −65 to +150°C
Ambient Temperature Under Bias .... −65 to +135°C
Power Dissipation 1W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS 1 VCC = 5V ±10%, TA = −55°C to +125°C unless otherwise noted

SYMBOL	DESCRIPTION	M2147			UNITS	NOTES
		MIN	TYP[1]	MAX		
V_{IH}	Input HIGH Voltage	2.0		6.0	V	
V_{IL}	Input LOW Voltage	−0.3		0.8	V	
I_{IL}	Input Leakage Current		0.01	10	µA	2
V_{OH}	Output HIGH Voltage	2.4			V	3
V_{OL}	Output LOW Voltage			0.45	V	4
I_{OLK}	Output Leakage Current		0.1	50	µA	5
I_{CCOP1}	Operating Supply Current		120	160	mA	6, 7
I_{CCOP2}	Operating Supply Current			180	mA	6, 8
I_{CCSB}	Standby Supply Current		15	30	mA	9
I_{CCPON}	Peak Power-On Supply Current		35	70	mA	10
I_{OS}	Output Short Circuit Current	−200		200	mA	

NOTES:

1. Typical values are measured at VCC = 5.0V, TA = 25°C and are not guaranteed.
2. VCC = 5.5V, GND ≤ VIN ≤ VCC
3. IOH = −1.0mA
4. IOL = 5mA
5. VCC = 5.5V, $\overline{S}$ = VIH, GND ≤ VO ≤ 4.5V
6. VCC = 5.5V, $\overline{S}$ = VIL, IO = 0
7. TA = 25°C
8. TA = −55°C
9. VCC = 4.5 to 5.5V, $\overline{S}$ = VIH
10. VCC = GND to 4.5V, $\overline{S}$ = lower of VCC or VIH min. A pullup resistor on $\overline{S}$ is required during power-on in order to keep the device deselected; otherwise ICCPON approaches ICCOP. VCC slew rate ≥ 1V/µS.

AC CHARACTERISTICS VCC = 5V ±10%, TA = −55°C to +125°C, unless otherwise noted

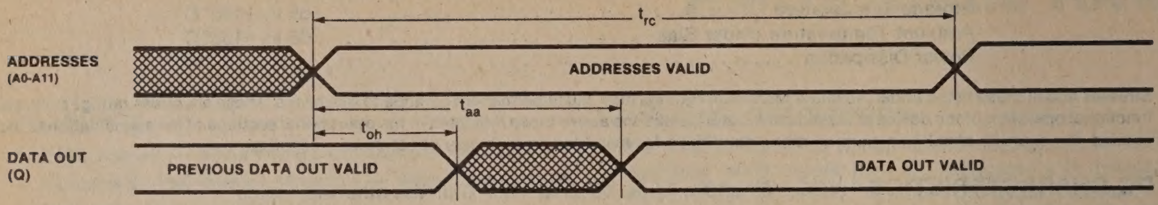
SYMBOL	DESCRIPTION	JEDEC SYMBOL	M2147		UNITS	TEST CONDITIONS
			MIN	MAX		
	READ CYCLE				ns	
t_{rc}	Read Cycle Time		85			
t_{aa}	Address Access Time	TAVQV		85		
t_{acs_1}	Chip Select Access Time	TSLQV		85		Note 2
t_{acs_2}	Chip Select Access Time	TSLQV		100		Note 3
t_{oh}	Output Hold from Address Change	TAXQX	5			
t_{lz}	Chip Selection to Output Enabled	TSLQX	10			
t_{hz}	Chip Deselection to Output Disabled	TSHQZ	0	40		
t_{pu}	Chip Selection to Power Up Time		0			
t_{pd}	Chip Deselection to Power Down Time			30		
	WRITE CYCLE					
t_{wc}	Write Cycle Time		85			
t_{cw}	Chip Selection to End of Write	TSLWH	70			
t_{aw}	Address Valid to End of Write	TAVWH	70			
t_{as}	Address Setup Time	TAVWL	0			
t_{wp}	Write Pulse Width	TWLWH	55			
t_{wr}	Write Recovery Time	TWHAX	15			
t_{dw}	Data Valid to End of Write	TDVWH	35			
t_{dh}	Data Hold Time	TWHDX	10			
t_{wz}	Write Enabled to Output Disabled	TWLQZ	0	50		
t_{ow}	Output Active from End of Write	TWHQX	0			

NOTES:

1. $t_r = t_f$ = 10ns. Input and output timing reference level = 1.5V. AC test conditions on page 8-19.
2. Device deselected for 55ns or more prior to selection.
3. Device deselected for a finite time less than 55ns prior to selection.

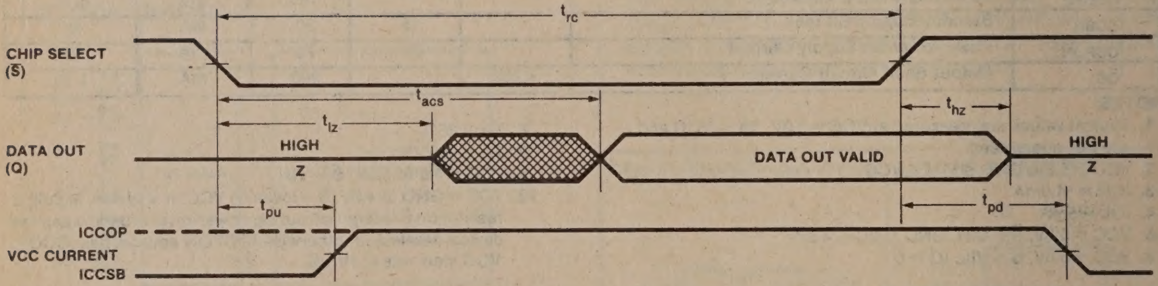
TIMING DIAGRAMS

Read Cycle (Address)


t_{rc}
ADDRESSES
(A0-A11)
ADDRESSES VALID
t_{aa}
t_{oh}
DATA OUT
(Q)
PREVIOUS DATA OUT VALID
DATA OUT VALID

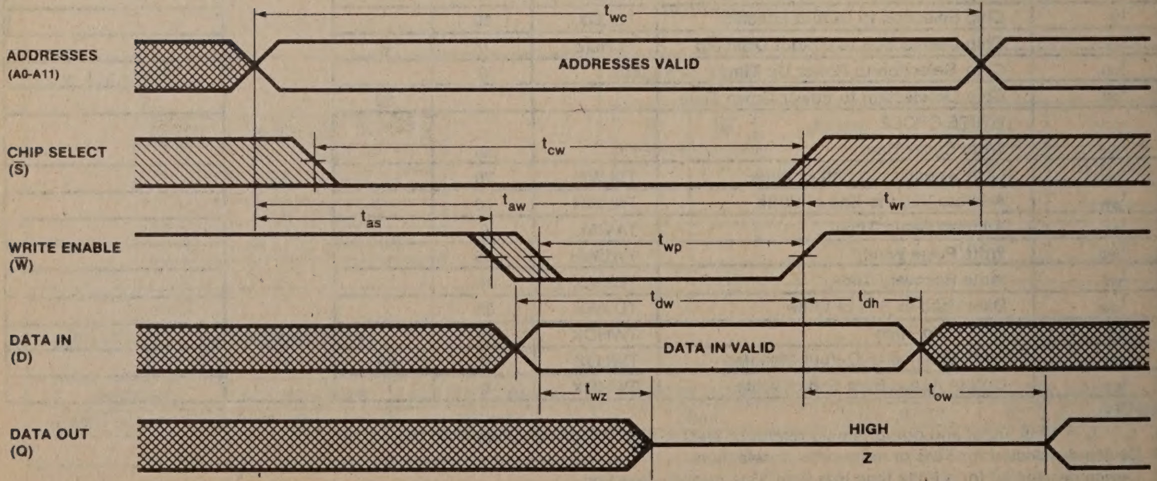
Notes: **1.** Device is continuously selected, $\overline{S} = V_{IL}$.
2. Write Enable is high for read cycle, $\overline{W} = V_{IH}$.

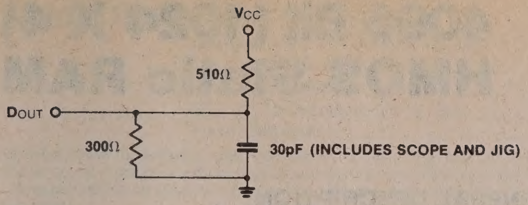
Read Cycle (Chip Select)


t_{rc}
CHIP SELECT
($\overline{S}$)
t_{acs}
t_{lz}
t_{hz}
DATA OUT
(Q)
HIGH
Z
DATA OUT VALID
HIGH
Z
t_{pu}
t_{pd}
ICCOP
VCC CURRENT
ICCSB

Note: Address is valid prior to or coincident with $\overline{S}$ transition low.

Write Cycle ($\overline{W}$ Controlled)


t_{wc}
ADDRESSES
(A0-A11)
ADDRESSES VALID
CHIP SELECT
($\overline{S}$)
t_{cw}
t_{aw}
t_{wr}
t_{as}
WRITE ENABLE
($\overline{W}$)
t_{wp}
t_{dw}
t_{dh}
DATA IN
(D)
DATA IN VALID
t_{wz}
t_{ow}
DATA OUT
(Q)
HIGH
Z


Vcc
510Ω
DOUT
300Ω
30pF (INCLUDES SCOPE AND JIG)

OUTPUT LOAD

AC TEST CONDITIONS

Input Pulse Levels .... GND to 3.5V
Input Rise and Fall Times .... $t_r = t_f = 10\mu s$
Input and Output Timing Reference Level 1.5V

INTERSIL

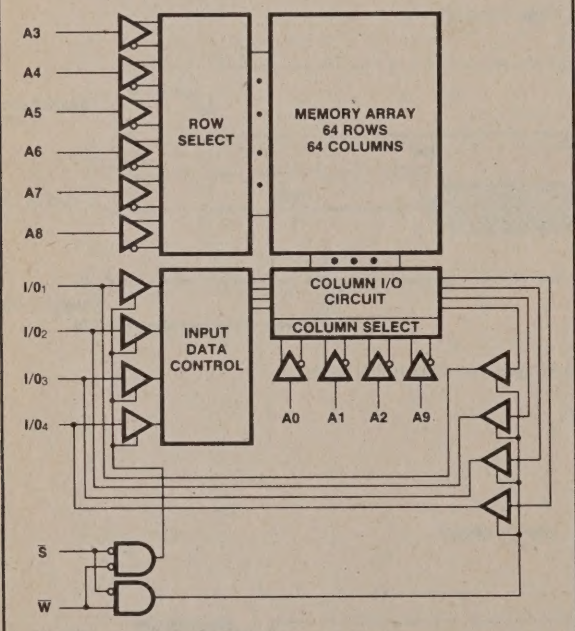
PRELIMINARY
Specifications Subject To Change Without Notice

2148
4096 Bit (1024 X 4) HMOS Static RAM

FEATURES

- High speed - 55ns maximum access time (2148-3)
- Automatic low-power standby - 165mW maximum
- Completely static - no clock required
- Single +5V supply
- TTL compatible inputs and outputs
- Three-state outputs
- HMOS Technology
- Pin compatible with industry standard 2114 and 2148 devices

BLOCK DIAGRAM


A3
A4
A5
A6
A7
A8
ROW SELECT
MEMORY ARRAY
64 ROWS
64 COLUMNS
I/O1
I/O2
I/O3
I/O4
INPUT DATA CONTROL
COLUMN I/O CIRCUIT
COLUMN SELECT
A0
A1
A2
A9
$\overline{S}$
$\overline{W}$

PIN NAMES

PIN NAMES	
A_0-A_9	Address Inputs
I/O_1-I/O_4	Data Input/Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Enable

GENERAL DESCRIPTION

The Intersil 2148 is a high speed 4096 bit static RAM organized 1024 words by 4 bits. It is a single-layer poly HMOS version of the industry standard 2114, and pin compatible with both the 2114 and 2148. Innovative design techniques result in minimum cell area and optimum circuit performance.

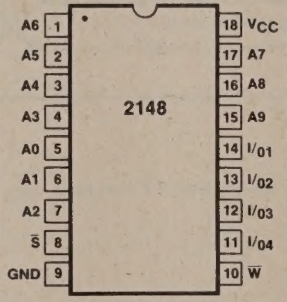
Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures.

An automatic low-power standby mode is controlled by chip select $\overline{S}$; less than one cycle time after $\overline{S}$ goes high, operating current drops from a maximum of 140 mA to a standby current of 30 mA.

The basic device operates over the 5V ±10% range with a worst-case access time of 70ns. A "-3" device is available with a worst-case access time of 55ns.

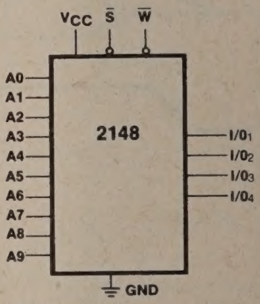
The Intersil 2148 is supplied in an 18-pin package with industry standard pin configuration.

PIN CONFIGURATION


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
$\overline{S}$ 8
GND 9
2148
18 VCC
17 A7
16 A8
15 A9
14 I/O1
13 I/O2
12 I/O3
11 I/O4
10 $\overline{W}$

(outline dwg JN)

LOGIC SYMBOL


VCC
$\overline{S}$
$\overline{W}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
2148
I/O1
I/O2
I/O3
I/O4
GND

TRUTH TABLE

$\overline{S}$	$\overline{W}$	MODE	I/O	POWER
H	X	Not Selected	High-Z	Standby
L	L	Write	DIN	Active
L	H	Read	DOUT	Active

ORDERING INFORMATION

PART NO.	ACCESS TIME	ACTIVE CURRENT	STANDBY CURRENT	PACKAGE	TEMP. RANGE
D2148	70ns	140mA	30mA	18 pin CERDIP	0°C to +70°C
D2148-3	55ns	140mA	30mA	18 pin CERDIP	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Voltage on any Pin Relative to GND1 .... –1.5 to +7V
D.C. Output Current 20mA
Storage Temperature .... –65 to +150°C
Ambient Temperature Under Bias .... –10 to +85°C
Power Dissipation 1.2W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES:

1. This device contains internal circuitry to protect against damage due to static charge. Conventional precautions should be observed, however, during storage, handling, and use to avoid exposure to excessive voltages.

ELECTRICAL PARAMETERS V_{CC} = 5V ±10%, T_A = 0°C to +70°C, unless otherwise noted

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
V_{IH}	Input HIGH Voltage	2.0	6.0	V	
V_{IL}	Input LOW Voltage	–1.0	0.8	V	
V_{OH}	Output HIGH Voltage	2.4		V	$I_{OH} = -2.0mA$
V_{OL}	Output LOW Voltage		0.4	V	$I_{OL} = 8mA$
I_{ILK}	Input Leakage Current		10	μA	$V_{CC} = 5.5V, GND \leq V_{IN} \leq V_{CC}$
I_{OLK}	Output Leakage Current		50	μA	$\overline{S} = V_{IH}, V_{CC} = 5.5V, GND \leq V_O \leq 4.5V$
I_{OS}	Output Short Circuit Current	–150	150	mA	$V_{OUT} = GND$ to V_{CC}

SYMBOL	DESCRIPTION	MAXIMUM VALUES		UNITS	NOTES
		2148-3	2148		
I_{CCOP1}	Operating Supply Current	135	135	mA	1, 2
I_{CCOP2}	Operating Supply Current	140	140	mA	1, 3
I_{CCSB}	Standby Supply Current	30	30	mA	4
I_{CCPON}	Peak Power-On Supply Current	50	50	mA	5

NOTES:

1. $V_{CC} = 5.5V, \overline{S} = V_{IL}, I_O = 0mA$
2. $T_A = 25°C$
3. $T_A = 0°C$
4. $V_{CC} = 4.5$ to $5.5V, \overline{S} = V_{IH}$
5. $V_{CC} = GND$ to $4.5V$, $\overline{S}$ = lower of V_{CC} or V_{IH} min. A pullup resistor on $\overline{S}$ is required during power-on in order to keep the device deselected; otherwise I_{CCPON} approaches I_{CCOP}. V_{CC} slew ≥ 1V/μs.

TIMING PARAMETERS V_{CC} = 5V ±10%, T_A = 0°C to +70°C Unless otherwise noted, 1, 4

SYMBOL	DESCRIPTION	JEDEC SYMBOL	2148-3		2148		UNITS	NOTES
			MIN	MAX	MIN	MAX		
	READ CYCLE						ns	
t_{rc}	Read Cycle Time		55		70			
t_{aa}	Address Access Time	TAVQV		55		70		
t_{asc1}	Chip Select Access Time	TSLQV		55		70		2
t_{asc2}	Chip Select Access Time	TSLQV		65		80		3
t_{oh}	Output Hold from Address Change	TAXQX	5		5			
t_{lz}	Chip Selection to Output Enabled	TSLQX	15		15			5
t_{hz}	Chip Deselection to Output Disabled	TSHQZ	0	25	0	25		5
t_{pu}	Chip Selection to Power Up Time		0		0			
t_{pd}	Chip Deselection to Power Down Time			30		30		
	WRITE CYCLE							
t_{wc}	Write Cycle Time		55		70			
t_{cw}	Chip Selection to End of Write	TSLWH	50		65			
t_{aw}	Address Valid to End of Write	TAVWH	50		65			
t_{as}	Address Setup Time	TAVWL	0		0			
t_{wp}	Write Pulse Width	TWLWH	40		50			
t_{wr}	Write Recovery Time	TWHAX	5		5			
t_{dw}	Data Valid to End of Write	TDVWH	25		25			
t_{dh}	Data Hold Time	TWHDX	5		5			
t_{wz}	Write Enabled to Output Disabled	TWLQZ	0	25	0	25		5
t_{ow}	Output Active from End of Write	TWHQX	5		5			

NOTES:

1. $t_r = t_f$ = 10ns. Input and output timing reference level = 1.5V. V_{IL} = 0V, V_{IH} = 3.0V.
2. Device deselected for 55ns or more prior to selection.
3. Device deselected for less than 55ns prior to selection. For deselect time of 0ns prior to select, read cycle (address) applies.
4. Operating temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
5. t_{lz} and t_{hz} are measured from 1.5V level of $\overline{S}$ to ±500mV from high impedance voltage of load circuit. t_{lz} and t_{hz} are sampled and not 100% tested.

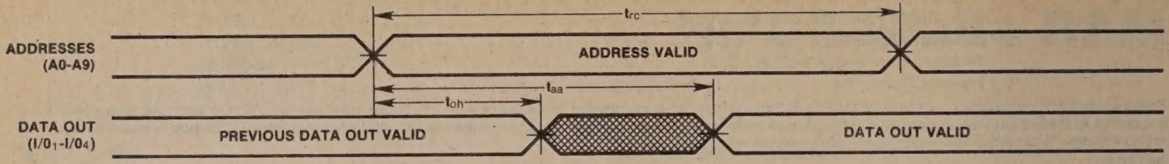
CAPACITANCE T_A = 25°C, f = 1.0mHz

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	7	pF	V_{OUT} = 0V

Note: Capacitance sampled and not 100% tested.

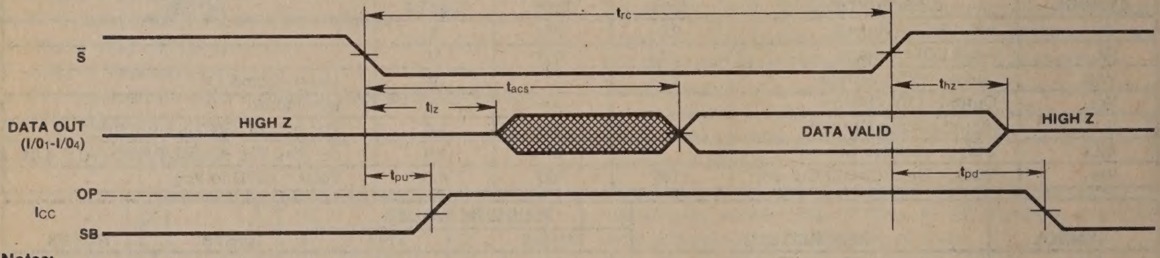
TIMING DIAGRAMS

Read Cycle (Address)


t_{rc}
ADDRESSES (A0-A9)
ADDRESS VALID
t_{aa}
t_{oh}
DATA OUT (I/O_1-I/O_4)
PREVIOUS DATA OUT VALID
DATA OUT VALID

Notes: 1. Device is continuously selected, $\overline{S} = V_{IL}$.
2. Write enable is high for read cycle, $\overline{W} = V_{IH}$.

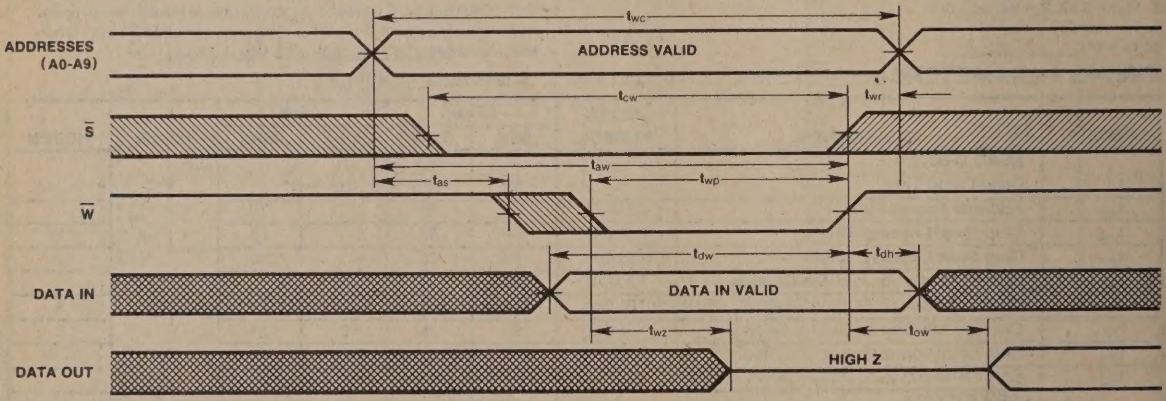
Read Cycle (Chip Select)


t_{rc}
$\overline{S}$
t_{acs}
t_{hz}
t_{lz}
DATA OUT (I/O_1-I/O_4)
HIGH Z
DATA VALID
HIGH Z
t_{pu}
t_{pd}
OP
I_{CC}
SB

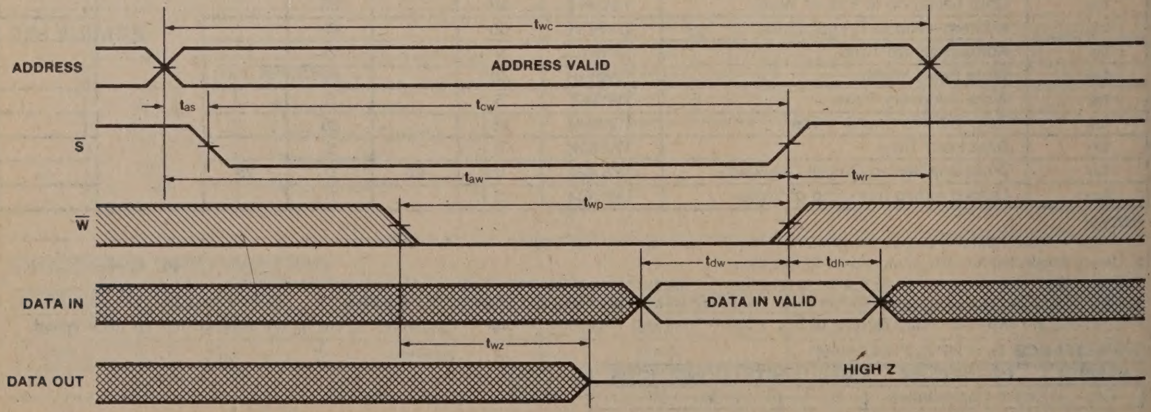
Notes:

1. Address is valid prior to or coincident with $\overline{S}$ transition low.
2. Write enable is high for read cycle, $\overline{W} = V_{IH}$.

Write Cycle ($\overline{W}$ Controlled)

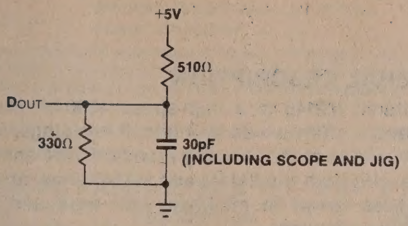

t_{wc}
ADDRESSES (A0-A9)
ADDRESS VALID
t_{cw}
t_{wr}
$\overline{S}$
t_{aw}
t_{as}
t_{wp}
$\overline{W}$
t_{dw}
t_{dh}
DATA IN
DATA IN VALID
t_{wz}
t_{ow}
DATA OUT
HIGH Z

Write Cycle ($\overline{S}$ Controlled)

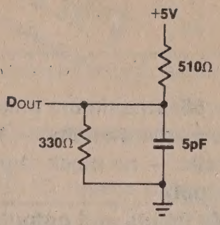

t_{wc}
ADDRESS
ADDRESS VALID
t_{as}
t_{cw}
$\overline{S}$
t_{aw}
t_{wr}
t_{wp}
$\overline{W}$
t_{dw}
t_{dh}
DATA IN
DATA IN VALID
t_{wz}
DATA OUT
HIGH Z

Note: Outputs remain high-Z if $\overline{S}$, $\overline{W}$ go high simultaneously.

TEST LOADS


+5V
510Ω
DOUT
330Ω
30pF
(INCLUDING SCOPE AND JIG)

AC PARAMETER LOAD CIRCUIT


+5V
510Ω
DOUT
330Ω
5pF

t_{lz}, t_{hz} LOAD CIRCUIT

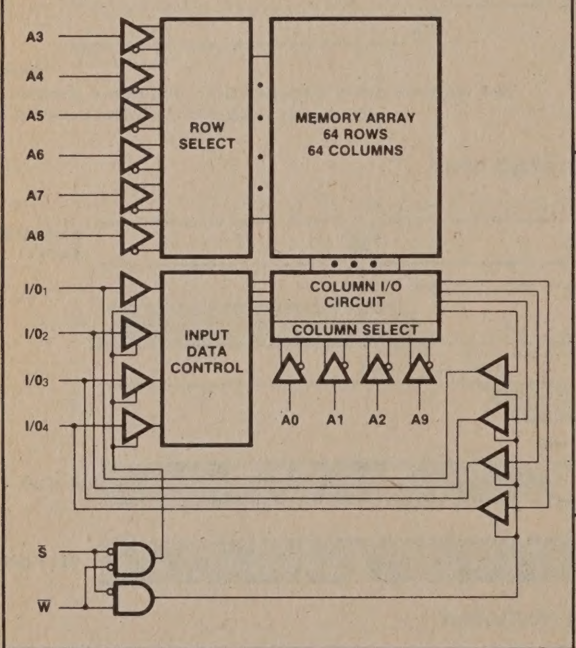
PRELIMINARY
Specifications Subject To Change Without Notice

M2148
4096 Bit (1024 X 4) HMOS Static RAM

FEATURES

- High speed — 85ns maximum access time
- Automatic low-power standby — 165mW maximum
- Completely static — no clock required
- Single +5V supply
- TTL compatible inputs and outputs
- Three-state outputs
- HMOS Technology
- Pin compatible with industry standard 2114M and M2148 devices

BLOCK DIAGRAM


A3
A4
A5
A6
A7
A8
ROW SELECT
MEMORY ARRAY 64 ROWS 64 COLUMNS
I/O1
I/O2
I/O3
I/O4
INPUT DATA CONTROL
COLUMN I/O CIRCUIT
COLUMN SELECT
A0
A1
A2
A9
S̄
W̄

PIN NAMES

PIN NAMES	
A_0-A_9	Address Inputs
I/O_1-I/O_4	Data Input/Output
S̄	Chip Select
W̄	Write Enable

GENERAL DESCRIPTION

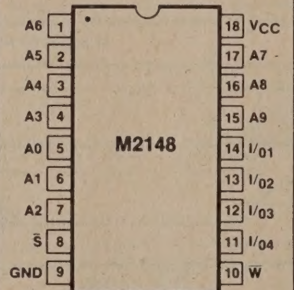
The Intersil M2148 is a high-speed 4096-bit static RAM organized 1024 words by 4 bits. It is a single-layer poly HMOS version of the industry standard 2114 and pin compatible with both the 2114M and M2148. Innovative design techniques result in minimum cell area and optimum circuit performance.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

An automatic low-power standby mode is controlled by chip select S̄; less than one cycle time after S̄ goes high, operating current drops from a maximum of 180 mA to a standby current of 30 mA.

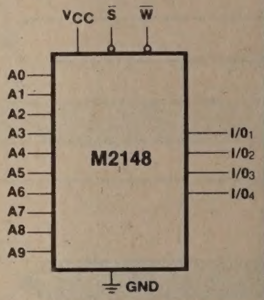
The device operates over the 5V ± 10% range with a worst-case access time of 85ns and is supplied in an 18-pin package with industry standard pin configuration.

PIN CONFIGURATION


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
S̄ 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 I/O1
13 I/O2
12 I/O3
11 I/O4
10 W̄
M2148

(outline dwg JN)

LOGIC SYMBOL


VCC
S̄
W̄
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
M2148
I/O1
I/O2
I/O3
I/O4
GND

TRUTH TABLE

S̄	W̄	MODE	I/O	POWER
H	X	Not Selected	High-Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

ORDERING INFORMATION

PART NO.	ACCESS TIME	ACTIVE CURRENT	STANDBY CURRENT	PACKAGE	TEMP. RANGE
MD2148	85ns	180mA	30mA	18 pin CERDIP	−55° to +125°C

ABSOLUTE MAXIMUM RATINGS

Voltage on any Pin Relative to GND1	−1.5 to +7V
D.C. Output Current	20mA
Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−65 to +135°C
Power Dissipation	1.2W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES:

1. This device contains internal circuitry to protect against damage due to static charge. Conventional precautions should be observed, however, during storage, handling, and use to avoid exposure to excessive voltages.

ELECTRICAL PARAMETERS V_{CC} = 5V ±10%, T_A = −55°C to +125°C, unless otherwise noted

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
V_{IH}	Input HIGH Voltage	2.0	6.0	V	
V_{IL}	Input LOW Voltage	−1.0	0.8	V	
V_{OH}	Output HIGH Voltage	2.4		V	$I_{OH} = -1.0mA$
V_{OL}	Output LOW Voltage		0.45	V	$I_{OL} = 5.0mA$
I_{ILK}	Input Leakage Current		10	μA	$V_{CC} = 5.5V$, $GND \leq V_{IN} \leq V_{CC}$
I_{OLK}	Output Leakage Current		50	μA	$\overline{S} = V_{IH}$, $V_{CC} = 5.5V$, $GND \leq V_O \leq 4.5V$
I_{OS}	Output Short Circuit Current	−200	200	mA	V_{OUT} = GND to V_{CC}

SYMBOL	DESCRIPTION	MAXIMUM VALUES	UNITS	NOTES
		M2148		
I_{CCOP1}	Operating Supply Current	160	mA	1, 2
I_{CCOP2}	Operating Supply Current	180	mA	1, 3
I_{CCSB}	Standby Supply Current	30	mA	4
I_{CCPON}	Peak Power-On Supply Current	70	mA	5

NOTES:

1. $V_{CC} = 5.5V$, $\overline{S} = V_{IL}$, $I_O = 0mA$
2. $T_A = 25°C$
3. $T_A = -55°C$
4. V_{CC} = 4.5 to 5.5V, $\overline{S} = V_{IH}$
5. V_{CC} = GND to 4.5V, $\overline{S}$ = lower of V_{CC} or V_{IH} min. A pullup resistor on $\overline{S}$ is required during power-on in order to keep the device deselected; otherwise I_{CCPON} approaches I_{CCOP}. V_{CC} slew ≥ 1V/μs.

TIMING PARAMETERS V_{CC} = 5V ±10%, T_A = −55°C to +125°C Unless otherwise noted, 1, 4

SYMBOL	DESCRIPTION	JEDEC SYMBOL	M2148		UNITS	NOTES
			MIN	MAX		
	READ CYCLE				ns	
t_{rc}	Read Cycle Time		85			
t_{aa}	Address Access Time	TAVQV		85		
t_{asc1}	Chip Select Access Time	TSLQV		85		2
t_{asc2}	Chip Select Access Time	TSLQV		100		3
t_{oh}	Output Hold from Address Change	TAXQX	5			
t_{lz}	Chip Selection to Output Enabled	TSLQX	10			5
t_{hz}	Chip Deselection to Output Disabled	TSHQZ	0	40		5
t_{pu}	Chip Selection to Power Up Time		0			
t_{pd}	Chip Deselection to Power Down Time			30		
	WRITE CYCLE					
t_{wc}	Write Cycle Time		85			
t_{cw}	Chip Selection to End of Write	TSLWH	70			
t_{aw}	Address Valid to End of Write	TAVWH	70			
t_{as}	Address Setup Time	TAVWL	0			
t_{wp}	Write Pulse Width	TWLWH	55			
t_{wr}	Write Recovery Time	TWHAX	15			
t_{dw}	Data Valid to End of Write	TDVWH	35			
t_{dh}	Data Hold Time	TWHDX	10			
t_{wz}	Write Enabled to Output Disabled	TWLQZ	0	50		5
t_{ow}	Output Active from End of Write	TWHQZ	10			

NOTES:

1. $t_r = t_f$ = 10ns. Input and output timing reference level = 1.5V. V_{IL} = 0V, V_{IH} = 3.0V.
2. Device deselected for 55ns or more prior to selection.
3. Device deselected for less than 55ns prior to selection. For deselect time of 0ns prior to select, read cycle (address) applies.
4. Operating temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
5. t_{lz} and t_{hz} are measured from 1.5V level of $\overline{S}$ to ±500mV from high impedance voltage of load circuit. t_{lz} and t_{hz} are sampled and not 100% tested.

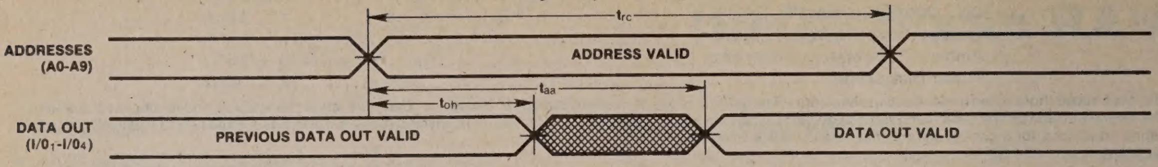
CAPACITANCE T_A = 25°C, f = 1.0mHz

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	7	pF	V_{OUT} = 0V

Note: Capacitance sampled and not 100% tested.

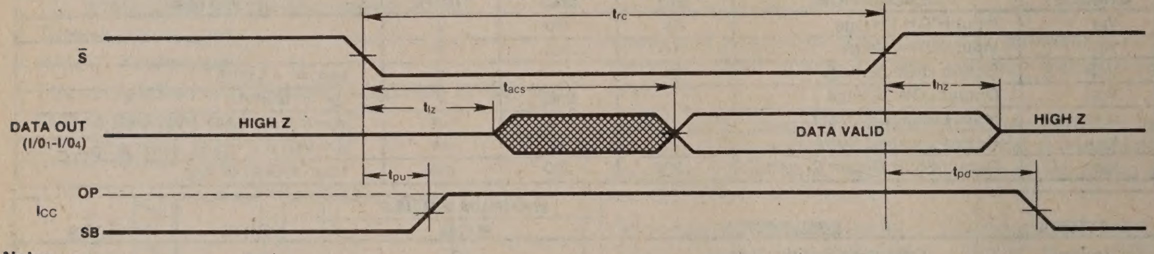
TIMING DIAGRAMS

Read Cycle (Address)


ADDRESSES (A0-A9)
t_{rc}
ADDRESS VALID
t_{aa}
t_{oh}
DATA OUT (I/O_1-I/O_4)
PREVIOUS DATA OUT VALID
DATA OUT VALID

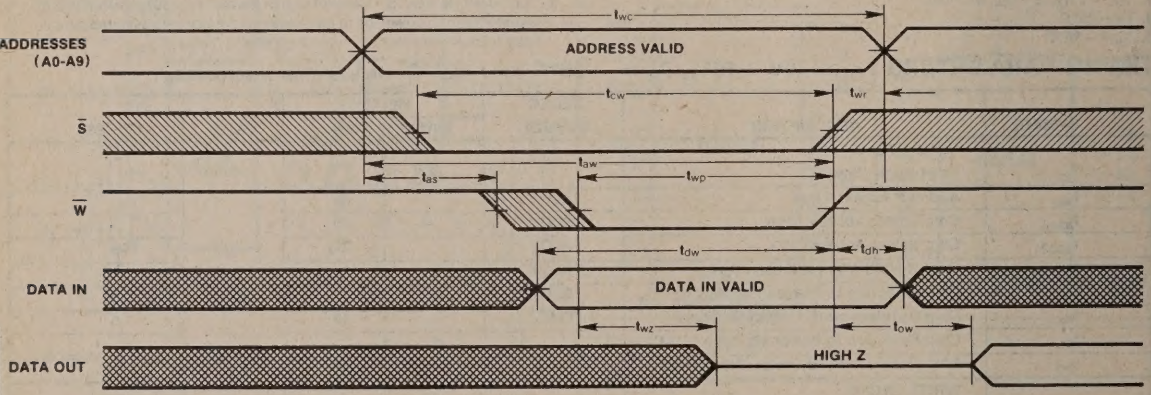
Notes: 1. Device is continuously selected, $\overline{S} = V_{IL}$.
2. Write enable is high for read cycle, $\overline{W} = V_{IH}$.

Read Cycle (Chip Select)

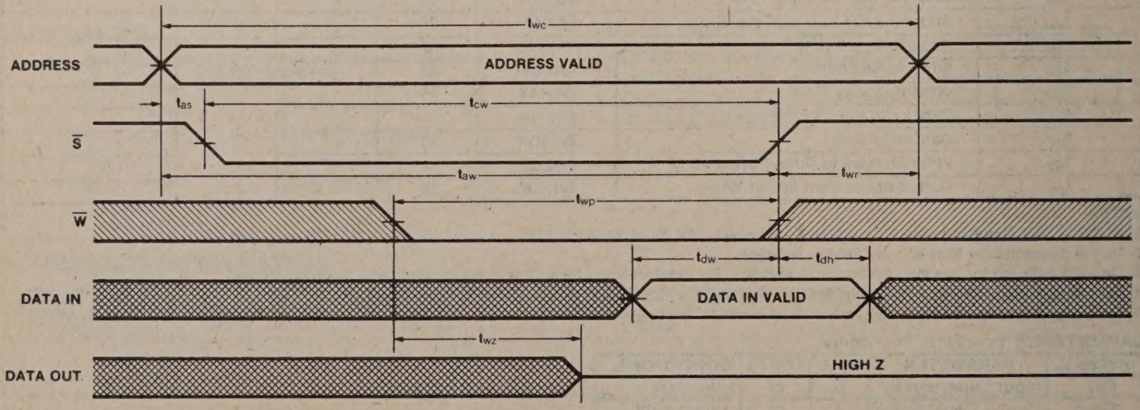

$\overline{S}$
t_{rc}
t_{acs}
t_{hz}
t_{lz}
DATA OUT (I/O_1-I/O_4)
HIGH Z
DATA VALID
HIGH Z
t_{pu}
t_{pd}
I_{CC}
OP
SB

Notes:
1. Address is valid prior to or coincident with $\overline{S}$ transition low.
2. Write enable is high for read cycle, $\overline{W} = V_{IH}$.

Write Cycle ($\overline{W}$ Controlled)

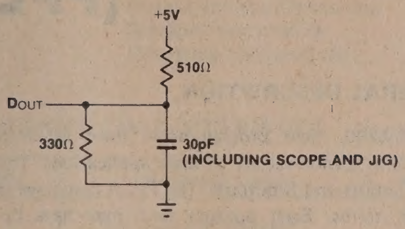

ADDRESSES (A0-A9)
t_{wc}
ADDRESS VALID
t_{cw}
t_{wr}
$\overline{S}$
t_{aw}
t_{as}
t_{wp}
$\overline{W}$
t_{dw}
t_{dh}
DATA IN
DATA IN VALID
t_{wz}
t_{ow}
DATA OUT
HIGH Z

Write Cycle ($\overline{S}$ Controlled)

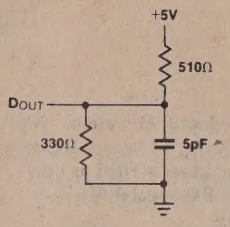

t_{wc}
ADDRESS
ADDRESS VALID
t_{as}
t_{cw}
$\overline{S}$
t_{aw}
t_{wr}
t_{wp}
$\overline{W}$
t_{dw}
t_{dh}
DATA IN
DATA IN VALID
t_{wz}
DATA OUT
HIGH Z

Note: Outputs remain high-Z if $\overline{S}$, $\overline{W}$ go high simultaneously.

TEST LOADS


+5V
510Ω
DOUT
330Ω
30pF
(INCLUDING SCOPE AND JIG)

AC PARAMETER LOAD CIRCUIT


+5V
510Ω
DOUT
330Ω
5pF

t_{lz}, t_{hz} LOAD CIRCUIT

IM5200 Field Programmable Logic Array (FPLA)

FEATURES

- Avalanche Induced Migration (AIM) Programmability
- 48 Product Terms, 14 Inputs, 8 Outputs
- Output Active Level – High or Low
- Product Term Expandability
- Edit Flexibility
- DTL/TTL Compatible Inputs and Outputs
- tpd – typically 65 ns
- 5 Volt ± 5% Power Supply
- Passive Pullup Outputs

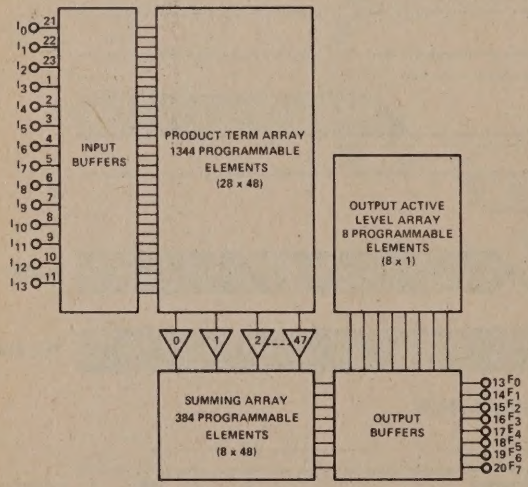
APPLICATIONS

- Random Combinatorial Logic
- Code Conversion
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits, Counters, Registers, RAMs, etc.
- Character Generators
- Decoders or Encoders

GENERAL DESCRIPTION

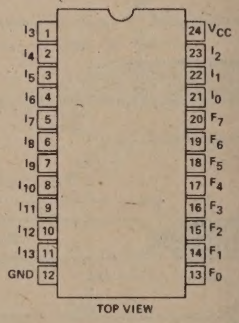
The IM5200, field programmable logic array (FPLA), is useful in a wide variety of logic applications. The device has 14 inputs and 8 outputs. The FPLA may have up to 48 product terms. Each product term may have up to 14 variables and each one of the outputs provides a sum of the product terms. The FPLA is functionally equivalent to a collection of AND gates which may be OR'ed at any of its outputs. Since some functions are more easily represented in their inverted form, the output level is also programmable to either a high or low active level. The IM5200 is provided with passive pullup outputs. This output configuration is useful for product term expansion by wire-ANDing the outputs of different IM5200's.

LOGIC DIAGRAM



I_0 21
I_1 22
I_2 23
I_3 1
I_4 2
I_5 3
I_6 4
I_7 5
I_8 6
I_9 7
I_{10} 8
I_{11} 9
I_{12} 10
I_{13} 11
INPUT BUFFERS
PRODUCT TERM ARRAY 1344 PROGRAMMABLE ELEMENTS (28 x 48)
OUTPUT ACTIVE LEVEL ARRAY 8 PROGRAMMABLE ELEMENTS (8 x 1)
0
1
2
47
SUMMING ARRAY 384 PROGRAMMABLE ELEMENTS (8 x 48)
OUTPUT BUFFERS
13 F_0
14 F_1
15 F_2
16 F_3
17 F_4
18 F_5
19 F_6
20 F_7

PIN CONFIGURATION (outline dwg JG)



I_3 1
I_4 2
I_5 3
I_6 4
I_7 5
I_8 6
I_9 7
I_{10} 8
I_{11} 9
I_{12} 10
I_{13} 11
GND 12
24 V_{CC}
23 I_2
22 I_1
21 I_0
20 F_7
19 F_6
18 F_5
17 F_4
16 F_3
15 F_2
14 F_1
13 F_0
TOP VIEW

ORDERING INFORMATION

MEMORY CIRCUIT MARKING AND PRODUCT CODE EXPLANATION

IM 5200 C JG

Package
JG = Cerdip 24 Pin Dip
Temperature Range
C = 0°C to +70°C
Device Type
Intersil Memory

MAXIMUM RATINGS

Supply Voltage Rating	– 0.5V to + 7V
Input Voltage	– 1.5V to + 5.5V
Output Voltage (Operating)	– 0.5V to + 5.5V
Storage Temperature	– 65 °C to 150 °C
Operating Temperature	0 °C to + 70 °C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V +5%, T_A = 0°C to 70°C

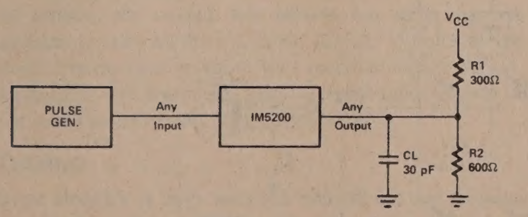
SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
I_{IL}	Low level input current		-0.63	-1.0	mA	V_{IL} = 0.4V
I_{IH}	High level input current		5	40	μA	V_{IH} = 4.5V
V_{IL}	Input low threshold voltage			0.8	V	
V_{IH}	Input high threshold voltage	2.0			V	
V_C	Input clamp voltage		-.9	-1.5	V	I_{IN} = -10 mA
BV_{in}	Input breakdown voltage	5.5	6.5		V	I_{IN} = 1.0 mA
V_{OH}	Output high voltage	2.4	3.25		V	I_{OH} = -250μA
I_{CEX}	Output leakage current		<1	50.	μA	V_O = 5.5V
I_{SC}	Output short circuit current	-0.7	-1.1	-1.7	mA	V_O = 0V
V_{OL}	Output low voltage		0.3	0.45	V	I_{OL} = 12 mA
I_{CC}	Power Supply Current		135		mA	Inputs either open or at ground (see note 3).
C_{in}	Input capacitance		5	10	pF	V_{in} = 2.0V, V_{CC} = 0V
C_{out}	Output capacitance		7	12	pF	V_O = 2.0V, V_{CC} = 0V
t_{pd}	Input to output switching delay (t_{+-}, t_{++}, t_{-+}, t_{--})	20	65	100	ns	See switching test circuit

NOTE 1: Conditions for all typical values are V_{CC} = 5V, T_A = 25°C.

NOTE 2: Conditions for all maximum and minimum specifications are the worst case for the complete range of V_{CC} and T_A.

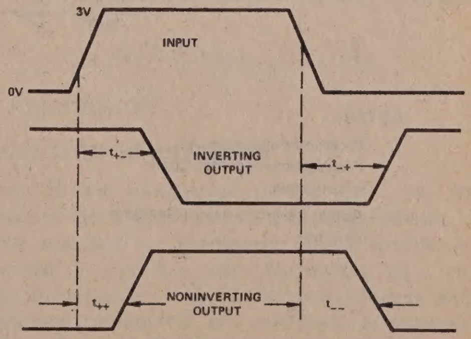
NOTE 3: Power consumption will increase after programming. The increase will be typically 0.75 mA per product term programmed.

SWITCHING DELAY TEST CIRCUIT



FREQ = 1MHz
DUTY CYCLE = 50%
AMPLITUDE = 0V to 3V
$t_R = t_F$ = 5 ns

SWITCHING WAVEFORMS



ALL MEASUREMENTS MADE AT 1.5V LEVELS

PRODUCT DESCRIPTION

AVALANCHE INDUCED MIGRATION TECHNOLOGY

The AIM element is a minimum size, open base, NPN transistor. The emitter is contacted by an aluminum "column" line and the collector is common with the collectors of other elements and the "row" driver collector. A conventional gold-doped TTL process is used to fabricate the AIM element and all other transistors, diodes and resistors on the chip. The programming technique is to force a high current through the element from emitter to collector. This forces the emitter-base junction beyond normal avalanche and into a second breakdown mode. In the second breakdown, the current constricts to a narrow high temperature filament. Aluminum then migrates down the filament to the emitter-base-junction and causes a short of that junction. The drop in power dissipation, as soon as the emitter-base short is achieved, causes a decrease in temperature. Since temperature is a driving force in the programming action, further advance of migrating aluminum is inhibited after programming is achieved. The action is thus self-limiting. The AIM programming technique assures superior reliability since the element junction where the programming action occurs is inherently hermetic.

GENERAL DESCRIPTION

The IM5200 Field Programmable Logic Array (FPLA) is a logic element designed to produce a sum of product terms, which may be programmed by the user, at each of eight outputs. The basic operating circuit is comprised of 56 input inverters, which generate the true and complement of the 14 inputs, 48 twenty-eight input AND gates, 8 forty-eight input NOR gates and 3 arrays of AIM programmable elements. Additional circuitry is dedicated to the functions of programming and testing before programming. All outputs have 4K resistor pull-ups which permit wire-ANDing. Inputs are DTL and TTL designs with 2 V_{BE} operating thresholds.

Product Term Array

The Product Term Array, consisting of a 48 x 28 element AND array, allows the desired true or complement inputs to be connected by programming to the 48 AND gates which form the product terms. Only the input variables included in the product terms are programmed. New variables may always be added to a previously programmed product-term until all 14 variables have been used.

Summing Array

A 48 x 8 element OR array allows any combination of as many as 48 product terms to be logically summed (OR'ed) at each output by programming.

Output Active Level Array

The Output Active Level Array consists of eight elements, one per output, which provide for changing the active level of any output from LOW to HIGH. Active LOW is the necessary active state when expanding product terms by the parallel connections of two (2) or more IM5200s. The programmable active HIGH feature may be used to advantage in nonexpanded applications to save inverters and/or product terms when system considerations so require.

LOGIC OPERATION

The operating logic and AIM programmable element arrays are shown in Figure 1. In logic equation form each output can be expressed in the SUM OF PRODUCTS form.

F_i or $\overline{F_i}$ = logical sum of any user programmed combination of 48 available product terms (PT_j)

where PT_j = any user programmed combination of the true or complement of the 14 available inputs (I_k).

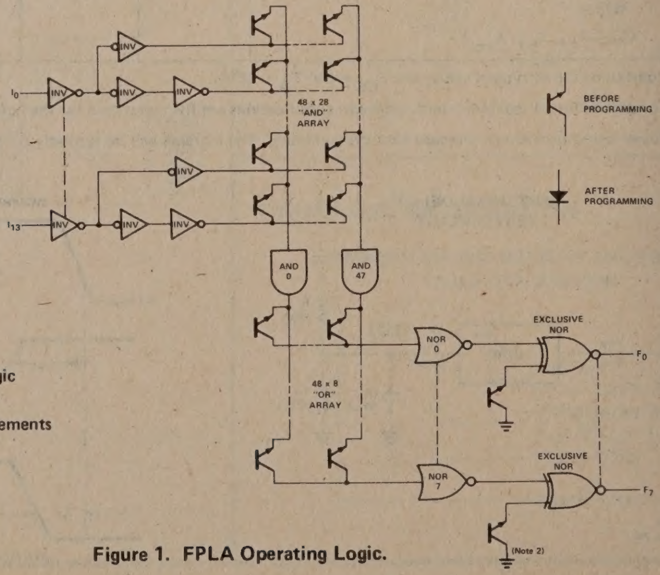


Figure 1. FPLA Operating Logic.

NOTES

1. Programming Logic and Preprogramming Test Logic is not shown.
2. Active Level Inversion Elements (8 total)

Some examples of possible SUM-OF-PRODUCT-TERMS functions and individual PRODUCT TERMS are:

SUM OF PRODUCT TERMS

$$\overline{F}_1 = PT_3 + PT_{28} + PT_{39} + PT_{47}$$

$$F_3 = PT_1 + PT_{33} + PT_{39} + PT_{45} + PT_{46} + PT_{47}$$

$$\overline{F}_7 = PT_2$$

PRODUCT TERMS

$$PT_3 = I_0\,\overline{I}_2\,\overline{I}_8\,\overline{I}_{13}$$

$$PT_{46} = I_1\,\overline{I}_6\,I_9\,I_{11}\,\overline{I}_{12}\,I_{13}$$

$$PT_2 = I_4$$

A product term is not necessarily a minterm since a minterm contains *all* input variables. The unprogrammed inputs of a product term that is not a minterm are "don't care". For example, the product term $I_1\,I_3\,\overline{I}_{13}$ will activate any output to which it is programmed whenever the I_1 input is HIGH, I_3 is HIGH, and I_{13} is LOW, regardless of the logic state of the other inputs. A minterm expansion of $I_1\,I_3\,\overline{I}_{13}$ would produce 2^{11} miniterms which means there are 2^{11} out of 2^{14} possible combinations of all 14 input variables that will activate any output to which the product term is programmed.

Any minterm condition applied to the IM5200 inputs will select (1) no product terms, (2) one product term, or (3) more than one product term.

In the case of no product term selection all the outputs will be in the inactive state (opposite to the levels specified in the ACTIVE LEVEL DATA for each output).

When only one product term is selected, the outputs assume the active levels specified by the SUMMING DATA TRUTH TABLE entry for the selected product term. The outputs not specified as active will assume the inactive state (opposite state to that specified in the ACTIVE LEVEL DATA).

To determine the output status for a case of multiple product term selection, first all of the product terms selected must be identified. Each output state can then be determined by examining the SUMMING DATA for all of the multiply selected product terms.

If *any* of the product terms has an active level specified for the output, the output will assume the active state as specified by the ACTIVE LEVEL DATA. If *none* of the product terms have an active level specified for the output, the outputs will assume the inactive state (opposite state to that specified by the ACTIVE LEVEL DATA.

TESTING

Some circuitry is built into the IM5200 for test purposes only. On an unprogrammed part it allows for:

1. Testing the output in the LOW state
2. Sampling the switching delay time through a maximum delay path
3. Checking the accuracy of programming circuitry decoding
4. Checking the integrity of programming paths under programming conditions

This test capability assures high programming yield and data sheet electrical performance after programming of parts.

PRODUCT TERM MINIMIZATION TECHNIQUES

Standard two (2) level multi-output minimization techniques (e.g. Quine-McCluskey algorithm) can be used to realize a minimal sum of product terms. In certain cases, the number of product terms can be further reduced by sharing product terms and by inverting the output active level. These techniques are important in cases where the initial specification indicates a need for more than 48 product terms.

APPLICATION OF BOOLEAN REDUCTION

REALIZE: $F_1 = \overline{I}_2\,\overline{I}_1\,\overline{I}_0 + I_2\,I_1\,\overline{I}_0 + I_2\,I_1\,I_0$

Applying the distributive law, product terms $I_2\ I_1\ I_0$ and $I_2\ I_1\ \overline{I}_0$ can be expressed as $I_2\ I_1\ (I_0 + \overline{I}_0)$. By the law of complement, $I_0 + \overline{I}_0 = 1$ and the entire expression is reduced to:

$$F_1 = \overline{I}_2\,\overline{I}_1\,\overline{I}_0 + I_2\,I_1$$

PRODUCT TERM SHARING

REALIZE: $F_1 = \overline{I}_2\,\overline{I}_1\,\overline{I}_0 + \overline{I}_2\,I_1\,\overline{I}_0$

$F_2 = \overline{I}_2\,I_1\,\overline{I}_0 + I_2\,\overline{I}_1\,\overline{I}_0$

Since $\overline{I}_2\ I_1\ \overline{I}_0$ is common to both F_1 and F_2, it may be shared so that only three product terms, rather than four, are required.

ACTIVE LEVEL INVERSION

REALIZE: $F_1 = \overline{I}_2\,\overline{I}_1\,\overline{I}_0 + \overline{I}_2\,I_1\,I_0 + I_2\,\overline{I}_1\,I_0 + I_2\,I_1$

To achieve a reduction in product terms, in this case, F_1 can be realized in its complement form using DeMorgan's Theorems. The true form required a HIGH active level and 4 product terms. The complement form requires a LOW active level and 3 product terms.

$$\overline{F}_1 = \overline{I}_2\,\overline{I}_1\,I_0 + \overline{I}_2\,I_1\,\overline{I}_0 + I_2\,\overline{I}_1\,\overline{I}_0$$

EDIT FLEXIBILITY

PRODUCT TERM DEACTIVATION

The true or the complement of any input may be connected to the AND gates by programming. However, if both the true *and* the complement of any variable are programmed in a product term, that product term will never be selected since $I_i \cdot \overline{I}_i = 0$. This feature may be used to deactivate permanently any previously programmed product term.

ADDITION OF NEW INPUT VARIABLES TO EXISTING PRODUCT TERMS

In the AIM technology only the active inputs are programmed. Unprogrammed inputs are "don't care." Therefore, additional input variables can be added to the "old" product terms at any time. For example,

Old Product Term

$I_0 I_1 \bar{I}_4$ ($I_2, I_3, I_5 \cdots I_{13}$ = don't care)

Adding input variable I_2 (true or complement) to the product term would yield:

New Product Term

$I_0 I_1 I_2 \bar{I}_4$ ($I_3, I_5 \cdots I_{13}$ = don't care)

EXPANDING A SUM OF PRODUCT TERMS BY ADDING NEW PRODUCT TERMS

New product terms may be added to the sum of product terms at any output by programming the AIM element that connects the product term AND gate to the output thereby enabling activation of the output when the product term is activated. The product term may be one already used in another output sum of product terms or it may be one that has not previously been used.

CHANGING AN OUTPUT ACTIVE LEVEL FROM LOW TO HIGH

Any outputs that are active LOW can be changed to active HIGH by programming the corresponding AIM element in the OUTPUT ACTIVE LEVEL ARRAY.

PROGRAMMING

GENERAL

Recommended Programmer is DATA I/O model 10.

Programming an IM5200 requires:

1. Two input pins, I_0 and I_9 corresponding to pins 21 and 7, respectively, to be forced to a voltage above normal TTL operating levels to establish the programming mode.
2. One input pin, I_3 corresponding to pin 1, to be switched between a high level and ground to select between the Summing Array (OR Array) or the Product Term Array (AND Array), respectively.
3. Four outputs, F_0, F_1, F_2, and F_3 corresponding to pins 13, 14, 15, and 16, respectively, for the routing of current into one of four sectors of the arrays.
4. Nine inputs, I_4, I_5, I_6, I_7, I_8, I_{10}, I_{11}, I_{12}, and I_{13} corresponding to pins 2, 3, 4, 5, 6, 8, 9, 10, and 11, respectively, to select a unique element within a sector.

OUTPUT	PIN	SECTOR	LOCATION
F_0	13	1	0 – 15 Product Terms; AND/OR Arrays
F_1	14	2	16 – 31 Product Terms; AND/OR Arrays
F_2	15	3	32 – 47 Product Terms; AND/OR Arrays
F_3	16	4	Output Active Level Array

Inputs I_1 and I_2, corresponding to pins 22 and 23, are used to enable testing of propagation delay, programming circuitry decoding and output low level characteristics before programming.

Programming current pulses are forced into the output pin, corresponding to a particular sector and routed to the element selected for programming. The elements are sensed at a reduced current level after each programming pulse to determine if programming has occurred.

After all necessary elements are programmed, the array is reverified by scanning the array and resensing all elements directly. Finally, a logical verification is conducted forcing all 2^{14} input states and checking the eight outputs for the correct logic levels.

EFFECTS OF PROGRAMMING (P) OR NOT PROGRAMMING (NP) AN ELEMENT IN EACH OF THE THREE ARRAYS

Output Active Level Array

AL_i	EFFECT ON AN OUTPUT
NP	Output active level will be a LOW for all product terms programmed to the output.
P	Output active level will be a HIGH for all product terms programmed to the output.

Product Term Array

I_k	$\bar{I}_k$	EFFECT ON A PRODUCT TERM
NP	NP	The logic state of the input cannot effect the product term. It is a "don't care" input.
NP	P	Low input becomes an active variable in the product term.
P	NP	High input becomes an active variable in the product term.
P	P	Disables the product term, preventing the product term from ever activating any output.

Summing Array

PT_j	EFFECT ON AN OUTPUT
NP	Output is isolated from the product term unless programmed. Therefore, activation of the product term can not affect the output.
P	Activation of the product term will force the output to its active level.

DATA FORMATS FOR PROGRAMMING

Intersil Inc. can program the IM5200 from data inputs consisting of a truth table, or paper tape. Format specifics follow. If TWX data inputting is used, TWX 910-338-0171. If mailing data input, mail to:

INTERSIL, INCORPORATED
ATTEN: ORDER ENTRY
10710 N. Tantau Avenue
Cupertino, CA 95014

FORMAT INFORMATION SUMMARY

	HAND ENTRY IN TRUTH TABLE FORM	TWX – RCVD AS HARD COPY OR PAPER TAPE	PAPER TAPE
Heading Information	Enter at top of the form as indicated	Enter as per example preceding start of data (STX). The asterisk (*) character may not be used in any heading information	Enter as per example preceding the start of data (STX). The asterisk (*) character may not be used in any heading information
Start of Data	Not required	STX (Control B)	STX (Control B)
Active Level Data Identifier	Not required	*A	*A
Active Level Data Entry	H = High active level L = Low active level	H = High active level L = Low active level	H = High active level L = Low active level
Product Term Number Identifier	Not required	*P	*P
Product Term Number Entry	Preprinted	MSD = Decimal 0-4 LSD = Decimal 0-9	MSD = Decimal 0-4 LSD = Decimal 0-9
Product Term Input Data Identifier	Not required	*I	*I
Product Term Input Data Entry	H = Active high input L = Active low input BLANK = Don't care input	H = Active high input L = Active low input — = Don't care input	H = Active high input L = Active low input — = Don't care input
Summing Data Identifier	Not required	*F	*F
Summing Data Entry	A = Product term is summed by this output BLANK = Product term is not summed by this output	A = Product term is summed by this output — = Product term is not summed by this output	A = Product term is summed by this output — = Product term is not summed by this output
End of Data	Not required	ETX (Control C)	ETX (Control C)
Deactivating a Product Term	Enter D as any input entry for a product term to be deactivated	Enter D as any input entry for a product term to be deactivated	Enter D as any input entry for a product term to be deactivated
Spacing, Carriage Returns, Line Feeds	Not applicable	As needed to give an easily readable appearance in teletype printed form See TWX description for recommended format	Not required unless examination by printout on a teletype is desirable See Paper Tape description for recommended format
Rubouts	Not applicable	May be used to correct errors	May be used to correct errors

TRUTH TABLES

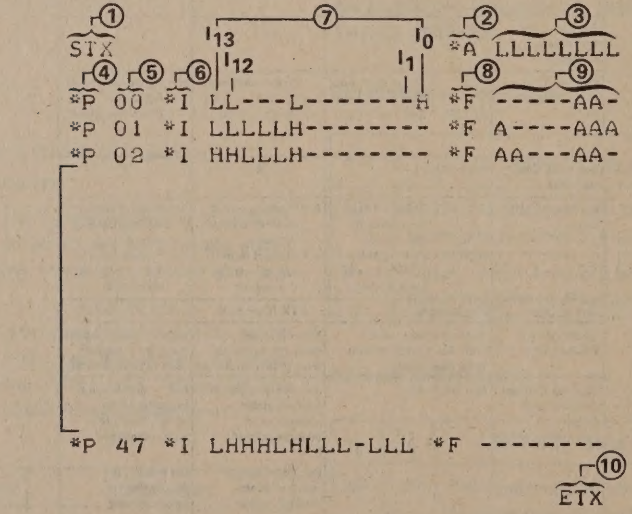
Truth tables can be submitted to Intersil Inc. by mail or by TWX (910-338-0171). A truth table format for mailing is presented as a part of this data sheet. Additional copies of this format are available upon request. The customer should complete all heading information on the format in order to assure that it will remain as a part of the purchase order which is entered.

When entering a truth table by TWX, the following format is recommended so that the data is compatible with the paper tape format. The TWX can, therefore, be received in punched paper tape form for direct processing by a programmer equipped with a paper tape reader input.

TWX FORMAT

```
ATTEN ORDER ENTRY

PO NUMBER 7-706574

BILL TO BRADY ELECTRONICS INC
        1074 SIXTH ST
        SYRACUSE NY 13206

SHIP TP BRADY ELECTRONICS INC
        764 EAST CARLTON
        SYRACUSE NY 13206

TELE (315) 463-5870

TWX 910-377-6402

BUYER HANK RENONE

SHIP AIR EXPRESS

ITEM 01 P/N 706475-001       12 PCS      DELIVERY ASAP


TRUTH TABLE P/N 706475-001
```

START OF DATA



```
STX
                                        *A LLLLLLLL
*P 00 *I LL---L-------H                 *F -----AA-
*P 01 *I LLLLLH--------                 *F A----AAA
*P 02 *I HHLLLH--------                 *F AA---AA-

*P 47 *I LHHHLHLLL-LLL *F --------
                                    ETX
```

EXPLANATION OF NUMBERS

① STX "CONTROL B" ON TELETYPEWRITER

② *A = ACTIVE LEVEL DATA IDENTIFIER CHARACTERS

③ ACTIVE LEVEL DATA (H OR L)

④ *P = PRODUCT TERM NUMBER IDENTIFIER CHARACTERS

⑤ PRODUCT TERM NUMBER

⑥ *I = PRODUCT TERM INPUT DATA IDENTIFIER CHARACTERS

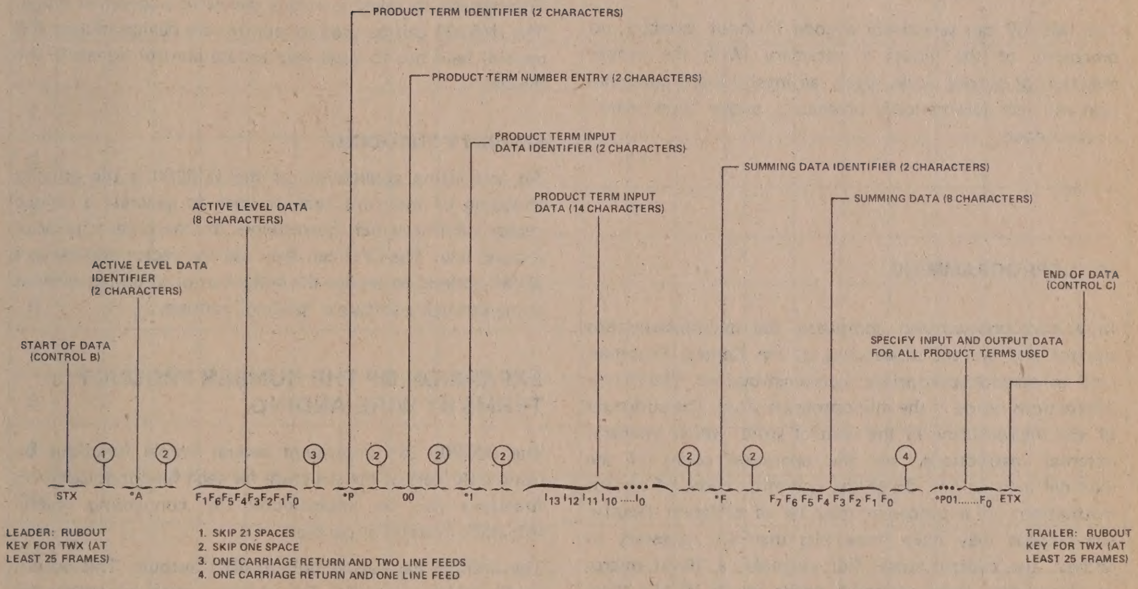
⑦ PRODUCT TERM INPUT DATA (H, L, D OR –)

⑧ *F = SUMMING DATA IDENTIFIER CHARACTERS

⑨ SUMMING DATA (A OR –)

⑩ ETX = "CONTROL C" ON TELETYPEWRITER

TAPE FORMAT


PRODUCT TERM IDENTIFIER (2 CHARACTERS)
PRODUCT TERM NUMBER ENTRY (2 CHARACTERS)
PRODUCT TERM INPUT DATA IDENTIFIER (2 CHARACTERS)
SUMMING DATA IDENTIFIER (2 CHARACTERS)
PRODUCT TERM INPUT DATA (14 CHARACTERS)
SUMMING DATA (8 CHARACTERS)
ACTIVE LEVEL DATA (8 CHARACTERS)
ACTIVE LEVEL DATA IDENTIFIER (2 CHARACTERS)
END OF DATA (CONTROL C)
SPECIFY INPUT AND OUTPUT DATA FOR ALL PRODUCT TERMS USED
START OF DATA (CONTROL B)
1
2
3
2
2
2
2
2
4
STX
*A
F1F6F5F4F3F2F1F0
*P
00
*I
I13 I12 I11 I10 .....I0
*F
F7 F6 F5 F4 F3 F2 F1 F0
*P01.......F0
ETX
LEADER: RUBOUT KEY FOR TWX (AT LEAST 25 FRAMES)
1. SKIP 21 SPACES
2. SKIP ONE SPACE
3. ONE CARRIAGE RETURN AND TWO LINE FEEDS
4. ONE CARRIAGE RETURN AND ONE LINE FEED
TRAILER: RUBOUT KEY FOR TWX (AT LEAST 25 FRAMES)

PAPER TAPE

Teletype 8 level TWX tape can be mailed to Intersil, Inc., Attention: Order Entry. Heading information similar to that used for the TWX truth table format presented above, should be punched on the tape.

The recommended format for the data portion of a paper tape is shown above. Deviations in spacing, carriage returns, line feeds and rubouts are allowed but the start and end characters, the data identifiers, the data characters and the order of data must be strictly followed.

APPLICATIONS

CODE CONVERSION

The IM5200 can be used efficiently in code conversion applications where all possible combinations of a particular code are not used. The conversion from 12 level Hollerith to 8 level ASCII provides such an example. In the standard solution to this problem, the 12 level Hollerith code is first reduced to 8 levels, with logic, before it is presented to a 256 x 8 ROM. All non-existing input combinations must be decoded as "don't care" output states in the ROM.

The IM5200 can selectively decode 14 input variables; no precoding of the inputs is necessary. With the proper selection of output active levels, an invalid input combination will also automatically produce a unique "don't care" or error code.

MICROPROGRAMMING

In a microprogrammed computer, the microinstructions control the correct sequencing of the Central Processor Unit to execute appropriate macroinstructions. The microinstructions reside in the microprogram store. The addresses of the microroutine in the control store, which interpret external instructions, are the operation codes of the external instructions. Since the operation codes of various instructions in a processor may be of different lengths, some codes may have more bits than are necessary to address the control store. For example, a 16-bit microprocessor may have operation codes up to 16 bits long. However, the microprocessor store may have only 256 words of memory.

The IM5200 can be conveniently used to translate an arbitrary operation code to obtain the proper control store address. The IM5200 can also be used in the control store to minimize the size of the microprogram memory by utilizing the unique capability of the device to cope with special address combinations — "don't care" bits in addresses, a single address for multiple words and multiple addresses for single words.

SEQUENTIAL CONTROL

The IM5200 can be used effectively in sequencing applications to implement flow charts of state diagrams, condition driven look up tables or arbitrary state sequencers. The IM5200 input set could come from external control points ("qualifying inputs") or the IM5200 outputs coupled through feed-back latches ("current state inputs").

PERIPHERAL DEVICE CONTROL

For a Central Processor Unit to communicate with a peripheral device, the CPU must select the device and the mode of communication. During an Input-Output instruction, the CPU transmits the device address and control information to select a unique device in a specified mode. The IM5200 can be used to monitor the device address and control field bus to issue appropriate control signals to the devices.

PRIORITY ENCODING

An interesting application of the IM5200 is the priority encoding of interrupt request lines to generate a unique vector address which corresponds to the highest priority request line. The CPU can then use the vector address as a JUMP address to service the highest priority device without going through a software "polling" routine.

EXPANSION OF THE NUMBER PRODUCT TERMS BY WIRE-ANDING

The IM5200 can implement several simple functions by using only part of the structure for each function. Complex functions can be implemented by connecting several IM5200's in series or parallel.

The IM5200 has passive pull-up (4K) outputs. This output configuration is useful for product term expansion by wire-ANDing the outputs of different IM5200's. For EPLA applications, expansion by wire-ANDing is preferrable to the conventional chip select approach, since in many applications, it is difficult to generate the chip select signal, in view of the fact that "chip select" decision may itself be based on a random combination of the input variables.

Active LOW is the necessary active state for the outputs that must be wire-ANDed. It must be noted that the fan-out of the wire-ANDed outputs is reduced by approximately one standard TTL load for each IM5200 output that is tied together.

COMPANY ______________________

ADDRESS ______________________

____

PHONE ______________________

DATE	Page of
CUSTOMER P.O. No.	
CUSTOMER PRINT OR I.D. No.	

IM5200
TRUTH TABLE

ACTIVE LEVEL DATA	H = High Active Level L = Low Active Level	PRODUCT TERM INPUT DATA	H = Active High Input L = Active Low Input Blank = Don't Care Input	SUMMING DATA	A = Product Term is Summed by This Output Blank - Product Term is Not Summed by this Output

ACTIVE LEVEL DATA							
F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0

	PRODUCT TERM INPUT DATA															SUMMING DATA							
	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
	PIN 11	PIN 10	PIN 9	PIN 8	PIN 7	PIN 6	PIN 5	PIN 4	PIN 3	PIN 2	PIN 1	PIN 23	PIN 22	PIN 21		PIN 20	PIN 19	PIN 18	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13
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ACTIVE LEVEL DATA	H = High Active Level L = Low Active Level	PRODUCT TERM INPUT DATA	H = Active High Input L = Active Low Input Blank = Don't Care Input	SUMMING DATA	A = Product Term is Summed by This Output Blank - Product Term is Not Summed by this Output

ACTIVE LEVEL DATA							
F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0

	PRODUCT TERM INPUT DATA														SUMMING DATA							
	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
	PIN 11	PIN 10	PIN 9	PIN 8	PIN 7	PIN 6	PIN 5	PIN 4	PIN 3	PIN 2	PIN 1	PIN 23	PIN 22	PIN 21	PIN 20	PIN 19	PIN 18	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13
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INTERSIL

IM5600/IM5610
256 Bit Bipolar Read Only Memory

FEATURES

- **Uses Patented AIM Programming Element for**
  - **— Superior Reliability**
  - **— High Programming Yield**
  - **— Fast Programming Speed < 1 sec**
  - **— TTL Processing Compatibility**
- **Low Power Consumption 1.5 mW/bit**
- **Operating Speed**
  - **— Address to Output — 50nS**
  - **— Chip Enable to Output — 40nS**
- **Large Output Drive — 16mA @ 0.45V**
- **TTL Compatible Inputs & Outputs**
- **Two Output Designs**
  - **— 5600 Open Collector**
  - **— 5610 Active Pull-up**
- **Chip Enable Facilitates Memory Expansion and Use in Bus Organized Systems**

APPLICATIONS

- **Code Conversion**
- **Logic Implementation**
- **Microprogramming**
- **Look-up Tables**
- **Control of Sequential Circuits**
- **Character Generation**

GENERAL DESCRIPTION

The Intersil IM5600 and IM5610 are high speed, electrically programmable, fully decoded, bipolar 256 bit read only memories organized as 32 words by 8 bits. On-chip address decoding, chip enable input and uncomitted collector or three-state outputs provide for simplified memory expansion and use in bus organized systems.

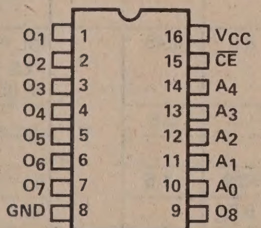
Unprogrammed AIM elements are sensed as ZERO's or low logic levels at the outputs. Programming with a commercially available programmer irreversibly converts selected elements in the array so that they are sensed as ONE's or high logic levels.

The following companies make programmers approved by Intersil:

1. Data I/O Corp., P.O. Box 1603, Bellevue, Wash. 98009
2. PRO-LOG Corp., 2411 Garden Rd., Monterey, CA 93940

Detailed programming specifications for all Intersil PROMs are presented in the Intersil BIPOLAR PROM PROGRAMMING SPECIFICATION Data Sheet.

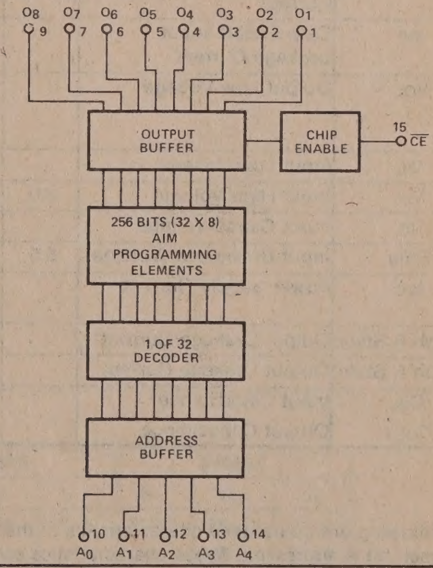
CONNECTION DIAGRAM



TOP VIEW

(outline dwgs JE, PE)

BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
IM5600	16 Pin Flatpack	0°C to +75°C Commercial −55°C to +125°C Military	IM5600CFE IM5600MFE*
	16 Pin Plastic DIP	0°C to +75°C	IM5600CPE
	16 Pin Cerdip DIP	0°C to +75°C Commercial −55°C to +125°C Military	IM5600CJE IM5600MJE*
IM5610	16 Pin Flatpack	0°C to +75°C Commercial −55°C to +125°C Military	IM5610CFE IM5610MFE*
	16 Pin Plastic DIP	0°C to +75°C	IM5610CPE
	16 Pin Cerdip DIP	0°C to +75° C Commercial −55°C to +125°C Military	IM5610CJE IM5610MJE*

* If 883B processing is desired add /883B to order number.

TRUTH TABLE

ADDRESS INPUTS A_0–A_4	$\overline{CE}$	ANY OUTPUT O_1–O_8
Any one of 32 possible addresses.	L	H—if the bit uniquely associated with this output and address has been electrically programmed. L—if it has not been programmed.
Any one of 32 possible addresses.	H	All outputs are forced to a high impedance state regardless of the address.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +7.0V
Input Voltage Applied .... −1.5V to +5.5V
Output Voltage Applied .... −0.5V to +V_{CC}
Output Voltage Applied (Programming Only) 28V
Current Into Output (Programming Only) .... 210 mA
Storage Temperature .... −65°C to +150°C
Operating Temperature Range*
(IM5600C and IM5610C) .... 0°C to +75°C
(IM5600M and IM5610M) .... −55°C to +125°C

*Operating temperature is defined as ambient temperature for the DIP and case temperature for the flatpack. Case temperature is measured directly below the die.

DC CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V ±5% T = 0°C to +75°C			LIMITS V_{CC} = 5.0V ±10% T = −55°C to +125°C			UNITS	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
I_{FA}	Address Input Load Current		−0.63	−1.0		−0.63	−1.0	mA	$V_A = 0.4V$
I_{FE}	Chip Enable Input Load Current		−0.63	−1.0		−0.63	−1.0		$V_{\overline{CE}} = 0.4V$
I_{RA}	Address Input Leakage Current		5.0	40		5.0	60	µA	$V_A = 4.5V$
I_{RE}	Chip Enable Input Leakage Current		5.0	40		5.0	60		$V_{\overline{CE}} = 4.5V$
V_{OL}	Output Low Voltage		0.3	0.45		0.3	0.45	V	$I_{OL} = 16$ mA $V_{CE} = 0.4V$ '0' bit is addressed.
V_{IL}	Input Low Voltage			0.8			0.8		
V_{IH}	Input High Voltage	2.0			2.0				
V_C	Input Clamp Voltage		−0.9	−1.5		−0.9	−1.5		$I_{IN} = -10$ mA
BV_{IN}	Input Breakdown Voltage	5.5	6.5		5.5	6.5			$I_{IN} = 1.0$ mA
I_{CC}	Power Supply Current		75	100		75	100	mA	Inputs Either Open or at Ground
I_O (High R State)	Output Leakage Current		<1.0	40		<1.0	100	µA	$V_O = 5.5V$, $V_{CE} = 2.4V$
I_O (High R State)	Output Leakage Current		<−1.0	−40		<−1.0	−100		$V_O = 0.4V$, $V_{CE} = 2.4V$
C_{IN}	Input Capacitance		5.0			5.0		pF	$V_{IN} = 2.0V$, $V_{CC} = 0V$
C_{OUT}	Output Capacitance		7.0			7.0			$V_O = 2.0V$, $V_{CC} = 0V$

The following are guaranteed characteristics of the output high level state when the chip is enabled ($\overline{CE}$ = 0.4V) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.

I_{OLK}	Output Leakage Current		<1.0	100		<1.0	100	µA	$V_O = 5.5V$, $V_{\overline{CE}} = 0.4V$
V_{OH} (IM5610)	Output High Voltage	2.4	3.2		2.4	3.2		V	$I_{OH} = -1.0$ mA (IM5610M) $I_{OH} = -2.4$ mA (IM5610C)
I_{SC} (IM5610)	Output Short Circuit	−15	−30	−60	−15	−30	−60	mA	$V_O = 0V$

NOTE 1: Typical characteristics are for V_{CC} = 5.0V, T_A = 25°C.

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LIMITS V_{CC} = 5V T_A = 25°C		LIMITS V_{CC} = 5V ±5% T_A = 0°C to +75°C		LIMITS V_{CC} = 5V ±10% T_A = −55°C to +125°C		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{aa}	Address Access Time	20	50	20	65	20	75	ns
t_{dis}	Output Disable Time*	10	40	10	50	10	60	
t_{en}	Output Enable Time*	5	40	5	50	5	60	

* Output disable time is the time taken for the output to reach a high resistance state when the chip enable is taken high. Output enable time is the time taken for the output to become active when the chip enable is taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

SWITCHING WAVEFORMS

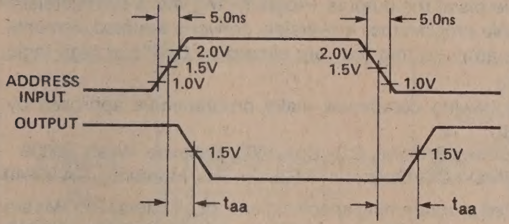

5.0ns
5.0ns
2.0V
1.5V
1.0V
2.0V
1.5V
1.0V
ADDRESS INPUT
OUTPUT
1.5V
1.5V
t_{aa}
t_{aa}

FIGURE 1: Access Time Via Address Input

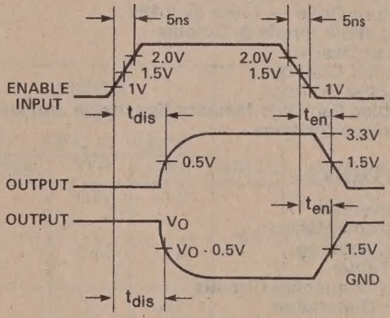
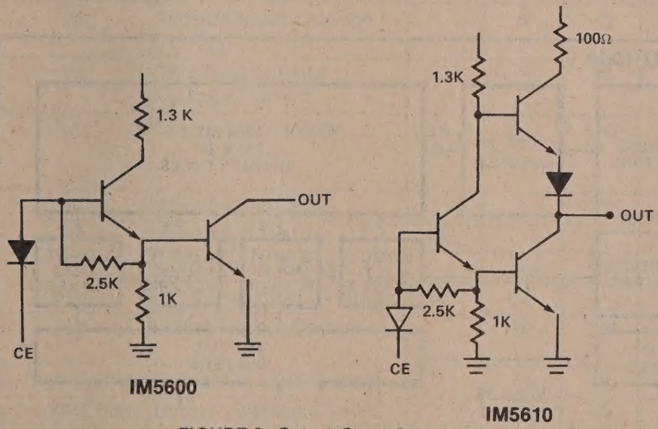

5ns
5ns
2.0V
1.5V
1V
2.0V
1.5V
1V
ENABLE INPUT
t_{dis}
t_{en}
3.3V
0.5V
1.5V
OUTPUT
t_{en}
OUTPUT
V_O
V_O - 0.5V
1.5V
GND
t_{dis}

FIGURE 2: Output Disable And Enable Time


1.3 K
OUT
2.5K
1K
CE
100Ω
1.3K
OUT
2.5K
1K
CE

IM5600

IM5610

FIGURE 3: Output Stage Schematics

SWITCHING TIME TEST CONDITIONS

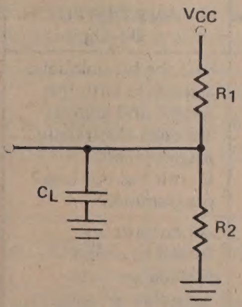


FIGURE 4: Output Load Circuit

SWITCHING PARAMETER	IM5600			IM5610		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{aa}	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF
t_{dis} '1'	∞	3.3 KΩ	10 pF	∞	600Ω	10 pF
t_{dis} '0'	300Ω	600Ω	10 pF	300Ω	600Ω	10 pF
t_{en} '1'	∞	3.3 KΩ	30 pF	∞	600Ω	30 pF
t_{en} '0'	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF

INPUT CONDITIONS

Amplitude — 0V to 3V
Rise and Fall Time — 5 ns From 1V to 2V
Frequency — 1 MHz

INTERSIL

IM5603/IM5623
Electrically Programmable 1024 Bit Bipolar Read Only Memory

FEATURES

- Uses Patented AIM Programming Element for
  - Superior Reliability
  - High Programming Yield
  - Fast Programming Speed < 1 sec
  - TTL Processing Compatibility
- Low Power Consumption 439 μW/bit
- Operating Speed
  - Address to Output — 60nS
  - Chip Enable to Output — 35nS
- Large Output Drive — 16mA @ 0.45V
- TTL Compatible Inputs & Outputs
- Two Output Designs
  - 5603 Open Collector
  - 5623 Active Pull-up
- Chip Enables Facilitate Memory Expansion and Use in Bus Organized Systems

APPLICATIONS

- Code Conversion
- Logic Implementation
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits
- Character Generation

GENERAL DESCRIPTION

The Intersil IM5603 and IM5623 are high speed, electrically programmable, fully decoded, bipolar 1024 bit read only memories organized as 256 words by 4 bits. On-chip address decoding, chip enable inputs and uncomitted collector or three-state outputs provide for simplified memory expansion and use in bus organized systems.

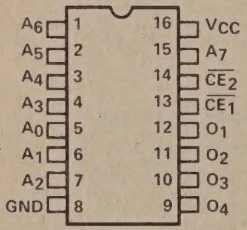
Unprogrammed AIM elements are sensed as ZERO's or low logic levels at the outputs. Programming with a commercially available programmer irreversibly converts selected elements in the array so that they are sensed as ONE's or high logic levels.

The following companies make programmers approved by Intersil:

1. Data I/O Corp., P.O. Box 1603, Bellevue, Wash. 98009
2. PRO-LOG Corp., 2411 Garden Rd., Monterey, CA 93940

Detailed programming specifications for all Intersil PROMs are presented in the Intersil BIPOLAR PROM PROGRAMMING SPECIFICATION Data Sheet.

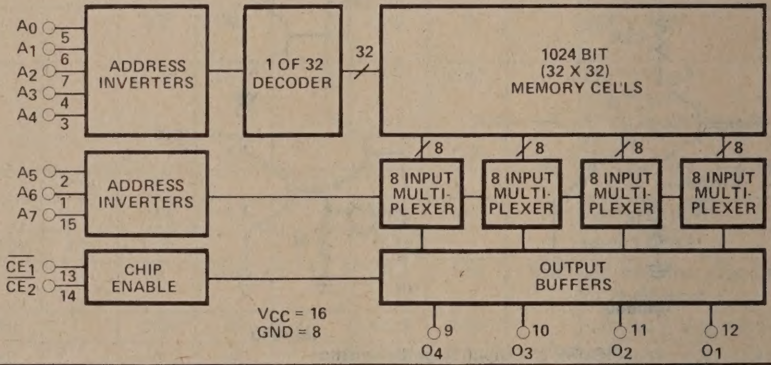
PIN CONFIGURATION



A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 $\overline{CE}_2$
13 $\overline{CE}_1$
12 O1
11 O2
10 O3
9 O4

TOP VIEW
(outline dwgs JE, PE, flatpak outline dwg FE)

BLOCK DIAGRAM



A0 5
A1 6
A2 7
A3 4
A4 3
ADDRESS INVERTERS
1 OF 32 DECODER
32
1024 BIT (32 X 32) MEMORY CELLS
8
8
8
8
A5 2
A6 1
A7 15
ADDRESS INVERTERS
8 INPUT MULTI-PLEXER
8 INPUT MULTI-PLEXER
8 INPUT MULTI-PLEXER
8 INPUT MULTI-PLEXER
$\overline{CE}_1$ 13
$\overline{CE}_2$ 14
CHIP ENABLE
OUTPUT BUFFERS
VCC = 16
GND = 8
9 O4
10 O3
11 O2
12 O1

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
IM5603	16 Pin Flatpack	0°C to +75°C Commercial −55°C to +125°C Military	IM5603CFE IM5603MFE*
	16 Pin Plastic DIP	0°C to +75°C	IM5603CPE
	16 Pin Cerdip DIP	0°C to +75°C Commercial −55°C to +125°C Military	IM5603CJE IM5603MJE*
IM5623	16 Pin Flatpack	0°C to +75°C Commercial −55°C to +125°C Military	IM5623CFE IM5623MFE*
	16 Pin Plastic DIP	0°C to +75°C	IM5623CPE
	16 Pin Cerdip DIP	0°C to +75° C Commercial −55°C to +125°C Military	IM5623CJE IM5623MJE*

* If 883B processing is desired add /883B to order number.

TRUTH TABLE

ADDRESS INPUTS A_0-A_7	CHIP ENABLE INPUTS $\overline{CE}_1$	$\overline{CE}_2$	ANY OUTPUT O_1-O_4
Any one of 256 possible addresses	L	L	H-if the bit uniquely associated with this output and address has been electrically programmed. L-if it has not been programmed.
Any one of 256 possible addresses	H X	X H	All outputs are forced to a high impedance state regardless of address.

X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +7.0V
Input Voltage Applied .... −1.5V to 5.5V
Output Voltage Applied .... −0.5V to +V_{CC}
Output Voltage Applied (Programming Only) 28V
Current Into Output (Programming Only) .... 210 mA
Storage Temperature .... −65° C to +150° C
Operating Temperature Range*
(IM5603C and IM5623C) .... 0° C to +75° C
(IM5603M and IM5623M) .... −55° C to +125° C

*Operating temperature is defined as ambient temperature for the DIP and case temperature for flatpack. Case temperature is measured directly below the die.

DC CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V ±5% T = 0°C to +75°C			LIMITS V_{CC} = 5.0V ±10% T = −55°C to +125°C			UNITS	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
I_{FA}	Address Input Load Current		0.63	−1.0		−0.63	−1.0	mA	V_A = 0.4V
I_{FE}	Chip Enable Input Load Current		−0.63	−1.0		−0.63	−1.0		V_{CE} = 0.4V
I_{RA}	Address Input Leakage Current		5	40		5	60	µA	V_A = 4.5V
I_{RE}	Chip Enable Input Leakage Current		5	40		5	60		V_{CE} = 4.5V
V_{OL}	Output Low Voltage		0.3	0.45		0.3	0.45	V	I_{OL} = 16 mA, $V_{\overline{CE1}} = V_{\overline{CE2}}$ = 0.4V '0' bit is addressed.
V_{IL}	Input Low Voltage			0.8			0.8		
V_{IH}	Input High Voltage	2.0			2.0				
V_C	Input Clamp Voltage		−0.9	−1.5		−0.9	−1.5		I_{IN} = −10 mA
BV_{IN}	Input Breakdown Voltage	5.5	6.5		5.5	6.5			I_{IN} = 1.0 mA
I_{CC}	Power Supply Current		90	130		90	130	mA	Inputs Either Open or at Ground
I_O (High R State)	Output Leakage Current		<1	40		<1	100	µA	V_O = 5.5V, $V_{\overline{CE1}}$ or
I_O (High R State)	Output Leakage Current		<−1	−40		<−1	−100		V_O = 0.4V, $V_{\overline{CE2}}$ = 2.4V
C_{IN}	Input Capacitance		5			5		pF	V_{IN} = 2.0V, V_{CC} = 0V
C_{OUT}	Output Capacitance		7			7			V_O = 2.0V, V_{CC} = 0V

The following are guaranteed characteristics of the output high level state when the chip is enabled ($\overline{CE1}$ and $\overline{CE2}$ = 0.4V) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.

I_{OLK}	Output Leakage Current		<1	100		<1	100	µA	V_O = 5.5V
V_{OH} (IM5603)	Output High Voltage	2.4	3.3		2.4	3.3		V	I_{OH} = −0.4 mA
V_{OH} (IM5623)	Output High Voltage	2.4	3.2		2.4	3.2			I_{OH} = −2.4 mA (IM5623C) I_{OH} = −1.0 mA (IM5623M)
I_{SC} (IM5603)	Output Short Circuit Current	−1.0	−3.0	−6.0	−1.0	−3.0	−6.0	mA	V_O = 0V
I_{SC} (IM5623)	Output Short Circuit Current	−15	−30	−60	−15	−30	−60		V_O = 0V

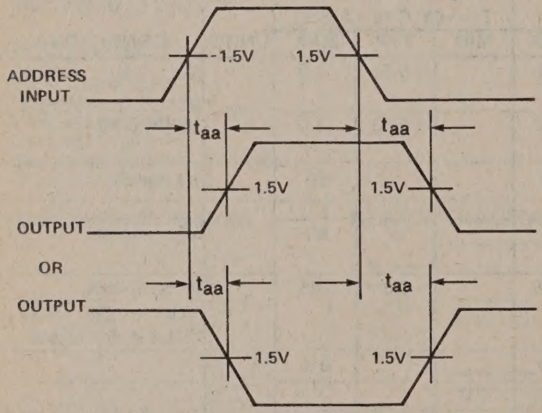
NOTE: Typical characteristics are for V_{CC} = 5.0V T_A = 25° C.

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS VCC = 5.0V TA = 25°C MIN	MAX	LIMITS VCC = 5.0V ±5% TA = 0°C to +75°C MIN	MAX	LIMITS VCC = 5.0V ±10% TA = -55°C to +125°C MIN	MAX	UNITS
t_{aa}	Access Time (Via Address Inputs) (See Figure 1)	20	60	20	70	20	80	ns
t_{dis}	Output Disable Time* (See Figure 2)	10	35	10	50	10	60	
t_{en}	Output Enable Time* (See Figure 2)	5	35	5	50	5	60	

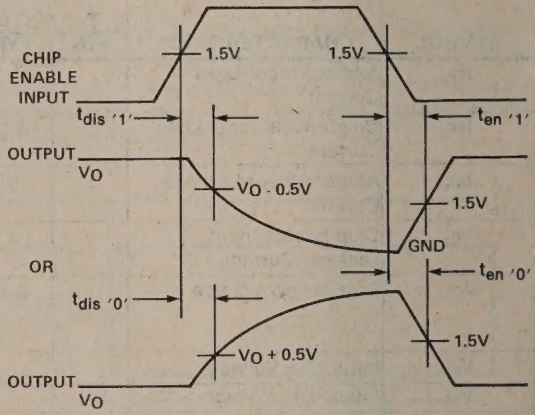
***NOTE:** Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

SWITCHING WAVEFORMS



ADDRESS INPUT
1.5V
1.5V
t_{aa}
t_{aa}
1.5V
1.5V
OUTPUT
OR
t_{aa}
t_{aa}
OUTPUT
1.5V
1.5V

FIGURE 1: Access Time Via Address Inputs



CHIP ENABLE INPUT
1.5V
1.5V
t_{dis} '1'
t_{en} '1'
OUTPUT
VO
VO - 0.5V
1.5V
GND
OR
t_{en} '0'
t_{dis} '0'
VO + 0.5V
1.5V
OUTPUT
VO

FIGURE 2: Output Enable And Disable Times

SWITCHING TIME TEST CONDITIONS

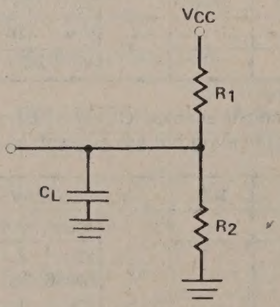


FIGURE 3: Output Load Circuit

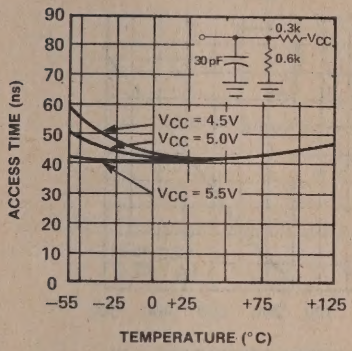
SWITCHING PARAMETER	IM5603 R1	R2	CL	IM5623 R1	R2	CL
t_{aa}	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF
t_{dis} '1'	∞	3.3 KΩ	10 pF	∞	600Ω	10 pF
t_{dis} '0'	300Ω	600Ω	10 pF	300Ω	600Ω	10 pF
t_{en} '1'	∞	3.3 KΩ	30 pF	∞	600Ω	30 pF
t_{en} '0'	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF

INPUT CONDITIONS

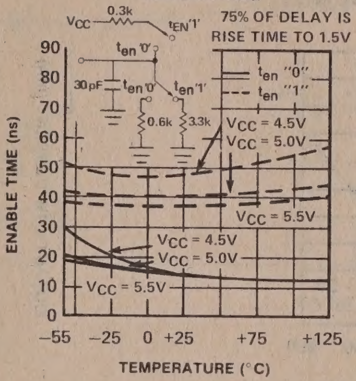
Amplitude — 0V to 3V
Rise and Fall Time — 5 ns From 1V to 2V
Frequency — 1 MHz

TYPICAL SWITCHING CHARACTERISTICS

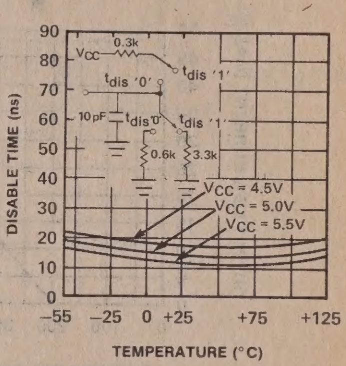
IM5603 ADDRESS TO OUTPUT ACCESS DELAY (TAA) VS TEMPERATURE



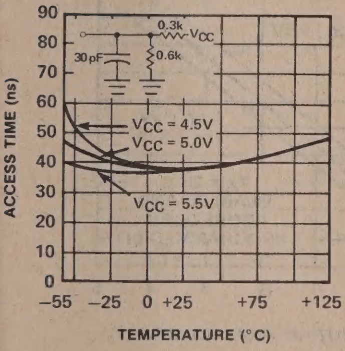
IM5603 CHIP ENABLE TO OUTPUT ACCESS DELAY (tEN) VS TEMPERATURE



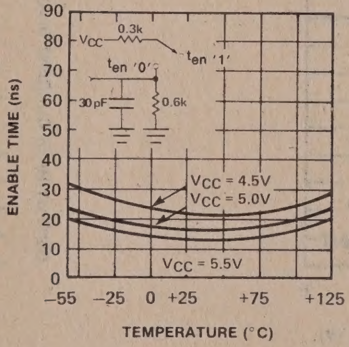
IM5603 CHIP ENABLE TO OUTPUT DISABLE TIME DELAY (tDIS) VS TEMPERATURE



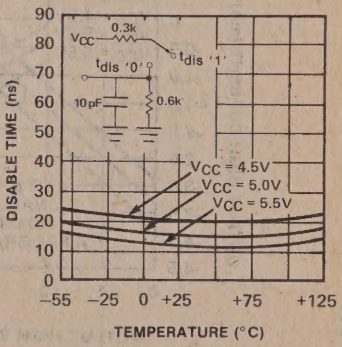
IM5623 ADDRESS TO OUTPUT ACCESS DELAY (tAA) VS TEMPERATURE



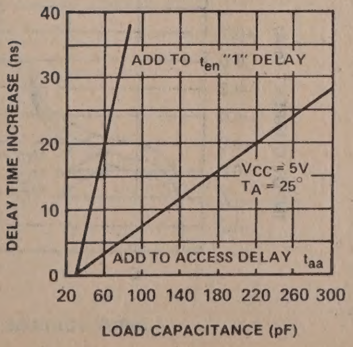
IM5623 CHIP ENABLE TO OUTPUT ACCESS DELAY (tEN) VS TEMPERATURE



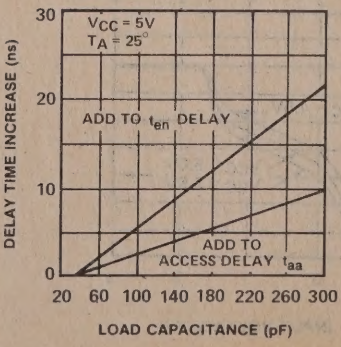
IM5623 CHIP ENABLE TO OUTPUT DISABLE TIME DELAY (tDIS) VS TEMPERATURE



IM5603 DELAY INCREASE WITH LOAD CAPACITANCE

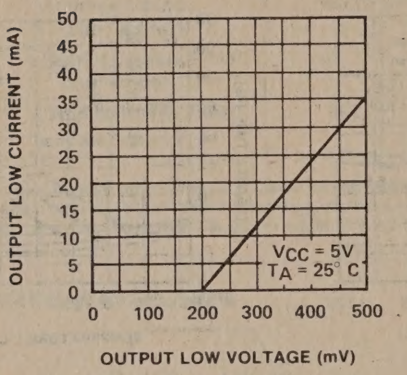


IM5623 DELAY INCREASE WITH LOAD CAPACITANCE

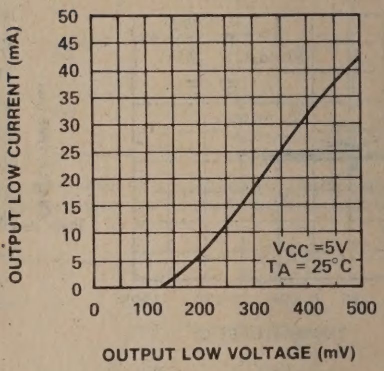


TYPICAL DC CHARACTERISTICS

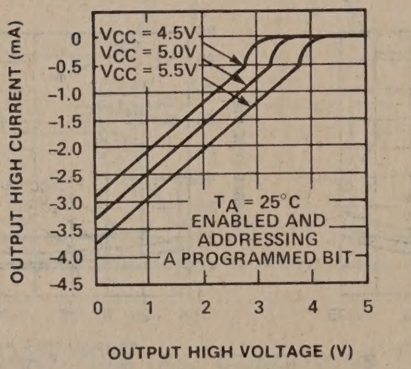
IM5603 OUTPUT LOW CURRENT (I_{OL})
VS OUTPUT LOW VOLTAGE (V_{OL})



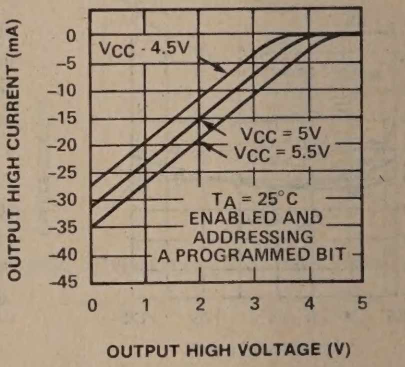
IM5623 OUTPUT LOW CURRENT (I_{OL})
VS OUTPUT LOW VOLTAGE (V_{OL})



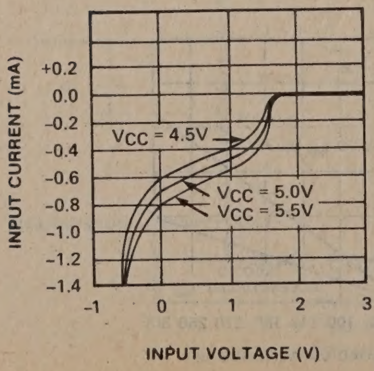
IM5603 OUTPUT HIGH CURRENT (I_{OH})
VS OUTPUT HIGH VOLTAGE (V_{OH})



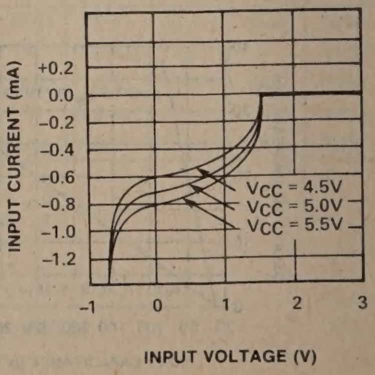
IM5623 OUTPUT HIGH CURRENT (I_{OH})
VS OUTPUT HIGH VOLTAGE (V_{OH})



IM5603 OR IM5623 CHIP ENABLE INPUT
CURRENT VS INPUT VOLTAGE

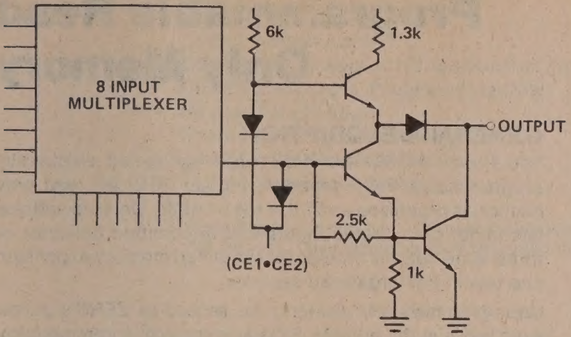


IM5603 OR IM5623 ADDRESS INPUT
CURRENT VS INPUT VOLTAGE

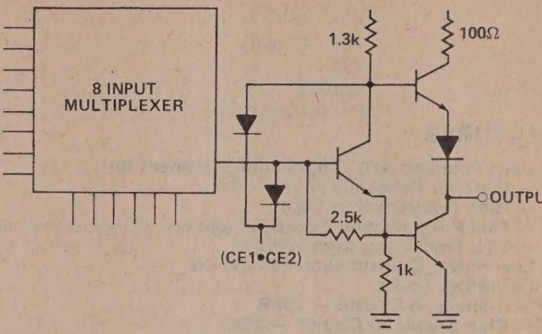


OUTPUT STAGE SCHEMATICS

IM5603


8 INPUT MULTIPLEXER
6k
1.3k
OUTPUT
2.5k
(CE1•CE2)
1k

IM5623


8 INPUT MULTIPLEXER
1.3k
100Ω
OUTPUT
2.5k
(CE1•CE2)
1k

INTERSIL

IM5604/IM5624
2048 Bit Bipolar Programmable Read Only Memory

FEATURES

- Uses Patented AIM Programming Element for
  - Superior Reliability
  - High Programming Yield
  - Fast Programming Speed < 1 sec
  - TTL Processing Compatibility
- Low Power Consumption 244 μW/bit
- Operating Speed
  - Address to Output — 70nS
  - Chip Enable to Output — 35nS
- Large Output Drive — 16mA @ 0.45V
- TTL Compatible Inputs & Outputs
- Two Output Designs
  - 5604 Open Collector
  - 5624 Active Pull-up
- Chip Enable Facilitates Memory Expansion and Use in Bus Organized Systems

APPLICATIONS

- Code Conversion
- Logic Implementation
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits
- Character Generation

GENERAL DESCRIPTION

The Intersil IM5604 and IM5624 are high speed, electrically programmable, fully decoded, bipolar 2048 bit read only memories organized as 512 words by 4 bits. On-chip address decoding, chip enable inputs and uncomitted collector or three-state outputs provide for simplified memory expansion and use in bus organized systems.

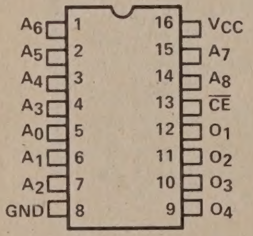
Unprogrammed AIM elements are sensed as ZERO's or low logic levels at the outputs. Programming with a commercially available programmer irreversibly converts selected elements in the array so that they are sensed as ONE's or high logic levels.

The following companies make programmers approved by Intersil:

1. Data I/O Corp., P.O. Box 1603, Bellevue, Wash. 98009
2. PRO-LOG Corp., 2411 Garden Rd., Monterey, CA 93940

Detailed programming specifications for all Intersil PROMs are presented in the Intersil BIPOLAR PROM PROGRAMMING SPECIFICATION DATA SHEET.

CONNECTION DIAGRAM

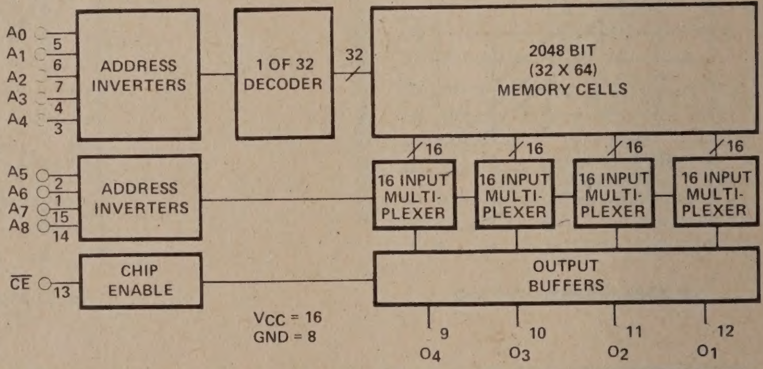


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 A8
13 $\overline{CE}$
12 O1
11 O2
10 O3
9 O4

TOP VIEW

(outline dwgs JE, PE)

BLOCK DIAGRAM



A0 5
A1 6
A2 7
A3 4
A4 3
ADDRESS INVERTERS
1 OF 32 DECODER
32
2048 BIT (32 X 64) MEMORY CELLS
16
16
16
16
A5 2
A6 1
A7 15
A8 14
ADDRESS INVERTERS
16 INPUT MULTI-PLEXER
16 INPUT MULTI-PLEXER
16 INPUT MULTI-PLEXER
16 INPUT MULTI-PLEXER
$\overline{CE}$ 13
CHIP ENABLE
OUTPUT BUFFERS
VCC = 16
GND = 8
9 O4
10 O3
11 O2
12 O1

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
IM5604	16 Pin Flatpack	0°C to +75°C −55°C to +125°C Military	IM5604CFE IM5604MFE*
	16 Pin Cerdip DIP	0°C to +75°C Commercial −55°C to +125°C Military	IM5604CJE IM5604MJE*
	16 Pin Plastic DIP	0°C to +75°C	IM5604CPE
IM5624	16 Pin Flatpack	0°C to +75°C Commercial −55°C to +125°C Military	IM5624CFE IM5624MFE*
	16 Pin Plastic DIP	0°C to +75°C −55°C to +125°C Military	IM5624CJE IM5610MJE*
	16 Pin Plastic DIP	0°C to +75° C	IM5624CPE

* If 883B processing is desired add /883B to order number.

TRUTH TABLE

ADDRESS INPUTS A0 — A8	$\overline{CE}$	ANY OUTPUT O1 — O4
Any one of 512 possible addresses	L	H — if the bit uniquely associated with this output and address has been electrically programmed. L — if it has not been programmed.
Any one of 512 possible addresses	H	All outputs are forced to a high impedance state regardless of the address.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input Voltage Applied	−1.5V to +5.5V
Output Voltage Applied	−0.5V to $+V_{CC}$
Output Voltage Applied (Programming Only)	28V
Current Into Output (Programming Only)	210 mA
Storage Temperature	−65°C to +150°C
Operating Temperature Range*	
(IM5604C and IM5624C)	0°C to +75°C
(IM5604M and IM5624M)	−55°C to +125°C

*Operating temperature is defined as ambient temperature for the DIP and case temperature for the flatpack. Case temperature is measured directly below the die.

DC CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V ±5% T = 0°C to +75°C MIN	TYP	MAX	LIMITS V_{CC} = 5.0V ±10% T = −55°C to +125°C MIN	TYP	MAX	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−0.63	−1.0		−0.63	−1.0	mA	V_A = 0.4V
I_{FE}	Chip Enable Input Load Current		−0.63	−1.0		−0.63	−1.0		$V_{\overline{CE}}$ = 0.4V
I_{RA}	Address Input Leakage Current		5.0	40		5.0	60	μA	V_A = 4.5V
I_{RE}	Chip Enable Input Leakage Current		5.0	40		5.0	60		$V_{\overline{CE}}$ = 4.5V
V_{OL}	Output Low Voltage		0.3	0.45		0.3	0.45	V	I_{OL} = 16 mA $V_{\overline{CE}}$ = 0.4V '0' bit is addressed.
V_{IL}	Input Low Voltage			0.8			0.8		
V_{IH}	Input High Voltage	2.0			2.0				
V_C	Input Clamp Voltage		−0.9	−1.5		−0.9	−1.5		I_{IN} = −10 mA
BV_{IN}	Input Breakdown Voltage	5.5	6.5		5.5	6.5			I_{IN} = 1.0 mA
I_{CC}	Power Supply Current		100	140		100	140	mA	Inputs Either Open or at Ground
I_O (High R State)	Output Leakage Current		<1.0	40		<1.0	100	μA	V_O = 5.5V, $V_{\overline{CE}}$ = 2.4V
I_O (High R State)	Output Leakage Current		<−1.0	−40		<−1.0	−100		V_O = 0.4V, $V_{\overline{CE}}$ = 2.4V
C_{IN}	Input Capacitance		5.0			5.0		pF	V_{IN} = 2.0V, V_{CC} = 0V
C_{OUT}	Output Capacitance		7.0			7.0			V_O = 2.0V, V_{CC} = 0V

The following are guaranteed characteristics of the output high level state when the chip is enabled ($\overline{CE}$ = 0.4V) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.

I_{OLK}	Output Leakage Current		<1.0	100		<1.0	100	μA	V_O = 5.5V, $V_{\overline{CE}}$ = 0.4V
V_{OH} (IM5604)	Output High Voltage	2.4	3.3		2.4	3.3		V	I_O = −0.4 mA
V_{OH} (IM5624)	Output High Voltage	2.4	3.2		2.4	3.2			I_O = −1.0 mA (IM5624M) I_O = −2.4 mA (IM5624C)
I_{SC} (IM5604)	Output Short Circuit Current	−1.0	−3.0	−6.0	−1.0	−3.0	−6.0	mA	V_O = 0V
I_{SC} (IM5624)	Output Short Circuit Current	−15	−30	−60	−15	−30	−60		V_O = 0V

NOTE: Typical characteristics are for V_{CC} = 5.0V, T_A = 25°C.

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5V T_A = 25°C MIN	MAX	LIMITS V_{CC} = 5V ±5% T_A = 0°C to 70°C MIN	MAX	LIMITS V_{CC} = 5V ±10% T_A = −55°C to +125°C MIN	MAX	UNITS
t_{aa}	Access Time (Via Address Inputs) (See Figure 1)	20	70	20	80	20	90	ns
t_{dis}	Output Disable Time* (See Figure 2)	10	35	10	50	10	60	
t_{en}	Output Enable Time* (See Figure 2)	5	35	5	50	5	60	

***NOTE:** Output disable time is the time for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

SWITCHING WAVEFORMS

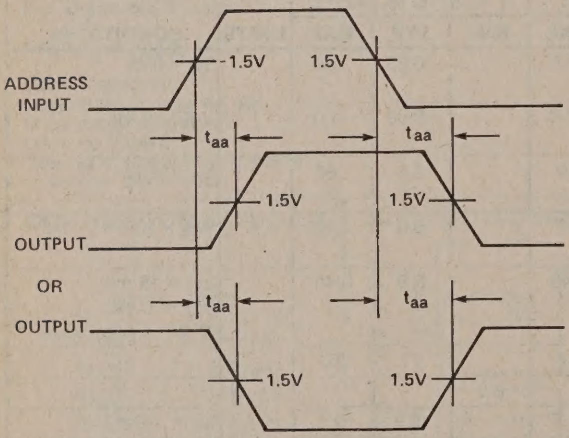

ADDRESS INPUT
1.5V
1.5V
t_{aa}
t_{aa}
OUTPUT
1.5V
1.5V
OR
t_{aa}
t_{aa}
OUTPUT
1.5V
1.5V

FIGURE 1: Access Time Via Address Inputs

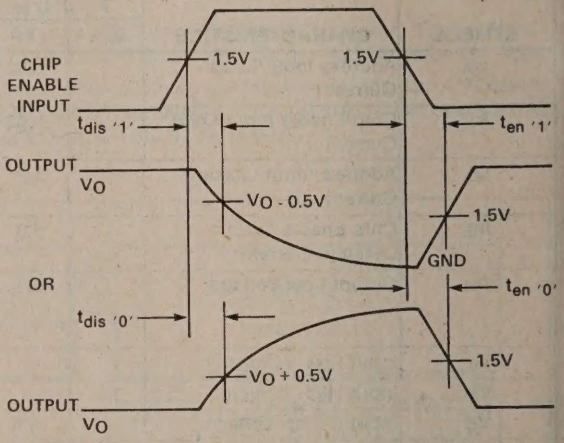

CHIP ENABLE INPUT
1.5V
1.5V
t_{dis} '1'
t_{en} '1'
OUTPUT
V_O
V_O - 0.5V
1.5V
GND
OR
t_{en} '0'
t_{dis} '0'
V_O + 0.5V
1.5V
OUTPUT
V_O

FIGURE 2: Output Enable And Disable Times

SWITCHING TIME TEST CONDITIONS

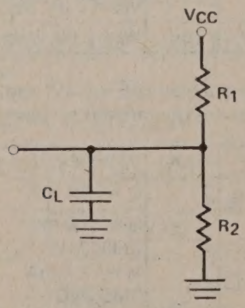


FIGURE 3: Output Load Circuit

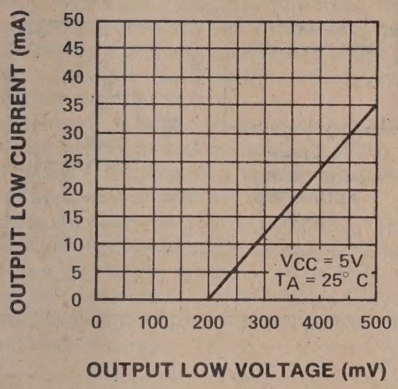
SWITCHING PARAMETER	IM5604 R_1	IM5604 R_2	IM5604 C_L	IM5624 R_1	IM5624 R_2	IM5624 C_L
t_{aa}	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF
t_{dis} '1'	∞	3.3 KΩ	10 pF	∞	600Ω	10 pF
t_{dis} '0'	300Ω	600Ω	10 pF	300Ω	600Ω	10 pF
t_{en} '1'	∞	3.3 KΩ	30 pF	∞	600Ω	30 pF
t_{en} '0'	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF

INPUT CONDITIONS

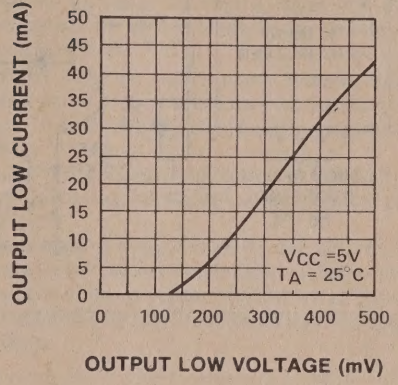
Amplitude — 0V to 3V
Rise and Fall Time — 5 ns From 1V to 2V
Frequency — 1 MHz

TYPICAL DC CHARACTERISTICS

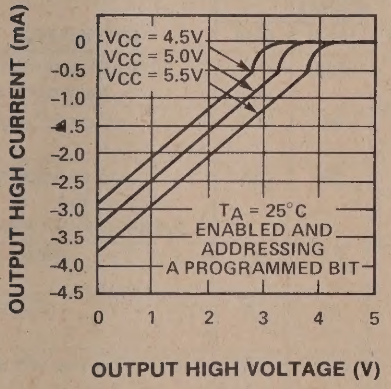
IM5604 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})



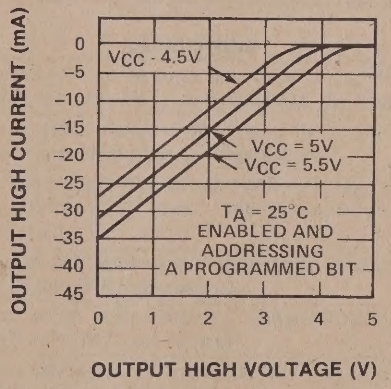
IM5624 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})



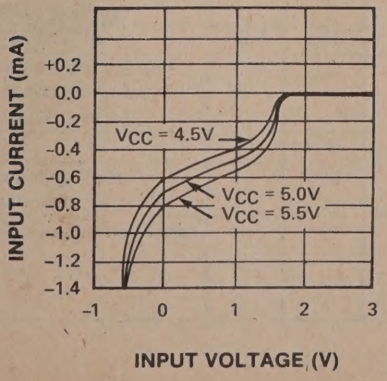
IM5604 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})



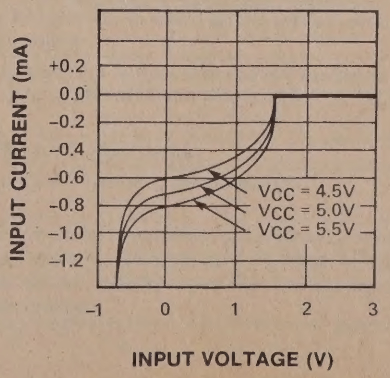
IM5624 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})



IM5604 OR IM5624 CHIP ENABLE INPUT CURRENT VS INPUT VOLTAGE

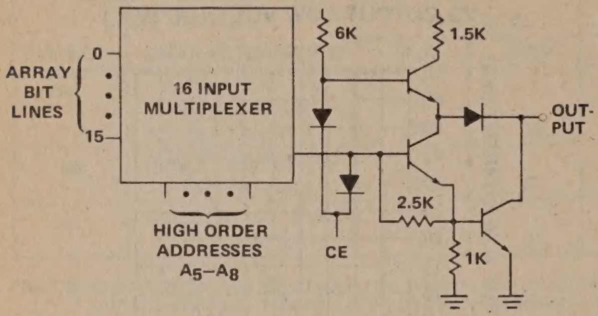


IM5604 OR IM5624 ADDRESS INPUT CURRENT VS INPUT VOLTAGE

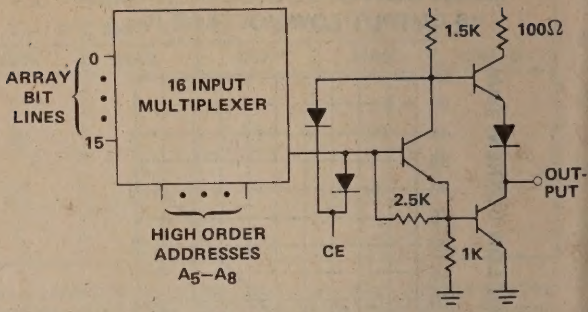


OUTPUT STAGE SCHEMATICS

IM5604


0
ARRAY BIT LINES
15
16 INPUT MULTIPLEXER
HIGH ORDER ADDRESSES A_5–A_8
6K
1.5K
OUT-PUT
CE
2.5K
1K

IM5624


0
ARRAY BIT LINES
15
16 INPUT MULTIPLEXER
HIGH ORDER ADDRESSES A_5–A_8
1.5K
100Ω
OUT-PUT
CE
2.5K
1K

Bipolar PROM Programming Specification

PROGRAMMING PROCEDURES

1. Prior to beginning a programming cycle, the part to be grammed must be searched for previously programmed bits. This must be done to eliminate the risk of programming a part that has some bits not conforming to the pattern desired.
2. Programming is begun by addressing the first word in the sequence, normally address ZERO, although satisfactory programming is not dependent on the word sequence or bit order used.
3. Disable the device by applying a normal TTL high logic level to any active low CE pin. Disabling the device forces the normal output circuitry to a high impedance condition so that it will not be affected by programming pulses applied through the output pins to the programming element array.
4. Sense the bit status by forcing 20mA into the associated output pin and comparing the resultant voltage to the SENSE VOLTAGE.
5. If the bit is to be programmed, increase the 20mA to 200mA at the proper ramp rate and maintain 200mA for 7.5μs. The constant current source must be clamped at 28V.
6. Reduce the current from 200 to 20mA and after 1μs compare the resultant 20mA voltage level to the SENSE VOLTAGE.
7. If the voltage is greater than the SENSE VOLTAGE the current should be increased again to 200mA for another 7.5μs. Generally, programming occurs on the first pulse, but repeated attempts are allowed up to an elapsed time of 100ms.

PROGRAMMING PARAMETER SPECIFICATIONS

The following specification details the necessary requirements for the correct programming of the IM56XX Series of AIM PROMs. Intersil will not accept responsibility for any device found to be defective if it was not programmed according to these specifications.

PARAMETER	LIMITS MIN	LIMITS NOM	LIMITS MAX	UNITS	CONDITIONS
Programming Current Pulse Amplitude	190	200	210	mA	Constant current to be supplied over a 10 to 28V voltage range. Set the nominal value with a 100Ω, 6W load @ 20V.
Voltage Clamp	27.5	28	28.5	Volts	Constant voltage clamp when sinking 130 to 210 mA. Adjust nominal level when sinking 200 mA.
Ramp Rate $\frac{dv}{dt}$ of Program Current Source	50	60	70	V/μs	Voltage ramp rate is measured by switching from 20 to 200 mA into a 100 ohm, 6W resistor with the maximum voltage clamped at 28V.
Pulse Width	7.0	7.5	8.0	μs	Measured at 10V when switching between 20 and 200 mA into a 100 ohm, 6W load resistor.
Duty Cycle	70	75	80	%	Measured at 10V when switching between 20 and 200 mA into a 100 ohm, 6W load resistor.
Sense Current Amplitude	19.5	20.0	20.5	mA	Constant current source amplitude is adjusted for a nominal value of 20 mA into a 12V, 400 mW zener diode load.
Ramp Rate $\frac{dv}{dt}$ Sense Current Source	50	60	70	V/μs	Voltage ramp rate is measured by switching from 0 to 20 mA into a 1.5k ohm, 1W resistor with the maximum voltage clamped at 28V.
Sense Voltage Analog Comparator Reference Voltage	6.9	7.0	7.1	Volts	An element is considered programmed when the voltage sensed at the appropriate output pin with 20 mA forced through the element is less than the analog comparator reference voltage.
5600/10 Only	12.4	12.5	12.6	Volts	
Min. delay from trailing edge of programming pulse before sensing	0.9	1.0	1.1	μs	Measured from the 10V level of the voltage pulse when switching from 200 to 20 mA into a 100 ohm, 6W load resistor.
Vcc	4.9	5.0	5.5	Volts	100 to 200 mA current range.
Programming Time Allocation/Bit	—	100	—	ms	Maximum time allowed to program a bit.
Extra Programming Pulses	—	4	—	Pulse	Absolute number of programming pulses to be issued after the bit output is first sensed as a programmed 'I'. This occurs when the sensed voltage is less than the comparator reference voltage.

PROGRAMMING PROCEDURES (Continued)

8. If the voltage after a programming current pulse is less than the SENSE VOLTAGE, four additional programming pulses are applied with a sense after each pulse.
9. After the fourth extra pulse and correct sense, programming is complete. The 20mA current pulse then is shut off and the address is changed to program the next bit.
10. Repeat steps 4 thru 9 until a successful programming and sense operation is performed at all address locations to be programmed.
11. After the programming cycle is complete, a logical verification must be performed. This is done by cycling through all address locations with the chip enabled and testing the voltage level at each output under the appropriate current forcing conditions (20mA for a low level and 100μA for a high level). This cycle should be completed at both low and high V_{CC}.

POST PROGRAMMING LOGICAL VERIFICATION

Both high (V_{OH}) and low (V_{OL}) logic levels on all outputs should be tested. For all truth-table addresses two passes must be made, one with V_{CC} high and one with V_{CC} low. Forcing conditions and limits for level testing are specified in the following tables.

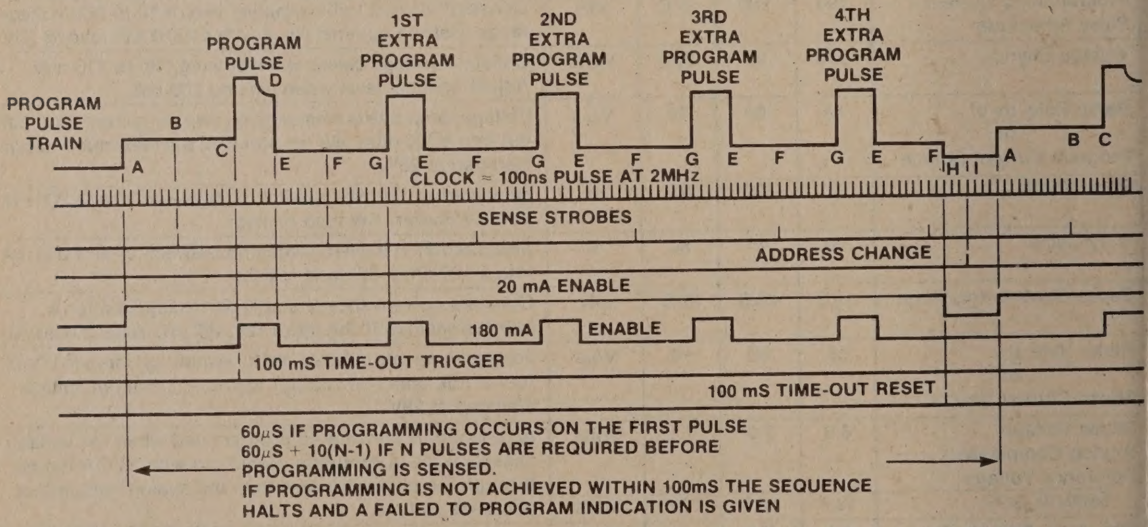
HIGH V_{CC} TESTS — $V_{CC} = 6.5 \pm .1V$

PARAMETER	LIMIT		FORCING CONDITION	LEVEL TESTED
	MIN	MAX		
V_{OL}	—	.85	$I_{OL} = 20mA \pm 1mA$	Zero
V_{OH}	6.9	—	$I_{OL} = 100\mu A \pm 10\mu A$	One

LOW V_{CC} TESTS — $V_{CC} = 4.0V \pm .1V$

PARAMETER	LIMIT		FORCING CONDITION	LEVEL TESTED
	MIN	MAX		
V_{OL}	—	.85	$I_{OL} = 20mA \pm 1mA$	Zero
V_{OH}	4.5	—	$I_{OL} = 100\mu A \pm 10\mu A$	One

PROGRAMMING CYCLE TIMING DIAGRAM


PROGRAM PULSE
1ST EXTRA PROGRAM PULSE
2ND EXTRA PROGRAM PULSE
3RD EXTRA PROGRAM PULSE
4TH EXTRA PROGRAM PULSE
PROGRAM PULSE TRAIN
A
B
C
D
E
F
G
E F G E F G E F G E F
H I I
A
B C
CLOCK = 100ns PULSE AT 2MHz
SENSE STROBES
ADDRESS CHANGE
20 mA ENABLE
180 mA ENABLE
100 mS TIME-OUT TRIGGER
100 mS TIME-OUT RESET

60μS IF PROGRAMMING OCCURS ON THE FIRST PULSE
60μS + 10(N-1) IF N PULSES ARE REQUIRED BEFORE PROGRAMMING IS SENSED.
IF PROGRAMMING IS NOT ACHIEVED WITHIN 100mS THE SEQUENCE HALTS AND A FAILED TO PROGRAM INDICATION IS GIVEN

A - 20mA CURRENT SOURCE TURNED ON (VOLTAGE OVERSHOOT MAY OCCUR)
B - VOLTAGE LEVEL IS SENSED AND COMPARED
C - 180mA CURRENT SOURCE IS TURNED ON (180 + 20 = 200mA)
D - VOLTAGE FALLS INDICATING PROGRAMMING
E - 180mA CURRENT SOURCE IS TURNED OFF
F - VOLTAGE LEVEL IS SENSED AND COMPARED
G - 180mA CURRENT SOURCED IS TURNED ON
H - 20mA CURRENT SOURCE IS TURNED OFF
I - ADDRESS IS CHANGED

INTERSIL

IM6100 CMOS 12 Bit Microprocessor

FEATURES

- **Silicon Gate Complementary MOS**
- **Fully Static - 0 to 5.7 MHz**
- **Single Power Supply**
  - **IM6100 V_{CC} = 5 volts**
  - **IM6100A V_{CC} = 10 volts**
- **Crystal Controlled On Chip Timing**
- **PDP®-8/e, Instruction Set Compatible**
- **Low Power Dissipation**
  - **< 10mW @ 3.3 MHz @ 5 volts**
- **TTL Compatible at 5 volts**
- **Excellent Noise Immunity**
- **Direct Memory Access (DMA)**
- **Interrupt**

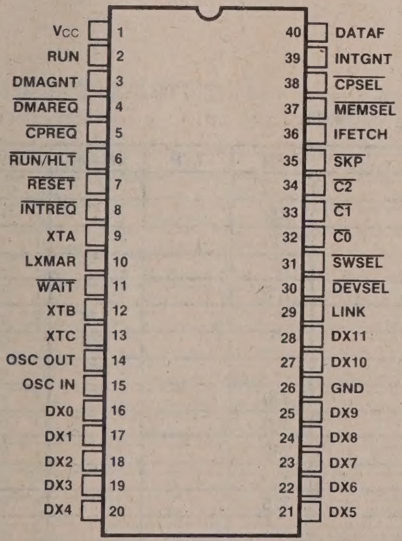
® PDP-8 is a registered trademark of Digital Electronics Corp.

GENERAL DESCRIPTION

The IM6100 is a fixed word length, single word instruction, parallel transfer microprocessor using 12-bit, two's complement arithmetic which recognizes the instruction set of Digital Equipment Corporation's PDP-8/e minicomputer. The internal circuitry is completely static and designed to operate at any speed between DC and the maximum operating frequency. Two pins are available to allow for an external crystal, thereby eliminating the need for clock generators and level translators. The crystal can be removed and the processor clocked by an external clock generator. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

The IM6100 family includes IM6101 (Programmable Interfacing Element), IM6102 (Memory Extension/DMA Controller/Interval Timer), IM6103 (Parallel Input-Output Port), IM6512 (64 x 12 RAM), IM6312 (1k x 12 ROM), and IM6402/03 (UART), all featuring ultra low power-high noise immunity CMOS characteristics. The entire family is supported by the 6910 Intercept II Microcomputer Development System.

PIN CONFIGURATION (outline dwg DL, PL)


VCC 1
RUN 2
DMAGNT 3
DMAREQ 4
CPREQ 5
RUN/HLT 6
RESET 7
INTREQ 8
XTA 9
LXMAR 10
WAIT 11
XTB 12
XTC 13
OSC OUT 14
OSC IN 15
DX0 16
DX1 17
DX2 18
DX3 19
DX4 20
40 DATAF
39 INTGNT
38 CPSEL
37 MEMSEL
36 IFETCH
35 SKP
34 C2
33 C1
32 C0
31 SWSEL
30 DEVSEL
29 LINK
28 DX11
27 DX10
26 GND
25 DX9
24 DX8
23 DX7
22 DX6
21 DX5

BLOCK DIAGRAM

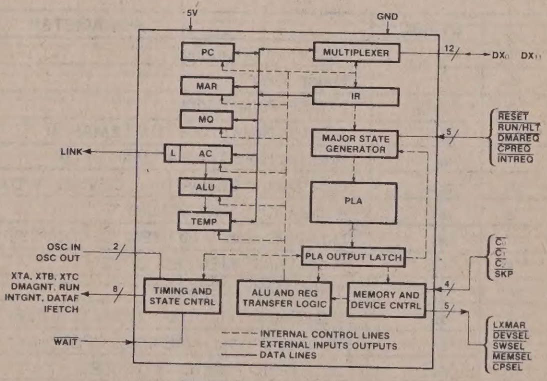

5V
GND
PC
MULTIPLEXER
12
DX0 DX11
MAR
IR
MQ
RESET
RUN/HLT
DMAREQ
CPREQ
INTREQ
5
MAJOR STATE GENERATOR
LINK
L
AC
ALU
PLA
TEMP
OSC IN
OSC OUT
2
PLA OUTPUT LATCH
C0
C1
C2
SKP
XTA, XTB, XTC
DMAGNT, RUN
INTGNT, DATAF
IFETCH
8
TIMING AND STATE CNTRL
ALU AND REG TRANSFER LOGIC
MEMORY AND DEVICE CNTRL
4
5
WAIT
INTERNAL CONTROL LINES
EXTERNAL INPUTS OUTPUTS
DATA LINES
LXMAR
DEVSEL
SWSEL
MEMSEL
CPSEL

Figure 1: Functional Block Diagram

ORDERING INFORMATION

ORDER CODE	IM6100-1	IM6100A	IM6100
PLASTIC PKG.	IM6100-1IPL	IM6100-AIPL	IM6100-IPL
CERAMIC PKG.	IM6100-1IDL	IM6100-AIDL	IM6100-IDL
MILITARY TEMP.	IM6100-1MDL	IM6100-AMDL	IM6100-IDL
MILITARY TEMP. WITH 883B	IM6100-1MDL/ 883B	IM6100-AMDL/ 883B	—

IM6100

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
  Industrial IM6100 .... −45°C to +85°C
Storage Temperature .... −65°C to +150°C
Operating Voltage .... +4.0V to +11.0V
Supply Voltage .... +12.0V
Voltage On Any Input or
  Output Pin .... −0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, T_A = −40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}−2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = −0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OLK}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN} = GND or V_{CC}			800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 2.5MHz			1.8	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS (See Figure 2 and 22)

TEST CONDITIONS: V_{CC} = 5.0V ±10%, C_L = 50pF, T_A −40°C to +85°C, f_C = 2.5MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	f_{op}	Operating Frequency			2.5	MHz
2	t_s	Major State Time	800			ns
3	t_{lxmar}	LXMAR Pulse Width	335			ns
4	t_{as}	Address Setup Time : DX-LXMAR (↓)	120			ns
5	t_{ah}	Address Hold Time : LXMAR (↓)-DX	175			ns
8	t_{end}	Data Output Enable Time: DEVSEL (↓)-DX			575	ns
6	t_{al}	Access Time from LXMAR			650	ns
7	t_{en}	Output Enable Time (MEM, CP, DEVSEL)			400	ns
9	t_{wp}	Pulse Width (MEMSEL, CPSEL)	320			ns
10	t_{wpd}	Pulse Width (DEVSEL)	320			ns
11	t_{ds}	Data Setup Time (DX- ↑ MEMSEL/CPSEL)	240			ns
12	t_{dh}	Data Hold Time (↑ MEMSEL/CPSEL-DX)	175			ns
13	t_{dsd}	Data Setup Time (DX-↑ DEVSEL)	275			ns
14	t_{dhd}	Data Hold Time (↑ DEVSEL-DX)	175			ns
15	t_{sl}	Logic Delay to MEM/DEV/CP/SWSEL	75		440	ns
16	t_{xt}	Logic Delay to LXMAR, XTA, XTB, XTC	65		380	ns
17	t_{st}	Logic Delay to DATAF, RUN, DMAGNT, INTGNT, LINK, IFETCH			475	ns
18	t_{rs}	Set up Time for CP/INT/DMAREQ	0			ns
19	t_{rh}	Hold Time for CP/INT/DMAREQ, RESET, RUN-HALT	300			ns
20	t_{rhp}	RUN-HALT Pulse Width	110			ns
21	t_{ws}	Set up Time for Wait	100			ns
22	t_{wh}	Hold Time for Wait	35			ns

Note: For capacitance greater than 50pF, the AC parameters will have a delay factor of 0.5ns/pF.

IM6100A

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6100AI .... −40°C to +85°C
Storage Temperature .... −65°C to +150°C
Operating Voltage .... +4.0V to +11.0V
Supply Voltage .... +12.0V
Voltage On Any Input or
Output Pin .... −0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ±5%, T_A = −40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = 0.0mA	V_{CC} −0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0.0mA			GND +0.01	V
6	I_{OLK}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN} = GND or V_{CC}			900	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 5.71MHz			4.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS (Ref: Figures 2 and 22)

TEST CONDITIONS: V_{CC} = 10V ±5%, C_L = 50pF, T_A = −40°C to +85°C, f_C = 5.71MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	f_{op}	Operating Frequency			5.71	MHz
2	t_s	Major State Time	350			ns
3	t_{lxmar}	LXMAR Pulse Width	150			ns
4	t_{as}	Address Setup Time : DX-LXMAR (↓)	55			ns
5	t_{ah}	Address Hold Time : LXMAR (↓)-DX	60			ns
8	t_{end}	Data Output Enable Time: DEVSEL (↓)-DX			250	ns
6	t_{al}	Access Time from LXMAR			295	ns
7	t_{en}	Output Enable Time (MEM, CP, DEVSEL)			185	ns
9	t_{wp}	Pulse Width (MEMSEL, CPSEL)	140			ns
10	t_{wpd}	Pulse Width (DEVSEL)	140			ns
11	t_{ds}	Data Setup Time (DX- ↑ MEMSEL/CPSEL)	115			ns
12	t_{dh}	Data Hold Time (↑ MEMSEL/CPSEL-DX)	60			ns
13	t_{dsd}	Data Setup Time (DX- ↑ DEVSEL)	110			ns
14	t_{dhd}	Data Hold Time (↑ DEVSEL-DX)	60			ns
15	t_{sl}	Logic Delay to MEM/DEV/CP/SWSEL	35		180	ns
16	t_{xt}	Logic Delay to LXMAR, XTA, XTB, XTC	35		155	ns
17	t_{st}	Logic Delay to DATAF, RUN, DMAGNT, INTGNT, LINK, IFETCH			190	ns
18	t_{rs}	Set up Time for CP/INT/DMAREQ	0			ns
19	t_{rh}	Hold Time for CP/INT/DMAREQ, RESET, RUN-HALT	125			ns
20	t_{rhp}	RUN-HALT Pulse Width	45			ns
21	t_{ws}	Set up Time for Wait	45			ns
22	t_{wh}	Hold Time for Wait	15			ns

Note: For capacitance greater than 50pF, the AC parameters will have a delay factor of 0.5ns/pF.

IM6100AM (Military)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6100AM .... −55°C to +125°C
Storage Temperature .... −65°C to +150°C
Operating Voltage .... +4.0V to +11.0V
Supply Voltage .... +12.0V
Voltage On Any Input or
Output Pin .... −0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ±5%, T_A = −55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH} = 0.0mA	V_{CC} −0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0.0mA			GND +0.01	V
6	I_{OLK}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	µA
7	I_{CC}	Power Supply Current-Standby	V_{IN} = GND or V_{CC}			900	µA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 5.0MHz			4.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS (Ref.: Figures 2 and 22)

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pF, T_A = −55°C to +125°C, fc = 5.0MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	f_{op}	Operating Frequency			5.0	MHz
2	t_s	Major State Time	400			ns
3	t_{lxmar}	LXMAR Pulse Width	170			ns
4	t_{as}	Address Setup Time : DX-LMAR (↓)	70			ns
5	t_{ah}	Address Hold Time : LXMAR (↓)-DX	70			ns
8	t_{end}	Data Output Enable Time: DEVSEL (↓)-DX			290	ns
6	t_{al}	Access Time from LXMAR			340	ns
7	t_{en}	Output Enable Time (MEM, CP, DEVSEL)			220	ns
9	t_{wp}	Pulse Width (MEMSEL, CPSEL)	160			ns
10	t_{wpd}	Pulse Width (DEVSEL)	160			ns
11	t_{ds}	Data Setup Time (DX- ↑ MEMSEL/CPSEL)	140			ns
12	t_{dh}	Data Hold Time (↑ MEMSEL/CPSEL-DX)	70			ns
13	t_{dsd}	Data Setup Time (DX- ↑ DEVSEL)	140			ns
14	t_{dhd}	Data Hold Time (↑ DEVSEL-DX)	70			ns
15	t_{sl}	Logic Delay to MEM/DEV/CP/SWSEL	35		210	ns
16	t_{xt}	Logic Delay to LXMAR, XTA, XTB, XTC	35		170	ns
17	t_{st}	Logic Delay to DATAF, RUN, DMAGNT, INTGNT, LINK, IFETCH			210	ns
18	t_{rs}	Set up Time for CP/INT/DMAREQ	0			ns
19	t_{rh}	Hold Time for CP/INT/DMAREQ, RESET, RUN-HALT	140			ns
20	t_{rhp}	RUN-HALT Pulse Width	50			ns
21	t_{ws}	Set up Time for Wait	50			ns
22	t_{wh}	Hold Time for Wait	20			ns

Note: For capacitance of greater than 50pF, the AC parameters will have a delay factor of 0.5ns/pF.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
Industrial IM6100-1I	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Operating Voltage	+4.0V to +11.0V
Supply Voltage	+12.0V
Voltage On Any Input or Output Pin	−0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, T_A = −40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC} −2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = −0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OLK}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN} = GND or V_{CC}			800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 3.33MHz			2.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS (Ref. Fig. 2 and 22)

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = −40°C to +85°C, f_C = 3.33MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	f_{op}	Operating Frequency			3.33	MHz
2	t_s	Major State Time	600			ns
3	t_{lxmar}	LXMAR Pulse Width	260			ns
4	t_{as}	Address Setup Time: DX-LXMAR (↓)	85			ns
5	t_{ah}	Address Hold Time : LXMAR (↓)-DX	125			ns
8	t_{end}	Data Output Enable Time: DEVSEL (↓)-DX			470	ns
6	t_{al}	Access Time from LXMAR			520	ns
7	t_{en}	Output Enable Time (MEM, CP, DEVSEL)			300	ns
9	t_{wp}	Pulse Width (MEMSEL, CPSEL)	235			ns
10	t_{wpd}	Pulse Width (DEVSEL)	235			ns
11	t_{ds}	Data Setup Time (DX-↑ MEMSEL/CPSEL)	135			ns
12	t_{dh}	Data Hold Time (↑ MEMSEL/CPSEL-DX)	125			ns
13	t_{dsd}	Data Setup Time (DX-↑ DEVSEL)	225			ns
14	t_{dhd}	Data Hold Time (↑ DEVSEL-DX)	125			ns
15	t_{sl}	Logic Delay to MEM/DEV/CP/SWSEL	75		380	ns
16	t_{xt}	Logic Delay to LXMAR, XTA, XTB, XTC	65		270	ns
17	t_{st}	Logic Delay to DATAF, RUN, DMAGNT, INTGNT, LINK, IFETCH			340	ns
18	t_{rs}	Set up Time for CP/INT/DMAREQ	0			ns
19	t_{rh}	Hold Time for CP/INT/DMAREQ, RESET, RUN-HALT	200			ns
20	t_{rhp}	RUN-HALT Pulse Width	80			ns
21	t_{ws}	Set up Time for Wait	100			ns
22	t_{wh}	Hold Time for Wait	20			ns

Note: For capacitance greater than 50pF, the AC parameters will have a delay factor of 0.5ns/pF.

IM6100-1M (Military)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6100-1M .... −55°C to +125°C
Storage Temperature .... −65°C to +150°C
Operating Voltage .... +4.0V to +11.0V
Supply Voltage .... +12.0V
Voltage On Any Input or
Output Pin .... −0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = −55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC} −2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH} = −0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OLK}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	µA
7	I_{CC}	Power Supply Current-Standby	V_{IN} = GND or V_{CC}			800	µA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 2.5MHz			2.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS (Ref. Fig. 2 and 22)

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = −55°C to +125°C, f_C = 2.5MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	f_{op}	Operating Frequency			2.5	MHz
2	t_s	Major State Time	800			ns
3	t_{lxmar}	LXMAR Pulse Width	355			ns
4	t_{as}	Address Setup Time : DX-LXMAR (↓)	200			ns
5	t_{ah}	Address Hold Time : LXMAR (↓)-DX	175			ns
8	t_{end}	Data Output Enable Time: DEVSEL (↓)-DX			655	ns
6	t_{al}	Access Time from LXMAR			745	ns
7	t_{en}	Output Enable Time (MEM, CP, DEVSEL)			470	ns
9	t_{wp}	Pulse Width (MEMSEL, CPSEL)	330			ns
10	t_{wpd}	Pulse Width (DEVSEL)	330			ns
11	t_{ds}	Data Setup Time (DX- ↑ MEMSEL/CPSEL)	250			ns
12	t_{dh}	Data Hold Time (↑ MEMSEL/CPSEL-DX)	170			ns
13	t_{dsd}	Data Setup Time (DX- ↑ DEVSEL)	350			ns
14	t_{dhd}	Data Hold Time (↑ DEVSEL-DX)	170			ns
15	t_{sl}	Logic Delay to MEM/DEV/CP/SWSEL	75		420	ns
16	t_{xt}	Logic Delay to LXMAR, XTA, XTB, XTC	65		300	ns
17	t_{st}	Logic Delay to DATAF, RUN, DMAGNT, INTGNT, LINK, IFETCH			375	ns
18	t_{rs}	Set up Time for CP/INT/DMAREQ	0			ns
19	t_{rh}	Hold Time for CP/INT/DMAREQ, RESET, RUN-HALT	220			ns
20	t_{rhp}	RUN-HALT Pulse Width	90			ns
21	t_{ws}	Set up Time for Wait	110			ns
22	t_{wh}	Hold Time for Wait	20			ns

Note: For capacitance of greater than 50pF, the AC parameters all have delay factor of 0.5ns/pF.

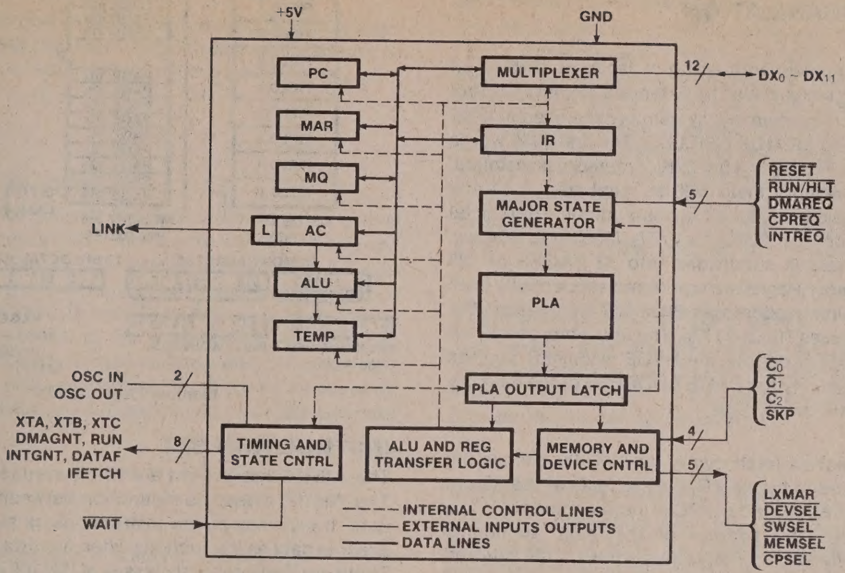

+5V
GND
PC
MULTIPLEXER
12
DX0 – DX11
MAR
IR
MQ
RESET
RUN/HLT
DMAREQ
CPREQ
INTREQ
5
MAJOR STATE GENERATOR
LINK
L
AC
ALU
PLA
TEMP
C0
C1
C2
SKP
OSC IN
OSC OUT
2
PLA OUTPUT LATCH
XTA, XTB, XTC
DMAGNT, RUN
INTGNT, DATAF
IFETCH
8
TIMING AND STATE CNTRL
ALU AND REG TRANSFER LOGIC
MEMORY AND DEVICE CNTRL
4
5
LXMAR
DEVSEL
SWSEL
MEMSEL
CPSEL
WAIT
INTERNAL CONTROL LINES
EXTERNAL INPUTS OUTPUTS
DATA LINES

Figure 1: Functional Block Diagram

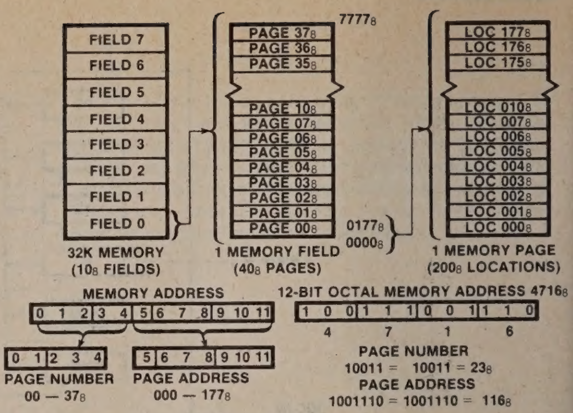
FUNCTIONAL PIN DESCRIPTIONS

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Supply voltage.
2	RUN	The signal indicates the runstate of the CPU and may be used to power down the external circuitry
3	DMAGNT	Direct Memory Access Grant—DX lines are three-state.
4	$\overline{\text{DMAREQ}}$	Direct Memory Access Request—DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the DMAREQ line is released.
5	$\overline{\text{CPREQ}}$	Control Panel Request—a dedicated interrupt which bypasses the normal device interrupt request structure.
6	$\overline{\text{RUN/HLT}}$	Pulsing the Run/Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN/HLT flip flop.
7	$\overline{\text{RESET}}$	Clears the AC and loads 7777_8 into the PC. CPU is halted.
8	$\overline{\text{INTREQ}}$	Peripheral device interrupt request.
9	XTA	External coded minor cycle timing—signifies input transfers to the IM6100.
10	LXMAR	The Load External Memory Address Register is used to store memory and peripheral addresses externally.
11	$\overline{\text{WAIT}}$	Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as WAIT is active. The CPU is in the lowest power state with clocks running.
12	XTB	External coded minor cycle timing—signifies output transfers from the IM6100.
13	XTC	External coded minor cycle timing—used in conjunction with the Select Lines to specify read or write operations.
14	OSC OUT	Crystal input to generate the internal timing (also external clock input).
15	OSC IN	See Pin 14—OSC OUT (also external clock ground)
16	DX_0	DataX—multiplexed data in, data out and address lines.
17	DX_1	See Pin 16—DX_0.
18	DX_2	See Pin 16—DX_0.
19	DX_3	See Pin 16—DX_0.
20	DX_4	See Pin 16—DX_0.
21	DX_5	See Pin 16—DX_0.
22	DX_6	See Pin 16—DX_0.
23	DX_7	See Pin 16—DX_0.
24	DX_8	See Pin 16—DX_0.
25	DX_9	See Pin 16—DX_0.
26	GND	Ground
27	DX_{10}	See Pin 16—DX_0.
28	DX_{11}	See Pin 16—DX_0.
29	LINK	Indicates state of link flip flop.
30	$\overline{\text{DEVSEL}}$	Device Select for I/O transfers.
31	$\overline{\text{SWSEL}}$	Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a Group 2 Operate Instruction which reads a 12 bit external switch register and OR's it with the contents of the AC.
32	$\overline{C_0}$	Control line inputs from the peripheral device during an I/O transfer (Table VI).
33	$\overline{C_1}$	See Pin 32—$\overline{C_0}$.
34	$\overline{C_2}$	See Pin 32—$\overline{C_0}$.
35	SKP	Skips the next sequential instruction if active during an I/O instruction.
36	$\overline{\text{IFETCH}}$	Instruction Fetch Cycle
37	$\overline{\text{MEMSEL}}$	Memory Select for memory transfers.
38	$\overline{\text{CPSEL}}$	The Control Panel Memory Select becomes active, instead of the MEMSEL, for control panel routines. Signal may be used to distinguish between control panel and main memories.
39	INTGNT	Peripheral device Interrupt Grant.
40	DATAF	Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.

MEMORY ORGANIZATION

The IM6100 has a basic addressing capacity of 4096 12-bit words which may be extended by Extended Memory Control hardware to 32K. The memory system is organized in 4096 word blocks, called MEMORY FIELDS. The first 4096 words of memory are in Field 0; if a full 32K of memory is installed, the uppermost Memory Field will be numbered 7. In any given Memory Field every location has a unique 4 digit octal (12 bit binary) address, 0000_8 to 7777_8 (0000_{10} to 4095_{10}). Each Memory Field is subdivided into 32 PAGES of 128 words each. Memory Pages are numbered sequentially from Page 00_8, containing addresses 0000-0177_8, to Page 37_8, containing addresses 7600_8-7777_8. The first 5 bits of a 12-bit MEMORY ADDRESS denote the PAGE NUMBER and the low order 7 bits specify the PAGE ADDRESS of the memory location within the given Page.

During an instruction fetch cycle, the IM6100 fetches the instruction pointed to by the PC, the contents of the PC are transferred to the MAR, and the PC is incremented by 1. The PC now contains the address of the 'next' sequential instruction and the MAR contains the address of the 'current' instruction which must be fetched from memory. Bits 0-4 of the MAR identify the CURRENT PAGE, that is, the Page from which instructions are currently being fetched, and bits 5-11 of the MAR identify the location within the Current Page. (PAGE ZERO (0), by definition, denotes the first 128 words of memory, 0000_8-0177_8.)


FIELD 7
FIELD 6
FIELD 5
FIELD 4
FIELD 3
FIELD 2
FIELD 1
FIELD 0
32K MEMORY
(10₈ FIELDS)
7777₈
PAGE 37₈
PAGE 36₈
PAGE 35₈
PAGE 10₈
PAGE 07₈
PAGE 06₈
PAGE 05₈
PAGE 04₈
PAGE 03₈
PAGE 02₈
PAGE 01₈
PAGE 00₈
0177₈
0000₈
1 MEMORY FIELD
(40₈ PAGES)
LOC 177₈
LOC 176₈
LOC 175₈
LOC 010₈
LOC 007₈
LOC 006₈
LOC 005₈
LOC 004₈
LOC 003₈
LOC 002₈
LOC 001₈
LOC 000₈
1 MEMORY PAGE
(200₈ LOCATIONS)
MEMORY ADDRESS
0 1 2 3 4 5 6 7 8 9 10 11
0 1 2 3 4
PAGE NUMBER
00 — 37₈
5 6 7 8 9 10 11
PAGE ADDRESS
000 — 177₈
12-BIT OCTAL MEMORY ADDRESS 4716₈
1 0 0 1 1 1 0 0 1 1 1 0
4 7 1 6
PAGE NUMBER
10011 = 10011 = 23₈
PAGE ADDRESS
1001110 = 1001110 = 116₈

Memory Organization

INSTRUCTION SET

The IM6100 instructions are 12-bit words stored in memory. The IM6100 makes no distinction between instructions and data; it can manipulate instructions as stored variables or execute data as instructions when it is programmed to do so. There are three general classes of IM6100 instructions. They are referred to as Memory Reference Instruction (MRI), Operate Instruction (OPR) and Input/Output Transfer Instruction (IOT).

The notations used in the following instruction tables are defined in Table I below:

TABLE 1. Notation Definitions

1. ( ) denotes the contents of the register or location within parenthesis. (EA) is read as "... the contents of the Effective Address."
2. (()) denotes the contents of the location pointed to by the contents of the location within the double parenthesis. ((PA)) is read as "... the contents of the location pointed to by the contents of the Pointer Address."
3. ← denotes "... is replaced by ..."
4. ↔ denotes the interchange operation.
5. ∧ denotes logical AND operation.
6. ∨ denotes logical OR operation.
7. EA denotes the Effective Address for Direct Addressing.
8. PA denotes the Pointer Address for Indirect Addressing. PA can be any address on the CURRENT PAGE or PA can be any address (0000_8) through (0177_8) on PAGE ZERO other than the addresses (0010_8) through (0017_8) which are reserved for autoindexing.
9. PAIX denotes the Pointer Address for autoindexing. It can be any address (0010_8) through (0017_8).
10. I represents bit 3, the Indirect Addressing Bit, of the instruction.
11. EA, PA, or PAIX is specified by bit 4 through bit 11 of the memory reference instruction.
12. PC denotes the Program Counter.
13. SR denotes the Switch Register.
14. (AC)n denotes the nth bit of the AC contents.
15. DEV denotes a specific peripheral device and "dddddd" denotes the device address code. CMND is the command issued to the device during an I/O operation and "eee" is its three bit code.

ARCHITECTURE

The IM6100 has 6 twelve bit registers, a programmable logic array, an arithmetic and logic unit and associated gating and timing circuitry. A block diagram of the IM6100 is shown in Figure 1.

ACCUMULATOR (AC)

The AC is a 12-bit register in which arithmetic and logical operations are performed. Data words may be transferred from memory to the AC or transferred from the AC into memory. Arithmetic and logical operations involve one or two operands, one held in the AC and the other fetched from the memory. The result of the operation is left in the AC which may be cleared, complemented, tested, incremented or rotated under program control. The AC also serves as an input-output register, as all programmed data transfers pass through the AC.

LINK (L)

The Link is a 1-bit flip-flop that serves as a high-order extension of the AC. It is used as a carry flip-flop for 2's complement arithmetic. A carry out of the accumulator complements the Link. Link can be cleared, set, complemented and tested under program control and rotated as part of the AC.

MQ REGISTER (MQ)

The MQ is a 12-bit temporary register which is program accessible. The contents of AC may be transferred to the MQ for temporary storage, or MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and the MQ may also be exchanged.

MEMORY ADDRESS REGISTER (MAR)

While accessing memory, the 12-bit MAR register contains the address of the memory location that is currently selected for reading or writing. The MAR is also used as an internal register for microprogram control during data transfers to and from memory and peripherals.

PROGRAM COUNTER (PC)

The 12-bit PC contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the PC is transferred to MAR and the PC is then incremented by 1. When there is a branch to another address in memory, the branch address is set into the PC. Branching normally takes place under program control, however, during an input-output operation, a device may specify a branch address. A skip (SKP) instruction increments the PC by 1, thus causing the next instruction to be skipped. The SKP instruction may be unconditional, or conditional on the state of the AC or the Link. During an input-output operation, a device can also cause the next sequential instruction to be skipped. Interrupts force the PC to 0000. Reset forces the PC to 7777_8.

ARITHMETIC AND LOGICAL UNIT (ALU)

The ALU performs both arithmetic and logical operations, –two's complement binary addition, AND, OR and complement. The ALU can perform a single position shift either to the left or to the right; a double rotate is implemented in two single bit shifts. The ALU can also shift by 3 positions to implement a byte swap in two steps. The AC is always one of the inputs to the ALU, however, under internal microprogram control, AC may be gated off and all one's or all zero's gated in. The second input may be any one of the other registers under internal microprogram control.

TEMPORARY REGISTER (TEMP)

The 12-bit TEMP register latches the result of an ALU operation, before it is sent to the destination register, to avoid race conditions. The TEMP is also used as an internal register for microprogram control.

INSTRUCTION REGISTER (IR)

During an instruction fetch, the 12-bit IR is loaded with the instruction that is to be executed by the CPU. The IR specifies the initial step of the microprogram sequence for each instruction, and is also used as an internal register to store temporary data for microprogram control.

MULTIPLEXER (DX)

The 12-bit Input/Output Multiplexer handles data, address and instruction transfers into and out of the CPU, and to or from the main memory and peripheral devices on a time-multiplexed basis.

MAJOR STATE GENERATOR AND THE PROGRAMMED LOGIC ARRAY (PLA)

During an instruction fetch the instruction to be executed is loaded into the IR. The PLA is then used for the correct sequencing of the CPU for the appropriate instruction. After an instruction is completely sequenced, the major state generator scans the internal priority network, which decides whether the machine is going to fetch the next instruction in sequence, or service one of the external request lines.

PLA OUTPUT LATCH

The PLA Output Latch permits the PLA to be pipelined; it fetches the next control sequence while the CPU is executing the current sequence.

MEMORY AND DEVICE CONTROL, ALU AND REG TRANSFER LOGIC

The Memory and Device Control Unit provides external control signals to communicate with peripheral devices (DEVSEL), switch register (SWSEL), memory (MEMSEL) and/or control panel memory (CPSEL). During I/O instructions this unit also modifies the PLA outputs depending on the states of the four device control lines (SKP, C_0, C_1, C_2). The ALU and Register Transfer Logic provides the control signals for the internal register transfers and ALU operation.

ARCHITECTURE (CONTINUED)

TIMING AND STATE CONTROL

The IM6100 internally generates all the timing and state signals. A crystal is used to control the CPU operating frequency, which is divided by two by the CPU. With a 4MHz crystal, the internal states will be of 500nsec duration. The major timing states are described in Figure 2.

T_1 For memory reference instructions, a 12-bit address is sent on the DX lines. The Load External Memory Address Register, LXMAR, is used to clock an external register to store the address information externally, if required. When executing an Input-Output I/O instruction, the instruction being executed is sent on the DX lines to be stored externally. The external address register then contains the device address and control information. The LXMAR pulse occurs only if a valid address is present on the DX lines.

Various CPU request lines are priority sampled if the next cycle is an Instruction Fetch cycle. Current state of the CPU is available externally.

T_2 Memory/Peripheral data is read for an input transfer (READ). WAIT controls the transfer duration. If WAIT is active during input transfers, the CPU waits in the T_2 state. The wait duration is an integral multiple of the crystal frequency — 250nsec for 4MHz.

For memory reference instructions, the Memory Select, MEMSEL, line is active. For I/O instructions the Device Select, DEVSEL, line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines, C_0, C_1, C_2, and SKP, are sampled if the instruction being executed is an I/O instruction.

Control Panel Memory Select, CPSEL, and Switch Register Select, SWSEL, become active low for data transfers between the IM6100 and Control Panel Memory and the Switch Register, respectively.

T_3,T_4,T_5 ALU operation and internal register transfers.

T_6 This state is entered for an output transfer (WRITE). The address is defined during T_1. WAIT controls the time for which the Write data must be maintained.

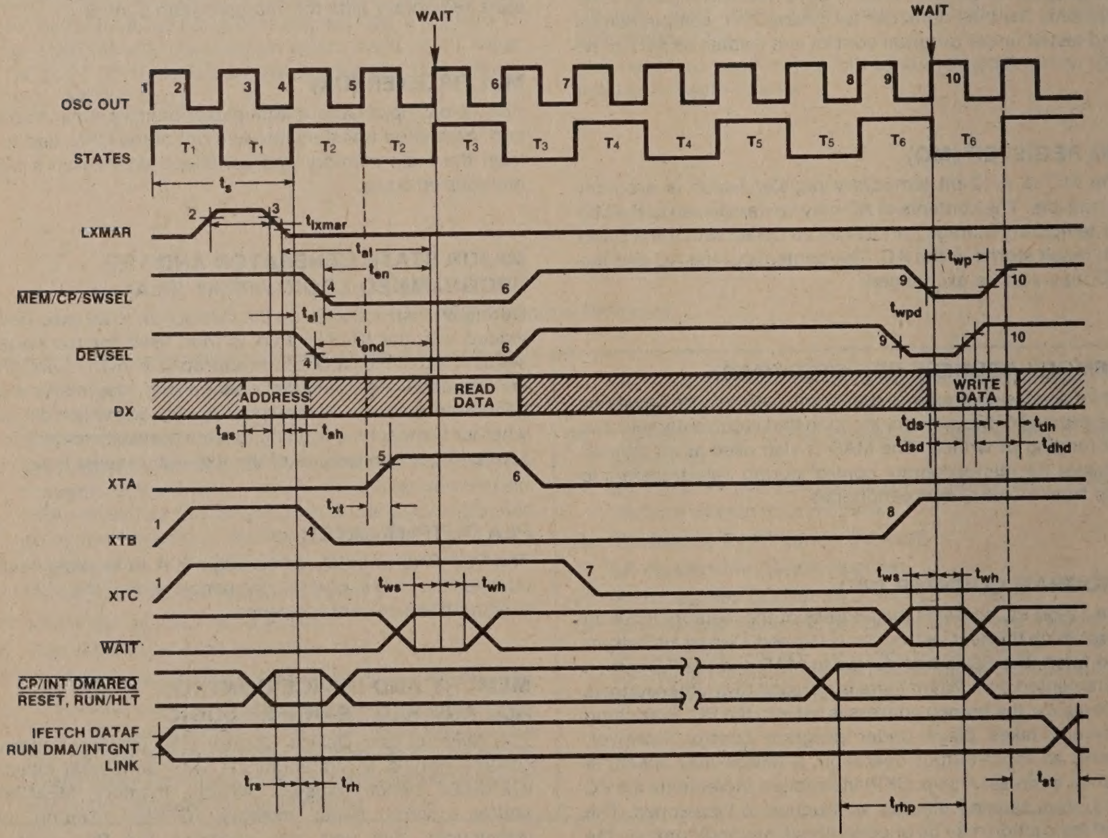

WAIT
WAIT
OSC OUT
1 2 3 4 5 6 7 8 9 10
STATES
T1 T1 T2 T2 T3 T3 T4 T4 T5 T5 T6 T6
ts
LXMAR
tlxmar
tal
ten
MEM/CP/SWSEL
tal
tend
DEVSEL
DX
ADDRESS
READ DATA
WRITE DATA
tas
tah
XTA
txt
XTB
XTC
tws
twh
WAIT
CP/INT DMAREQ
RESET, RUN/HLT
IFETCH DATAF
RUN DMA/INTGNT
LINK
trs
trh
twp
twpd
tds
tdsd
tdh
tdhd
tws
twh
trhp
tst

Figure 2: IM6100 AC Timing Diagram

INSTRUCTION SET (CONTINUED)

MEMORY REFERENCE INSTRUCTION (MRI)

The Memory Reference Instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. The first 3 bits of a Memory Reference Instruction specify the operation code, or OPCODE, and the low order 9 bits, the OPERAND address, as shown in Figure 3.

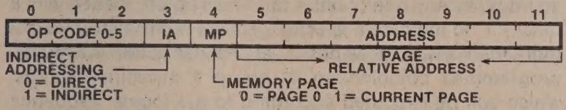


Figure 3: Memory Reference Instruction Format

Bits 5 through 11, the PAGE ADDRESS, identify the location of the OPERAND on a given page, but they do not identify the page itself. The page is specified by bit 4, called the CURRENT PAGE OR PAGE 0 BIT. If bit 4 is a 0, the page address is interpreted as a location on Page 0. If bit 4 is a 1, the page address specified is interpreted to be on the Current Page.

For example, if bits 5 through 11 represent 123$_8$ and bit 4 is a 0, the location referenced is the absolute address 0123$_8$. However, if bit 4 is a 1 and the current instruction is in a memory location whose absolute address is 4610$_8$ the page address 123$_8$ designates the absolute address 4723$_8$, as shown below.

4610$_8$ = 100 110 001 000 = PAGE 10 011 = PAGE 23$_8$

Location 4610$_8$ is in PAGE 23$_8$. Location 123$_8$ in PAGE 23$_8$, CURRENT PAGE, will be:

10 011 1 010 011 = 100 111 010 011 = 4723$_8$

PAGE ADDRESS 123$_8$

PAGE NUMBER 23$_8$

By this method, 256 locations may be directly addressed, 128 on PAGE 0 and 128 on the CURRENT PAGE. Other locations are addressed indirectly by setting bit 3. An INDIRECT ADDRESS (pointer address) identifies the location that contains the desired address (effective address). To address a location that is not directly addressable, not in PAGE 0 or in the CURRENT PAGE, the absolute address of the desired location is stored in one of the 256 directly addressable locations (pointer address). Upon execution, the MRI will operate on the contents of the location identified by the address contained in the pointer location.

It should be noted that locations 0010$_8$-0017$_8$ in PAGE 0 are AUTOINDEXED. If these locations are addressed indirectly, the contents are incremented by 1 and restored before they are used as the operand address. These locations may, therefore, be used for indexing applications.

Table II lists the mnemonics for the six memory reference instructions, their OPCODEs, the operations they perform and the number of states required for execution.

It should be noted that the data is represented in Two's Complement Integer notation. In this system, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most significant bit. In the 12-bit word used by the IM6100, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The maximum single precision number ranges for this system are 3777$_8$ (+2047) and 4000$_8$ (−2048).

Table II

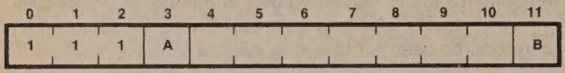
MNEMONIC	OP CODE	IA	STATES	OPERATION
AND EA	0$_8$	0	10	LOGICAL AND DIRECT Operation: $(AC) \leftarrow (AC) \wedge (EA)$ Description: Contents of the EA are logically AND'ed with the contents of the AC and the result is stored in AC.
AND I PA		1	15	LOGICAL AND INDIRECT (PA ≠ 0010-0017$_8$) Operation: $(AC) \leftarrow (AC) \wedge ((PA))$
AND PAIX		1	16	LOGICAL AND AUTOINDEX (PAIX = 0010-0017$_8$) Operation: $(PA) \leftarrow (PA) + 1$; $(AC) \leftarrow (AC) \wedge ((PA))$
TAD EA	1$_8$	0	10	BINARY ADD DIRECT Operation $(AC) \leftarrow (AC) + (EA)$ Description: Contents of the EA are ADD'ed with the contents of the AC and the result is stored in the AC, carry out complements the LINK. If AC is initially cleared, this instruction acts as LOAD from Memory.
TAD I PA		1	15	BINARY ADD INDIRECT (PA ≠ 0010-0017$_8$) Operation $(AC) \leftarrow (AC) + ((PA))$
TAD I PAIX		1	16	BINARY ADD AUTOINDEX (PAIX = 0010-0017$_8$) Operation $(PA) \leftarrow (PA) + 1$, $(AC) \leftarrow (AC) + ((PA))$
ISZ EA	2$_8$	0	16	INCREMENT AND SKIP IF ZERO DIRECT Operation: $(EA) \leftarrow (EA) + 1$, if $(EA) = 0000_8$, $PC \leftarrow PC + 1$ Description: Contents of the EA are incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.
ISZ I PA		1	21	INCREMENT AND SKIP IF ZERO INDIRECT (PA ≠ 0010-0017$_8$) Operation: $((PA)) \leftarrow ((PA)) + 1$, if $((PA)) = 0000_8$, $PC \leftarrow PC + 1$
ISZ I PAIX		1	22	INCREMENT AND SKIP IF ZERO AUTOINDEX (PAIX = 0010-0017$_8$) Operation $(PA) \leftarrow (PA) + 1$; $((PA)) \leftarrow ((PA)) + I$; if $((PA)) = 0000_8$, $PC \leftarrow PC + 1$
DCA EA	3$_8$	0	11	DEPOSIT AND CLEAR THE ACCUMULATOR DIRECT Operation $(EA) \leftarrow (AC)$, $(AC) \leftarrow 0000_8$ Description: The contents of the AC are stored in EA and the AC is cleared.
DCA I PA		1	16	DEPOSIT AND CLEAR THE ACCUMULATOR INDIRECT (PA ≠ 0010-0017$_8$) Operation $((PA)) \leftarrow (AC)$, $(AC) \leftarrow 0000_8$
DCA I PAIX		1	17	DEPOSIT AND CLEAR THE ACCUMULATOR AUTOINDEX (PAIX = 0010-0017$_8$) Operation $(PA) \leftarrow (PA) + 1$, $((PA)) \leftarrow (AC)$, $(AC) \leftarrow 0000_8$
JMS EA	4$_8$	0	11	JUMP TO SUBROUTINE DIRECT Operation: $(EA) \leftarrow (PC)$, $(PC) \leftarrow EA + 1$ Description: The contents of the PC are stored in the EA. The PC is incremented by 1 immediately after every instruction fetch. The contents of the EA now point to the next sequential instruction following the JMS (return address). The next instruction is taken from EA + 1
JMS I PA		1	16	JUMP TO SUBROUTINE INDIRECT (PA ≠ 0010-0017$_8$) Operation $((PA)) \leftarrow PC$, $(PC) \leftarrow (PA) + 1$
JMS I PAIX		1	17	JUMP TO SUBROUTINE AUTOINDEX (PAIX = 0010-0017$_8$) Operation $(PA) \leftarrow (PA) + 1$, $((PA)) \leftarrow PC$, $(PC) \leftarrow (PA) + 1$
JMP EA	5$_8$	0	10	JUMP DIRECT Operation $(PC) \leftarrow EA$ Description: The next instruction is taken from the EA.
JMP I PA		1	15	JUMP INDIRECT (PA ≠ 0010-0017$_8$) Operation (PC) (PA)
JMP I PAIX		1	16	JUMP AUTOINDEX (PAIX = 0010-0017$_8$) Operation $(PA) + 1$, $(PC) \leftarrow (PA)$

INSTRUCTION SET (CONTINUED)

OPERATE INSTRUCTIONS

The Operate Instructions, which have an OPCODE of 7_8 (111), consist of 3 groups of microinstructions. Group 1, which is identified by the presence of the 0 in bit 3, is used to perform logical operations on the contents of the accumulator and link. Group 2, which is identified by the presence of a 1 in bit 3 and a 0 in bit 11, is used primarily to test the contents of the Accumulator and/or Link and then conditionally skip the next sequential instruction. Group 3 has a 1 in bit 3 and a 1 in bit 11 and performs logical operations on the contents of the AC and MQ.

The basic OPR instruction format is shown in Figure 4.



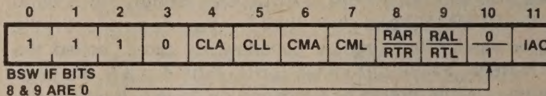
MICROINSTRUCTION	A	B
GROUP 1	0	0/1
GROUP 2	1	0
GROUP 3	1	1

Figure 4: Basic OPR Instruction Format

Operate microinstructions from any group may be microprogrammed with other operate microinstructions of the same group providing the instruction codes do not conflict. The actual code for a microprogrammed combination of two, or more, microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 performed first, logical sequence number 2 performed second, logical sequence number 3 performed third and so on. Two operations with the same logical sequence number, within a given group of microinstructions, are performed simultaneously.

GROUP MICROINSTRUCTIONS

Figure 5 shows the instruction format of a group 1 microinstruction. Any one of bits 4 to 11 may be set, loaded with a binary 1, to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 5.



BSW IF BITS
8 & 9 ARE 0
AND BIT 10 IS 1.

LOGICAL SEQUENCES:
1—CLA, CLL
2—CMA, CML
3—IAC
4—RAR, RAL, RTR, RTL, BSW

Figure 5: Group 1 Microinstruction Format

Table III lists commonly used group 1 microinstructions, their assigned mnemonics, octal code, logical sequence, the number of states, and the operation they perform. The same format is followed in Table IV and V which lists group 2 and 3 microinstructions, respectively.

Table III: Group 1 Operate Microinstructions

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7000	1	10	NO OPERATION—This instruction causes a 10 state delay in program execution, without affecting the state of the IM6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.
IAC	7001	3	10	INCREMENT ACCUMULATOR—The content of the AC is incremented by one (1) and carry out complements the Link (L).
RAL	7004	4	15	ROTATE ACCUMULATOR LEFT—The contents of the AC and L are rotated one binary position to the left. AC (0) is shifted to L and L is shifted to AC (11).
RTL	7006	4	15	ROTATE TWO LEFT—The contents of the AC and L are rotated two binary positions to the left. AC (1) is shifted to L and L is shifted to AC (10).
RAR	7010	4	15	ROTATE ACCUMULATOR RIGHT—The content of the AC and L are rotated one binary position to the right. AC (11) is shifted to L and L is shifted to AC (0).
RTR	7012	4	15	ROTATE TWO RIGHT—The contents of the AC and L are rotated two binary positions to the right. AC (10) is shifted to L and L is shifted to AC (1).
BSW	7002	4	15	BYTE SWAP—The right six (6) bits of the AC are exchanged or SWAPPED with the left six bits. AC (0) is swapped with AC (6), AC (1) with AC (7), etc. L is not affected.
CML	7020	2	10	COMPLEMENT LINK—The content of the link is complemented.
CMA	7040	2	10	COMPLEMENT ACCUMULATOR—The content of each bit of the AC is complemented having the effect of replacing the content of the AC with its one's complement.
CIA	7041	2,3	10	COMPLEMENT AND INCREMENT ACCUMULATOR—The content of the AC is replaced with its two's complement. Carry out complements the LINK.
CLL	7100	1	10	CLEAR LINK—The link is loaded with a binary 0.
CLL RAL	7104	1,4	15	CLEAR LINK—ROTATE ACCUMULATOR LEFT.
CLL RTL	7106	1,4	15	CLEAR LINK—ROTATE TWO LEFT.
CLL RAR	7110	1,4	15	CLEAR LINK—ROTATE ACCUMULATOR RIGHT.
CLL RTR	7112	1,4	15	CLEAR LINK—ROTATE TWO RIGHT.
STL	7120	1,2	10	SET THE LINK—The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.
CLA	7200	1	10	CLEAR ACCUMULATOR—The accumulator is loaded with binary 0's.
CLA IAC	7201	1,3	10	CLEAR ACCUMULATOR—INCREMENT ACCUMULATOR.
GLT	7204	1,4	15	GET THE LINK—The AC is cleared; the content of L is shifted into AC (11), a 0 is shifted into L. This is a microprogrammed combination of CLA and RAL.
CLA CLL	7300	1	10	CLEAR ACCUMULATOR—CLEAR LINK.
STA	7240	1,2	10	SET THE ACCUMULATOR—Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.

INSTRUCTION SET (CONTINUED)

GROUP 2 MICROINSTRUCTIONS

Figure 6 shows the instruction format of group 2 microinstructions. Bits 4-10 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4-7 or 9-10 is set, the instruction is a microprogrammed combination of group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 6.

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or, when bit 8 is 1, the decision will be based on the logical AND.

By combining skip instructions properly, all possible relational conditions can be tested (i.e., =, ≠, <, ≤, >, ≥). Skip microinstructions which have a 0 in bits 5, 6, 7, or 8 may not be microprogrammed with skip microinstructions which have a 1 in those same bits.

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	SMA SPA	SZA SNA	SNL SZL	0 1	OSR	HLT	0

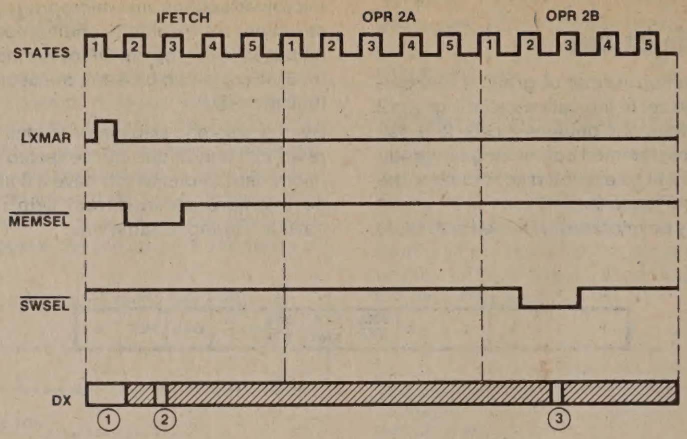
LOGICAL SEQUENCES:
1 (BIT 8 IS ZERO)—SMA OR SZA OR SNL
(BIT 8 IS ONE) —SPA AND SNA AND SZL
2 —CLA
3 —OSR, HLT

Figure 6: Group 2 Microinstruction Format

Table IV: Group 2 Operate Microinstructions

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7400	1	10	NO OPERATION—See Group 1 MICROINSTRUCTIONS
HLT	7402	3	10	HALT—Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.
OSR	7404	3	15	OR WITH SWITCH REGISTER—The content of the Switch Register if OR'ed with the content of the AC and the result is stored in the AC. The OSR INSTRUCTION TIMING is shown in Figure 7. The IM6100 sequences the OSR instruction through a 2-cycle execute phase referred to as OPR 2A and OPR 2B.
SKP	7410	1	10	SKIP—The content of the PC is incremented by 1, to skip the next sequential instruction.
SNL	7420	1	10	SKIP ON NON-ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.
SZL	7430	1	10	SKIP ON ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 0. If the L contains a 1, the next instruction is executed.
SZA	7440	1	10	SKIP ON ZERO ACCUMULATOR—The content of the AC is sampled; the next sequential instruction is skipped if the AC has all bits which are 0. If any bit in the AC is a 1, the next instruction is executed.
SNA	7450	1	10	SKIP ON NON-ZERO ACCUMULATOR—The content of the AC is sampled; the next sequential instruction is skipped if the AC has any bits which are not 0. If every bit in the AC is 0, the next instruction is executed.
SZA SNL	7460	1	10	SKIP ON ZERO ACCUMULATOR, OR SKIP ON NON-ZERO LINK, OR BOTH
SNA SZL	7470	1	10	SKIP ON NON-ZERO ACCUMULATOR AND SKIP ON ZERO LINK
SMA	7500	1	10	SKIP ON MINUS ACCUMULATOR—If the content of AC (0) contains a 1, indicating that the AC contains a negative two's complement number, the next sequential instruction is skipped. If AC (0) contains a 0, the next instruction is executed.
SPA	7510	1	10	SKIP ON POSITIVE ACCUMULATOR—The contents of AC (0) are sampled. If AC (0) contains a 0, indicating that the AC contains a positive two's complement number, the next sequential instruction is skipped. If AC (0) contains a 1, the next instruction is executed.
SMA SNL	7520	1	10	SKIP ON MINUS ACCUMULATOR OR SKIP ON NON-ZERO LINK OR BOTH
SPA SZL	7530	1	10	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON ZERO LINK
SMA SZA	7540	1	10	SKIP ON MINUS ACCUMULATOR OR SKIP ON ZERO ACCUMULATOR OR BOTH
SPA SNA	7550	1	10	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON NON-ZERO ACCUMULATOR
SMA SZA SNL	7560	1	10	SKIP ON MINUS ACCUMULATOR OR SKIP ON ZERO ACCUMULATOR OR SKIP ON NON-ZERO LINK OR ALL
SPA SNA SZL	7570	1	10	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON NON-ZERO ACCUMULATOR AND SKIP ON ZERO LINK
CLA	7600	2	10	CLEAR ACCUMULATOR—The AC is loaded with binary 0's.
LAS	7604	1,3	15	LOAD ACCUMULATOR WITH SWITCH REGISTER—The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.
SZA CLA	7640	1,2	10	SKIP ON ZERO ACCUMULATOR THEN CLEAR ACCUMULATOR
SNA CLA	7650	1,2	10	SKIP ON NON-ZERO ACCUMULATOR THEN CLEAR ACCUMULATOR
SMA CLA	7700	1,2	10	SKIP ON MINUS ACCUMULATOR THEN CLEAR ACCUMULATOR
SPA CLA	7710	1,2	10	SKIP ON POSITIVE ACCUMULATOR THEN CLEAR ACCUMULATOR

INSTRUCTION SET (CONTINUED)



① INSTRUCTION ADDRESS ② INSTRUCTION→ CPU ③ SWITCH REGISTER,→ CPU DATA

Figure 7: OSR Instruction Timing

GROUP 3 MICROINSTRUCTIONS

Figure 8 shows the instruction format of group 3 microinstructions which requires bits 3 and 11 to contain a 1. Bits 4, 5 or 7 may be set to indicate a specific group 3 microinstruction. If more than one of the bits is set, the instruction is a microprogrammed combination of group 3 microinstructions following the logical sequence listed in Figure 8. All unused bits are "don't care".

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	MQA		MQL				1

*DON'T CARE

LOGICAL SEQUENCES:
1—CLA
2—MQA, MQL
3—ALL OTHERS

Figure 8: Group 3 Microinstruction Format

Table V: Group 3 Operate Microinstructions

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7401	3	10	NO OPERATION—See Group 1 Microinstructions
MQL	7421	2	10	MQ REGISTER LOAD—The content of the AC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost.
MQA	7501	2	10	MQ REGISTER INTO ACCUMULATOR—The content of the MQ is OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the programmer with an inclusive OR operation.
SWP	7521	3	10	SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are interchanged accomplishing a microprogrammed combination of MQA and MQL.
CLA	7601	1	10	CLEAR ACCUMULATOR
CAM	7621	3	10	CLEAR ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are loaded with binary 0's. This is equivalent to a microprogrammed combination of CLA and MQL.
ACL	7701	3	10	CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR—This is equivalent to a microprogrammed combination of CLA and MQA.
CLA SWP	7721	3	10	CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared.

INSTRUCTION SET (CONTINUED)

INPUT/OUTPUT (IOT) INSTRUCTIONS

The input/output transfer instructions, which have an OP-CODE of 6_8 are used to control the operation of peripheral devices and to transfer data between peripherals and the IM6100. Three types of data transfer may be used to receive or transmit information between the IM6100 and one or more peripheral I/O devices: PROGRAMMED DATA TRANSFER, which provides a straightforward means of communicating with relatively slow I/O devices, such as Teletypes, cassettes, card readers and CRT displays, INTERRUPT TRANSFERS which use the interrupt system to service several peripheral devices simultaneously, and DIRECT MEMORY ACCESS, DMA, which transfers variable-size blocks of data between high-speed peripherals and memory without IM6100 intervention.

IOT INSTRUCTION FORMAT

The Input/Output Transfer Instruction format is represented in Figure 9. The instruction executes in 17 states.

The first three bits, 0-2, are always set to 6_8 (110) to specify an IOT instruction. The low order nine bits are used for device selection and control. PDP-8/e compatible interfaces use bits 3-8 for device selection and bits 9-11 for control of the selected device. The IM6101 PIE interface uses bits 3-7 for device selection and bits 8-11 for control. In user designed systems, the 512 possible IOT instructions may be alloted according to the user's needs. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

PROGRAMMED DATA TRANSFER

Programmed Data Transfer is the easiest, simplest, most convenient and most common means of performing data I/O. For microprocessor applications, it may also be the most cost effective approach. The data transfer begins when the IM6100 fetches an instruction from the memory and recognizes that the current instruction is an IOT (Figure 10). This is referred to as IFETCH and consists of five (5) internal states. The IM6100 sequences the IOT instruction through a 2-cycle execute phase referred to as IOT$_A$ and IOT$_B$. Bits 0-11 of the IOT instructions are available on DX0-11 at IOT$_A$ • LXMAR; these bits must be latched in an external address register. DEVSEL is active low to enable data transfers between the IM6100 and the peripheral device(s). The selected peripheral device communicates with the IM6100 through 4 control lines - C$_0$, C$_1$, C$_2$ and SKP. In the IM6100 the type of data transfer, during an IOT instruction, is specified by the peripheral device(s) by asserting the control lines as shown in Table VI.

The control line SKP, when low during an IOT, causes the IM6100 to skip the next sequential instruction. This feature is used to sense the status of various signals in the device interface. The C$_0$, C$_1$, and C$_2$ lines are treated independently of the SKP line. In the case of a RELATIVE or ABSOLUTE JUMP, the skip operation is performed after the jump. The input signals to the IM6100, DX 0-11, C$_0$, C$_1$, C$_2$, and SKP, are sampled at IOT$_A$ during DEVSEL • XT$_C$ and the data from the IM6100 is available to the device(s) during that time. IOT$_B$ is used by the IM6100 to perform the operations requested during IOT$_A$. Both IOT$_A$ and IOT$_B$ consist of six (6) internal states.

In summary, Programmed Data Transfer performs data I/O with a minimum of hardware support. The maximum rate at which programmed data transfers may take place is limited by the IM6100 instruction execution rate, however, the data rate of the most commonly used peripheral devices is much lower than the maximum rate at which programmed transfers can take place in the IM6100. The major drawback associated with Programmed Data Transfer is the IM6100 must hang up in a waiting loop while the I/O device completes the last transfer and prepares for the next transfer. On the other hand, this technique permits easy hardware implementation and simple, economical interface design. For this reason, almost all devices except mass storage units rely on programmed data transfer.

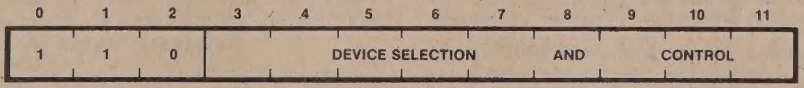


Figure 9: IOT Instruction Format

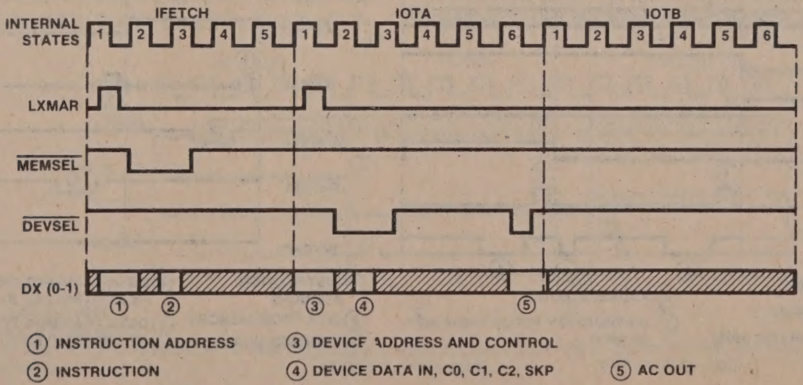


Figure 10: Input-Output Instruction Timing

INSTRUCTION SET (CONTINUED)

Table VI: Programmed I/O Control Lines

CONTROL LINES C_0	C_1	C_2	OPERATION	DESCRIPTION
H	H	H	DEV ←AC	The content of the AC is sent to the device.
L	H	H	DEV ←AC; CLA	The content of the AC is sent to a device and then the AC is cleared.
H	L	H	AC ←AC V DEV	Data is received from a device, OR'ed with the data in the AC and the result is stored in the AC.
L	L	H	AC←DEV	Data is received from a device and loaded into the AC.
*	H	L	PC←PC + DEV	Data from the device is added to the contents of the PC. This is referred to as a RELATIVE JUMP.
*	L	L	PC ←DEV	Data is received from a device and loaded into the PC. This is referred to as an ABSOLUTE JUMP.

*Don't Care

INTERRUPT TRANSFER

PROGRAM INTERRUPT TRANSFERS

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device I/O is greatly reduced or eliminated altogether. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device status is set, indicating that the device is actually ready to perform a data transfer.

The interrupt system allows certain external conditions to interrupt the computer program by driving the INTREQ input Low. If no higher priority requests are outstanding and the interrupt system is enabled, the IM6100 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the Interrupt Enable Flip-Flop in the IM6100 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

DEVICE INTERRUPT GRANT TIMING

The current contents of the Program Counter, PC, are deposited in location 0000_8 of the memory and the program fetches the instruction from location 0001_8. The return address is available in location 0000_8. This address must be saved in a software stack, before the interrupts are re-enabled, if nested interrupts are permitted. The INTGNT signal, Figure 11, is activated by the IM6100 when a device interrupt is acknowledged; this signal is reset by executing any IOT instruction as shown in Figure 12. The INTGNT signal is necessary to implement an External Vectored Priority Interrupt network. The IM6101 PIE contains the logic necessary to implement both vectored and non-vectored interrupts.

The user program controls the interrupt mechanism of the IM6100 by executing the processor IOT instructions listed in Table VII. Several of these interrupt IOT instructions are also used if the memory is extended beyond 4K words to save and restore extended memory status during interrupt servicing.

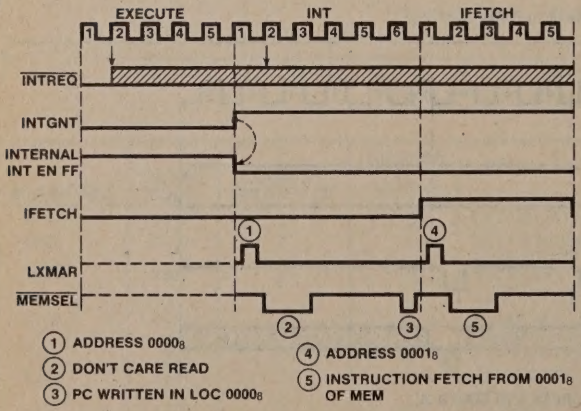

EXECUTE
INT
IFETCH
1 2 3 4 5 1 2 3 4 5 6 1 2 3 4 5
INTREQ
INTGNT
INTERNAL INT EN FF
IFETCH
LXMAR
MEMSEL
① ② ③ ④ ⑤
① ADDRESS 0000₈
② DON'T CARE READ
③ PC WRITTEN IN LOC 0000₈
④ ADDRESS 0001₈
⑤ INSTRUCTION FETCH FROM 0001₈ OF MEM

Figure 11: Device Interrupt Grant Timing

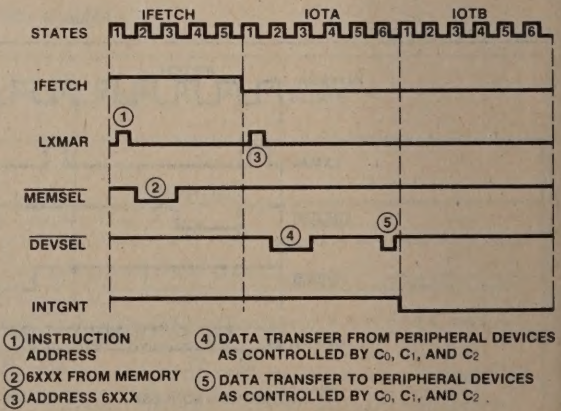
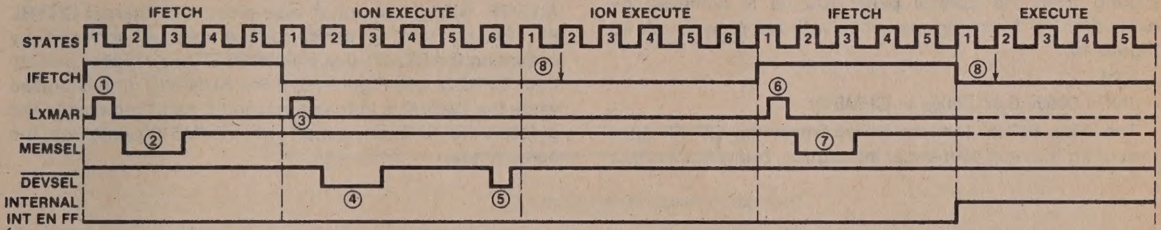

STATES
IFETCH
IOTA
IOTB
1 2 3 4 5 1 2 3 4 5 6 1 2 3 4 5 6
IFETCH
LXMAR
MEMSEL
DEVSEL
INTGNT
① ② ③ ④ ⑤
① INSTRUCTION ADDRESS
② 6XXX FROM MEMORY
③ ADDRESS 6XXX
④ DATA TRANSFER FROM PERIPHERAL DEVICES AS CONTROLLED BY C₀, C₁, AND C₂
⑤ DATA TRANSFER TO PERIPHERAL DEVICES AS CONTROLLED BY C₀, C₁, AND C₂

Figure 12: Device Interrupt Grant Reset Timing

INSTRUCTION SET (CONTINUED)

Table VII: Processor IOT Instructions

MNE-MONIC	OCTAL CODE	OPERATION
SKON	6000	SKIP IF INTERRUPT ON — If interrupt system is enabled, the next sequential instruction is skipped. The Interrupt system is disabled.
ION	6001	INTERRUPT TURN ON — The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction. The INTERRUPT ENABLE TIMING is shown in Figure 13.
IOF	6002	INTERRUPT TURN OFF — The interrupt system is disabled. Note that the interrupt system is automatically disabled when the CPU acknowledges an INT request.
SRQ	6003	SKIP IF INT REQUEST — The next sequential instruction is skipped if the INT request bus is low.
GTF	6004	GET FLAGS — The following machine states are read into the indicated bits of AC. bit 0 — Link bit 2 — INT request bus bit 4 — Interrupt Enable FF Other bits may be modified by external devices by controlling the C-lines, (ex. Extended memory control).
RTF	6005	RETURN FLAGS — Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states. (ex. Extended memory control).
SGT	6006	Operation is determined by external devices, if any.
CAF	6007	CLEAR ALL FLAGS — AC and Link are cleared. Interrupt system is disabled.



① INSTRUCTION ADDRESS
② INSTRUCTION FETCH
③ DEVICE ADDRESS (6001_8)
④ DON'T CARE DEV READ, SAMPLE C0, C1, C2 & SKP
⑤ DON'T CARE DEV WRITE
⑥ INSTRUCTION ADDRESS
⑦ INSTRUCTION FETCH
⑧ SAMPLE REQUEST LINES

Figure 13: Interrupt Enable FF ON (ION)

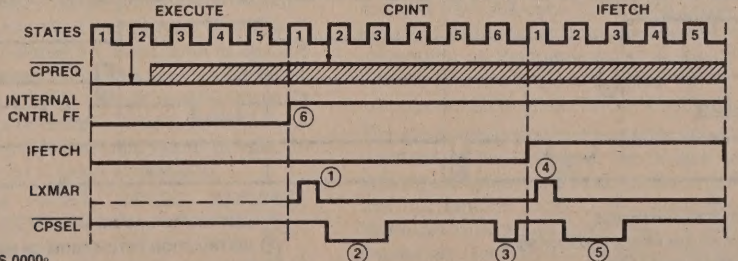
CONTROL PANEL INTERRUPT TRANSFER

The IM6100 supports a memory space completely separate from main memory, called control panel memory. Therefore, the IM6100 control panel and other supervisory functions are implemented in software. This implementation need not use any part of the main memory or change the processor state. This is an important feature, since the final version of the system may not have a control panel and the system designer would like to use the entire capacity of the main memory for the specific system application.

The control panel communicates with the IM6100 with the Control Panel Request, CPREQ, line. The CPREQ is functionally similar to the INTREQ with some important differences. The CPREQ is granted even when the machine is in the HALT state; the IM6100 is temporarily put in the RUN state for the duration of the panel routine. The IM6100 reverts to its original processor state after the panel routine has been executed.

The CPREQ does not affect the interrupt enable system, and the processor IOT instruction, ION is redefined and IOF is ignored while the IM6100 is in the Control Panel Mode. Once a CPREQ is granted, the IM6100 will not recognize any DMAREQ or INTREQ until CPREQ has been fully serviced.

When a CPREQ is granted, the PC is stored in location 0000_8 of the Panel Memory and the IM6100 resumes operation at location 7777_8. The Panel Memory would be organized with RAM's in the lower pages and PROM's in the higher pages. The control panel service routine would be stored in the higher pages in the nonvolatile PROM's, starting at 7777_8.



① ADDRESS 0000_8
② DON'T CARE READ
③ PC WRITTEN IN LOC 0000_8 OF CP MEM
④ ADDRESS 7777_8
⑤ INSTRUCTION FETCHED FROM LOC 7777_8 OF CP MEM
⑥ IF CPU IS HALTED, THE RUN IS TRUE AT T1 OF CPINT

Figure 14: Control Panel Interrupt Grant Timing

INSTRUCTION SET (CONTINUED)

A Control Panel Flip-Flop, CNTRL FF, internal to the IM6100, is set when the CPREQ is granted. The CNTRL FF prevents further CPREQ's from being granted.

When the CNTRL FF is set, the Control Panel Memory Select, CPSEL, is active rather than the Memory Select, MEMSEL, for memory references. The CPSEL signal may therefore be used to distinguish the Control Panel Memory from the Main Memory. However, during the Execute phase of indirectly addressed AND, TAD, ISZ or DCA instructions, the MEMSEL is made active. The instructions are always fetched from the control panel memory, and the operand address for indirectly address AND, TAD, ISZ or DCA refers first to the control panel memory for an effective address, which, in turn, refers to a location in the main memory. A main memory location may therefore be examined and changed by indirectly addressed TAD and DCA instructions, Figure 15, respectively. Every location in the main memory is accessible to the control panel routine.

Exiting from the control panel routine is achieved by executing the following sequence with reference made to Figure 16.

ION

JMP I 0000_8 (Loc 0000_8 in CPMEM)

The ION, 6001_8, instruction will reset the CP FF after executing the next sequential instruction, but will not affect the interrupt system since the CNTRL FF is still active. Location 0000_8 of the CPMEM contains either the original return address, deposited by the IM6100 when the CP routine was entered, or a new starting address defined by the CP routine, for example, by activating the LOAD ADDRESS SWITCH. CPREQ's are normally generated by the manual actuation of the control switches. If the CPU registers must be displayed in real-time, the CPREQ's must be generated by a timer at fixed intervals.

The designer may also make use of the control panel features to implement Bootstrap loaders in the CP Memory so that the loader will be "transparent" to the main memory. Programs will be loaded by DCA I POINTER instruction, the pointer being developed in the CP RAM to point to the main memory location to be loaded.

Approximately 64 P/ROM locations are sufficient to implement all the functions of the PDP®-8/e Control Panel. The IM6100 provides for a 12-bit switch register which can be read by the IM6100 under program control with the SWITCH REGISTER, OSR, instruction even without a control panel.

An RTF, 6005_8, instruction also resets the internal CNTRL FF. Exiting from a panel routine can be achieved by activating the RESET line since RESET has a higher priority than CPREQ, see Figure 18. If the RUN/HLT line is pulsed while the IM6100 is in the panel mode, it will 'remember' the pulses(s) but defer any action until the IM6100 exits from the panel mode.

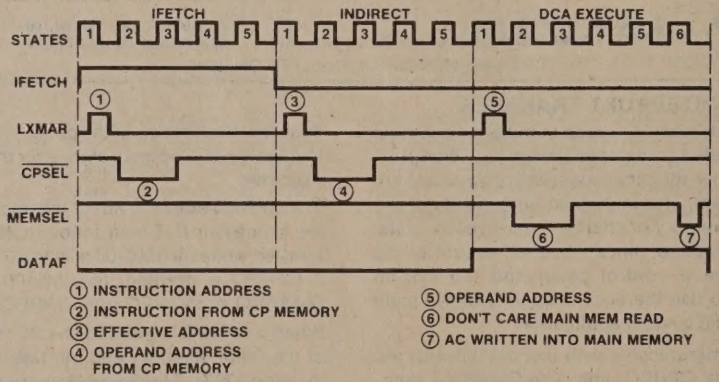

IFETCH
INDIRECT
DCA EXECUTE
STATES
1 2 3 4 5 1 2 3 4 5 1 2 3 4 5 6
IFETCH
LXMAR
CPSEL
MEMSEL
DATAF
①
②
③
④
⑤
⑥
⑦
① INSTRUCTION ADDRESS
② INSTRUCTION FROM CP MEMORY
③ EFFECTIVE ADDRESS
④ OPERAND ADDRESS FROM CP MEMORY
⑤ OPERAND ADDRESS
⑥ DON'T CARE MAIN MEM READ
⑦ AC WRITTEN INTO MAIN MEMORY

Figure 15: "DCA Indirect" In Control Panel Routine

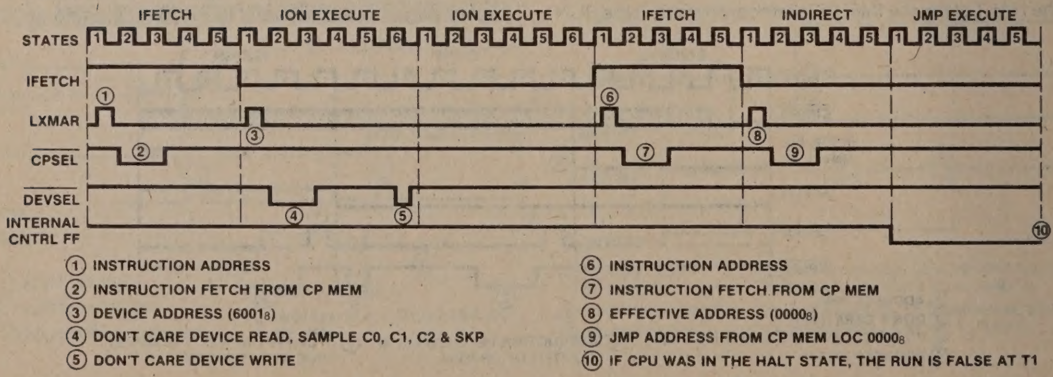

IFETCH
ION EXECUTE
ION EXECUTE
IFETCH
INDIRECT
JMP EXECUTE
STATES
1 2 3 4 5 1 2 3 4 5 6 1 2 3 4 5 6 1 2 3 4 5 1 2 3 4 5 1 2 3 4 5
IFETCH
LXMAR
CPSEL
DEVSEL
INTERNAL CNTRL FF
①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
① INSTRUCTION ADDRESS
② INSTRUCTION FETCH FROM CP MEM
③ DEVICE ADDRESS (6001₈)
④ DON'T CARE DEVICE READ, SAMPLE C0, C1, C2 & SKP
⑤ DON'T CARE DEVICE WRITE
⑥ INSTRUCTION ADDRESS
⑦ INSTRUCTION FETCH FROM CP MEM
⑧ EFFECTIVE ADDRESS (0000₈)
⑨ JMP ADDRESS FROM CP MEM LOC 0000₈
⑩ IF CPU WAS IN THE HALT STATE, THE RUN IS FALSE AT T1

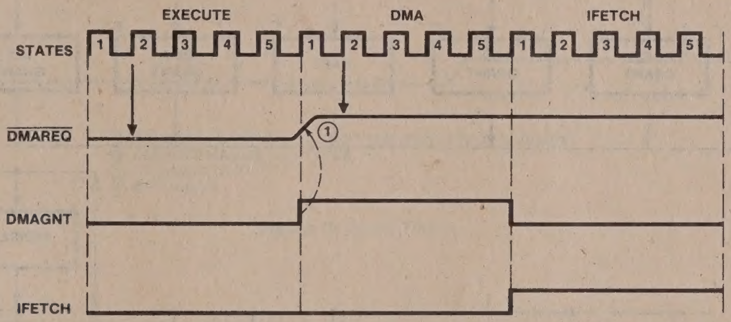
Figure 16: "ION; JMP I 0000_8" In Control Panel Routine

DIRECT MEMORY ACCESS (DMA)

Direct Memory Access, sometimes called data break, is the preferred form of data transfer for use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices, and the IM6100 is involved only in setting up the transfer; the transfers take place on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The device generates a DMA Request when it is ready to transfer data. The IM6100 grants the DMAREQ by activating the DMAGNT signal at the end of the current instruction as shown in Figure 17. The IM6100 suspends any further instruction fetches until the DMAREQ line is released. The DX lines are tri-stated, all SEL lines are high, and the external timing signals XT_A, XT_B, and XT_C are active and LXMAR remains low. The device which generated the DMAREQ must provide the address and the necessary control signals to the memory for data transfers. The DMAREQ line can also be used as a level sensitive "pause" line.

DMA may also be implemented in a transparent mode without stealing processor cycles by using the DX bus during idle periods. The IM6102 MEDIC operates in this manner.



① DMAREQ REMOVED AFTER DMAGNT

Figure 17: Direct Memory Access (DMA)

INTERNAL PRIORITY STRUCTURE

After an instruction is completely sequenced, the major state generator scans the internal priority network as shown in Figure 18. The state of the priority network decides the next sequence of the IM6100.

The request lines, RESET, CPREQ, RUN/HLT, DMAREQ and INTREQ, are sampled in the last cycle of an instruction execution, at time T1. The worst case response time of the IM6100 to an external request is, therefore, the time required to execute the longest instruction preceded by any 6-state execution cycle. For the IM6100, this is an autoindexed ISZ, 22 states, preceded by any 6-state execution cycle instruction.

When the IM6100 is initially powered up, the state of the timing generator is undefined. The generator is automatically initialized with a maximum of 34 clock pulses. The request inputs, as the IM6100 is powered on, must span at least 58 clock pulses to be recognized, 34 clocks for the counter to initialize and a maximum of two IM6100 cycles (20 to 24 clocks) for the state generator to sample the request lines. A positive transition on RUN/HALT should occur at least 10 clock pulses after RESET for it to be recognized.

The internal priority is RESET, CPREQ, RUN/HLT, DMAREQ, INTREQ, and IFETCH.

IFETCH

If no external requests are pending, the IM6100 fetches the next instruction pointed to by the contents of the PC. The IFETCH line is active during the cycle in which the instruction is fetched. External devices can monitor DX, 0-2, during IFETCH-XT_A to determine the functional class of the current instruction. For example, the external memory extension hardware must know when JMP or JMS instructions are fetched to implement the Extended Memory Control. The IM6102 does this to implement extended memory addressing.

The Programmable Logic Array, PLA, in the IM6100 sequences the IM6100 to execute the fetched instruction. All INDIRECT and AUTOINDEX Memory Reference Instructions go through a common state sequence to generate the Effective Address, EA, of the operand. The subsequent sequence, referred to as the EXECUTE phase, is controlled by the functional class of the instruction. The EXECUTE phase of AND, TAD, DCA, JMS, JMP and OPR Group 3 Microinstructions consists of only one cycle. ISZ and IOT have a 2-cycle EXECUTE phase. OPR Group 1 and Group 2 Microinstructions have an optional second cycle, depending on the microcoding of the OPR instructions. An IM6100 cycle consists of 5 states, T_1, T_2, T_3, T_4 and T_5, with an optional sixth state, T_6, for Output Transfers (WRITE).

The state sequence for internal (processor) and external IOT instructions are identical. The Device Address and Control bits are available in the External Address Register for internal IOT instructions. External hardware, for example Extended Memory Control, can control the C-lines for data transfers to implement Get Flags (GTF), Return Flags (RTF), and Clear All Flags (CAF) instructions. External Control of the C-lines is necessary to implement these internal IOT instructions since the flag bits may be distributed both inside and outside the IM6100.

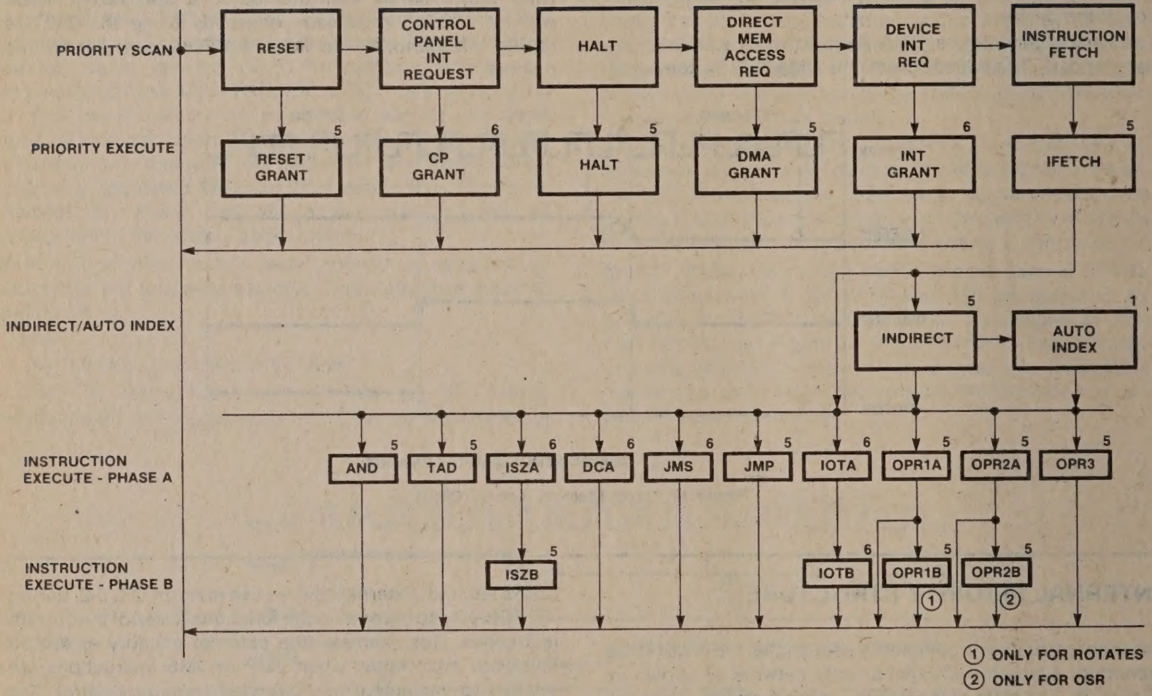
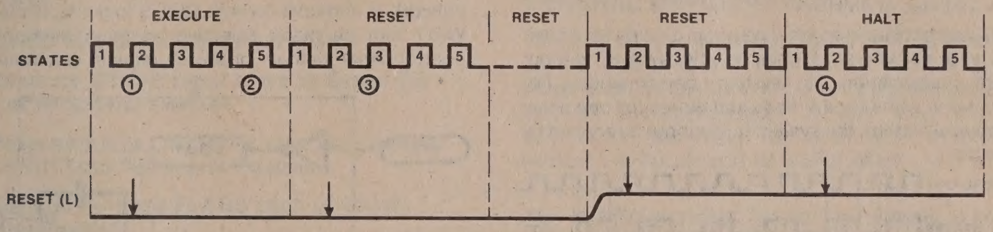

PRIORITY SCAN
RESET
CONTROL PANEL INT REQUEST
HALT
DIRECT MEM ACCESS REQ
DEVICE INT REQ
INSTRUCTION FETCH
PRIORITY EXECUTE
RESET GRANT
5
CP GRANT
6
HALT
5
DMA GRANT
5
INT GRANT
6
IFETCH
5
INDIRECT/AUTO INDEX
INDIRECT
5
AUTO INDEX
1
INSTRUCTION EXECUTE - PHASE A
AND
5
TAD
5
ISZA
6
DCA
6
JMS
6
JMP
5
IOTA
6
OPR1A
5
OPR2A
5
OPR3
5
INSTRUCTION EXECUTE - PHASE B
ISZB
5
IOTB
6
OPR1B
5
①
OPR2B
5
②
① ONLY FOR ROTATES
② ONLY FOR OSR

Figure 18: Major Processor States and Number of Clock Cycles in Each State

RESET

The Reset initializes all internal IM6100 flags and clears the AC and the LINK. The machine is halted.

As long as the RESET line is low, the IM6100 remains in the reset state and the DX lines are three stated. The IM6100 continues to provide the external timing signals XT_A, XT_B and XT_C, all SEL lines are high, and the PC is set to 7777_8. In most applications, the higher memory locations utilize P/ROM's or ROM's. Therefore, a power-up routine starting at the highest memory location can be used to initialize the system. It is also possible to force entry into control panel memory on power-up.


EXECUTE
RESET
RESET
RESET
HALT
STATES
1
2
3
4
5
①
②
③
④
RESET (L)

① REQUESTS SAMPLED AT T1 OF THE FINAL EXECUTE PHASE
② EXECUTE MAY BE 5/6 STATES
③ PC IS SET TO 7777_8
④ CPU HALTS

Figure 19: Reset Timing

RUN/HALT

RUN/HLT changes the state of the IM6100's RUN/HLT flip-flop. Pulsing the line low causes the IM6100 to alternately run and halt. The RUN/HLT line is normally high. The IM6100 recognizes the positive transition of the signal.

The RUN/HLT flip-flop can be put in the halt state under program control by executing the HLT, 7402_8, instruction. When the IM6100 is halted, RUN/HLT is functionally identical to the CONTINUE switch of the PDP-8/e control panel and the RUN signal is low. The RUN signal can be used to power down external circuitry for a low power system.

The RUN/HLT can also be used to make the IM6100 execute one instruction at a time as shown in Figure 21. The RUN/HLT combines the functional features of STOP, CONTINUE, and SINGLE INSTRUCTION as defined by the PDP-8/e Control Panel.

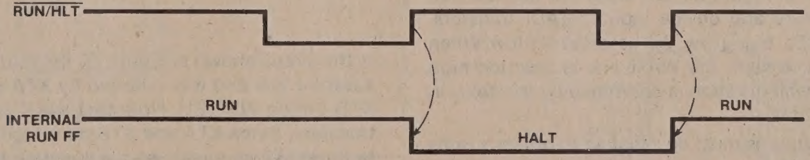
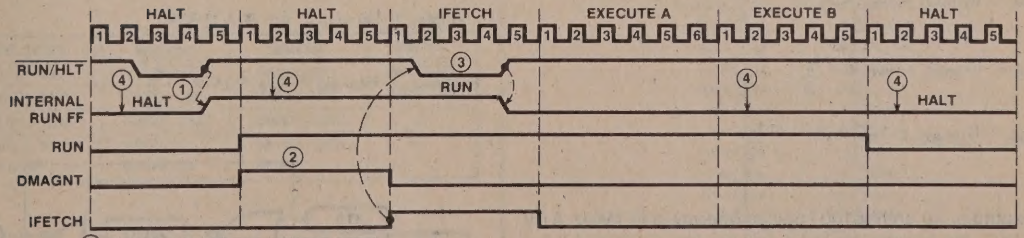

$\overline{\text{RUN/HLT}}$
INTERNAL RUN FF
RUN
HALT
RUN

Figure 20: Run/Halt Timing


HALT
HALT
IFETCH
EXECUTE A
EXECUTE B
HALT
1
2
3
4
5
6
$\overline{\text{RUN/HLT}}$
INTERNAL RUN FF
RUN
DMAGNT
IFETCH
HALT
RUN
HALT
①
②
③
④

① RUN/HLT PULSE FOR "SINGLE STEP"
② DMAGNT ON FOR 1 CYCLE FOR HALT TO RUN TRANSITION
③ TRIGGER RUN/HLT WITH IFETCH
④ RUN FF SAMPLED IN THE LAST EXECUTE CYCLE

Figure 21: "Single Step" With Run/Hlt

WAIT

The IM6100 samples the WAIT line during input-output data transfers (Figure 22). The WAIT line, if low, controls the transfer duration. If WAIT is active during input transfers (READ), the CPU waits in the T2 state. For an output transfer (WRITE), WAIT controls the time for which the write data is maintained on the DX lines by extending the T6 state. The wait duration is an integral multiple of the oscillator time period — 250nsec at 4MHz.

The WAIT mechanism is an ideal way of providing for slower memory and peripheral devices in the system without significant degradation in system performance. For example, if one waits for all reads and writes for one delay unit (250nsec at 4MHz), the system throughput is reduced by less than 3%.

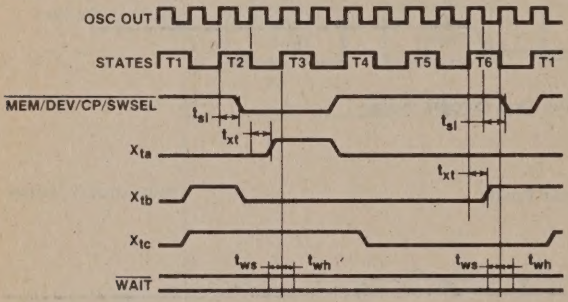


Figure 22: Wait Line Sampling Timing

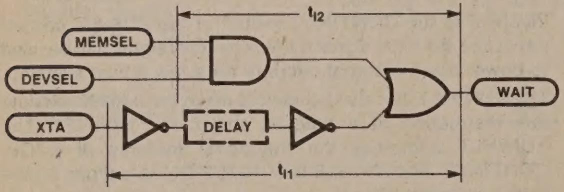


Figure 23: Memory And Input Transfer Wait Circuit

The circuit shown in Figure 23 will make the IM6100 wait during main memory and device input (READ) transfers. MEMSEL or DEVSEL, being low, will assert WAIT low. When XTA becomes active high, the WAIT line is asserted high after a delay. The wait duration is controlled by the delay in the XTA-WAIT path (t_{L1}).

The following conditions must be satisfied to obtain x units of delay during READ's:

$$t_{sl(max)} + t_{l2(max)} + t_{ws} < t_s$$

$$t_{xt(min)} + t_{l1(min)} - t_{wh} \geq x\,\frac{t_s}{2}$$

$$t_{xt(max)} + t_{l1(max)} + t_{ws} < (x + 1)\,\frac{t_s}{2}$$

For example, for an IM6100 I device operating at 4MHz, 5.0V and 25°C, the constraints to be met to obtain 1 unit of delay (250nsec) are as follows:

$t_{l2(max)} < t_s - t_{sl(max)} - t_{ws}$
$< 500 - 300 - 30$
$< 170\text{nsec}$

$t_{l1(min)} \geq \frac{t_s}{2} - t_{xt(min)} + t_{wh}$
$\geq 250 - 100 + 30$
$\geq 180\text{nsec}$
$t_{l1(max)} < t_s - t_{xt(max)} - t_{ws}$
$< 500 - 250 - 30$
$< 220\text{nsec}$

Note that the delay circuit can be as simple as an R-C network in conjunction with CMOS logic. Note also that the WAIT can be made selective on main memory, device, control panel memory or switch register select line.

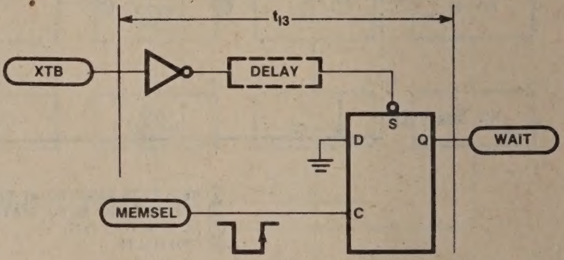


Figure 24: Write Transfer Wait Circuit

Figure 24 shows a logic implementation to wait during WRITE's only.

The rising edge of MEMSEL (or CPSEL or DEVSEL) during READ clocks in a zero on the WAIT line. XTB, after a delay, releases the WAIT line. Every WRITE pulse is preceded by a READ pulse, and if no write operation is performed in a cycle, the T6 state is not entered and the WAIT line is not sampled. For x units of delay, the following conditions must be met:

$$t_{xt(min)} + t_{l3(min)} - t_{wh} \geq x\,\frac{t_s}{2} \text{ and}$$

$$t_{xt(max)} + t_{l3(max)} + t_{ws} < (x + 1)\,\frac{t_s}{2}$$

In the circuit shown in Figure 25, the WAIT signal is normally asserted low and it is released by XTA during READ's and XTB during WRITE's. Note that WAIT is active for all data transfers. Since XTA and XTB have identical timing relative to the WAIT sample point, the constraints to be satisfied are as follows:

$$t_{xt(min)} + t_{l4(min)} - t_{wh} \geq x\,\frac{t_s}{2} \text{ and}$$

$$t_{xt(max)} + t_{l4(max)} + t_{ws} < (x + 1)\,\frac{t_s}{2}$$

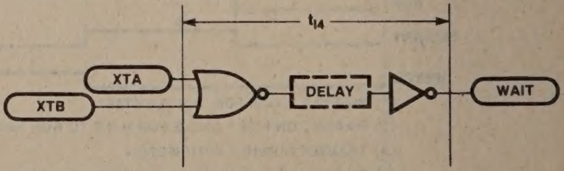


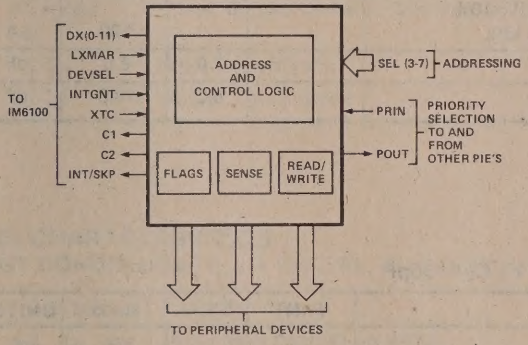
Figure 25: Data Transfer Wait Circuit

IM6101
Programmable Interface Element (PIE)

FEATURES

- **Compatible with IM6100 Microprocessor**
- **Four Separate SENSE Input Lines to Sense the Status of Peripheral Devices**
- **Four Programmable OPERATE Control Lines for READ/WRITE on Peripheral Devices**
- **Four General Purpose FLAGS each of which is Programmable**
- **Chained Vectored Priority Interrupt Structure Possible**
- **Low Power: Less than 1mW @ 5V**
- **TTL Compatible at +5V**

FUNCTIONAL BLOCK DIAGRAM



TO IM6100
DX(0-11)
LXMAR
DEVSEL
INTGNT
XTC
C1
C2
INT/SKP
ADDRESS AND CONTROL LOGIC
FLAGS
SENSE
READ/WRITE
SEL (3-7)
ADDRESSING
PRIN
POUT
PRIORITY SELECTION TO AND FROM OTHER PIE'S
TO PERIPHERAL DEVICES

FIGURE 1.

ORDERING INFORMATION

ORDER CODE	IM6101-1	IM6101A	IM6101
PLASTIC PKG.	IM6101-1IPL	IM6101-AIPL	IM6101-IPL
CERAMIC PKG.	IM6101-1IDL	IM6101-AIDL	IM6101-IDL
MILITARY TEMP.	IM6101-1MDL	IM6101-AMDL	—
MILITARY TEMP. WITH 883B	IM6101-1 MDL/883B	IM6101-AMDL/ 883B	—

GENERAL DESCRIPTION

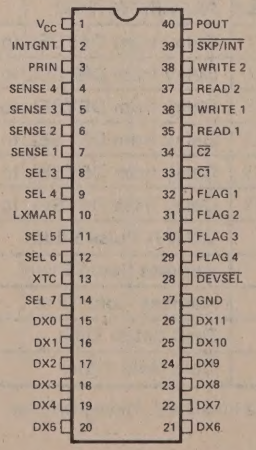
The IM6101 is a Programmable Interface Element (PIE) device designed for interfacing various peripheral chips such as UART's, FIFO's, Keyboard Scanner's to IM6100 Microprocessor. In this way, the IM6101 eliminates the need for additional external logic between 6100 μP and its peripherals.

The IM6101 provides the control signals to peripheral devices for READING or WRITING on the DX bus by activating the WRITE CNTRL and READ CNTRL lines with IOT (Input Output Transfer) instructions.

Each IM6101 can sample 4 status lines from peripheral devices. It can also generate interrupt requests to the μP if the corresponding individual interrupt enable bits in the PIE are enabled and the respective status lines become active.

The four FLAG lines may be set or reset under program control to send control information to the peripheral devices or to send binary data.

PIN CONFIGURATION (outline dwg DL, PL)



V_CC 1
INTGNT 2
PRIN 3
SENSE 4 4
SENSE 3 5
SENSE 2 6
SENSE 1 7
SEL 3 8
SEL 4 9
LXMAR 10
SEL 5 11
SEL 6 12
XTC 13
SEL 7 14
DX0 15
DX1 16
DX2 17
DX3 18
DX4 19
DX5 20
40 POUT
39 SKP/INT
38 WRITE 2
37 READ 2
36 WRITE 1
35 READ 1
34 C2
33 C1
32 FLAG 1
31 FLAG 2
30 FLAG 3
29 FLAG 4
28 DEVSEL
27 GND
26 DX11
25 DX10
24 DX9
23 DX8
22 DX7
21 DX6

IM6101

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6101I .... -40°C to +85°C
Storage Temperature .... -65°C to 150°C
Operating Voltage .... 4.0V to 7.0V
Supply Voltage .... +8.0V
Voltage On Any Input or
Output Pin .... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CCSB}	Power Supply Current—Standby	V_{CC} = 5V ± 10%		1.0	100	μA
8	I_{CCOP}	Power Supply Current—Dynamic	V_{CC}=5V±10% f=250 kHz			500	μA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{dr}	Delay from DEVSEL to READ			375	ns
2	t_{dw}	Delay from DEVSEL to WRITE	100		375	ns
3	t_{df}	Delay from DEVSEL to FLAG			475	ns
4	t_{dc}	Delay from DEVSEL to C1, C2			560	ns
5	t_{di}	Delay from DEVSEL to SKP/INT			560	ns
6	t_{da}	Delay from DEVSEL to DX			560	ns
7	t_{lxmar}	LXMAR Pulse Width	300			ns
8	t_{as}	Address Setup Time	100			ns
9	t_{ah}	Address Hold Time	150			ns
10	t_{ds}	Data Setup Time	90			ns
11	t_{dh}	Data Hold Time	150			ns

Note: See Figure 2 for an A.C. Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6101A .... -40° C to +85° C
Storage Temperature .... -65° C to 150° C
Operating Voltage .... 4.0V to 11.0V
Supply Voltage .... +12.0V
Voltage On Any Input or
Output Pin .... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -40° C to +85° C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CCSB}	Power Supply Current—Standby	V_{CC}=10V±5%		1.0	500	μA
8	I_{CCOP}	Power Supply Current—Dynamic	V_{CC}=10V±5% f=571 kHz			2.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ±5%, T_A = -40° C to +85° C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{dr}	Delay from DEVSEL to READ			150	ns
2	t_{dw}	Delay from DEVSEL to WRITE	50		150	ns
3	t_{df}	Delay from DEVSEL to FLAG			200	ns
4	t_{dc}	Delay from DEVSEL to C1, C2			215	ns
5	t_{di}	Delay from DEVSEL to SKP/INT			215	ns
6	t_{da}	Delay from DEVSEL to DX			215	ns
7	t_{lxmar}	LXMAR Pulse Width	120			ns
8	t_{as}	Address Setup Time	40			ns
9	t_{ah}	Address Hold Time	50			ns
10	t_{ds}	Data Setup Time	65			ns
11	t_{dh}	Data Hold Time	50			ns

Note: See Figure 2 for an A.C. Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6101AM .... -55°C to +125°C
Storage Temperature .... -65°C to 150°C
Operating Voltage .... 4.0V to 11.0V
Supply Voltage .... +12.0V
Voltage On Any Input or
Output Pin .... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage	$GND \le V_{IN} \le V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OLK}	Output Leakage	$GND \le V_{OUT} \le V_{CC}$	-1.0		1.0	μA
7	I_{CCSB}	Power Supply Current—Standby	V_{CC}=10V±5%		1.0	500	μA
8	I_{CCOP}	Power Supply Current—Dynamic	V_{CC}=10V±5% f=571 kHz			2.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -55°C to +125°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{dr}	Delay from DEVSEL to READ			165	ns
2	t_{dw}	Delay from DEVSEL to WRITE	50		165	ns
3	t_{df}	Delay from DEVSEL to FLAG			220	ns
4	t_{dc}	Delay from DEVSEL to C1, C2			240	ns
5	t_{di}	Delay from DEVSEL to SKP/INT			240	ns
6	t_{da}	Delay from DEVSEL to DX			240	ns
7	t_{lxmar}	LXMAR Pulse Width	135			ns
8	t_{as}	Address Setup Time	45			ns
9	t_{ah}	Address Hold Time	55			ns
10	t_{ds}	Data Setup Time	70			ns
11	t_{dh}	Data Hold Time	55			ns

Note: See Figure 2 for an A.C. Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
 Industrial IM6101-1I .... -40°C to +85°C
Storage Temperature .... -65°C to 150°C
Operating Voltage .... 4.0V to 7.0V
Supply Voltage .... +8.0V
Voltage On Any Input or
 Output Pin .... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CCSB}	Power Supply Current—Standby	V_{CC} = 5V ± 10%		1.0	100	μA
8	I_{CCOP}	Power Supply Current—Dynamic	V_{CC}=5V±10% f=330 kHz			500	μA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{dr}	Delay from DEVSEL to READ			300	ns
2	t_{dw}	Delay from DEVSEL to WRITE	100		300	ns
3	t_{df}	Delay from DEVSEL to FLAG			375	ns
4	t_{dc}	Delay from DEVSEL to C1, C2			460	ns
5	t_{di}	Delay from DEVSEL to SKP/INT			460	ns
6	t_{da}	Delay from DEVSEL to DX			460	ns
7	t_{lxmar}	LXMAR Pulse Width	240			ns
8	t_{as}	Address Setup Time	80			ns
9	t_{ah}	Address Hold Time	125			ns
10	t_{ds}	Data Setup Time	80			ns
11	t_{dh}	Data Hold Time	100			ns

Note: See Figure 2 for an A.C. Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6101-IM .... -55°C to +125°C
Storage Temperature .... -65°C to 150°C
Operating Voltage .... 4.0V to 7.0V
Supply Voltage .... +8.0V
Voltage On Any Input or
Output Pin .... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND≤V_{IN}≤V_{CC}	-1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	µA
7	I_{CCSB}	Power Supply Current—Standby	V_{CC} = 5V ± 10%		1.0	100	µA
8	I_{CCOP}	Power Supply Current—Dynamic	V_{CC}=5V±10% f=330 kHz			500	µA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{dr}	Delay from DEVSEL to READ			330	ns
2	t_{dw}	Delay from DEVSEL to WRITE	100		330	ns
3	t_{df}	Delay from DEVSEL to FLAG			415	ns
4	t_{dc}	Delay from DEVSEL to C1, C2			510	ns
5	t_{di}	Delay from DEVSEL to SKP/INT			510	ns
6	t_{da}	Delay from DEVSEL to DX			510	ns
7	t_{lxmar}	LXMAR Pulse Width	265			ns
8	t_{as}	Address Setup Time	90			ns
9	t_{ah}	Address Hold Time	140			ns
10	t_{ds}	Data Setup Time	80			ns
11	t_{DH}	Data Hold Time	110			ns

Note: See Figure 2 for an A.C. Timing Diagram.

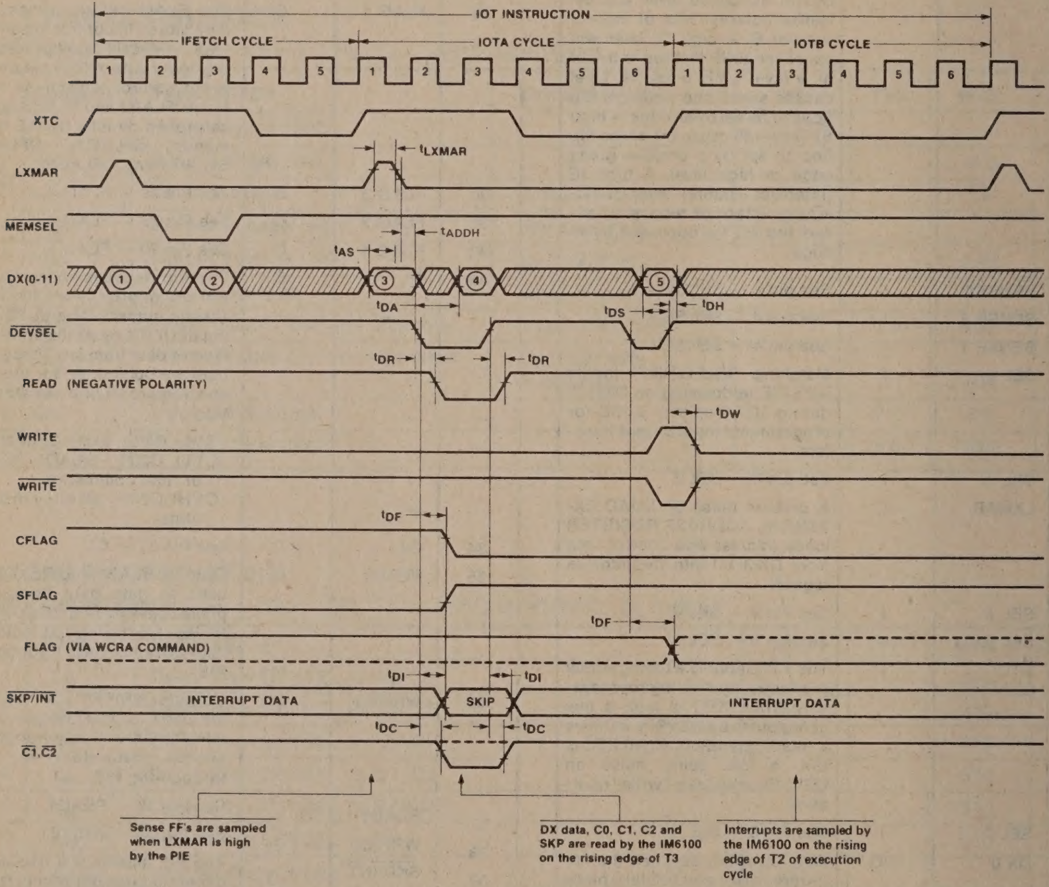
IM6101 FUNCTIONAL DESCRIPTION

Pin Number	Symbol	Input/ Output	Description
1	Vcc		+5 volts
2	INTGNT	I	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	I	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	I	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the SKIP flip flop to be set by a level while a low SL level causes sense and interrupt flip flops to be set by an edge. A high SP level will cause the sense flip flop to set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the INT flip flop is set (by an edge).
5	SENSE 3	I	See pin 4 — SENSE 4
6	SENSE 2	I	See pin 4 — SENSE 4
7	SENSE 1	I	See pin 4 — SENSE 4
8	SEL 3	I	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.
9	SEL 4	I	See pin 8 — SEL 3
10	LXMAR	I	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	I	See Pin 8 — SEL 3
12	SEL 6	I	See Pin 8 — SEL 3
13	XTC	I	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on DEVSEL initiates a "read" operation. When XTC is low, a low going pulse on DEVSEL initiates a "write" operation.
14	SEL 7	I	See Pin 8 — SEL 3
15	DX 0	I/O	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	I/O	See Pin 15 — DX 0
17	DX 2	I/O	See Pin 15 — DX 0
18	DX 3	I/O	See Pin 15 — DX 0
19	DX 4	I/O	See Pin 15 — DX 0
20	DX 5	I/O	See Pin 15 — DX 0
21	DX 6	I/O	See Pin 15 — DX 0
22	DX 7	I/O	See Pin 15 — DX 0
23	DX 8	I/O	See Pin 15 — DX 0

Pin Number	Symbol	Input/ Output	Description
24	DX 9	I/O	See Pin 15 — DX 0
25	DX 10	I/O	See Pin 15 — DX 0
26	DX 11	I/O	See Pin 15 — DX 0
27	GND		
28	$\overline{\text{DEVSEL}}$	I	The DEVSEL input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	O	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	O	See Pin 29 — FLAG 4
31	FLAG 2	O	See Pin 29 — FLAG 4
32	FLAG 1	O	See Pin 29 — FLAG 4
33	$\overline{\text{C1}}$ —	O	The PIE decodes address, control and priority information and asserts outputs C1 and C2 during the IOTA cycle to control the type of data transfer. These outputs are open drain for bussing and require pullup resistors to Vcc. C1(L), C2(L) - vectored interrupt C1(L), C2(H) - READ1, READ3 or RRA commands C1(H), C2(H) - all other instructions
34	C2	O	See Pin 33 — C1
35	READ1	O	Outputs READ1 and READ2 are used to gate data from peripheral devices onto the DX bus for input to the IM6100. Note the data does not pass through the PIE.
36	WRITE1	O	Outputs WRITE1 and WRITE2 are used to gate data from the IM6100 DX bus into peripheral devices. Data does not pass through the PIE.
37	READ2	O	See Pin 35 — READ1
38	WRITE2	O	See Pin 36 — WRITE1
39	$\overline{\text{SKP/INT}}$	O	The PIE asserts this line low to generate interrupt requests and to signal the IM6100 when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	O	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PRIN input of the next lower priority PIE in the chain.

TIMING DIAGRAM

Timing for a typical IOT transfer is shown in Figure 2. During the IFETCH cycle, the processor obtains from memory an IOT instruction of the form 6XXX. During the IOTA the processor places that instruction back on the DX lines ③ and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is high ④ is used by the addressed PIE along with decoded control information to generate $\overline{\text{C1}}$, $\overline{\text{C2}}$, $\overline{\text{SKP}}$ and controls for data transfers to the processor. Control outputs READ1 and READ2 are used to gate peripheral data to the DX lines during this time. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is low ⑤ is used to generate WRITE1 and WRITE2 controls. These signals are used to clock processor accumulator data into peripheral devices.


IOT INSTRUCTION
IFETCH CYCLE
IOTA CYCLE
IOTB CYCLE
1 2 3 4 5 1 2 3 4 5 6 1 2 3 4 5 6
XTC
t_{LXMAR}
LXMAR
$\overline{\text{MEMSEL}}$
t_{ADDH}
t_{AS}
DX(0-11)
① ② ③ ④ ⑤
t_{DA}
t_{DS}
t_{DH}
$\overline{\text{DEVSEL}}$
t_{DR}
t_{DR}
READ (NEGATIVE POLARITY)
t_{DW}
WRITE
$\overline{\text{WRITE}}$
t_{DF}
CFLAG
SFLAG
t_{DF}
FLAG (VIA WCRA COMMAND)
t_{DI}
t_{DI}
$\overline{\text{SKP}}/\overline{\text{INT}}$
INTERRUPT DATA
SKIP
INTERRUPT DATA
t_{DC}
t_{DC}
$\overline{\text{C1}},\overline{\text{C2}}$

Sense FF's are sampled when LXMAR is high by the PIE

DX data, C0, C1, C2 and SKP are read by the IM6100 on the rising edge of T3

Interrupts are sampled by the IM6100 on the rising edge of T2 of execution cycle

FIGURE 2. IM6101 PIE Timing Diagram.

All PIE timing is generated from IM6100 signals LXMAR, $\overline{\text{DEVSEL}}$, and XTC. No additional timing signals, clocks, or one shots are required. Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the IM6100.

PIE ADDRESS AND INSTRUCTIONS

The IM6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle (See Figure 1) an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIE's. Address zero is reserved for IOT's internal to the IM6100. The four control bits are decoded to select one of 16 instructions. Note also that the IOT instructions 66XX are reserved for the Parallel Input/Output Port (P10 - IM6103).

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	ADDRESS					CONTROL			

FIGURE 3. PIE Instruction Format.

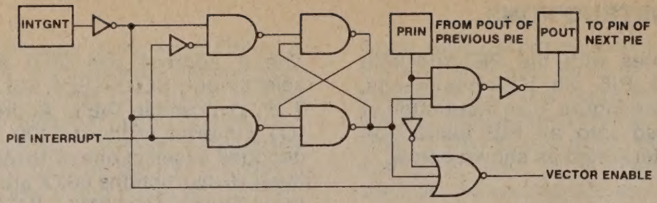
CONTROL	MNEMONICS	DESCRIPTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate data onto the DX bus to be "OR'ed" with the IM6100 accumulator data.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the IM6100 accumulator data on the DX lines into peripheral data registers.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the SKP/INT output causing the IM6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE does not assert the SKP/INT output and the IM6100 will execute the next instruction.
0100	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time ④ to be "OR" transferred to the IM6100 AC. (See Figure 2)
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer IM6100 AC data on the DX lines during time ⑤ of IOTA into the appropriate register. (See Figure 2) Bits 10, 11 of the VR;5, 7 of CRA; 8-11 of CRB are don't care bits for these instructions.
0110 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	IM6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops. It has no effect on control register output flags FL1, FL2, FL3, FL4. To clear these output flags, bits 0-3 of CRA must be cleared using WCRA with bits 0-3 of AC cleared.

PRIORITY FOR VECTORED INTERRUPT

A hardware priority network uniquely selects a PIE to provide a vectored address. *The first IOT command of any type,* after the IM6100 signal INTERRUPT GRANT goes high, resets the line INTGNT to a low level. The signal INTGNT is used to freeze the priority network and enable vector generation. Within a given PIE, the internal priority is interrogated during every LXMAR.

The highest priority PIE has PRIN tied to Vcc. The lowest priority PIE is the last one on the chain. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt.

A. Daisy-chaining of several PIE chips.



B. Interrupt Vector Register Format.

0	1	2	3	4	5	6	7	8	9	10	11
INTERRUPT VECTOR										SPRI	

SPRI: Sense Priority

SPRI	Conditions*
00	SENSE1
01	SENSE2 and not SENSE1
10	SENSE3 and not (SENSE2 or SENSE1)
11	SENSE4 and not (SENSE3 or SENSE2 or SENSE1)

*All sense input lines are enabled for interrupts.

FIGURE 4. IM6101 Priority for Vectored Interrupt.

I/O CONTROL LINES (C1 AND C2)

The type of input-output transfer is controlled by the selected PIE by activating the $\overline{C1}$, $\overline{C2}$ lines as shown below. These outputs are open drain.

$\overline{C1}$	$\overline{C2}$	
H	H	DEV/PIE ← AC Write
L	H	AC ← AC + DEV/PIE "OR" Read
L	L	PC ← VECTOR ADDRESS Vectored Interrupt

INTERRUPT/SKIP (INT/SKP)

Interrupt and skip information are time multiplexed on the same lines. Since the IM6100 samples skip and interrupt data at separate times (see Figure 1) there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits on the rising edge of $\overline{LXMAR}$. Interrupt requests are asserted by driving the $\overline{INT/SKP}$ line low. During IOTA of SKIP instructions the INT/SKP reflects the SENSE flip flop data.

If the SENSE flip flop is set, the INT/SKP line is driven low to cause the IM6100 to skip the next instruction. This output is open drain.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the IM6100 via the RCRA and WCRA commands. The format and meaning of control bits are shown below.

0	1	2	3	4	5	6	7	8	9	10	11
FL4	FL3	FL2	FL1	WP2	*	WP1	*	IE4	IE3	IE2	IE1

* Don't care for WCRA, 0 for RCRA

FIGURE 5. Format for Control Register A.

FL(1-4)

Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits in CRA changes the corresponding FLAG output.

WP(1,2)

A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs (see Figure 1).

IE(1-4)

A high level on INTERRUPT ENABLE enables interrupts.

CONTROL REGISTER B

The CRB can be written by the IM6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown below. Bits 8-11 are don't care bits.

0	1	2	3	4	5	6	7
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1

FIGURE 6. Format for Control Register B.

SL(1-4)

A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level on the SL bits causes the SENSE inputs to be edge sensitive. The INT FFs are set only if a sense line is set up to be edge sensitive.

SP(1-4)

A high level on the SENSE POLARITY bits causes the SKIP flip flop to be set by a high level or positive going edge. A low level causes the SKIP flip flop to be set by a low level or negative going edge.

PERIPHERAL INTERFACE LINES

SENSE(1-4)

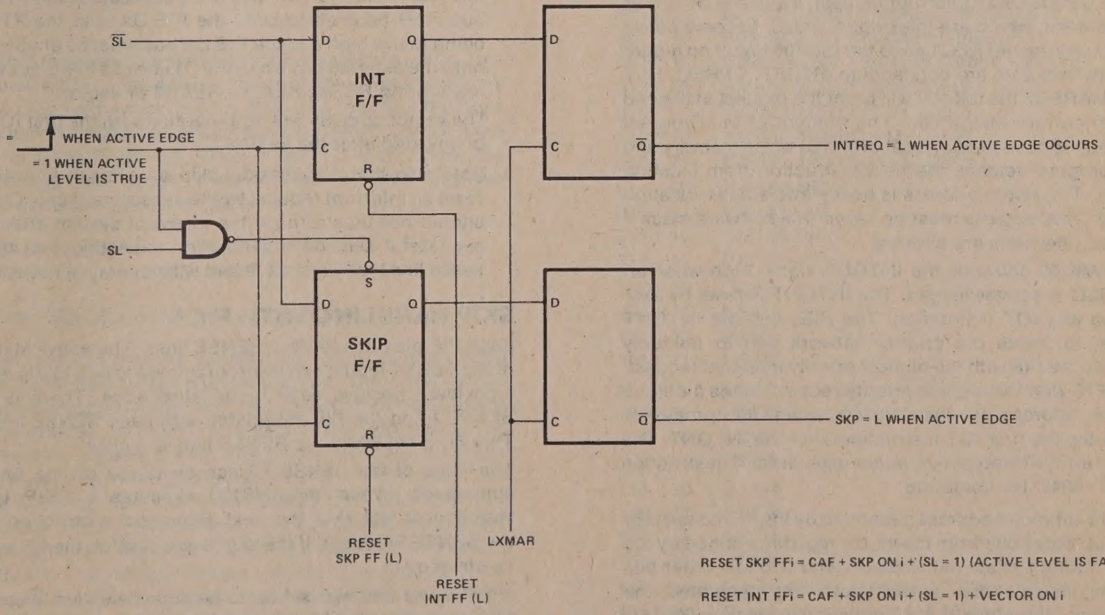
The IM6101 has two latches associated with each sense input — a SKIP flip flop and an INTERRUPT flip flop.

For the Interrupt flip flop to be set, the corresponding interrupt enable bit must be set to 'one'. If the sense input is programmed to be edge sensitive, the flip flop is set when the edge occurs. If it was initially programmed to be level sensitive and then the mode is changed to be edge sensitive, the flip flop will be set if the polarity of sense input line corresponds to its SP bit.

All conditions that set the Interrupt flip flop also set the associated Skip flip flop. In addition, the Skip flip flop is set when the polarity of the sense input corresponds to its SP bit in the level sensitive mode.

The Skip flip flop is cleared at IOTA READ time by executing a CAF (6007) instruction or a SKIP instruction on the associated sense input that actually skips. In the level sensitive mode, whenever the polarity of sense input does not correspond to its SP bit, the sense FF is cleared.

The Interrupt flip flop is cleared whenever the sense flip flop is cleared. In addition, it is cleared if the associated sense logic actually creates a vector, the interrupt enable bit is cleared to a 'zero' or the sense input is programmed to be level sensitive. Detailed operation of resetting Interrupt and Skip flop flops are as shown in Figure 7.



RESET SKP FFi = CAF + SKP ON i + (SL = 1) (ACTIVE LEVEL IS FALSE)

RESET INT FFi = CAF + SKP ON i + (SL = 1) + VECTOR ON i

Figure 7. IM6101 SKIP Flip Flop and INTERRUPT Flip Flop Input Diagram.

APPLICATIONS

INTRODUCTION

The IM6101, Programmable Interface Element (PIE), provides a universal means of interfacing industry standard LSI devices and peripheral equipment controllers to the IM6100 Microprocessor.

The IM6100 configures each PIE for a specific interface during system initialization by programming the control registers within the PIE for write enable polarities, sense polarities, sense edges or levels, flag values and interrupt enables. On power-up, the registers will contain random bit patterns.

The data transfer between the IM6100 and the peripheral devices does not take place through the PIE. The programmable Interface Element provides the steering signals for data transfers. This approach was chosen since all the standard LSI elements such as Keyboard chips, UARTs, FIFOs, etc. have internal storage latches and they require only control signals to take data from the bus or to put data on the bus. If some user defined peripheral interfaces do not have these built-in storage elements, discrete CMOS or low power Schottky latches, or flip-flops, must be provided to store the data from the IM6100 until the peripheral device is ready to accept it and to latch data from the peripheral devices until the IM6100 asks for it.

INTERRUPT PROCESSING WITH PIE'S

The PIEs provide for a vectored priority interrupt scheme. Up to 31 PIEs may be chained to obtain 124 interrupt lines. The microprocessor will recognize, identify and start servicing the highest priority interrupt request within 36.6μs at 3.3MHz.

The INTREQ lines from all PIEs are wire-ANDed together. A PIE generates an interrupt request, if any one of its four sense lines, which are interrupt enabled, become active by driving the INTREQ line to the IM6100 low. If no higher priority requests are outstanding (RESET, CPREQ, HLT or DMAREQ), the IM6100 will grant the request at the end of the current instruction. The content of the Program Counter is deposited in location 0000_8 of the memory and the program fetches the next instruction from location 0001_8. The return address is hence available in location 0000_8. This address must be saved in a software stack if nested interrupts are allowed.

The IM6100 activates the INTGNT signal high when an INTREQ is acknowledged. The INTGNT is reset by executing any IOT instruction. The PIEs use the INTGNT signal to freeze the priority network and to uniquely specify the PIE with the highest priority interrupt request. The PIE with the highest priority request sends a unique vector address to the IM6100 when the processor executes the first IOT instruction after the INTGNT. The Interrupt II Prototyping System uses the IOT instruction VECT (6047) for Vectoring.

The 12-bit vector address generated by the PIE consists of 10 high order bits from the vector register, defined by the user during system initialization, and two low order bits which indicate the sense input that generated the interrupt. Therefore, if the instruction in location 0001_8 is VECT-6047_8, the processor will branch to 1 of 4 locations, depending on which of the sense lines within a PIE generated the request. Each one of these locations must contain a Jump instruction pointing to the specific service routine for the corresponding sense input. The 36.6μs interrupt acknowledge time at 3.3 MHz consists of 17μs (max) to recognize an interrupt request, 3.6μs to grant an interrupt request, 10μs to execute the VECT for vectoring and 6.0μs to execute a Jump instruction to a specific service routine.

Proper vectoring requires the following conditions:

1. The IM6100 must be enabled for interrupts with the ION command.
2. The INTGNT output of the IM6100 must be connected to the INTGNT of all the PIEs and the PRIN of the PIE with the highest priority must be connected to VCC and its PROUT should be connected to the PRIN of the PIE with the next highest priority and so on.
3. The IE bit of the sense line that is expected to generate the interrupt must be set to 1.
4. The sense line must be programmed to be edge sensitive. If a sense line is programmed to be level sensitive, it will not generate an INTREQ nor will it generate a vector.
5. The vector register of the PIE must be initialized with the proper vector. Note that the two least significant bits are generated by the PIE itself.
6. The $\overline{C1}$ and $\overline{C2}$ lines of all the PIEs must be wired together with the $\overline{C1}$ and $\overline{C2}$ of the IM6100 and pull up resistors must be provided on these lines since the PIE $\overline{C1}$ and $\overline{C2}$ outputs are open drain. The $\overline{SKP/INT}$ line of the PIE must be wired with the INT and SKP lines of the IM6100. If the PIE DX lines are buffered, the external bus must be enabled onto the PIE DX with the XTB being active high and the PIE DX bus must be enabled onto the external bus when the C1 line of a PIE is active low (during RCRA, READ1, READ2 or vector).
7. The vector address will be generated with the first IOT of any kind after the INTGNT.
8. Note also that a successful skip on a sense line will reset an interrupt request by the sense line, if any. One should not thus turn on the interrupt system after a successful skip on a sense line expecting that the sense line that was just tested will generate a request.

SKIP HANDLING WITH PIE'S

Each PIE provides for four SENSE lines. The active state of the SENSE inputs can be programmed to be a low level, high level, positive edge or negative edge. There is a SENSE FF in the PIE associated with each SENSE line. This FF is set when the SENSE line is "active".

The state of the SENSE FF can be tested by the SKP commands. When the IM6100 executes a SKIP instruction, it will skip the next sequential instruction if the SENSE FFi is set. If the skip is successful, the FF will be cleared.

If the sense line was set up to be edge sensitive, it can, therefore, be tested for the 'set' state only once. If the FF is set by a level, it will be cleared by the successful skip and then, set immediately by the active level.

If the SENSE FF was set by an edge, and the respective IE bit is enabled, the PIE will generate an INTREQ to the IM6100. Provided the priority conditions are met, the PIE will supply the vector address to the IM6100 when it executes the first IOT instruction of any kind, after the INTREQ has been granted. If the vector address is generated by FFi, one may still skip once on sense line i.

It should be noted that if priority vectoring is inhibited by grounding PRIN, an INTREQ will be cleared only if a SKIPi instruction is executed to test the FFi that generated the request. Note also that an INTREQ will not be generated if the sense line was set up to be level sensitive.

In certain instances, one may be interested in restoring the set state of a SENSE FF after it has been successfully tested and cleared and if the SENSE line has been programmed to be edge sensitive. For example, assume that SENSE1 is programmed to be positive edge sensitive (SL1 = 0, SP1 = 1). The transition from a 0 to 1 occurred; SENSE FF1 is set; SENSE1 is at a 1 level. SKIP1 instruction will clear SENSE FF1. The SENSE FF1 can be set, under program control, by creating an internal edge. This is accomplished, in this specific instance, by programming SP1 to a 0 and then back to a 1. Since SP1 is in CRB and it cannot be read from the PIE, the CRB constant must be stored in user memory, for example, location KCRB.

```
CLA
TAD KCRB     /Get CRB constant
AND K7740    /SP1 = 0
WCRB         /Write CRB to clear SP1
TAD K0020    /SP1 = 1
WCRB         /Write CRB to set SP1

KCRB, CRB    /CRB constant
K7740, 7740
K0020, 0020
```

Software systems employing Skip's on a Sense input while allowing the same input to create an Interrupt should pay attention to the fact that the Skip and Interrupt flip flops are synchronized by LXMAR from the IM6100. Since there is no LXMAR during IOTB of an I/O instruction, the following can occur. Assume that the following two instruction sequence is used:

```
SKIP SENSEX      /SENSE F/F SET?
JMP   .-1        /NO: WAIT FOR IT
```

Where SENSEX is also Interupt enabled.

Now, assume that the appropriate 'Edge' occurs during the fetch state of the Skip instruction. The Edge causes both flip flops to be set and the LXMAR produced at IOTA time creates an Interrupt request. The Skip instruction execution causes a Skip and clears the Skip flop flop. However, the Interrupt flip flop will not reflect the fact that the Skip flip flop has been cleared until after the next LXMAR occurs. So, the Interrupt request remains active during IOTB time since the IOTB cycle does not have a LXMAR. The IM6100 honors the Interrupt request since the next LXMAR doesn't occur until after the IOT is finished. The Interrupt servicing routine will not Skip again if it tries to find the device that created the Interrupt. Note that the proper Vector Address will still be generated.

PIE INSTRUCTION FORMAT

The IM6100 communicates with the PIEs using the Input-Output Transfer (IOT) instructions. The first three bits, 0-2, are always set to 6_8 (110) to specify an IOT instruction. The standard PDP-8/E™ convention is to set the next 6 bits, 3-8, to specify 1 of 64 I/O devices and then to control the operation of the selected I/O device by using bits 9-11. However, the PDP-8/E interfaces are not standardized since a specific pattern of bits 9-11 could specify completely different operations in different I/O devices. For example, the pattern 000 in bits 9-11 could mean a read operation for Interface A, a write operation for Interface B, a skip instruction for Interface C and so on since the operation for any IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

The IOT instruction format for the PIE is different from that used by PDP-8/E™ interfaces. The first three bits are, as usual, set to 6_8 to indicate an IOT instruction. The next 5 bits, 3-7, specify 1 of 31 PIEs and then the operation of the selected PIE is controlled by bits 8-11 in 16 uniquely specified ways. For example, the specific pattern 0000 in bits 8-11 means exactly the same operation for all PIEs, namely activate READ1 line.

Of the 32 possible combinations of bits 3-7, the pattern 00000 is reserved for internal Processor IOT instructions and hence not available as a PIE address.

Recommended address assignments for the IM6101-PIE (Programmable Interface Element) are as follows:

000	00	Internal IOT (600X) and DEC HS RDR (601X)
000	01	DEC HS PUNCH (602X) and DEC TTY Keyboard (603X)
000	10	DEC TTY PRINTER (604X)
000	11	INTERCEPT PIE-UART Serial Interface
001	00	INTERCEPT PIE-UART PRINTER Interface
001	01	IM6102-MEDIC REAL TIME CLOCK
001	10	Reserved for Intercept Option - 1
001	11	Reserved for Intercept Option - 2
010	00	IM6102-MEDIC EMC/DMA
010	01	IM6102-MEDIC EMC/DMA
010	10	IM6102-MEDIC EMC/DMA
010	11	IM6102-MEDIC EMC/DMA
011	00	IM6103-PIO
011	01	IN6103-PIO
011	10	IN6103-PIO
011	11	IN6103-PIO
100	00	USER
100	01	USER
100	10	USER
100	11	USER
101	00	USER
101	01	USER
101	10	USER
101	11	USER
110	00	USER
110	01	USER
110	10	USER
110	11	USER
111	00	Reserved for Intercept Option - 5
111	01	Reserved for Intercept Option - 4
111	10	Intercept FLOPPY DISK System (675X)
111	11	Reserved for Intercept Option - 3

PARAMETER	DEFINITION
Minimum Peripheral device write data setup time w.r.t. leading edge of WRITE	t_{WPD} (IM6100) + $t_{DW\ (MIN)}$ (IM6101) - t_{DSD} (IM6100)
Minimum Peripheral device write data hold time w.r.t. leading edge of WRITE	t_{DHD} (IM6100) + t_{WPD} (IM6100) - $t_{DW\ (MAX)}$ (IM6101)
Maximum Peripheral device read data enable time	t_{END} (IM6100) - t_{DR} (IM6101)

TIMING REQUIREMENTS ON PERIPHERAL DEVICES

The timing required on peripheral devices is affected by the combined delays of the IM6100 and IM6101 devices. The table above describes the peripheral device timing requirements with respect to the data given for the IM6100 and IM6101 AC characteristics.

The values at any operating frequency, temperature and/or power supply voltage can be evaluated by substituting the calculated values for the IM6100 and IM6101 parameters in the defining expressions.

ASYNCHRONOUS SERIAL INTERFACE WITH PIE AND UART

The IM6402/03 Universal Asynchronous Receiver/Transmitter is a general, purpose programmable serial device for interfacing an asynchronous serial data channel to a parallel synchronous data channel. The receiver converts a serial word with start, data, parity and stop bits to a parallel data word and checks for parity, framing and data overrun errors. The transmitter section converts a parallel data word into a serial word with start, data, parity and stop bits. The data word length may be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The number of stop bits may be 1 or 2 or 1 1/2 when transmitting a 5 bit code.

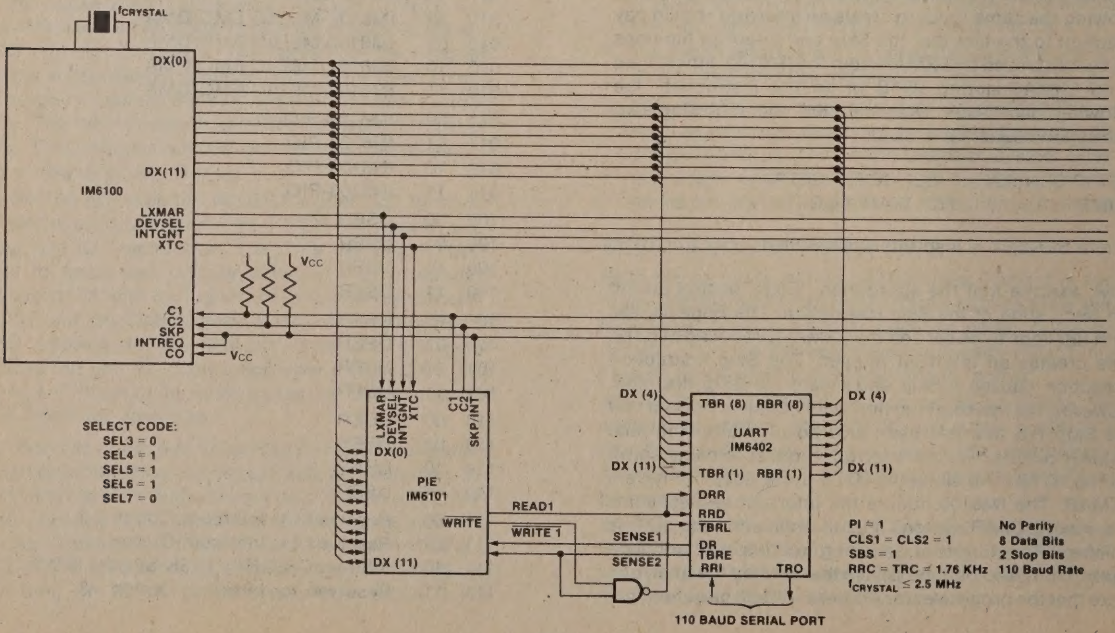
The IM6402/03 can be used in a wide variety of applications including interfacing modems, Teletype™ and remote data acquisition systems to the IM6100 microprocessor. The IM6403 makes provisions for a crystal oscillator and internal divider chain to specify the data transfer rate. In the IM6402 the data transfer rate is controlled by an external timing source, for example, a Baud Generator.

A functional block diagram of the PIE/UART/IM6100 interface is shown below. The UART is configured, in this specific example, to interface with an ASR-33 Teletype which has a data format that consists of 11 bits — a start bit, 8 data bits and 2 stop bits. The UART is clocked at 16X the data rate. For the 10 character per second ASR-33, the UART clock frequency would be 1.76 KHz.

An 8-bit data word from the IM6100 Accumulator is loaded into the Transmitter Buffer Register via inputs TBR8-TBR1 when the Transmit Buffer Register Load (TBRL) signal makes a zero to one transition. A high level on Transmit Buffer Register Empty (TBRE) indicates that the buffer is ready to accept a new character for transmission. The microprocessor checks the status of TBRE via SENSE2 before it transmits a new character to the UART by pulsing WRITE1. The start bit, data bits and stop bits appear serially at the Transmit Register Output (TRO).

A serial data stream on the Receiver Register Input (RRI) is clocked into the Receive Buffer Register. A high level on Data Received (DR) indicates that a character has been received. The contents of Receiver Buffer Register appear on the outputs RBR8-RBR1 when a low level is applied to Receiver Register Disable (RRD) input. The RBR outputs are tristated when RRD is high. A low level on Data Received Reset (DRR) clears the DR flag. RRD and DRR

PIE/UART/IM6100 INTERFACE


fCRYSTAL
DX(0)
DX(11)
IM6100
LXMAR
DEVSEL
INTGNT
XTC
Vcc
C1
C2
SKP
INTREQ
CO
Vcc
SELECT CODE:
SEL3 = 0
SEL4 = 1
SEL5 = 1
SEL6 = 1
SEL7 = 0
LXMAR
DEVSEL
INTGNT
XTC
C1
C2
SKP/INT
DX(0)
PIE
IM6101
WRITE
DX (11)
READ1
WRITE 1
SENSE1
SENSE2
DX (4)
DX (11)
TBR (8)
RBR (8)
UART
IM6402
TBR (1)
RBR (1)
DRR
RRD
TBRL
DR
TBRE
RRI
TRO
DX (4)
DX (11)
110 BAUD SERIAL PORT
PI = 1
CLS1 = CLS2 = 1
SBS = 1
RRC = TRC = 1.76 KHz
fCRYSTAL ≤ 2.5 MHz
No Parity
8 Data Bits
2 Stop Bits
110 Baud Rate

may be tied together to clear DR as the register data is being read. The microprocessor monitors the status of the DR flag via SENSE1 to see if a new character has been received before it reads the information stored in the buffer register by pulsing READ1 low.

The UART interface uses only the low order 8 bits of the IM6100 data bus (DX) to receive and transmit characters.

The NAND gate is used to load the UART with the leading edge of the WRITE pulse since the IM6100 data is valid only with respect to the leading edge at higher operating frequencies.

PIE CONTROL REGISTER ASSIGNMENTS FOR IM6402 UART INTERFACE:

	0	1	2	3	4	5	6	7	8	9	10	11
CRA	*	*	*	*	*	*	WP1	*	*	*	IE2	IE1

	0	1	2	3	4	5	6	7
CRB	*	*	SL2	SL1	*	*	SP2	SP1

WP1 = 0	Active low WRITE1 (TBRL)
IE2 = 1	Interrupt enable for SENSE2 (TBRE)
IE1 = 1	Interrupt enable for SENSE1 (DR) If vectored interrupts are used (PIN = 1 or is part of a priority chain) the Interrupt Vector Register must be loaded with the desired vector address.
SL2 = 0; SP2 = 1	SENSE2 (TBRE) active on 0 to 1 transition
SL1 = 0; SP1 = 1	SENSE1 (DR) active on 0 to 1 transition

PIE ADDRESS AND CONTROL ASSIGNMENTS:

EXTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
0 1 2 3 4 5 6 7 8 9 10 11 1 1 0 | 0 1 1 1 0 | 0 0 0 0 IOT Address READ1	6340	Activate RRD low to transfer Receiver Register contents onto the DX lines and clear the Data Received Flag.
1 1 0 | 0 1 1 1 0 | 0 0 0 1 WRITE1	6341	Activate TBRL low to transfer data from the DX lines to the Transmit Buffer Register.
1 1 0 | 0 1 1 1 0 | 0 0 1 0 SKIP1	6342	Skip the next instruction if the internal SENSE FF1 was set by a positive transition on Data Received (DR) and then clear SENSE FF1.
1 1 0 | 0 1 1 1 0 | 0 0 1 1 SKIP2	6343	Skip the next instruction if the internal SENSE FF2 was set by a positive transition on Transmit Buffer Register Empty (TBRE) and then clear Sense FF2.

INTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
0 1 2 3 4 5 6 7 8 9 10 11 1 1 0 | 0 1 1 1 0 | 0 1 0 0 IOT Address RCRA	6344	'OR' transfer Control Register A to the AC.
1 1 0 | 0 1 1 1 0 | 0 1 0 1 WCRA	6345	Transfer AC to Control Register A
1 1 0 | 0 1 1 1 0 | 1 1 0 1 WCRB	6355	Transfer AC to Control Register B
1 1 0 | 0 1 1 1 0 | 1 1 0 0 WVR	6354	Transfer AC (0-9) to Vector Register (0-9)

PIE Address and Control Assignments:

EXTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
0 1 2 3 4 5 6 7 8 9 10 11 1 1 0 1 0 1 0 0 0 0 1 0 IOT Address SKIP1	6502	Skip and clear if SENSE1 is low — used to detect the status of the receive line.
1 1 0 1 0 1 0 0 0 1 1 0 SFLAG1	6506	Set FLAG1 to put the transmit line high ("MARK")
1 1 0 1 0 1 0 0 0 1 1 1 CFLAG1	6507	Clear FLAG1 to put the transmit line low ("SPACE")
1 1 0 1 0 1 0 0 1 1 1 0 SFLAG3	6516	Set FLAG3 to enable the paper tape reader
1 1 0 1 0 1 0 0 1 1 1 1 CFLAG3	6517	Clear FLAG3 to disable the paper tape reader

INTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
0 1 2 3 4 5 6 7 8 9 10 11 1 1 0 1 0 1 0 0 0 1 0 0 IOT Address RCRA	6504	'OR' transfer Control Register A to AC
1 1 0 1 0 1 0 0 0 1 0 1 WCRA	6505	Transfer AC to Control Register A
1 1 0 1 0 1 0 0 1 1 0 1 WCRB	6515	Transfer AC to Control Register B
1 1 0 1 0 1 0 0 1 1 0 0 WVR	6514	Transfer AC (0-9) to Vector Register (0-9)

Subroutines for programmed IOT transfers:

Program Listing:

```
                                /REFER TO THE APPLICATION BULLETIN M008
                                 /"ROM BASED SUBROUTINE CALLS WITH THE
                                 /IM6100" FOR THE IMPLEMENTATION OF A
                                 /SOFTWARE STACK. THE ROUTINES IN THIS
                                 /NOTE ASSUME THAT THE SUBROUTINES
                                 /ARE RESIDENT IN RAM AND ARE CALLED BY
                                 /THE CONVENTIONAL JMS INSTRUCTION.


                                *3200

                                /INPUT-OUTPUT ROUTINES FOR UART
                                 /INPUT ROUTINE READS AN 8-BIT CHAR
                                 /FROM THE UART INTO THE AC RIGHT
                                 /JUSIFIED. THE OUTPUT ROUTINE XMTS
                                 /A CHAR FROM THE AC TO THE UART AND
                                 /THEN CLEARS THE AC.
                                        /USER DEFINED MNEMONICS
                                        RUART=6340      /READ UART DATA
                                        WUART=6341      /WRITE UART

                                        SKPDR=6342      /SKP IF DATA RECD
                                       SKPTBR=6343      /SKP IF XMT RDY

3200  0000  INPUT,  0                                   /ENTRY FOR SUBROUTINE
3201  6342          SKPDR
3202  5201          JMP .-1                             /WAIT FOR DATA READY

3203  7200          CLA
3204  6340          RUART                               /AC<= UART
3205  0207          AND K0377                           /STRIP 0-3
3206  5600          JMP I INPUT                         /RETURN

3207  0377  K0377,  0377



3210  0000  OUTPUT, 0
3211  6343          SKPTBR
3212  5211          JMP .-1                             /WAIT FOR XMT RDY

3213  6341          WUART
3214  7200          CLA                                 /WRITE UART & CLA
3215  5610          JMP I OUTPUT                        /RETURN
```

TELETYPE INTERFACE WITH PIE

A simple economical program controlled serial interface for a Teletype can be built using only the Programmable Interface Element. The interface uses one Sense line to receive serial data, one Flag line to transmit serial data and one Flag line to control the Teletype paper tape reader, as shown below. Timing for proper transmit pulse widths, setting and clearing FLAG1, and proper receiver sampling times, testing SENSE1, is created via software timing loops.

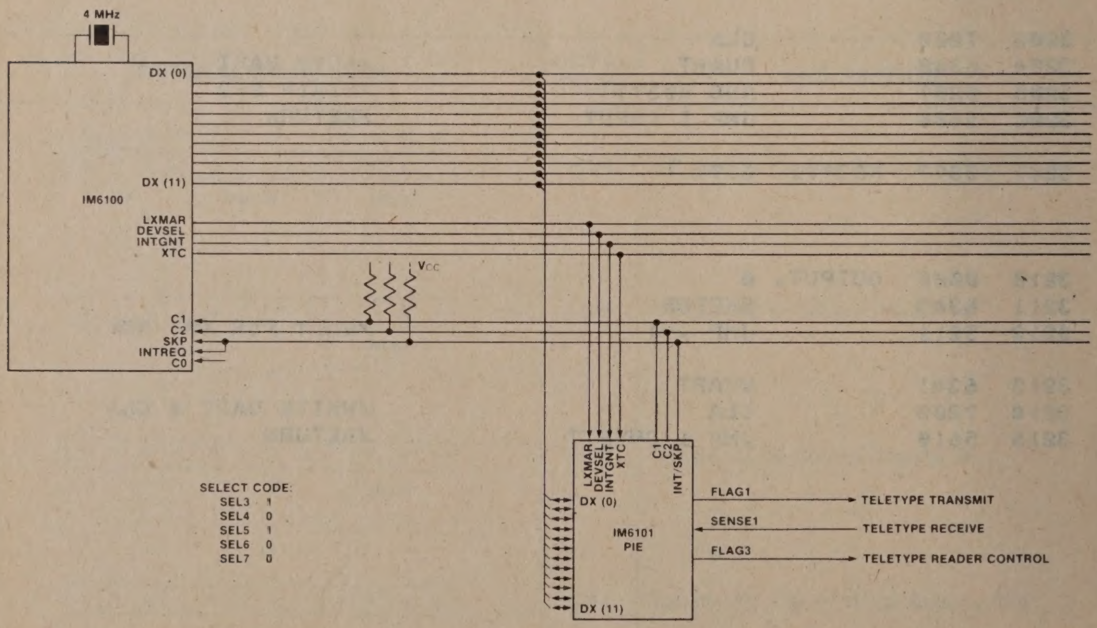
PIE Control Register Assignments

	0	1	2	3	4	5	6	7	8	9	10	11
CRA	•	•	•	•	•	•	•	•	•	•	•	•

	0	1	2	3	4	5	6	7
CRB	•	•	•	SL1	•	•	•	SP1

SL1 = 1; SP1 = 0 SENSE1 is level sensitive and active low.

IM6100/PIE/TELETYPE INTERFACE


4 MHz
IM6100
DX (0)
DX (11)
LXMAR
DEVSEL
INTGNT
XTC
Vcc
C1
C2
SKP
INTREQ
C0
LXMAR
DEVSEL
INTGNT
XTC
C1
C2
INT/SKP
DX (0)
IM6101
PIE
DX (11)
FLAG1
TELETYPE TRANSMIT
SENSE1
TELETYPE RECEIVE
FLAG3
TELETYPE READER CONTROL
SELECT CODE:
SEL3 1
SEL4 0
SEL5 1
SEL6 0
SEL7 0

Subroutines for programmed IOT transfers:

Transmit character routine:

The transmit routine takes an 8-bit character from the Accumulator and transmits it to the Teletype via FLAG1. FLAG1 is initially set high or "mark". For each character, the program sends out a start bit ("space" - zero), 8 data bits with the least significant bit first and 2 stop bits ("mark" - one).

Program listing:

```
                    /TELETYPE XMT ROUTINE
                     /FLAG1 IS INITIALISED TO 1(MARK)
                     /CHAR TO BE XMTED IN AC4-11
                     /NOMINAL BIT TIME 9.09 MS
                     /4MHZ OPERATION FOR IM6100
                     /AC AND L CLEARED AFTER XMT

                            /USER DEFINED MNEMONICS

                            TMARK=6506       /XMT MARK (1)
                            TSPACE=6507      /XMT SPACE(0)

                    *3000

3000  0000  XMT,    0
3001  3160          DCA TEMP1        /SAVE AC
3002  1235          TAD M8
3003  3161          DCA TEMP2        /-8 IN TEMP2
3004  1160          TAD TEMP1        /RESTORE AC

3005  6507          TSPACE           /START BIT
3006  4225          JMS DELAY        /TIME OUT BIT

                            /XMT 8 DATA BITS LSB FIRST
3007  7010  LOOP,   RAR              /XMT BIT IN L
3010  7430          SZL
3011  5214          JMP .+3          /JMP IF 1

3012  6507          TSPACE           /XMT 0
3013  7410          SKP

3014  6506          TMARK            /XMT 1

3015  4225          JMS DELAY        /TIME OUT BIT
                                     /9.082 MS NOMINAL <.1% ERROR

3016  2161          ISZ TEMP2
3017  5207          JMP LOOP         /XMT 8 BITS

3020  6506          TMARK            /STOP BIT
3021  4225          JMS DELAY
3022  4225          JMS DELAY        /2 STOP BITS

3023  7300          CLA CLL
3024  5600          JMP I XMT        /RETURN

3025  0000  DELAY,  0000             /9.043 MS
3026  3160          DCA TEMP1        /SAVE AC
3027  1236          TAD M693
3030  3162          DCA TEMP3        /-693 IN TEMP3
3031  1160          TAD TEMP1        /RESTORE AC

3032  2162          ISZ TEMP3
3033  5232          JMP .-1          /TIME OUT LOOP
                                     /9.009 MS

3034  5625          JMP I DELAY      /RETURN

3035  7770  M8,     7770
3036  6513  M693,   6513

                    *160
0160  0000  TEMP1,  0000
0161  0000  TEMP2,  0000
0162  0000  TEMP3,  0000
```

Receiver character routine:

The receive routine accepts a serial data string from the Teletype which consists of a start bit, 8 data bits with the least significant bit first and 2 stop bits and assembles them, right justified, into an 8-bit word in the Accumulator. Each bit is sampled in the middle of the bit interval. The user can read character by character from the Teletype reader by turning the reader off after receiving each character and then reenabling it under program control to fetch the next character in sequence. The routine assumes that the program is waiting for a character from the Teletype.

Program listing:

```
                                 *3100
                                 /TELETYPE RECEIVE ROUTINE
                                  /SENSE1 IS INITIALISED TO BE LEVEL
                                        /SENSITIVE AND ACTIVE LOW
                                  /AC AND L ARE CLEARED. CHAR IN AC 4-11

                                        /USER DEFINED MNEMONICS

                                        SKPLOW=6502      /SKP IF TTY IN IS 0
                                        RDRON=6516       /ENABLE RDR
                                        RDROFF=6517      /RDR OFF

           3100   0000   RCVE,    0000
           3101   7300            CLA CLL
           3102   1235            TAD M8
           3103   3161            DCA TEMP2        /-8 IN TEMP2

           3104   6516            RDRON            /ENABLE RDR

           3105   6502   START,   SKPLOW
           3106   5305            JMP .-1          /WAIT FOR START BIT

           3107   1330            TAD M349
           3110   3162            DCA TEMP3        /-349 IN TEMP3

           3111   2162            ISZ TEMP3
           3112   5311            JMP .-1          /1/2 BIT DELAY
                                                   /4.532 MS

           3113   6502            SKPLOW
           3114   5305            JMP START        /FALSE START BIT

           3115   6517            RDROFF           /GOOD START BIT
                                                   /TURN OFF RDR
           3116   4225   DATA,    JMS DELAY        /FULL BIT DELAY TO THE
                                                   /MIDDLE OF NEXT BIT
                                                   /<.15% ERROR
           3117   7100            CLL
           3120   6502            SKPLOW
           3121   7020            CML              /L=1 IF MARK
           3122   7010            RAR

           3123   2161            ISZ TEMP2
           3124   5316            JMP DATA         /RCVE 8 BITS

           3125   7012            RTR
           3126   7012            RTR              /RIGHT JUSIFY

           3127   5700            JMP I RCVE       /RETURN

           3130   7243   M349,    7243
```

IM6102
Memory Extension/ DMA Controller/ Interval Timer (MEDIC)

FEATURES

- **Provides Extended Memory Address to 32K Words**
- **Simultaneous DMA — Provides Simultaneous DMA Channel that Uses DX Bus During Second Half of a Cycle to Access Memory**
- **DMA Channel Can be Used for Dynamic RAM Refresh**
- **12-Bit Programmable Interval Timer**
- **Direct Interface with IM6100 Microprocessor Via Bidirectional DX Bus and Handshake Lines**
- **Hardware Reset**
- **28 Different I/O Instructions**

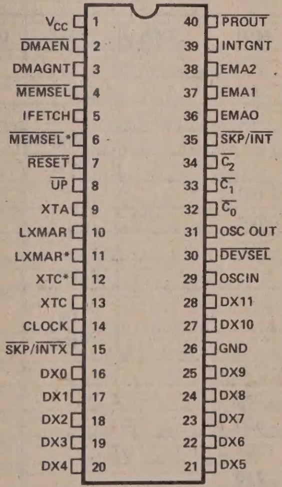
GENERAL DESCRIPTION

The IM6102 is a multi-function peripheral controller chip incorporating functions such as memory extension, direct memory access control, and a programmable real time clock.

The IM6102 provides necessary control to address up to 32K words of memory, and its DMA channel can be used with Dynamic RAM Components for "transparent refresh". The programmable real time clock is 12-bit long, and its output frequency can be programmed for 5 decades.

It features a high degree of system integration, putting into one chip all the functions which are normally available in three or more LSI circuits. As a result of this large integration, the user can design and produce a compact microcomputer with minicomputer performance.

PIN CONFIGURATION (outline dwg DL, PL)

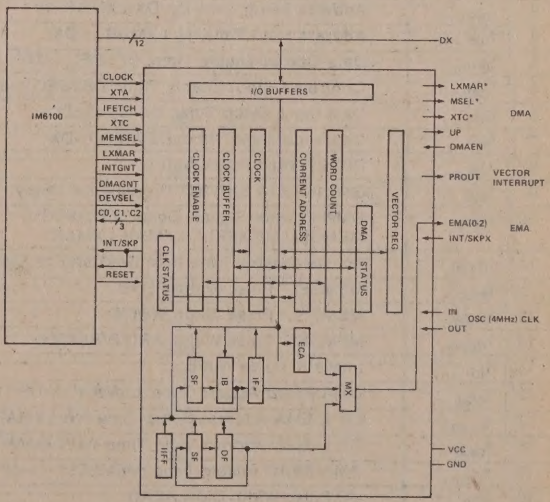


V_{CC} 1
$\overline{DMAEN}$ 2
DMAGNT 3
$\overline{MEMSEL}$ 4
IFETCH 5
$\overline{MEMSEL}$* 6
$\overline{RESET}$ 7
$\overline{UP}$ 8
XTA 9
LXMAR 10
LXMAR* 11
XTC* 12
XTC 13
CLOCK 14
$\overline{SKP/INTX}$ 15
DX0 16
DX1 17
DX2 18
DX3 19
DX4 20
40 $\overline{PROUT}$
39 INTGNT
38 EMA2
37 EMA1
36 EMA0
35 $\overline{SKP/INT}$
34 $\overline{C_2}$
33 $\overline{C_1}$
32 $\overline{C_0}$
31 OSC OUT
30 $\overline{DEVSEL}$
29 OSCIN
28 DX11
27 DX10
26 GND
25 DX9
24 DX8
23 DX7
22 DX6
21 DX5

ORDERING INFORMATION

ORDER CODE	IM6102-1	IM6102A	IM6102
PLASTIC PKG.	IM6102-1IPL	IM6102-AIPL	IM6102-IPL
CERAMIC PKG	IM6102-1IDL	IM6102-AIDL	IM6102-IDL
MILITARY TEMP.	IM6102-1MDL	IM6102-AMDL	—
MILITARY TEMP. WITH 883B	IM6102-1 MDL/883B	IM6102-AMDL/ 883B	—

BLOCK DIAGRAM



IM6100
12
DX
CLOCK
XTA
IFETCH
XTC
MEMSEL
LXMAR
INTGNT
DMAGNT
DEVSEL
C0, C1, C2
3
INT/SKP
RESET
I/O BUFFERS
CLOCK ENABLE
CLOCK BUFFER
CLOCK
CURRENT ADDRESS
WORD COUNT
DMA
STATUS
VECTOR REG
CLK STATUS
ECA
SF
IB
IF
MX
IIFF
SF
DF
LXMAR*
MSEL*
XTC*
UP
DMAEN
DMA
PROUT
VECTOR INTERRUPT
EMA(0-2)
INT/SKPX
EMA
IN
OUT
OSC (4MHz) CLK
VCC
GND

IM6102

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6102 .... -40° C to +85° C
Storage Temperature .... -65° C to 150° C
Operating Voltage .... +4.0V to +7.0V
Supply Voltage .... +8.0V
Voltage On Any Input or
Output Pin .... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = -40° C to +85° C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage(1)	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High(2)	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}		1.0	800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 2.5MHz			1.8	mA
9	C_{IN}	Input Capacitance(1)			7.0	8.0	pF
10	C_O	Output Capacitance(1)			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: 5.0V ± 10%, C_L = 50pF, T_A = -40°C to +85°C, f_C = 2.5MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{lin}	LXMAR Pulse Width IN	300			ns
2	t_{ais}	Address Setup Time IN: DX-LXMAR (↓)	80			ns
3	t_{aih}	Address Hold Time IN: LXMAR(↓)-DX	120			ns
4	t_{den}	Data Output Enable Time: DEVSEL(↓)-DX			400	ns
5	t_{cen}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			400	ns
6	t_{dis}	Data Input Setup Time: DX-DEVSEL(↑)	100			ns
7	t_{dih}	Data Input Hold Time: DEVSEL(↑)-DX	100			ns
8	t_{rst}	RESET Input Pulse Width	500			ns
9	t_{sid}	SKP/INTX to SKP/INT Propagation Delay			150	ns
10	t_{dmlx}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			150	ns
11	t_{dem}	Enable/Disable Time from DMAGNT to EMA Lines			100	ns
12	t_{mdr}	MEMSEL* Pulse Width READ	750			ns
13	t_{mdw}	MEMSEL* Pulse Width WRITE	950			ns
14	t_{mdwr}	MEMSEL* Pulse Width WRITE/REFSH	550			ns
15	t_{ld}	LXMAR* Pulse Width	350			ns
16	t_{drat}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	750			ns
17	t_{dxas}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	120			ns
18	t_{dxah}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	175			ns
19	t_{dren}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	550			ns
20	t_{rup}	UP Pulse Width DMA READ	350			ns
21	t_{dwat}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	750			ns
22	t_{dwen}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	550			ns
23	t_{mws}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	100			ns
24	t_{dms}	DMAEN Setup Time Wrt XTA (↑)	100			ns
25	t_{dmh}	DMAEN Hold Time Wrt XTA (↑)	100			ns
26	t_{wup}	UP Pulse Width DMA WRITE	750			ns

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
Industrial IM6102A	-40°C to +85°C
Storage Temperature	-65°C to 150°C
Operating Voltage	+4.0V to +11.0V
Supply Voltage	+12.0V
Voltage On Any Input or Output Pin	-0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 10V \pm 5\%$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	$GND \le V_{IN} \le V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High[2]	$I_{OH} = 0mA$	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	$I_{OL} = 0mA$			GND+0.01	V
6	I_{OLK}	Output Leakage	$GND \le V_{OUT} \le V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			900	μA
8	I_{CC}	Power Supply Current-Dynamic	$f_C = 5.71MHz$			4.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 10V \pm 5\%$, $C_L = 50pF$, $T_A = -40°C$ to $+85°C$, $f_C = 5.71MHz$

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{lin}	LXMAR Pulse Width IN	125			ns
2	t_{ais}	Address Setup Time IN: DX-LXMAR (↓)	50			ns
3	t_{aih}	Address Hold Time IN: LXMAR(↓)-DX	50			ns
4	t_{den}	Data Output Enable Time: DEVSEL(↓)-DX			240	ns
5	t_{cen}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			240	ns
6	t_{dis}	Data Input Setup Time: DX-DEVSEL(↑)	50			ns
7	t_{dih}	Data Input Hold Time: DEVSEL(↑)-DX	50			ns
8	t_{rst}	RESET Input Pulse Width	250			ns
9	t_{sid}	SKP/INTX to SKP/INT Propagation Delay			100	ns
10	t_{dmlx}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			100	ns
11	t_{dem}	Enable/Disable Time from DMAGNT to EMA Lines			50	ns
12	t_{mdr}	MEMSEL* Pulse Width READ	300			ns
13	t_{mdw}	MEMSEL* Pulse Width WRITE	380			ns
14	t_{mdwr}	MEMSEL* Pulse Width WRITE/REFSH	240			ns
15	t_{ld}	LXMAR* Pulse Width	150			ns
16	t_{drat}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	300			ns
17	t_{dxas}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	150			ns
18	t_{dxah}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	55			ns
19	t_{dren}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	210			ns
20	t_{rup}	UP Pulse Width DMA READ	150			ns
21	t_{dwat}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	300			ns
22	t_{dwen}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	210			ns
23	t_{mws}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	50			ns
24	t_{dms}	DMAEN Setup Time Wrt XTA (↑)	50			ns
25	t_{dmh}	DMAEN Hold Time Wrt XTA (↑)	50			ns
26	t_{wup}	UP Pulse Width DMA WRITE	300			ns

IM6102AM (Military)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6102AM .... -55°C to +125°C
Storage Temperature .... -65°C to 150°C
Operating Voltage .... +4.0V to +11.0V
Supply Voltage .... +12.0V
Voltage On Any Input or
Output Pin .... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 10V \pm 5\%$, $T_A = -55°C$ to $+125°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	$GND \le V_{IN} \le V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High[2]	$I_{OH} = 0mA$	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	$I_{OL} = 0mA$			GND+0.01	V
6	I_{OLK}	Output Leakage	$GND \le V_{OUT} \le V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			900	μA
8	I_{CC}	Power Supply Current-Dynamic	$f_C = 5.0MHz$			4.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 10V \pm 5\%$, $C_L = 50pF$, $T_A = -55°C$ to $+125°C$, $f_C = 5.0MHz$

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{lin}	LXMAR Pulse Width IN	135			ns
2	t_{ais}	Address Setup Time IN: DX-LXMAR (↓)	60			ns
3	t_{aih}	Address Hold Time IN: LXMAR(↓)-DX	60			ns
4	t_{den}	Data Output Enable Time: DEVSEL(↓)-DX			260	ns
5	t_{cen}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			260	ns
6	t_{dis}	Data Input Setup Time: DX-DEVSEL(↑)	60			ns
7	t_{dih}	Data Input Hold Time: DEVSEL(↑)-DX	60			ns
8	t_{rst}	RESET Input Pulse Width	250			ns
9	t_{sid}	SKP/INTX to SKP/INT Propagation Delay			120	ns
10	t_{dmlx}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			120	ns
11	t_{dem}	Enable/Disable Time from DMAGNT to EMA Lines			60	ns
12	t_{mdr}	MEMSEL* Pulse Width READ	375			ns
13	t_{mdw}	MEMSEL* Pulse Width WRITE	475			ns
14	t_{mdwr}	MEMSEL* Pulse Width WRITE/REFSH	275			ns
15	t_{ld}	LXMAR* Pulse Width	175			ns
16	t_{drat}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	375			ns
17	t_{dxas}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	70			ns
18	t_{dxah}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	70			ns
19	t_{dren}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	275			ns
20	t_{rup}	UP Pulse Width DMA READ	175			ns
21	t_{dwat}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	375			ns
22	t_{dwen}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	275			ns
23	t_{mws}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	50			ns
24	t_{dms}	DMAEN Setup Time Wrt XTA (↑)	50			ns
25	t_{dmh}	DMAEN Hold Time Wrt XTA (↑)	50			ns
26	t_{wup}	UP Pulse Width DMA WRITE	375			ns

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6102-1I .... -40° C to +85° C
Storage Temperature .... -65° C to 150° C
Operating Voltage .... +4.0V to +7.0V
Supply Voltage .... +8.0V
Voltage On Any Input or
Output Pin .... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = -40° C to +85° C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High[2]	I_{OH} = -0.2mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			GND+0.01	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 3.33MHz			2.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: 5.0V ± 10%, C_L = 50pF, T_A = -40° C to +85° C, f_C = 3.33MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{lin}	LXMAR Pulse Width IN	250			ns
2	t_{ais}	Address Setup Time IN: DX-LXMAR (↓)	70			ns
3	t_{aih}	Address Hold Time IN: LXMAR(↓)-DX	100			ns
4	t_{den}	Data Output Enable Time: DEVSEL(↓)-DX			350	ns
5	t_{cen}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			350	ns
6	t_{dis}	Data Input Setup Time: DX-DEVSEL(↑)	100			ns
7	t_{dih}	Data Input Hold Time: DEVSEL(↑)-DX	100			ns
8	t_{rst}	RESET Input Pulse Width	500			ns
9	t_{sid}	SKP/INTX to SKP/INT Propagation Delay			120	ns
10	t_{dmlx}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			120	ns
11	t_{dem}	Enable/Disable Time from DMAGNT to EMA Lines			80	ns
12	t_{mdr}	MEMSEL* Pulse Width READ	550			ns
13	t_{mdw}	MEMSEL* Pulse Width WRITE	700			ns
14	t_{mdwr}	MEMSEL* Pulse Width WRITE/REFSH	400			ns
15	t_{ld}	LXMAR* Pulse Width	260			ns
16	t_{drat}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	85			ns
17	t_{dxas}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	125			ns
18	t_{dxah}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	125			ns
19	t_{dren}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	400			ns
20	t_{rup}	UP Pulse Width DMA READ	260			ns
21	t_{dwat}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	550			ns
22	t_{dwen}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	400			ns
23	t_{mws}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	100			ns
24	t_{dms}	DMAEN Setup Time Wrt XTA (↑)	100			ns
25	t_{dmh}	DMAEN Hold Time Wrt XTA (↑)	100			ns
26	t_{wup}	UP Pulse Width DMA WRITE	550			ns

IM6102

IM6102-1M (Military)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6102-1M .... -55°C to +125°C
Storage Temperature .... -65°C to 150°C
Operating Voltage .... +4.0V to +7.0V
Supply Voltage .... +8.0V
Voltage On Any Input or
Output Pin .... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC} -2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage(1)	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High(2)	I_{OH} = 0mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			0.45	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 2.5MHz			2.0	mA
9	C_{IN}	Input Capacitance(1)			7.0	8.0	pF
10	C_O	Output Capacitance(1)			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31   2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C, f_C = 2.5MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{lin}	LXMAR Pulse Width IN	300			ns
2	t_{ais}	Address Setup Time IN: DX-LXMAR (↓)	80			ns
3	t_{aih}	Address Hold Time IN: LXMAR(↓)-DX	120			ns
4	t_{den}	Data Output Enable Time: DEVSEL(↓)-DX			400	ns
5	t_{cen}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			400	ns
6	t_{dis}	Data Input Setup Time: DX-DEVSEL(↑)	100			ns
7	t_{dih}	Data Input Hold Time: DEVSEL(↑)-DX	100			ns
8	t_{rst}	RESET Input Pulse Width	500			ns
9	t_{sid}	SKP/INTX to SKP/INT Propagation Delay			130	ns
10	t_{dmlx}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			130	ns
11	t_{dem}	Enable/Disable Time from DMAGNT to EMA Lines			100	ns
12	t_{mdr}	MEMSEL* Pulse Width READ	750			ns
13	t_{mdw}	MEMSEL* Pulse Width WRITE	950			ns
14	t_{mdwr}	MEMSEL* Pulse Width WRITE/REFSH	550			ns
15	t_{ld}	LXMAR* Pulse Width	350			ns
16	t_{drat}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	750			ns
17	t_{dxas}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	120			ns
18	t_{dxah}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	175			ns
19	t_{dren}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	550			ns
20	t_{rup}	UP Pulse Width DMA READ	350			ns
21	t_{dwat}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	750			ns
22	t_{dwen}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	550			ns
23	t_{mws}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	100			ns
24	t_{dms}	DMAEN Setup Time Wrt XTA (↑)	100			ns
25	t_{dmh}	DMAEN Hold Time Wrt XTA (↑)	100			ns
26	t_{wup}	UP Pulse Width DMA WRITE	750			ns

ARCHITECTURE

The IM6102 is composed of three distinct functions:

a) A DMA port that uses the bus during the second half of a cycle to read, write, or refresh memory. The DMA port logic includes a word count register WC, a current address register CA, an extended current address register ECA, and a DMA status register.

b) An extended memory address controller that augments the 12-bit addresses generated by the IM6100 microprocessor by supplying a 3-bit address field that may be decoded to select one of eight 4096 word memory fields. The memory extension controller logic consists of an instruction field register IF, a data field register DF, an instruction buffer register IB, and a save field register SF.

c) A realtime clock whose mode and time base rate may be programmed by the user. The clock logic includes a clock enable register CE, a clock buffer register CB, a clock counter register CC, and a time base multiplexer.

A block diagram of the IM6102 is shown in Figure 1.

The IM6102 registers are summarized as follows:

A. Simultaneous DMA Channel (Figure 3)

CURRENT ADDRESS (CA) REGISTER

This register is a 12-bit presettable binary counter. At the beginning of a SDMA transfer, the current address must be set to the first location to be accessed. The content of the CA register is incremented by 1 after a SDMA transfer, and the incremented value is used as the address of the memory location with which the next transfer will be performed.

EXTENDED CURRENT ADDRESS (ECA) REGISTER

This is a 3-bit presettable binary counter and if the carry enable bit of the DMA status register is set, the 12-bit CA register and the 3 ECA bits are treated as one 15-bit register with the ECA bits most significant. If memory field 7 (all 3 bits at logic one) is selected, the ECA cannot increment, but will wrap around in field 7 and an F7 error (F7E) will occur. The Interrupt Enable bit IE in SR11 must be set to enable F7E interrupts. If enabled the F7E will request an interrupt. If the carry enable bit CE in SR9 is not set, the ECA is not incremented when CA goes from 7777$_8$ to 0000$_8$.

WORD COUNT (WC) REGISTER

A 12-bit presettable binary counter is used as a word counter. At the beginning of a SDMA transfer, the two's complement of the number of 12-bit words to be transferred must be loaded into the WC. If enabled this will initiate the SDMA operation. The WC register is incremented by 1 after a SDMA transfer. If this value becomes zero, word count overflow has occurred and if the IE bit in SR11 is set, interrupts are enabled and an interrupt is requested. Unless instructed to be in the continuous run mode, a WC overflow inhibits further transfers. The WOF is set when the MSB of the WC register makes a "1" to "0" transition.

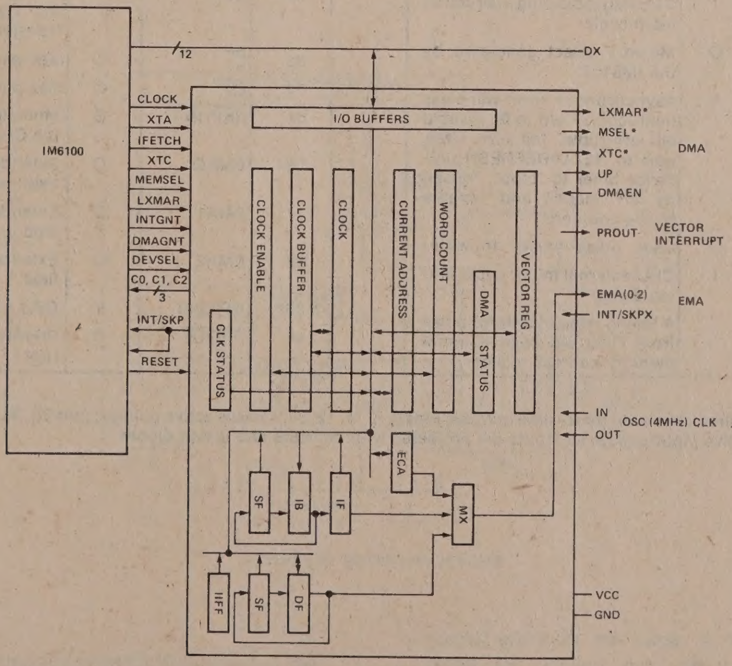
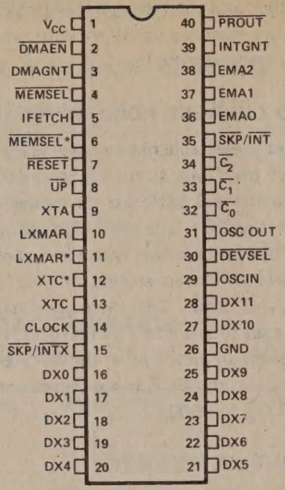

IM6100
12
DX
CLOCK
XTA
IFETCH
XTC
MEMSEL
LXMAR
INTGNT
DMAGNT
DEVSEL
C0, C1, C2
3
INT/SKP
RESET
I/O BUFFERS
CLOCK ENABLE
CLOCK BUFFER
CLOCK
CURRENT ADDRESS
WORD COUNT
DMA STATUS
VECTOR REG
CLK STATUS
ECA
SF
IB
IF
MX
IIFF
SF
DF
LXMAR*
MSEL*
XTC*
UP
DMAEN
DMA
PROUT
VECTOR INTERRUPT
EMA(0-2)
INT/SKPX
EMA
IN
OUT
OSC (4MHz) CLK
VCC
GND

FIGURE 1: IM6102 MEMORY EXTENSION/DMA/INTERVAL TIMER CONTROLLER (MEDIC)


V_{CC} 1
$\overline{\text{DMAEN}}$ 2
DMAGNT 3
$\overline{\text{MEMSEL}}$ 4
IFETCH 5
$\overline{\text{MEMSEL}}$* 6
$\overline{\text{RESET}}$ 7
$\overline{\text{UP}}$ 8
XTA 9
LXMAR 10
LXMAR* 11
XTC* 12
XTC 13
CLOCK 14
$\overline{\text{SKP/INTX}}$ 15
DX0 16
DX1 17
DX2 18
DX3 19
DX4 20
40 $\overline{\text{PROUT}}$
39 INTGNT
38 EMA2
37 EMA1
36 EMAO
35 $\overline{\text{SKP/INT}}$
34 $\overline{C_2}$
33 $\overline{C_1}$
32 $\overline{C_0}$
31 OSC OUT
30 $\overline{\text{DEVSEL}}$
29 OSCIN
28 DX11
27 DX10
26 GND
25 DX9
24 DX8
23 DX7
22 DX6
21 DX5

IM6102 FUNCTIONAL PIN DESCRIPTION

Pin Number	Symbol	Input/ Output	Description
1	Vcc		Supply voltage
2	$\overline{\text{DMAEN}}$	I	Enable the IM6102 DMA channel to transfer data
3	DMAGNT	I	Direct memory access grant from CPU
4	$\overline{\text{MEMSEL}}$	I	Memory select for read or write from CPU
5	IFETCH	I	CPU flag indicating instruction fetch cycle
6	$\overline{\text{MEMSEL}}$*	O	Memory select generated by the IM6102
7	$\overline{\text{RESET}}$	I	Asynchronous reset will clear Instruction Field to 0_8, disable all interrupts, initialize DMA port to READ/REFRESH, initialize timer to "stop", "divide by 2^{12} mode" and "enable divide counters"
8	$\overline{\text{UP}}$	O	User pulse (read or write)
9	XTA	I	CPU external minor cycle timing signal
10	LXMAR	I	A falling edge of LXMAR pulse from CPU will load external memory address register
11	LXMAR*	O	LXMAR generated by the IM6102
12	XTC*	O	XTC generated by the IM6102
13	XTC	I	CPU external minor cycle timing signal
14	CLOCK	I	Oscillator OUT pulses from CPU for timing the IM6102 DMA transfers.
15	$\overline{\text{SKP/INTX}}$	I	Multiplexed SKP/INT line from lower priority devices
16	DX0	I/O	Most significant bit of the 12-bit multiplexed address and data I/O bus
17	DX1	I/O	See pin 16-DX0
18	DX2	I/O	See pin 16-DX0
19	DX3	I/O	See pin 16-DX0
20	DX4	I/O	See pin 16-DX0
21	DX5	I/O	See pin 16-DX0
22	DX6	I/O	See pin 16-DX0
23	DX7	I/O	See pin 16-DX0
24	DX8	I/O	See pin 16-DX0
25	DX9	I/O	See pin 16-DX0
26	GND	I/O	Power Supply
27	DX10	I/O	See pin 16-DX0
28	DX11	I/O	See pin 16-DX0
29	OSCIN	I	Crystal input for timer oscillator
30	$\overline{\text{DEVSEL}}$	I	Device select for read or write from CPU
31	OSC OUT	O	See pin 29
32	$\overline{C_0}$	O	Control lines to CPU determining type of peripheral data transfer
33	$\overline{C_1}$	O	See pin 32-C_0
34	$\overline{C_2}$	O	See pin 32-C_0
35	$\overline{\text{SKP/INT}}$	O	Multiplexed SKP/INT input to the CPU
36	EMAO	O	Extended memory address field (most significant bit)
37	EMA1	O	Extended memory address field
38	EMA2	O	Extended memory address field
39	INTGNT	I	CPU interrupt grant
40	$\overline{\text{PROUT}}$	O	Priority out for vectored interrupt

NOTE: All DX lines are bidirectional with three-state outputs: Pins 6, 8, 11, 12, 35, 40 have active pullups; pins 32, 33, 34 have open drain outputs; pin 15 has a resistive input pullup; all inputs are protected with resistors and clamp diodes.

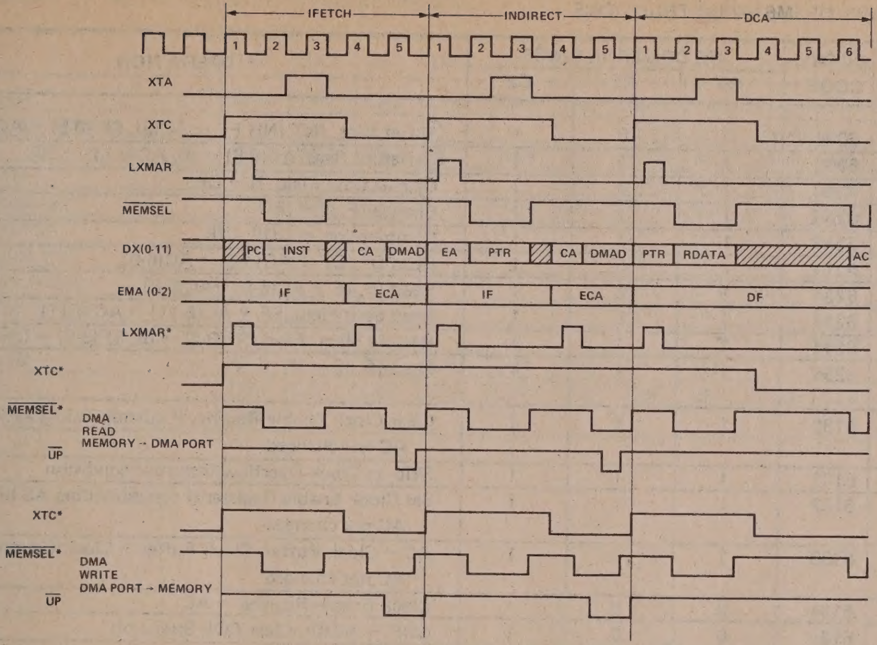

IFETCH
INDIRECT
DCA
1
2
3
4
5
1
2
3
4
5
1
2
3
4
5
6
XTA
XTC
LXMAR
MEMSEL
DX(0-11)
PC
INST
CA
DMAD
EA
PTR
CA
DMAD
PTR
RDATA
AC
EMA (0-2)
IF
ECA
IF
ECA
DF
LXMAR*
XTC*
MEMSEL*
DMA
READ
MEMORY → DMA PORT
UP
XTC*
MEMSEL*
DMA
WRITE
DMA PORT → MEMORY
UP

FIGURE 2: MEDIC TIMING FOR DCA I

DMA Status Register

This register consists of 5 control bits and 2 flag bits for the SDMA feature. For a description refer to the register bit assignments.

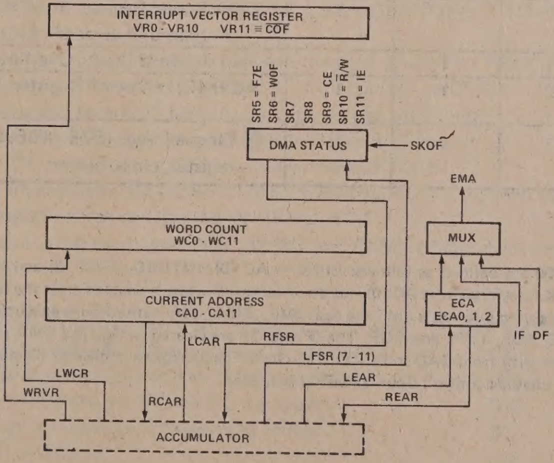

INTERRUPT VECTOR REGISTER
VR0 - VR10 VR11 ≡ COF
SR5 = F7E
SR6 = WOF
SR7
SR8
SR9 = CE
SR10 = R/W
SR11 = IE
DMA STATUS
SKOF
EMA
MUX
WORD COUNT
WC0 - WC11
CURRENT ADDRESS
CA0 - CA11
ECA
ECA0, 1, 2
IF
DF
LCAR
RFSR
LFSR (7 - 11)
LEAR
REAR
LWCR
WRVR
RCAR
ACCUMULATOR

FIGURE 3: SDMA REGISTERS

OPERATION

The IM6102 SDMA channel augments the throughput of the IM6100 during DMA operations by transferring data between memory and peripheral devices simultaneously with normal processor bus usage. In other words, no memory cycles are "stolen" from the processor; but the DMA address and data are transferred on the bus during periods that the DX bus is inactive.

TABLE 1 SUMMARY OF IM6102 INSTRUCTIONS

MNEMONIC	OCTAL CODE	I/O CONTROL LINES			OPERATION
		C0	C1	C2	
GTF	6004	0	0	1	① Get flags, INT INH FF → AC(3), SF (0-5) → AC(6-11)
RTF	6005	1	1	1	② Return flags, AC(6-8) → IB, AC(9-11) → DF
CDF	62N1	1	1	1	Change Data Field, N → DF
CIF	62N2	1	1	1	Change IF, N → IB
CDF, CIF	62N3	1	1	1	Combination of CDF, CIF
RDF	6214	1	0	1	Read DF, DF + AC(6-8) → AC(6-8)
RIF	6224	1	0	1	Read IF, IF + AC(6-8) →AC(6-8)
RIB	6234	1	0	1	Read Save Field, SF + AC(6-11) → AC(6-11)
RMF	6244	1	1	1	Restore Mem. Field, SF(0-2) → IB, SF(3-5) → DF
LIF	6254	1	1	1	Load IF, IB → IF
CLZE	6130	1	1	1	Clear Clock Enable Register if corresponding AC bit is set AC not changed
CLSK	6131	1	1	1	Skip on Clock Overflow Interrupt condition
CLOE	6132	1	1	1	Set Clock Enable Register if corresponding AC bit is set AC not changed
CLAB	6133	1	1	1	AC → Clock Buffer; Clock Buffer → Clock Counter; AC not changed
CLEN	6134	0	0	1	Clock Enable Register → AC
CLSA	6135	0	0	1	COF → AC(0), Clear COF Status bit
CLBA	6136	0	0	1	Clock Buffer → AC
CLCA	6137	0	0	1	Clock Counter → Clock Buffer; Clock Buffer → AC
LCAR	6205	0	1	1	AC → Current Address Register, 0 → AC
RCAR	6215	0	0	1	Current Address Register → AC
LWCR	6225	0	1	1	AC → Word Count Register, Start DMA, 0 → AC; clears word count overflow (WOF)
LEAR	62N6	1	1	1	N → Extended Current Address Register (ECA)
REAR	6235	1	0	1	Read ECA, ECA + AC(6-8) → AC(6-8)
LFSR	6245	0	1	1	AC(7-11) → Status Register, 0 → AC
RFSR	6255	1	0	1	DMA Status Register + AC(5-11) → AC(5-11); clears Field 7 Wraparound error (F7E)
SKOF	6265	1	1	1	Skip on Word Count Overflow
WRVR	6275	0	1	1	AC(0-10) → Vector Register, 0 → AC
CAF	6007	1	1	1	③ Clear all flags (F7E, WOF, COF) Clear clock Enable register, clock buffer

NOTES:

1. The internal flags of the IM6100 are defined as follows: LINK → AC (0), INTREQ → AC (2) and INTERRUPT ENABLE FF → AC (4).
2. When RTF is executed, the LINK is restored from AC (0) and the Interrupt System is enabled after the next sequential instruction is executed. The Interrupt Inhibit FF is set preventing interrupts until the next JMP, JMS or LIF instruction is executed.
3. A hardware RESET clears F7E, WOF, 11FF and COF. The IF and DF are cleared to 0_8. The DMA status register is cleared. (Read; refresh; disable F7E and WOF interrupts; no carry from CAO to ECA2). The clock Enable register is cleared (Disable COF interrupt; disable clock buffer to clock counter transfer on COF; disable counter). Counter/buffer is cleared.

TABLE 2 SUMMARY OF IM6102 REGISTER BIT ASSIGNMENTS

	DX0	DX1	DX2	DX3	DX4	DX5	DX6	DX7	DX8	DX9	DX10	DX11
Current Address	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
Extended Current Address							ECA0	ECA1	ECA2			
Word Count	WC0	WC1	WC2	WC3	WC4	WC5	WC6	WC7	WC8	WC9	WC10	WC11
DMA Status (1)						SR5	SR6	SR7	SR8	SR9	SR10	SR11
Interrupt Vector (2)	VR0	VR1	VR2	VR3	VR4	VR5	VR6	VR7	VR8	VR9	VR10	VR11
RIF Instruction (3)							IF0	IF1	IF2			
RTF, CIF Instruction							IB0	IB1	IB2			
GTF, RIB Instruction				IIFF(4)			SF0	SF1	SF2	SF3	SF4	SF5
CDF, RDF Instruction							DF0	DF1	DF2			
RTF Instruction										DF0	DF1	DF2
Clock Enable (5)	EN0		EN2	EN3	EN4	EN5		EN7				
Clock Buffer	CB0	CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	CB9	CB10	CB11
Clock Overflow (6)	COF											

(1) DMA STATUS

SR5 Set if Field 7 wraparound carry error — F7E; cleared by CAF, RFSR (at IOTA · $\overline{\text{XTC}}$ time), RESET
SR6 Set if DMA Word Counter Overflow WOF; cleared by CAF, LWCR, RESET
} READ ONLY BITS
SR7 Mode Bit 7 } ; Cleared by RESET (REFRESH MODE)
SR8 Mode Bit 8 } See below
SR9 Carry enable from CA0-11 to ECA2 if set — CE
SR10 DMA Write if set
SR11 Enable F7E or WOF interrupt if set — IE

(2) VR0-VR10 loaded from AC. VR11 is equivalent to $\overline{\text{COF}}$

(3) IF — Instruction Field; cleared to 0_8 by RESET AND INTGNT

(4) IIFF — Interrupt Inhibit Flip-Flop; set whenever IB ≠ IF; (CIF, CDF/CIF, RMF, RTF) cleared by RESET and IB → IF transfer

(5) EN0 — Enable Clock Overflow (COF) interrupt; cleared (interrupt disable) by RESET, CAF

EN2 — When set causes clock buffer to be transferred to clock counter on COF. Counter runs at selected rate; COF remains set until cleared with CLSA. When cleared to 0, counter runs at selected rate, overflow occurs every 2^{12} counts and COF remains set. EN2 is cleared by RESET, CAF

EN3, EN4, EN5 — Select interval between pulses. Cleared to 000 by RESET (counter disabled), CAF See below.

EN7 — Inhibits clock prescaler when set. Cleared by RESET, CAF

(6) COF — Clock Overflow status bit; cleared by CAF, RESET and CLSA; complement provides LSB of interrupt vector.

SR 7, 8	
00	Refresh mode; WC is frozen, no UP, DMAEN don't care
01	Normal mode; DMAEN(H) freezes WC, CA and no UP if WC has not overflowed; stop if WC overflows
10	Burst mode; DMAEN (H) freezes WC, CA and no UP if WC has not overflowed; reverts to refresh mode if WC overflows.
11	Stops SDMA

EN 3, 4,5	with	2 MHz clock
000		STOP
001		STOP
010		20 ms interval
011		2 ms interval
100		200 μs interval
101		20 μs interval
110		2 μs interval
111		STOP

NOTES:

1. Bits SR 7 and 8 do not change when the DMA controller stops or reverts to refresh mode as a result of WC overflow.
2. The "overflow" status is defined as set when the most significant bit of a counter makes a "1" to "0" transition.

TABLE 3 SDMA INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
LCAR	6205_8	LOAD CURRENT ADDRESS REGISTER (CA) The contents of the AC replace the contents of the CA and the AC is cleared. DMA sequencing is stopped.
RCAR	6215_8	READ CURRENT ADDRESS REGISTER Description: Contents of CA transferred to AC.
LWCR	6225_8	LOAD WORD COUNT REGISTER (WC) Description: Contents of AC are transferred to the WORD COUNT REGISTER, the AC is cleared WORD COUNT OVERFLOW (WOF) is cleared and DMA operation started.
LEAR	$62N6_8$	LOAD IMMEDIATE TO EXTENDED CURRENT ADDRESS REGISTER (ECA) Description: Field N of the IOT instruction is transferred to the Extended current address register.
REAR	6235_8	READ EXTENDED CA Description: Extended current address register contents OR'd into bits 6, 7, 8, of AC.
LFSR	6245_8	LOAD DMA FLAGS and STATUS REGISTER Description: AC bits 7-11 are transferred to the DMA STATUS REGISTER and the AC is cleared.
RFSR	6255_8	READ DMA FLAGS and STATUS REGISTER Description: DMA Flags and Status Register bits are OR transferred into AC bits 5-11 and Field 7 wraparound error (F7E) is cleared.
SKOF	6265_8	SKIP ON OVERFLOW INTERRUPT Description: The PC is incremented by 1 if a word count register overflow interrupt condition is present causing next instruction to be skipped.
WRVR	6275_8	WRITE VECTOR REGISTER Description: AC bits 0-10 are transferred to the Vector Register and the AC is cleared.
CAF	6007_8	CLEAR ALL FLAGS—clears F7E and WOF (and also COF), Clock enable and clock buffer. The DMA process is initiated if the status register is not set to the "stop" mode.

TABLE 4 DMA FLAGS AND STATUS REGISTER BIT ASSIGNMENTS

0	1	2	3	4	5	6	7	8	9	10	11
•	•	•	•	•	F7E	WOF	SR7	SR8	CE	R̄/W	IE

where* — don't care for write and zero for read.

F7E	Field 7 wrap around carry error; cleared by CAF, RFSR and RESET.	
WOF	Logic one indicates word counter overflow; clear by CAF, LWCR and RESET	
CE	Carry enable from CA(0-11) to ECA; cleared by RESET	
$\bar{R}/W$	Logic one indicates DMA write (Port to Memory transfer). Cleared (DMA Read) by RESET	
IE	Enable interrupt when WC overflows or Field 7 error occurs; cleared by RESET	
SR7, 8	00	Refresh mode; WC is frozen, no UP, DMAEN is don't care
	01	Normal mode; DMAEN(H) freezes WC CA and no UP if WC has not overflowed; stop if WC overflows
	10	Burst mode; DMAEN(H) freezes WC, CA and no UP if WC has not overflowed; refresh condition if WC overflows
	11	Stops DMA

DMA MODES

$SR_7 = SR_8 = 0$ REFRESH MODE

This is the mode to which the 6102 reverts on RESET. The word count register clock input is disabled, the user pulse (DMA data strobe) is suppressed and the DMAEN input is ignored. However, provided valid DMA transfer conditions are met in a particular memory cycle, the DMA sequencer will be started, appropriate timing signals will be generated and the current address register will be clocked. Thus DMA read accesses will be performed continually with an essentially free-running current address register. Read accesses will refresh dynamic memory. No WOF is possible but an F7E is possible if bit SR9 is set, enabling a carry from the current address register to the extended current address register.

$SR_7 = 0$; $SR_8 = 1$ NORMAL MODE

This mode is used for normal SDMA operations with static memory. The following instruction sequence can be used:

```
CLA       /Clear AC
TAD CA    /Get starting address
LCAR      /Load into current address register and
          clear AC
```

```
TAD SR   /Get DMA status Register Constant
LFSR     /Change status (from refresh to normal
          for example)
TAD WC   /Get two's complement of block length
LWCR     /Load word count register and start
          DMA TRANSFERS
```

Note that LWCR will start the sequencer so it should be the last instruction in the initialization sequence. The ECA register and vector register could also have been initialized in this sequence.

The SDMA sequencer samples DMAEN on the rising edge of every XTA and latches the condition of the enable line. If DMAEN is low, the sequencer is enabled, external timing signals XTC*, MSEL*, UP, LXMAR* are generated, the WC and CA registers are clocked. If DMAEN is high, at XTA (↑) time, the signal is sampled and latched and if the WC has not overflowed, the WC and CA registers are frozen, UP is suppressed. If the WOF condition comes up, the SDMA operation stops, regardless of DMAEN level.

The DMAEN and UP signals provide a simple interlocked handshaking method for transferring data one or more characters at a time (entire blocks) concurrently with processor operations on the bus. Of course, at all times, independent of DMAEN, the SDMA sequencer can proceed only if other bus usage conditions for DMA operations are met (not IOTA, IAUTOI, DCA, JMS, IJMS, ISZ, DMAGNT, or access of location $X0000_8$),

NOTE: IAUTOI is an indirect cycle of any autoindexed instruction; IJMS is indirect cycle of JMS. An autoindexed JMP instruction may not be executed when the DMA mode is active.

$SR_7 = 1; SR_8 = 0$ BURST MODE

This mode is the same as the normal mode except when the word count register overflows. When this happens, the SDMA sequencer will set the WOF flag and revert to the refresh mode (ignoring DMAEN, freezing WC and suppressing UP). This mode is used when SDMA operations and dynamic memory refresh must be concurrently performed. The system designer must control the block lengths to be transferred, the refresh interval, and memory system design according to the application and performance desired.

$SR_7 = 1; SR_8 = 1$ STOP MODE

In this mode, no SDMA operations will take place. Naturally, cycle stealing DMA is still possible, and indeed may be used in any of the modes but the designer must be aware that cycle stealing may adversely affect dynamic memory refresh intervals. LWCR and LFSR may be executed in either order to change mode and start DMA.

B. Extended Memory Address Control

Figure 4 shows the EMA registers in more detail along with the register transfers caused by various instructions. The EMA function of the IM6102 is program compatible with the DEC PDP-8/E KM8-E Memory Extension option. The purpose of the EMA function is to extend the effective addressing space of the system from 4K to 32K words. To perform this function, the EXTENDED MEMORY CONTROLLER maintains a 3-bit extended address which is decoded by the memory modules to select 1 of 8 memory fields each containing 4096 words of storage. These 4K fields start with FIELD 0 and progress to FIELD 7 when 32K of memory is used. All software communication with the controller is via programmed IOT instructions for which a summary is included in Table 1.

Figure 4 shows two 3-bit field registers: the Instruction Field, which acts as an extension to the Instruction and directly obtained operand addresses and the Data Field, which augments indirectly obtained operand addresses. The program can, therefore, use one field for instructions and address pointers and another field for data. The selection between Instruction and Data Fields is signalled by the DATAF signal generated by the IM6100. A discussion of the various registers follows.

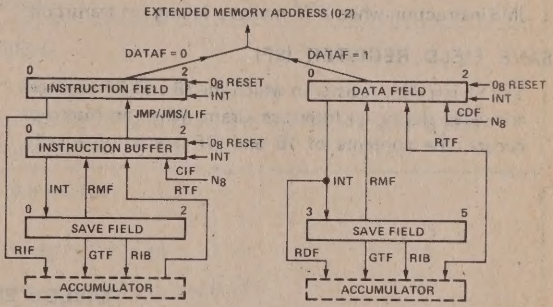


FIGURE 4: EMA REGISTERS

INSTRUCTION FIELD REGISTER (IF)

The IF is a 3-bit register that serves as an extension of the Program Counter (PC). The IF, however, is not incremented when the PC goes from 7777_8 to 0000_8. The contents of the IF determine the field from which all instructions are taken. Operands for all directly addressed memory reference instructions also come from the Instruction Field. The indirect pointer for all indirectly addressed memory reference instructions reside in the Instruction Field. The IF is cleared to 0_8 and the IM6100 Program Counter is set to 7777_8 by RESET.

DATA FIELD REGISTER (DF)

The DF is a 3-bit register which determines the memory field from which operands are fetched in indirectly addressed AND, TAD, ISZ or DCA instructions. However, the branch address for indirectly addressed JMS or JMP instructions is obtained from the Instruction Field. The Data Field register may be modified under program control. The DF is set to 0_8, on reset.

INSTRUCTION BUFFER REGISTER (IB)

The IB is a 3-bit register which serves as an input buffer for the Instruction Field (IF) register. All programmed modifications of the IF register are made through the IB register. The transfer from IB to IF takes place at the beginning of the execute phase of the "next" JMP or JMS instruction or immediately upon execution of an LIF instruction. Using this feature, a program segment can execute an instruction to modify the IF and then "exit" the program segment before the actual modification of the IF takes place. If instructions could change the IF directly, it would be impossible to execute the "next" sequential instruction, followed by a Change IF instruction. The IB to IF transfer is inhibited if the JMP/JMS instruction is fetched from control panel memory, which is restricted to 4K, but the LIF instruction is used here to provide the ability to load the IF register from the IB register. This allows the control panel routines to be executed transparently while the IB and IF differ and also yields a method for the panel to extract or alter the status of the primary EMA registers. The IB is set to 0_8, on reset. The IB to IF transfer takes place during the second cycle of a JMP/JMS instruction when XTC makes a falling (↓) transition.

SAVE FIELD REGISTER (SF)

The SF is a 6-bit register in which the IB and DF registers are saved during an Interrupt Grant. When an Interrupt occurs, the contents of IB and DF are automatically stored in SF (0-2) and SF (3-5), respectively, and the IF, IB and DF registers are cleared. The INTGNT (Interrupt Grant) cycle stores the "current" Program Counter (PC) in location 0000_8 of Memory Field 0_8 and the CPU resumes operation in location 0001_8 of Memory Field 0_8. The Instruction Field and Data Field of the program segment being executed by the CPU before the interrupt was acknowledged are available in the SF register.

INTERRUPT INHIBIT FLIP-FLOP

The INTREQ (Interrupt Request) line to the IM6100 must be "gated" by the Interrupt Inhibit Flip-Flop so that, when the Instruction Field is changed under program control, all interrupts are disabled until a JMP or JMS instruction is executed. Since the actual modification of the Instruction Field takes place only after the "next" JMP/JMS, this inhibition of the INTREQ's ensures that the program sequence resumes operation in the "new" memory field before an Interrupt Request is granted.

Since Interrupt Requests are asynchronous in nature, a situation may arise in which an INTREQ is generated when the IF and IB bits are different. The Interrupt Inhibit FF guarantees the structural integrity of the program segment. The IIF is cleared on reset.

TABLE 5 EMA INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
GTF	6004_8	GET FLAGS Operation: AC (0) ← LINK AC (2) ← INTREQ Line AC (3) ← INT INHIBIT FF AC (4) ← INT ENABLE FF AC (6-11) ← SF (0-5) Description: LINK, INTREQ and INT ENABLE FF are internal to the CPU. The INT INHIBIT FF and SF are in the MEDIC.
RTF	6005_8	RETURN FLAGS Operation: LINK ← AC (0) IB ← AC (6-8) DF ← AC (9-11) Description: LINK is restored. All AC bits are available externally during IOTA T6 to restore other flag bits. The internal Interrupt System is enabled. However, the Interrupt Inhibit FF is made active until the "next" JMS/JMP/LIF. The IB is transferred to IF after the "next" JMS/JMP/LIF.
CDF	$62N1_8$	CHANGE DATA FIELD Operation: DF ← N_8 Description: Change DF register to N (0_8-7_8).

TABLE 5, Continued

MNEMONIC	OCTAL CODE	OPERATION
CIF	$62N2_8$	CHANGE INSTRUCTION FIELD Operation: IB ← N_8 Description: Change IB to N (0_8-7_8). Transfer IB to IF after the "next" JMP/JMS/LIF. The Interrupt Inhibit FF is active until the "next" JMP/JMS/LIF.
CDF, CIF	$62N3_8$	CHANGE DF, IF Operation: DF ← N_8 IB ← N_8 Description: Combination of CDF and CIF.
RDF	6214_8	READ DATA FIELD Operation: AC (6-8) ← AC (6-8) + DF Description: OR's the contents of DF into bits 6-8 of the AC. All other bits are unaffected.
RIF	6224_8	READ INSTRUCTION FIELD Operation: AC (6-8) ← AC (6-8) + IF Description: OR's the contents of IF into bits 6-8 of the AC. All other bits of the AC are unaffected.
RIB	6234_8	READ INSTRUCTION BUFFER READ SAVE FIELD Operation: AC (6-11) ← AC (6-11) + SF Description: OR's the contents of SF into bits 6-11 of the AC. All other bits are unaffected.
RMF	6244_8	RESTORE MEMORY FIELD Operation: IB ← SF (0-2) DF ← SF (3-5) Description: The SF register saves the contents of the IB and DF when an interrupt occurs. This command is used to restore IB and DF when "exiting" from the interrupt service routine in another field. Transfer IB to IF after the next JMP/JMS/LIF. The Interrupt Inhibit Flip-Flop is active until the next JMP/JMS/LIF.
LIF	6254_8	LOAD INSTRUCTION FIELD Operation: IF ← IB Description: Transfer IB to IF and clear the Interrupt Inhibit FF.

+: "OR"

●: "AND"

←: "IS REPLACED BY"

OPERAND FETCHING

Instructions are accessed from the currently assigned Instruction Field. For indirect AND, TAD, ISZ or DCA instructions, the operand address refers first to the Instruction Field to obtain an Effective Address which in turn refers to a location in the currently addressed Data Field. All instructions and operands are obtained from the field designated by the IF, except for indirectly addressed operands, which are specified by the DF.

Thus, DF is active only in the Execute phase of an AND, TAD, ISZ or DCA when it is directly preceded by an Indirect phase.

ADDRESS MODE	IF	DF	AND, TAD, ISZ or DCA
Direct	m	n	Operand in field m
Indirect	m	n	Absolute address of operand in field m; operand in field n

Each field of extended memory contains eight auto-index registers in addresses 10 through 17. For example, assume that a program in field 2 is running (IF = 2) and using operands in field 1 (DF = 1) when the instruction TAD I 10 is fetched. The indirect autoindex cycle is entered, and the contents of location 10 in field 2 are read, incremented, and rewritten. If address 10 in field 2 originally contained 0546, it now contains 0547. In the execute cycle, the operand is fetched from location 0547 of field 1.

Program control is transferred between memory fields by the CIF instruction. The instruction does not change the instruction field directly, as this would make it impossible to execute the next sequential instruction; instead, it loads the new instruction field in the IB for automatic transfer into the IF when either a JMP or JMS instruction is executed. The DF is unaffected by the JMP and JMS instructions.

The 12-bit program counter is set in the normal manner and, because the IF is an extension on the most significant end of the PC, the program sequence resumes in the new memory field following a JMP or JMS. Entry into a program interrupt is inhibited after the CIF instruction until a JMP or JMS is executed.

NOTE: The IF is not incremented if the PC goes from 7777_8 to 0000_8. This feature protects the user from accidentally entering a nonexistent field.

To call a subroutine that is out of the current field, the data field register is set to indicate the field of the calling JMS, which establishes the location of the operands as well as the identity of the return field. The instruction field is set to the field of the starting address of the subroutine. The following sequence returns program control to the main program from a subroutine that is out of the current field.

```
/PROGRAM OPERATIONS IN MEMORY FIELD 2
/INSTRUCTION FIELD = 2; DATA FIELD = 2
/CALL A SUBROUTINE IN MEMORY FIELD 1
/INDICATE CALLING FIELD LOCATION BY THE
/CONTENTS OF THE DATA FIELD
          CIF  10        /CHANGE TO INSTRUCTION
                         /FIELD 1 = 6212
          JMS I SUBRP    /SUBRP = ENTRY ADDRESS
          CDF  20        /RESTORE DATA FIELD
             .
             .
             .
SUBRP,    SUBR           /POINTER
                                          FIELD 2
--------------------------------------------------
                                          FIELD 1

                         /CALLED SUBROUTINE,
                         /LOCATION IN FIELD 1
SUBR,     0              /RETURN ADDRESS
                         /STORED HERE
          CLA
          RDF            /READ DATA FIELD INTO AC
          TAD RETURN     /CONTENTS OF THE AC =
                         /6202 + DATA FIELD BITS
          DCA EXIT       /STORE CIF N INSTRUCTION
             .           /NOW CHANGE DATA FIELD
             .           /IF DESIRED
             .
EXIT,     0              /A CIF INSTRUCTION
          JMP I SUBR     /RETURN TO CALLING
                         /PROGRAM
RETURN,   CIF            /USED TO FORM CIF N
                         /INSTRUCTION
```

When a program interrupt occurs, the current instruction and data field numbers are automatically stored in the 6-bit save field register; then the IF and DF are cleared. The 12-bit program counter is stored in location 0000_8 of field 0_8 and program control advances to location 0001_8 of field 0_8. At the end of the program interrupt subroutine, the RMF instruction restores the IF and DF from the contents of the SF. Alternatively, the GTF and RTF instructions may be used to handle the Save Field and Link information. The following instruction sequence at the end of the program interrupt subroutine continues the interrupted program after the interrupt has been processed:

```
             .
             .
             .
             .
          CLA
          TAD AC         /RESTORE AC
          RMF            /LOAD IB AND DF FROM SF
          ION            /TURN ON INTERRUPT
                         /SYSTEM
          JMP I 0        /RESTORE PC WITH
                         /CONTENTS OF LOCATION
                         /0000₈ AND LOAD
                         /IF FROM IB
```

IM6100 control panel memory programs, if used must be careful in the manner that EMA register data is manipulated. Control panel interrupt requests bypass the device interrupt enable flip flop, and indeed, are granted even by a halted CPU. The interrupts from a control panel may occur at any time, and in particular when the IB and IF registers do not contain the same data. The EMA logic inhibits IB to IF transfers in control panel memory so that panel routines may execute transparently (in particular, JMP/JMS instructions). The panel routines may alter the IF by executing the LIF instruction.

Users should also note that the GTF and RIB instructions read the SF register, and only the RIF instruction reads the IF register. Note also that the SF saves the IB register rather than the IF during an interrupt. However, interrupts are inhibited until the IF and IB registers are the same.

The memory extension controller that we have discussed in this section shows three important design considerations involved in extending memory addressing space. The first is the concept of having separate instruction and data fields for program flexibility. The second is the importance of double buffering the instruction field register to maintain structural integrity of programs and the third is the provision for saving the current field status upon interrupts and disabling interrupts until a change of instruction field has been completely executed.

C. Programmable Real Time Clock

The programmable real time clock offers the 6100 user a number of ways to accurately measure and count intervals in order to implement real time data acquisition and data processing systems.

The crystal used should have the following characteristics:

$R_S \leqslant 150$ ohms

$C_M = 3\text{-}30$ mpF (10^{-15}F)

$C_O = 10\text{-}50$ pF

Static capacitance should be around 5pF; for the greatest stability, C_O should be around 12pF and the oscillator is parallel resonant.

TABLE 6 CLOCK ENABLE REGISTER BIT ASSIGNMENTS

0	1	2	3	4	5	6	7	8	9	10	11
EN0	*	EN2	EN3	EN4	EN5	*	EN7	*	*	*	*

* Don't care for write and zero for read.

Where EN0 — When set to 1, enables clock overflow (COF flag) to cause an interrupt. Cleared by RESET, CAF.

EN2 — When reset to a 0-counter runs at selected rate. Overflow occurs every 4096 (2^{12}) counts.COF flag remains set until cleared by IOT 6135 (CLSA), CAF, RESET. When set to a 1-counter runs at selected rate. If the COF flag is cleared, overflow causes clock buffer to be transferred to the clock counter which continues to run. COF flag remains set until cleared with IOT 6135 (CLSA). Also cleared by RESET, CAF.

EN3, 4, 5 — Assuming 2 MHz crystal oscillator cleared by RESET, CAF.

Bits 3,4,5	Octal	Interval Between Pulses	Frequency
000	0	Stop	0
001	1	Stop	0
010	2	20 msec	50 Hz
011	3	2 msec	500 Hz
100	4	200 μsec	5 KHz
101	5	20 μsec	50 KHz
110	6	2 μsec	500 KHz
111	7	Stop	0

EN7 — Inhibits clock prescaler when set to 1 cleared by RESET, CAF. EN3-5 and EN7 should not be changed simultaneously.

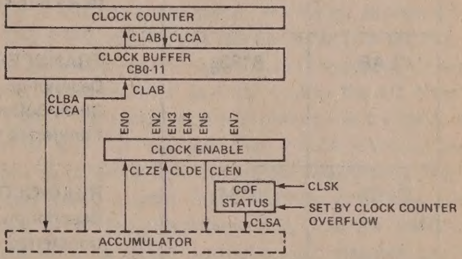


FIGURE 5 RTC REGISTERS

A discussion of the Real Time Clock registers as shown in Fig. 5 follows:

CLOCK ENABLE REGISTER

This register controls the mode of counting, whether clock interrupts are allowed, and the rate of the time base of the clock. For a description refer to the register bit assignments.

CLOCK BUFFER REGISTER (CB)

This 12-bit register stores data being transferred from the AC to the clock counter, or from the clock counter to the AC. It also permits presetting of the clock counter.

CLOCK COUNTER REGISTER (CC)

This register is a 12-bit binary counter that may load the clock buffer or be loaded from it. It is driven by a 2 MHz crystal oscillator with the proper predivision set by the time base selection. When an overflow occurs and if bit 0 of the clock enable register is a logic one, an interrupt is requested. If bit 2 is also 1, overflow causes the clock buffer to be transferred automatically into the clock counter.

TIME BASE MULTIPLEXER

The multiplexer provides count pulses to the clock counter according to the rate set by the clock enable register. Use of other than a 2 MHz crystal for the clock will result in proportionately different time bases.

CLOCK OVERFLOW FLAG

This flag is set by a clock counter overflow. It is cleared by CAF, CLSA and RESET. Its complement provides LSB (VR11) of interrupt vector. If ENO of clock enable counter is set, COF can cause an interrupt request. The COF is set when the MSB of the counter makes a "1" to "0" transition.

TABLE 7 RTC INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
CLZE	6130_8	CLEAR ENABLE REGISTER PER AC Description: Clears the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed.
CLSK	6131_8	SKIP ON CLOCK INTERRUPT Description: Causes the program counter to be incremented by one if clock interrupt conditions exists, so that the next sequential instruction is skipped. EN0 must be 1.
CLOE	6132_8	SET ENABLE REGISTER PER AC Description: Sets the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed.
CLAB	6133_8	TRANSFER AC TO CLOCK BUFFER Description: Causes the contents of the AC to be transferred to the Clock Buffer, then causes the contents of the Clock Buffer to be transferred to the Clock Counter. The AC is not changed.
CLEN	6134_8	READ CLOCK ENABLE REGISTER Description: Causes the contents of the clock enable register to be transferred into the AC.
CLSA	6135_8	READ CLOCK STATUS Description: Interrogates the clock overflow status flip flop by clearing AC, then transferring clock status into AC bit 0. COF is cleared.
CLBA	6136_8	READ CLOCK BUFFER Description: Clears the AC, then transfers the contents of the Clock Buffer into the AC.
CLCA	6137_8	READ CLOCK COUNTER Description: Clears the AC, transfers the contents of the Clock Counter to the Clock Buffer, then transfers the contents of the Clock Buffer into the AC. If EN7 is set to 1 (click prescaler is inhibited), the CLCA instruction increments the prescaler input by one. If the clock is in the "stop" mode but EN7 is not inhibited, the prescaler will not be clocked by the CLCA instruction.
CAF	6007_8	CLEAR ALL FLAGS Description: Clears COF flag (and also F7E, WOF flags), clock enable and clock buffer registers.

SYSTEM CONSIDERATIONS

The IM6102 is the highest priority device in a priority interrupt scheme. It provides an active low signal on pin 40, POUT, to signal the next lower priority device in the chain (thus, a high level on POUT indicates that the 6102 is not requesting an interrupt) via its "priority-in", PRIN, input.

The IM6102 when requesting an interrupt activates the SKP/INT line low on pin 35 and the POUT line low on pin 40 if its interrupt inhibit flip-flop is not set.

The IOT instructions used by the IM6102 preclude the use of certain device addresses when the system uses IM6101 PIEs. The addresses that may not be used are those given by bits 3 through 7 of the IOT instructions that are used with the IM6102. These addresses are 00101, 01000, 01001, 01010, 01011 corresponding to IOT instructions 612X, 613X, 620X, 621X, 622X, 623X, 624X, 625X, 626X and 627X.

The IM6102 does not generate DMAREQ signals to the 6100 because of its simultaneous use of the DX bus. It monitors the DMAGNT signal in order to place the EMA 0, 1, 2 lines on pins 36, 37, 38 in a high impedance state while DMAGNT is high.

If the application requires other peripherals requiring direct memory access on a cycle stealing basis, for example, bus contention problems will be resolved by the IM6102 as it monitors the DMAGNT line and gets off the bus (by placing all lines in the high impedance state) when DMAGNT is active.

If interrupts are enabled and a request is pending, during the first INTGNT cycle, the IM6102 will detect the referencing of location 0000_8 by the IM6100 in order to save the PC and will suspend simultaneous DMA during that cycle. The logic will in fact suspend simultaneous DMA in any cycle that location 0000_8 is referenced, either in main memory or control panel memory.

This makes it possible to disable automatic interrupt vectoring by grounding the INTGNT line to the IM6102. This will not affect the generation of INTREQ so the IM6100 will have to poll peripheral devices (skip on flag instructions) to determine the interrupting source.

Grounding INTGNT is not possible in extended memory applications since the INTGNT signal is used to save the Instruction Buffer and Data Field Register and clear the IF, IB and DF registers. (All peripheral device interrupt service routines have their entry point at location 0001_8 of Memory Field 0_8).

If no interrupt requests are pending in the 6102 (COF, F7E or WOF) from the DMA or RTC functions, the IM6102 interrupt request flip-flop is clear and POUT, the priority out signal, is high, enabling interrupt requests downstream in the priority chain. In the event that interrupts are enabled (DMA status bit SR11 is set and/or clock enable bit ENO is set) and an interrupting condition occurs (F7E, WOF, COF), the POUT signal goes low asynchronously disabling interrupt vectors downstream.

If the Interrupt Inhibit Flip-Flop is not set, the SKP/INT line is driven low by the interrupt request. If the IIFF is set, the SKP/INT line stays high until the IIFF is cleared (by RESET or an IB to IF transfer) at which time SKP/INT may be driven low. Skip requests will always propagate independently of IIFF during IOTA $\bullet\overline{\text{DEVSEL}}\bullet$ XTC.

Interrupt requests from devices downstream of the IM6102 must also be channeled via the IM6102 in order that the IIFF may condition the request timing. The IM6102 provides a built in pull-up on the SKP/INTX line coming in from devices downstream in the priority chain. At 5v, the pull-up looks like a 10K resistor; at 10V, it looks like 5K.

The execution of any IOT instruction will reset INTGNT to a low level at the end of IOTA time. This IOT instruction will be the first instruction in the interrupt service routine after saving status. If hardware vectoring is being used, any IOT instruction when INTGNT is high will cause the IM6102 to place a vector address on the bus if it requested an interrupt and pull the C1 and C2 lines low, thus placing the vector in PC and forcing a branch to the service routine. If the C2 line is left unconnected, the vector address will not be forced into the PC, but will be OR'ed into the AC. The interrupt service routine would have to execute a CLA after its first IOT instruction in order to clear the AC. Note that the LSB of the vector address is determined by the complement of the COF flag and that a DMA interrupt service routine must distinguish between the two possible interrupting conditions, a word count overflow or a field 7 wraparound error. The programmer may read the DMA status register with an RFSR instruction and also test the WOF flag with a skip instruction, SKOF. The COF flag may also be tested with the CLSK skip instruction. The flag may be read (and cleared) with the CLSA instruction. The skip instructions cause the SKP/INT line to go low during IOTA • XTC time if the flag being tested is set. At all other times, the SKP/INT line carries interrupt requests as modified by the IM6102 interrupt inhibit logic. The flags must always be explicitly cleared by the interrupt service routine.

The DMA transfer rate depends on the program. The minimum rate would be obtained if the processor was executing an autoindexed DCA or an indirect JMS (even if non-autoindexed, DMA is suppressed during indirect phase of JMS). Continuously executing these instructions would cause DMA transfers to occur only every third memory cycle (IFETCH). The maximum rate could be obtained by executing a JMP• loop (JMP to itself); data would be transferred on every cycle and the interrupt routine entered when word count overflows could bump the return address out of the loop.

In dynamic memory systems it should be noted that the MEMSEL* signal narrows when the mode changes from write to refresh (burst mode). RESET signals may need to be limited in duration to prevent loss of memory data in dynamic memory systems.

The accuracy of the clock counter in the programmable real time clock section of the IM6102 is as follows:

CASE 1: Counter running; CC loaded from AC via CB using instruction CLAB (IOT 6133) accuracy is 0 to +1 count.

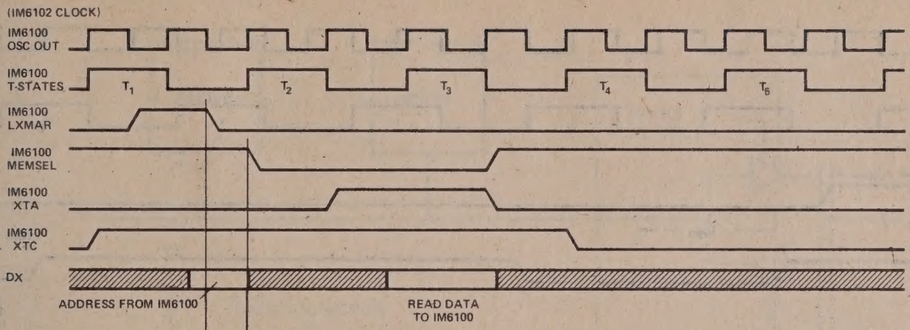
CASE 2: CC loaded from CB automatically on overflow; the accuracy of counting is then only dependent on accuracy of oscillator.

IM6102 users who do not need all the capabilities of the device may improve systems performance by not using some of the features. To do this properly, certain pins on the device will become unused. The following table summarizes what may be done with certain pins when using only part of the IM6102 functions. All unlisted pins must be used when implementing any of the three basic features.

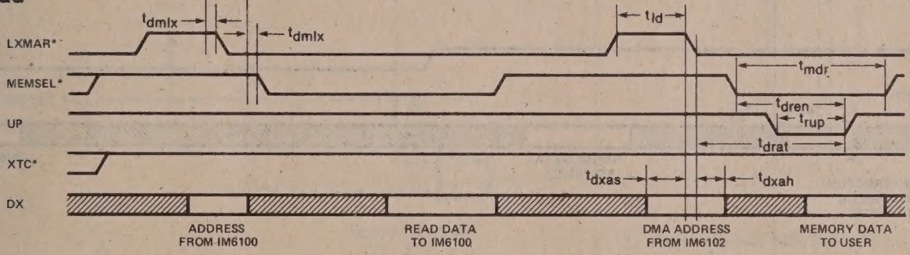
PIN NUMBER	PIN NAME	RTC ONLY	SDMA ONLY	EMC ONLY	EMC & DYNAMIC REFRESH
2	DMAEN	VCC	USED	VCC	VCC
3	DMAGNT	USED	USED	USED	USED
6	MEMSEL*	N/C	USED	N/C	USED
8	UP	N/C	USED	N/C	N/C
11	LXMAR*	N/C	USED	N/C	USED
12	XTC*	N/C	USED	N/C	USED
15	SKP/INTX	VCC	VCC	USED	USED
29	OSCIN	USED	GND	GND	GND
31	OSC OUT	USED	N/C	N/C	N/C
34	C2	USED	USED	N/C	N/C
36	EMAO	N/C	N/C	USED	USED
37	EMA 1	N/C	N/C	USED	USED
38	EMA 2	N/C	N/C	USED	USED
40	PROUT	USED	USED	N/C	N/C

SDMA OPERATIONS TIMING

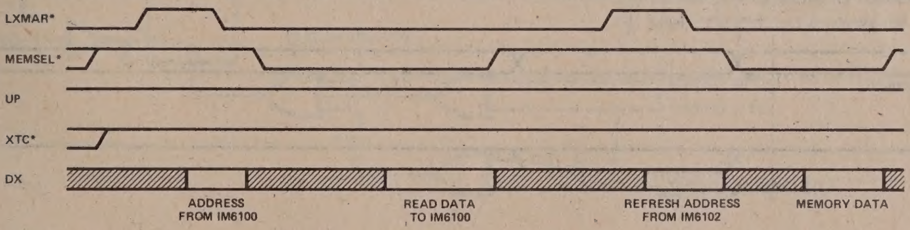
A. IM6100 Signals


(IM6102 CLOCK)
IM6100 OSC OUT
IM6100 T-STATES
T1
T2
T3
T4
T5
IM6100 LXMAR
IM6100 MEMSEL
IM6100 XTA
IM6100 XTC
DX
ADDRESS FROM IM6100
READ DATA TO IM6100

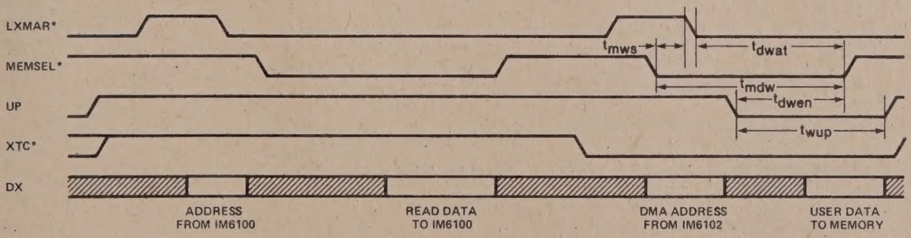
B. DMA Read


tdmlx
tdmlx
tld
LXMAR*
MEMSEL*
UP
XTC*
DX
tmdr
tdren
trup
tdrat
tdxas
tdxah
ADDRESS FROM IM6100
READ DATA TO IM6100
DMA ADDRESS FROM IM6102
MEMORY DATA TO USER

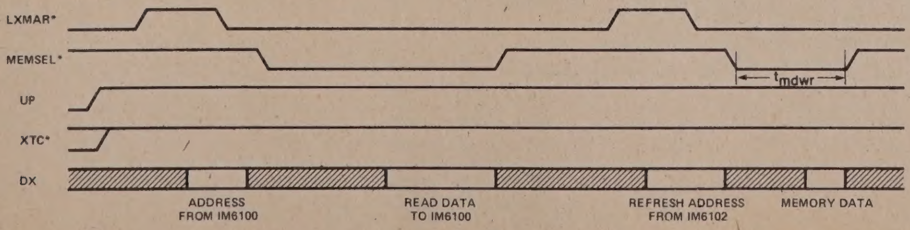
C. DMA Read/Refresh


LXMAR*
MEMSEL*
UP
XTC*
DX
ADDRESS FROM IM6100
READ DATA TO IM6100
REFRESH ADDRESS FROM IM6102
MEMORY DATA

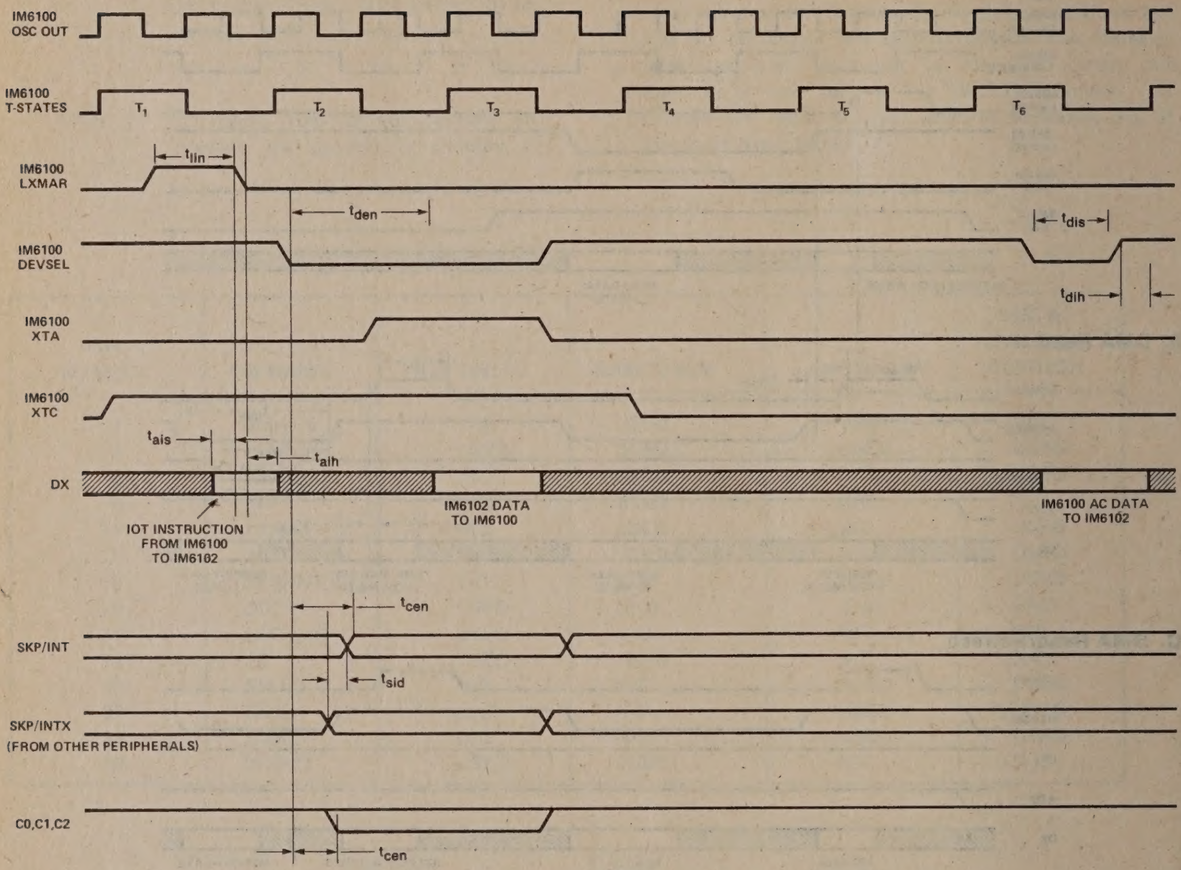
D. DMA Write


LXMAR*
MEMSEL*
UP
XTC*
DX
tmws
tdwat
tmdw
tdwen
twup
ADDRESS FROM IM6100
READ DATA TO IM6100
DMA ADDRESS FROM IM6102
USER DATA TO MEMORY

E. DMA Write/Refresh

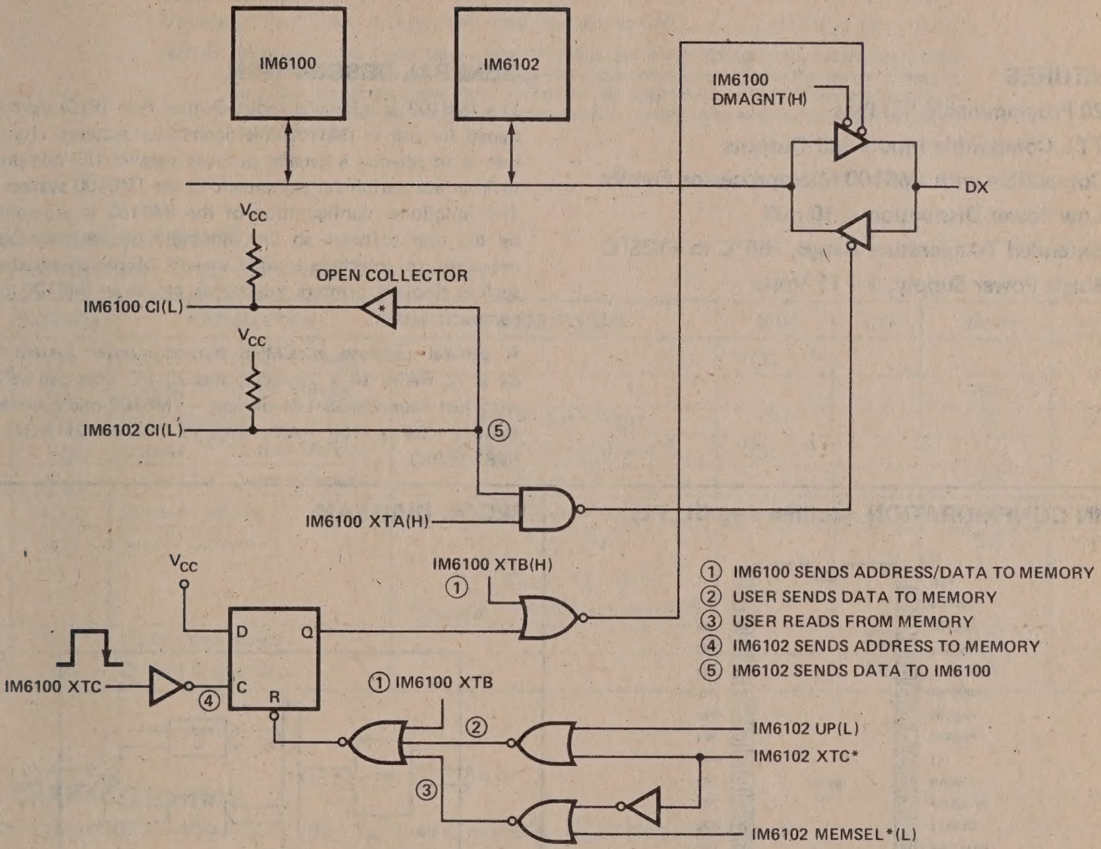

LXMAR*
MEMSEL*
UP
XTC*
DX
tmdwr
ADDRESS FROM IM6100
READ DATA TO IM6100
REFRESH ADDRESS FROM IM6102
MEMORY DATA

TIMING DIAGRAM


IM6100 OSC OUT
IM6100 T-STATES
T1
T2
T3
T4
T5
T6
IM6100 LXMAR
tlin
tden
IM6100 DEVSEL
tdis
tdih
IM6100 XTA
IM6100 XTC
tais
taih
DX
IOT INSTRUCTION FROM IM6100 TO IM6102
IM6102 DATA TO IM6100
IM6100 AC DATA TO IM6102
tcen
SKP/INT
tsid
SKP/INTX (FROM OTHER PERIPHERALS)
C0,C1,C2
tcen

APPLICATION

IM6100-IM6102 Interface in a Buffered System.


IM6100
IM6102
IM6100
DMAGNT(H)
DX
V_{CC}
OPEN COLLECTOR
IM6100 CI(L)
V_{CC}
IM6102 CI(L)
⑤
IM6100 XTA(H)
V_{CC}
IM6100 XTB(H)
①
D
Q
IM6100 XTC
C
R
④
① IM6100 XTB
②
IM6102 UP(L)
IM6102 XTC*
③
IM6102 MEMSEL*(L)

① IM6100 SENDS ADDRESS/DATA TO MEMORY
② USER SENDS DATA TO MEMORY
③ USER READS FROM MEMORY
④ IM6102 SENDS ADDRESS TO MEMORY
⑤ IM6102 SENDS DATA TO IM6100

INTERSIL

IM6103 CMOS Parallel Input-Output Port (PIO)

FEATURES

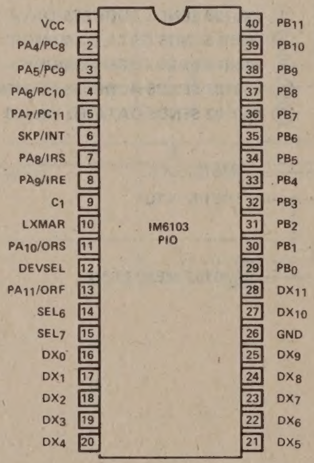
- 20 Programmable I/O Pins
- TTL Compatible Inputs and Outputs
- Compatible with IM6100 Microprocessor Family
- Low Power Dissipation < 10 mW
- Extended Temperature Range, -55°C to +125°C
- Single Power Supply, 4 - 11 Volts

GENERAL DESCRIPTION

The IM6103 is a Parallel Input-Output Port (PIO) device designed for use in IM6100 microcomputer systems. Its function is to provide a general purpose parallel I/O component to interface peripheral equipment to the IM6100 system bus. The functional configuration of the IM6103 is programmed by the user software so that normally no external logic is necessary to interface a wide variety of peripheral devices such as displays, printers, keyboards, etc. to an IM6100 microcomputer system.

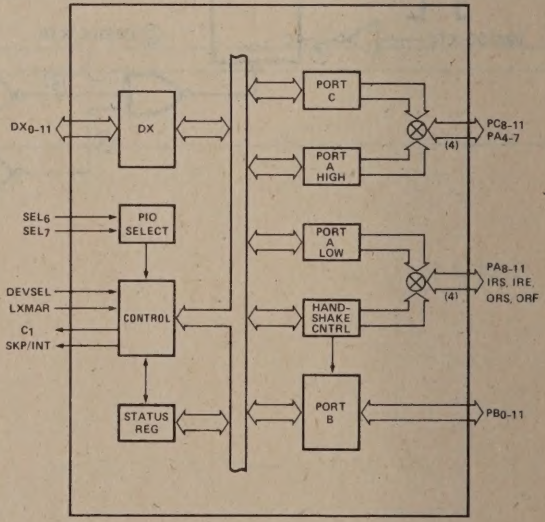
A general purpose all-CMOS microcomputer system with 64 x 12 RAM, 1k x 12 ROM and 20 I/O lines can be built with just four CMOS LSI devices — IM6100 microprocessor, IM6512 (64 x 12) RAM, IM6312 (1k x 12) ROM and IM6103 PIO.

PIN CONFIGURATION (outline dwg DL, PL)



VCC 1
PA4/PC8 2
PA5/PC9 3
PA6/PC10 4
PA7/PC11 5
SKP/INT 6
PA8/IRS 7
PA9/IRE 8
C1 9
LXMAR 10
PA10/ORS 11
DEVSEL 12
PA11/ORF 13
SEL6 14
SEL7 15
DX0 16
DX1 17
DX2 18
DX3 19
DX4 20
IM6103
PIO
40 PB11
39 PB10
38 PB9
37 PB8
36 PB7
35 PB6
34 PB5
33 PB4
32 PB3
31 PB2
30 PB1
29 PB0
28 DX11
27 DX10
26 GND
25 DX9
24 DX8
23 DX7
22 DX6
21 DX5

BLOCK DIAGRAM



DX0-11
DX
PORT C
PORT A HIGH
PC8-11
PA4-7
(4)
SEL6
SEL7
PIO SELECT
PORT A LOW
PA8-11
IRS, IRE,
ORS, ORF
(4)
DEVSEL
LXMAR
C1
SKP/INT
CONTROL
HAND-SHAKE CNTRL
STATUS REG
PORT B
PB0-11

ORDERING INFORMATION

ORDER CODE	IM6103-1	IM6103A	IM6103
PLASTIC PKG	IM6103-1IPL	IM6103-AIPL	IM6103-IPL
CERAMIC PKG	IM6103-1IDL	IM6103-AIDL	IM6103-IDL
MILITARY TEMP.	IM6103-1MDL	IM6103-AMDL	—
MILITARY TEMP. WITH 883B	IM6103-1MDL/MDL/883B	IM6103-AMDL/883B	—

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM61031 . . . . -40°C to +85°C
Storage Temperature . . . . -65°C to +150°C
Supply Voltage . . . . +12V
Voltage on Any Input or Output Pin With Respect to GND . . . . . -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = Industrial

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Logical "1" Input Voltage		V_{CC}-1.7			V
2	V_{IL}	Logical "0" Input Voltage				0.8	
3	I_{IL}	Input Leakage	$0V \leqslant V_{IN} \leqslant V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Logical "1" Output Voltage	I_{OUT} = 0 except pins 6, 9	V_{CC}-1.0			V
5	V_{OL}	Logical "0" Output Voltage	I_{OUT} = 0			0.45	
6	I_{OLK}	Output Leakage	$0V \leqslant V_O \leqslant V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Supply Current	V_{CC} = 5V C_L = 50 pF; T_A = 25°C F_{CLOCK} = Operating Frequency			2.5	mA
8	C_{IN}	Input Capacitance			7.0	8.0	pF
9	C_O	Output Capacitance			8.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, C_L = 50pF, All times in ns.

	SYMBOL	PARAMETER		MIN	MAX	UNITS
1	t_{adds}	Address Set-Up Time	DX–LXMAR↓			ns
2	t_{addh}	Address Hold Time	LXMAR↓–DX	150		
3	t_{den}	Output Enable Time	DEVSEL↓–DX		550	
4	t_{dc}	Output Enable Time	DEVSEL↓–C_1		550	
5	t_{di}	Output Enable Time	DEVSEL↓–SKP		400	
6	t_{ds}	Data Set-Up Time	DX–DEVSEL↑	200		
7	t_{dh}	Data Hold Time	DEVSEL↑–DX	150		
8	t_{ps}	Data In Set-Up Time	Port Data In–LXMAR↓	200		
9	t_{ph}	Data In Hold Time	LXMAR↓–Port Data In	225		
10	t_{d1}	Delay Time	DEVSEL↑–Port Data Out		550	
11	t_{bs}	Data In Set-Up Time	Port B In–IRS↓	200		
12	t_{bh}	Data In Hold Time	IRS↓–Port B In	150		
13	t_{d2}	Output Enable Time	ORS↑–Port B Out		550	
14	t_{d2}	Output Disable Time	ORS↓–Port B Out		200	
15	t_{d3}	Delay Time	IRS↓–IRE↓ ORS↓–ORF↓ DEVSEL↑–IRE↑ DEVSEL↑–ORF↑		550	

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IMM6103I. . . . . -40°C to +85°C
Storage Temperature . . . . -65°C to +150°C
Supply Voltage . . . . +8V
Voltage on Any Input or Output Pin With Respect to GND . . . . . . -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = Industrial

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Logical "1" Input Voltage		V_{CC}-1.7			V
2	V_{IL}	Logical "0" Input Voltage				0.8	
3	I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Logical "1" Output Voltage	I_{OH} = -0.2 mA except pins 6,9	V_{CC}-1.0			V
5	V_{OL}	Logical "0" Output Voltage	I_{OL} = 2.0 mA			0.45	
6	I_{OLK}	Output Leakage	$0V \leq V_O \leq V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Supply Current	V_{CC} = 5.0V C_L = 50 pF; T_A = 25°C F_{CLOCK} = Operating Frequency			2.5	mA
8	C_{IN}	Input Capacitance			7.0	8.0	pF
9	C_O	Output Capacitance			8.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, C_L = 50pF, All times in ns.

	SYMBOL	PARAMETER		MIN	MAX	UNITS
1	t_{adds}	Address Set-Up Time	DX—LXMAR↓	80		ns
2	t_{addh}	Address Hold Time	LXMAR↓—DX	100		
3	t_{den}	Output Enable Time	DEVSEL↓—DX		450	
4	t_{dc}	Output Enable Time	DEVSEL↓—C_1		450	
5	t_{di}	Output Enable Time	DEVSEL↓—SKP		330	
6	t_{ds}	Data Set-Up Time	DX—DEVSEL↑	150		
7	t_{dh}	Data Hold Time	DEVSEL↑—DX	100		
8	t_{ps}	Data In Set-Up Time	Port Data In—LXMAR↓	150		
9	t_{ph}	Data In Hold Time	LXMAR↓—Port Data In	175		
10	t_{d1}	Delay Time	DEVSEL↑—Port Data Out		450	
11	t_{bs}	Data In Set-Up Time	Port B in—IRS↓	150		
12	t_{bh}	Data In Hold Time	IRS↓—Port B In	100		
13	t_{d2}	Output Enable Time	ORS↑—Port B Out		450	
14	t_{d2}	Output Disable Time	ORS↓—Port B Out		200	
15	t_{d3}	Delay Time	IRS↓—IRE↓ ORS↓—ORF↓ DEVSEL↑—IRE↑ DEVSEL↑—ORF↑		450	

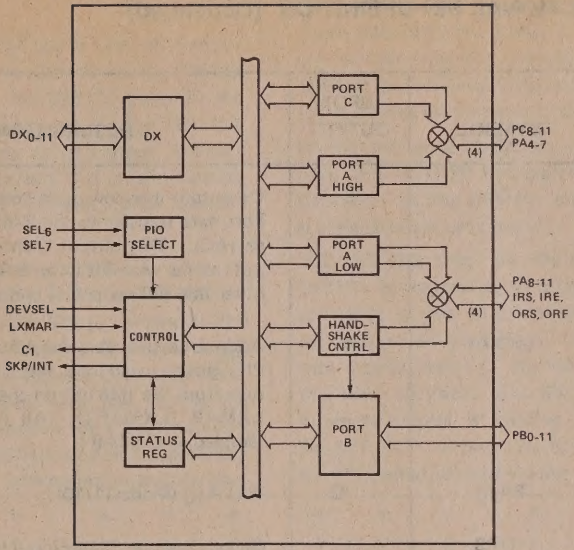

DX$_{0-11}$
DX
SEL$_6$
SEL$_7$
PIO SELECT
DEVSEL
LXMAR
C$_1$
SKP/INT
CONTROL
STATUS REG
PORT C
PORT A HIGH
PORT A LOW
HAND-SHAKE CNTRL
PORT B
PC$_{8-11}$
PA$_{4-7}$
(4)
PA$_{8-11}$
IRS, IRE, ORS, ORF
(4)
PB$_{0-11}$

FIGURE 1: Functional Block Diagram.

IM6103 FUNCTIONAL PIN DEFINITION

PIN NUMBER	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
1	V_{CC}		Positive Power Supply
2	PA_7	I/O	Port A I/O Line (4). Most Significant Bit of Port A in Mode 10.
	PC_{11}	I/O	Port C I/O Line (8) in Mode 11/OX—Most Significant Bit.
3 ~ 5	$PA_6 \sim PA_4$	I/O	Port $A_5 \sim A_7$ (Mode 10).
	$PC_{10} \sim PC_8$	I/O	Port $C_9 \sim C_{11}$ (Mode 11/OX).
6	SKP/INT	O	Time Multiplexed SKP and INTREQ lines to the IM6100 Microprocessor – Active Low.
7	PA_8	I/O	Port A I/O Line in Mode 11/10 – Most Significant Bit of Port A in Mode 11.
	IRS	O	Input Register Strobe to clock data into Port B in Handshake Mode (Mode OX). Port B Latches in the data on the falling edge of IRS (IRS↓).
8	PA_9	I/O	Port A_9 (Mode 11/10).
	IRE	O	Input Register Empty output goes high when Port B input buffer has been read by the IM6100 microprocessor. It goes low when Port B input buffers are strobed in by IRS↓. (Mode OX). PIO may be programmed to generate an INTREQ on IRE↓.

IM6103 FUNCTIONAL PIN DEFINITION (Continued)

PIN NUMBER	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
9	C_1	O	C_1 output goes low upon completion of PIO Port data transfer to the IM6100 Accumulaor (AC). This output is an open-drain output to be wire-OR'D with C_1 Lines from other IM6100 peripheral controllers.
10	LXMAR	I	Address Latch enable signal from the IM6100. PIO clocks in address and control information from the IM6100 on the falling edge of LXMAR (LXMAR↓). All Port inputs are sampled at LXMAR↓.
11	PA_{10}	I/O	Port A_{10} (Mode 11/10).
	ORS	I	Output Register Strobe input to enable Port B output buffers in Mode OX. Port B is tri-stated when ORS is low.
12	DEVSEL	I	Input-Output Device Select control line from the IM6100. It performs both the read and write function. The first negative transition after LXMAR↓, enables the DX output buffers of the selected PIO for a 'read' operation. When DEVSEL returns high, the 'read' operation is terminated. The second negative-going pulse on DEVSEL serves as a 'write' pulse to the selected PIO and the IM6100 AC data is written into the selected PIO register or port on the rising edge.
13	PA_{11}	I/O	Port A_{11} (Mode 11/10)—Least Significant bit of Port A.
	ORF	O	Output Register Full output goes high when the IM6100 writes into Port B in a handshake mode. It goes low when the peripheral device reads Port B by enabling ORS high. The PIO may be programmed to generate an INTREQ on ORF↓ (Mode OX).
14	SEL_6	I	A Chip Select Input. PIO has two chip selects, SEL_6 and SEL_7, thereby enabling up to four PIO chips in a system.
15	SEL_7	I	A Chip Select Input.
16 ~ 25	$DX_0 \sim DX_9$	I/O	The IM6100 System bus (Data and Address).
26	GND		Ground
27 ~ 28	$DX_{10} \sim DX_{11}$	I/O	IM6100 System bus (Data and Address).
29 ~ 40	$PB_0 \sim PB_{11}$	I/O	I/O Port Pin. PB_0 is the most significant bit, and PB_{11} is the least significant bit.

IM6100 SYSTEM TIMING

The tristate bidirectional 12-bit DX bus is used to transfer data and control information (Figure 3) between the IM6103 and the IM6100 microprocessor. The IM6100 transmits the device address and control information on the DX bus during the 'execute' phase of an Input-Output Transfer (IOT) instruction. The IM6103 accepts this information on the falling edge of the LXMAR (Address Latch Enable) Signal.

The address bits (6-7) are compared with the chip select inputs (SEL_6 and SEL_7) to address 1 of 4 PIO's. The IOT address bits (3-5) are programmed internally to respond to the bit pattern 011. The SEL_6 and SEL_7 inputs should be externally hard-wired to match the DX_6 and DX_7 chip select bits. As shown in Fig. 3, DEVSEL goes low, during the first half of an IOT execute machine cycle for a read operation and it goes low again in the second half for a write operation. The IM6103 responds to a 'read' instruction by putting data on the DX bus and C_1 output (of IM6103) low when DEVSEL (from IM6100) input is low. C_1 line goes low to indicate an input transfer cycle to the IM6100. All PIO data transfers to the IM6100 Accumulator (AC) is an 'OR' transfer, (i.e., PIO data is OR'ed into the contents of the AC).

During the write operation into PIO, the PIO accepts data from the IM6100 Accumulator on the rising edge of the DEVSEL. During and after the PIO write, the contents of the accumulator are not cleared.

SKP/INT line goes low during the 'read' DEVSEL if the IM6103 is responding to a 'skip' instruction, and the 'skip' condition is met, therefore causing the IM6100 to skip the next sequential instruction. SKP/INT line reflects the interrupt request status of the IM6100 at all times except during the 'read' DEVSEL. The SKP/INT line goes low if an active interrupt request is pending. During read DEVSEL mode, the SKP/INT indicates the current skip condition. The bits are interpreted as shown below:

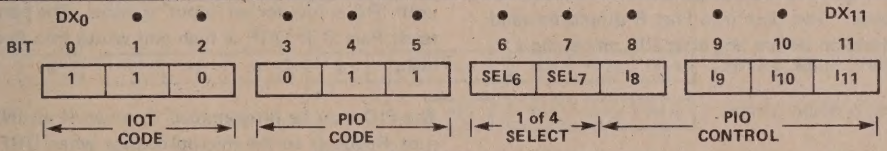

DX0
DX11
BIT
0 1 2 3 4 5 6 7 8 9 10 11
1 1 0
0 1 1
SEL6 SEL7 I8
I9 I10 I11
IOT CODE
PIO CODE
1 of 4 SELECT
PIO CONTROL

FIGURE 2: PIO instruction format.

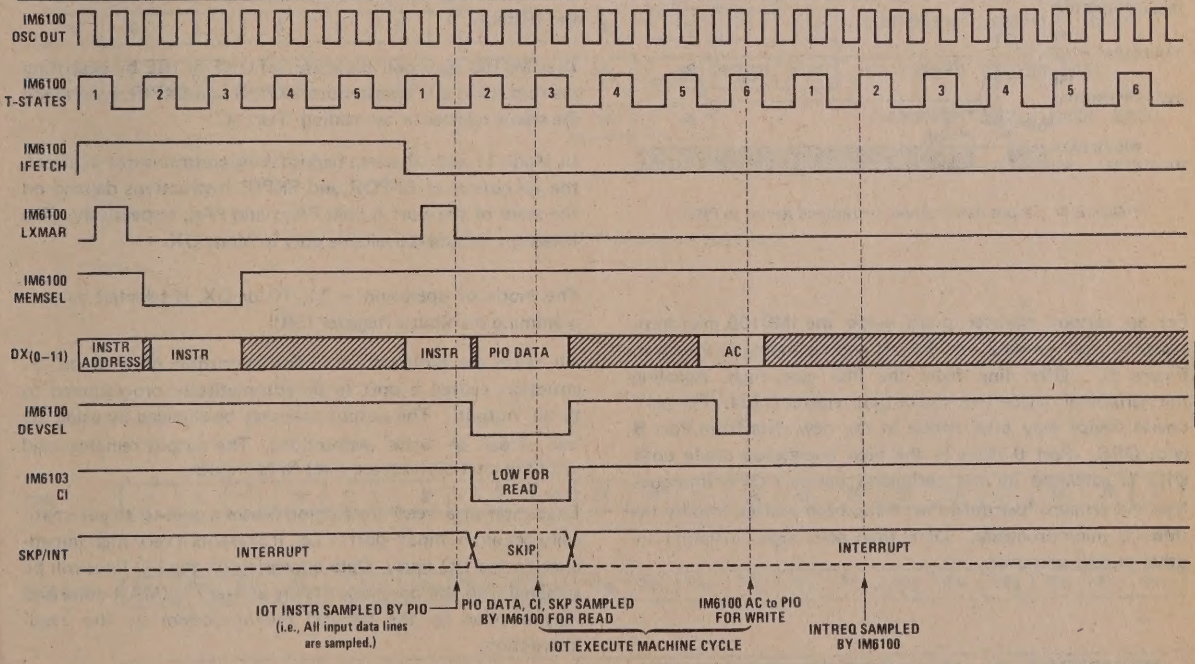

IM6100 OSC OUT
IM6100 T-STATES
1 2 3 4 5 1 2 3 4 5 6 1 2 3 4 5 6
IM6100 IFETCH
IM6100 LXMAR
IM6100 MEMSEL
DX(0–11)
INSTR ADDRESS
INSTR
INSTR
PIO DATA
AC
IM6100 DEVSEL
IM6103 CI
LOW FOR READ
SKP/INT
INTERRUPT
SKIP
INTERRUPT
IOT INSTR SAMPLED BY PIO (i.e., All input data lines are sampled.)
PIO DATA, CI, SKP SAMPLED BY IM6100 FOR READ
IM6100 AC to PIO FOR WRITE
IOT EXECUTE MACHINE CYCLE
INTREQ SAMPLED BY IM6100

FIGURE 3: IM6103 system timing diagram.

OPERATION OF PORT BUFFERS

The IM6103 has 20 I/O pins which can be individually programmed in groups of 4, 8 or 12 bits in three different modes of operation.

In Mode 11, the 20 I/O lines are divided into three ports:
–Port A with 4 bits (PA_8-PA_{11})
–Port B with 12 bits (PB_0-PB_{11})
–Port C with 4 bits (PC_8-PC_{11})

In Mode 10, the 20 I/O lines are grouped into 2 ports–
–Port A with 8 bits (PA_4-PA_{11})
–Port B with 12 bits (PB_0-PB_{11})
–The four I/O lines associated with Port C in Mode 11 (PC_8-PC_{11}) are allocated to Port A as PA_4-PA_7.

In Mode OX, there are two ports—Port B with 12 bits and Port C with 4 bits and four lines for handshake control logic. Four lines of Port A in Mode 11 (PA_8-PA_{11}) are reassigned as handshake control lines. They are:

—Input Register Strobe (IRS)
—Input Register Empty (IRE)
—Output Register Strobe (ORS)
—Output Register Empty (ORE)

The handshake logic controls the data transfer for the Port B. Port C operation remains the same as in Mode 11.

For an 'input' transfer in OX Mode, the input register empty (IRE) output goes high to indicate to the peripheral device that the input register is empty (as shown in Fig. 4). The peripheral device may then strobe in the new data into Port B with Input Register Strobe (IRS). At this time, IRE goes low to indicate to the peripheral device that the input buffer is full, and remains low until Port B has been read by the IM6100 microprocessor. IRE then goes high after the IM6100 executes a Read Port B (RPB) instruction to initiate another input sequence. The data into Port B should be valid only for a short duration before and after IRS makes the 1 to 0 transition.

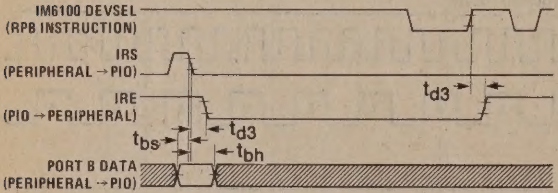


FIGURE 4: Input data transfer (peripheral device to PIO).

For an 'output' transfer in OX mode, the IM6100 microprocessor writes the data into Port B and its timing is shown in Figure 5. ORF line from the PIO goes high, signaling the peripheral device that the output register is full. The peripheral device may then strobe in the new data from Port B with ORS. Port B stays in the high impedance mode until ORS is activated by the peripheral device. ORF line goes low and remains low until Port B has been written into by the IM6100 microprocessor. ORF then goes high, initiating another output sequence.

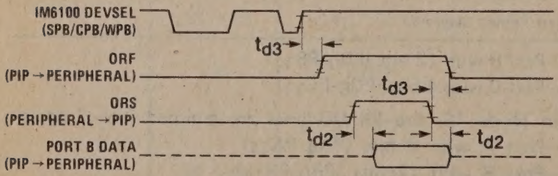


FIGURE 5: Output data transfer (PIO to peripheral device).

The IM6100 monitors the status of ORF (Output Register Full). If it is low (i.e., output register is empty), IM6100 may load data into Port B output buffer with SPB/CPB/WPB instruction. ORF goes high a delay time after the rising edge of the 'write' DEVSEL, signaling the peripheral device that output buffer has new data. During this time, Port B output buffers remain tristated. The peripheral device may then enable and read out Port B output latches by activating ORS (Output Register Strobe) high. The falling edge of ORS (from high to low) signals the PIO that the peripheral device no longer needs the valid current information. Port B is tristated and ORF then goes low, thereafter, to indicate another output sequence.

ORF should be set to 0 and IRE to 1 with a 'write' command in Mode OX, to initiate the handshaking sequence.

The IM6100 microprocessor should not write into Port B until ORF is low for an 'output' transfer and should not read Port B until IRE is low for an 'input' transfer. The peripheral device reads Port B if ORF is high and writes into Port B if IRE is high.

The PIO may be programmed to generate an INTREQ (Interrupt Request) to the microprocessor when ORF or IRE goes low by setting the respective Interrupt enable bits, OREN and IREN.

The IM6100 may poll the status of ORF or IRE by executing the respective skip instructions SKPOR and SKPIR, by reading the status register or by reading "Port A".

In Mode 11 and 10, when handshaking control is not in effect, the execution of SKPOR and SKPIR Instructions depend on the state of the Port A lines PA_{11} and PA_8, respectively. The Interrupt feature is available only in Mode OX.

The mode of operation — 11, 10 or OX, is selected by programming the Status Register (SR).

All ports are bidirectional. The execution of a 'write' instruction caused a port to be automatically programmed to be an 'output'. The output data may be changed by using the 'set', 'clear' or 'write' instructions. The output remains valid until the port bit lines are reset to be inputs.

Execution of a 'read' instruction causes a port to be automatically set as an 'input' port — i.e., it presents a very high impedance to the I/O lines. Data appearing on the I/O lines will be sampled into the port input latch at every LXMAR pulse and may be read by the IM6100 microprocessor by the 'read' instruction.

In Mode OX, Port B acts as a tristate bidirectional buffer which is controlled by an external peripheral device. ORF and IRE lines are outputs and ORS and IRS lines are inputs.

At power-on, all ports are defined to be input ports and the PIO is initialized to be in Mode 10. With 20 I/O lines partitioned into the 8/12 (i.e., Port A = 8 bits, Port B = 12 bits) format.

DX_0	DX_1	DX_2	DX_3	DX_4	DX_5	DX_6	DX_7	DX_8	DX_9	DX_{10}	DX_{11}	DX BUS
1	1	0	0	1	1	SEL_6	SEL_7	I_8	I_9	I_{10}	I_{11}	PIO INSTRUCTION
0	0	0	0	0	0	0	0	PA_8	PA_9	PA_{10}	PA_{11}	PORT A MODE 11 READ
								PA_8	PA_9	PA_{10}	PA_{11}	PORT A MODE 11 WRITE
0	0	0	0	PA_4	PA_5	PA_6	PA_7	PA_8	PA_9	PA_{10}	PA_{11}	PORT A MODE 10 READ
				PA_4	PA_5	PA_6	PA_7	PA_8	PA_9	PA_{10}	PA_{11}	PORT A MODE 10 WRITE
0	0	0	0	0	0	0	0	IRS	IRE	ORS	ORF	PORT A MODE 0X READ
								IREN	IRE	OREN	ORF	PORT A MODE 0X WRITE
PB_0	PB_1	PB_2	PB_3	PB_4	PB_5	PB_6	PB_7	PB_8	PB_9	PB_{10}	PB_{11}	PORT B MODE 11/10/0X READ/WRITE
0	0	0	0	0	0	0	0	PC_8	PC_9	PC_{10}	PC_{11}	PORT C MODE 11/0X READ
								PC_8	PC_9	PC_{10}	PC_{11}	PORT C MODE 11/0X WRITE
0	0	0	0	0	0	0	0	M_8	M_9	PA_{11}	PA_9	STATUS REG MODE 11/10 READ
0	0	0	0	0	0	0	0	M_8	M_9	ORINT	IRINT	STATUS REG MODE 0X READ
								M_8	M_9			STATUS REG MODE 11/10/0X WRITE

FIGURE 6: IM6103 PIO register bit assignments.

PINS	2	3	4	5	7	8	11	13	29	30	31	32	33	34	35	36	37	38	39	40
MODE 10	PA_7	PA_6	PA_5	PA_4	PA_8	PA_9	PA_{10}	PA_{11}	PB_0	PB_1	PB_2	PB_3	PB_4	PB_5	PB_6	PB_6	PB_8	PB_9	PB_{10}	PB_{11}
MODE 11	PC_{11}	PC_{10}	PC_9	PC_8	PA_8	PA_9	PA_{10}	PA_{11}	PB_0	PB_1	PB_2	PB_3	PB_4	PB_5	PB_6	PB_7	PB_8	PB_9	PB_{10}	PB_{11}
MODE 0X	PC_{11}	PC_{10}	PC_9	PC_8	IRS	IRE	ORS	ORF	PB_0	PB_1	PB_2	PB_3	PB_4	PB_5	PB_6	PB_7	PB_8	PB_9	PB_{10}	PB_{11}

FIGURE 7: IM6103 PIO port pin assignments.

PIO INSTRUCTION

NOTE: Symbol Definition – "•" - AND
"+" - OR
"=" - Is Replaced By

PIO CONTROL	MNEMONICS	DESCRIPTION
0 0 0 0	SETPA (Set Port A)	Set PA_i to 1 if AC_i is 1. AC is not cleared. Mode 11: $PA_i=PA_i+AC_i$, $8 \leq i \leq 11$ Mode 10: $PA_i=PA_i+AC_i$, $4 \leq i \leq 11$ Mode OX: $IREN = IREN + AC_8$ $IRE = IRE + AC_9$ $OREN = OREN + AC_{10}$ $ORF = ORF + AC_{11}$
0 0 0 1	CLRPA	Clear Port A. Clear PA_i to 0 if AC_i is 1. AC is not cleared. Mode 11: $PA_i=PA_i \bullet \overline{AC_i}$, $8 \leq i \leq 11$ Mode 10: $PA_i=PA_i \bullet \overline{AC_i}$, $4 \leq i \leq 11$ Mode OX: $IREN = IREN \bullet \overline{AC_8}$ $IRE = IRE \bullet \overline{AC_9}$ $OREN = OREN \bullet \overline{AC_{10}} \bullet$ $ORF = ORF \bullet \overline{AC_{11}}$
0 0 1 0	WPA	Write Port A. Set PA_i equal to AC_i. AC is not cleared. Mode 11: $PA_i=AC_i$, $8 \leq i \leq 11$ Mode 10: $PA_i=AC_i$, $4 \leq i \leq 11$ Mode OX: $IREN = AC_8$ $IRE = AC_9$ $OREN = AC_{10}$ $ORF = AC_{11}$
0 0 1 1	RPA	Read Port A. 'OR' transfer PA to AC. Mode 11: $AC_i=AC_i+PA_i$, $8 \leq i \leq 11$ $AC_i=AC_i$, $0 \leq i \leq 7$ Mode 10: $AC_i=AC_i+PA_i$, $4 \leq i \leq 11$ $AC_i=AC_i$, $0 \leq i \leq 3$ Mode OX: $AC_8=AC_8+IRS$ $AC_9=AC_9+IRE$ $AC_{10}=AC_{10}+ORS$ $AC_{11}=AC_{11}+ORF$ $AC_i=AC_i$, $0 \leq i \leq 7$
0 1 0 0	SETPB	Set Port B. Set PB_i to 1 if AC_i is 1. AC is not cleared. $PB_i=PB_i+AC_i$, $0 \leq i \leq 11$
0 1 0 1	CLRPB	Clear Port B. Clear PB_i to 0 if AC_i is 1. AC is not cleared. $PB_i=PB_i \bullet \overline{AC_i}$, $0 \leq i \leq 11$
0 1 1 0	WPB	Write Port B. Set PB_i equal to AC_i. AC is not cleared. $PB_i=AC_i$, $0 \leq i \leq 11$

PIO CONTROL	MNEMONICS	DESCRIPTION
0 1 1 1	RPB	Read Port B. 'OR' transfer PB to AC. $AC_i=AC_i+PB_i$, $0 \leq i \leq 11$
1 0 0 0	SETPC	Set Port C. Set PC_i to 1 if AC_i is 1. AC is not cleared. Mode 11 and OX: $PC_i=PC_i+AC_i$ $8 \leq i \leq 11$ Mode 10: No operation
1 0 0 1	CLRPC	Clear Port C. Clear PC_i to 0 if AC_i is 1. AC is not cleared. Mode 11 and OX: $PC_i=PC_i \bullet \overline{AC_i}$ $8 \leq i \leq 11$ Mode 10: No operation
1 0 1 0	WPC	Write Port C. Set PC_i equal to AC_i. AC is not cleared. Mode 11 and OX: $PC_i=AC_i$ $8 \leq i \leq 11$ Mode 10: No operation
1 0 1 1	RPC	Read Port C. 'OR' transfer PC to AC. Mode 11 and OX: $AC_i=AC_i+PC_i$ $8 \leq i \leq 11$ Mode 10: No operation
1 1 0 0	SKPOR	Skip the next sequential instruction if PA_{11}/ORF is low. Mode 11 and 10: Skip if PA_{11} is low. Mode OX: Skip if ORF is low.
1 1 0 1	SKPIR	Skip the next sequential instruction if PA_9/IRE is low. Mode 11 and 10: Skip if PA_9 is low. Mode OX: Skip if IRE is low.
1 1 1 0	WSR	Write Status Register. AC is not cleared. $M_8 = AC_8$ $M_9 = AC_9$
1 1 1 1	RSR	Read Status Register. 'OR' transfer Status register to AC. $AC_8 = AC_8 + M_8$ $AC_9 = AC_9 + M_9$ $AC_i = AC_i$, $0 \leq i \leq 7$ Mode 11 and 10: $AC_{10}=AC_{10}+PA_{11}$ $AC_{11}=AC_{11}+PA_9$ Mode OX: $AC_{10}=AC_{10}+ORINT$ $AC_{11}=AC_{11}+IRINT$

STATUS REGISTER

The Status Register (SR) has 2 mode bits, M_8 and M_9 which can be modified by the WSR (Write Status Register) instruction. These two bits define the mode of operation for the IM6103 as shown in Figure 8.

M_8	M_9	MODE	PORT OPERATION
0	*	Mode OX	PB_{0-11}, PC_{8-11}, IRS, IRE, ORS, ORF
1	0	Mode 10	PB_{0-11}, PA_{4-11}
1	1	Mode 11	PB_{0-11}, PC_{8-11}, PA_{8-11}

FIGURE 8: Mode bit assignments.

The Mode and Interrupt status bits, ORINT (Output Register empty Interrupt) and IRINT (Input Register empty Interrupt), may be read with the RSR (Read Status Register) instruction. The interrupt status bits are set to 0 if the corresponding flag is requesting an interrupt.

In Mode 11/10 the current value of PA_{11} and PA_9 can be interrogated. In this mode, Port A can be either an input or an output. M_8 and M_9 are initialized to "11" at power-on.

DX_8	DX_9	DX_{10}	DX_{11}	DX	BUS	
M_8	M_9	ORINT	IRINT	SR	MODE OX	READ
M_8	M_9	PA_{11}	PA_9	SR	MODE 11/10	READ
M_8	M_9			SR	MODE 11/10/OX	WRITE

FIGURE 9: Status register bit assignments.

SKIP OPERATION

The IM6100 may poll the status of ORF or IRE in Mode OX, by executing a skip instruction, SKPOR or SKPIR. The IM6103 will assert the SKP/INT line low if the corresponding status line (ORF or IRE) is low, causing the next sequential instruction to be skipped. During this cycle, ORF and IRE remain unchanged.

In Mode 11/10, SKPOR and SKPIR instruction executions depend on the state of PA_{11} and PA_9, respectively. Port A may be an input or output port.

If ORF is reset to 0 by executing a CLRPA or WPA instruction to initiate the handshaking sequence, the next SKPOR instruction will cause the next sequential instruction to be skipped.

INTERRUPT OPERATION

The IM6103 may be programmed to generate an interrupt request input (INTREQ) when ORF or IRE goes low, by setting the corresponding interrupt enable bits, OREN or IREN, to 1. If the IM6100 interrupt system has been previously enabled, the microprocessor will acknowledge the INTREQ input. If the IM6100 μP does not see the higher priority INTREQ's, inputs from other peripheral controllers such as IM6102 Memory Extender/Direct Memory Access/Internal Timer Controller (MEDIC) or IM6101 Parallel Interface Elements (PIE) in the system, the interrupt service routine should initiate a software poll of the PIO's in the system to identify the particular PIO that generated the INTREQ. In Mode OX, the interrupt request status of ORF and IRE may be identified by reading the Status Register. ORINT or IRINT will be set to 0 if ORF (being low) or IRE (being low) is generating an INTREQ. Note that IM6102 MEDIC and IM6101 PIE provide an automatic priority vectoring.

The interrupt feature of IM6103 is available only in Mode OX. An ORF INTREQ may be removed by one of the following methods:

- executing a SPB/CPB/WPB Instruction (ORF goes high if Port B is written into), or
- setting ORF to 1 with SPA/WPA Instruction, or
- by resetting OREN to 0 with a CPA/WPA Instruction, or
- by changing to Mode 11/10.

An IRE INTREQ may be removed by:

- executing a RPB Instruction (IRE goes high after Port B is read), or
- setting IRE to 1 with SPA/WPA Instructions, or
- resetting IREN to 0 with a CPA/WPA Instruction, or
- changing to Mode 11/10.

PIO may be software programmed to generate an INTREQ to the IM6100 by resetting ORF or IRE to 0 with a CPA/WPA Instruction and by setting the corresponding enable bit, OREN or IREN, with a SPA/WPA Instruction in Mode OX.

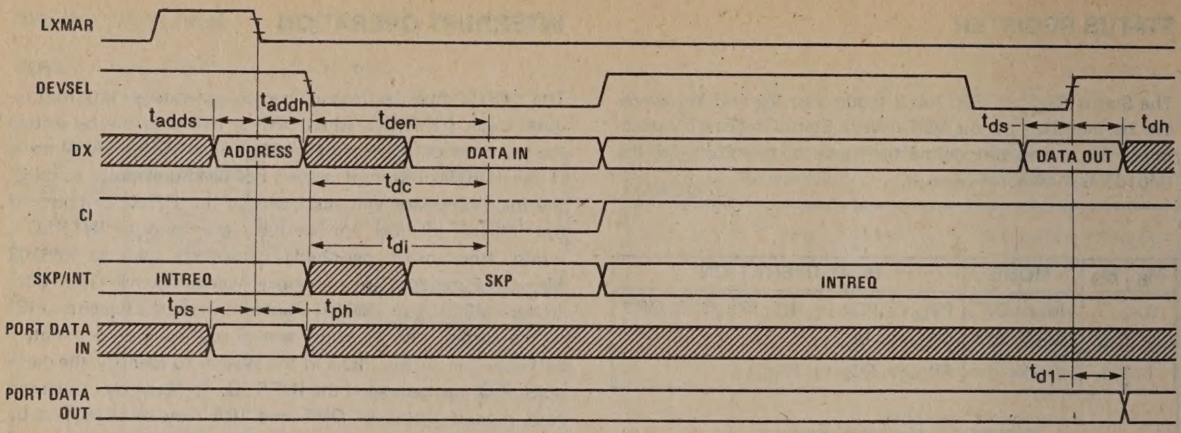

LXMAR
DEVSEL
DX
CI
SKP/INT
PORT DATA IN
PORT DATA OUT
t_{adds}
t_{addh}
t_{den}
t_{dc}
t_{di}
t_{ps}
t_{ph}
t_{ds}
t_{dh}
t_{d1}
ADDRESS
DATA IN
DATA OUT
INTREQ
SKP
INTREQ

FIGURE 10: IM6103 PIO timing diagram.

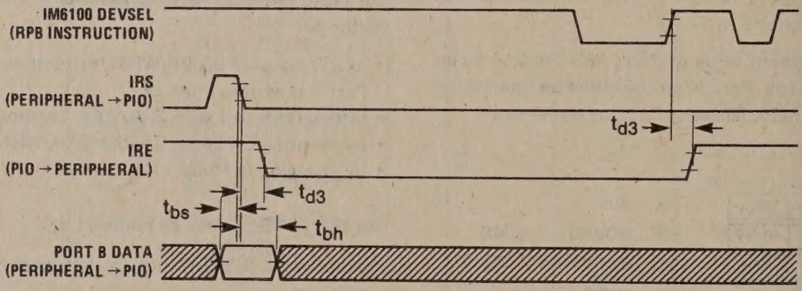

IM6100 DEVSEL (RPB INSTRUCTION)
IRS (PERIPHERAL → PIO)
IRE (PIO → PERIPHERAL)
PORT B DATA (PERIPHERAL → PIO)
t_{d3}
t_{d3}
t_{bs}
t_{bh}

FIGURE 11: Input data transfer (peripheral device to PIO).

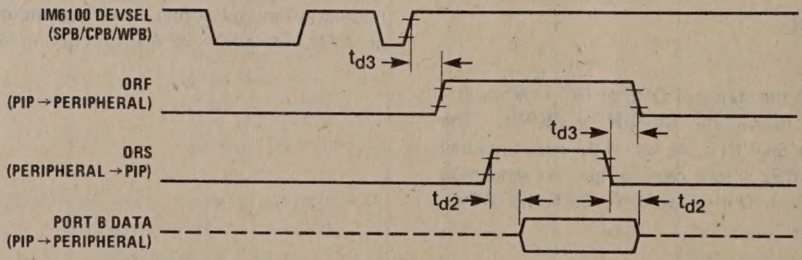

IM6100 DEVSEL (SPB/CPB/WPB)
ORF (PIP → PERIPHERAL)
ORS (PERIPHERAL → PIP)
PORT B DATA (PIP → PERIPHERAL)
t_{d3}
t_{d3}
t_{d2}
t_{d2}

FIGURE 12: Output data transfer (PIO to peripheral device).

APPLICATION OF IM6103

Figure 13 illustrates a microcomputer system block diagram using IM6103 in a dual processor system.

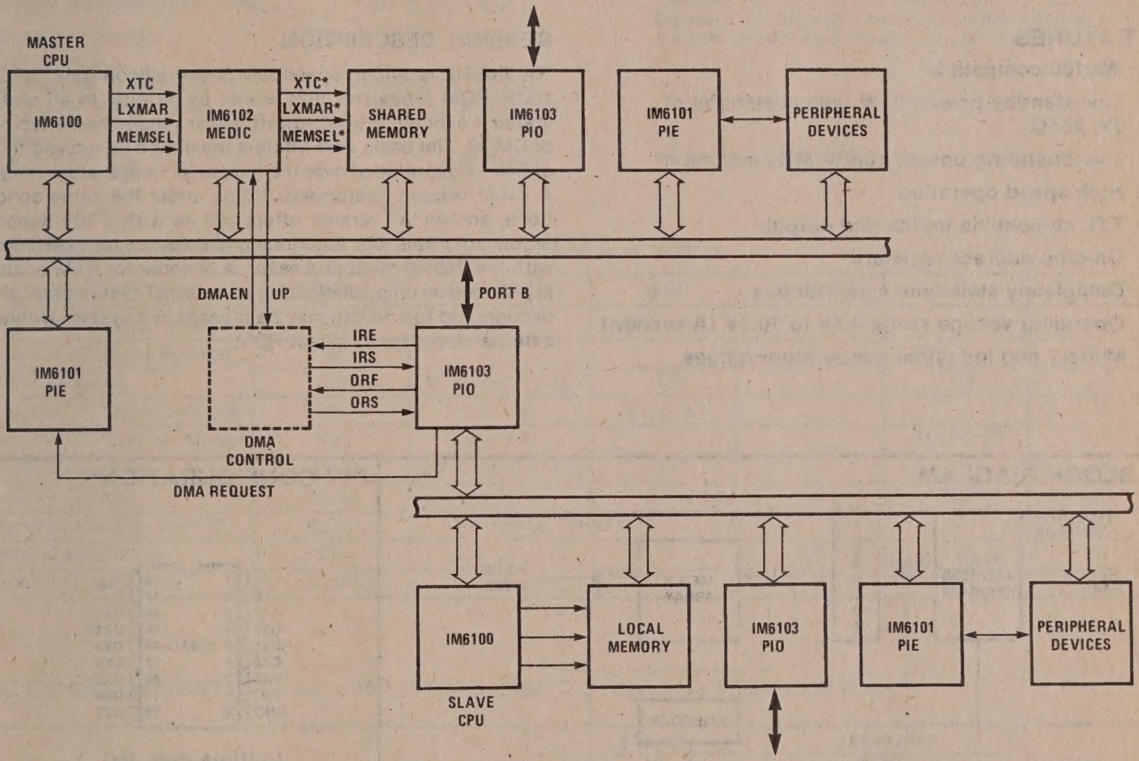

MASTER CPU
IM6100
XTC
LXMAR
MEMSEL
IM6102 MEDIC
XTC*
LXMAR*
MEMSEL*
SHARED MEMORY
IM6103 PIO
IM6101 PIE
PERIPHERAL DEVICES
DMAEN
UP
PORT B
IM6101 PIE
IRE
IRS
ORF
ORS
IM6103 PIO
DMA CONTROL
DMA REQUEST
IM6100
LOCAL MEMORY
IM6103 PIO
IM6101 PIE
PERIPHERAL DEVICES
SLAVE CPU

FIGURE 13: Dual processor system with shared memory.

IM6312 CMOS ROM
1024 Word x 12 Bit

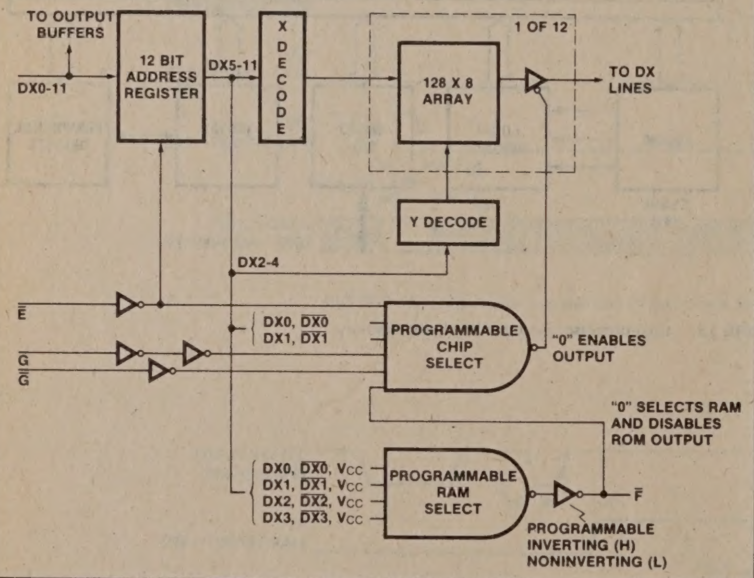
FEATURES

- IM6100 compatible
- Low standby power: 5μW typical standby at 5V, 25°C
- Low operating power: 10mW/MHz maximum
- High speed operation
- TTL compatible inputs and outputs
- On-chip address registers
- Completely static and synchronous
- Operating voltage range 4.5V to 10.5V (A version)
- Military and industrial temperature ranges

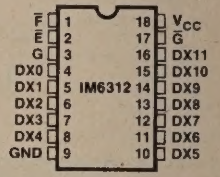
GENERAL DESCRIPTION

The IM6312 is a high speed low power silicon gate CMOS static ROM organized 1024 words by 12 bits. In all static states it exhibits the microwatt power requirements typical of CMOS. The basic part offers a maximum 5V access time of 640 ns guaranteed over the industrial temperature range. A "–1" version guarantees 510 ns under the same conditions, and an "A" version offers 200 ns with a 10V supply. Signal polarities and functions are specified for interfacing with the IM6100 microprocessor. A decoder for RAM enable is provided on chip, eliminating an external 4 bit register and decoder. Up to 4 ROMs may be present in a system without external decoders to select ROM.

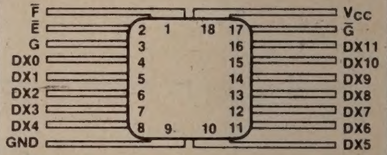
BLOCK DIAGRAM


TO OUTPUT BUFFERS
DX0-11
12 BIT ADDRESS REGISTER
DX5-11
X DECODE
1 OF 12
128 X 8 ARRAY
TO DX LINES
Y DECODE
DX2-4
$\overline{E}$
G
$\overline{G}$
DX0, $\overline{DX0}$
DX1, $\overline{DX1}$
PROGRAMMABLE CHIP SELECT
"0" ENABLES OUTPUT
"0" SELECTS RAM AND DISABLES ROM OUTPUT
DX0, $\overline{DX0}$, Vcc
DX1, $\overline{DX1}$, Vcc
DX2, $\overline{DX2}$, Vcc
DX3, $\overline{DX3}$, Vcc
PROGRAMMABLE RAM SELECT
$\overline{F}$
PROGRAMMABLE INVERTING (H) NONINVERTING (L)

PIN CONFIGURATIONS


$\overline{F}$ 1
$\overline{E}$ 2
G 3
DX0 4
DX1 5
DX2 6
DX3 7
DX4 8
GND 9
IM6312
18 Vcc
17 $\overline{G}$
16 DX11
15 DX10
14 DX9
13 DX8
12 DX7
11 DX6
10 DX5

(outline dwg JN)


$\overline{F}$
$\overline{E}$
G
DX0
DX1
DX2
DX3
DX4
GND
1 2 3 4 5 6 7 8 9
18 17 16 15 14 13 12 11 10
Vcc
$\overline{G}$
DX11
DX10
DX9
DX8
DX7
DX6
DX5

(outline dwg FN)

ORDERING INFORMATION

MEMORY CIRCUIT MARKING AND PRODUCT CODE EXPLANATION

IM 6312 A I JN

Package
JN — Cerdip 18 pin
FN — Flatpack 18 pin

Temperature Range
I — Industrial (–40°C to +85°C)
M — Military (–55°C to +125°C)

Voltage Range Option
No code = 5V
A = 10V

Device Type

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +12.0V

Applied Input or Output Voltage .... GND -0.3V to V_{CC} + 0.3V

Storage Temperature Range .... -65°C to +150°C

Operating Range
  Temperature
    Industrial (IM6312AI) .... -40°C to +85°C
    Military (IM6312AM) .... -55°C to +125°C

Voltage
  IM6312AI, AM 4.5-10.5V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS V_{CC} = 4.5V—10.5V, T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{ILK}	$0V \le V_{IN} \le V_{CC}$	−1.0		+1.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OH} = 0$	V_{CC}—0.1			V
Logical "0" Output Voltage	V_{OL}	$I_{OL} = 0$			GND +.01	V
Output Leakage	I_{OLK}	$0V \le V_{OLK} \le V_{CC}$	−1.0		1.0	μA
Supply Current	I_{CCSB}			1.0	500	μA
Dynamic Supply Current	I_{CCOP}	f = 1MHz			2	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_{OUT}			6.0	10.0	pF

AC CHARACTERISTICS V_{CC} = 10V ±5%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	6312AI		6312AM		UNITS
		MIN	MAX	MIN	MAX	
Access time from $\overline{E}$	TELQV		250		300	ns
Output enable time	TGHQV		160		175	
Output disable time	TGLQZ		160		175	
Strobe ($\overline{E}$) positive pulse width	TEHEL	125		140		
Address setup time	TAVEL	30		35		
Address hold time	TELAX	60		60		
Propagation delay, address to $\overline{F}$	TAVFV		100		110	
Propagation delay, address to $\overline{F}$	TEHFX		100		110	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Applied Input or Output Voltage	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Range	
Temperature	
Industrial (IM6312I/-1I)	-40°C to +85°C
Military (IM6312-1M)	-55°C to +125°C
Voltage	
IM6312-1I, -1M, I, M	4.5-5.5V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS V_{CC} = 5.0V ±10%, T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	IM6312-1I/-1M MIN.	TYP.	MAX.	IM6312I, M MIN.	TYP.	MAX.	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}-2V			V_{CC}-1.5			V
Logical "0" Input Voltage	V_{IL}				0.8V			0.8	V
Input Leakage	I_{ILK}	$0V \leq V_{IN} \leq V_{CC}$	-1.0		+1.0	-5.0		+5.0	µA
Logical "1" Output Voltage	V_{OH}	I_{OH}=-0.2mA	2.4			2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL}=2.0mA			0.45				V
Logical "0" Output Voltage	V_{OL}	I_{OL}=1.6mA						0.45	V
Output Leakage	I_{OLK}	$0V \leq V_O \leq V_{CC}$	-1.0		1.0	-5.0		5.0	µA
Supply Current	I_{CCSB}	V_{IN}=V_{CC} or GND		1.0	100			800	µA
Dynamic Supply Current	I_{CCOP}	f=1MHz		1.5	1.8		1.5	1.8	mA
Input Capacitance	C_{IN}			5.0	7.0		5.0	7.0	pF
Output Capacitance	C_{OUT}			6.0	10.0		6.0	10.0	pF

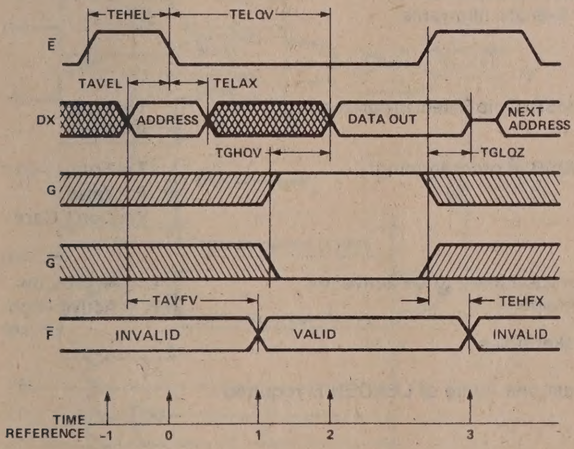
AC CHARACTERISTICS V_{CC} = 5.0V ±10%, C_L = 50pF, T_A = Industrial or Military

PARAMETER	SYMBOL	IM6312-1I MIN.	MAX.	IM6312-1M MIN.	MAX.	IM6312I,M MIN.	MAX.	UNITS
Access Time from $\overline{E}$	TELQV		510		560		640	ns
Output Enable Time	TGHQV		290		320		390	
Output Disable Time	TGLQZ		290		320		390	
Strobe Positive Pulse Width	TEHEL	260		285		300		
Address Setup Time	TAVEL	75		75		85		
Address Hold Time	TELAX	120		135		140		
Propagation Delay, Address to $\overline{F}$	TAVFV		220		240		250	
Propagation Delay, Address to $\overline{F}$	TEHFX		220		240		250	

PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	$\overline{F}$	H/L	RAM select, can be programmed to be active high or low. Used to enable specified RAM address field and disable ROM outputs.
2	$\overline{E}$	L	Strobe, latches address lines and enables outputs
3	G	H	Output enable
4-8, 10-16	DX_0-DX_{11}	—	Address inputs, data outputs
9	GND	—	Ground
17	$\overline{G}$	L	Output enable
18	V_{CC}	—	Chip +V supply

READ CYCLE TIMING



READ OPERATION

Address information is latched into on-chip registers by the falling edge of strobe line $\overline{E}$. Address information must be removed after address hold time (TELAX) to allow placing of Data Out on DX lines. Data Out is valid an access time (TELQV) after the falling edge of $\overline{E}$ if outputs are enabled, i.e. if $\overline{E}$ remains low, G is high and $\overline{G}$ is low.

RAM select $\overline{F}$ becomes valid a propagation delay time TAVFV after the address has been asserted, and invalid a propagation time TEHFX after strobe $\overline{E}$ returns to a high level.

Valid output data will be read only if decoded states of DX0 and DX1 are true. (See Chip Select Programming)

FUNCTION TABLE

TIME REF	INPUTS			OUTPUTS		NOTES
	E	G	A*	F	Q*	
-1	H	X	X	$\overline{V}$	Z	Memory inactive, DX lines indeterminate RAM is disabled
0		X	V	$\overline{V}$	Z	Addresses placed on DX lines, latched by E
1	L	X	X	V	Z	RAM select valid
2	L	H	Z	V	V	Data out valid on DX lines or RAM selected depending on address
3	H	X	X	$\overline{V}$	Z	Output disabled, DX lines switching to high Z

*Addresses (A) and data out (Q) multiplexed on DX lines.

**$\overline{V}$ = Invalid Level

IM6312 CUSTOM ROM PROGRAMMING

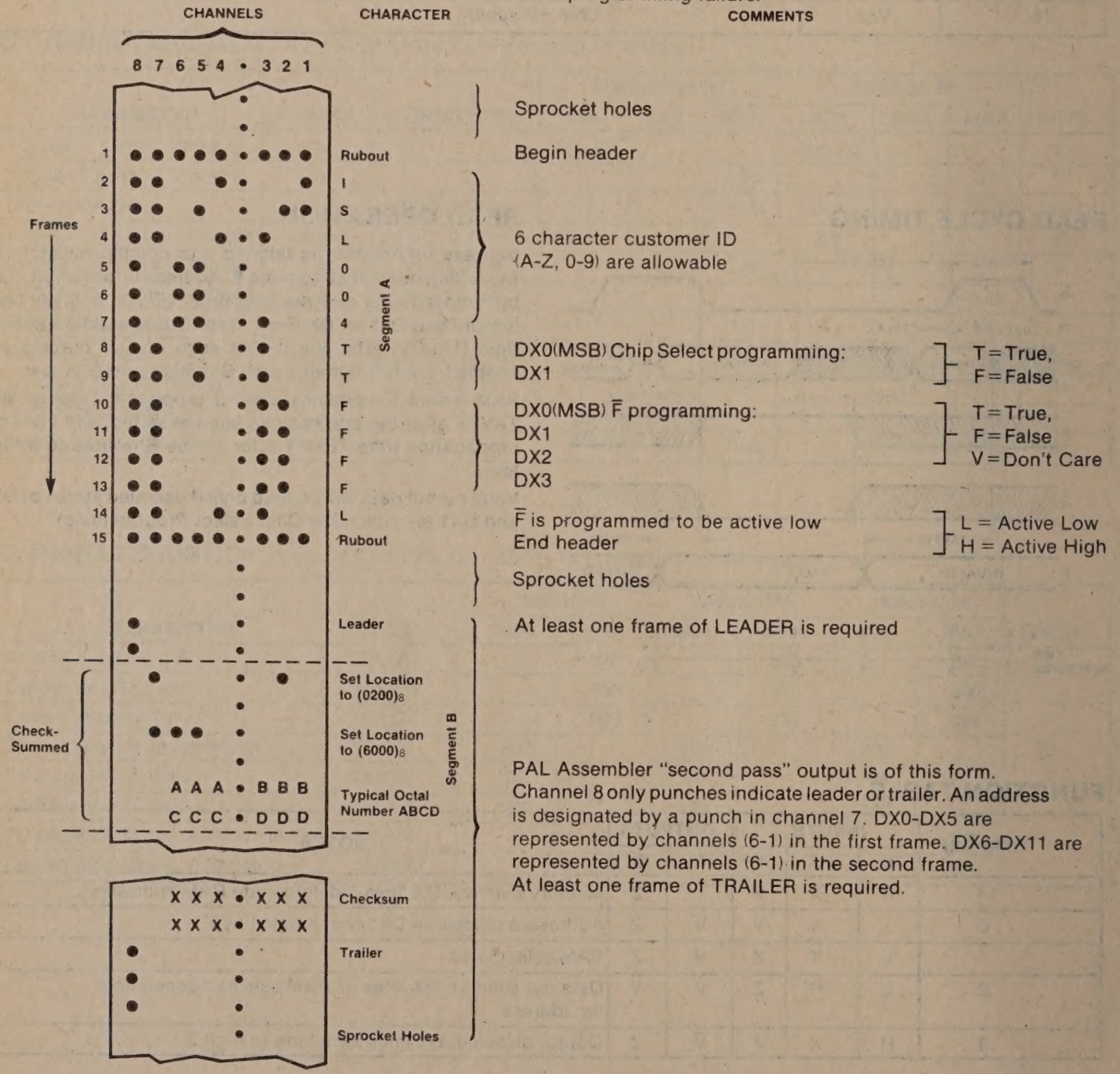
An IM6312 ROM programming papertape consists of two segments (A and B), preceded by at least one foot of sprocket holes (no channels punched). Segment A is the header, and consists of frames 1-15 (see Fig. 1). Segment B contains at least one leader frame, location setting commands, data and checksum. The tape concludes with a minimum of one leader/trailer frame and a foot or more of sprocket holes.

NOTES

1. Each ROM pattern must be prepared on a separate papertape.
2. Data/address (DX) lines are numbered from DX0 (MSB) to DX11 (LSB).
3. A *punched* hole is considered a logical "1".
4. The following terms are synonymous
   (True, High, T, H, Logical "1")
   (False, Low, F, L, Logical "0")
5. No field change characters are allowed.

HEADER (Frames 1-15)

The header (Figure 1) begins with a rubout followed by six ASCII characters identifying the customer and pattern number. Frames 8 and 9 specify the states of DX0 and DX1 during $\overline{E}$, which enable the chip. The RAM Select ($\overline{F}$) output is programmed with frames 10-14. A rubout (all eight channels punched) in frame 15 concludes the header. Any rubout between frames 1 and 15 will invalidate the header and cause programming failure.


CHANNELS
CHARACTER
COMMENTS
8 7 6 5 4 • 3 2 1
Frames
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Rubout
I
S
L
0
0
4
T
T
F
F
F
F
L
Rubout
Segment A
Leader
Set Location to $(0200)_8$
Set Location to $(6000)_8$
A A A • B B B
C C C • D D D
Typical Octal Number ABCD
Check-Summed
Segment B
X X X • X X X
X X X • X X X
Checksum
Trailer
Sprocket Holes
T = True, F = False
T = True, F = False, V = Don't Care
L = Active Low
H = Active High

Sprocket holes

Begin header

6 character customer ID (A-Z, 0-9) are allowable

DX0(MSB) Chip Select programming:
DX1

DX0(MSB) $\overline{F}$ programming:
DX1
DX2
DX3

$\overline{F}$ is programmed to be active low
End header

Sprocket holes

At least one frame of LEADER is required

PAL Assembler "second pass" output is of this form. Channel 8 only punches indicate leader or trailer. An address is designated by a punch in channel 7. DX0-DX5 are represented by channels (6-1) in the first frame. DX6-DX11 are represented by channels (6-1) in the second frame. At least one frame of TRAILER is required.

The example shown above has customer ID and pattern ISL004. Chip selects are programmed to recognize addresses $6000-7777_8$ or $3072-4095_{10}$. $\overline{F}$ is active low for addresses $0000-0377_8$ or $0000-0255_{10}$. Unused locations are automatically programmed to a logic zero.

Figure 1

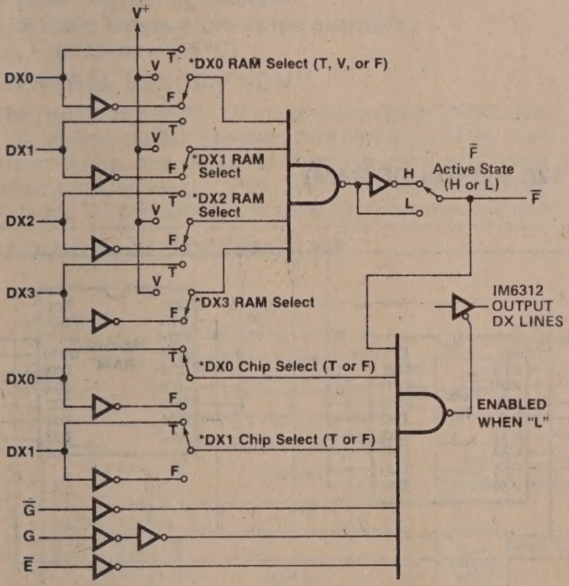
CHIP SELECT PROGRAMMING (Frames 8, 9)

IM6312 outputs are enabled when $\overline{G}$ and $\overline{E}$ are low, G is high, and the states of DX0 and DX1 agree with the conditions specified in frames 8 (DX0) and 9 (DX1) of the header. To specify a particular ROM address field frames 8 and 9 must be programmed as follows:

Table 1

FRAME 8 (DX$_0$)	FRAME 9 (DX$_1$)	ADDRESS FIELD
F	F	0000_8-1777_8
F	T	2000_8-3777_8
T	F	4000_8-5777_8
T	T	6000_8-7777_8

For example, to program the ROM for address field 4000_8-5777_8 header frame 8 must be T and frame 9 must be F. Figure 2 diagrams the chip and RAM select logic.


V+
DX0
DX1
DX2
DX3
DX0
DX1
$\overline{G}$
G
$\overline{E}$
T
V
F
*DX0 RAM Select (T, V, or F)
*DX1 RAM Select
*DX2 RAM Select
*DX3 RAM Select
*DX0 Chip Select (T or F)
*DX1 Chip Select (T or F)
$\overline{F}$ Active State (H or L)
H
L
$\overline{F}$
IM6312 OUTPUT DX LINES
ENABLED WHEN "L"

*The "positions" of these "switches" are specified by the ROM programming tape (segment A).

Figure 2

RAM SELECT PROGRAMMING (Frames 10-14)

Most memory systems contain both RAM and ROM. The designer of such a system must insure that accesses to RAM memory space do not enable the ROMs and vice versa. The IM6312 ROM decodes address information on DX0 and DX1 to provide a unique 1024 word address space dedicated to itself. It also provides a RAM Select ($\overline{F}$) output which may be used to enable an address space dedicated to RAM. The states of DX0-DX3 which activate $\overline{F}$ are programmed by frames 10-13 respectively. Frame 14 determines whether $\overline{F}$ is considered active when high (frame 14 = H) or active when low (frame 14 = L).

Frames 10-13 may be T (true), V (don't care), or F (false). For example, if frames 10-13 are FTFV respectively, $\overline{F}$ will be active when address information on DX0 and DX2 is F (low) and DX1 is T (high). DX3 may be either T or F, since it is programmed V ("don't care") (see Table 3). Thus, in this example, RAMs using $\overline{F}$ as an enable will respond to addresses 2000_8 through 2777_8.

Table 2

Channel	Function
8 only	Leader/Trailer
8+ (6-1)	Header
7+ (6-1)	Location Setting (first frame)
6-1 only	Data, Checksum, Location Setting (second frame)

Table 3

Frames 10-13	RSEL Enable Condition
T	DXn must be high to enable
F	DXn must be low to enable
V	DXn may be either high or low to enable

LOCATION SETTING/DATA

It is not necessary to specify the contents of all 1024 words in the IM6312. Words that are not explicitly programmed will contain all zeros.

Data words are entered into sequential locations in ROM, beginning from the address specified by the most recently encountered location setting command. For this reason, such a command must precede any data words. A new location setting command may be given; subsequent data words will be entered beginning at the *new* address.

The location setting command consists of two sequential frames. The initial frame has channel 7 punched with the remaining channels (6-1) representing the most significant six bits of a 12-bit word. The second frame has no punches in channel 8 or 7, and represents the least significant 6 bits of the word (see Table 1).

Figure 3 shows an example of location setting to 0410_8. Subsequent data words will be stored in locations 0410_8, 0411_8, etc.

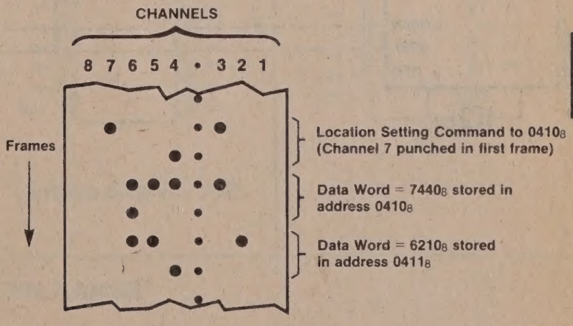

CHANNELS
8 7 6 5 4 • 3 2 1
Frames
Location Setting Command to 0410_8 (Channel 7 punched in first frame)
Data Word = 7440_8 stored in address 0410_8
Data Word = 6210_8 stored in address 0411_8

Figure 3

A data word consists of two frames with channels 8 and 7 unpunched. The two groups of six holes remaining are then concatenated to form a 12-bit binary number (punched = H, unpunched = L). The most significant six bits are punched first (channels 6-1 with 8 and 7 unpunched), followed by the least significant bits. The MSB of the 12-bit data word is channel 6 of the first frame; the LSB is channel 1 of the second frame. Figure 3 shows examples of two data words, 7440_8 and 6210_8.

CHECKSUM

A two frame checksum precedes the leader/trailer at the end of segment B. It is the modulo 4096 sum of all frames in segment B following the initial leader/trailer and preceding the final leader/trailer (except the two frames that represent the checksum itself). For purposes of checksum computation, each frame is to be considered an 8-bit binary word. The 12-bit result is punched out in two sequential frames, with channels 8 and 7 unpunched. The most significant six bits are punched first, followed by the least significant six bits as with the data word format. Any frame with channel 7 or 8 punched (e.g. leader or location setting command) is not included in the checksum computation. For additional BIN format information, refer to "PDP®-8 Family/Commonly Used Utility Routines".

COMPATIBLE ASSEMBLER PROGRAMS

PAL III, FOPAL III, MACRO-8, PAL 8, and IFDOS PAL are assembler programs for the IM6100 microprocessor which prepare a papertape conforming to the specifications for the second tape segment. The header must in any case be produced manually.

The input to a PAL assembler is ASCII source code. More information and PAL assemblers are available from Intersil. The first frame-pair in a segment B produced by PAL III is a location setting command to address 0200_8. This is ignored if another origin setting follows immediately afterwards.

Some PAL assemblers produce a checksum with 13 bits (i.e., channel 7 of the first frame of the checksum may be punched). If channel 7 is punched, it is ignored.

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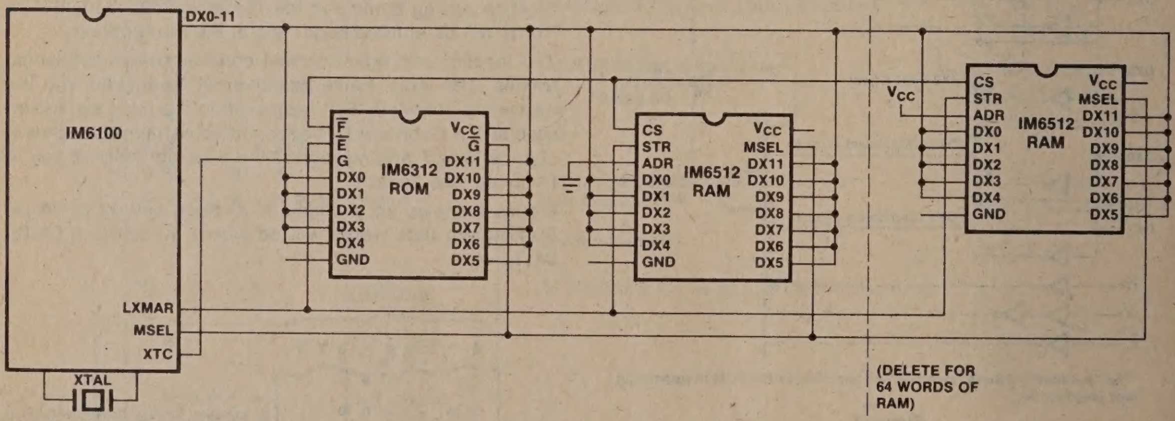
A MINIMAL MICROPROCESSOR SYSTEM (64 OR 128 WORDS OF RAM)



IM6100
DX0-11
LXMAR
MSEL
XTC
XTAL
F̄
Ē
G
DX0
DX1
DX2
DX3
DX4
GND
IM6312
ROM
V_CC
Ḡ
DX11
DX10
DX9
DX8
DX7
DX6
DX5
CS
STR
ADR
DX0
DX1
DX2
DX3
DX4
GND
IM6512
RAM
Vcc
MSEL
DX11
DX10
DX9
DX8
DX7
DX6
DX5
Vcc
CS
STR
ADR
DX0
DX1
DX2
DX3
DX4
GND
IM6512
RAM
Vcc
MSEL
DX11
DX10
DX9
DX8
DX7
DX6
DX5
(DELETE FOR 64 WORDS OF RAM)

INTERSIL

IM6316
16,384 Bit (2048x8) CMOS ROM

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

- Low standby power: 11 mW maximum
- High speed: 550ns maximum
- On-chip address registers
- TTl compatible inputs and three-state outputs
- Completely static and asynchronous
- Single 5V supply
- Intel 2316E and Mostek MK34000 pin compatible
- Two mask programmable chip selects (active level latched/unlatched)
- Outputs mask programmable (latched/unlatched)
- 883B Processing available
- Military temperature range available (−55°C to +125°C)

GENERAL DESCRIPTION

The IM6316 is a 16,384-bit static silicon-gate CMOS read-only-memory (ROM) organized 2048 words by 8 bits. In all static states, this device exhibits the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and two mask programmable chip-selects simplify system interfacing requirements.

The IM6316 operates over a 4.5V to 5.5V range, with an access time of 550ns and standby current of 200 μA guaranteed over the industrial temperature range.

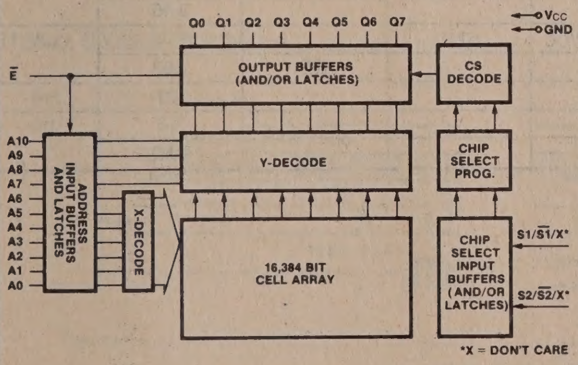
FUNCTIONAL DESCRIPTION

The falling edge of chip enable (E) latches addresses in the on-chip register and initiates a read cycle. Address and chip selects to be latched must be present a setup time (TAVEL) prior to, and a hold time (TELAX) following the falling edge of E. After an access time, valid data will be available.

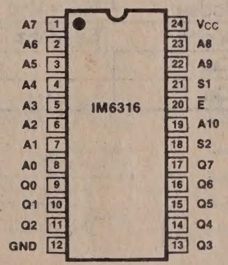
Optional latched outputs are active when S1 and S2 (or latched S1 and S2) are active. For unlatched outputs, E must also be low to enable.

Optional latches for S1 and S2 are level sensitive. When E is high, latched S1 and S2 thus perform as if they were not latched.

LOGICAL BLOCK DIAGRAM

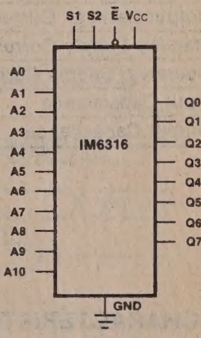

Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
Vcc
GND
Ē
OUTPUT BUFFERS (AND/OR LATCHES)
CS DECODE
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
ADDRESS INPUT BUFFERS AND LATCHES
Y-DECODE
CHIP SELECT PROG.
X-DECODE
16,384 BIT CELL ARRAY
CHIP SELECT INPUT BUFFERS (AND/OR LATCHES)
S1/S̄1/X*
S2/S̄2/X*
*X = DON'T CARE

PIN CONFIGURATION


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
IM6316
24 Vcc
23 A8
22 A9
21 S1
20 Ē
19 A10
18 S2
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

(outline dwg JG, PG)

LOGIC SYMBOL


S1 S2 Ē Vcc
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
IM6316
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
GND

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
IM6316IPG	24 PIN PLASTIC	−40°C to +85°C
IM6316IJG	24 PIN CERDIP	−40°C to +85°C
IM6316MJG	24 PIN CERDIP	−55°C to +125°C

PIN NAMES

A0-A10	ADDRESS INPUTS
Q0-Q7	DATA OUTPUTS
Ē	ADDR. STROBE/CHIP ENABLE
S1, S2	CHIP SELECTS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND −0.3V to V_{CC} +0.3V
Storage Temperature Range	−65° C to +150° C
Operating Range	
Temperature	
Industrial	−40° C to +85° C
Voltage	
IM6316I	4.5V to 5.5V

Note:

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Test Conditions: V_{CC} = 5V ±10%, T_A = Operating Temperature Range

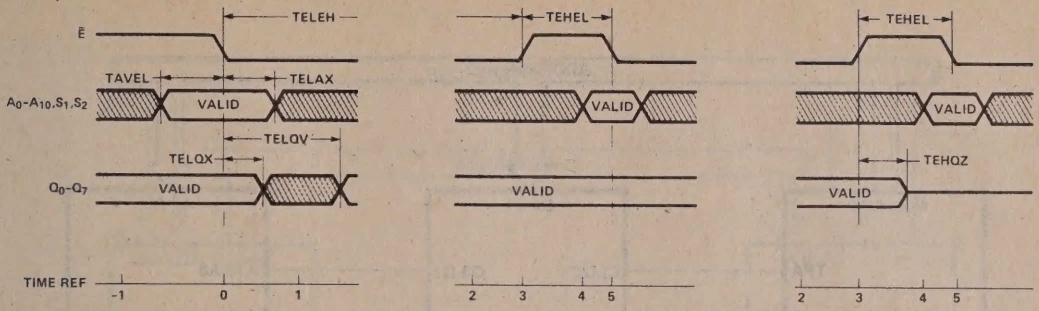
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC} −2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage Current	I_{ILK}	GND ≤ V_{IN} ≤ V_{CC}	−1.0		+1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC} −0.01			V
	V_{OH}	I_{OUT} = −0.2mA	2.4			
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND +0.01	
	V_{OL}	I_{OUT} = 2.0mA			0.45	
Output Leakage Current	I_{OLK}	GND ≤ V_{IN} ≤ V_{CC}	−1.0		+1.0	μA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}		100	200	
Operating Supply Current	I_{CCOP}	f = 1Mhz			20	mA
Input Capacitance	C_{IN}				7.0	pf
Output Capacitance	C_O				10.0	

AC CHARACTERISTICS

Test Conditions: V_{CC} = 5V ±10%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	6316I			6316M			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Access Time From $\bar{E}$	TELQV			550			625	ns
Output Enable Time	TSVQX			200			220	ns
Chip Deselect Time	TSXQZ			200			220	ns
Output Disable Time	TEHQZ			200			220	ns
$\bar{E}$ Pulse Width (Pos)	TEHEL	300			330			ns
$\bar{E}$ Pulse Width (Neg)	TELEH	550			625			ns
Address Setup Time	TAVEL	10			10			ns
Address Hold Time	TELAX	110			120			ns
Latched Chip Select Enable Time	TELQX			0			0	ns

READ CYCLE TIMING • Latched Chip Selects


Ē
TELEH
TAVEL
TELAX
A_0-A_{10},S_1,S_2
VALID
TELQV
TELQX
Q_0-Q_7
VALID
TIME REF
-1
0
1
TEHEL
VALID
VALID
2
3
4
5
TEHEL
VALID
TEHQZ
VALID
2
3
4
5

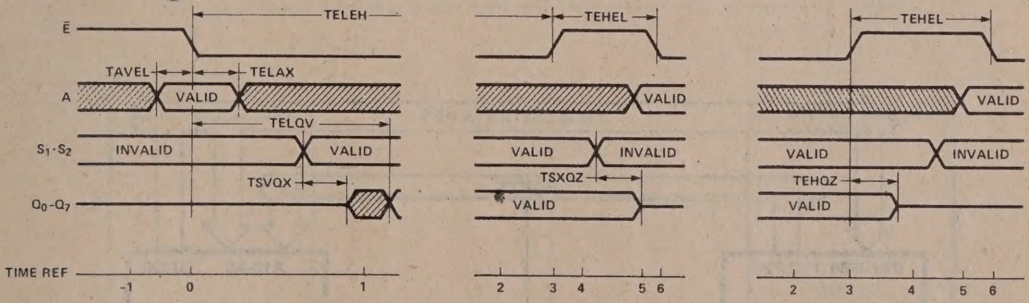
LATCHED OUTPUTS

UNLATCHED OUTPUTS

FUNCTION TABLE • Latched Chip Selects

TIME REF	INPUTS			Q OUTPUTS		NOTES
	E	A	$S_1 \bullet S_2$	LATCHED	UNLATCHED	
−1	H	X	V	V	Z	LATCHED DATA VALID FROM PREVIOUS CYCLE
0	↓	V	V	Z	Z	STROBE LATCHES VALID ADDRESS, CHIP SELECT INFORMATION
1	L	X	X	ACTIVE	ACTIVE	OUTPUTS ENABLED AND ACTIVE
2	L	X	X	V	V	OUTPUTS VALID
3	↑	X	X	V	V	STROBE RETURNS HIGH, LATCHES OUTPUT
4	H	X	X	V	Z	OUTPUTS DISABLED ON UNLATCHED DEVICES
5	↓	V	V	V	Z	NEXT CYCLE BEGINS, SAME AS 0.

READ CYCLE TIMING • Unlatched Chip Selects


Ē
TELEH
TAVEL
TELAX
A
VALID
TELQV
S_1·S_2
INVALID
VALID
TSVQX
Q_0-Q_7
TIME REF
-1
0
1
TEHEL
VALID
VALID
INVALID
TSXQZ
VALID
2
3
4
5
6
TEHEL
VALID
VALID
INVALID
TEHQZ
VALID
2
3
4
5
6

LATCHED OUTPUTS

UNLATCHED OUTPUTS

FUNCTION TABLE • Unlatched Chip Selects

TIME REF	INPUTS			Q OUTPUTS		NOTES
	E	A	$S_1 \bullet S_2$	LATCHED	UNLATCHED	
−1	H	X	$\overline{V}$	Z	Z	MEMORY INACTIVE, OUTPUTS HIGH Z
0	↓	V	$\overline{V}$	Z	Z	STROBE LATCHES ADDRESS INFORMATION
1	L	X	V	ACTIVE	ACTIVE	OUTPUTS ENABLED AND ACTIVE
2	L	X	V	V	V	OUTPUTS VALID
3	↑	X	V	V	V	STROBE RETURNS HIGH, LATCHES OUTPUTS
4	H	X	V	V	Z	OUTPUTS DISABLED ON UNLATCHED DEVICES
5	H	X	$\overline{V}$	Z	Z	OUTPUTS DISABLED ON LATCHED DEVICES
6	↓	V	$\overline{V}$	Z	Z	NEXT CYCLE BEGINS, SAME AS 0.

NOTES

1. X = Don't Care 2. V = Valid 3. Z = High Impedance 4. $\overline{V}$ = Invalid.

APPLICATIONS

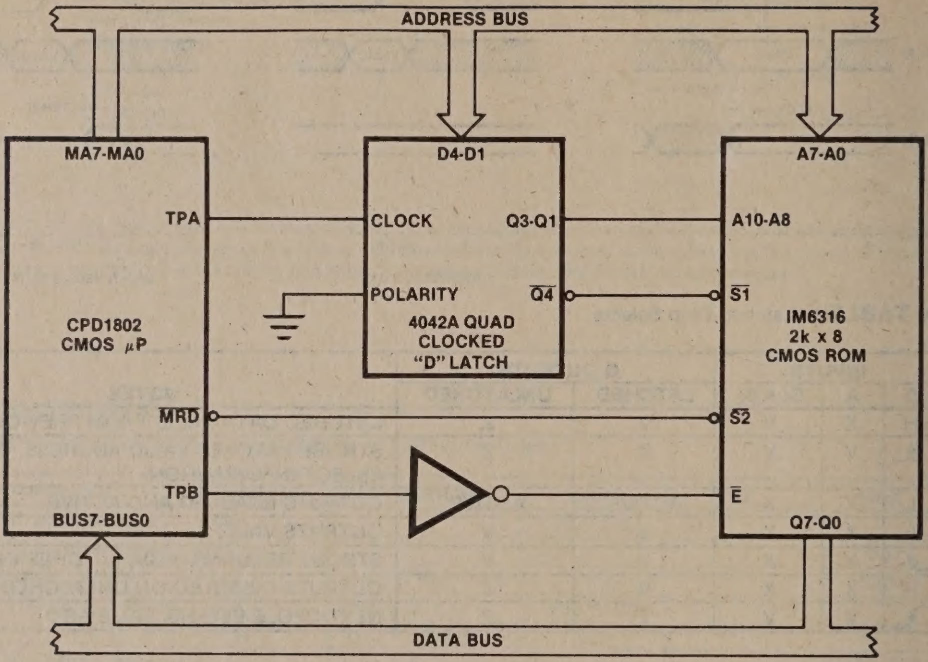

ADDRESS BUS
MA7-MA0
D4-D1
A7-A0
TPA
CLOCK
Q3-Q1
A10-A8
POLARITY
$\overline{Q4}$
$\overline{S1}$
CPD1802
CMOS μP
4042A QUAD
CLOCKED
"D" LATCH
IM6316
2k x 8
CMOS ROM
MRD
$\overline{S2}$
TPB
$\overline{E}$
BUS7-BUS0
Q7-Q0
DATA BUS

FIG. 1. 2K x 8 CMOS ROM MEMORY FOR CPD1802 CMOS MICROPROCESSOR

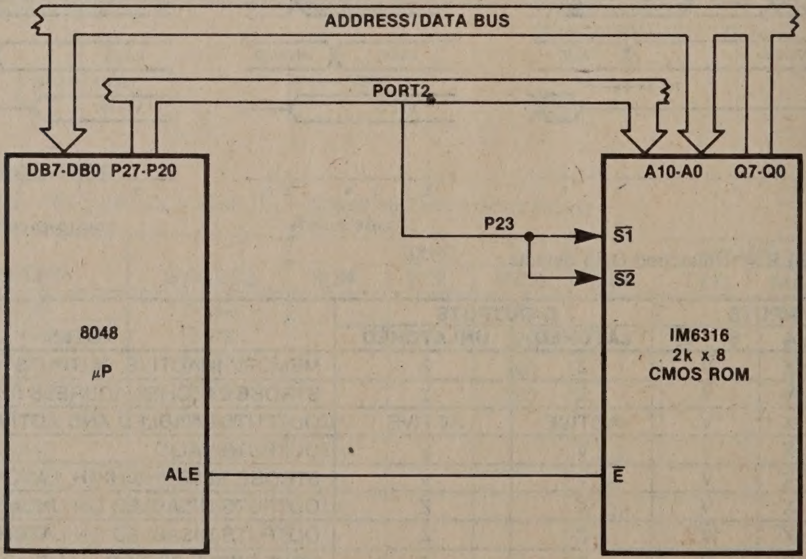

ADDRESS/DATA BUS
PORT2
DB7-DB0 P27-P20
A10-A0
Q7-Q0
P23
$\overline{S1}$
$\overline{S2}$
8048
μP
IM6316
2k x 8
CMOS ROM
ALE
$\overline{E}$

FIG. 2. 2 k x 8 CMOS ROM MEMORY FOR 8048 or 8035 MICROCOMPUTERS

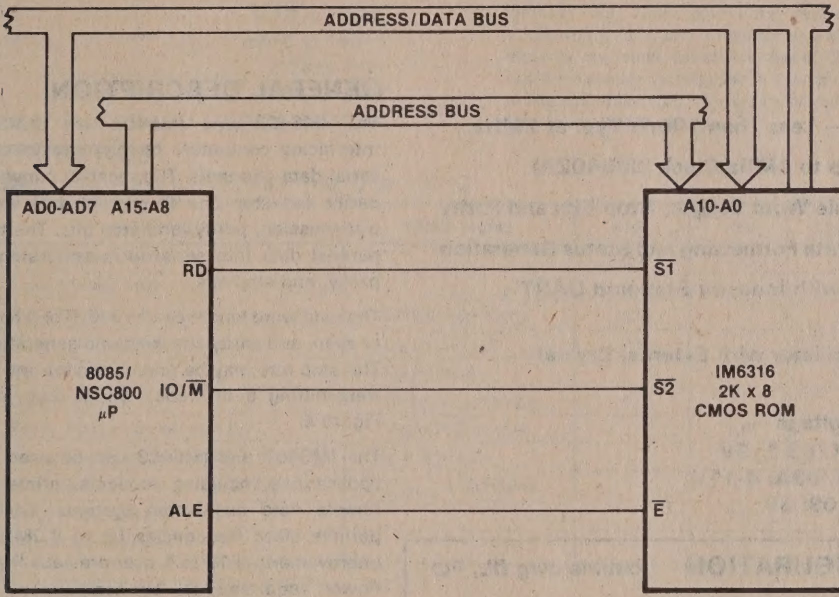

ADDRESS/DATA BUS
ADDRESS BUS
AD0-AD7
A15-A8
RD
8085/
NSC800
μP
IO/M
ALE
A10-A0
S1
S2
IM6316
2K x 8
CMOS ROM
E

FIG. 3. 2 k x 8 CMOS ROM MEMORY FOR 8085/NSC 800 MICROPROCESSORS

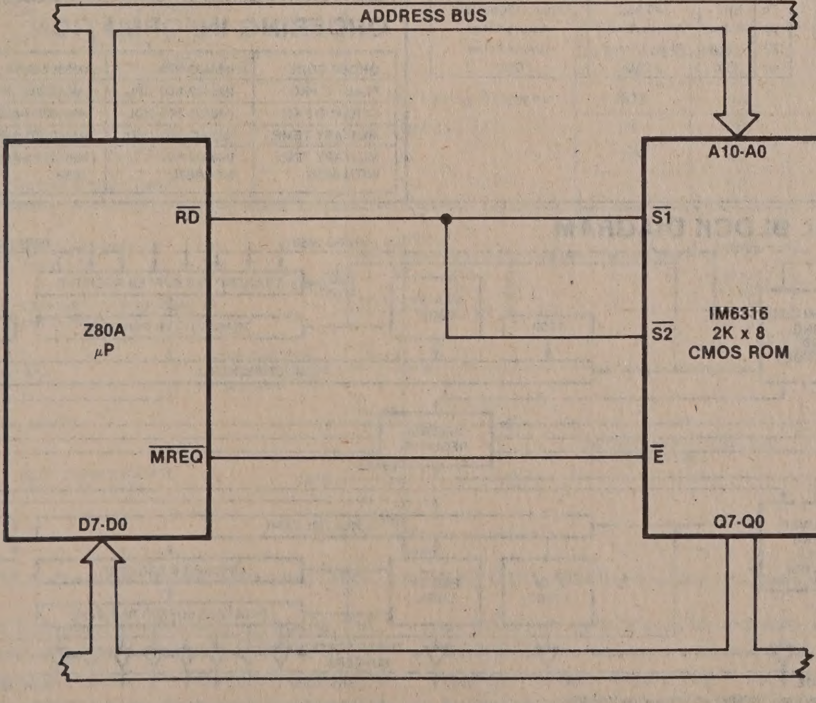

ADDRESS BUS
A10-A0
RD
S1
S2
Z80A
μP
IM6316
2K x 8
CMOS ROM
MREQ
E
D7-D0
Q7-Q0

FIG. 4. 2 k x 8 CMOS ROM MEMORY FOR Z80A MICROPROCESSOR DATA BUS

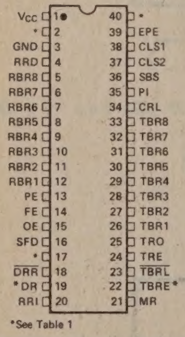
INTERSIL

IM6402/IM6403 Universal Asynchronous Receiver Transmitter (UART)

FEATURES

- Low Power — Less Than 10mW Typ. at 2MHz
- Operation Up to 4MHz Clock (IM6402A)
- Programmable Word Length, Stop Bits and Parity
- Automatic Data Formatting and Status Generation
- Compatible with Industry Standard UART's (IM6402)
- On-Chip Oscillator with External Crystal (IM6403)
- Operating Voltage —
  IM6402-1/03-1: 5V
  IM6402A/03A: 4-11V
  IM6402/03: 5V

PIN CONFIGURATION (outline dwg DL, PL)



Vcc 1
* 2
GND 3
RRD 4
RBR8 5
RBR7 6
RBR6 7
RBR5 8
RBR4 9
RBR3 10
RBR2 11
RBR1 12
PE 13
FE 14
OE 15
SFD 16
* 17
$\overline{\text{DRR}}$ 18
*DR 19
RRI 20
40 *
39 EPE
38 CLS1
37 CLS2
36 SBS
35 PI
34 CRL
33 TBR8
32 TBR7
31 TBR6
30 TBR5
29 TBR4
28 TBR3
27 TBR2
26 TBR1
25 TRO
24 TRE
23 $\overline{\text{TBRL}}$
22 TBRE*
21 MR

*See Table 1

TABLE 1

PIN	IM6402	IM6403 w/XTAL	IM6403 w/EXT CLOCK
2	N/C	Divide Control	Divide Control
17	RRC	XTAL	External Clock Input
19	Tri-State	Always Active	Always Active
22	Tri-State	Always Active	Always Active
40	TRC	XTAL	GND

GENERAL DESCRIPTION

The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even, and parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 6.

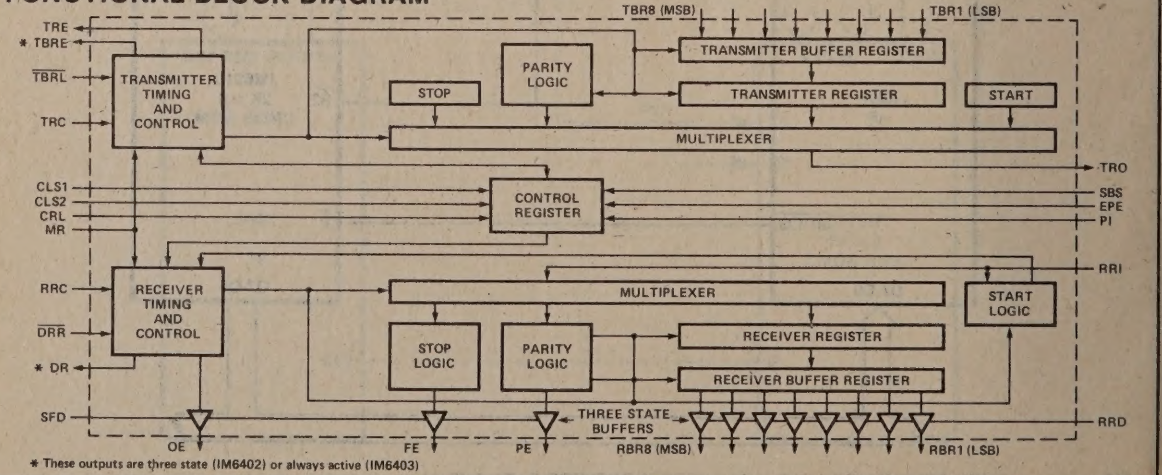
The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits clock frequencies up to 4.0MHz (250K Baud), an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 670mW to 10mW. Status logic increases flexibility and simplifies the user interface.

The IM6402 differs from the IM6403 in the use of five device pins as indicated in Table 1 and Figure 1.

ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402/03
PLASTIC PKG	IM6402-1/03-1IPL	IM6402/03-AIPL	IM6402/03-IPL
CERAMIC PKG	IM6402-1/03-1IDL	IM6402/03-AIDL	IM6402/03IDL
MILITARY TEMP.	IM6402-1/03-1MDL	IM6402/03-AMDL	—
MILITARY TEMP. WITH 883B	IM6402-1/03-1 MDL/883B	IM6402/03-AMDL/ 883B	—

FUNCTIONAL BLOCK DIAGRAM



TRE
* TBRE
$\overline{\text{TBRL}}$
TRC
TRANSMITTER TIMING AND CONTROL
TBR8 (MSB)
TBR1 (LSB)
PARITY LOGIC
TRANSMITTER BUFFER REGISTER
STOP
TRANSMITTER REGISTER
START
MULTIPLEXER
TRO
CLS1
CLS2
CRL
MR
CONTROL REGISTER
SBS
EPE
PI
RRI
RRC
RECEIVER TIMING AND CONTROL
MULTIPLEXER
START LOGIC
$\overline{\text{DRR}}$
STOP LOGIC
PARITY LOGIC
RECEIVER REGISTER
* DR
RECEIVER BUFFER REGISTER
SFD
THREE STATE BUFFERS
RRD
OE
FE
PE
RBR8 (MSB)
RBR1 (LSB)

* These outputs are three state (IM6402) or always active (IM6403)

IM6402/IM6403

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
IM6402/03	-40°C to +85°C
Storage Temperature	-65°C to 150°C
Operating Voltage	4.0V to 7.0V
Supply Voltage	+8.0V
Voltage On Any Input or Output Pin	-0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5.0 \pm 10\%$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	$GND \leq V_{IN} \leq V_{CC}$	-5.0		5.0	μA
4	V_{OH}	Output Voltage High	$I_{OH} = -0.2mA$	2.4			V
5	V_{OL}	Output Voltage Low	$I_{OL} = 1.6mA$			0.45	V
6	I_{OLK}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-5.0		5.0	μA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	800	μA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_c = 500 KHz			1.2	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{crystal}$ = 2.46MHz			3.7	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

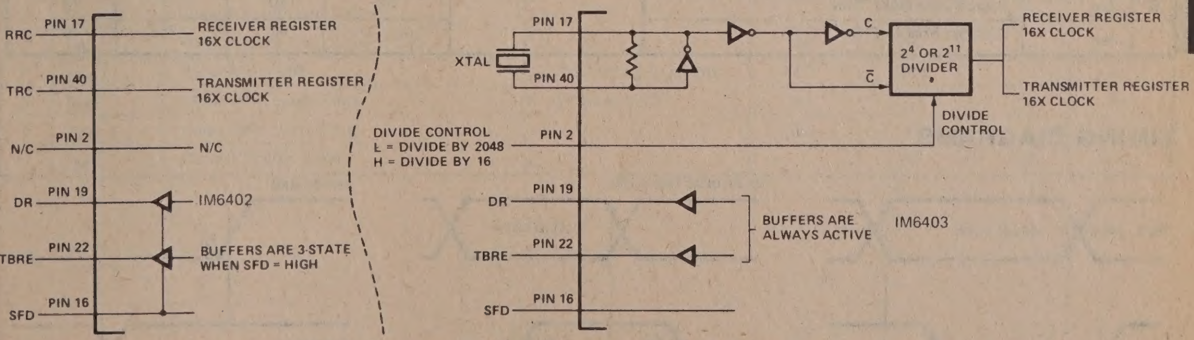
NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).

NOTE 2: $V_{CC} = 5V$, $T_A = 25°C$.

A.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5.0V \pm 10\%$, $C_L = 50pF$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	f_c	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.		1.0	MHz
2	$f_{crystal}$	Crystal Frequency IM6403				2.46	MHz
3	t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		225	50		ns
4	t_{mr}	Pulse Width MR		600	200		ns
5	t_{ds}	Input Data Setup Time		75	20		ns
6	t_{dh}	Input Data Hold Time		90	40		ns
7	t_{en}	Output Enable Time			80	190	ns



RRC
PIN 17
RECEIVER REGISTER 16X CLOCK
TRC
PIN 40
TRANSMITTER REGISTER 16X CLOCK
N/C
PIN 2
N/C
DR
PIN 19
IM6402
TBRE
PIN 22
BUFFERS ARE 3-STATE WHEN SFD = HIGH
SFD
PIN 16
DIVIDE CONTROL
L = DIVIDE BY 2048
H = DIVIDE BY 16
PIN 17
XTAL
PIN 40
C
$\bar{C}$
2^4 OR 2^{11} DIVIDER
RECEIVER REGISTER 16X CLOCK
TRANSMITTER REGISTER 16X CLOCK
DIVIDE CONTROL
PIN 2
DR
PIN 19
BUFFERS ARE ALWAYS ACTIVE
IM6403
TBRE
PIN 22
SFD
PIN 16

FIGURE 1. Functional Difference Between IM6402 and IM6403 UART (6403 has On-Chip 4/11 Stage Divider)

The IM6403 differs from the IM6402 on three Inputs (RRC, TRC, pin 2) as shown in Figure 1. Two outputs (TBRE, DR) are not three-state as on the IM6402, but are always active. The on-chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface (Figure 10). A 9600 baud interface may be implemented using a 2.4576MHz crystal with the divider set to divide by 16.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
Industrial IM6402AI/03AI	-40°C to +85°C
Military IM6402AM/03AM	-55°C to +125°C
Storage Temperature	-65°C to 150°C
Operating Voltage	4.0V to 11.0V
Supply Voltage	+12.0V
Voltage On Any Input or Output Pin	-0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4.0V to 11.0V, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		5.0	500	μA
8	I_{CC}	Power Supply Current IM6402A Dynamic	f_c = 4MHz			9.0	mA
9	I_{CC}	Power Supply Current IM6403A Dynamic	$f_{crystal}$ = 3.58MHz			13.0	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10.0V ± 5%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	f_c	Clock Frequency IM6402A	See Timing Diagrams (Figures 2,3,4)	D.C.		4.0	MHz
2	$f_{crystal}$	Crystal Frequency IM6403A				6.0	MHz
3	t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		100	40		ns
4	t_{mr}	Pulse Width MR		400	200		ns
5	t_{ds}	Input Data Setup Time		40	0		ns
6	t_{dh}	Input Data Hold Time		30	30		ns
7	t_{en}	Output Enable Time			40	70	ns

TIMING DIAGRAMS

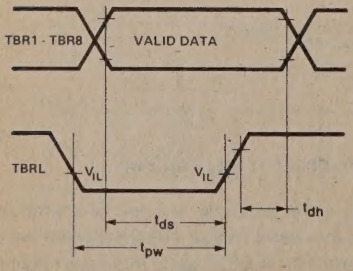


FIGURE 2. Data Input Cycle

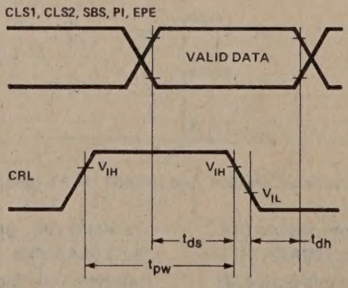


FIGURE 3. Control Register Load Cycle

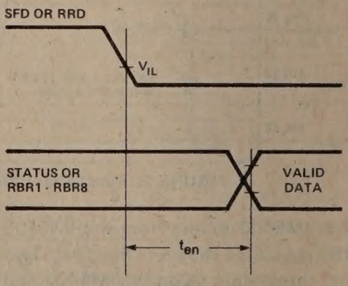


FIGURE 4. Status Flag Enable Time or Data Output Enable Time

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
  Industrial IM6402-1I/03-1I .... -40°C to +85°C
  Military IM6402-1M/03-1M .... -55°C to +125°C
Storage Temperature .... -65°C to +150°C
Operating Voltage .... 4.0V to 7.0V
Supply Voltage .... +8.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5.0 \pm 10\%$, T_A = Industrial or Military

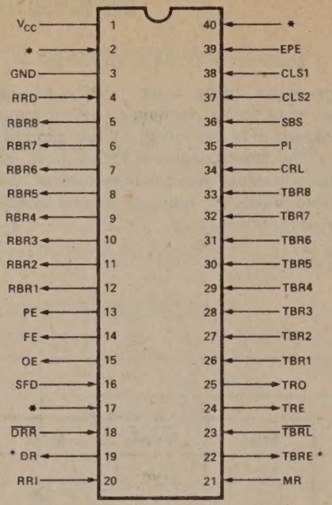
	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	$GND \leq V_{IN} \leq V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH}=-0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OLK}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	100	μA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_c = 2MHz			1.9	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{crystal}$ = 3.58MHz			5.5	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5.0V \pm 10\%$, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	f_c	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.		2.0	MHz
2	$f_{crystal}$	Crystal Frequency IM6403				3.58	MHz
3	t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		150	50		ns
4	t_{mr}	Pulse Width MR		400	200		ns
5	t_{ds}	Input Data Setup Time		50	20		ns
6	t_{dh}	Input Data Hold Time		60	40		ns
7	t_{en}	Output Enable Time			80	160	ns



*DIFFERS BETWEEN IM6402 AND IM6403.

FIGURE 5. Pin Configuration

IM6403 FUNCTIONAL PIN DEFINITION

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Positive Power Supply
2	IM6402-N/C IM6403-Control	No Connection Divide Control High: 2^4 (16) Divider Low: 2^{11} (2048) Divider
3	GND	Ground
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 — RBR8
7	RBR6	See Pin 5 — RBR8
8	RBR5	See Pin 5 — RBR8
9	RBR4	See Pin 5 — RBR8
10	RBR3	See Pin 5 — RBR8
11	RBR2	See Pin 5 — RBR8
12	RBR1	See Pin 5 — RBR8
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.

IM6403 FUNCTIONAL PIN DEFINITION
(Continued)

PIN	SYMBOL	DESCRIPTION
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if $\overline{DRR}$ has been performed (i.e., $\overline{DRR}$: active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR,* TBRE* to a high impedance state. See Block Diagram and Figure 4. *IM6402 only.
17	IM6402-RRC IM6403-XTAL or EXT CLK IN	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register, and is required after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end. See Figure 2.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.

IM6403 FUNCTIONAL PIN DEFINITION
(Continued)

PIN	SYMBOL	DESCRIPTION
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 — TBR1
28	TBR3	See Pin 26 — TBR1
29	TBR4	See Pin 26 — TBR1
30	TBR5	See Pin 26 — TBR1
31	TBR6	See Pin 26 — TBR1
32	TBR7	See Pin 26 — TBR1
33	TBR8	See Pin 26 — TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register. See Figure 3.

IM6403 FUNCTIONAL PIN DEFINITION
(Continued)

PIN	SYMBOL	DESCRIPTION
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits) (CLS1 high CLS2 low 6-bits) (CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits)
38	CLS1*	See Pin 37 — CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-XTAL or GND	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table 2 (Control Word Function)

TABLE 2. Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form (Figure 6) on the TROutput terminal.

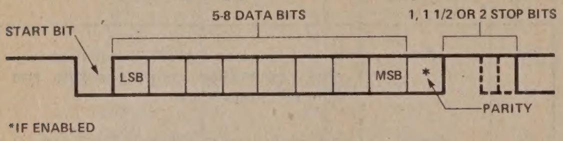


FIGURE 6. Serial Data Format

Transmitter timing is shown in Figure 7. Ⓐ Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{\text{TBRL}}$oad input. Valid data must be present at least t_{DS} prior to and t_{DH} following the rising edge of $\overline{\text{TBRL}}$. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. Ⓑ The rising edge of $\overline{\text{TBRL}}$ clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register, TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high. Output data is clocked by TRClock, which is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins.

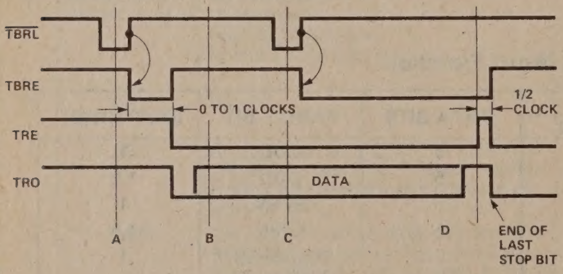


FIGURE 7. Transmitter Timing (Not to Scale)

RECEIVER OPERATION

Data is received in serial form at the RI input. When no data is being received, RI input must remain high. The data is clocked by the RRClock, which is 16 times the data rate. Receiver timing is shown in Figure 8.

Ⓐ A low level on $\overline{\text{DRR}}$eset clears the DReady line. Ⓑ During the first stop bit, data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates an overrun which occurs when DReady has not been cleared before the present character was transferred to the RBRegister. A logic high on PError indicates a parity error. Ⓒ 1/2 clock cycle later, DReady is set to a logic high and FError is evaluated. A logic high on FError indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a stop bit is received.

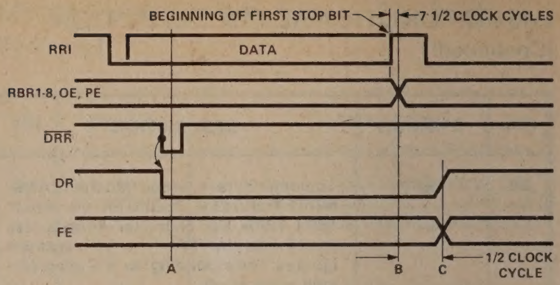


FIGURE 8. Receiver Timing (Not to Scale)

START BIT DETECTION

The receiver uses a 16X clock for timing (see Figure 9.) The start bit Ⓐ could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at the center of the first stop bit.

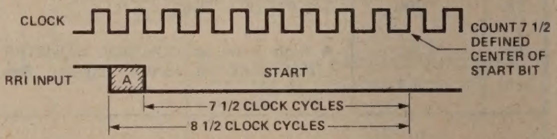


FIGURE 9. Start Bit Timing

TYPICAL APPLICATION

Microprocessor systems, which are inherently parallel in nature, often require an asynchronous serial interface. This function can be performed easily with the IM6402/03 UART. Figure 10 shows how the IM6403 can be interfaced to an IM6100 microcomputer system with the aid of an IM6101 Programmable Interface Element (PIE). The PIE interprets Input/Output transfer (IOT) instructions from the processor and generates read and write pulses to the UART. The SENSE lines on the PIE are also employed to allow the processor to detect UART status. In particular, the processor must know when the Receive Buffer Register has accumulated a character (DR active), and when the Transmit Buffer Register can accept another character to be transmitted.

In this example the characters to be received or transmitted will be eight bits long (CLS 1 and 2: both HIGH) and transmitted with no parity (PI:HIGH) and two stop bits (SBS:HIGH). Since these control bits will not be changed during operation, Control Register Load (CRL) can be tied high. Remember, since the IM6402/03 is a CMOS device, all unused inputs should be committed.

The baud rate at which the transmitter and receiver will operate is determined by the external crystal and DIVIDE CONTROL pin on the IM6403. The internal divider can be set to reduce the crystal frequency by either 16 (PIN 2:HIGH) or 2048 (PIN 2:LOW) times. The frequency out of the internal divider should be 16 times the desired baud rate. To generate 110 baud, this example will use a 3.579545MHz color TV crystal and DIVIDE CONTROL set low. The IM6402 may use different receive (RRC) and transmit (TRC) clock rates, but requires an external clock generator.

To ensure consistent and correct operation, the IM6402/03 must be reset after power-up. The Master Reset (MR) pin is active high, and can be driven reliably from a Schmitt trigger inverter and R-C delay. In this example, the IM6100 is reset through still another inverter. The Schmitt trigger between the processor and R-C network is needed to assure that a slow rising capacitor voltage does not re-trigger RESET. A long reset pulse after power-up (~100ms) is required by the processor to assure that the on-board crystal oscillator has sufficient time to start.

The IM6402 supports the processor's bi-directional data bus quite easily by tying the TBR and RBR buses together. A read command from the processor will enable the RECEIVER BUFFER REGISTER onto the bus by using the RECEIVER REGISTER DISABLE (RRD) pin. A write command from the processor clocks data from the bus into the TRANSMITTER BUFFER REGISTER using $\overline{TBRL}$. Figure 10 shows a NAND gate driving $\overline{TBRL}$ from the $\overline{WRITE_2}$ pin on the PIE. This gate is used to generate a rising edge to $\overline{TBRL}$ at the point where data is stable on the bus, and to hold $\overline{TBRL}$ high until the UART actually transfers the data to it's internal buffer. If $\overline{TBRL}$ were allowed to return low before TBRE went high, the intended output data would be overwritten, since the TBR is a transparent latch.

Although not shown in this example, the error flags (PE, FE, OE) could be read by the processor, using the other READ line from the PIE. Since an IM6403 is used, TBRE and DR are not affected by the STATUS FLAGS DISABLE pin, thus, the three error flags can be tied to the data bus and gated by connecting SFD to $\overline{READ_2}$.

If parity is not inhibited, a parity error will cause the PE pin to go high until the next valid character is received.

A framing error is generated when an expected stop bit is not received. FE will stay high after the error until the next complete character's stop bit is received.

The overrun error flag is set if a received character is transferred to the RECEIVER BUFFER REGISTER when the previous character has not been read. The OE pin will stay high until the next received stop bit after a $\overline{DRR}$ is performed.

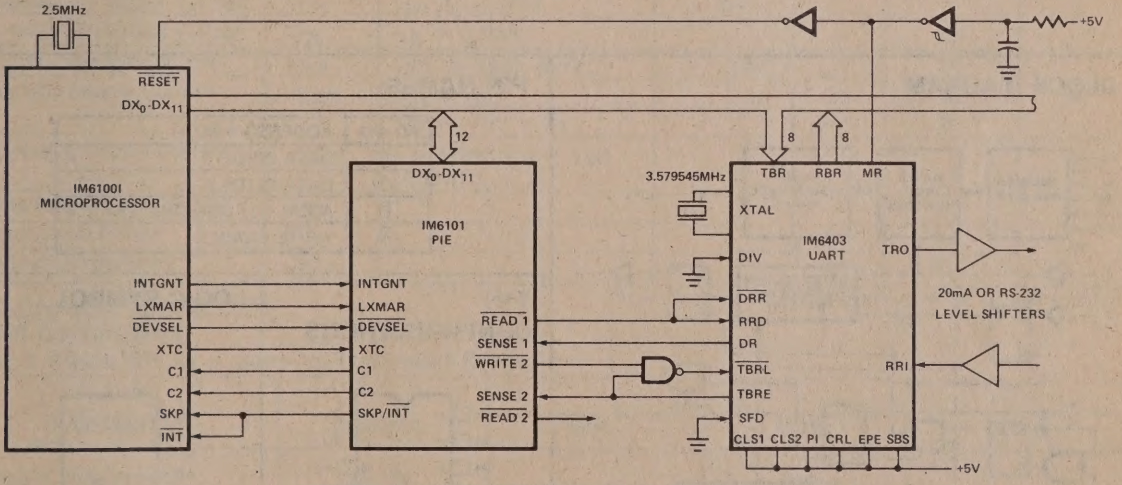

2.5MHz
RESET
DX0-DX11
IM6100I MICROPROCESSOR
INTGNT
LXMAR
DEVSEL
XTC
C1
C2
SKP
INT
12
DX0-DX11
IM6101 PIE
INTGNT
LXMAR
DEVSEL
XTC
C1
C2
SKP/INT
READ 1
SENSE 1
WRITE 2
SENSE 2
READ 2
8
8
+5V
3.579545MHz
TBR
RBR
MR
XTAL
DIV
IM6403 UART
DRR
RRD
DR
TBRL
TBRE
SFD
TRO
RRI
CLS1 CLS2 PI CRL EPE SBS
+5V
20mA OR RS-232 LEVEL SHIFTERS

FIGURE 10. 110 Baud Serial Interface for IM6100 System

INTERSIL

ADVANCE INFORMATION
Specifications Subject To Change Without Notice

IM6504
4096 Bit (4096 x 1) CMOS Static RAM

FEATURES

- **Low Standby Power—275 μW maximum**
- **Low Operating Power—38.5 mW/MHz maximum**
- **High Speed—300 ns Maximum Access Time**
- **TTL Compatible Inputs and Outputs**
- **Three State Outputs**
- **Data Retention to V_{CC} = 2V**
- **On-Chip Address Register**
- **Military and Industrial Temperature Ranges**
- **Harris 6504/Mostek 4104 Compatible**

GENERAL DESCRIPTION

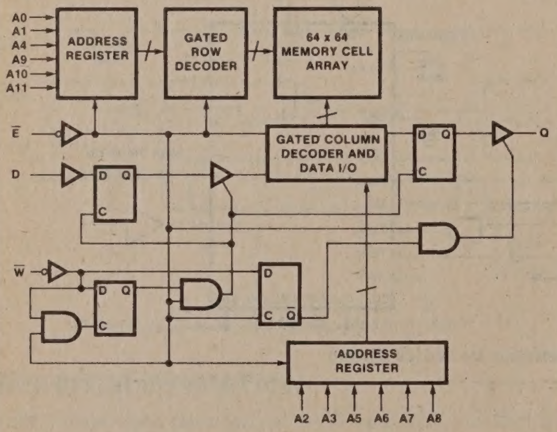
The IM6504 is a high speed, low power CMOS Static RAM organized 4096 words by 1 bit. Input and three state outputs are TTL compatible and allow for direct interface with common system bus structures. An on-chip address register simplifies system interfacing requirements.

This device is fully compatible with the Harris HM6504, but is fabricated with Intersil's selective oxidation, ion-planted, self aligned silicon gate CMOS process, called SELOX C, to achieve higher reliability and performance.

The standard part operates from 4.5 to 5.5 volts with an access time of 300ns and standby supply current of 50μA guaranteed over operating temperature range.

Minimum standby current is drawn when chip select line Ē is held at either V_{CC} or GND. Data rentention is guaranteed to a V_{CC} of 2.0V.

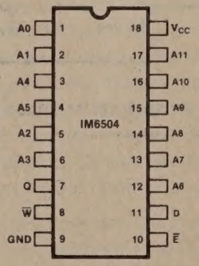
BLOCK DIAGRAM


A0
A1
A4
A9
A10
A11
ADDRESS REGISTER
GATED ROW DECODER
64 x 64 MEMORY CELL ARRAY
Ē
D
GATED COLUMN DECODER AND DATA I/O
D Q
C
Q
W̄
C Q̄
ADDRESS REGISTER
A2 A3 A5 A6 A7 A8

PIN NAMES

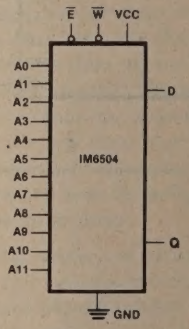
A0-A11	ADDRESS INPUTS
D	DATA INPUT
Q	DATA OUTPUT
Ē	ADDR. STROBE/CHIP ENABLE
W̄	WRITE ENABLE

PIN CONFIGURATIONS


A0 1
A1 2
A4 3
A5 4
A2 5
A3 6
Q 7
W̄ 8
GND 9
18 Vcc
17 A11
16 A10
15 A9
14 A8
13 A7
12 A6
11 D
10 Ē
IM6504

(outline dwg JN)

LOGIC SYMBOL


Ē
W̄
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
IM6504
D
Q
GND

ORDERING INFORMATION

PART NO.	PACKAGE	TEMP. RANGE
IM6504 IJN	18 PIN CERDIP	−40°C to +85°C
IM6504 MJN	18 PIN CERDIP	−55°C to +125°C
IM6504 CJN	18 PIN CERDIP	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V_{CC}) .... +8V
Input or Output Voltage Applied .... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range .... −65° to +150°C
Operating Range
Temperature
Industrial .... −40°C to +85°C
Military .... −55°C to +125°C
Voltage
6504I,M 4.5-5.5V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS:

V_{CC} = 5.0V ± 10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0		V_{CC} +0.3	V
Logical "0" Input Voltage	V_{IL}		−0.3		0.8	
Input Leakage Current	I_{ILK}	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = −1.0mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 2.0mA			0.4	
Output Leakage Current	I_{OLK}	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}		0.1	50	
		V_{CC} = 3.0V = $\overline{E}_1$		0.01	25	
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_0 = 0		5.0	7.0	mA
Data Retention Voltage	V_{DR}				2.0	V
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_{OUT}			6.0	10.0	

Note: Capacitance values guaranteed but not 100% tested.

AC CHARACTERISTICS①

TEST CONDITIONS:

V_{CC} = 5.0V ± 10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNIT
Access Time From Ē	TELQV		300	ns
Output Disable From Ē	TEHQZ		100	
Ē Pulse Width (Pos)	TEHEL	120		
Ē Pulse Width (Neg)	TELEH	300		
Address Setup	TAVEL	20		
Address Hold	TELAX	50		
Write Enable Pulse Width	TWLWH	80		
Data Setup	TDVWL	0		
Data Hold	TWLDX	80		
Write Enable Read Setup	TWHEL	0		
Write Enable Pulse Setup	TWLEH	200		
Early Write Pulse Setup	TWLEL	0		
Early Write Pulse Hold	TELWH	80		
Early Write Data Setup	TDVEL	0		
Early Write Data Hold	TELDX	80		
Data Valid to Write	TQVWL	0		
Read or Write Cycle Time	TELEL	420		

1.) AC Test Conditions: Input rise and fall times are 20 ns; Output load is 1 TTL load and 50 pf. All timing measurements are taken at ½ V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V_{CC}) .... +8V
Input or Output Voltage Applied .... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range .... −65° to +150°C
Operating Range
  Temperature .... 0°C to +70°C
  Voltage .... 4.75V to 5.25V

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS:

V_{CC} = 5.0V ± 5%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logical "1" Input Voltage	V_{IH}		$V_{CC}-2.0$		$V_{CC}+0.3$	V
Logical "0" Input Voltage	V_{IL}		−0.3		0.8	
Input Leakage Current	I_{IL}	GND ≤ V_{IN} ≤ V_{CC}	−10.0		+10.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = −0.4mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 1.6mA			0.4	
Output Leakage Current	I_{OLK}	GND ≤ V_{IN} ≤ V_{CC}	−10.0		+10.0	μA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}		100	500	
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_0 = 0		5.0	7.0	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_{OUT}			6.0	10.0	

Note: Capacitance values guaranteed but not 100% tested.

AC CHARACTERISTICS①

TEST CONDITIONS:

V_{CC} = 5.0V ± 5%, T_A = Operating Temperature Range

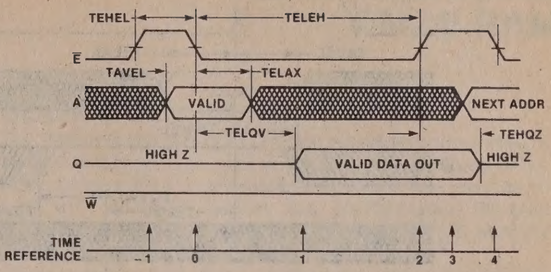
PARAMETER	SYMBOL	LIMITS		UNIT
		MIN.	MAX.	
Access Time From $\bar{E}$	TELQV		350	ns
Output Disable From $\bar{E}$	TEHQZ		100	
$\bar{E}$ Pulse Width (Pos)	TEHEL	150		
$\bar{E}$ Pulse Width (Neg)	TELEH	350		
Address Setup	TAVEL	20		
Address Hold	TELAX	50		
Write Enable Pulse Width	TWLWH	100		
Data Setup	TDVWL	30		
Data Hold	TWLDX	100		
Write Enable Read Setup	TWHEL	0		
Write Enable Pulse Setup	TWLEH	250		
Early Write Pulse Setup	TWLEL	0		
Early Write Pulse Hold	TELWH	100		
Early Write Data Setup	TDVEL	30		
Early Write Data Hold	TELDX	100		
Data Valid to Write	TQVWL	0		
Read or Write Cycle Time	TELEL	500		

1.) AC Test Conditions: Input rise and fall times are 20 ns; Output load is 1 TTL load and 50 pF. All timing measurements are taken at ½ V_{CC}.

READ CYCLE

The falling edge of chip enable ($\overline{E}$) latches addresses in the on-chip register and initiates a read cycle (T = 0). Addresses to be latched must be present one setup time (TAVEL) prior to and one hold time (TELAX) following the falling edge of $\overline{E}$. During time T = 1 the outputs become valid from the high Z state. There is no period of active, but invalid, data on the bus. Write enable ($\overline{W}$) must remain high until after time T = 2. The read cycle is terminated when $\overline{E}$ goes high, disabling the output buffers.

TIMING


TEHEL
TELEH
$\overline{E}$
TAVEL
TELAX
A
VALID
NEXT ADDR
TELQV
TEHQZ
HIGH Z
Q
VALID DATA OUT
HIGH Z
$\overline{W}$
TIME REFERENCE
−1
0
1
2
3
4

FUNCTION TABLE • READ

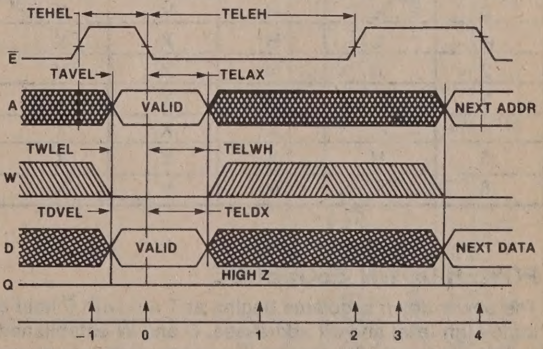
TIME REF	INPUTS			OUTPUT	NOTES
	$\overline{E}$	$\overline{W}$	A	Q	
−1	H	X	X	Z	MEMORY INACTIVE
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	H	X	V	OUTPUT VALID
2	↗	H	X	V	READ COMPLETE
3	H	X	X	V	MEMORY INACTIVE (SAME AS −1)
4	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAMES AS 0)

EARLY WRITE CYCLE

The falling edge of $\overline{E}$ latches addresses in the on-chip register and initiates an early write cycle. Address, $\overline{W}$ and D inputs must be present for the appropriate setup and hold times prior to and following the falling edge of $\overline{E}$. The early write operation is complete at T = 2, after one minimum negative $\overline{E}$ pulse width (TELEH).

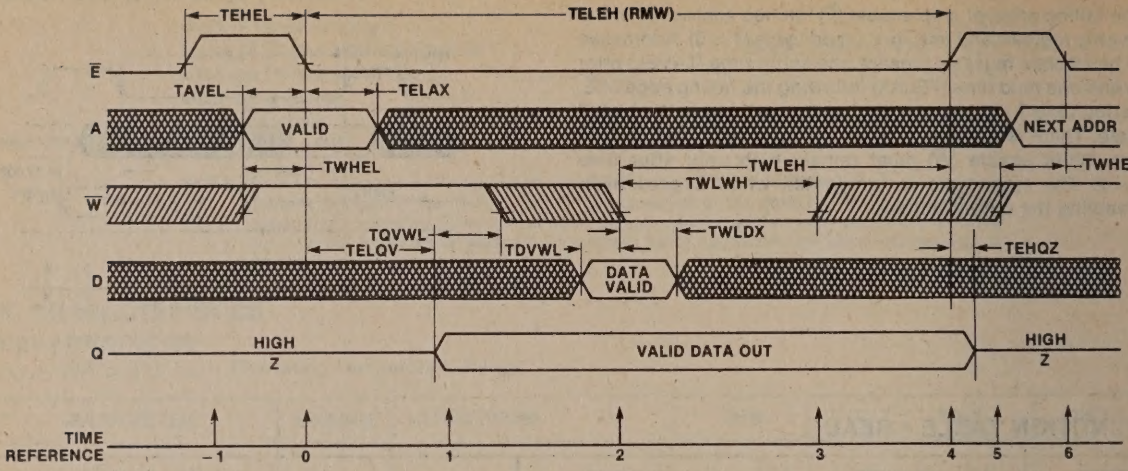
During the early write cycle, output data line Q remains in a high impedance state.

TIMING


TEHEL
TELEH
$\overline{E}$
TAVEL
TELAX
A
VALID
NEXT ADDR
TWLEL
TELWH
W
TDVEL
TELDX
D
VALID
NEXT DATA
HIGH Z
Q
−1
0
1
2
3
4

FUNCTION TABLE • EARLY WRITE

TIME REF		INPUTS				NOTES
	$\overline{E}$	$\overline{W}$	A	D	Q	
−1	H	X	X	X	Z	MEMORY INACTIVE
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS
2	↗	X	X	X	Z	WRITE COMPLETE
3	H	X	X	X	Z	CYCLE ENDS, MEMORY INACTIVE (SAME AS −1)
4	↘	L	V	V	Z	NEXT CYCLE BEGINS (SAME AS 0)


TEHEL
TELEH (RMW)
$\overline{E}$
TAVEL
TELAX
A
VALID
NEXT ADDR
TWHEL
TWLEH
TWLWH
TWHEL
$\overline{W}$
TQVWL
TELQV
TDVWL
TWLDX
TEHQZ
D
DATA VALID
Q
HIGH Z
VALID DATA OUT
HIGH Z
TIME REFERENCE
−1
0
1
2
3
4
5
6

READ — MODIFY — WRITE CYCLE

A read - modify - write cycle may be performed if the write portion of the cycle is controlled by $\overline{W}$, and $\overline{E}$ remains low throughout. Data is read normally, with $\overline{W}$ held high, address inputs latched at T = 0 and Q data out valid at T = 1. A data out valid to write time (TQVWL) must be observed before $\overline{W}$ is brought low to begin the write portion of the cycle. Input Data must be valid a setup time prior to (TDVWL) and a hold time following (TWLDX) the falling edge of $\overline{W}$. At time T = 3 $\overline{W}$ is returned high, and at T = 4 $\overline{E}$ is returned high to complete the cycle. The output Q is disabled by $\overline{E}$ and goes to a high impedance state an output disable time (TEHQZ) after $\overline{E}$ is returned high (T = 5).

FUNCTION TABLE • READY—MODIFY—WRITE

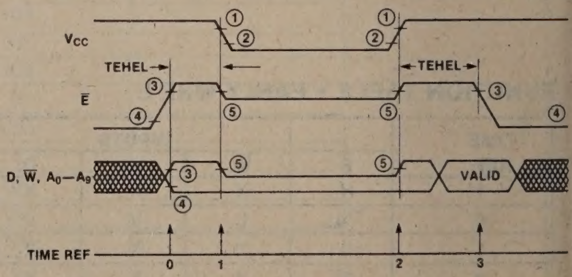
TIME REF.	INPUTS				OUTPUT	NOTES
	$\overline{E}$	$\overline{W}$	A	D	Q	
−1	H	X	X	X	Z	MEMORY INACTIVE
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	H	X	X	V	OUTPUT VALID, READ/MODIFY TIME
2	L	↘	X	V	V	WRITE BEGINS, DATA LATCHED
3	L	↗	X	X	V	WRITE IN PROGRESS
4	↗	X	X	X	V	WRITE COMPLETE
5	H	X	X	X	Z	MEMORY INACTIVE (SAME AS −1)
6	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

POWER DOWN SEQUENCE

The power down sequence begins at T = 0 with $\overline{E}$ held at a logic high level and all addresses, D and $\overline{W}$ established at valid logic levels. Chip enable $\overline{E}$ must be high one minimum positive pulse width (TEHEL) before power-down. At T = 1 power supply V_{CC} may be decreased to minimum V_{CCDR}. As V_{CC} is decreased, $\overline{E}$ must remain within data retention high logic level threshold limits (V_{IHDR}), and $\overline{W}$ and A_0-A_9, must remain within V_{IHDR} or V_{IL} limits. Failure to remain within these limits may cause data loss or SCR latch-up.

The same conditions must be met, in reverse, when returning to normal power (T = 2,3).

POWER DOWN SEQUENCE


V_{CC}
①
②
①
②
TEHEL
TEHEL
③
④
⑤
⑤
③
④
$\overline{E}$
D, $\overline{W}$, A_0—A_9
③
⑤
⑤
④
VALID
TIME REF
0
1
2
3

① 4.5V
② V_{CCDR} (5.5V ≥ V_{CCDR} ≥ 2.0V)
③ V_{IH} (V_{CC} + 0.3V ≥ V_{IH} ≥ V_{CC} − 2.0V)
④ V_{IL} (0.8 ≥ V_{IL} ≥ GND—0.3V)
⑤ V_{IHDR} (V_{CC} + 0.3V ≥ V_{IHDR} ≥ V_{CC} − 2.0V ≥ 2.0V)

IM65X08/IM65X18
1024 Bit (1024 x 1) High Speed CMOS RAM

FEATURES

- **Low Standby Power: 55μW Maximum**
- **Low Operating Power: 10mW/MHz Maximum**
- **High Speed Operation**
- **High Noise Immunity**
- **Data Retention to V_{CC} = 2.0V**
- **TTL Compatible Inputs and Outputs**
- **Three-State Outputs**
- **High Output Drive = 2 TTL Loads**
- **On-Chip Address Registers**
- **Completely Static and Synchronous**
- **Two Chip Selects (IM65X18)**
- **Military and Industrial Temperature Ranges**
- **Operating Voltage Range 4.5V to 10.5V (A Version)**

GENERAL DESCRIPTION

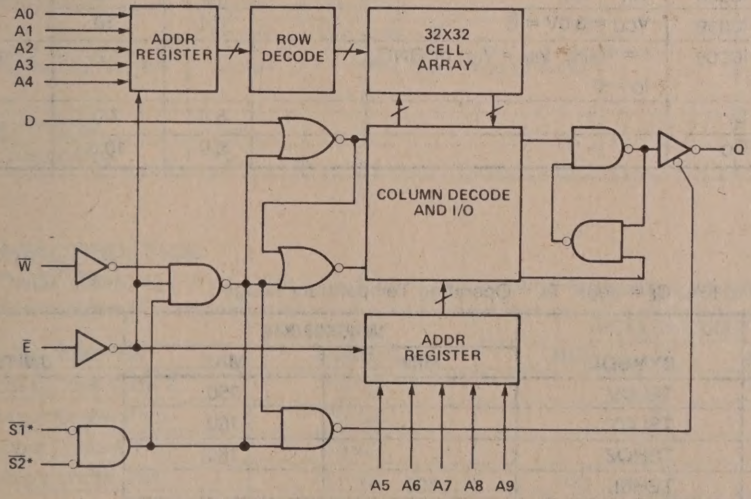
The IM65X08 and IM65X18 are high speed, low power CMOS static RAMs organized 1,024 words by 1 bit. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus architectures. On-chip address registers and two chip-selects (65X18) simplify system interfacing requirements.

These devices are fully compatible with the industry standard 6508/18 CMOS 1K x 1 RAMs but are fabricated in SELOX C, a CMOS process that uses selective oxidation to achieve higher reliability and performance.

The standard parts operate from 4.5 to 5.5 volts, with access times of 250 ns and standby supply currents of 10 μa guaranteed over operating temperature range. Access times of 180 ns are offered in "-1" versions. High operating voltage range is offered in "A" versions.

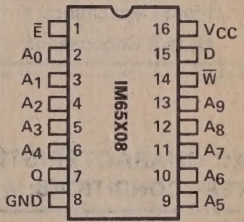
Minimum standby current is drawn when $\overline{E}$ is held at CMOS V_{CC} and all address, data and control lines are held at either CMOS V_{CC} or GND. Data retention is guaranteed to a CMOS V_{CC} of 2.0V.

BLOCK DIAGRAM (IM65X18)

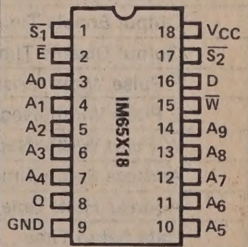

A0
A1
A2
A3
A4
ADDR REGISTER
ROW DECODE
32X32 CELL ARRAY
D
COLUMN DECODE AND I/O
Q
W̄
Ē
ADDR REGISTER
S̄1*
S̄2*
A5 A6 A7 A8 A9

*IM65X08 FUNCTIONS AS IF $\overline{E}$, $\overline{S_1}$, $\overline{S_2}$, WERE TIED TOGETHER

PIN CONFIGURATION


Ē 1
A0 2
A1 3
A2 4
A3 5
A4 6
Q 7
GND 8
16 VCC
15 D
14 W̄
13 A9
12 A8
11 A7
10 A6
9 A5
IM65X08

(outline dwg JE, PE)


S̄1 1
Ē 2
A0 3
A1 4
A2 5
A3 6
A4 7
Q 8
GND 9
18 VCC
17 S̄2
16 D
15 W̄
14 A9
13 A8
12 A7
11 A6
10 A5
IM65X18

TOP VIEW

(outline dwg JN, PN)

Flatpaks (FE, FN) have same pin outs as above

ORDERING INFORMATION

	COMMERCIAL	INDUSTRIAL				MILITARY*			
IM65X08	STD 5V	STD 5V	STD 10V	HI SPEED 5V	HI SPEED 10V	STD 5V	STD 10V	STD 10v	HI SPEED 5v
16 pin Cerdip	CJE	IJE	AIJE	– 1IJE	A-1IJE	MJE	AMJE	A-1MJE	– 1MJE
16 pin Plastic Dip	CPE	IPE	AIPE	– 1IPE	A-1IPE				
16 pin Flatpak						MFE	AMFE	A-1AMFE	– 1MFE
IM65X18 18 pin Cerdip	CJN	IJN	AIJN	– 1IJN	A-1IJN	MJN	AMJN	A-1MJN	– 1MJN
18 pin Plastic Dip	CPN	IPN	AIPN	– 1IPN	A-1IPN				
18 pin Flatpak						MFN	AMFN	A-1MFN	– 1MFN

* For 883B processing add /883B to order number.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +8.0V
Input or Output Voltage Applied .... GND –0.3V to V_{CC} +0.3V
Storage Temperature Range .... –65°C to +150°C
Operating Ranges
Temperature
Industrial .... –40°C to +85°C
Military .... –55°C to +125°C
Voltage
IM65X08/X18 .... 4.5V-5.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}–2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_I	GND ≤ V_{IN} ≤ V_{CC}	–1.0		+1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = 0	V_{CC}–0.01			V
		I_{OH} = –0.4 mA	2.4			
Logical "0" Output Voltage	V_{OL}	I_{OL} = 0			GND +0.01	
		I_{OL} = 3.2 mA			0.4	
Output Leakage	I_O		–1.0		+1.0	μA
IM65X08/X18	I_{CCSB}	V_{IN} = V_{CC}		1.0	10	
	I_{CCSB}	V_{CC} = 3.0V = $\bar{E}$		0.1	10	
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_O = 0			2	mA
Input Capacitance	C_I			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM65X08/X18		UNITS
		MIN	MAX	
Access Time From $\bar{E}$	TELQV		250	ns
Output Enable Time	TSLQX		160	
Output Disable Time	TSHQZ		160	
$\bar{E}$ Pulse Width (Pos)	TEHEL	100		
$\bar{E}$ Pulse Width (Neg)	TELEH	250		
$\overline{W}$ Pulse Width (Neg)	TWLWH	130		
Address Setup Time	TAVEL	15		
Address Hold Time	TELAX	50		
Data Setup Time	TDVEH	110		
Data Hold Time	TEHDX	0		

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +8.0V
Input or Output, Voltage Applied .... GND −0.3V to V_{CC} +.3V
Storage Temperature Range .... −65°C to +150°C
Operating Ranges
  Temperature
    Industrial .... −40°C to +85°C
    Military .... −55°C to +125°C
  Voltage
    IM65X08-1/X18-1 .... 4.5V to 5.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC} −2.0V			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{ILK}	GND ≤ V_{IN} ≤ V_{CC}	−1.0		+1.0	µA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC}−0.01			V
	V_{OH}	I_{OUT} = −0.4 mA	2.4			
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND +0.01	
	V_{OL}	I_{OUT} = 3.2 mA			0.4	
Output Leakage	I_{OLK}	GND ≤ V_O ≤ V_{CC}	−1.0		+1.0	µA
Standby Supply Current IM65X08-1/X18-1	I_{CCSB}	V_{IN} = V_{CC}		1.0	10	
	I_{CCSB}	V_{CC} = 3V = $\overline{E}$		0.01	10	
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_O = 0			2	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ±10%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM65X08-1/X18-1		UNITS
		MIN	MAX	
Access Time From $\overline{E}$	TELQV		180	ns
Output Enable Time	TSLQX		120	
Output Disable Time	TSHQZ		120	
$\overline{E}$ Pulse Width (Pos)	TEHEL	100		
$\overline{E}$ Pulse Width (Neg)	TELEH	180		
$\overline{W}$ Pulse Width (Neg)	TWLWH	100		
Address Setup Time	TAVEL	10		
Address Hold Time	TELAX	40		
Data Setup Time	TDVEH	80		
Data Hold Time	TEHDX	0		

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output, Voltage Applied	GND –0.3V to V_{CC} to .3V
Storage Temperature Range	–65°C to +150°C
Operating Ranges	
Temperature	
Industrial	–40°C to +85°C
Military	–55°C to +125°C
Voltage	
IM65X08A/X18A	4.5V to 10.5V
IM65X08A-1/X18A-1	4.5V to 10.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4.5V to 10.5V, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{ILK}	0V ≤ V_{IN} ≤ V_{CC}	–1.0		+1.0	µA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC}–0.01			V
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND +0.01	
Output Leakage	I_{OLK}	0V ≤ V_O ≤ V_{CC}	–1.0		+1.0	µA
Standby Supply Current IM65X08A-1/X18A-1	I_{CCSB}	V_{IN} = V_{CC}		5.0	500	
	I_{CCSB}	V_{CC} = 3V = $\bar{E}_1$		0.1	50	
IM65X08A/X18A	I_{CCSB}	V_{IN} = V_{CC}		5.0	500	
	I_{CCSB}	V_{CC} = 3V = $\bar{E}_1$		0.1	50	
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_O = 0			10	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pf, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM65X08A-1/X18A-1		IM65X08A/X18A		UNITS
		MIN	MAX	MIN	MAX	
Access Time From $\bar{E}$	TELQV		125		200	ns
Output Enable Time	TSLQX		75		120	
Output Disable Time	TSHQZ		75		120	
$\bar{E}$ Pulse Width (Pos)	TEHEL	85		125		
$\bar{E}$ Pulse Width (Neg)	TELEH	125		200		
$\bar{W}$ Pulse Width (Neg)	TWLWH	85		125		
Address Setup Time	TAVEL	10		15		
Address Hold Time	TELAX	40		60		
Data Setup Time	TDVEH	85		125		
Data Hold Time	TEHDX	0		0		

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 8.0V
Input or Output Voltage Applied .... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range .... −65°C to +150°C
Operating Ranges
Temperature
Commercial .... 0°C to 75°C
Voltage
IM6508C/18C 4.75V-5.25V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 5%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{ILK}	0V ≤ V_{IN} ≤ V_{CC}	−1.0		+1.0	µA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC}−0.01			V
		I_{OH} = −0.2 mA	2.4			
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND ±0.01	
		I_{OL} = 1.6mA			0.4	
Output Leakage	I_{OLK}	GND ≤ V_O ≤ V_{CC}	−5.0		+5.0	
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}		10	100	µA
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_O = 0			4	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 5%, C_L = 50pF, T_A = Operating Temperature Range

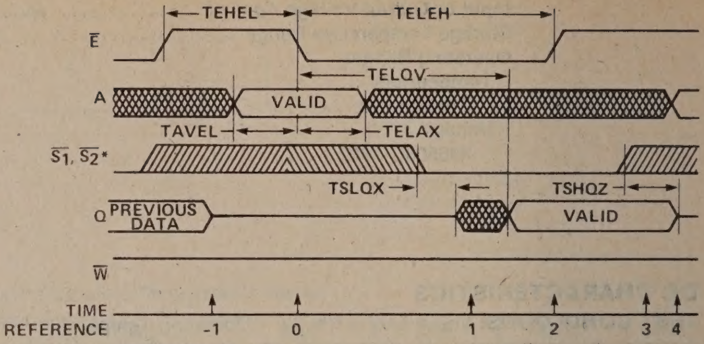
PARAMETER	SYMBOL	IM6508C/18C		UNITS
		MIN	MAX	
Access Time From $\overline{E}$	TELQV		300	ns
Output Enable Time	TSLQX		200	
Output Disable Time	TSHQZ		200	
$\overline{E}$ Pulse Width (Pos)	TEHEL	150		
$\overline{E}$ Pulse Width (Neg)	TELEH	300		
$\overline{W}$ Pulse Width (Neg)	TWLWH	160		
Address Setup Time	TAVEL	20		
Address Hold Time	TELAX	70		
Data Setup Time	TDVEH	130		
Data Hold Time	TEHDX	0		

READ MODE OPERATION

In a typical READ operation the address lines are latched by the falling edge of strobe input $\overline{E}$. If the chip has been selected, i.e. $\overline{S}_1$ and $\overline{S}_2$ (65X18 only) are low, data becomes valid an access time (TELQV) after the falling $\overline{E}$ edge. Data out for 65X08 (16 pin) remains valid until $\overline{E}$ returns high. Data out for 65X18 (18 pin) is latched when $\overline{E}$ returns high, and remains valid until a chip select ($\overline{S}_1$ or $\overline{S}_2$) is returned high.

Address information is edge triggered and must be valid a setup time (TAVEL) before and a hold time (TELAX) after the falling $\overline{E}$ edge. $\overline{S}_1$ and $\overline{S}_2$ on the 65X18 are level sensitive and may occur after $\overline{E}$ transition without affecting access time.

READ CYCLE TIMING


TEHEL
TELEH
$\overline{E}$
TELQV
A
VALID
TAVEL
TELAX
$\overline{S}_1$, $\overline{S}_2$*
TSLQX
TSHQZ
Q
PREVIOUS DATA
VALID
$\overline{W}$
TIME REFERENCE
-1
0
1
2
3
4

*65X18 ONLY

FUNCTION TABLE • READ

TIME REF	INPUTS				OUTPUT	NOTES
	$\overline{E}$	A	$\overline{S}$	$\overline{W}$	Q	
-1	H	X	H	H	Z	Memory inactive, output high Z
0	↓	V	X	H	Z	Addresses latched, output still high Z
1	L	X	L	H	X	Output enabled and active
2	L	X	L	H	V	Output valid
3	↑	X	L	H	V	Output latched and valid (65X18). Output (65X08).
4	H	X	H	H	Z	Output disabled, high Z. Ready for next cycle.

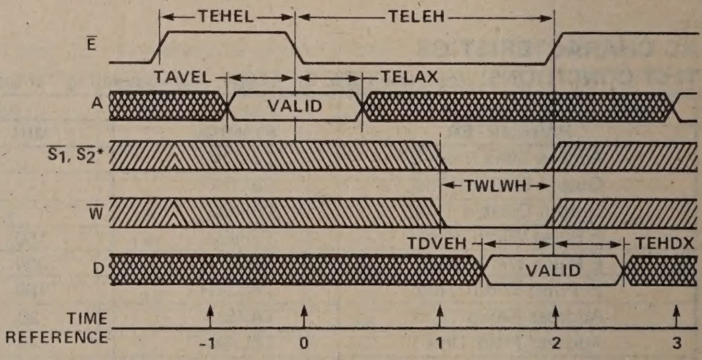
WRITE MODE OPERATION

For a WRITE operation, address lines are latched by $\overline{E}$ as in a READ operation. Writing begins when strobe ($\overline{E}$), chip selects ($\overline{S}_1$, $\overline{S}_2$) and write ($\overline{W}$) are low and ends when one of these lines returns high. Data (D) must be valid a setup time (TDVEH) before and a hold time (TEHDX) after the final rising edge.

Minimum write pulse widths are specified as TWLWH for $\overline{W}$, $\overline{S}_1$ and $\overline{S}_2$. Minimum write pulse width is specified as TELEH for $\overline{E}$.

NOTE: Transitions on strobe line $\overline{E}$ during power down or standby modes may cause change of address or loss of data. When in either mode care must be taken to maintain $\overline{E}$ at CMOS V_{CC} level.

WRITE CYCLE TIMING


TEHEL
TELEH
$\overline{E}$
TAVEL
TELAX
A
VALID
$\overline{S}_1$, $\overline{S}_2$*
TWLWH
$\overline{W}$
TDVEH
TEHDX
D
VALID
TIME REFERENCE
-1
0
1
2
3

*65X18 ONLY

FUNCTION TABLE • WRITE

TIME REF	INPUT					OUTPUT	NOTES
	$\overline{E}$	A	$\overline{S}$*	$\overline{W}$	D	Q	
-1	H	X	H	X	X	Z	Memory inactive, output high Z
0	↓	V	H	X	X	Z	Addresses latched
1	L	X	L	↓	X	Z	Write operation begins
2	L	X	L	↑	V	Z	Write operation ends
3	H	X	H	H	X	Z	Output disabled, high Z. Ready for next cycle.

INTERSIL

IM6512/A
768 BIT (64 x 12) CMOS RAM

FEATURES

- Low Power Operation
- TTL or CMOS Compatible on Inputs and Outputs
- 4V-11V V_{CC} Operation
- Static Operation
- On-Chip Address Register
- Two IM6512's can be used with IM6100 and IM6312 without additional components

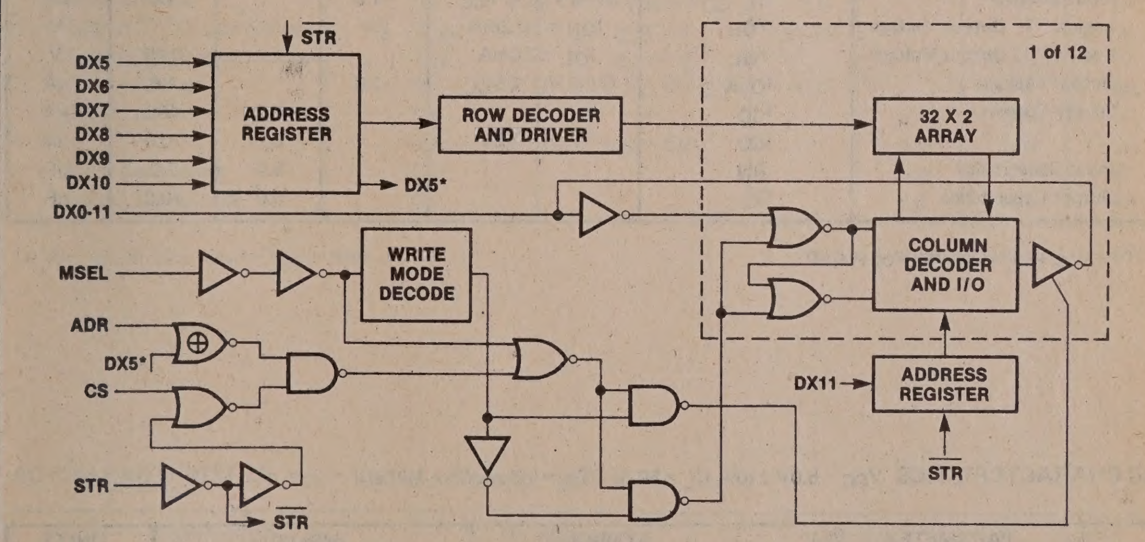
GENERAL DESCRIPTION

The IM6512 is a high speed, low power, silicon gate 768 bit CMOS static RAM organized 64 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. Inputs and three state outputs are TTL compatible. The basic part operates at 4-7 volts with a typical 5 volt, 25°C access time of 350ns. A wider operating voltage range, 4-11 volts, is available with the A version. Signal polarities and functions are specified for direct interfacing with the IM6100 microprocessor. The device is ideally suited for minimum system all CMOS applications where low power, minimum cost, or non-volatility is required.

FUNCTIONAL DESCRIPTION

The MSEL pin performs both chip enable and write-enable functions. The IM6512 has three modes of operation: read-modify-write, read only, and write. The ADR input allows two IM6512's to be used without additional decoding circuitry.

FUNCTIONAL DIAGRAM


STR
DX5
DX6
DX7
DX8
DX9
DX10
ADDRESS REGISTER
ROW DECODER AND DRIVER
DX5*
1 of 12
32 X 2 ARRAY
DX0-11
COLUMN DECODER AND I/O
MSEL
WRITE MODE DECODE
ADR
DX5*
CS
DX11
ADDRESS REGISTER
STR
STR
STR

ORDERING INFORMATION

IM6512 A I JN

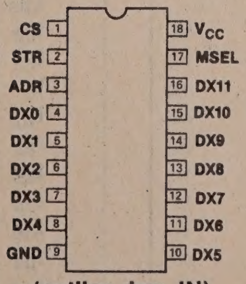
Package
JN - Ceramic Dip
FN - Flatpak

Temperature Range
C = (0°C to 70°C)
I = (−40°C to +85°C)
M = (−55°C to +125°C)

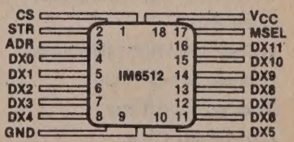
Electrical Option

Base Part Number

PIN CONFIGURATION


CS 1
STR 2
ADR 3
DX0 4
DX1 5
DX2 6
DX3 7
DX4 8
GND 9
18 VCC
17 MSEL
16 DX11
15 DX10
14 DX9
13 DX8
12 DX7
11 DX6
10 DX5

(outline dwg JN)


CS
STR
ADR
DX0
DX1
DX2
DX3
DX4
GND
VCC
MSEL
DX11
DX10
DX9
DX8
DX7
DX6
DX5
IM6512
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

(outline dwg FN)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +8.0V
Input or Output Voltage Supplied .... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range .... −65° to +150°C
Operating Temperature Range
  Industrial IM6512I .... −40°C to +85°C
  Military IM6512M .... −55°C to +125°C

DC CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$ T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		$V_{CC}-2.0$			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OH} = -0.2mA$	2.4			V
Logical "0" Output Voltage	V_{OL}	$I_{OL} = 2.0mA$			0.45	V
Output Leakage	I_{OLK}	$0V \leq V_O \leq V_{CC}$	−1.0		1.0	μA
Supply Current	I_{CC}	*		1.0	100	μA
	I_{CC}	$^*V_{CC} = 3.0V$		0.1	10.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

* STR = V_{CC}, all other inputs = V_{CC} or GND

AC CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$, $C_L = 50$ pF, T_A = Industrial or Military

PARAMETER	SYMBOL	IM6512		UNITS
		MIN	MAX	
Access Time From STR	t_{ac}		460	ns
Output Enable Time	t_{en}		285	ns
Output Disable Time	t_{dis}		285	ns
STR Pulse Width (Positive)	t_{str}	300		ns
STR Pulse Width (Negative)	t_{str}	460		ns
Cycle Time	t_c	760		ns
Write Pulse Width (Negative)	t_{wp}	300		ns
Address Setup Time	t_{as}	40		ns
Address Hold Time	t_{ah}	130		ns
Data Setup Time	t_{ds}	300		ns
Data Hold Time	t_{dh}	0		ns
MSEL Pulse Separation	t_{ps}	150		ns
MSEL Setup Time	t_{ms}	50		ns
MSEL Hold Time	t_{mh}	50		ns

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND −0.3V to V_{CC} +0.3V
Storage Temperature Range	−65° to +150°C
Operating Temperature Range	
Industrial IM6512I	−40°C to +85°C
Military IM6512AM	−55°C to +125°C

DC CHARACTERISTICS V_{CC} = 4V to 11V, T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	V_{CC}−0.01			V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$			GND+0.01	V
Output Leakage	I_{OLK}	$0V \leq V_O \leq V_{CC}$	−1.0		1.0	μA
Supply Current	I_{CC}	*		5.0	500	μA
	I_{CC}	*V_{CC} = 3.0V		0.1	10.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

* STR = V_{CC}, all other inputs = V_{CC} or GND

AC CHARACTERISTICS V_{CC} = 10V, C_L = 50pF, T_A = 25°C

PARAMETER	SYMBOL	IM6512A		UNITS
		MIN	MAX	
Access Time From STR	t_{ac}		150	ns
Output Enable Time	t_{en}		90	ns
Output Disable Time	t_{dis}		90	ns
STR Pulse Width (Positive)	t_{str}	95		ns
STR Pulse Width (Negative)	$t_{\overline{str}}$	150		ns
Cycle Time	t_c	245		ns
Write Pulse Width (Negative)	t_{wp}	95		ns
Address Setup Time	t_{as}	20		ns
Address Hold Time	t_{ah}	45		ns
Data Setup Time	t_{ds}	95		ns
Data Hold Time	t_{dh}	0		ns
MSEL Pulse Separation	t_{p}	60		ns
MSEL Setup Time	t_{ms}	20		ns
MSEL Hold Time	t_{mh}	20		ns

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +7.0V
Input or Output Voltage Supplied .... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range .... −65° to +150°C
Operating Temperature Range
  Commercial IM6512C .... 0°C to +70°C

DC CHARACTERISTICS V_{CC} = 5.0V ±5%, T_A = Commercial

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}–1.5			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	–5.0		5.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = –0.2mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 1.6mA			0.45	V
Output Leakage	I_{OLK}	$0V \leq V_O \leq V_{CC}$	–5.0		5.0	μA
Supply Current	I_{CC}	*			800	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

*STR = V_{CC}, all other inputs = V_{CC} or GND

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AC CHARACTERISTICS V_{CC} = 5.0V ±5%, C_L = 50 pF, T_A = Commercial

PARAMETER	SYMBOL	IM6512C		UNITS
		MIN	MAX	
Access Time From STR	t_{ac}		600	ns
Output Enable Time	t_{en}		375	ns
Output Disable Time	t_{dis}		375	ns
STR Pulse Width (Positive)	t_{str}	395		ns
STR Pulse Width (Negative)	$t_{\overline{str}}$	600		ns
Cycle Time	t_c	995		ns
Write Pulse Width (Negative)	t_{wp}	395		ns
Address Setup Time	t_{as}	40		ns
Address Hold Time	t_{ah}	130		ns
Data Setup Time	t_{ds}	395		ns
Data Hold Time	t_{dh}	0		ns
MSEL Pulse Separation	t_{ps}	150		ns
MSEL Setup Time	t_{ms}	50		ns
MSEL Hold Time	t_{mh}	50		ns

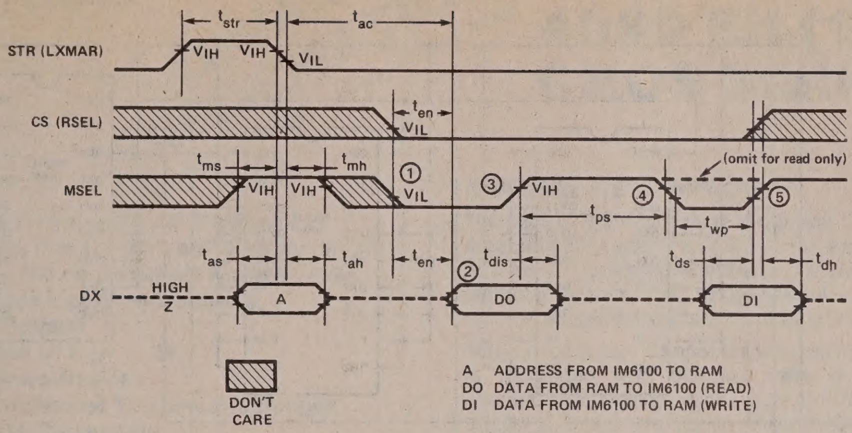

t_str
t_ac
STR (LXMAR)
VIH VIH
VIL
CS (RSEL)
t_en
VIL
t_ms
t_mh
MSEL
VIH VIH
①
VIL
③
VIH
④
⑤
(omit for read only)
t_ps
t_wp
t_as
t_ah
t_en
②
t_dis
t_ds
t_dh
DX
HIGH Z
A
DO
DI
DON'T CARE
A ADDRESS FROM IM6100 TO RAM
DO DATA FROM RAM TO IM6100 (READ)
DI DATA FROM IM6100 TO RAM (WRITE)

FIGURE 1. Read-Modify-Write or Read Cycle

Read-Modify-Write (MSEL high when STR goes low)

DX pins are high impedance until the first negative-going edge on MSEL ① which enables the outputs to read data from memory ②. When MSEL returns high ③ the DX pins return to high impedance for the remainder of the cycle.

The (optional) second negative-going MSEL pulse ④ causes a write to memory. Data at DX pins to be written into memory should be valid for a time (t_{DS}) prior to, and a time (t_{DH}) following the rising edge of MSEL ⑤. MSEL must remain high until STR returns high ending the cycle.

Read Only

Same as Read-Modify-Write except the second negative-going MSEL pulse is omitted.

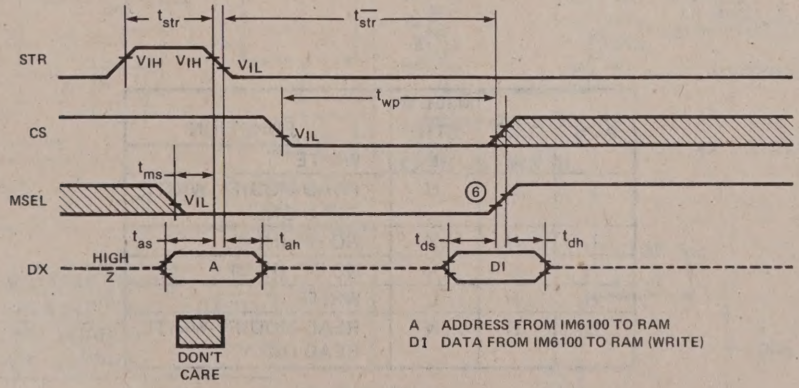

t_str
t_str
STR
VIH VIH
VIL
t_wp
CS
VIL
t_ms
MSEL
VIL
⑥
t_as
t_ah
t_ds
t_dh
DX
HIGH Z
A
DI
DON'T CARE
A ADDRESS FROM IM6100 TO RAM
DI DATA FROM IM6100 TO RAM (WRITE)

FIGURE 2. Write Cycle

Write (MSEL low when STR goes low)

DX pins are always high impedance. Data at DX pins to be written into memory should be valid for a time (t_{DS}) prior to, and a time (t_{DH}) following the rising edge of MSEL ⑥.

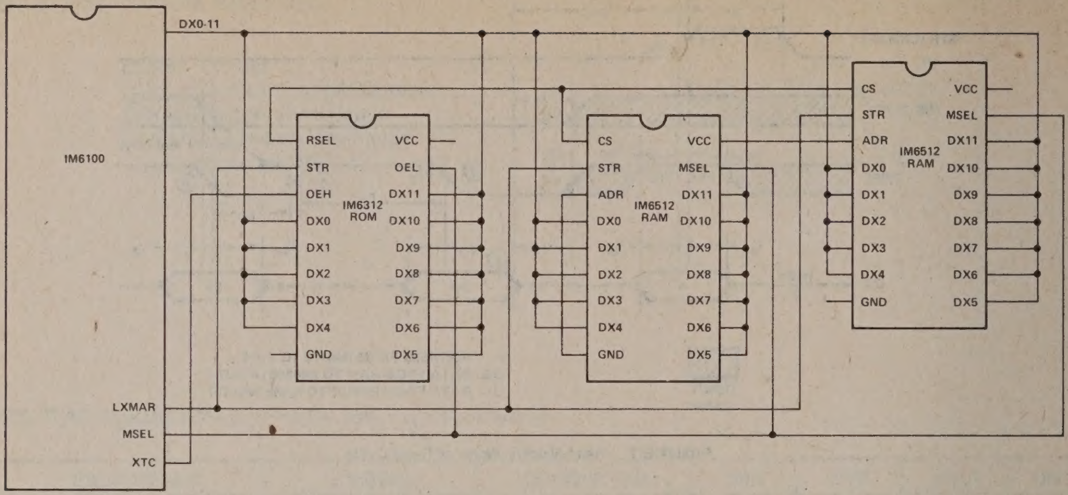

IM6100
DX0-11
LXMAR
MSEL
XTC
RSEL
VCC
STR
OEL
OEH
IM6312 ROM
DX11
DX0
DX10
DX1
DX9
DX2
DX8
DX3
DX7
DX4
DX6
GND
DX5
CS
VCC
STR
MSEL
ADR
IM6512 RAM
DX11
DX0
DX10
DX1
DX9
DX2
DX8
DX3
DX7
DX4
DX6
GND
DX5
CS
VCC
STR
MSEL
ADR
IM6512 RAM
DX11
DX0
DX10
DX1
DX9
DX2
DX8
DX3
DX7
DX4
DX6
GND
DX5

FIGURE 3. A Typical Microprocessor System

Typical Microprocessor System (Figure 3)

In the example shown, the IM6312 RSEL (RAM Select) output is programmed to go low for addresses 0-255. IM6512 with ADR = "0" will respond to addresses 0-63 (and 128-191); IM6512 with ADR = "1" will respond to addresses 64-127 (and 192-255).

ADR

ADR should be either tied to logic "0" (GND) or logic "1" (V_{CC}). The data on this pin is compared internally with address data on DX5. If the two match, the chip will respond to MSEL and CS, otherwise the IM6512 DX lines remain high impedance and data is unchanged. As a result, two IM6512 memories can be used with the IM6100 and IM6312 without additional components.

ADR	DX5*	MSEL @ $\overline{\text{STR}}^1$	FUNCTION
L	L	L	WRITE
L	L	H	READ-MODIFY-WRITE, READ ONLY
L	H	X	NO OP. (HI-Z)
H	L	X	NO OP. (HI-Z)
H	H	L	WRITE
H	H	H	READ-MODIFY-WRITE, READ ONLY

X = DON'T CARE

Note 1: Addresses are latched on chip by the falling edge of STR

FIGURE 4. IM6512 Truth Table

INTERSIL

ADVANCE INFORMATION
Specifications Subject To Change Without Notice

IM6514
4096 Bit (1K x 4) CMOS Static RAM

FEATURES

- **Low Standby Power—275 μW maximum**
- **Low Operating Power—38.5 mW/MHz maximum**
- **High Speed—300 ns Maximum Access Time**
- **TTL Compatible Inputs and Outputs**
- **Three State Outputs**
- **Data Retention to V_{CC} = 2V**
- **On-Chip Address Register**
- **Military and Industrial Temperature Ranges**
- **Harris HM6514 Compatible**

GENERAL DESCRIPTION

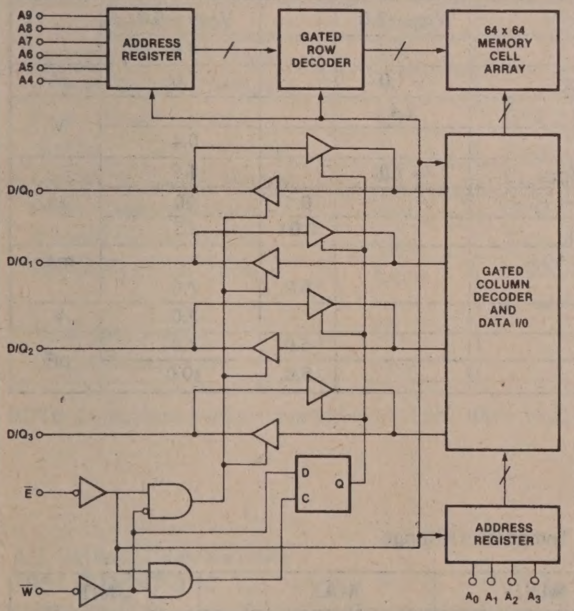
The IM6514 is a high speed, low power CMOS Static RAM organized 1024 words by 4 bits. Input and three state outputs are TTL compatible and allow for direct interface with common system bus structures. An on-chip address register simplifies system interfacing requirements.

This device is fully compatible with the Harris HM6514, but is fabricated with Intersil's selective oxidation, ion-planted, self aligned silicon gate CMOS process, called SELOX C, to achieve higher reliability and performance.

The standard part operates from 4.5 to 5.5 volts with an access time of 300ns and standby supply current of 50μA guaranteed over operating temperature range.

Minimum standby current is drawn when chip select line $\overline{E}$ is held at V_{CC} and all address, data and control lines are held at either V_{CC} or GND. Data retention is guaranteed to a V_{CC} of 2.0V.

BLOCK DIAGRAM


A9
A8
A7
A6
A5
A4
ADDRESS REGISTER
GATED ROW DECODER
64 x 64 MEMORY CELL ARRAY
D/Q₀
D/Q₁
D/Q₂
D/Q₃
GATED COLUMN DECODER AND DATA I/O
E
W
D
C
Q
ADDRESS REGISTER
A₀ A₁ A₂ A₃

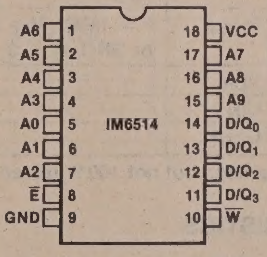
PIN NAMES

AO-A9	ADDRESS INPUTS
D/Q_{0-3}	DATA INPUTS, Q OUTPUTS
$\overline{E}$	CHIP ENABLE
$\overline{W}$	WRITE ENABLE

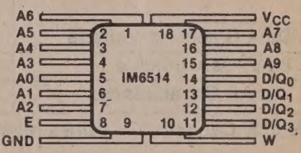
ORDERING INFORMATION

PART NO.	PACKAGE	TEMP. RANGE
IM6514IJN	18-PIN CERDIP	−40°C to +85°C
IM6514IPN	18-PIN PLASTIC	−40°C to +85°C
IM6514MJN	18-PIN CERDIP	−55°C to +125°C
IM6514MFN	18-PIN FLATPACK	−55°C to +125°C
IM6514CJN	18-PIN CERDIP	0°C to +70°C

PIN CONFIGURATIONS

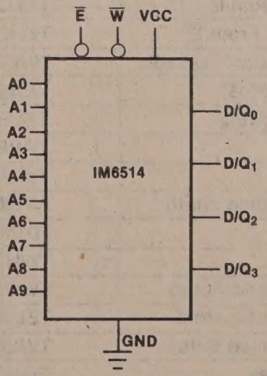

A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
E 8
GND 9
IM6514
18 VCC
17 A7
16 A8
15 A9
14 D/Q₀
13 D/Q₁
12 D/Q₂
11 D/Q₃
10 W

(outline dwgs JN, PN)


A6
A5
A4
A3
A0
A1
A2
E
GND
2 1 18 17
3 16
4 15
5 IM6514 14
6 13
7 12
8 9 10 11
VCC
A7
A8
A9
D/Q₀
D/Q₁
D/Q₂
D/Q₃
W

(outline dwg FN)

LOGIC SYMBOL


E
W
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
IM6514
D/Q₀
D/Q₁
D/Q₂
D/Q₃
GND

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	+8V
Input or Output Voltage Applied	GND −0.3V to V_{CC} +0.3V
Storage Temperature Range	−65° to +150°C
Operating Range	
Temperature	
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Voltage	
6514 I,M	4.5V to +5.5V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0		V_{CC} +0.3	V
Logical "0" Input Voltage	V_{IL}		−0.3		0.8	
Input Leakage Current	I_{ILK}	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = −1.0mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 2.0mA			0.4	
Output Leakage Current	I_{OLK}	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}		0.1	50	
		V_{CC} = 3.0V = $\bar{E}_1$		0.01	25	
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_0 = 0		5.0	7.0	mA
Data Retention Voltage	V_{DR}				2.0	V
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_{OUT}			6.0	10.0	

NOTE: Capacitance values guaranteed but not 100% tested.

OPERATING CHARACTERISTICS

AC CHARACTERISTICS[1]

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Access Time From $\bar{E}$	TELQV		300	ns
Output Disable From $\bar{E}$	TEHQZ		100	
Write Enable Output Disable	TWLQZ		100	
$\bar{E}$ Pulse Width (Pos)	TEHEL	120		
$\bar{E}$ Pulse Width (Neg)	TELEH	300		
Address Setup	TAVEL	0		
Address Hold	TELAX	50		
Write Enable Pulse Width	TWLWH	300		
Data Setup	TDVWH	200		
Data Hold	TWHDZ	0		
Write Enable Read Setup	TWHEL	0		
Write Enable Pulse Hold	TELWH	300		
Write Enable Pulse Setup	TWLEH	300		
Write Data Delay	TWLDV	100		
Data Valid to Write	TQVWL	0		
Read or Write Cycle Time	TELEL	420		

1.) AC Test Conditions: Input rise and fall times are 20 ns; Output load is 1 TTL load and 50 pf. All timing measurements are taken at ½ V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V_{CC}) .... +8V
Input or Output Voltage Applied .... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range .... −65° to +150°C
Operating Range
  Temperature .... 0°C to +70°C
  Voltage .... 4.75V to 5.25V

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5.0V \pm 5\%$, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		$V_{CC}-2.0$		$V_{CC}+0.3$	V
Logical "0" Input Voltage	V_{IL}		−0.3		0.8	
Input Leakage Current	I_{ILK}	$GND \le V_{IN} \le V_{CC}$	−10.0		+10.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OH} = -0.4mA$	2.4			V
Logical "0" Output Voltage	V_{OL}	$I_{OL} = 1.6mA$			0.4	
Output Leakage Current	I_{OLK}	$GND \le V_{IN} \le V_{CC}$	−10.0		+10.0	μA
Standby Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$		100	500	
Operating Supply Current	I_{CCOP}	$f = 1MHz$, $V_{IN} = V_{CC}$ or GND, $I_0 = 0$		5.0	7.0	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_{OUT}			6.0	10.0	

NOTE: Capacitance values guaranteed but not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5.0V \pm 5\%$, $C_L = 50pF$, T_A = Operating Temperature Range

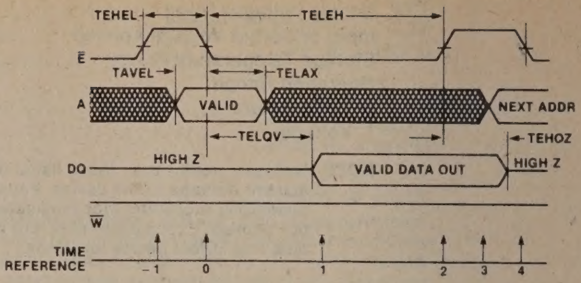
PARAMETER	SYMBOL	MIN	MAX	UNITS
Access Time from $\overline{E}$	TELQV		350	ns
Output Disable from $\overline{E}$	TEHQZ		100	
Write Enable Output Disable	TWLQZ		100	
$\overline{E}$ Pulse Width (Pos)	TEHEL	150		
$\overline{E}$ Pulse Width (Neg)	TELEH	350		
Address Setup	TAVEL	20		
Address Hold	TELAX	50		
Write Enable Pulse Width	TWLWH	350		
Data Setup	TDVWH	250		
Data Hold	TWHDZ	0		
Write Enable Read Setup	TWHEL	0		
Write Enable Pulse Hold	TELWH	350		
Write Enable Pulse Setup	TWLEH	300		
Write Data Delay	TWLDV	100		
Data Valid to Write	TQVWL	0		
Read or Write Cycle Time	TELEL	500		

1.) AC Test Conditions: Input rise and fall times are 20 ns; Output load is 1 TTL load and 50 pf. All timing measurements are taken at ½ V_{CC}.

READ CYCLE

The falling edge of chip enable (Ē) latches addresses in the on-chip register and initiates a read cycle (T = 0). Addresses to be latched must be present one setup time (TAVEL) prior to and one hold time (TELAX) following the falling edge of Ē. During time T = 1 the outputs become valid from the high Z state. There is no period of active, but invalid, data on the bus. Write enable (W̄) must remain high until after time T = 2. The read cycle is terminated when Ē goes high, disabling the output buffers.

READ CYCLE TIMING


TEHEL
TELEH
Ē
TAVEL
TELAX
A
VALID
NEXT ADDR
TELQV
TEHOZ
HIGH Z
DQ
VALID DATA OUT
HIGH Z
W̄
TIME REFERENCE
-1
0
1
2
3
4

FUNCTION TABLE • READ

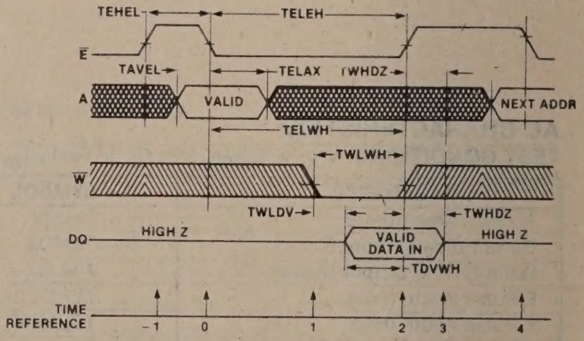
TIME REF	INPUTS			OUTPUT	NOTES
	Ē	W̄	A	Q	
-1	H	X	X	Z	MEMORY INACTIVE
0	↓	H	V	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	H	X	V	OUTPUT VALID
2	↑	H	X	V	READ COMPLETE
3	H	X	X	V	MEMORY INACTIVE (SAME AS - 1)
4	↓	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

WRITE CYCLE

The falling edge of Ē latches addresses in the on-chip register and initiates a write cycle (T = 0). Write begins when W̄ goes low (T = 1) and ends when W̄ or Ē goes high (T = 2). Data to be written must be valid one setup time before (TDVWH) the rising edge of W̄ or Ē, but not before one data delay time (TWLDV) after the falling edge of W̄ (T = 1).

At write cycle termination (T = 3), data lines become high Z one hold time (TWHDZ) after the rising edge of W or one hold time (TEHDZ) after the rising edge of Ē. The next write cycle begins at T = 4.

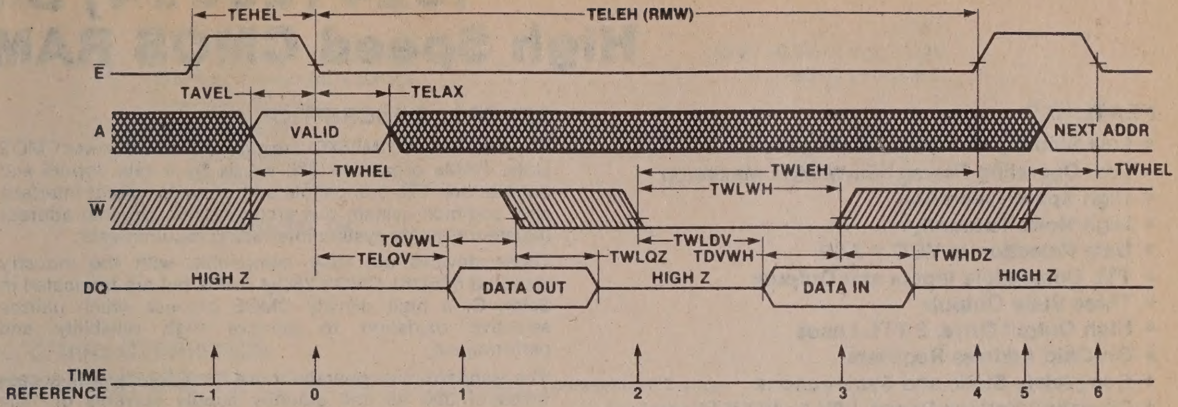
WRITE CYCLE TIMING


TEHEL
TELEH
Ē
TAVEL
TELAX
tWHDZ
A
VALID
NEXT ADDR
TELWH
TWLWH
W̄
TWLDV
TWHDZ
DQ
HIGH Z
VALID DATA IN
HIGH Z
TDVWH
TIME REFERENCE
-1
0
1
2
3
4

FUNCTION TABLE • WRITE

TIME REF	INPUTS				NOTES
	Ē	W̄	A	DQ	
-1	H	X	X	Z	MEMORY INACTIVE
0	↓	X	V	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	↓	X	Z	WRITE IN PROGRESS
2	L	↑	X	V	WRITE COMPLETE
3	H	H	X	Z	CYCLE ENDS, OUTPUTS HIGH Z
4	↓	X	V	Z	NEXT CYCLE BEGINS

READ—MODIFY—WRITE CYCLE TIMING


TEHEL
TELEH (RMW)
E
TAVEL
TELAX
A
VALID
NEXT ADDR
TWHEL
TWLEH
TWLWH
TWHEL
W
TQVWL
TELQV
TWLDV
TWLQZ
TDVWH
TWHDZ
DQ
HIGH Z
DATA OUT
HIGH Z
DATA IN
HIGH Z
TIME REFERENCE
–1
0
1
2
3
4
5
6

READ — MODIFY — WRITE CYCLE

A read - modify - write cycle may be performed if the write portion of the cycle is controlled by $\overline{W}$ and $\overline{E}$ remains low throughout. Data is read normally, with $\overline{W}$ held high, addresses latched at T = 0 and data out valid at T = 1. A data out valid to write time (TQVWL) must be observed before $\overline{W}$ is brought low to begin the write cycle. One write output disable time (TWLQZ) after W is low, the data lines return to a high-Z state and new data to be written into the address may placed on the data bus. Data to be written must be valid one setup time before (TDVWH) and one hold time after (TWHDZ) the rising edge of $\overline{W}$ (T = 3). The output buffers are latched to a high-Z state by the rising edge of $\overline{W}$, so that when input data is removed the bus remains high-Z until the next cycle.

FUNCTION TABLE • READY—MODIFY—WRITE

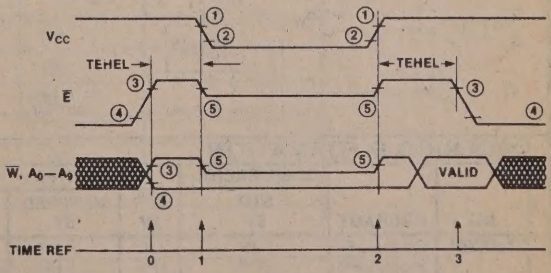
TIME REF.	INPUTS				OUTPUT	NOTES
	$\overline{E}$	$\overline{W}$	A	D	Q	
–1	H	X	X	X	Z	MEMORY INACTIVE
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	H	X	X	V	OUTPUT VALID, READ/MODIFY TIME
2	L	↘	X	X	Z	WRITE BEGINS, OUTPUT HIGH Z
3	L	↗	X	V	Z	WRITE IN PROGRESS
4	↗	X	X	X	Z	WRITE COMPLETE
5	H	X	X	X	Z	MEMORY INACTIVE (SAME AS – 1)
6	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

POWER DOWN SEQUENCE

The power down sequence begins at T = 0 with $\overline{E}$ held at a logic high level and all addresses, $\overline{W}$, established at valid logic levels. Chip enable $\overline{E}$ must be high one minimum positive pulse width (TEHEL) before power-down. At T = 1 power supply V_{CC} may be decreased to minimum V_{CCDR}. As V_{CC} is decreased, $\overline{E}$ must remain within data retention high logic level threshold limits (V_{IHDR}), and $\overline{W}$ and A_0-A_9, must remain within V_{IHDR} or V_{IL} limits. Failure to remain within these limits may cause data loss or SCR latch-up.

The same conditions must be met, in reverse, when returning to normal power (T = 2,3).

POWER DOWN TIMING


V_{CC}
①
②
①
②
TEHEL
TEHEL
③
③
$\overline{E}$
④
⑤
⑤
④
$\overline{W}$, A_0—A_9
③
⑤
⑤
④
VALID
TIME REF
0
1
2
3

① 4.5V

② V_{CCDR} ($5.5V \geq V_{CCDR} \geq 2.0V$)

③ V_{IH} ($V_{CC} + 0.3V \geq V_{IH} \geq V_{CC} - 2.0V$)

④ V_{IL} ($0.8 \geq V_{IL} \geq GND—0.3V$)

⑤ V_{IHDR} ($V_{CC} + 0.3V \geq V_{IHDR} \geq V_{CC} - 2.0V \geq 2.0V$)

IM65X51/IM65X61
1024 (256 x 4) Bit
High Speed CMOS RAM

FEATURES

- **Low Standby Power: 55μW Maximum**
- **Low Operating Power: 10mW/MHz Maximum**
- **High Speed Operation**
- **High Noise Immunity**
- **Data Retention to VCC = 2.0V**
- **TTL Compatible Inputs and Outputs**
- **Three State Outputs**
- **High Output Drive: 2 TTL Loads**
- **On-Chip Address Registers**
- **Completely Static and Synchronous**
- **Operating Voltage Range 4.5V to 10.5V (A version)**
- **Military and Industrial Temperature Ranges**

GENERAL DESCRIPTION

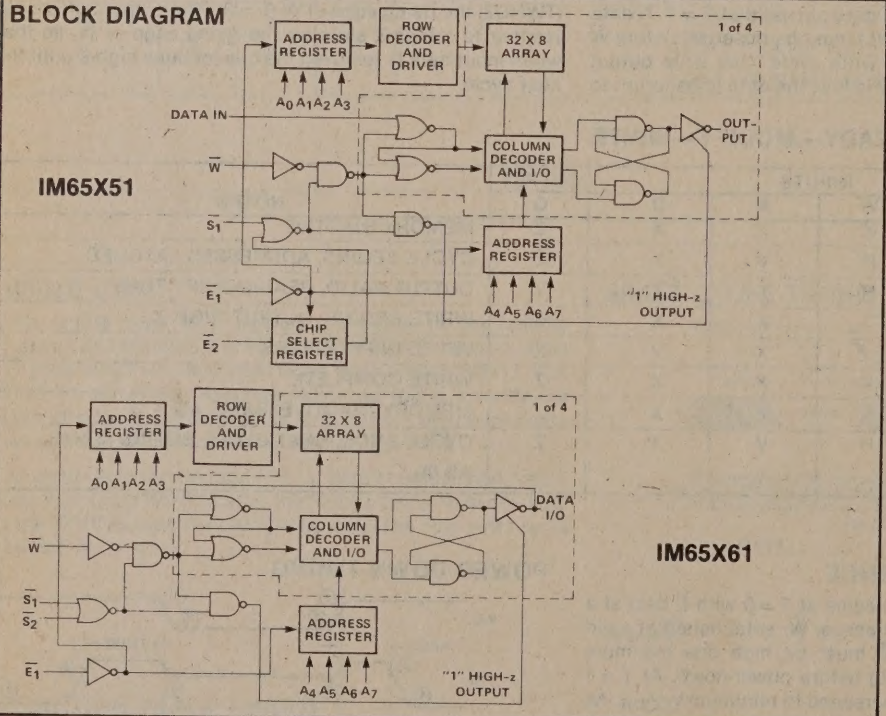
The IM65X51 and IM65X61 are high speed, low power CMOS static RAMs organized 256 words by 4 bits. Inputs and outputs are TTL compatible and allow for direct interface with common system bus architectures. On-chip address registers simplify system interfacing requirements.

These devices are fully compatible with the industry standard 6551/61 CMOS 256x4 RAMs but are fabricated in Selox C, a high density CMOS process which utilizes selective oxidation to achieve high reliability and performance.

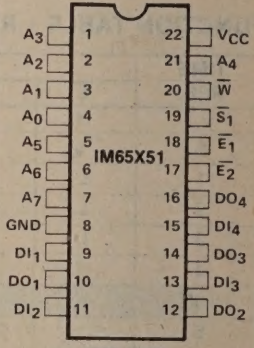
The standard parts operate from 4.5 to 5.5 volts, with access times of 300 ns and standby supply currents of 10μa guaranteed over operating temperature range. Access times of 220 ns are offered in "-1" versions, and 4.5 to 10.5 volt operating ranges are available in "A" versions.

Minimum standby current is drawn when $\overline{E}$ is held at V_{CC} and all address, data and control lines are held at either V_{CC} or GND. Data retention is guaranteed to a V_{CC} of 2.0V.

BLOCK DIAGRAM

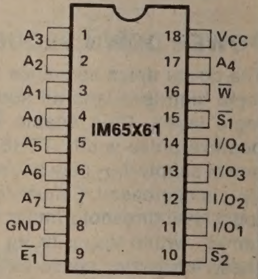

IM65X51
ADDRESS REGISTER
ROW DECODER AND DRIVER
32 X 8 ARRAY
1 of 4
A0 A1 A2 A3
DATA IN
W
S1
E1
E2
COLUMN DECODER AND I/O
OUT-PUT
ADDRESS REGISTER
A4 A5 A6 A7
CHIP SELECT REGISTER
"1" HIGH-z OUTPUT
IM65X61
ADDRESS REGISTER
ROW DECODER AND DRIVER
32 X 8 ARRAY
1 of 4
A0 A1 A2 A3
DATA I/O
W
S1
S2
E1
COLUMN DECODER AND I/O
ADDRESS REGISTER
A4 A5 A6 A7
"1" HIGH-z OUTPUT

PIN CONFIGURATION


A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
DI1 9
DO1 10
DI2 11
22 VCC
21 A4
20 W
19 S1
18 E1
17 E2
16 DO4
15 DI4
14 DO3
13 DI3
12 DO2
IM65X51

TOP VIEW

(outline dwg JF, PF)


A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
E1 9
18 VCC
17 A4
16 W
15 S1
14 I/O4
13 I/O3
12 I/O2
11 I/O1
10 S2
IM65X61

TOP VIEW

(outline dwg JN, PN)

Pin 1 is designated by a dot or a notch.

ORDERING INFORMATION

NO.	PACKAGE	COMMERCIAL	INDUSTRIAL			MILITARY*		
		STD 5V	STD 5V	HI SPEED 5V	STD 10V	STD 5V	HI SPEED 5V	STD 10V
IM65X51	Cerdip JF	CJF	IJF	– 1 IJF	AIJF	MJF	– 1 MJF	AMJF
	Plastic PF	CPF	IPF	– 1 IPF	AIPF	—	—	—
IM65X61	Cerdip JN	CJN	IJN	– 1 IJN	AIJN	MJN	– 1 MJN	AMJN
	Plastic PN	CPN	IPN	– 1 IPN	AIPN	—	—	—
	Flatpak					MFN		AMFN

*If 883B processing is desired, add /883B to order number.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Supplied	GND −0.3V to V_{CC} +0.3V
Storage Temperature Range	−65° C to +150° C
Operating Range	
Temperature	
Industrial	−40° C to +85° C
Military	−55° C to +125° C
Voltage	
IM65X51/X61 I,M	4.5V to 5.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{IL}	GND≤V_{IN}≤V_{CC}	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH1}	I_{OH} = −0.4mA	2.4			V
Logical "0" Output Voltage	V_{OL1}	I_{OL} = 3.2mA			0.45	
Output Leakage	I_{OLK}	GND≤V_O≤V_{CC}	−1.0		1.0	μA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}		1	10	
		V_{CC} = 3V = $\bar{E}_1$		0.1	10	
Operating Supply Current	I_{CCOP}	f = 1 MHz, V_{IN} = V_{CC} or GND, I_O = 0			2	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM65X51/X61 I,M		UNITS
		MIN	MAX	
Access Time From $\bar{E}_1$	TE_1LQV		300	ns
Output Enable Time	TSLQV		150	
Output Disable Time	TSHQZ		150	
$\bar{E}_1$ Pulse Width (Positive)	TE_1HE_1L	100		
$\bar{E}_1$ Pulse Width (Negative)	TE_1LE_1H	300		
$\bar{W}$ Pulse Width (Negative)	TWLWH	300		
Address Setup Time	$TAVE_1L$	0		
Address Hold Time	TE_1LAX	60		
Data Setup Time	$TDVE_1H$	150		
Data Hold Time	TE_1HDX	0		

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +8.0V
Input or Output Voltage Applied .... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range .... −65°C to +150°C
Operating Range
  Temperature
    Industrial .... −40°C to +85°C
    Military .... −55°C to +125°C
  Voltage
    IM65X51-1/X61-1I, -1M .... 4.5V to 5.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{IL}	GND≤V_{IN}≤V_{CC}	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH1}	I_{OH} = −0.4mA	2.4			V
Logical "0" Output Voltage	V_{OL1}	I_{OL} = 3.2mA			0.45	
Output Leakage	I_{OLK}	GND≤V_O≤V_{CC}	−1.0		1.0	μA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}		1	10	
		V_{CC} = 3V = $\overline{E}_1$		0.1	10	
Operating Supply Current	I_{CCOP}	f = 1 MHz, V_{IN} = V_{CC} or GND, I_O = 0			2	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM65X51-1/X61-1I, -1M		UNITS
		MIN	MAX	
Access Time From $\overline{E}$	TE_1LQV		220	ns
Output Enable Time	TSLQV		130	
Output Disable Time	TSHQZ		130	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HEL	100		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LEH	220		
$\overline{W}$ Pulse Width (Negative)	TWLWH	220		
Address Setup Time	$TAVE_1L$	0		
Address Hold Time	TE_1LAX	60		
Data Setup Time	$TDVE_1H$	100		
Data Hold Time	TE_1HDX	0		

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +12.0V
Input or Output Voltage Applied .... GND −0.3V to VCC +0.3V
Storage Temperature Range .... −65°C to +150°C
Operating Range
Temperature
Industrial .... −40°C to +85°C
Military .... −55°C to +125°C
Voltage
IM65X51A, IM65X61A .... 4.5V to 10.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4.5V to 10.5V, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{IL}	$GND \leq V_{IN} \leq V_{CC}$	−1.0		1.0	µA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	V_{CC} −0.01			V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$			GND +0.01	
Output Leakage	I_{OLK}	$GND \leq V_O \leq V_{CC}$	−1.0		1.0	µA
Standby Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$		5.0	500	
		$V_{CC} = 3.0V = \overline{E}_1$		0.1	50	
Operating Supply Current	I_{CCOP}	f = 1 MHz, $V_{IN} = V_{CC}$ or GND, $I_O = 0$			10	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM65X51A/X61A I,M		UNITS
		MIN	MAX	
Access Time From $\overline{E}_1$	TE_1LQV		235	ns
Output Enable Time	TSLQV		120	
Output Disable Time	TSHQV		120	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	80		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	145		
$\overline{W}$ Pulse Width (Negative)	TWLWH	160		
Address Setup Time	$TAVE_1L$	35		
Address Hold Time	TE_1LAX	80		
Data Setup Time	$TDVE_1H$	80		
Data Hold Time	TE_1HDX	40		

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8.0V
Input or Output Voltage Applied	GND −0.3V to VCC +0.3V
Storage Temperature Range	−65° C to +150° C
Operating Range	
Temperature	
Commercial	0° C to 75° C
Voltage	
IM65X51/X61C	4.75V to 5.25V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 5%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		$V_{CC}-2.0$			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{IL}	$GND \leq V_{IN} \leq V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH1}	$I_{OH} = -0.2mA$	2.4			V
Logical "0" Output Voltage	V_{OL1}	$I_{OL} = 1.6mA$			0.45	
Output Leakage	I_{OLK}	$GND \leq V_O \leq V_{CC}$	−1.0		1.0	μA
Standby Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$		10	100	
Operating Supply Current	I_{CCOP}	f = 1 MHz, $V_{IN} = V_{CC}$ or GND, $I_O = 0$			4.0	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 5%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM65X51C/X61C		UNITS
		MIN	MAX	
Access Time From $\overline{E}_1$	TE_1LQV		350	ns
Output Enable Time	TSLQV		180	
Output Disable Time	TSHQZ		180	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	150		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	350		
$\overline{W}$ Pulse Width (Negative)	TWLWH	350		
Address Setup Time	$TAVE_1L$	20		
Address Hold Time	TE_1LAX	70		
Data Setup Time	$TDVE_1H$	170		
Data Hold Time	TE_1HDX	0		

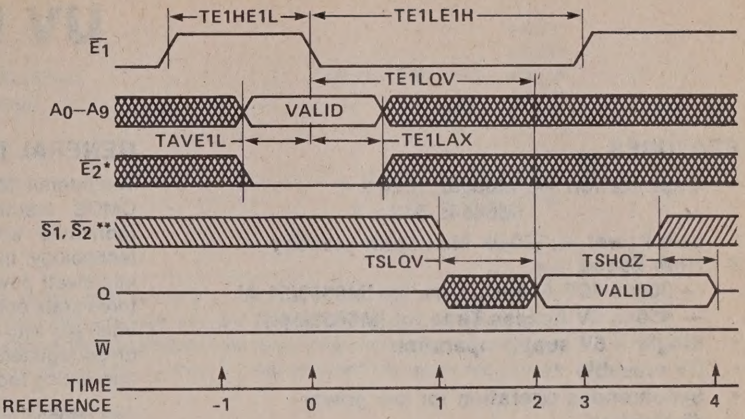
READ MODE OPERATION

In a typical READ operation the address lines are latched by the falling edge of strobe input $\overline{E}_1$. If the chip has been selected, i.e. $\overline{S}_1$ and $\overline{S}_2$ (65X51 only) are low, data becomes valid an access time (TE_1LQV) after the falling edge of $\overline{E}_1$. Data is latched into output registers by rising $\overline{E}_1$ and remains valid until the next cycle or until a chip select ($\overline{S}_1$ or $\overline{S}_2$) is returned high.

Address and $\overline{E}_2$ information is edge triggered and must be valid a setup time ($TAVE_1L$) before and a hold time (TE_1LAX) after the falling edge of $\overline{E}_1$.

$\overline{S}_1$, $\overline{S}_2$ and $\overline{W}$ are level sensitive and may occur after $\overline{E}_1$ transitions without affecting access time.

READ CYCLE TIMING



FUNCTION TABLE • READ

TIME REF.	INPUTS					OUTPUTS	NOTES
	$\overline{E}_1$	A	$\overline{E}_2$*	$\overline{S}$	$\overline{W}$	Q	
-1	H	X	X	H	X	Z	Memory Inactive, output high Z.
0	↘	V	L	X	H	Z	Addresses and $\overline{E}_2$ latched, output still high Z.
1	L	X	X	L	H	X	Output enabled and active.
2	L	X	X	L	H	V	Output valid.
3	↗	X	X	L	H	V	Output latched and valid, memory inactive.
4	H	X	X	H	H	Z	Output high Z. Ready for next cycle.

*65X51 only **65X61 only

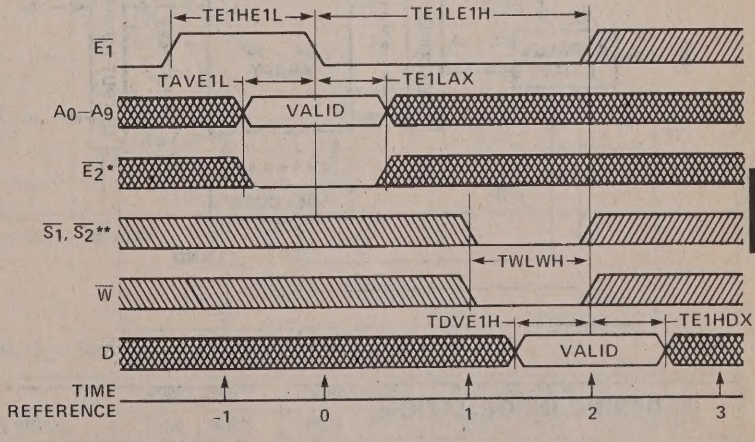
WRITE MODE OPERATION

For a WRITE operation addresses and $\overline{E}_2$ are latched by $\overline{E}_1$ as in a READ operation. Data is written when strobe ($\overline{E}_1$), chip selects ($\overline{S}_1$, $\overline{S}_2$) and write ($\overline{W}$) are low. WRITE operation ends when one of these lines returns high. Minimum write pulse requirements are specified for $\overline{E}_1$ as TE_1LE_1H and for $\overline{S}_1$, $\overline{S}_2$, $\overline{W}$ as TWLWH.

Data must be valid a setup time ($TDVE_1H$) before and a hold time (TE_1HDX) after the rising edge of $\overline{E}_1$.

Note: Transitions on strobe line $\overline{E}_1$ when addresses are at indeterminate levels such as the transition to power down or standby mode may cause change of address or loss of data. When in either mode care must be taken to maintain $\overline{E}_1$ at V_{CC} level.

WRITE CYCLE TIMING



FUNCTION TABLE • WRITE

TIME REF.	INPUTS						OUTPUTS	NOTES
	$\overline{E}_1$	A	$\overline{E}_2$*	$\overline{S}$	$\overline{W}$	D	Q	
-1	H	X	X	H	X	X	Z	Memory Inactive, Outputs high Z.
0	↘	V	L	H	X	X	Z	Addresses and $\overline{E}_2$ latched.
1	L	X	X	L	↘	X	Z	Write operation begins.
2	L	X	X	L	↗	V	Z	Write operation ends.
3	H	X	X	H	H	X	Z	Outputs high Z. Ready for next cycle.

*65X51 only **65X61 only

INTERSIL

IM6653/IM6654
4096 Bit CMOS UV Erasable PROM

FEATURES

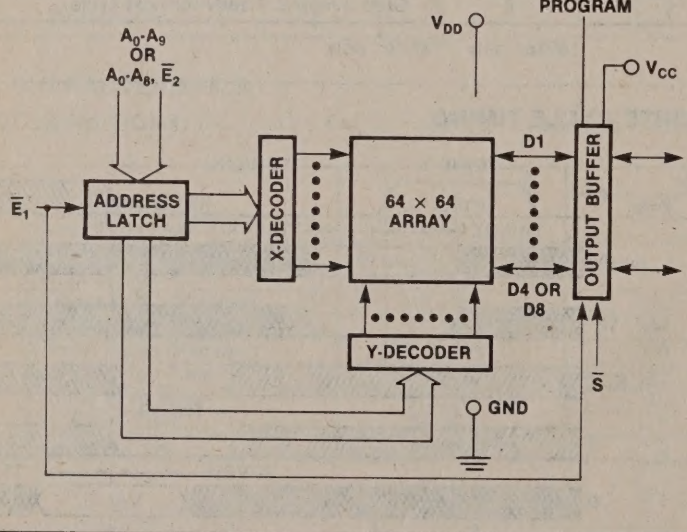
- Organization — IM6653: 1024 x 4
  IM6654: 512 x 8
- Low Power — 770μW Maximum Standby
- High Speed
  — 300ns 10V Access Time for IM6653/54 AI
  — 450ns 5V Access Time for IM6653/54-1I
- Single +5V supply operation
- UV erasable
- Synchronous operation for low power dissipation
- Three-state outputs and chip select for easy system expansion
- Full −55°C to +125°C MIL range devices—IM6653/54 M, IM6653A/64A M

GENERAL DESCRIPTION

The Intersil IM6653 and IM6654 are fully decoded 4096 bit CMOS electrically programmable ROMs (EPROMs) fabricated with Intersil's advanced CMOS processing technology. In all static states these devices exhibit the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and chip select functions simplify system interfacing requirements.

The IM6653 and IM6654 are specifically designed for program development applications where rapid turn-around for program changes is required. The devices may be erased by exposing their transparent lids to ultra-violet light, and then re-programmed.

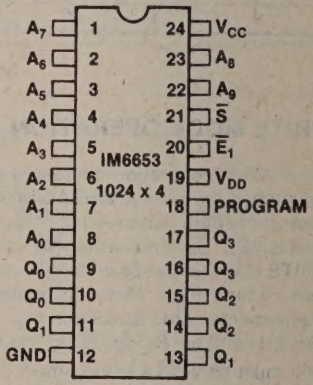
BLOCK DIAGRAM

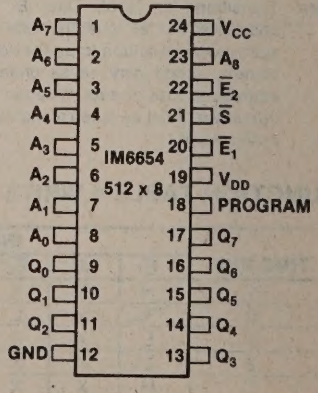

A_0-A_9
OR
A_0-A_8, $\bar{E}_2$
V_{DD}
PROGRAM
V_{CC}
$\bar{E}_1$
ADDRESS LATCH
X-DECODER
64 × 64 ARRAY
D1
D4 OR D8
OUTPUT BUFFER
Y-DECODER
GND
$\bar{S}$

ORDERING INFORMATION

24 PIN PACKAGE	SELECTION/TEMPERATURE RANGE				
	INDUSTRIAL			MILITARY	
	STD 5V	HI SPEED 5V	STD 10V	STD 5V	STD 10V
CERDIP JG (FRIT SEAL)	IJG	-1I JG	AIJG	MJG	AMJG

PIN CONFIGURATION
(outline dwg JG/W)


A_7 1
A_6 2
A_5 3
A_4 4
A_3 5
A_2 6
A_1 7
A_0 8
Q_0 9
Q_0 10
Q_1 11
GND 12
24 V_{CC}
23 A_8
22 A_9
21 $\bar{S}$
20 $\bar{E}_1$
19 V_{DD}
18 PROGRAM
17 Q_3
16 Q_3
15 Q_2
14 Q_2
13 Q_1
IM6653
1024 x 4


A_7 1
A_6 2
A_5 3
A_4 4
A_3 5
A_2 6
A_1 7
A_0 8
Q_0 9
Q_1 10
Q_2 11
GND 12
24 V_{CC}
23 A_8
22 $\bar{E}_2$
21 $\bar{S}$
20 $\bar{E}_1$
19 V_{DD}
18 PROGRAM
17 Q_7
16 Q_6
15 Q_5
14 Q_4
13 Q_3
IM6654
512 x 8

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
  V_{DD} .... +8.0V
  $V_{CC} = V_{DD}$ .... +8.0V
Input or Output Voltage Supplied .... GND − 0.3V to V_{DD} + 0.3V
Storage Temperature Range .... −65°C to +150°C
Operating Range
  Temperature
    Industrial .... −40°C to +85°C
    Military .... −55°C to +125°C
  Voltage
    6653/54 I, −1I .... 4.5 − 5.5
    6653/54 M .... 4.5 − 5.5

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 10\%$, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	IM6653/54I, -1I,M		UNITS
			MIN	MAX	
Logical "1" Input Voltage	V_{IH}	$\overline{E}_1, \overline{S}$	$V_{DD} - 2.0$		V
	V_{IH}	Address Pins	2.7		
Logical "0" Input Voltage	V_{IL}			0.8	
Input Leakage	I_I	$GND \le V_{IN} \le V_{DD}$	−1.0	1.0	µA
Logical "1" Output Voltage	$V_{OH}2$	$I_{OUT} = 0$	$V_{CC} - 0.01$		V
Logical "1" Output Voltage	V_{OH1}	$I_{OH} = -0.2mA$	2.4		
Logical "0" Output Voltage	V_{OL2}	$I_{OUT} = 0$		GND + 0.01	
Logical "0" Output Voltage	V_{OL1}	$I_{OL} = 2.0mA$		0.45	
Output Leakage	I_{OLK}	$GND \le V_O \le V_{CC}$	−1.0	1.0	µA
Standby Supply Current	I_{DDSB}	$V_{IN} = V_{DD}$		100	
	I_{CC}	$V_{IN} = V_{DD}$		40	
Operating Supply Current	I_{DDOP}	f = 1 MHz		6	mA
Input Capacitance	C_I	Note 1		7.0	pF
Output Capacitance	C_O	Note 1		10.0	

Note 1: These parameters guaranteed but not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 10\%$, $C_L = 50pf$, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6653/54-1I		IM6653/54 I		IIM6653/54 M		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Access Time From $\overline{E}_1$	TE_1LQV		450		550		600	ns
Output Enable Time	TSLQV		110		140		150	
Output Disable Time	TE_1HQZ		110		140		150	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	130		150		150		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	450		550		600		
Address Setup Time	$TAVE_1L$	0		0		0		
Address Hold Time	TE_1LAX	80		100		100		
Chip Enable Setup Time (6654)	TE_2VE_1L	0		0		0		
Chip Enable Hold Time (6654)	TE_1LE_2X	80		100		100		

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
V_{DD} .... +11.0V
$V_{CC} = V_{DD}$ .... +11.0V
Input or Output Voltage Supplied .... GND − 0.3V to V_{DD} + 0.3V
Storage Temperature Range .... −65°C to +150°C
Operating Range
Temperature
Industrial .... −40°C to +85°C
Military .... −55°C to +125°C
Voltage
6653/54 AI, AM .... 4.5 to 10.5V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 4.5V$ to $10.5V$, T_A = Operational Temperature Range

PARAMETER	SYMBOL	CONDITIONS	IM6653/54AI, AM		UNITS
			MIN	MAX	
Logical "1" Input Voltage	V_{IH}	$\overline{E}_1,\overline{S}$	$V_{DD} - 2.0$		V
	V_{IH}	Address Pins	$V_{DD} - 2.0$		
Logical "0" Input Voltage	V_{IL}			0.8	
Input Leakage	I_I	$GND \leq V_{IN} \leq V_{DD}$	-1.0	1.0	µA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	$V_{CC} - 0.01$		V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$		GND + 0.01	
Output Leakage	I_{OLK}	$GND \leq V_0 \leq V_{CC}$	−1.0	1.0	µA
Standby Supply Current	I_{DDSB}	$V_{IN} = V_{DD}$		100	
	I_{CC}	$V_{IN} = V_{DD}$		40	
Operating Supply Current	I_{DDOP}	f = 1 MHz		12	mA
Input Capacitance	C_I	Note 1		7.0	pF
Output Capacitance	C_O	Note 1		10.0	

Note 1: These parameters guaranteed but not 100% tested.

AC CHARACTERISTICS

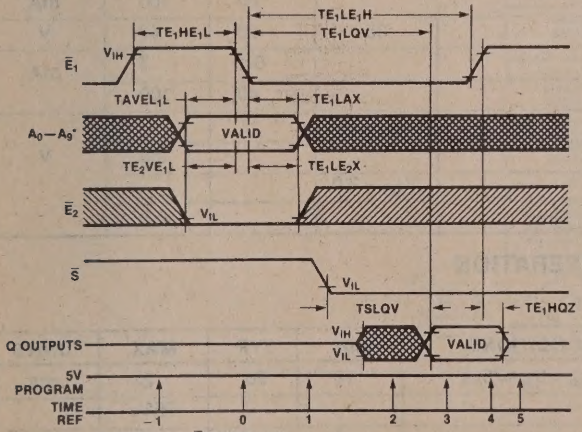
TEST CONDITIONS: $V_{CC} = V_{DD} = 10V \pm 5\%$, $C_L = 50pf$, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6653/54 AI		IM6653/54 AM		UNITS
		MIN	MAX	MIN	MAX	
Access Time From $\overline{E}_1$	TE_1LQV		300		350	ns
Output Enable Time	TSLQV		60		70	
Output Disable Time	TE_1HQZ		60		70	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	125		125		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	300		350		
Address Setup Time	$TAVE_1L$	0		0		
Address Hold Time	TE_1LAX	60		60		
Chip Enable Setup Time (6654)	TE_2VE_1L	0		0		
Chip Enable Hold Time (6654)	TE_1LE_2X	60		60		

PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1-8,23	A_0-A_7,A_8	—	Address Lines
9-11,13-17	Q_0-Q_7	—	Data Out lines, 6654
	Q_0-Q_3	—	Data Out lines, 6653
12	GND	—	
18	Program	—	Programming pulse input
19	V_{DD}	—	Chip V+ supply, normally tied to V_{CC}
20	$\overline{E}_1$	L	Strobe line, latches both address lines and, for 6654, Chip enable $\overline{E}_2$
21	$\overline{S}$	L	Chip select line, must be low for valid data out
22	A_9	—	Additional address line for 6653
	$\overline{E}_2$	L	Chip enable line, latched by Chip enable $\overline{E}_1$ on 6654
24	V_{CC}	—	Output buffer +V Supply

READ CYCLE TIMING



*A_9 IM6653 only, $\overline{E}_2$ IM6654 only

READ MODE OPERATION

In a typical READ operation address lines and chip enable $\overline{E}_2$* are latched by the falling edge of chip enable $\overline{E}_1$ (T = 0). Valid data appears at the outputs one access time (TELQV) later, provided level-sensitive chip select line $\overline{S}$ is low (T = 3). Data remains valid until either $\overline{E}_1$ or $\overline{S}$ returns to a high level (T = 4). Outputs are then forced to a high-Z state.

Address lines and $\overline{E}_2$ must be valid one setup time before (TAVEL), and one hold time after (TELAX), the falling edge of $\overline{E}_1$ starting the read cycle. Before becoming valid, Q output lines become active (T = 2). The Q output lines return to a high-Z state one output disable time (TE_1HQZ) after any rising edge on $\overline{E}_1$ or $\overline{S}$.

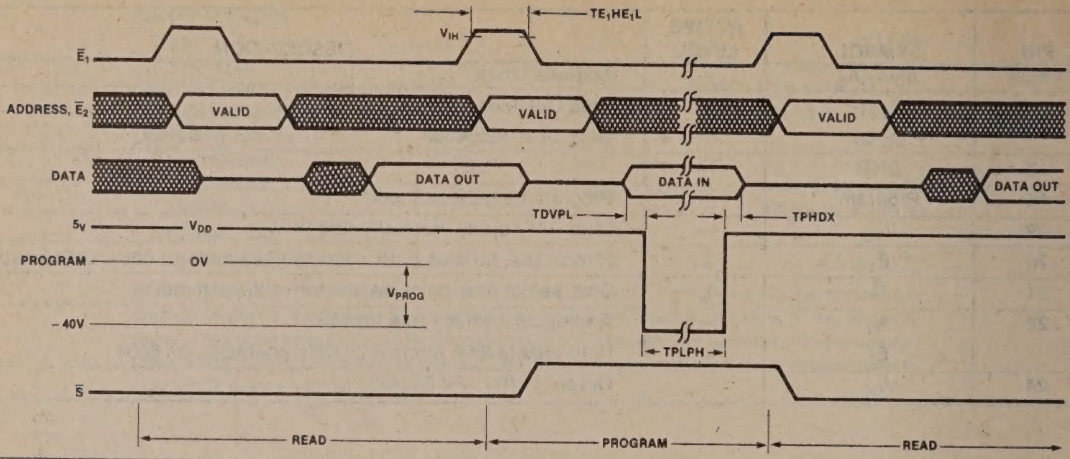
The program line remains high throughout the READ cycle.

Chip enable line $\overline{E}_1$ must remain high one minimum positive pulse width (TEHEL) before the next cycle can begin.

FUNCTION TABLE

TIME	INPUTS				OUTPUTS	NOTES
REF	Ē1	Ē2*	S̄	A	Q	
−1	H	X	X	X	Z	DEVICE INACTIVE
0	↓	L	X	V	Z	CYCLE BEGINS; ADDRESSES, $\overline{E}_2$ LATCHED*
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY
2	L	X	L	X	A	OUTPUTS ACTIVE UNDER CONTROL OF $\overline{E}_1$, $\overline{S}$
3	L	X	L	X	V	OUTPUTS VALID AFTER ACCESS TIME
4	↑	X	L	X	V	READ COMPLETE
5	H	X	X	X	Z	CYCLE ENDS (SAME AS -1)

READ AND PROGRAM CYCLES



DC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 5\%$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pin Load Current	I_{PROG}			80	100	mA
Programming Pulse Amplitude	V_{PROG}		38	40	42	V
V_{CC} Current	I_{CC}			0.1	5	mA
V_{DD} Current	I_{DD}			40	100	
Address Input High Voltage	V_{IHA}		$V_{DD} - 2.0$			V
Address Input Low Voltage	V_{ILA}				0.8	
Data Input High Voltage	V_{IH}		$V_{DD} - 2.0$			
Data Input Low Voltage	V_{IL}				0.8	

AC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 5\%$, $T_A = 25°$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pulse Width	TPLPH	$t_{rise} = t_{fall} = 5\mu s$	18	20	22	ms
Program Pulse Duty Cycle					75%	
Data Setup Time	TDVPL		9			μS
Data Hold Time	TPHDX		9			
Strobe Pulse Width	TE₁HE₁L		150			ns
Address Setup Time	TAVE₁L		0			
Address Hold Time	TE₁LE₁X		100			
Access Time	TE₁LQV				1000	

PROGRAM MODE OPERATION

Initially, all 4096 bits of the EPROM are in the logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode for all EPROMs, V_{CC} and V_{DD} are tied together to a +5V operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at $V_{DD} - 2V$ minimum. Low logic levels must be set at GND + .8V maximum. Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select (S̄) pins are set high. The address is latched by the downward edge on the strobe line (Ē₁). During valid DATA IN time, the PROGRAM pin is pulsed from V_{DD} to −40V. This pulse initiates the programming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. PULSE RISE AND FALL TIMES MUST NOT BE FASTER THAN 5μs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences, such as the Intersil 6920 CMOS EPROM programmer, is recommended.

PROGRAMMING SYSTEM CHARACTERISTICS

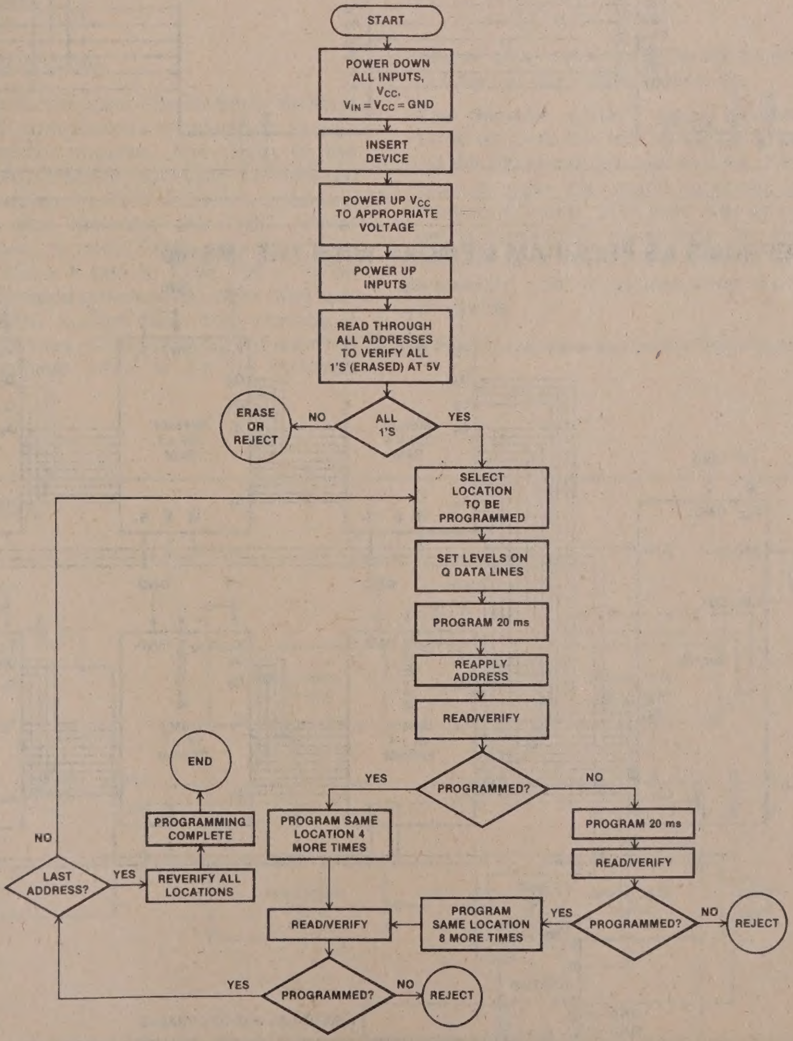
1. During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
2. The programming pin is driven from V_{DD} to −40 volts (±2V) by pulses of 20 milliseconds duration. These pulses should be applied in the sequence shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
3. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins. Both "A" (10V) and non "A" EPROMs are programmed at V_{CC}, V_{DD} of 5V ±5%.
4. Programming is to be done at room temperature.

ERASING PROCEDURE

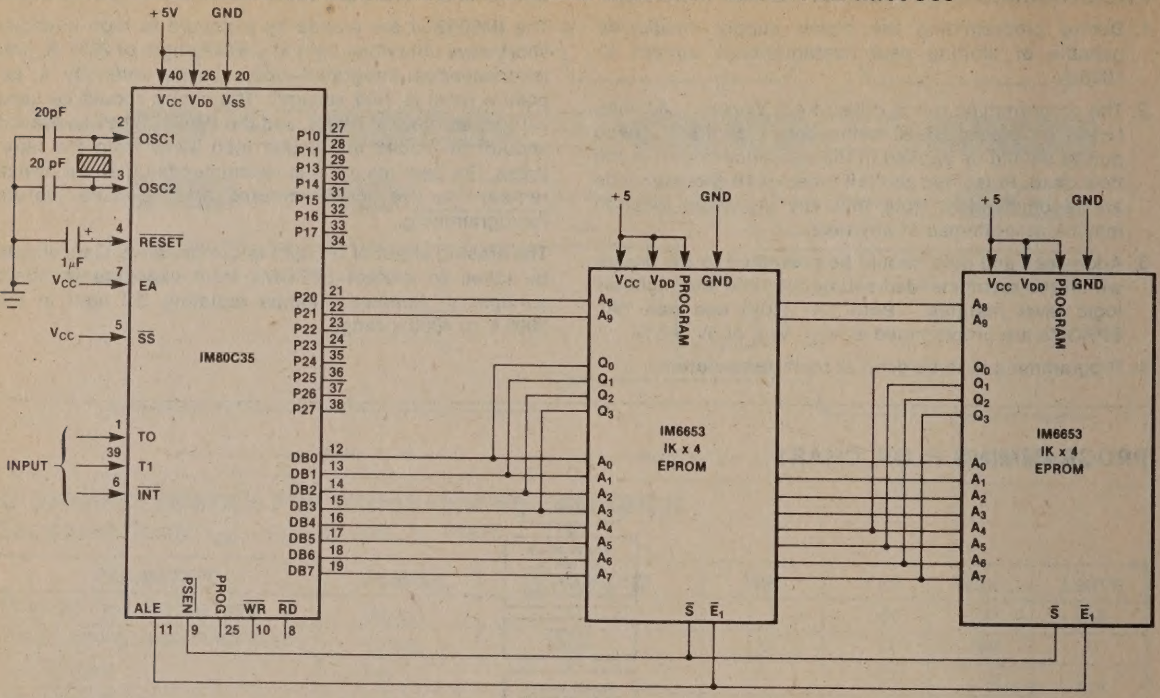
The IM6653/54 are erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537 Å. The recommended integrated dose (i.e.,UV intensity x exposure time) is 10W sec/cm^2. The lamps should be used without short-wave filters, and the IM6653/54 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before reprogramming.

The erasing effect of UV light is cummulative. Care should be taken to protect EPROMs from exposure to direct sunlight or florescent lamps radiating UV light in the 2000Å to 4000Å range.

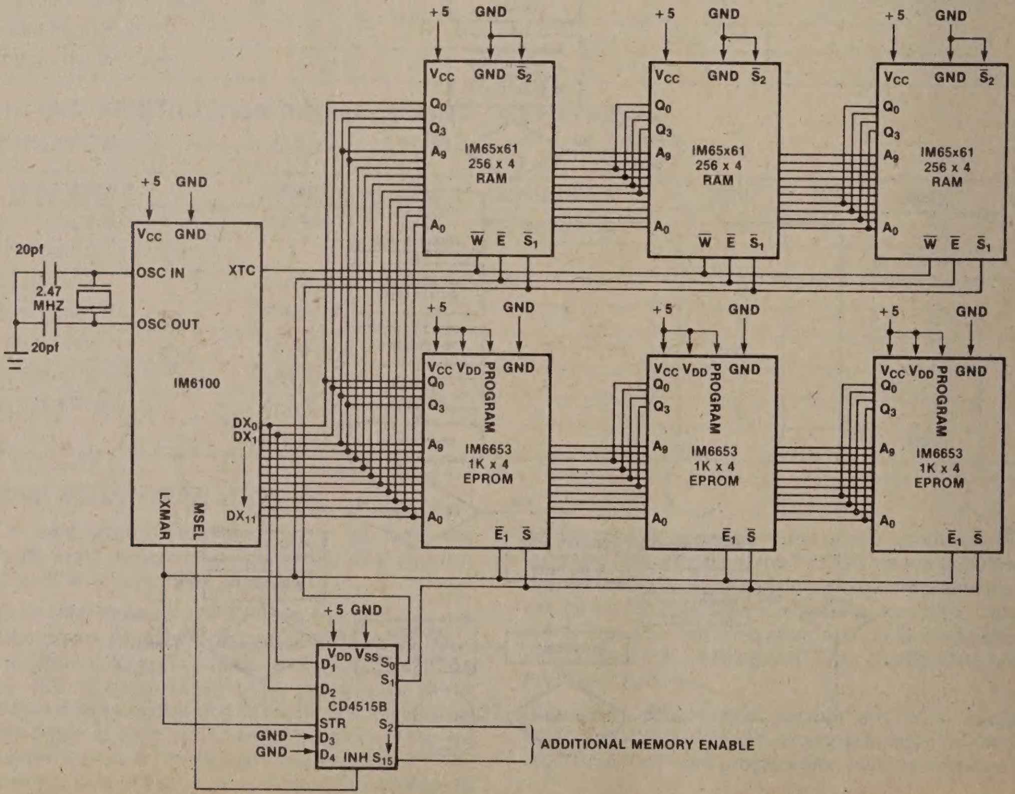
PROGRAMMING FLOW CHART


START
POWER DOWN ALL INPUTS, Vcc, VIN = Vcc = GND
INSERT DEVICE
POWER UP Vcc TO APPROPRIATE VOLTAGE
POWER UP INPUTS
READ THROUGH ALL ADDRESSES TO VERIFY ALL 1'S (ERASED) AT 5V
ALL 1'S
NO
ERASE OR REJECT
YES
SELECT LOCATION TO BE PROGRAMMED
SET LEVELS ON Q DATA LINES
PROGRAM 20 ms
REAPPLY ADDRESS
READ/VERIFY
PROGRAMMED?
YES
NO
PROGRAM SAME LOCATION 4 MORE TIMES
PROGRAM 20 ms
READ/VERIFY
PROGRAMMED?
YES
NO
REJECT
PROGRAM SAME LOCATION 8 MORE TIMES
READ/VERIFY
PROGRAMMED?
YES
NO
REJECT
LAST ADDRESS?
NO
YES
REVERIFY ALL LOCATIONS
PROGRAMMING COMPLETE
END

IM6653 CMOS EPROMS AS EXTERNAL PROGRAM MEMORY WITH THE IM80C35


+5V
GND
40
26
20
V_{CC} V_{DD} V_{SS}
20pF
2
OSC1
20 pF
3
OSC2
4
RESET
1µF
7
V_{CC}
EA
5
V_{CC}
SS
IM80C35
P10 P11 P13 P14 P15 P16 P17
27 28 29 30 31 32 33 34
P20 P21 P22 P23 P24 P25 P26 P27
21 22 23 24 35 36 37 38
INPUT
1 TO
39 T1
6 INT
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
12 13 14 15 16 17 18 19
ALE 11
PSEN 9
PROG 25
WR 10
RD 8
+5
GND
V_{CC} V_{DD} PROGRAM GND
A_8 A_9
Q_0 Q_1 Q_2 Q_3
IM6653
IK x 4
EPROM
A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7
S E_1

IM6653 CMOS EPROMS AS PROGRAM MEMORY WITH THE IM6100


+5
GND
V_{CC} GND S_2
Q_0
Q_3
A_9
IM65x61
256 x 4
RAM
A_0
W E S_1
+5 GND
V_{CC} GND
20pf
OSC IN
XTC
2.47 MHZ
OSC OUT
20pf
IM6100
DX_0
DX_1
DX_{11}
LXMAR
MSEL
V_{CC} V_{DD} PROGRAM GND
IM6653
1K x 4
EPROM
E_1 S
+5 GND
V_{DD} V_{SS}
D_1 S_0
S_1
D_2
CD4515B
STR S_2
GND D_3
GND D_4 INH S_{15}
ADDITIONAL MEMORY ENABLE

6801
CMOS Microcomputer Family Sampler Kit
6960 — Sampler PC Board

FEATURES

- **Provides fast and simple exposure to the IM6100 Microcomputer Family**
- **Very inexpensive**
- **Interfaces to any ASCII RS-232 or 20mA terminal**
- **Includes ODT monitor in ROM**
  - **Includes tape punch and load routines in ROM**
- **All CMOS components**
- **Executes PDP®-8/E instruction set**
- **Sampler PC board available — easy to use and inexpensive**

GENERAL DESCRIPTION

The 6801 CMOS Microcomputer Family Sampler Kit is a complete set of LSI components necessary to build a general purpose microcomputer. The heart of the Sampler Kit is the IM6100 Microprocessor. The IM6100 Microprocessor executes the PDP-8/E instruction set. The Sampler Kit also includes the ODT (Octal Debugging Technique) monitor ROM (1K x 12), three RAM's (each with 256 x 4 bits to form 256 x 12 bit words), the Programmable Interface Element (IM6101) and a UART (IM6403). A significant cost savings is realized through purchase of the Sampler Kit over the single quantity purchase price of all the included components.

In addition, a printed circuit board is available to simplify construction of the Sampler system (part number 6960). The Sampler board is laid out so that it may interface with both RS-232C and 20mA current loop. The user may enhance the capability of the Sampler system with the addition of sixteen optional SSI packages, assorted switches, and LEDs (optional parts not included). The added capabilities include:

- Address/Bus Display
- Status Display
- Single Instruction Step
- Single Cycle Step
- 12-Bit Input Port
- 12-Bit Output Port

Any of these options can easily be added when desired, but are not required for operation.

The Sampler system, when teamed with any ASCII terminal, gives the user an easy to understand, yet powerful IM6100 Microcomputer system. The ODT Monitor program provides the control necessary to display and alter memory contents, start execution at a particular address, set a breakpoint, manipulate the registers, or search memory for a value. If the terminal has tape punch/read capability, built-in routines allow loading and saving of programs.

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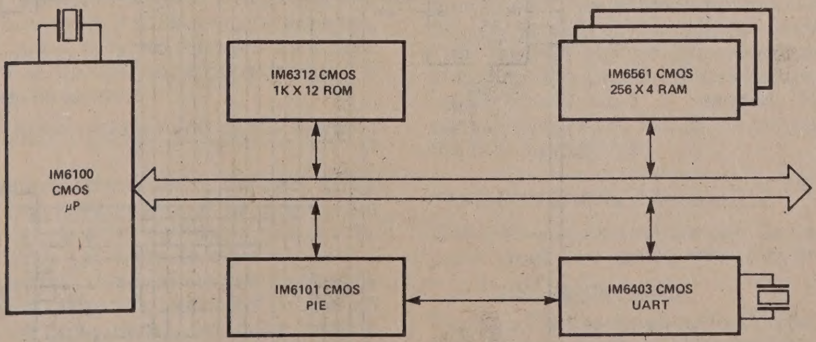
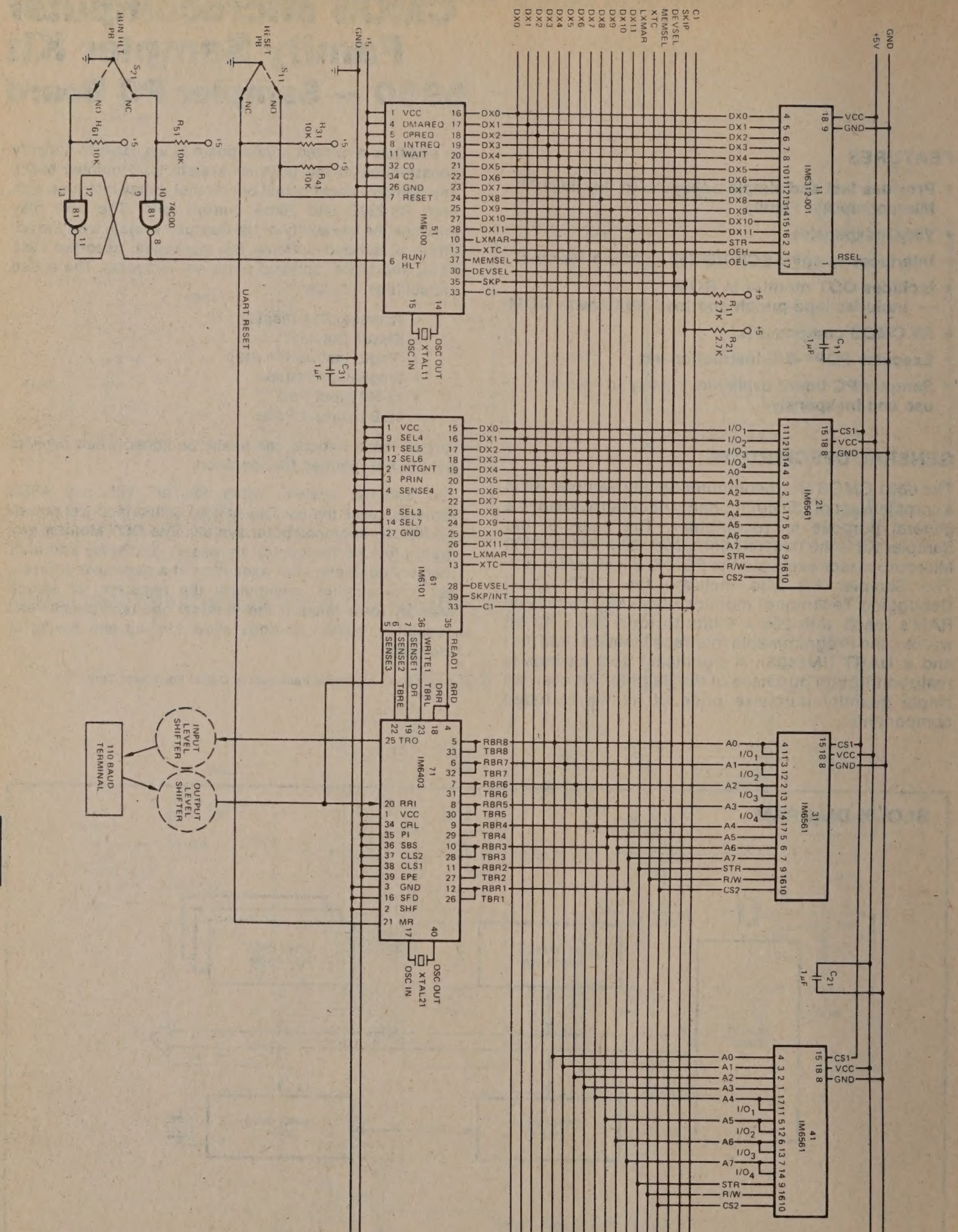
BLOCK DIAGRAM




RUN/HLT PB
S21
NO
NC
R61 10K
+5
RESET PB
S11
R51 10K
R31 10K
R41 10K
74C00
81
UART RESET
GND
+5
C1
SKIP
DEVSEL
MEMSEL
XTC
LXMAR
DX11
DX10
DX9
DX8
DX7
DX6
DX5
DX4
DX3
DX2
DX1
DX0
GND
+5V
IM6100
51
1 VCC
4 DMAREQ
5 CPREQ
8 INTREQ
11 WAIT
32 C0
34 C2
26 GND
7 RESET
6 RUN/HLT
LXMAR
XTC
MEMSEL
DEVSEL
SKP
C1
XTAL11
OSC OUT
OSC IN
C31 1μF
IM6312-001
11
VCC
GND
RSEL
STR
OEH
OEL
R11 2.7K
R21 2.7K
C11 1μF
IM6101
61
1 VCC
9 SEL4
11 SEL5
12 SEL6
2 INTGNT
3 PRIN
4 SENSE4
8 SEL3
14 SEL7
27 GND
SKP/INT
READ1
WRITE1
SENSE1
SENSE2
SENSE3
RRD
DRR
TBRL
DR
TBRE
IM6561
21
I/O1
I/O2
I/O3
I/O4
A0
A1
A2
A3
A4
A5
A6
A7
STR
R/W
CS2
CS1
IM6403
71
25 TRO
20 RRI
1 VCC
34 CRL
35 PI
36 SBS
37 CLS2
38 CLS1
39 EPE
3 GND
16 SFD
2 SHF
21 MR
RBR8
TBR8
RBR7
TBR7
RBR6
TBR6
RBR5
TBR5
RBR4
TBR4
RBR3
TBR3
RBR2
TBR2
RBR1
TBR1
XTAL21
OSC OUT
OSC IN
INPUT LEVEL SHIFTER
OUTPUT LEVEL SHIFTER
110 BAUD TERMINAL
IM6561
31
IM6561
41
C21 1μF

System Hookup Diagram

ODT MONITOR COMMANDS

ODT commands consist of a control character or an octal number followed by a control character. The commands may be typed in any time the terminal is idle and are executed as soon as the control character is typed.

BINARY LOAD COMMAND

L — Load from the tape reader

Typing an L will load binary tape from a reader. The checksum will be printed out on the terminal following the end of the load. Printed out checksum should be 0000 for a proper load.

EXAMINE/MODIFY COMMANDS

/ (slash) — Opens a location

Typing an octal number nnnn followed by a slash causes the location whose address is nnnn to be opened. When a location is opened, its content is printed out as an octal number. Typing a slash not preceded by a number causes the most recently opened location to be reopened.

(carriage return) — Closes a location

When a location is open, typing an octal number, nnnn, followed by a carriage return causes the contents of the location to be changed to the number nnnn and closes the location. Typing a carriage return not preceded by a number causes the location to be closed without modifying its contents.

(line feed) — Closes and opens next

When a location is open, typing a line feed causes the location to be closed and the next memory location (that with an address one higher than the current location) to be opened. The address of the new location will be typed out, followed by a slash, followed by the contents of the new location. Typing an octal number, nnnn, before typing the line feed causes the contents of the old location to be changed to nnnn.

← (back arrow) — Closes location and opens indirect reference

When a location is open, typing a back arrow causes the location to be closed. The contents of the location are then treated as an indirect reference. That is, the content of the old location is taken as an address, and the new location is opened. If while a location is open, an octal number, nnnn, is typed followed by a back arrow, the content of the open location is changed to nnnn and proceeds as above.

↑ (up arrow) — Closes location and opens memory reference

This command behaves identically to the back arrow command except that the contents of the location are treated as a memory reference instruction, and it is the location referenced by that instruction that is opened. The location opened is that immediately referenced by the instruction. If the instruction is indirect (bit 3 is set to 1), then typing the up arrow only opens the location containing the pointer to the operand of the instruction. To open the effective location referred to by an indirect instruction, type an up arrow (memory reference) followed by a back arrow (indirection).

PROGRAM CONTROL AND BREAKPOINT COMMANDS

G — Go to

Typing an octal number, nnnn, followed by a G causes ODT to begin executing the program stored in memory, starting at location nnnn.

B — Breakpoint

Typing an octal number, nnnn, followed by a B causes ODT to set a breakpoint at location nnnn. Typing a B without preceding it by a number causes the current breakpoint to be cleared.

C — Continue

After a breakpoint causes control to return to ODT from a user program, typing C causes the program to resume execution where it left off.

A — Examine/modify accumulator, link, MQ

Three consecutive ODT RAM locations are reserved for storing the contents of the AC, link and MQ registers when a breakpoint occurs. When execution of the user's program resumes (via the G or C command), the contents of these registers are restored from these locations. Typing A causes the first of these locations, containing the contents of the AC, to be opened.

WORD SEARCH COMMANDS

M — Open search mask, lower bound, upper bound

The mask, lower bound and upper bound for word searches are kept in that order in three consecutive reserved ODT locations. The first of these locations, the mask, can be opened by typing M.

W — Word search command

Typing an octal number, nnnn, followed by a W causes a word search to occur. The search proceeds as follows: The number, nnnn, that was typed is masked and remembered as the quantity which is being searched for. (The operation of masking is to take the bitwise boolean AND of the given word with the contents of the mask word.) Then each location, beginning with the location whose address is stored in the lower bound word, is masked and compared with the quantity being searched for. If the two are equal, then the address of the word, followed by a slash and the (unmasked) contents of the word are printed out. Then the next location is examined and so on until (and including) the location whose address is stored in the upper bound word is reached. The word search command does not change the contents of any word in the user's programs.

TAPE PUNCHING COMMANDS

The following commands can be used to punch out paper tapes that can be read in by the BIN loader.

T — Punch leader/trailer

Typing a T will cause about four inches of leader/trailer tape (tape punched with 200 octal) to be punched. The T command also causes the accumulated checksum to be set to zero (cleared).

P — Punch tape

Typing an octal number, nnnn, followed by a semicolon (;) followed by a second octal number, mmmm, followed by a P, causes a tape corresponding to the contents of the block of memory beginning at location nnnn and ending at location mmmm to be punched. No checksum is punched at the end of the block so that several blocks can be punched together with one inclusive checksum.

E — Punch checksum and trailer

Typing an E will cause the accumulated checksum to be punched, followed by about four inches of leader/trailer tape. The checksum is also reset to zero (cleared).

SAMPLER ODT EXAMPLE

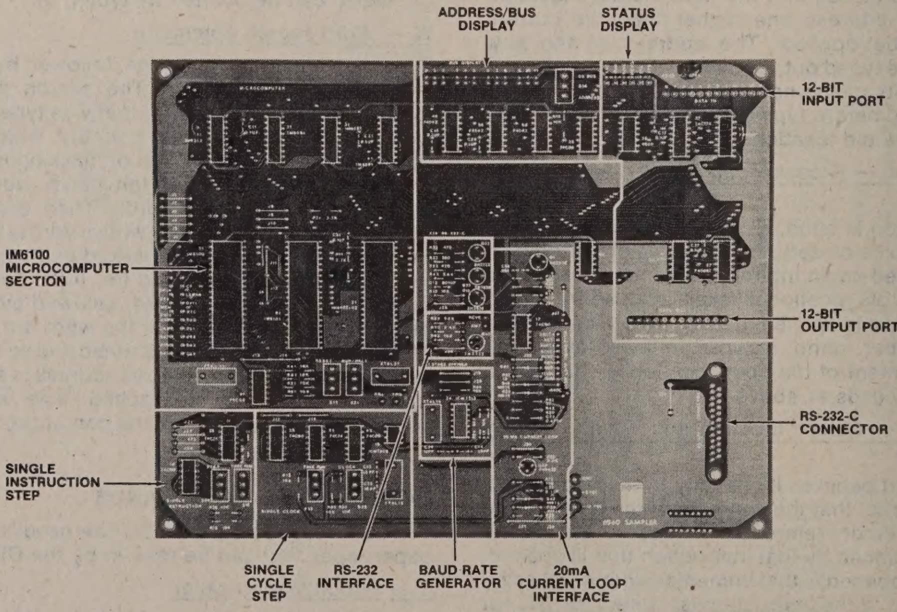
Say that the simple program

```
300  7001  START, IAC
301  7440         SZA
302  5300         JMP START
303  7402         HLT
```

is stored in memory. Then the following might be the result of a session with ODT. (Note: The underlined portion is typed by the user, and the remainder is typed by the computer. The symbol CR stands for carriage return, and LF stands for line feed.)

```
300/7001 LF        LIST THE PROGRAM IN OCTAL
301/7440 LF        LF MEANS — SHOW NEXT
                   LOCATION
302/5300 LF
303/7400 7402 CR   LOCATION 303 IS WRONG —
                   CHANGE AND VERIFY
/ 7402 CR
A1764 0LF          ACCUMULATOR CONTAINS
                   GARBAGE, MAKE IT ZERO
0050/0001 0CR      SAME FOR LINK
302B               SET BREAKPOINT AT JMP START
300G               EXECUTE PROGRAM (GO)
0302 (0001         BREAKPOINT OCCURS;
                   ACCUMULATOR HAS BEEN
                   INCREMENTED
7774C              CONTINUE PAST BREAKPOINT
                   1 + 7774 TIMES
0302 (7776         BREAKPOINT OCCURS; AC=7776
303B               RESET BREAKPOINT TO HLT
                   INSTRUCTION
C                  CONTINUE
0303 (0000         PROGRAM STOPS WHEN AC
                   REACHES 0 AGAIN
A0000LF            EXAMINE AC AND LINK
0050/0001 CR       LINK HAS BEEN CHANGED BY
                   OVERFLOW
B                  CLEAR ALL BREAKPOINTS
```

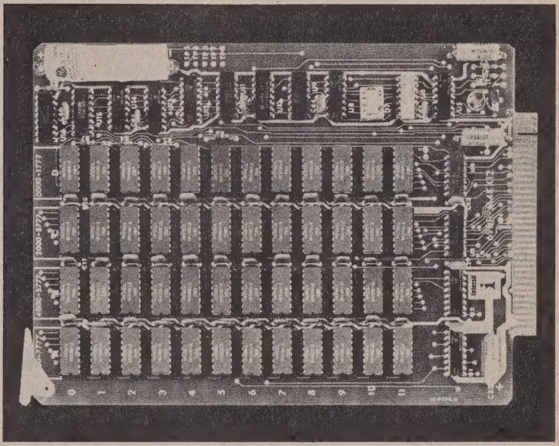
6960 — SAMPLER PC BOARD LAYOUT


ADDRESS/BUS DISPLAY
STATUS DISPLAY
12-BIT INPUT PORT
IM6100 MICROCOMPUTER SECTION
12-BIT OUTPUT PORT
RS-232-C CONNECTOR
SINGLE INSTRUCTION STEP
SINGLE CYCLE STEP
RS-232 INTERFACE
BAUD RATE GENERATOR
20mA CURRENT LOOP INTERFACE

6901
4K x 12 CMOS Memory Module with Battery Back-up

FEATURES

- Rechargeable battery back-up
- Data Retention of up to 80 days
- Low power
- Compact size
- Low cost
- Switch selectable field addressing

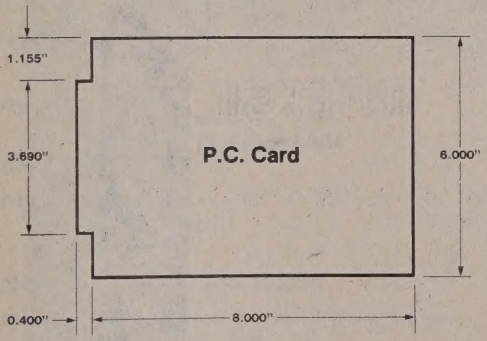


GENERAL DESCRIPTION

The 6901 CMOS memory module provides the Intercept System with 4096 twelve-bit words of battery-backed-up memory. The module retains its data when system power is off; an on-board rechargeable NiCad battery insures and uninterrupted power supply to the CMOS RAMs for up to 80 days. When system power is on, the NiCad batteries are recharged for future use. Up to eight 6901 modules may be installed in a system by setting on-board switches so each module responds to a unique memory field.

SPECIFICATIONS

PHYSICAL CHARACTERISTICS



ELECTRICAL CHARACTERISTICS

DC Power Requirements:	150mA at +5V typical, 500mA maximum

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature Range:	0°C to 50°C
Operating Humidity Range:	10% to 90% (no condensation)

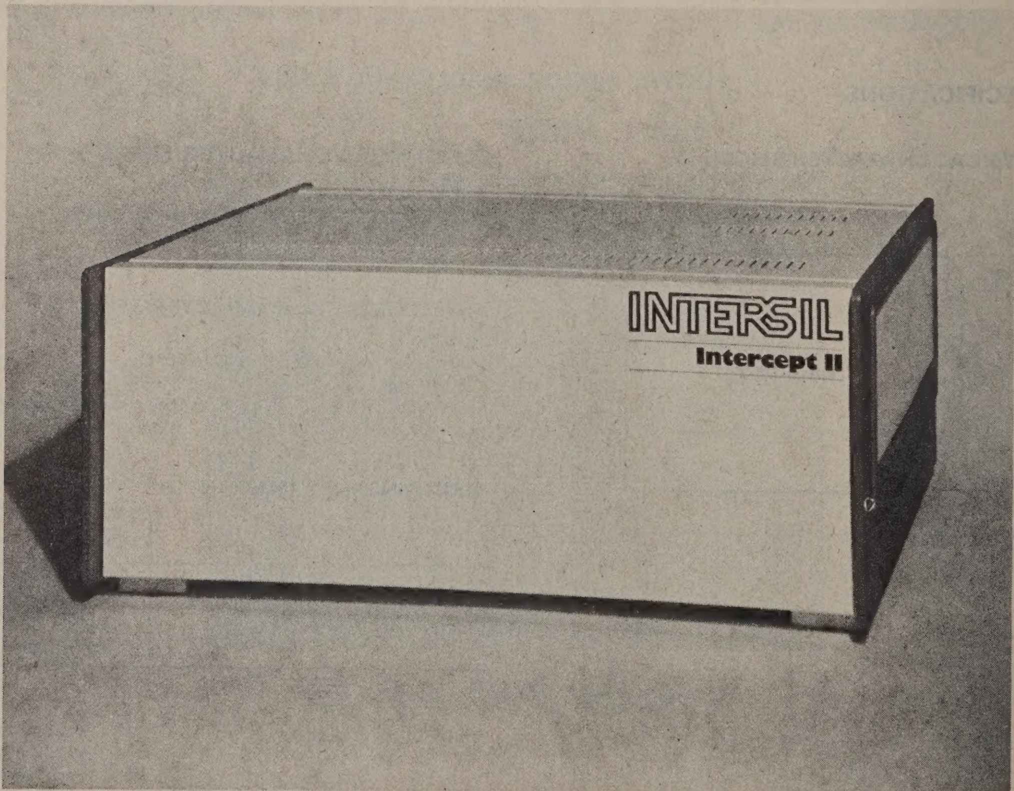
ORDERING INFORMATION

	Order No.
Module:	6901-M4KX12
Documentation:	6998 LSI-8 User's Manual

6910
Intercept II Microcomputer Development System

FEATURES:
- Low Cost
- Powerful PDP®-8/e compatible processor
- Compact size
- Modular design
- 4K CMOS memory
- Bus supports easy I/O expansion
- Resident firmware monitor/debugger
- Large available software base
- Low power
- Supports Interrupt and DMA operations
- Real Time Clock

HARDWARE FEATURES:
- 4K Words of Resident Memory (RAM) for Program and Data Storage
- Expandable to 32K Words of Memory
- Resident Control Panel Memory (2K Words ROM and 256 Words RAM)
  - Transparent to User Programs
  - Floppy Disk Operating System Bootstrap
  - Up to 8 Simultaneous Breakpoints
  - Highly Interactive Debugging Facilities
- Two High Speed Serial I/O Ports with Multiple Baud Rates (14 Different Baud Rates)
  - User Selectable
  - RS232C Standard on Both I/O Ports
  - Either Port May be Strapped for 20mA Current Loop
- Compact Size (21.5cm x 51.4cm x 47.8cm)
- Extensive Hardware Options
  - Memory Modules
  - Wirewrap Module
  - Extender Module
  - Teletype Relay Module
  - Dual Floppy Disk System



Intercept II

GENERAL DESCRIPTION

Intercept II is a general purpose microcomputer development system for Intersil's IM6100 Microprocessor components. It consists of two PC boards, a Central Processor Module Board, and a Memory Module Board. The Central Processor Module Board includes the IM6100 CPU, resident memory (2K words ROM and 256 words RAM) for firmware storage, memory extension capability and two channels of serial I/O ports. The Memory Module Board includes 4K words (4K x 12) of CMOS RAM for the user's PROGRAM/DATA storage.

All of the system control features, such as an extended memory control (for memory expansion up to 32K words); a real time clock, and DMA control functions are resident in the system. The resident firmware eliminates the need for the hardware control panel.

The Intercept II has a compact enclosure size of 21.5cm x 51.4cm x 47.8cm (HxWxD), and it allows a total of twelve PC boards in the system. Because two cards come with the system, the user may add up to ten additional cards to Intercpt II.

Standardized board sizes and uniform bus definitions ensure compatibility with previous Intercept designs. Intersil offers hardware and software support including 4K memory modules, floppy disk hardware, Intercept Floppy Disk Operating System, Parallel I/O Module, etc.

HARDWARE SPECIFICATIONS

Word Size

Host Processor: Intersil IM6100
Data: 12-bits
Instruction: 12 or 24-bits

Memory Size

Main Memory

RAM: 4K expandable to 32K (CMOS with battery backup standard)

Control Panel Memory (2K words x 12)

RAM: 256 words (resident on CPU — monitor uses 128 words)
ROM: 2K (resident on CPU — used by monitor)

System Clock

Crystal Controlled: 3.3MHz typical

Serial I/O Interfaces

(RS232C is standard on both I/O ports; either port may be strapped for 20mA current loop operation)

Primary Port

Baud Rates: 50/75/110/134.5/150/200/300/600/1200/1800/2400/4800/9600/19200

Any of these 14 different baud rates is switch selectable.

Code Format: 10 level code

Parity: None

Secondary Port

Same as Primary Port except: Baud Rate is console controlled or software programmable (50/75/110/134.5/150/200/300/600/1200/1800/2400/4800/9600/38400.)

Includes four RS232C supervisory signals (two inputs and two outputs)

Interrupt

Single level, maskable, prioritized, vectored or polled.

Direct Memory Access

Standard IM6102 DMA, bus control implemented on CPU module — transfer rate user controlled (direct or user controlled block DMA) — typically greater than 2MHz.

Real Time Clock

4MHz DEC compatible

Physical Characteristics

Dimensions: (HxWxD) 21.5cm x 51.4cm x 47.8cm

Weight: 15.9KG

Electrical Characteristics

DC Power Supply	Power Supply Current	Basic System Current Requirements (Typ.)
+5V ± 5%	6 A	.8 A
+12V ± 5%	1.0A	.1 A
-12V ± 5%	1.0A	.1 A

AC Power Requirements

Frequency: 50 or 60 Hz
Voltage: 115 or 230V AC
Power: 175W max.

Environmental Characteristics

Operating Temperature: 0°C to 50°C

Humidity: 10% to 90% (no condensation)

Equipment Supplied (Basic System)

- 6912 Central Processor Module
- 6901 4K CMOS RAM Module
- Finished Cabinet with Power Supplies, Card Cage and Fan
- Intercept User's Manual
- Two RS232C and One 20mA Current Loop Cable
- AC Power Line Cord

Hardware Options

6901 — M4K x 12
4K Nonvolatile CMOS Memory Module

6905 — WIRE WRAP
Wirewrap Module for User Interfaces to Intercept

6906 — EXTEND
Extender Module

6909 — RELAY
Teletype Paper Tape Reader Remote Control Module

6914 — IFDC
Single Board Floppy Disk Controller

6915 — M32K x 12
32K NMOS Dynamic RAM Board

6917 — Parallel I/O
REMDAC Compatible 8 bit Parallel I/O

6970 — IFDOS Dual Floppy Disk Unit
Dual Floppy Disk System with Single Board Interface to Intercept Bus

SOFTWARE/FIRMWARE SPECIFICATIONS

Resident Control Panel Firmware Monitor

Capabilities

- Accumulator, Link, Program Counter, Instruction/Data Fields, MQ, Switch Register-examine/modify
- Control Panel and Main Memory-examine/modify
- Single Instruction, Breakpoint, Snapshot and Trace-debugging and modify
- IFDOS and OS/8 Operating System Bootstraps
- Memory Bit Pattern/Word Search
- Binary Paper Tape Input/Output Commands (Loader/Punch)
- DEC PDP-8/E® Console Terminal, HLT, OSR Emulation
- Up to 8 Simultaneous Breakpoints

Features

- High Speed Resident Operation
- Highly Interactive Debugging Facilities
- Completely Transparent to User Programs

SOFTWARE OPTIONS

Compatible with OS/8 Operating System Licensed from Digital Equipment Corp. Including:

- System Utilities PIP, DIRECT, FOTP, BUILD
- Editors Edit, TECO
- Assemblers PAL 8, SABR, MACREL, RALF.
- High Level Languages FOCAL, FORTRAN II, FORTRAN IV BASIC

— Intercept Floppy Disk Operating System (IFDOS)

- File System Controls Floppy Disk Input/Output Operation
- Keyboard Monitor for Communication Between User and IFDOS
- Text Editor Creates and Modifies ASCII Text at the Terminal
- PAL Assembler translates IM6100 assembly language to machine language in one or two passes. About 400 symbols can be created in standard system of 4K word memory. 1024 more symbols can be created with each 4K additional RAM with maximum symbol limit of up to 4095 symbols.
- Numerous Switch Options and Pseudo-operations for Assembly and Listing Control
- Numerous Utility Programs for File Manipulation and Disk Dumping and Copying
- Disk Diagnostic Programs
- Supplied with IFDOS in a Standard Floppy Diskette and Listing
- Required Hardware:
  - — Intercept System
  - — ASCII Terminal
  - — 6970-IFDOS Dual Floppy Disk Unit

6981 — FOPAL III

PAL III Fortran Cross Assembler

- Written in Standard Fortran IV
- Card Deck Based
- Can Use with Any Fortran Compiler and a Card Reader (such as 029 Reader)

6982 — FOCAL®8

(Order No. 6982-IS-LFOCA) — See Note 1

- Interactive Algebraic Language
- Extensive Math. Functions
- Easy to Learn High Level Language
- Needs only 4K Words of RAM
- Paper Tape Based

- Multitude of Programs available through Digital Equipment Corporation User's Society, Including:
  - — Utilities
  - — Languages
  - — Applications

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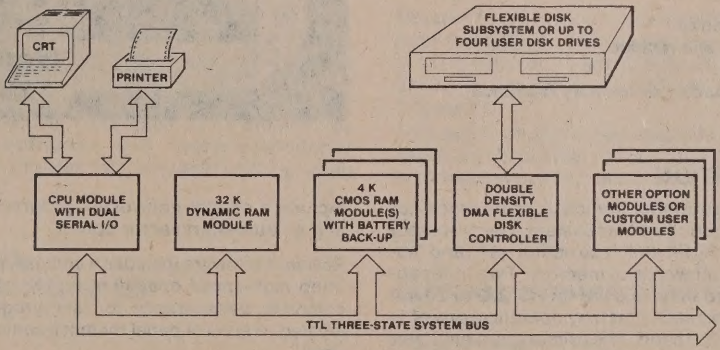

CRT
PRINTER
FLEXIBLE DISK SUBSYSTEM OR UP TO FOUR USER DISK DRIVES
CPU MODULE WITH DUAL SERIAL I/O
32 K DYNAMIC RAM MODULE
4 K CMOS RAM MODULE(S) WITH BATTERY BACK-UP
DOUBLE DENSITY DMA FLEXIBLE DISK CONTROLLER
OTHER OPTION MODULES OR CUSTOM USER MODULES
TTL THREE-STATE SYSTEM BUS

INTERCEPT SYSTEM BLOCK DIAGRAM

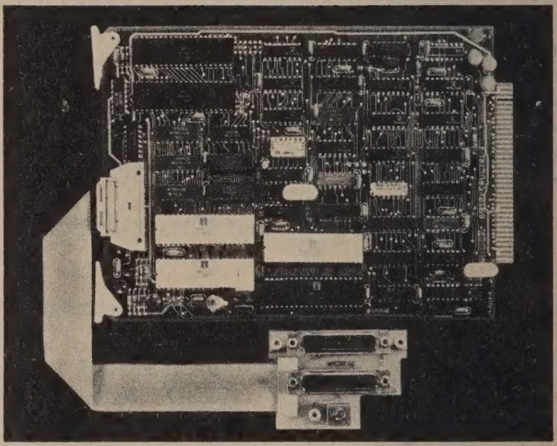
6912
CPU with Dual Serial I/O

HARDWARE FEATURES

- **Powerful PDP®-8/e instruction set**
- **Two independent serial ports (RS-232 or 20mA current loop)**
- **14 selectable baud rates**
- **Resident memory extension controller**
- **Real-time clock**
- **Auto-start vector option**
- **Single compact board**
- **Low power**
- **Reliable**

FIRMWARE FEATURES

- **Resident debugger**
- **Memory/register examination/modification**
- **Up to 8 breakpoints**
- **Single instruction in RAM or ROM**
- **Single instruction trace in RAM or ROM**
- **Snapshot mode**
- **Operating system bootstrap**
- **Memory search/search and replace**
- **Paper tape load/punch**
- **Effective address calculation for memory reference instructions**



GENERAL DESCRIPTION

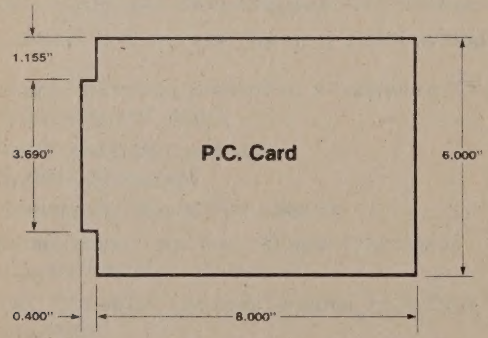
The 6912 CPU module is a powerful, compact central processor for the Intercept OEM Microcomputer System. The processor executes the powerful PDP®-8/3 instruction set, and addresses up to 3K twelve bit words of memory. Two independent serial ports on board may be used for RS-232 or 20 mA current loop operation and each port may operate at one of 14 rates between 50 and 19,200 baud. The primary port emulates the PDP®-8/e terminal interface. Other hardware features include a crystal-controlled, programmable real-time clock and an auto-start vector option.

Resident firmware includes a concise, powerful debugger featuring high-speed operation, highly interactive structure, and complete transparency to user programs. The firmware is located in control panel memory so no user memory space is used.

®PDP-8 is a registered trademark of Digital Equipment Corp.

SPECIFICATIONS

PHYSICAL CHARACTERISTICS:



ELECTRICAL CHARACTERISTICS

DC Power Requirements:	400mA (typ.) at +5V	1.2A max.
	2mA (typ.) at +12V	4mA max.
	2mA (typ.) at -12V	4mA max.

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature Range:	0°C to 50°C
Operating Humidity Range:	10% to 90% (no condensation)

ORDERING INFORMATION

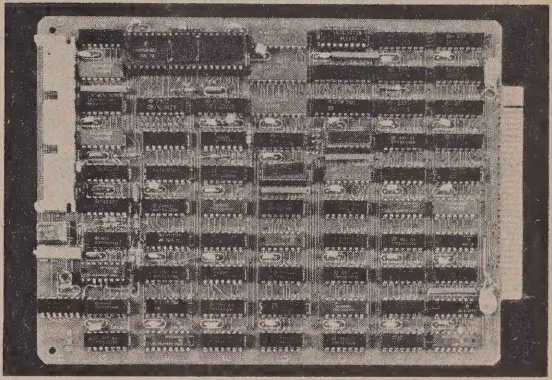
	Order No.
Module:	6912 Intercept CPU
Ribbon Cable Serial I/O Assembly:	6925 Serial I/O Assy
Documentation:	6998 LSI-8 User's Manual

INTERSIL

6914 IFDC
Double Density DMA Floppy Disk Controller

FEATURES

- Single or double density
- Up to 8 industry standard flexible disk drives
- Single or double sided
- Industry standard or non-standard formats for custom applications
- Automatic address verification
- Automatic CRC on address and data
- Variable stepping rates
- DMA transfer of data in 8-bit or 12-bit modes
- Capability to format diskettes
- Full diagnostics



GENERAL DESCRIPTION

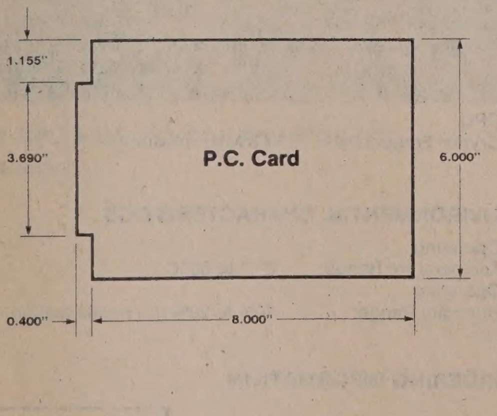
The Intercept floppy disk controller board provides inexpensive, reliable, compact mass storage for the Intercept system. It uses a single bus slot and controls up to eight diskette drives with a maximum sub-system capacity of 10 megabytes. Many types of drives can be used, including single or double-density and single or double-sided. Data integrity is ensured by employing address verification and cyclic redundancy checking (CRC). Data transfer rate is maximized by using direct memory access.

Because the 6914 uses an advanced LSI controller, the user has great flexibility in choosing the drive and/or format best suited to the application. Stepping rates, sector sizes, and sector positions can be varied to increase both data capacity and throughput.

For users wishing pre-packaged disk drive sub-systems, Intersil offers the 6975 Dual Floppy Disk Drives, consisting of two enclosed drives with power supply, cables, and documentation.

SPECIFICATIONS

PHYSICAL CHARACTERISTICS



ELECTRICAL CHARACTERISTICS

DC Power Requirements	
Voltage:	+5V ± .25V +12V ± .6V
Current:	1.3A nominal, 2.2A max. 10mA nominal, 35mA max.

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature Range:	0°C to 50°C
Operating Humidity Range:	10% to 90% (no condensation)

ORDERING INFORMATION

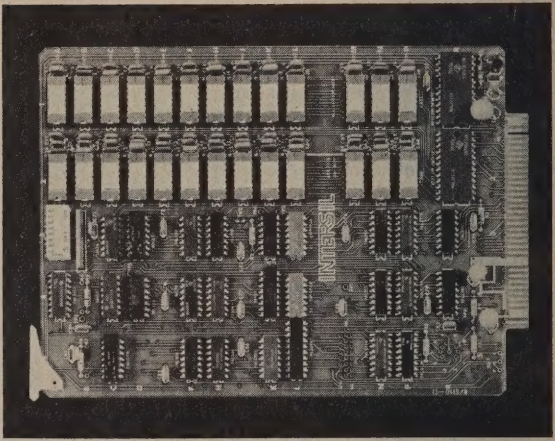
	Order No.
Module:	6914-IFDC
Flexible Disk Drive Cable:	6926-IFDCCABLEASSY
Dual Flexible Disk Drives:	6975-IFDD
Documentation:	6998 LSI-8 User's Manual

INTERSIL

6915
32K x 12 RAM Board

FEATURES

- **32K x 12 full memory complement for the Intercept System**
- **Many options for custom applications**
- **Low power**
- **Small parts count for reliability**
- **Compact size**



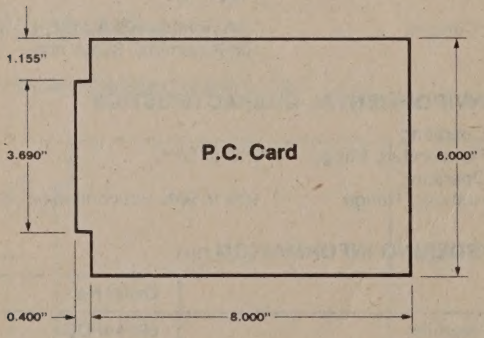
GENERAL DESCRIPTION

The 6915 memory module provides 32K twelve-bit words of memory for the Intercept system, using NMOS dynamic RAMs for low cost and small parts count. All necessary refresh circuitry is resident on the module.

The module has a host of options for custom application flexibility. These include selective 4K field disable for mixed memory (e.g., dynamic and battery-backed) systems, RAM inhibit for shadowing ROM over RAM, and parity storage for off-board error checking.

SPECIFICATIONS

PHYSICAL CHARACTERISTICS



ELECTRICAL CHARACTERISTICS

DC Power
Requirements: 560mA (typ.) at +5V, 1.2A max.
160mA (typ.) at +12V, 840A max.
10mA (typ.) at -12V, 12A max.

CPU
Crystal Frequency: 3.3 MHz maximum

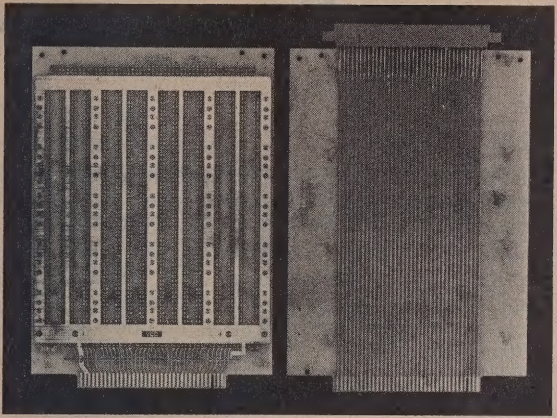
ENVIRONMENTAL CHARACTERISTICS

Operating
Temperature Range: 0°C to 50°C
Operating
Humidity Range: 10% to 90% (no condensation)

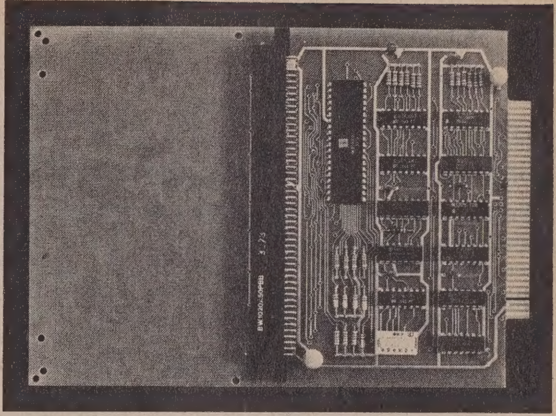
ORDERING INFORMATION

	Order No.
Module:	6915-M32KX12
Documentation:	6998 LSI-8 User's Manual

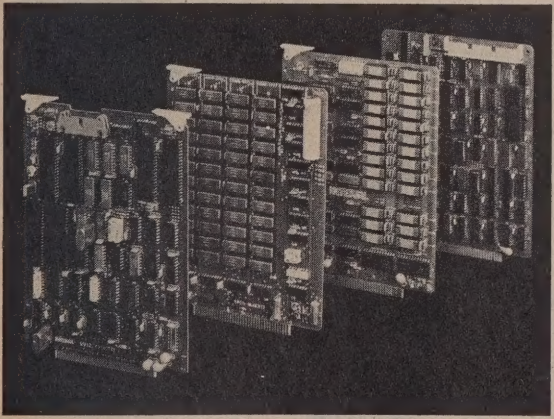
ADDITIONAL MODULES



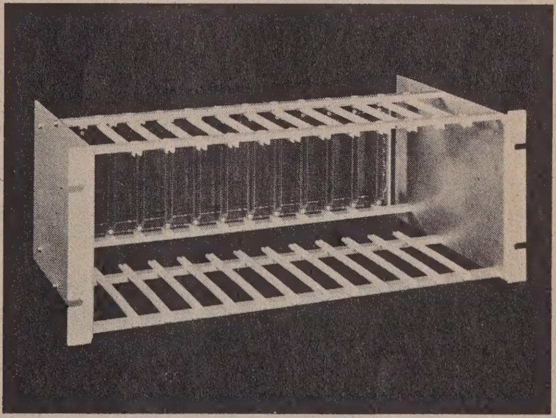
6905 — Wirewrap-Universal Wirewrap Module (Left)
6906 — Extend-Card Extender Module (Right)



6917 — REMDAC Compatible 8-bit Parallel I/O



6912-CPU, 6901-M4k x 12, 6915 M32k x 12, 6914-IFDC



Intercept II Card Cage without Power Supply.

6920
CMOS EPROM Programmer

FEATURES

- **Programs Intersil's IM6653/54 CMOS EPROM**
- **Software controlled for ease of expandability**
- **IM6100 microprocessor based**
  - **16K bit buffer memory**
- **Serial data communication**
  - **20 mA current loop**
  - **RS232C**
  - **110 to 9600 selectable baud rate**
- **Three operating modes**
  - **Master with CRT terminal or Teletype®**
  - **Slave with development system**
  - **Stand-alone for duplicating EPROMS**
- **Self contained D/A controlled power supplies**
- **Check sum error detection**

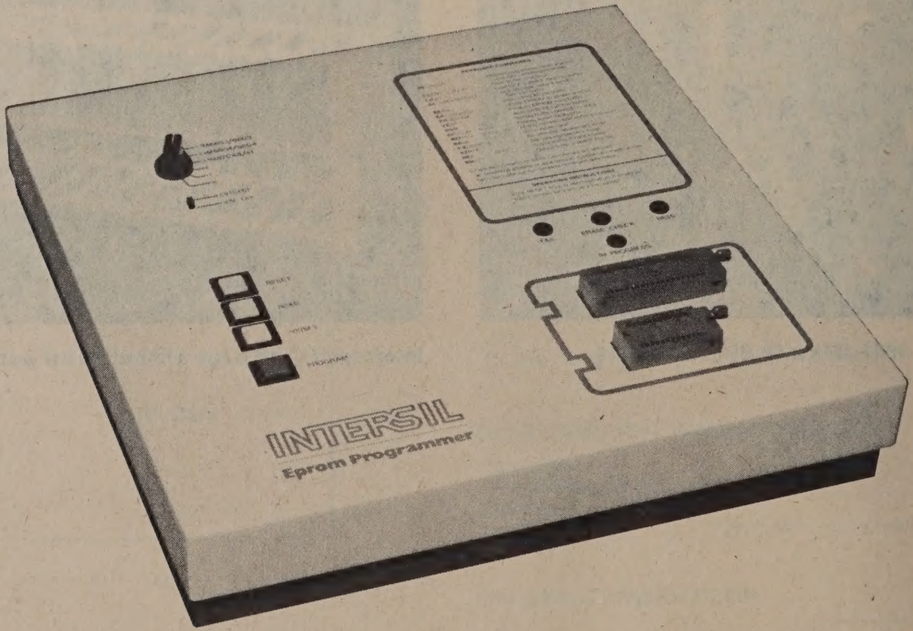
®Teletype is a registered trademark of Teletype Corp.

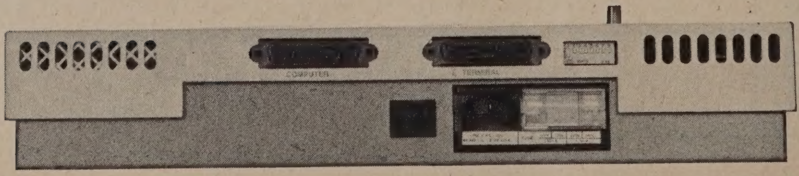
DESCRIPTION

Intersil's 6920 CMOS EPROM programmer is a multi-mode cost effective instrument used to program Intersil's IM6653/54 family of CMOS EPROMs.

The 6920 is microprocessor controlled, allowing the programmer to operate as a stand-alone unit, for duplicating EPROMs; a master, for operation with CRT terminals or Teletype®; or a slave, for operation with a software development system or minicomputer.

Serial data communication is used for all command and data transfers with a 20 mA current loop and an RS232C interface provided. Check sum error detection is employed for data validation.





8

INTERSIL

PRELIMINARY
Specifications Subject To Change Without Notice

6941/42 CONCEPT-48 8048 Tutorial Unit-Development Tool

FEATURES

- **Executes 8048 Code**
- **Compact Single Board Design Fits Into 3-Ring Binder**
- **Operated by Standard 9 Volt Battery or calculator type wall-mount power supply**
- **Tactile Feedback Keypad**
- **7 Character LCD Display**
- **44-Pin Edge Connector for System Expansion**
- **3 MHz Execution of User Program**
- **Optional I/O Expansion with IM82C43**
- **2K ROM-based Monitor includes Load, Run, Debug, Modify, and Save Commands**
- **Single Step Operation**
- **8 Breakpoints — User Selectable**
- **6941 CONCEPT-48 Tutorial Unit: Includes 256 Bytes of External Program Memory and 64 Bytes of Internal Data Memory**
- **6942 CONCEPT-48 Development Tool: Includes 2K Bytes of External Program Memory, 64 Bytes of Internal and 256 Bytes of External Data Memory, on board negative voltage converter, and RS-232/TTY Serial Interface with Selectable Baud Rates of 50 thru 19200**
- **Detailed User's Manual**

GENERAL DESCRIPTION

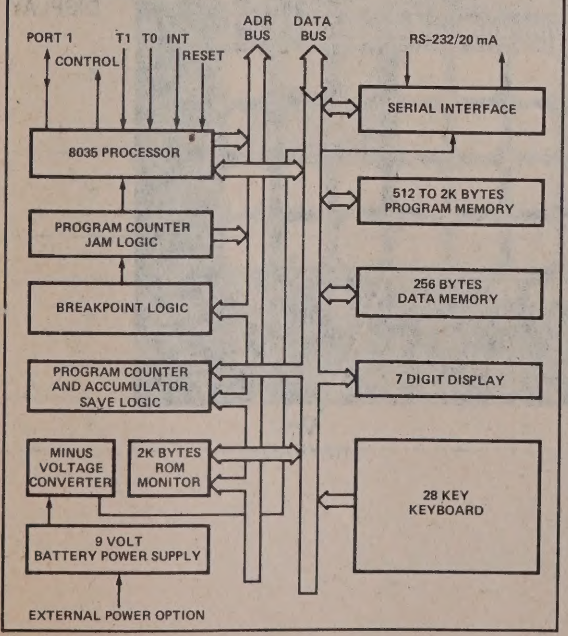
The CONCEPT-48 is a versatile single board system designed to execute and debug software written for the 8048 single-chip microcomputer family. Object code may be down-loaded from a development system via the serial interface or entered in hex via the 28-position keypad. A 7-digit LCD display provides information about current operations and input commands.

Programs are executed at 3 MHz using an 8035 with external memory. Valuable debugging tools include 8 breakpoints and the ability to single step. Debugging is further enhanced by the ability to examine and/or modify registers, ports, flags, or counter. These capabilities also simplify user exploration of the 8048 family architecture.

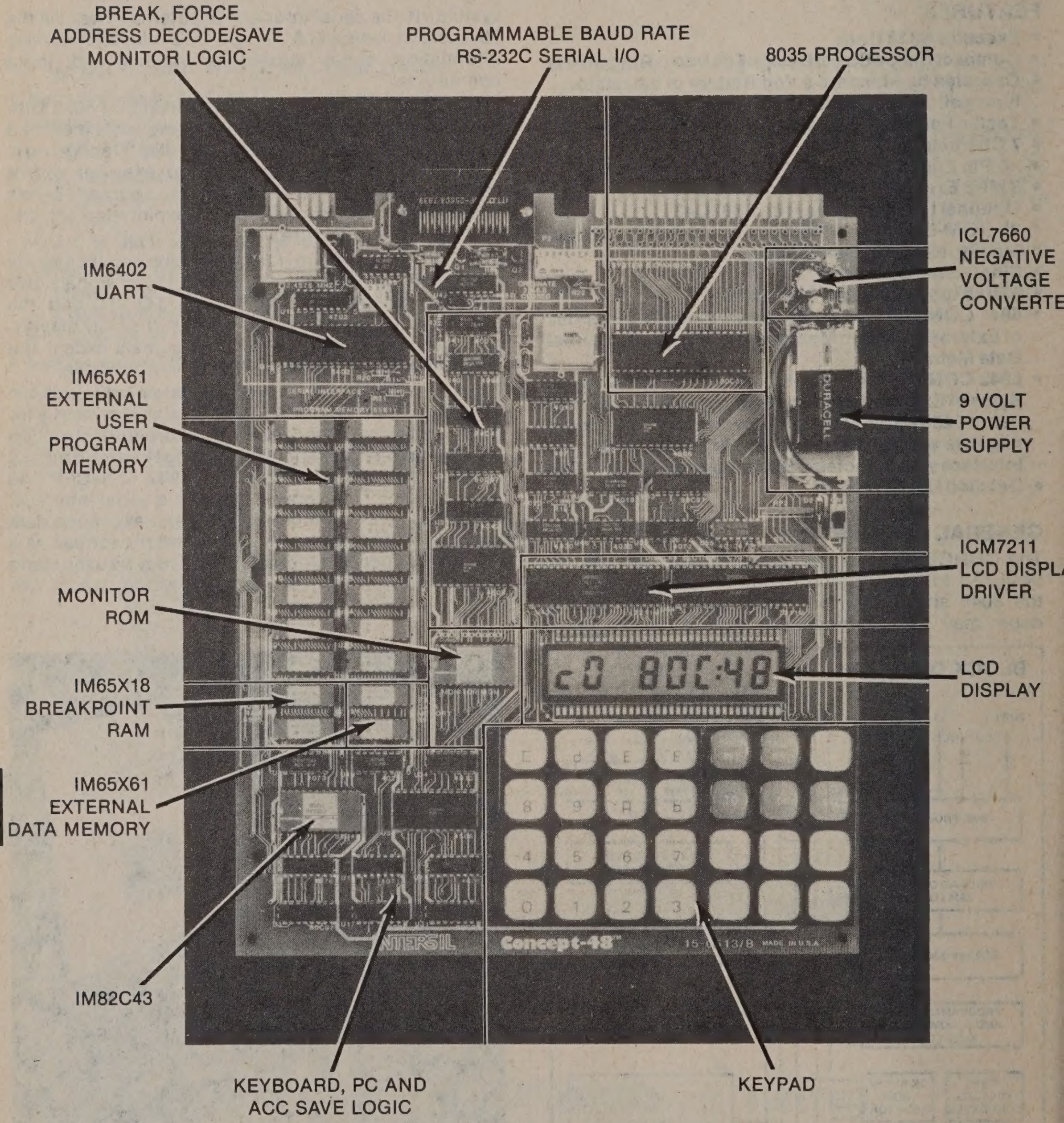
The CONCEPT-48 provides expansion capabilities via a 44-pin edge connector. The unbuffered signals give software access to all of Port I, TO, TI, and the timer/counter, as well as the keypad, the LCD display, and the optional UART. All 8048 signals except the crystal inputs, SS, EA, and P24-P27 are available.

The CONCEPT-48 is available in two configurations. The 6941 CONCEPT-48 Tutorial version is primarily for learning the use of the 8048 architecture and instruction set. The battery operation and notebook card size make it ideal for classroom use. The 6942 CONCEPT-48 Development Tool version includes a serial interface, expanded program memory (2K), and expanded data memory (256), and is intended primarily for use as a limited product development tool. It may be used stand alone, or with any development system which can assemble 8048 program code.

BLOCK DIAGRAM


PORT 1
T1
T0
INT
CONTROL
RESET
ADR BUS
DATA BUS
RS-232/20 mA
SERIAL INTERFACE
8035 PROCESSOR
512 TO 2K BYTES PROGRAM MEMORY
PROGRAM COUNTER JAM LOGIC
256 BYTES DATA MEMORY
BREAKPOINT LOGIC
PROGRAM COUNTER AND ACCUMULATOR SAVE LOGIC
7 DIGIT DISPLAY
MINUS VOLTAGE CONVERTER
2K BYTES ROM MONITOR
28 KEY KEYBOARD
9 VOLT BATTERY POWER SUPPLY
EXTERNAL POWER OPTION

INTERSIL
Concept-48
Microcomputer Development System
User's Manual
INTERSIL Concept-48

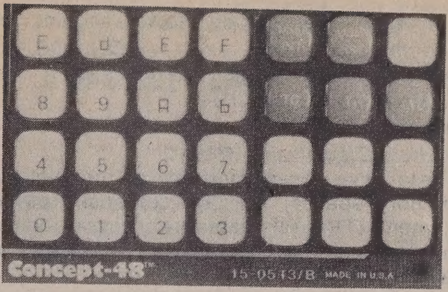

BREAK, FORCE ADDRESS DECODE/SAVE MONITOR LOGIC
PROGRAMMABLE BAUD RATE RS-232C SERIAL I/O
8035 PROCESSOR
IM6402 UART
ICL7660 NEGATIVE VOLTAGE CONVERTE
IM65X61 EXTERNAL USER PROGRAM MEMORY
9 VOLT POWER SUPPLY
DURACELL
ICM7211 LCD DISPL DRIVER
MONITOR ROM
LCD DISPLAY
c0 8DC:48
IM65X18 BREAKPOINT RAM
IM65X61 EXTERNAL DATA MEMORY
IM82C43
INTERSIL
Concept-48™
KEYBOARD, PC AND ACC SAVE LOGIC
KEYPAD

6941/42 CONCEPT-48

KEYPAD DESCRIPTION

The keypad monitor firmware of the CONCEPT-48 resides in a ROM and operates the keypad, display and peripheral functions of the system.

The keypad consists of two portions. The 16-key portion is doubly-labeled with the hexadecimal numbers 0-9, A-F, and a function abbreviation above. The 12-key portion is labeled with a single function. Keys take effect on the upstroke or release, except MON, BOOT, U0, T0, T1 and CANCEL which are all actuated during the key press.



COMMAND SUMMARY

GROUP	KEY	PARAMETERS	DESCRIPTION
1	BOOT	—	Reset and initialize System
	MON	—	Exit program execution
2	CANCEL	—	Aborts command input
	CLOSE	—	Ends command parameter input
	EXAM	—	Delimits and extends command input
3	PMEM	Addr EXAM	Program memory access
	DMEM	Addr EXAM	Data memory access
	RB0	Reg # EXAM	Register bank 0 access
	RB1	Reg # EXAM	Register bank 1 access
	XMEM	Addr EXAM	External data memory access
	PORT	Port # EXAM	Port access
	XPORT	Port # EXAM	External port access
	BKPT	Bkpt # EXAM	Breakpoint access (CCC is clear)
	DUMP	ST. Addr EXAM End Addr CLOSE	Dump programs in hex format
	LIST	St. Addr EXAM End Addr CLOSE	Dump programs in list format
4	ACC	—	Accumulator access
	PSW	—	Program status word access
	PC	—	Program counter access
	TCNT	—	Timer/counter access
	FLAGS	—	Flag word access
5	GO	—	Enter program execution
	STEP	—	Single instruction execution
6	USER RST	—	User reset
	USER INT	—	User interrupt
	T0	—	Test pin 0
	T1	—	Test pin 1
	U0	—	User key signal
7	LOAD	—	Program load from serial port

The keys have been divided into seven logical groups:

1. *Terminate execution, return to MONITOR.*
   Other function keys may now be used.
2. *Command entry modifier.*
   Used to delimit, or otherwise control input.
3. *Address Display and Modify.*
   These keys access portions of the system (e.g., memory spaces) that are composed of multiple elements. These elements are accessed individually, or in groups, using individual addresses or address ranges.
4. *Single Element Display and Modify.*
   These keys are used to access portions of the system that are normally defined as single elements.
5. *Enter User Program Execution.*
   Execution will be stopped by reaching a breakpoint, receiving a BREAK character from the serial port, actuating MON or BOOT. STEP stops after every instruction.
6. *Direct Inputs to Processor During User Program Execution.*
   These keys allow the user to input signals to the microprocessor during real time execution of a program. Some of these are disabled during monitor execution, and others are just not used by the monitor. None have any effect during monitor execution.
7. *Load Program Memory from Serial Port.*
   This function key loads a program, or portion of a program, into the user program memory from the serial port. The program must be in Hex format.

   Incidentally, the serial port on CONCEPT-48 can be configured for 14 baud rates. An ICL7660 voltage converter chip generates the negative voltage required for RS-232 from the 9-volt supply. An IM6402 UART handles the data communication.

The use of the keys is facilitated somewhat by prompts from the liguid crystal display. The LCD display is a seven segment, eight-character type and is driven by two ICM7211M devices. The leftmost position on the display has been provided a custom set of characters. By selecting a subset of seven segments from the 14 driver lines of two-digit addresses, a new set of characters has been created. This set includes the numerics 0-9, and contains alphabetic characters in a mixture of upper and lower case:

A, b, c, C, d, E, F, G, h, H, L, P, r, o, ?, blank

These have been used for display prompts. The decimal points in the display are driven by an output port and reflect its contents.

INTERFACING THE CONCEPT-48 WITH OTHER SYSTEMS

The CONCEPT-48 was designed for ease of program entry via the keypad. However in many cases, users with access to other equipment will find it advantageous to use the serial I/O facility of the 6942 to interface ASCII terminals, PROM programmers, or host computers used as part of an 8048 development system. For example, the source program can be stored on discs and the assembled object code down-loaded in hex format to the CONCEPT-48. Later the debugged code may be uploaded to the development system/programmer.

CONCEPT-48 may also be connected to a teletype® or CRT terminal. Programs may be entered on the terminal, which is connected to the CONCEPT-48. However, to use all the powerful features of the monitor program, the keypad must be used.

Another application interfaces the CONCEPT-48 to a PROM programmer. Programs may be transmitted to the CONCEPT-48 from the programmer for debugging and modification, then transmitted back to the programmer to begin programming a new PROM.

Users of the INTERCEPT development systems can assemble 8048 code using the ASM X48 cross assembler, and transmit object modules to the CONCEPT-48 for debugging, hardware simulation, etc.

®Teletype is a registered trademark of Teletype, Inc.

6950 INTERCEPT JR. MICROCOMPUTER TUTORIAL SYSTEM

FEATURES

- **Battery operation**
- **Executes PDP®-8/E instruction set**
- **Keyboard monitor program in ROM**
- **8 seven-segment displays for address and data**
- **256 words of non-volatile RAM**
- **3 expansion sockets for optional modules**
- **Fully assembled and tested**
- **Low cost**
- **Tutorial manual included**

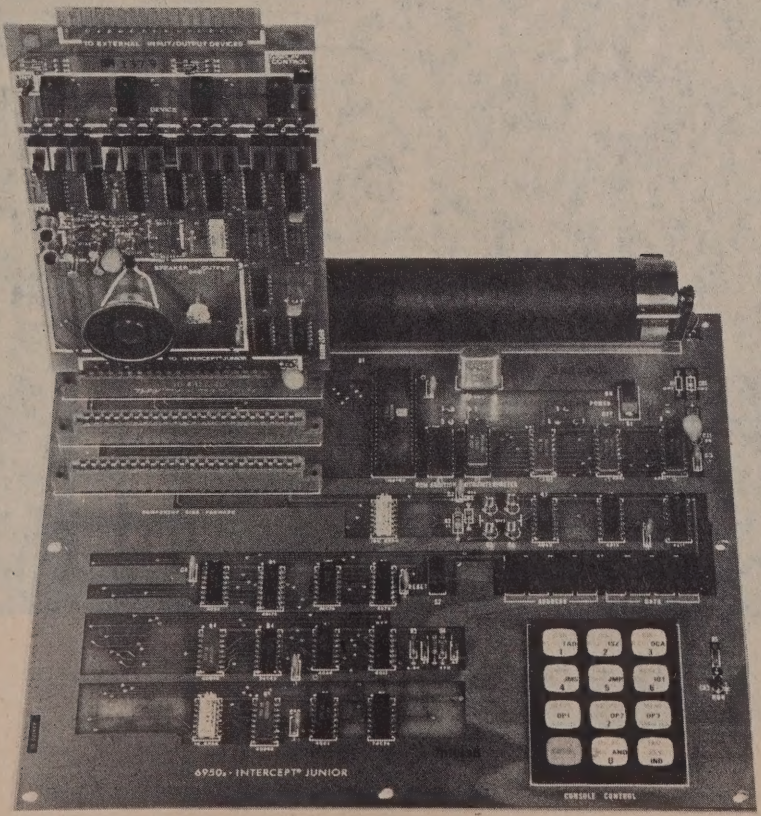
®Registered trademark of Digital Equipment Corp.

GENERAL DESCRIPTION

A practical exposure to the Intersil IM6100 microprocessor, RAMs, P/ROMs, and Input/Output interfacing can be achieved with the INTERCEPT JR. TUTORIAL SYSTEM and the owners handbook supplied.

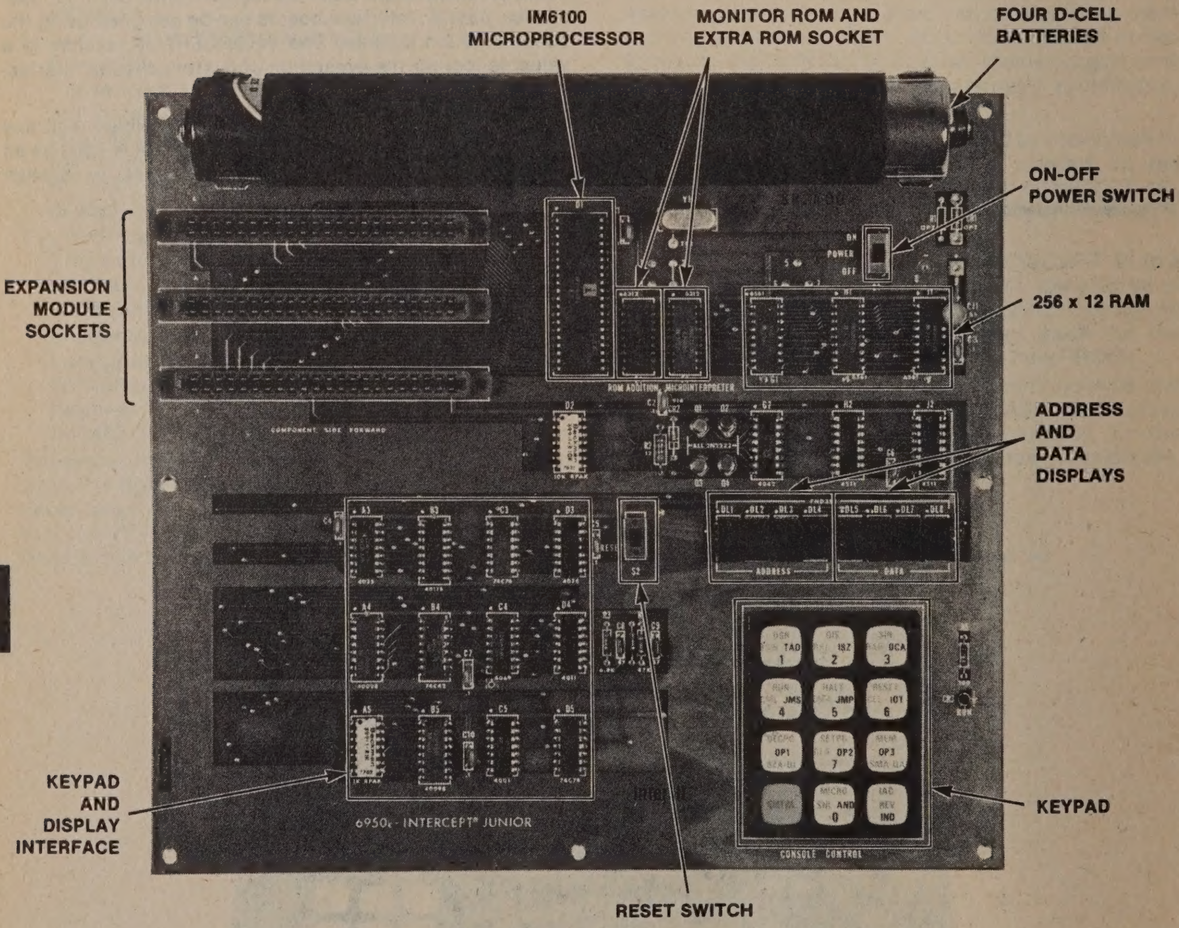
This fully assembled and factory tested system is battery operated. Moreover, it executes the same instruction set as the popular PDP® -8E minicomputer, thus providing a rich supply of proven software. The INTERCEPT JR. is designed with a modular concept to enable the user to purchase only those modules which meet his requirements. Or, if the user wishes, custom interface boards can be designed using the documentation supplied The INTERCEPT JR. system is a valuable tool for the evaluation of custom circuits interfaced to an IM6100 microcomputer system.

With its simplicity of design, broad capabilities, and low cost, the INTERCEPT JR. TUTORIAL SYSTEM is ideal as an educational tool for the student, hobbyist, or system designer.


TO EXTERNAL INPUT/OUTPUT DEVICES
CONTROL
DEVICE
SPEAKER OUTPUT
TO INTERCEPT JUNIOR
ADDRESS
DATA
TAD 1
ISZ 2
DCA 3
JMS 4
JMP 5
IOT 6
OP1
OP2 7
OP3
AND 0
IND
6950A - INTERCEPT® JUNIOR
CONSOLE CONTROL

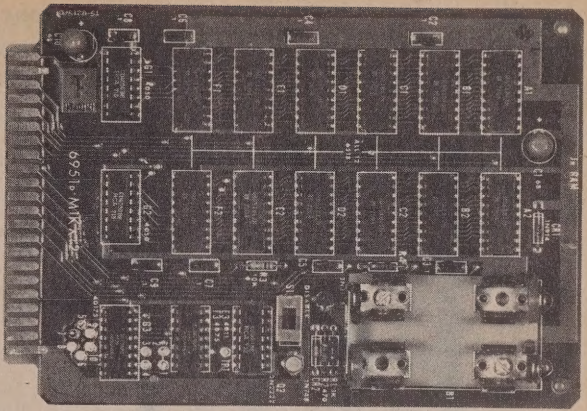
6950-INTERCEPT JR. MODULE

INTERCEPT JR. provides an all CMOS computer on a 10″ × 11″ double sided PC board. A multiple function calculator type keypad in concert with a 1024 × 12 CMOS ROM (IM6312) monitor provides control functions, a serial bootstrap loader, as well as the INTERCEPT JR. MICROINTERPRETER. Memory addresses and data are displayed in octal on two four-digit LED displays. The IM6100 CMOS microprocessor interfaces via a three-state address/data bus to 256 × 12 CMOS RAM. Four D-cell batteries allow for non-volatile RAM and battery operation of the entire system. External terminals permit the user to provide a 5 volt power source. A socket is provided for evaluation of a user generated CMOS ROM (IM6312/12A). Three edge connectors with 44 pins on 0.156″ pin-to-pin spacing are provided for expansion using the optional boards available.


IM6100 MICROPROCESSOR
MONITOR ROM AND EXTRA ROM SOCKET
FOUR D-CELL BATTERIES
ON-OFF POWER SWITCH
EXPANSION MODULE SOCKETS
256 x 12 RAM
ADDRESS AND DATA DISPLAYS
KEYPAD AND DISPLAY INTERFACE
KEYPAD
RESET SWITCH
6950 - INTERCEPT® JUNIOR
CONSOLE CONTROL

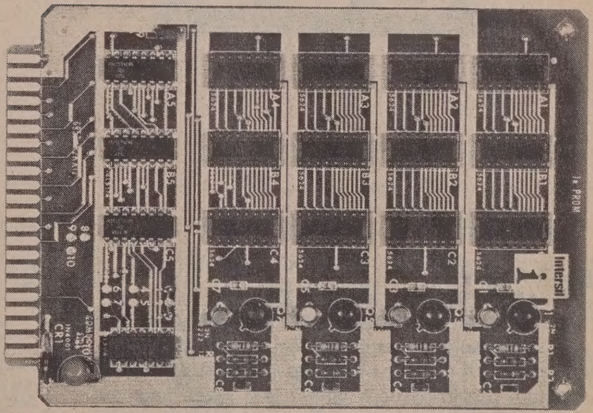
6951-M1KX12
JR. RAM MODULE

The JR. RAM MODULE, utilizing twelve (12) IM6518 1024 x 1 CMOS RAMS on a 4½" x 6½" PC board, provides a convenient memory extension module. Non-volatility is assured by two (2) penlight batteries which are provided.



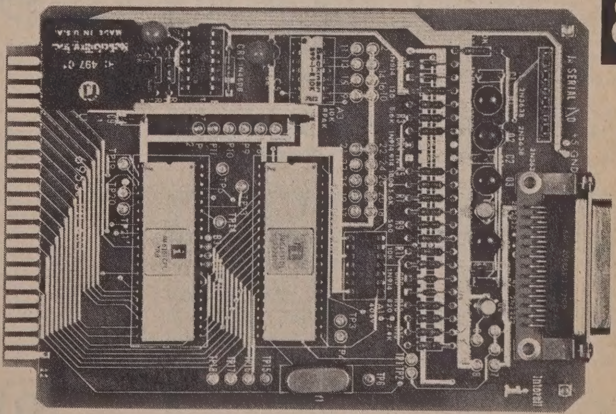
6952-P2KX12
JR. PROGRAMMABLE ROM-P/ROM MODULE

The JR. P/ROM MODULE provides the user with twelve (12) sockets organized on a 4½" x 6½" PC board. The user has the option of utilizing the IM5623, 256 x 4, or IM5624, 512 x 4 three-state-output Avalanche Induced Migration (AIM) programmable bipolar P/ROMs to obtain from 256 to 2048 words of program. Each of the four (4) rows of sockets are power strobed to permit 0.75 watts average when the P/ROMs are accessed.



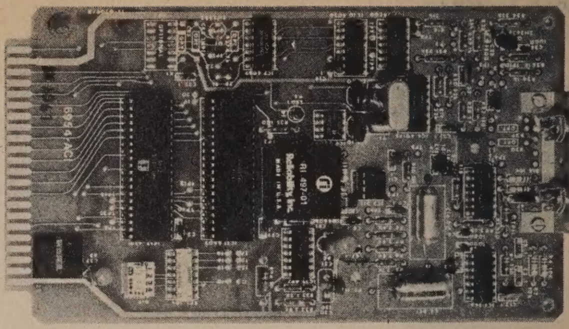
6953-PIEART
JR. SERIAL I/O MODULE

The JR. SERIAL I/O MODULE featuring the IM6101 CMOS Parallel Interface Element (PIE) and the IM6403 CMOS Universal Asynchronous Receiver Transmitter (UART) provides the user with serial I/O capability with both RS232 and 20 mA current loop interfaces. The IM6100 controls the UART via the PIE. The CMOS ROM monitor contains a bootstrap routine for loading programs from the 6953-PIEART using BIN** formatted media.



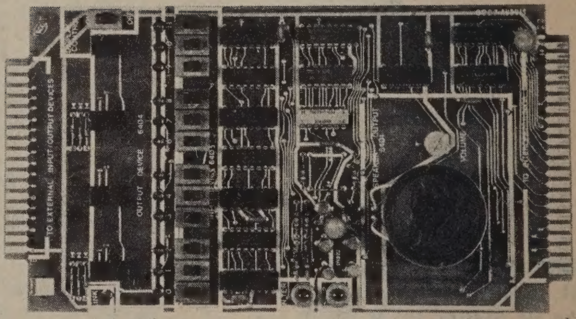
6954-ACI
JR. AUDIO CASSETTE INTERFACE MODULE

The INTERCEPT JR. AUDIO CASSETTE INTERFACE MODULE allows the user to store and retrieve programs on an inexpensive cassette tape recorder. The module transfers data at 30 characters per second. Thus, approximately 200,000 characters may be recorded on a standard two hour cassette. The module employs the IM6101 PIE and IM6402 UART to accomplish serial/parallel conversion, as well as two phaselock loops and a digital sinewave generator for the analog interface.



6957-AUDVIS
JR. AUDIO VISUAL MODULE

The JR. AUDIO VISUAL MODULE provides the user with an excellent tutorial device. A switch register, acting as an input, can be loaded into two LED display registers providing both binary and seven segment octal readout. A volume controlled speaker can be "clicked" or used to produce tones by controlling the rate at which the speaker is pulsed. A display control on-off switch is provided for power conservation.



MICROINTERPRETER SIMPLIFIES PROGRAM ENTRY

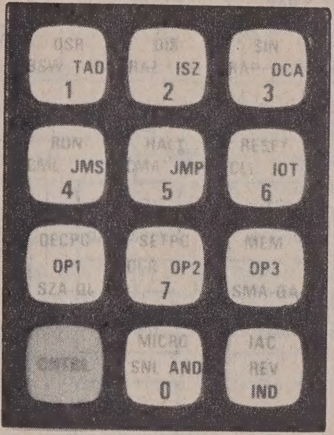
The INTERCEPT JR. MICROINTERPRETER provides an assembler-like method of entering programs. The user needn't remember opcodes! The MICROINTERPRETER converts assembler mnemonics into machine language opcodes.

EXAMPLE:

Add 7_{10} (0007_8) which is stored in memory location 22_{10} (0026_8), to 15_{10} (0017_8), which is stored in memory location 23_{10} (0027_8), and store the result in 21_{10} (0025_8).

PROGRAM

```
0020    CLA         /Clear Accumulator
0021    TAD 0026    /Read Location 0026
0022    TAD 0027    /Add Location 0027
0023    DCA 0025    /Deposit Result in 0025
0024    HLT         /Halt
```


OSR
SW TAD
1
DIS
RAL ISZ
2
SIN
RAR DCA
3
RUN
CML JMS
4
HALT
CMA JMP
5
RESET
CLL IOT
6
DECPC
OP1
SZA-QL
SETPC
CLA OP2
7
MEM
OP3
SMA-QA
CNTRL
MICRO
SNL AND
0
IAC
REV
IND

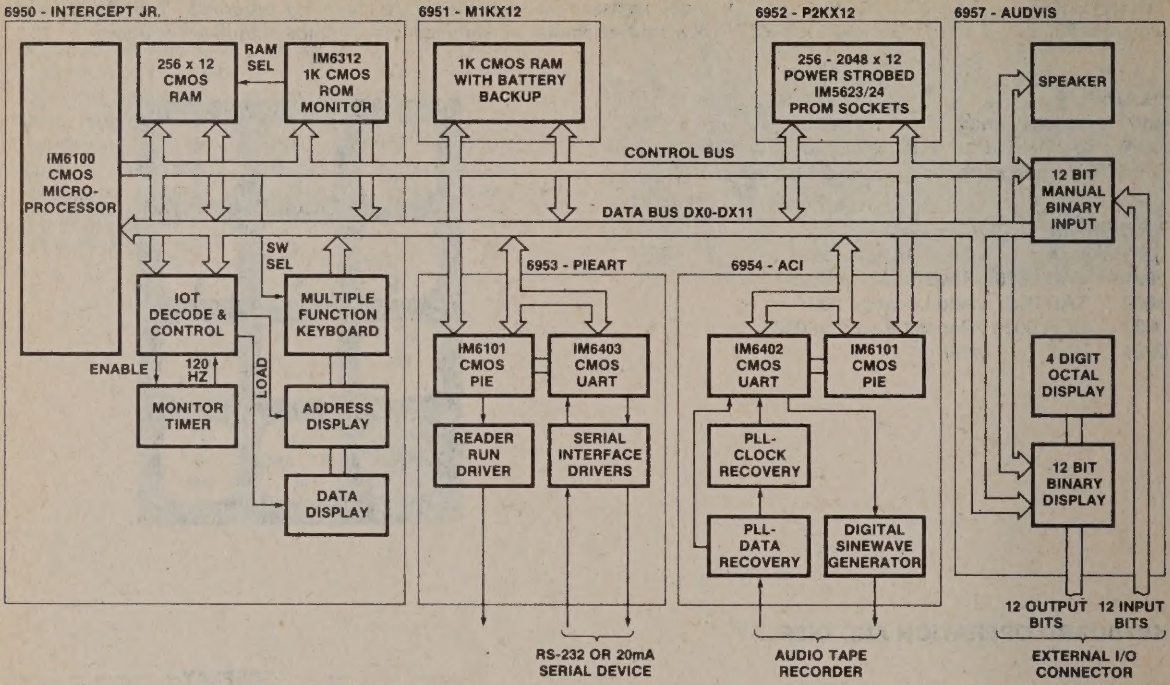
KEYBOARD OPERATION AND DISPLAY

OPERATION	KEYBOARD ENTRIES (Left to Right)	DISPLAY ADDRESS	DISPLAY MEMORY
	CNTRL SET PC 0 0 2 0	0020	* * * *
PROGRAM	CNTRL MICRO OP1 CLA	0020	7200
	CNTRL TAD 0 0 2 6	0021	1026
	CNTRL TAD 0 0 2 7	0022	1027
	CNTRL DCA 0 0 2 5	0023	3025
	CNTRL OP2 HALT	0024	7402
EXIT FROM MICROINTERPRETER	CNTRL CNTRL	0025	* * * *
ENTER ARGUMENTS	MEM 0 0 0 0	0025	0000
	MEM 0 0 0 7	0026	0007
	MEM 0 0 1 7	0027	0017
EXECUTE PROGRAM	CNTRL SET PC 0 0 2 0	0020	7600
	CNTRL RUN	0025	0026

Answer is displayed as 0026_8 (22_{10}).

*Don't Care

SYSTEM BLOCK DIAGRAM


6950 - INTERCEPT JR.
6951 - M1KX12
6952 - P2KX12
6957 - AUDVIS
IM6100 CMOS MICRO-PROCESSOR
256 x 12 CMOS RAM
RAM SEL
IM6312 1K CMOS ROM MONITOR
1K CMOS RAM WITH BATTERY BACKUP
256 - 2048 x 12 POWER STROBED IM5623/24 PROM SOCKETS
SPEAKER
CONTROL BUS
12 BIT MANUAL BINARY INPUT
DATA BUS DX0-DX11
SW SEL
IOT DECODE & CONTROL
MULTIPLE FUNCTION KEYBOARD
ENABLE
120 HZ
LOAD
MONITOR TIMER
ADDRESS DISPLAY
DATA DISPLAY
6953 - PIEART
IM6101 CMOS PIE
IM6403 CMOS UART
READER RUN DRIVER
SERIAL INTERFACE DRIVERS
6954 - ACI
IM6402 CMOS UART
IM6101 CMOS PIE
PLL-CLOCK RECOVERY
PLL-DATA RECOVERY
DIGITAL SINEWAVE GENERATOR
4 DIGIT OCTAL DISPLAY
12 BIT BINARY DISPLAY
12 OUTPUT BITS
12 INPUT BITS
RS-232 OR 20mA SERIAL DEVICE
AUDIO TAPE RECORDER
EXTERNAL I/O CONNECTOR

6970-IFDOS
Intercept Floppy Disc Operating System

DESCRIPTION

The 6970-IFDOS Floppy Disc Operating System is designed to facilitate development of software for an IM6100 microprocessor-based system. An ASCII terminal such as the ASR33 is required, as well as at least 4K words of memory (included with the INTERCEPT prototyping system).

HARDWARE

The hardware components of 6970-IFDOS consist of two completely interfaced floppy disc drive mechanisms with all electronics, power supplies, and cables necessary to add over four (4) million bits of "on line" mass storage capability to the INTERCEPT prototyping system. All components are contained in a single covered enclosure which is rack mountable or can be placed on any flat surface. The interface module is inserted directly into the INTERCEPT bus and is connected to the disc system via a multi-conductor ribbon cable.

Features:

- IBM 3740 compatible media with multiple sources
- Software compatible with DEC RX8 for the PDP-8 minicomputers
- Intelligent disc drive/controller formatter/interface communications which provide the ability to:
  - Detect, identify, and correct errors resulting from mechanical, electrical, media or human malfunction
  - Completely format a diskette within industry standards
- Automatic transparent self tests on disc related equipment are performed at times when system throughput is least affected
- Flexible Programmed Input/Output for applications that require direct communications between user programs and the storage system

SOFTWARE

Features:

- A file system which maintains a catalog of user files on floppy disc and performs file handling and input/output operations as specified by user

Features (con't):

- A keyboard monitor which provides communication between the user and the operating system thereby enabling simple commands to enter and delete files in the user catalog, transfer files between memory and mass storage, print the user file catalog, and call system programs
- An easy to learn text editor which allows the user to create and modify ASCII text at the console terminal
- An extremely fast and flexible assembler which accepts source programs created by the editor and produces binary output for subsequent loading and execution
- A binary loader which loads and executes assembler output files and facilitates loading of existing binary paper tapes
- An octal debugger which allows the user to examine, modify, and control execution of programs from the terminal
- Numerous utility programs for absolute block copying and dumping of floppy discs, system data handling, control of system parameters, and printing of system program catalogs

DIAGNOSTIC SOFTWARE

- Binary programs to test the floppy disc system and interface
- A listing of the programs

PHYSICAL SPECIFICATIONS

- DIMENSIONS Height 10.5 inches
  Width 19 inches
  Depth 22.5 inches
- WEIGHT 54 lbs
- POWER REQUIREMENTS
  110 volts @ 60 Hz (2.0 Amps) or
  200 volts @ 50 Hz (1.5 Amps)

The listing for 6980-ISOFT can be ordered separately by specifying 6980-ILIST.

INTERSIL

IM7027/MK4027
Dynamic RAM
4096 Bit (4K x 1)

FEATURES

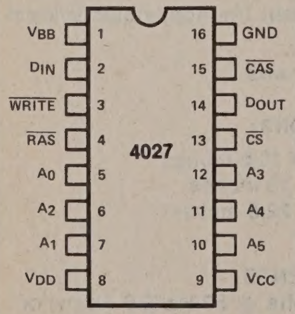
- 4096 X 1 Bit Organization
- Gated $\overline{\text{CAS}}$
- $\overline{\text{RAS}}$ Only Refresh
- All Inputs TTL Compatible
- On-Chip Latches for Addresses, Chip Select and Data In
- 10% Supply Tolerances (+12V, +5V, -5V)
- Three-State TTL Compatible Output
- Low Power Dissipation
  - –470 mW Operating
  - – 27 mW Standby
- Chip Select Decode Does Not Add to Access Time
- Output Data Latched and Valid Into Next Cycle
- N-Channel Silicon Gate Technology
- Pin and Performance Compatibility with Mostek MK4027

GENERAL DESCRIPTION

The IM7027 is a 4096 X 1 bit dynamic random access memory which is packaged in 16 pin DIP. The cell array is organized into 64 rows of 64 cells. Each of the 64 row addresses requires refreshing every 2 milliseconds. Any read cycle refreshes the selected row as does a refresh cycle using $\overline{\text{RAS}}$ only. A write, read/write or read/modify/write cycle also refreshes the selected row, but non-accessed chips should not be selected to avoid writing data into the selected row. A page-mode feature is included to reduce the access and/or cycle time for block data operations. Page-mode operation is useful in direct memory access (DMA) operations.

System oriented features include direct interfacing with TTL, on-chip registers which eliminate the need for interface registers, logic input levels selected for best noise immunity. Twelve address bits are required to decode 1 of 4096 cell locations, and are multiplexed onto 6 address pins and latched into the row and column address latches. The Row Address Strobe ($\overline{\text{RAS}}$) latches the 6 row address bits onto the chip. The Column Address Strobe ($\overline{\text{CAS}}$) latches the 6 column address bits and Chip Select ($\overline{\text{CS}}$) onto the chip. Since the Chip Select signal is not required until well into the cycle, its decoding time does not add to the system address or cycle time.

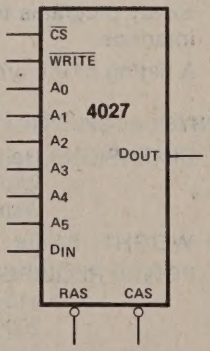
PIN CONFIGURATION



4027
VBB 1
DIN 2
WRITE 3
RAS 4
A0 5
A2 6
A1 7
VDD 8
16 GND
15 CAS
14 DOUT
13 CS
12 A3
11 A4
10 A5
9 VCC

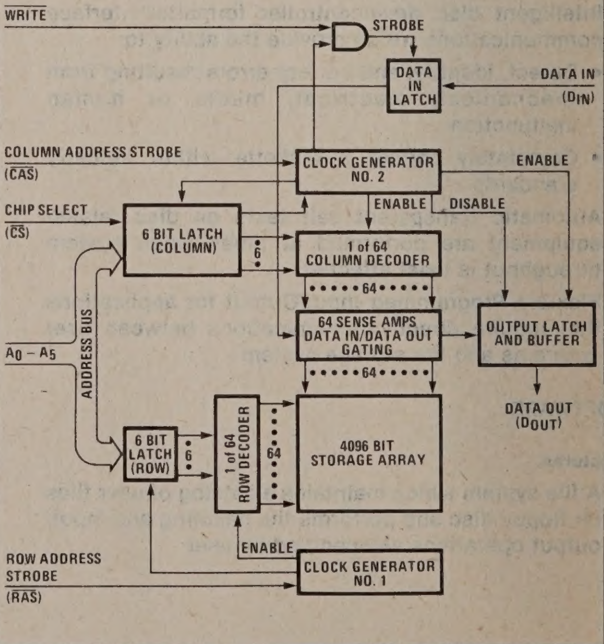
(outline dwg JE)

LOGIC SYMBOL



4027
CS
WRITE
A0
A1
A2
A3
A4
A5
DIN
DOUT
RAS
CAS

BLOCK DIAGRAM



WRITE
STROBE
DATA IN LATCH
DATA IN (DIN)
COLUMN ADDRESS STROBE (CAS)
CLOCK GENERATOR NO. 2
ENABLE
ENABLE
DISABLE
CHIP SELECT (CS)
6 BIT LATCH (COLUMN)
6
1 of 64 COLUMN DECODER
64
A0 – A5
ADDRESS BUS
64 SENSE AMPS DATA IN/DATA OUT GATING
OUTPUT LATCH AND BUFFER
64
DATA OUT (DOUT)
6 BIT LATCH (ROW)
6
1 of 64 ROW DECODER
64
4096 BIT STORAGE ARRAY
ENABLE
ROW ADDRESS STROBE (RAS)
CLOCK GENERATOR NO. 1

ORDERING INFORMATION

ORDER NUMBER	ACCESS TIME	CYCLE TIME	PACKAGE
IM7027-1CJE	120 ns	250 ns	16 PIN CERDIP
MK4072P-2	150 ns	320 ns	16 PIN CERDIP
MK4027P-3	200 ns	375 ns	16 PIN CERDIP
MK4027P-4	250 ns	375 ns	16 PIN CERDIP

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +150°C
Voltage On Any Pin w/Respect to V_{BB}	-0.5V to +20.0V
Power Dissipation	1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

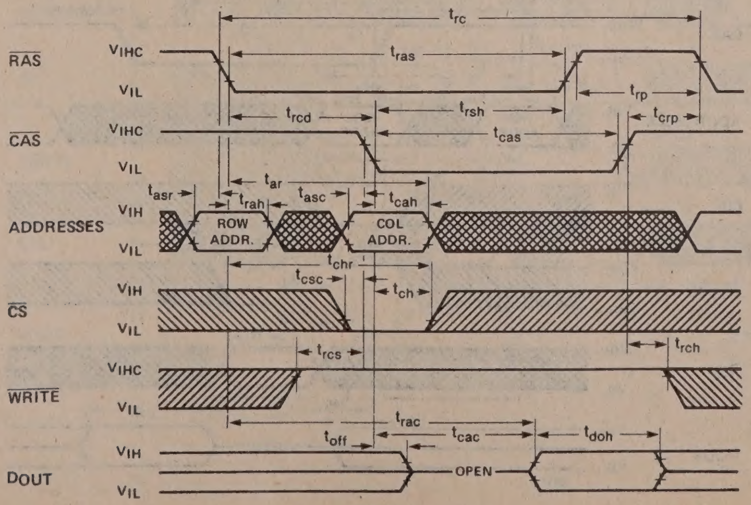
TEST CONDITIONS: $V_{DD} = +12.0V \pm 10\%$, $V_{CC} = +5.0V \pm 10\%$, $V_{BB} = -5.0V \pm 10\%$, $T_A = 0°C$ to $+70°C$

	SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
1	V_{IHC}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ Voltage High		2.4	7.0	V	
2	V_{IH}	Input Voltage High		2.2	7.0	V	
3	V_{IL}	Input Voltage Low		-1.0	0.8	V	
4	I_{ILK}	Input Leakage Current			10	μA	4
5	I_{OLK}	Output Leakage Current			10	μA	5, 6
6	I_{DD1}	Average V_{DD} Power Supply Current			35	mA	2
7	I_{CC}	V_{CC} Power Supply Current					3
8	I_{BB}	Average V_{BB} Power Supply Current	-2, -3, -4		300	μA	
			-1		400	μA	
9	I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	5
10	I_{DD3}	Average V_{DD} Current ("$\overline{RAS}$ Only" Refresh)			25	mA	
11	V_{OH}	Output Voltage High $I_{OH} = -5$ mA		2.4		V	
12	V_{OL}	Output Voltage Low $I_{OL} = 3.2$ mA			0.4	V	

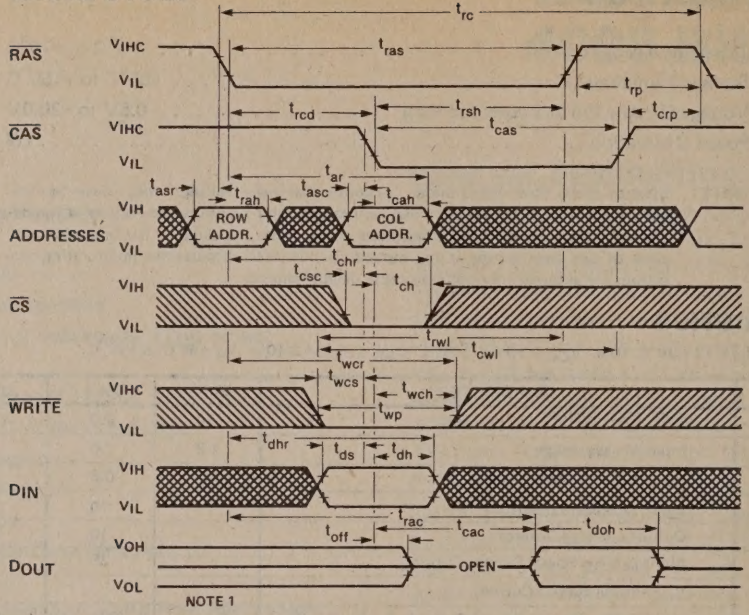
NOTES:
1. V_{BB} must be applied before and removed after other supply voltages.
2. I_{DD1} (max) measured at t_{RC} (min). I_{DD1} is proportional to cycle rate.
3. I_{CC} depends on output loading.
4. All pins except V_{BB} at 0V, $V_{BB} = -5V$ and test pin = +10V.
5. Output disabled, $\overline{RAS}$ and $\overline{CAS} \geqslant V_{IHC}$ (min).
6. $0V \leqslant V_{OUT} \leqslant +10V$.

TIMING DIAGRAMS

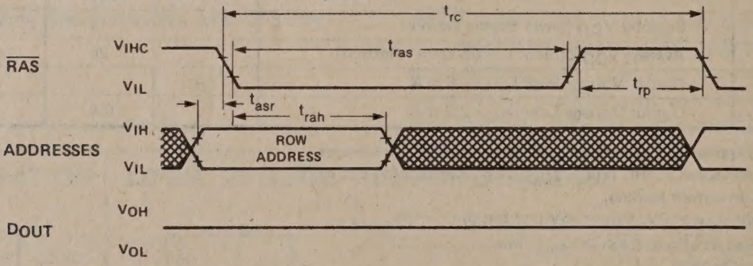
READ AND REFRESH CYCLE



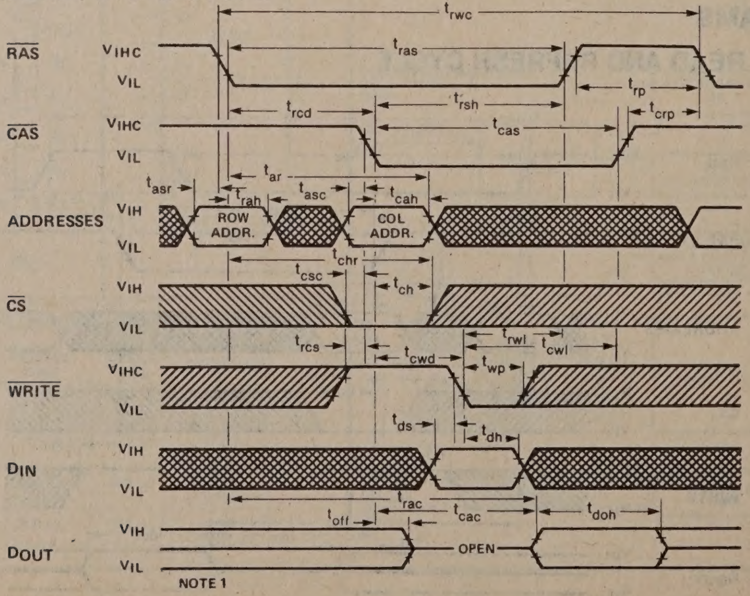
WRITE CYCLE


t_rc
RAS
VIHC
VIL
t_ras
t_rp
t_rcd
t_rsh
t_crp
CAS
t_cas
t_ar
t_asr
t_rah
t_asc
t_cah
ADDRESSES
VIH
ROW ADDR.
COL ADDR.
t_chr
t_csc
t_ch
CS
t_rwl
t_cwl
t_wcr
t_wcs
t_wch
t_wp
WRITE
t_dhr
t_ds
t_dh
DIN
t_rac
t_off
t_cac
t_doh
DOUT
VOH
VOL
OPEN
NOTE 1

RAS ONLY REFRESH CYCLE

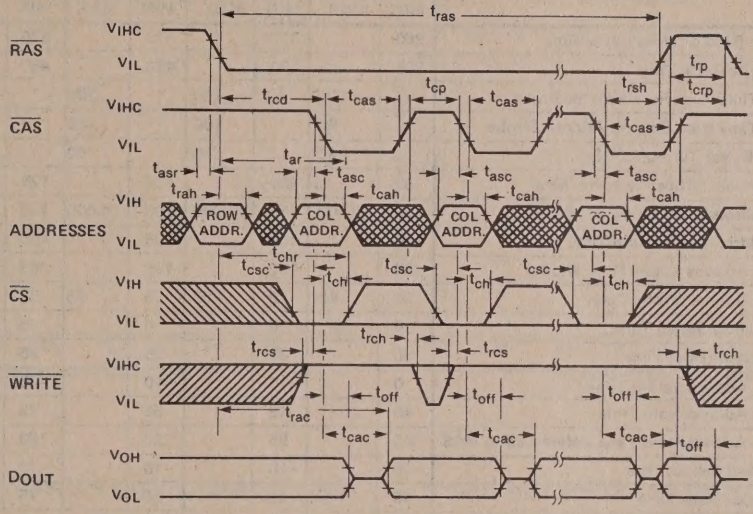

t_rc
RAS
VIHC
VIL
t_ras
t_rp
t_asr
t_rah
ADDRESSES
VIH
ROW ADDRESS
DOUT
VOH
VOL

READ/WRITE CYCLE

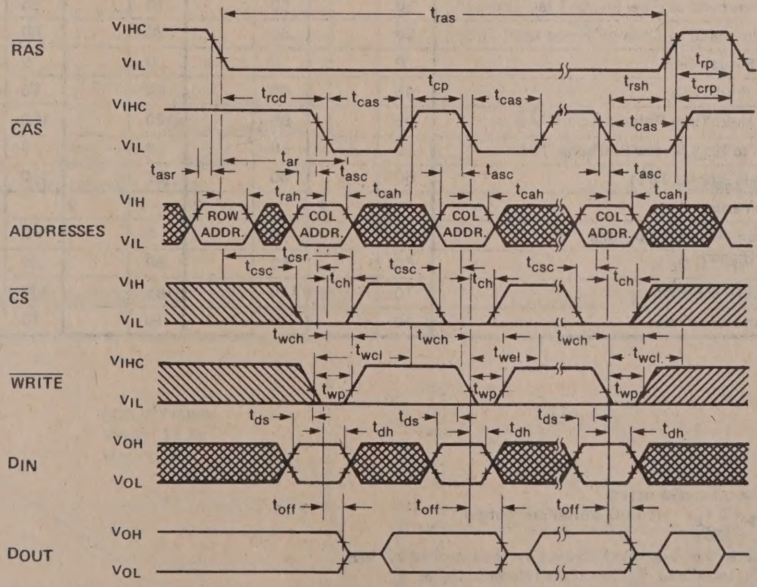

t_rwc
RAS
VIHC
VIL
t_ras
t_rp
t_rcd
t_rsh
t_crp
CAS
t_cas
t_ar
t_asr
t_rah
t_asc
t_cah
ADDRESSES
VIH
ROW ADDR.
COL ADDR.
t_chr
t_csc
t_ch
CS
t_rwl
t_cwl
t_rcs
t_cwd
t_wp
WRITE
t_ds
t_dh
DIN
t_rac
t_off
t_cac
t_doh
DOUT
OPEN
NOTE 1

TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE


tras
RAS
VIHC
VIL
trp
tcrp
trsh
trcd
tcas
tcp
tcas
tcas
CAS
VIHC
VIL
tasr
tar
tasc
tasc
tasc
trah
tcah
tcah
tcah
ADDRESSES
VIH
VIL
ROW ADDR.
COL ADDR.
COL ADDR.
COL ADDR.
tchr
tcsc
tcsc
tcsc
tch
tch
tch
CS
VIH
VIL
trcs
trch
trcs
trch
WRITE
VIHC
VIL
toff
toff
toff
trac
tcac
tcac
tcac
toff
DOUT
VOH
VOL

PAGE MODE WRITE CYCLE


tras
RAS
VIHC
VIL
trp
tcrp
trsh
trcd
tcas
tcp
tcas
tcas
CAS
VIHC
VIL
tasr
tar
tasc
tasc
tasc
trah
tcah
tcah
tcah
ADDRESSES
VIH
VIL
ROW ADDR.
COL ADDR.
COL ADDR.
COL ADDR.
tcsr
tcsc
tcsc
tcsc
tch
tch
tch
CS
VIH
VIL
twch
twch
twch
twcl
twcl
twcl
WRITE
VIHC
VIL
twp
twp
twp
tds
tds
tds
tdh
tdh
tdh
DIN
VOH
VOL
toff
toff
toff
DOUT
VOH
VOL

AC CHARACTERISTICS

TEST CONDITIONS: V_{DD} = +12.0V ± 10%, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{BB} = –5.0V ± 10%, T_A = 0°C to +70°C (NOTES 1, 5 and 8)

	SYMBOL	PARAMETER	IM7027-1CJE		MK4027 P-2		MK4027 P-3		MK4027 P-4		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{rc}	Random Read or Write Cycle Time	250		320		375		375		ns	2
2	t_{rwc}	Read Write Cycle Time	325		330		420		480		ns	
3	t_{rac}	Access Time from Row Address Strobe		120		150		200		250	ns	3
4	t_{cac}	Access Time from Column Address Strobe		80		100		135		165	ns	3
5	t_{off}	Output Buffer Turn-off Delay		40		40		50		60	ns	
6	t_{rp}	Row Address Strobe Precharge Time	80		100		120		120		ns	
7	t_{ras}	Row Address Strobe Pulse Width	120	10,000	150	10,000	200	10,000	250	10,000	ns	
8	t_{rsh}	Row Address Strobe Hold Time	80		100		135		165		ns	
9	t_{cas}	Column Address Strobe Pulse Width	80		100		135		165		ns	
10	t_{rcd}	Row to Column Strobe Delay	20	40	20	50	25	65	35	85	ns	4
11	t_{asr}	Row Address Set-up Time	0		0		0		0		ns	
12	t_{rah}	Row Address Hold Time	20		20		25		35		ns	
13	t_{asc}	Column Address Set-up Time	0		–10		–10		–10		ns	
14	t_{cah}	Column Address Hold Time	45		45		55		75		ns	
15	t_{ar}	Column Address Hold Time Referenced to $\overline{\text{RAS}}$	95		95		120		160		ns	
16	t_{csc}	Chip Select Set-up Time	–10		–10		–10		–10		ns	
17	t_{ch}	Chip Select Hold Time	45		45		55		75		ns	
18	t_{chr}	Chip Select Hold Time Referenced to $\overline{\text{RAS}}$	95		95		120		160		ns	
19	t_t	Transition Time (Rise and Fall)	3	35	3	35	3	50	3	50	ns	
20	t_{rcs}	Read Command Set-up Time	0		0		0		0		ns	
21	t_{rch}	Read Command Hold Time	0		0		0		0		ns	
22	t_{wch}	Write Command Hold Time	45		45		55		75		ns	
23	t_{wcr}	Write Command Hold Time Referenced to $\overline{\text{RAS}}$	95		95		120		160		ns	
24	t_{wp}	Write Command Pulse Width	45		45		55		75		ns	
25	t_{rwl}	Write Command to Row Strobe Lead Time	50		50		70		85		ns	
26	t_{cwl}	Write Command to Column Strobe Lead Time	50		50		70		85		ns	
27	t_{ds}	Data in Set-up Time	0		0		0		0		ns	7
28	t_{dh}	Data in Hold Time	45		45		55		75		ns	7
29	t_{dhr}	Data in Hold Time Referenced to $\overline{\text{RAS}}$	95		95		120		160		ns	
30	t_{crp}	Column to Row Strobe Precharge Time	0		0		0		0		ns	
31	t_{cp}	Column Precharge Time	60		60		80		110		ns	
32	t_{rfsh}	Refresh Period		2		2		2		2	ms	
33	t_{wcs}	Write Command Set-up Time	0		0		0		0		ns	6
34	t_{cwd}	$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay	60		60		80		90		ns	6
35	t_{rwd}	$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay	110		110		145		175		ns	6
36	t_{doh}	Data Out Hold Time	10		10		10		10		ns	

NOTES 1: t_t = 5 ns unless otherwise noted.

2: $t_{rc} > t_{ras} + t_{rp} + 2\,t_t$ to limit power dissipation.

3: Load = 2TTL + 100 pF.

4: If t_{rcd} is greater than t_{rcd} (max) access time is controlled by t_{cac}.

5: V_{ihc} (min), V_{ih} (min) and V_{il} (max) are reference levels.

6: t_{wcs}, t_{cwd} and t_{rwd} are not restrictive parameters, they are electrical characteristics only as follows:

a. $t_{cwd} + t_t \leq t_{cwd}$ minimum output latch contains data written into current address.

b. $t_{cwd} \geq t_{cwd}$ (max) + t_t and $t_{rwd} \geq t_{rwd}$ (max) + t_t the data output latch contains data read from the current address.

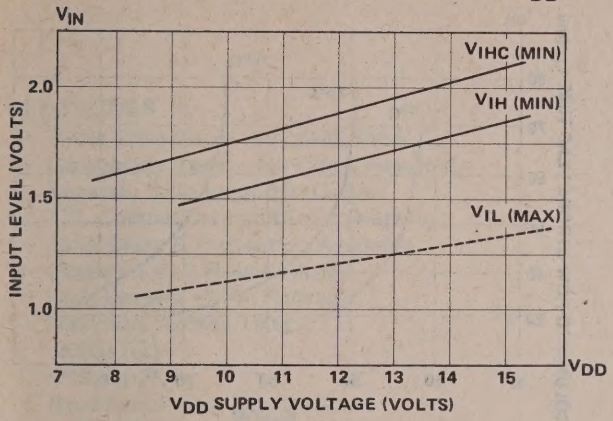
c. If t_{cwd} does not meet the above, data output state is indeterminate.

7: Referenced to latest of $\overline{\text{CAS}}$ or $\overline{\text{WRITE}}$.

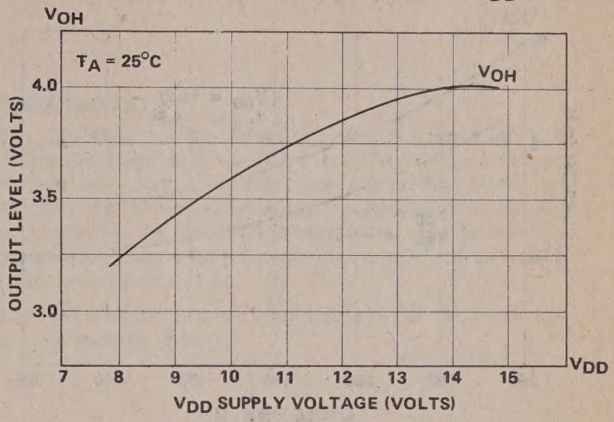
8: Any 8 cycles that perform refresh are required after power is applied.

TYPICAL DEVICE CHARACTERISTICS

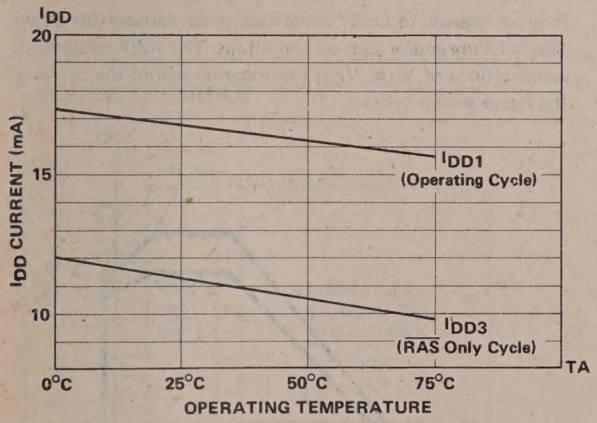
TYPICAL ADDRESS DATA INPUT LEVELS VS. V_{DD}



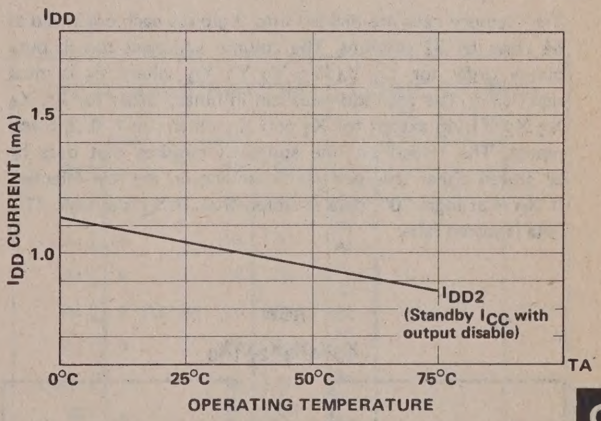
TYPICAL DATA OUTPUT LEVEL VS. V_{DD}



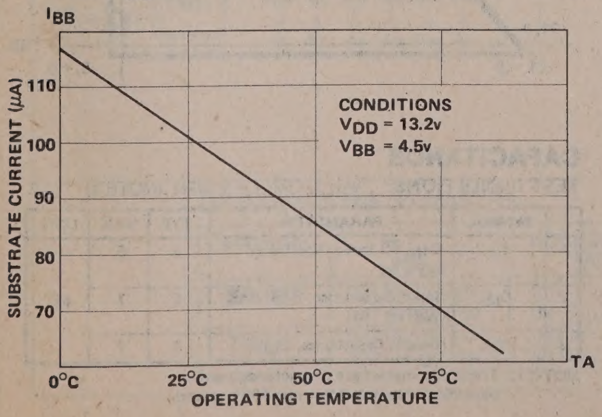
TYPICAL I_{DD} CURRENT VS. OPERATING TEMPERATURE



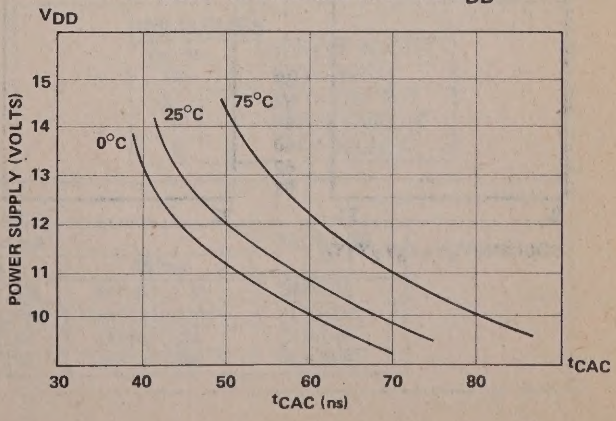
TYPICAL I_{DD} CURRENT VS. OPERATING TEMPERATURE



TYPICAL I_{BB} CURRENT VS. OPERATING TEMPERATURE

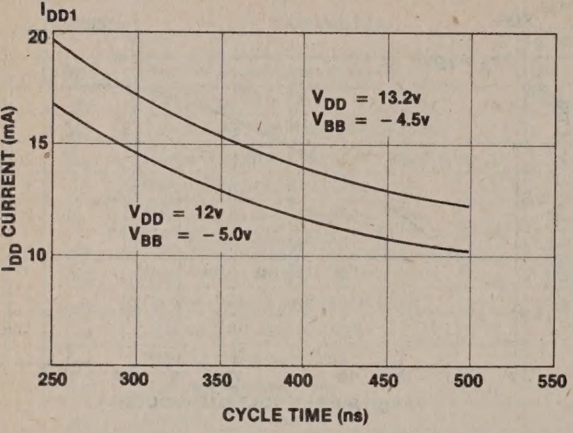


TYPICAL t_{CAC} ACCESS TIME VS. V_{DD}

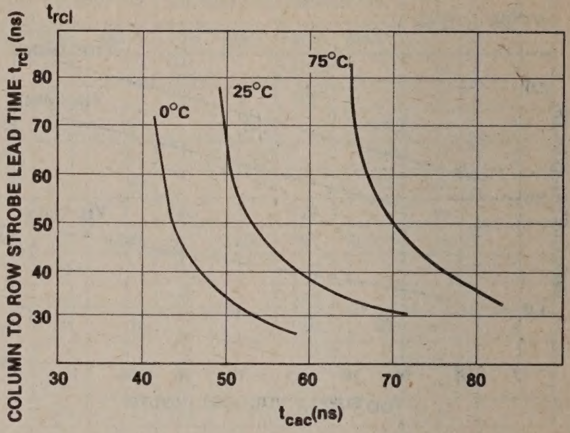


TYPICAL DEVICE CHARACTERISTICS (Continued)

TYPICAL I_{DD} CURRENT VS. CYCLE TIME

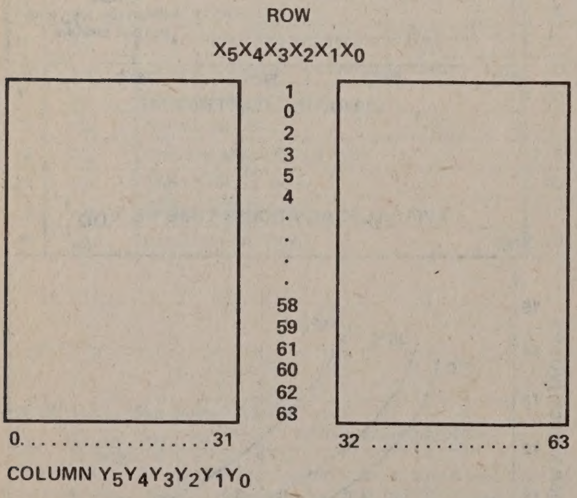


TYPICAL t_{cac} VS. t_{rcl}



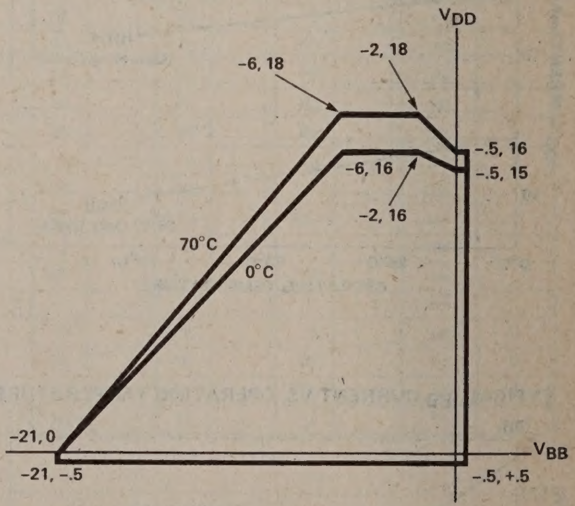
BIT MAP

The memory cells are divided into 2 groups each organized as 64 rows by 32 columns. The column addresses run in pure binary order for Y_5 Y_4 Y_3 Y_2 Y_1 Y_0, where Y_5 is most significant. The row addresses run in binary order for X_5 X_4 X_3 X_2 X_1 X_0 except for X_1 and X_0 which run 1, 0, 2, 3 and repeat. The folded bit line approach requires that data be be stored either true or false depending on the row selected. If X_0 is at logic "0", data is stored true. If X_0 is at logic "1", data is stored false.



MAXIMUM STRESS VOLTAGES

It is of interest to know worst case stress voltages for power supply failure and/or turn-on conditions. The 7027 can tolerate combinations of V_{BB}, V_{DD} that operate within the curves of the figure shown below.



CAPACITANCE

TEST CONDITIONS: V_{IN} = OV, f = 1 MHz (NOTE 1)

	SYMBOL	PARAMETER	TYP	MAX	UNIT
1	C_{I1}	D_{IN}, $\overline{CS}$ Input Capacitance A_0 - A_5	3	5	pF
2	C_{I2}	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	5	7	
3	C_O	Output Capacitance, D_{OUT}	5	7	

NOTE 1: These parameters are characterized and periodically sampled but not 100% tested.

INTERSIL

IM7141
4096 Bit (4096 x 1) NMOS Static RAM

FEATURES

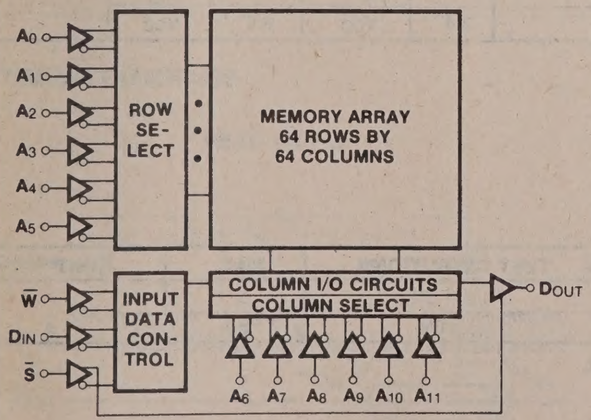
- **Cycle Time Equal to Access Time**
- **Completely Static - No Clock Required**
- **Separate Data Input and Output**
- **TTL Compatible Inputs and Outputs**
- **883A Class B Processing Available**
- **Single +5 Volt Power Supply**
- **High Density 18 Pin Package**
- **Maximum Access Time:**
  -200ns (-2)
  -300ns (-3)
- **Maximum Power Dissipation:**
  – 256mW (L)
  – 370mW (Standard)

DESCRIPTION

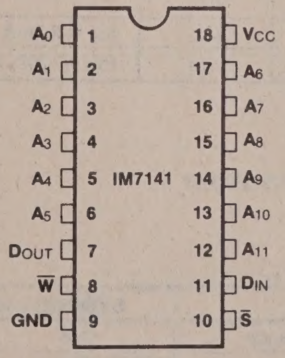
The IM7141 is a 4096-bit static Random Access Memory device organized 4096 words X 1. bit. The storage cells and decode and control circuitry are completely static; no clocks or refresh operations are required. Memory access occurs within the specified access time after all address inputs are stable. A Chip Select input is provided for simple memory array expansion.

The 7141 is assembled in a standard 18 pin DIP for maximum system packing density.

BLOCK DIAGRAM

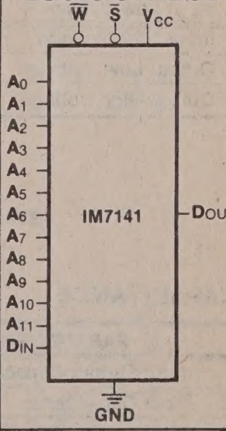

A0
A1
A2
A3
A4
A5
ROW SE- LECT
MEMORY ARRAY 64 ROWS BY 64 COLUMNS
W̄
DIN
S̄
INPUT DATA CON- TROL
COLUMN I/O CIRCUITS
COLUMN SELECT
DOUT
A6
A7
A8
A9
A10
A11

PIN CONFIGURATION


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
DOUT 7
W̄ 8
GND 9
18 VCC
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 DIN
10 S̄
IM7141

(outline dwgs JN, PN)

LOGIC SYMBOL


W̄
S̄
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DIN
IM7141
DOUT
GND

PIN NAMES

A_0-A_{11}	ADDRESS INPUTS
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
$\overline{W}$	WRITE ENABLE
$\overline{S}$	CHIP SELECT

ORDERING INFORMATION

POWER	ACCESS TIME			PACKAGE
	200ns	300ns	450ns	
265mW	IM7141L2CJN	IM7141L3CJN	IM7141LCJN	CERDIP
	IM7141L2CPN	IM7141L3CPN	IM7141LCPN	PLASTIC
370mW	IM7141-2CJN	IM7141-3CJN	IM7141CJN	CERDIP
	IM7141-2CPN	IM7141-3CPN	IM7141CPN	PLASTIC

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0° C to +70° C
Storage Temperature	−65° C to +150° C
Voltage on any Pin to Ground	−0.5V to +7V
Power Dissipation	1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $T_A = 0°C$ to $+70°C$, $V_{CC} = +5\ V \pm 5\ \%$

PARAMETER	SYMBOL	TEST CONDITIONS	7141L MIN	7141L MAX	7141 MIN	7141 MAX	UNITS
Input Load Current (All Inputs)	I_{INLD}	$V_{IN} = 0$ to 5.25V		10		10	μA
Output Leakage Current	I_{OLK}	$\overline{S} = 2.4V$, $V_{I/O} = 0.4V$ to V_{CC}		10		10	
Power Supply Current	I_{CC2}	VIN = 5.25, $T_A = 0°C$ Output Open		45		65	mA
Power Supply Current	I_{CC1}	VIN = 5.25V, $T_A = 0°C$ Output Open		50		70	
Input Low Voltage	V_{IL}		−0.5	0.8	−0.5	0.8	V
Input High Voltage	V_{IH}		2.0	V_{CC}	2.0	V_{CC}	
Output Low Voltage	V_{OL}	$I_{OL} = 3.2mA$		0.4		0.4	
Output High Voltage	V_{OH}	$I_{OH} = -200\mu A$	2.4	V_{CC}	2.4	V_{CC}	

CAPACITANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	5	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	5	

NOTE: These parameters are periodically sampled, not 100% tested.

DEVICE OPERATION

When $\overline{W}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{W}$ remains high, the data stored cannot be changed by the addresses, Chip select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be changed by $\overline{W}$, the addresses, or the input data as long as $\overline{S}$ is high. Either $\overline{S}$ or $\overline{W}$ by itself, or in conjunction with the other, can prevent the extraneous writing due to signal transitions.

A READ occurs during the overlap of $\overline{S}$ low and $\overline{W}$ high. Data within the array can only be changed during a Write time, defined as the overlap of $\overline{S}$ low and $\overline{W}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{wr}.

AC CHARACTERISTICS

TEST CONDITIONS: $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

$t_r = t_f = 10ns$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, Output Load = 1 TTL Gate and 100pF

Input and output timing reference level = 1.5V

READ CYCLE

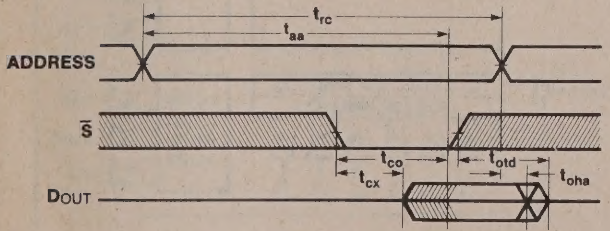
PARAMETER	SYMBOL	7141L2, 7141-2 MIN	7141L2, 7141-2 MAX	7141L3, 7141-3 MIN	7141L3, 7141-3 MAX	7141L, 7141 MIN	7141L, 7141 MAX	UNITS
Read Cycle	t_{rc}	200		300		450		ns
Access Time	t_{aa}		200		300		450	
$\overline{S}$ to Output Valid	t_{co}		70		100		100	
$\overline{S}$ to Output Active	t_{cx}	0		0		0		
Output 3 State from Deselect	t_{otd}	0	60	0	80	0	100	
Output Hold from Address Change	t_{oha}	10		10		10		

WRITE CYCLE

PARAMETER	SYMBOL	7141L2, 7141-2 MIN	7141L2, 7141-2 MAX	7141L3, 7141-3 MIN	7141L3, 7141-3 MAX	7141L, 7141 MIN	7141L, 7141 MAX	UNITS
Write Time Cycle	t_{wc}	200		300		450		ns
Write Time	t_w	120		150		200		
Write Release Time	t_{wr}	0		0		0		
Output 3 State from Write	t_{otw}	0	60	0	80	0	100	
Data to Write Time Overlap	t_{dw}	120		150		200		
Data Hold from Write Time	t_{dh}	15		15		15		
Address Setup Time	t_{aw}	0		0		0		
$\overline{S}$ Select Pulse Width	t_{cw}	120		150		200		

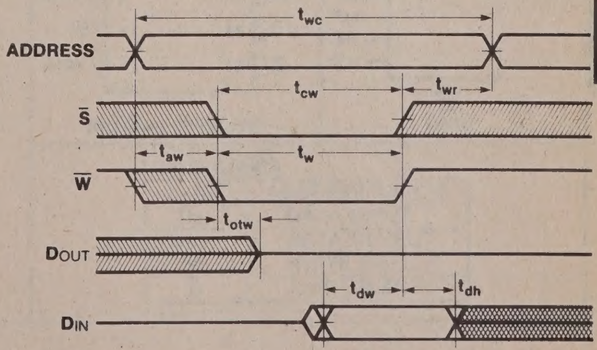
TIMING DIAGRAMS

READ CYCLE

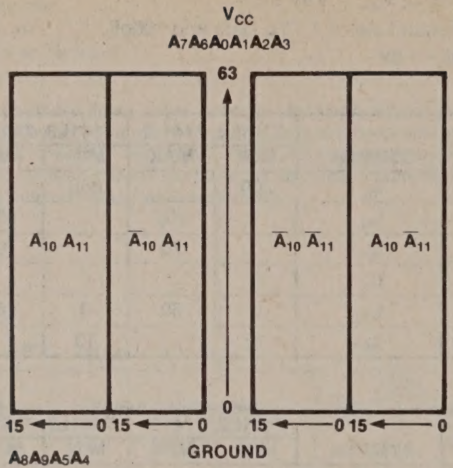

t_{rc}
t_{aa}
ADDRESS
$\overline{S}$
t_{co}
t_{otd}
t_{cx}
t_{oha}
DOUT

Note: 1. $\overline{W}$ is high for a READ cycle.

WRITE CYCLE


t_{wc}
ADDRESS
t_{cw}
t_{wr}
$\overline{S}$
t_{aw}
t_w
$\overline{W}$
t_{otw}
DOUT
t_{dw}
t_{dh}
DIN

7141 BIT MAP DIAGRAM


V_{CC}
$A_7A_6A_0A_1A_2A_3$
63
$A_{10}\ A_{11}$
$\overline{A}_{10}\ A_{11}$
$\overline{A}_{10}\ \overline{A}_{11}$
$A_{10}\ \overline{A}_{11}$
0
15 ← 0 15 ← 0
15 ← 0 15 ← 0
$A_8A_9A_5A_4$
GROUND

INTERSIL

IM7141M
4096 Bit (4096 x 1) NMOS Static RAM

FEATURES

- **Cycle Time Equal to Access Time**
- **Completely Static-No Clock Required**
- **Separate Data Input and Output**
- **TTL Compatible Inputs and Outputs**
- **883A Class B Processing Available**
- **Military Temperature Operation:**
  −55°C to +125°C
- **Single +5 Volt Power Supply**
- **Maximum Access Time:**
  −200ns (−2)
  −300ns (−3)
- **Maximum Power Dissipation: 495mW**

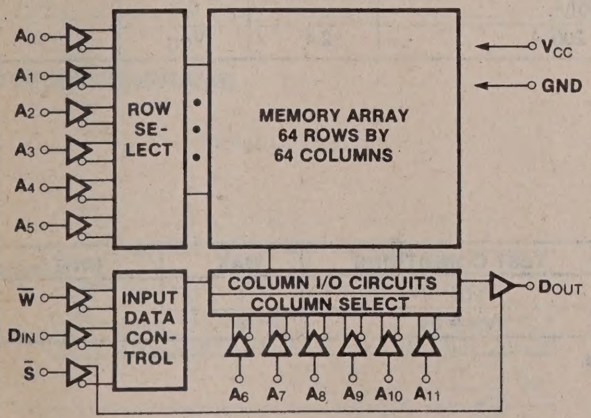
DESCRIPTION

The IM7141 is a 4096-bit static Random Access Memory organized 4096 words x 1 bit. The storage cells and decode and control circuitry are completely static; no clocks or refresh operations are required. Memory access occurs within the specified access time after all address inputs are stable. A Chip Select input is provided for simple memory array expansion.

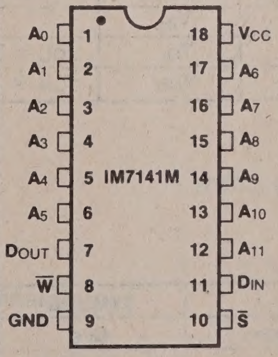
The IM7141M operates at 90mA over a 5V ± 10% range. The worst-case access time is 450ns with speeds of 300ns (−3) and 200ns (−2) available.

The device is assembled in a standard 8 pin DIP for maximum system packing density.

BLOCK DIAGRAM

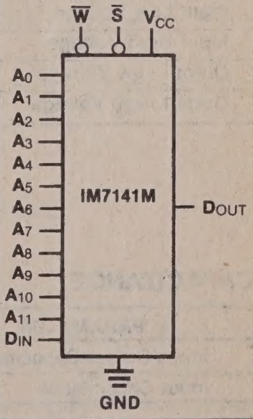

A0
A1
A2
A3
A4
A5
ROW SE-LECT
MEMORY ARRAY 64 ROWS BY 64 COLUMNS
VCC
GND
W̄
DIN
S̄
INPUT DATA CON-TROL
COLUMN I/O CIRCUITS
COLUMN SELECT
DOUT
A6
A7
A8
A9
A10
A11

PIN CONFIGURATION


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
DOUT 7
W̄ 8
GND 9
18 VCC
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 DIN
10 S̄
IM7141M

(outline dwg JN)

LOGIC SYMBOL


W̄
S̄
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DIN
IM7141M
DOUT
GND

PIN NAMES

A_0-A_{11}	ADDRESS INPUTS
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
$\overline{W}$	WRITE ENABLE
$\overline{S}$	CHIP SELECT

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE
IM7141-2MJN	200ns	CERDIP
IM7141-3MJN	300ns	CERDIP
IM7141MJN	450ns	CERDIP

ABSOLUTE MAXIMUM RATINGS

Operating Temperature .... −50°C to +125°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin to Ground .... −0.5V to +7V
Power Dissipation 1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input Load Current (All Inputs)	I_{INLD}	V_{IN} = 0V to 5.5V		10	μA
Output Leakage Current	I_{OLK}	$\overline{S}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}		10	
Power Supply Current	I_{CC1}	V_{IN} = 5.5V, Output Open $T_A = 25°C$		65	mA
Power Supply Current	I_{CC2}	V_{IN} = 5.5V, Output Open $T_A = -55°C$		90	
Input Low Voltage	V_{IL}		−0.5	0.8	V
Input High Voltage	V_{IH}		2.0	V_{CC}	
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA		0.4	
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4	V_{CC}	

CAPACITANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	5	

NOTE: These parameters are periodically sampled, not 100% tested.

DEVICE OPERATION

When $\overline{W}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{W}$ remains high the data stored cannot be changed by the addresses, Chip Select, or data input voltage levels and timing transitions. The block diagram also shows data storage cannot be changed by $\overline{W}$ the addresses, or the input data as long as $\overline{S}$ is high. Either $\overline{S}$ or $\overline{W}$ by itself, or in conjunction with the other, can prevent extraneous writing due to signal transitions.

A READ occurs during the overlap of $\overline{S}$ low and $\overline{W}$ high. Data within the array can only be changed during a Write time, defined as the overlap of $\overline{S}$ low and $\overline{W}$ low. To prevent the loss data, the addresses must be properly established during the entire Write time plus t_{WR}.

AC CHARACTERISTICS

TEST CONDITIONS: $T_A = -55°C$ to $+125°C$, $V_{CC} = =5V \pm 10\%$
$t_r = t_f = 10ns$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, Output Load = 1 TTL Gate and 100pF
Input and output timing reference level = 1.5V

READ CYCLE

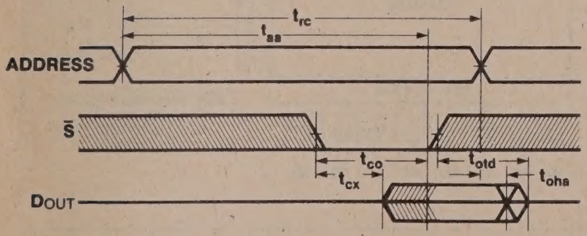
PARAMETER	SYMBOL	IM7141-2M		IM7141-3M		IM7141M		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle	t_{rc}	200		300		450		ns
Access Time	t_{aa}		200		300		450	
$\overline{S}$ to Output Valid	t_{co}		70		100		100	
$\overline{S}$ to Output Active	t_{cx}	0		0		0		
Output 3 State from Deselect	t_{otd}	0	60	0	80	0	100	
Output Hold from Address Change	t_{oha}	10		10		10		

WRITE CYCLE

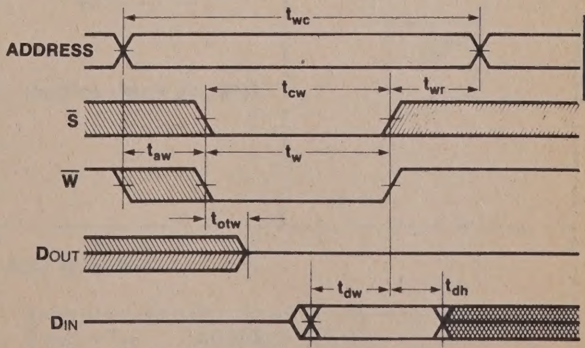
PARAMETER	SYMBOL	IM7141-2M		IM7141-3M		IM7141M		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Time Cycle	t_{wc}	200		300		450		ns
Write Time	t_w	120		150		200		
Write Release Time	t_{wr}	0		0		0		
Output 3 State from Write	t_{otw}	0	60	0	80	0	100	
Data to Write Time Overlap	t_{dw}	120		150		200		
Data Hold from Write Time	t_{dh}	15		15		15		
Address Setup Time	t_{aw}	0		0		0		
$\overline{S}$ Select Pulse Width	t_{cw}	120		150		200		

TIMING DIAGRAMS

READ CYCLE

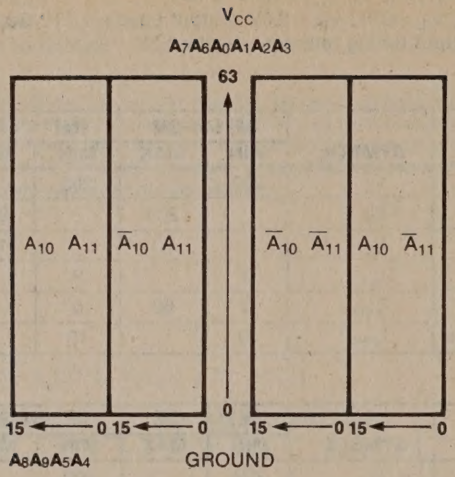


WRITE CYCLE



Note: 1. $\overline{W}$ is high for a READ cycle.

7141 BIT MAP DIAGRAM


V$_{CC}$
A$_7$A$_6$A$_0$A$_1$A$_2$A$_3$
63
0
A$_{10}$ A$_{11}$
$\overline{A}_{10}$ A$_{11}$
$\overline{A}_{10}$ $\overline{A}_{11}$
A$_{10}$ $\overline{A}_{11}$
15 ← 0 15 ← 0
15 ← 0 15 ← 0
A$_8$A$_9$A$_5$A$_4$
GROUND

INTERSIL

IM7332
32,768 BIT
(4096 x 8) HMOS ROM

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

- **High Speed — 300ns Maximum access time**
- **Completely static — no clock required**
- **Single +5V supply**
- **Fully TTL Compatible**
- **Two programmable Chip Selects**
- **Three-state outputs**
- **Industry standard 24 lead pinout**

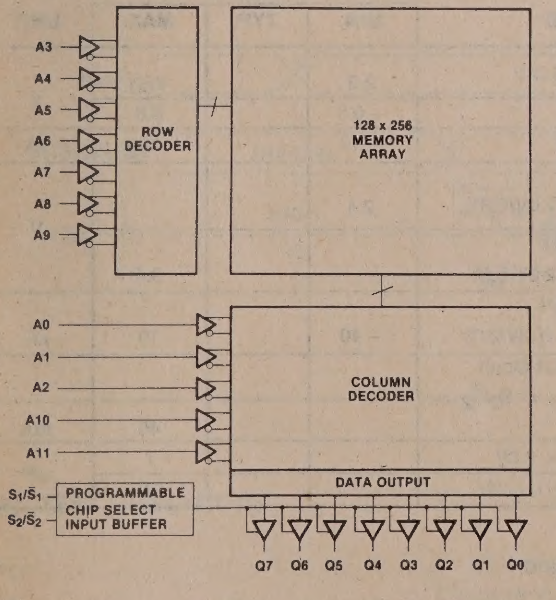
GENERAL DESCRIPTION

The IM7332 is a 32,768 bit read-only memory (ROM) organized 4096 words by 8 bits. The device is fabricated using Intersil's HMOS technology to minimize cell area and optimize circuit performance.

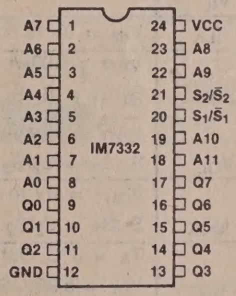
Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. Two chip select inputs which are programmable to either active high or active low, facilitate ease of memory expansion.

The IM7332 operates over 5V ±5% at 45mA with an access time of 300ns.

LOGICAL BLOCK DIAGRAM

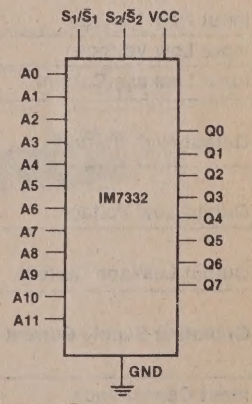

A3
A4
A5
A6
A7
A8
A9
ROW DECODER
128 x 256 MEMORY ARRAY
A0
A1
A2
A10
A11
COLUMN DECODER
DATA OUTPUT
$S_1/\overline{S}_1$
$S_2/\overline{S}_2$
PROGRAMMABLE CHIP SELECT INPUT BUFFER
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0

PIN CONFIGURATION


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 VCC
23 A8
22 A9
21 $S_2/\overline{S}_2$
20 $S_1/\overline{S}_1$
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
IM7332

(outline dwgs JG, PG)

LOGIC SYMBOL


$S_1/\overline{S}_1$ $S_2/\overline{S}_2$ VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
IM7332
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
GND

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
IM7332CPG	24 Pin PLASTIC	0°C to +70°C
IM7332 CJG	24 Pin CERDIP	0°C to +70°C

NOTE: Plastic package not yet available — pending qualification

PIN NAMES

$A_0 - A_{11}$	ADDRESS INPUTS
$Q_0 - Q_7$	DATA OUTPUTS
$S_1/\overline{S}_1$, $S_2/\overline{S}_2$	PROGRAMMABLE CHIP SELECTS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Voltage on Any Pin Relative to GND	−0.5V to +7.0V
Commercial Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TEST CONDITIONS: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $+70°C$

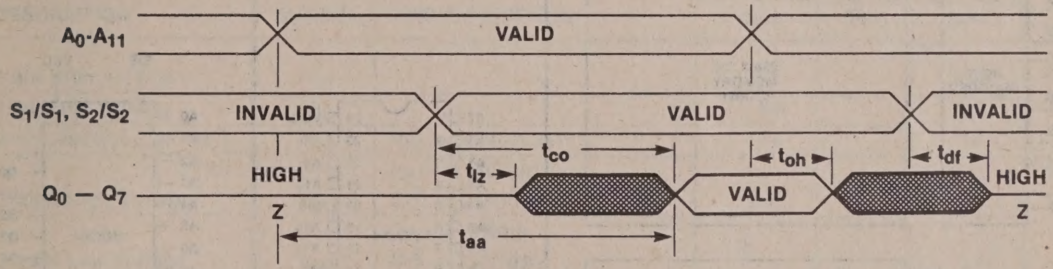
DESCRIPTION	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		−0.5		0.8	
Input Leakage Current	I_{ILK}	$V_{IN} = 0V$ to 5.25V	−10		10	μA
Output High Voltage	V_{OH}	$I_{OUT} = -100\mu A$ $S_1/\bar{S}_1 = S_2/\bar{S}_2 = 2.0V/0.8V$	2.4			V
Output Low Voltage	V_{OL}	$I_{OUT} = 1.6mA$ $S_1/\bar{S}_1 = S_2/\bar{S}_2 = 2.0V/0.8V$			0.4	
Output Leakage Current	I_{OLK}	$V_{OUT} = 0V$ to 5.25V $S_1/\bar{S}_1 = S_2/\bar{S}_2 = 0.8V/2.0V$	−10		10	μA
Operating Supply Current	I_{CC}	$T_A = 0°C$, Data Out Open $V_{IN} = 5.25V$, $S_1/\bar{S}_1 = S_2/\bar{S}_2 =$ 2.0V/0.8V			45	mA
Input Capacitance	C_{IN}	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$			7	pF
Output Capacitance	C_{OUT}	$V_{CC} = 5.0V$, $V_{OUT} = 2.0V$			10	

NOTE: 1. Typical values are measured at $V_{CC} = 5.0V$ and $T_A = +25°C$.
2. Capacitance values are sampled, not 100% tested.

AC CHARACTERISTICS

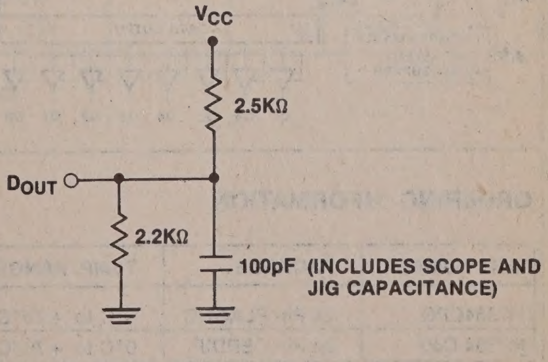
DESCRIPTION	SYMBOL	JEDEC SYMBOL	MIN	TYP	MAX	UNIT
Address Access Time	t_{aa}	TAVQV			300	ns
Chip Select to Low Impedance	t_{lz}	TSVQX	20			
Chip Select Delay	t_{co}	TSVQV			100	
Chip Deselect Delay	t_{df}	TSXQZ			100	
Output Hold Time	t_{oh}	TAXQX	20			

READ CYCLE TIMING


A_0-A_{11}
VALID
$S_1/\overline{S_1}$, $S_2/\overline{S_2}$
INVALID
VALID
INVALID
t_{co}
t_{oh}
t_{df}
HIGH
t_{lz}
HIGH
Q_0 — Q_7
VALID
Z
Z
t_{aa}

AC TEST CONDITIONS

V_{CC} .... 5V ± 5%
T_A .... 0°C to 70°C
Input rise and fall times .... 20ns (10% to 90%)
Input and output reference level 1.5V


V_{CC}
2.5KΩ
D_{OUT}
2.2KΩ
100pF (INCLUDES SCOPE AND JIG CAPACITANCE)

OUTPUT LOAD CIRCUIT

PRELIMINARY
Specifications Subject To Change Without Notice

IM7364
65,536 BIT (8192 x 8) HMOS ROM

FEATURES

- **High Speed — 350ns Maximum access time**
- **Completely static — no clock required**
- **Single +5V supply**
- **Fully TTL Compatible**
- **Two Programmable Chip Select**
- **Three-state outputs**
- **Industry standard 24 lead pinout**

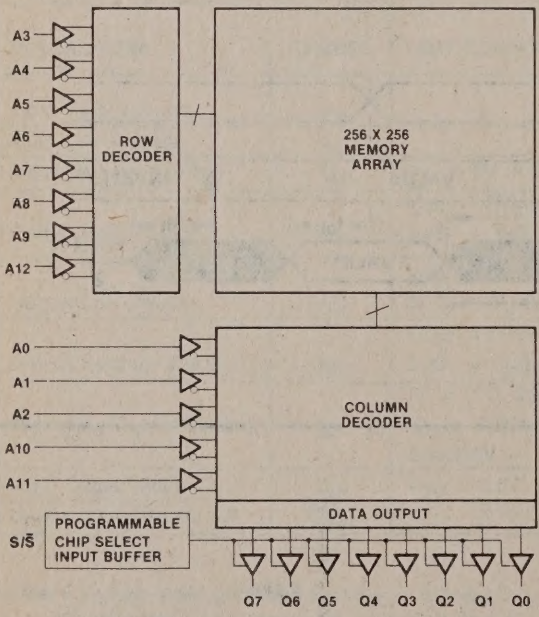
GENERAL DESCRIPTION

The IM7364 is a 65,536 bit read-only memory (ROM) organized 8192 words by 8 bits. The device is fabricated using Intersil's HMOS technology to minimize cell area and optimize circuit performance.

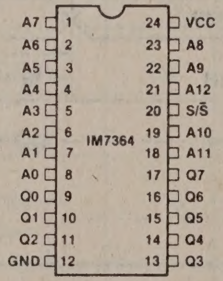
Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. A chip select input, which is programmable to either active high or active low, facilitates ease of memory expansion.

The IM7364 operates over 5V ± 5% at 60mA with an access time of 350ns.

LOGICAL BLOCK DIAGRAM

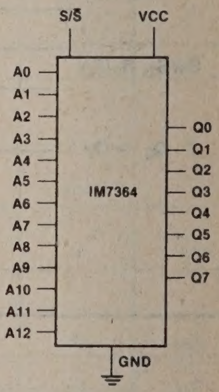

A3
A4
A5
A6
A7
A8
A9
A12
ROW DECODER
256 X 256 MEMORY ARRAY
A0
A1
A2
A10
A11
COLUMN DECODER
DATA OUTPUT
S/S̄
PROGRAMMABLE CHIP SELECT INPUT BUFFER
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

PIN CONFIGURATION


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
IM7364
24 VCC
23 A8
22 A9
21 A12
20 S/S̄
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

(outline dwgs JG, PG)

LOGIC SYMBOL


S/S̄
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
IM7364
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
GND

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
IM7364CPG	24 Pin PLASTIC	0°C to +70°C
IM7364 CJG	24 Pin CERDIP	0°C to +70°C

NOTE: Plastic package not yet available – pending qualification

PIN NAMES

$A_0 - A_{12}$	ADDRESS INPUTS
$Q_0 - Q_7$	DATA OUTPUTS
S/S̄	PROGRAMMABLE CHIP SELECT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Voltage on Any Pin Relative to GND	−0.5V to +7.0V
Commercial Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $+70°C$

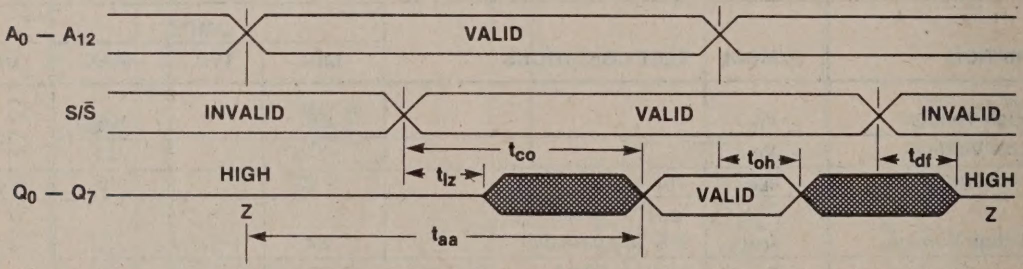
DESCRIPTION	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		−0.5		0.8	
Input Leakage Current	I_{ILK}	V_{IN} = 0V to 5.25V	−10		10	μA
Output High Voltage	V_{OH}	$I_{OUT} = -100\mu A$ S/$\overline{S}$ = 2.0V/0.8V	2.4			V
Output Low Voltage	V_{OL}	I_{OUT} = 1.6mA S/$\overline{S}$ = 2.0V/0.8V			0.4	
Output Leakage Current	I_{OLK}	V_{OUT} = 0V to 5.25V S/$\overline{S}$ = 0.8V/2.0V	−10		10	μA
Operating Supply Current	I_{CC}	T_A = 0°C, Data Out Open V_{IN} = 5.25V, S/$\overline{S}$ = 2.0V/0.8V			60	mA
Input Capacitance	C_{IN}	V_{CC} = 5.0V, V_{IN} = 2.0V			7	pF
Output Capacitance	C_{OUT}	V_{CC} = 5.0V, V_{OUT} = 2.0V			10	

NOTE: 1. Typical values are measured at V_{CC} = 5.0V and T_A = +25°C.
2. Capacitance values are sampled, not 100% tested.

AC CHARACTERISTICS

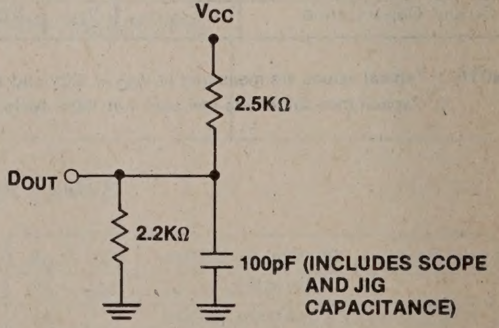
DESCRIPTION	SYMBOL	JEDEC SYMBOL	MIN	TYP	MAX	UNIT
Address Access Time	t_{aa}	TAVQV			350	ns
Chip Select to Low Impedance	t_{lz}	TSVQX	20			
Chip Select Delay	t_{co}	TSVQV			120	
Chip Deselect Delay	t_{df}	TSXQZ			120	
Output Hold Time	t_{oh}	TAXQX	20			

READ CYCLE TIMING


$A_0 - A_{12}$
VALID
S/S̄
INVALID
VALID
INVALID
t_{co}
t_{oh}
t_{df}
t_{lz}
HIGH
$Q_0 - Q_7$
VALID
HIGH
Z
Z
t_{aa}

AC TEST CONDITIONS

V_{CC} .... 5V ± 5%
T_A .... 0°C to 70°C
Input rise and fall times .... 20ns (10% to 90%)
Input and output reference level 1.5V


V_{CC}
2.5KΩ
D_{OUT}
2.2KΩ
100pF (INCLUDES SCOPE AND JIG CAPACITANCE)

OUTPUT LOAD CIRCUIT

ADVANCE INFORMATION
Specifications Subject To Change Without Notice

IM82C43
CMOS Input/Output Expander

FEATURES

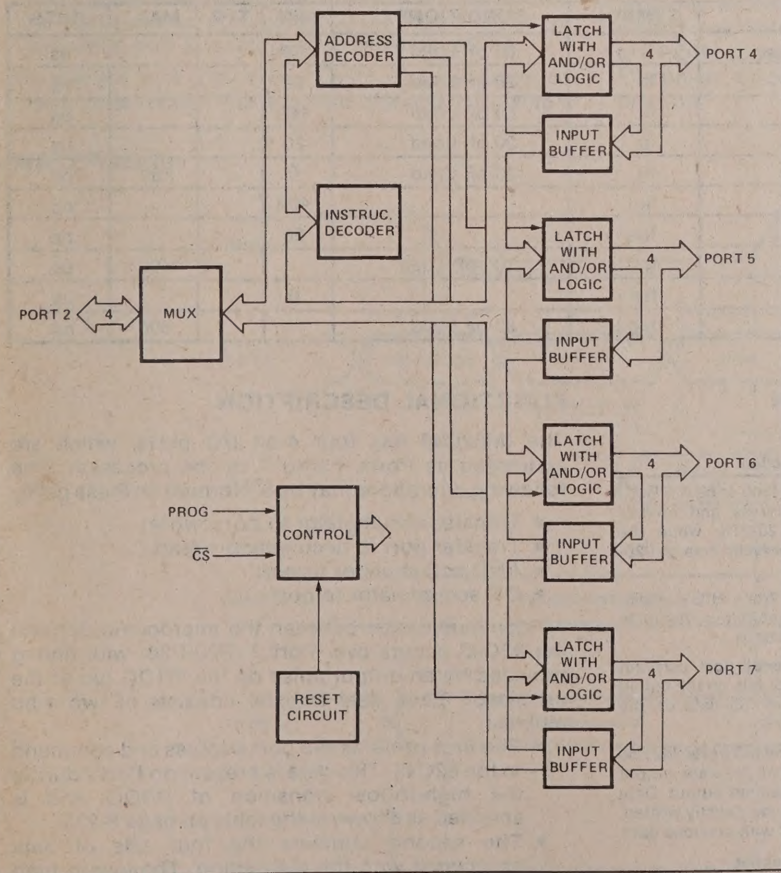
- **8048/41 compatible I/O expander**
- **CMOS pin-for-pin replacement for standard NMOS 8243**
- **Low power dissipation — typically 25mW active**
- **Extended temperature range: -40° C to +85° C**
- **Four 4-bit I/O ports in 24-pin DIP**
- **Logical AND/OR directly to ports**
- **High output drive**
- **High noise immunity — typically 33%**
- **Single +5V supply**

DESCRIPTION

The Intersil IM82C43 is a CMOS input/output expander equivalent to the NMOS 8243. It is designed to provide I/O expansion for the 8048, and 8041 single-chip microcomputers.

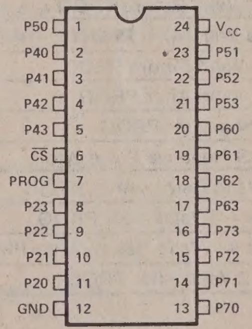
The 24-pin IM82C43 provides four 4-bit bidirectional I/O ports; 8048/41 instructions implement accumulator/IM82C43 port transfers, as well as logical AND/OR operations. P20-P23 on the 8048/41 serves as a 4-bit bus for transfer of control and data to the IM82C43.

LOGICAL BLOCK DIAGRAM


ADDRESS DECODER
INSTRUC. DECODER
PORT 2
4
MUX
PROG
CS̄
CONTROL
RESET CIRCUIT
LATCH WITH AND/OR LOGIC
INPUT BUFFER
4
PORT 4
PORT 5
PORT 6
PORT 7

PIN CONFIGURATION

(OUTLINE DRAWING JG, PG)


P50 1
P40 2
P41 3
P42 4
P43 5
CS̄ 6
PROG 7
P23 8
P22 9
P21 10
P20 11
GND 12
24 VCC
23 P51
22 P52
21 P53
20 P60
19 P61
18 P62
17 P63
16 P73
15 P72
14 P71
13 P70

8

ORDERING INFORMATION

PART NO.	PACKAGE
IM82C43IJG	24 PIN CERDIP
IM82C43IPG	24 PIN PLASTIC

ABSOLUTE MAXIMUM RATINGS

Operating Temperature .... -40°C to +85°C
Storage Temperature .... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground .. Ground -0.5 to V_{CC} +0.5
Power Dissipation .... 1 W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Low Voltage	V_{IL}		-0.5		0.8	V
Input High Voltage	V_{IH}		V_{CC} -2.0		V_{CC}+0.5	V
Output Low Voltage Ports 4-7	V_{OL}	I_{OL} = 30mA			0.40	V
Output High Voltage Ports 4-7	V_{OH}	I_{OH} = 240μA	2.8			V
Input Leakage Ports 4-7, Port 2, CS, PROG	I_{ILK}	V_{in} = V_{CC} to 0V	-1.0		1.0	μA
Output Low Voltage Port 2	V_{OL}	I_{OL} = 0.6 mA			0.1	V
Supply Current	I_{CC}	WRITE mode, All outputs open, t_K = 700ns		1	5.0	mA
Output Voltage Port 2	V_{OH}	I_{OH} = 100μA	2.8			mA
Sum of all I_{OL} from 16 Outputs	I_{OL}	10mA Each Pin			160	

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Code Valid Before PROG	t_A	80 pF Load	100			ns
Code Valid After PROG	t_B	20 pF Load	60			ns
Data Valid Before PROG	t_C	80 pF Load	140			ns
Data Valid After PROG	t_D	20 pF Load	20			ns
Floating After PROG	t_H	20 pF Load	0		150	ns
PROG Negative Pulse Width	t_K		400			ns
$\overline{CS}$ Valid Before/After PROG	t_{OS}		50			ns
Ports 4-7 Valid After PROG	t_{PO}	100 pF Load			400	ns
Ports 4-7 Valid Before/After PROG	t_{LP1}		0			ns
Port 2 Valid After PROG	t_{ACC}	80 pF Load			500	ns

FUNCTIONAL PIN DESCRIPTION

Designator	Pin Number	Function
PROG	7	**Clock input.** The falling edge of PROG indicates valid address and control information on P20-P23, while the rising edge indicates valid data on P20-P23.
$\overline{CS}$	6	**Chip select input.** When HIGH, it disables PROG, thus inhibiting change in output or internal status.
P20-P23	8-11	**Four bit bidirectional port** carrying address and control bits on the falling edge of PROG and I/O data on the rising edge of PROG.
P40-P43 P50-P53 P60-P63 P70-P73	2-5 1,21-23 17-20 13-16	**Four bit bidirectional I/O ports.** May be configured for input, tri-state output (READ mode) or latched output. Data on pins P20-23 may be directly written, or ANDed or ORed with previous data.
GND	12	**Circuit ground potential**
Vcc	24	**+5 volt supply.**

FUNCTIONAL DESCRIPTION

The IM82C43 has four 4-bit I/O ports, which are addressed as Ports 4 thru 7 by the processor. The following operations may be performed on these ports:

- Transfer accumulator to port (write)
- Transfer port to accumulator (read)
- AND accumulator to port
- OR accumulator to port

All communication between the microcomputer and the 82C43 occurs over Port 2 (P20-P23) with timing provided by an output pulse on the PROG pin of the processor. Each data transfer consists of two 4-bit nibbles:

- The first contains the port address and command to the 82C43. This data is present on Port 2 during the high-to-low transition of PROG and is encoded as shown in the table on page 8-235.
- The second contains the four bits of data associated with the instruction. The low-to-high transition of PROG indicates the presence of data.

Port Address And Command Format

P23	P22	INSTRUCTION CODE	P21	P20	ADDRESS CODE
0	0	Read	0	0	Port 4
0	1	Write	0	1	Port 5
1	0	ORLD	1	0	Port 6
1	1	ANLD	1	1	Port 7

Write Modes

The device has three write modes. MOVD P,A directly writes new data into the selected port with old data being lost; ORLD P,A ORs the new data with the old data and writes it to the port; and ANLD P,A ANDs new data with old data and writes it to the port.

After the designated operation is performed, the data is latched and directed to the port. The old data remains latched until the new data is written.

Read Mode

The device has one read mode. The command and port address are latched from port 2 on the high-to-low transition of the PROG pin. As soon as the read operation and port address are decoded, the designated port output buffers are disabled and the input buffers enabled. The read operation is terminated by the low-to-high transition of the PROG pin. The port selected is switched to the high impedance state while port 2 is returned to the input mode.

Normally a port will be in an output mode (write) or input mode (read). The first read of a port, following a mode change from write to read should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the 82C43 output. A read of any port will leave that port in a high impedance state.

I/O Expansion

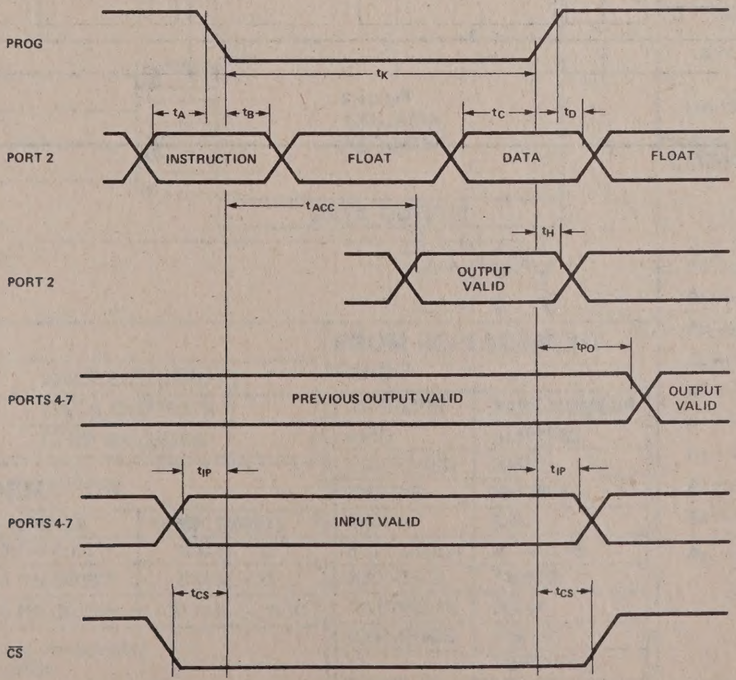
The use of a single 82C43 with an 80C48 or 8021 is shown in figure 1. If more ports are required, more 82C43s can be added as shown in figure 2. Here, the upper nibble of port 2 is used to select one of the 82C43s. Two lines could have been decoded but that would require additional hardware. Assuming that the leftmost 82C43 chip select is connected to P24, the instructions to select and de-select would be:

```
MOV A, #OEFH        P24 = 0
OUTL P2, A          Enable 82C43
.
.
.
MOV A, #OFFH        Disable All
OUTL P2, A          Send It
```

Power On Initialization

Initial application of power to the device forces ports 4, 5, 6, and 7 to the high impedance state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high-to-low transition of PROG causes the device to exit the power-on mode. The power-on sequence is initiated if V_{CC} drops below one volt.

WAVEFORMS



TYPICAL APPLICATIONS

EXPANDER INTERFACE

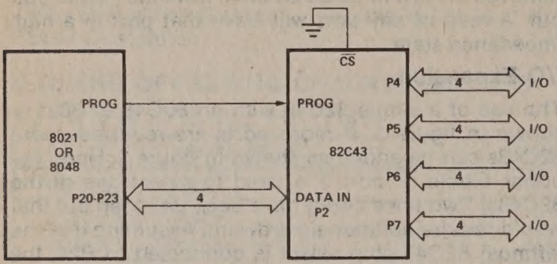
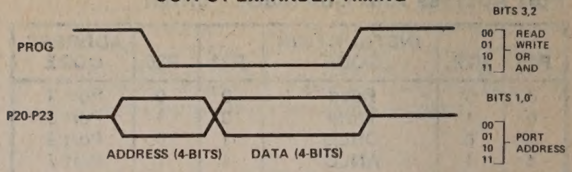

PROG
8021
OR
8048
P20-P23
4
CS
PROG
82C43
DATA IN
P2
P4
P5
P6
P7
4
I/O

Figure 1

OUTPUT EXPANDER TIMING


PROG
P20-P23
ADDRESS (4-BITS)
DATA (4-BITS)
BITS 3,2
00 READ
01 WRITE
10 OR
11 AND
BITS 1,0
00
01
10
11
PORT
ADDRESS

Note:
The 82C43 does not have the same quasi-bidirectional port structure as P1/P2 of the 80C48. When a "1" is written to P4-7 of the 82C43 it is a "hard 1" (low impedance to +5V) which cannot be pulled low by an external device. All 4 bits of any port can be switched from output mode to input mode by executing a dummy read which leaves the port in a high impedance (no pullup or pulldown) state.

USING MULTIPLE 82C43s

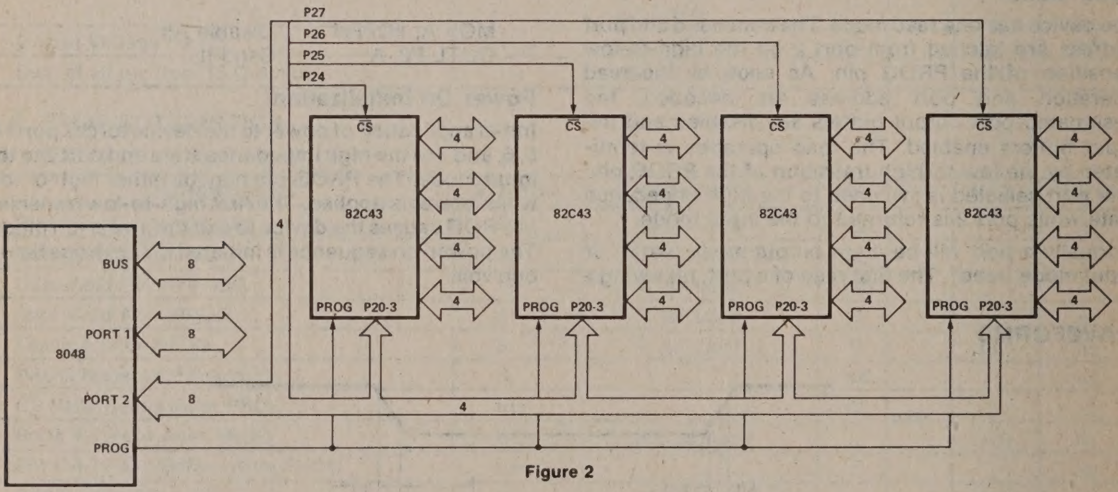

P27
P26
P25
P24
CS
82C43
PROG P20-3
4
BUS
8
PORT 1
8
8048
PORT 2
8
PROG

Figure 2

INTERSIL

ADVANCE INFORMATION
Specifications Subject To Change Without Notice

82HM137
4096 BIT
(1024 x 4) HMOS ROM

FEATURES

- **High speed — 70ns maximum access time**
- **Low Power 630mW (82HM137C)**
- **Completely static — no clock required**
- **Single +5V supply**
- **Fully TTL compatible**
- **Two Chip Select inputs**
- **Three-state outputs**
- **883B processing available**
- **Mil temp operation (−55°C to +125°C) available**
- **Pinout and functionally compatible to industry standard Bipolar PROMS, using only 75% the power**

GENERAL DESCRIPTION

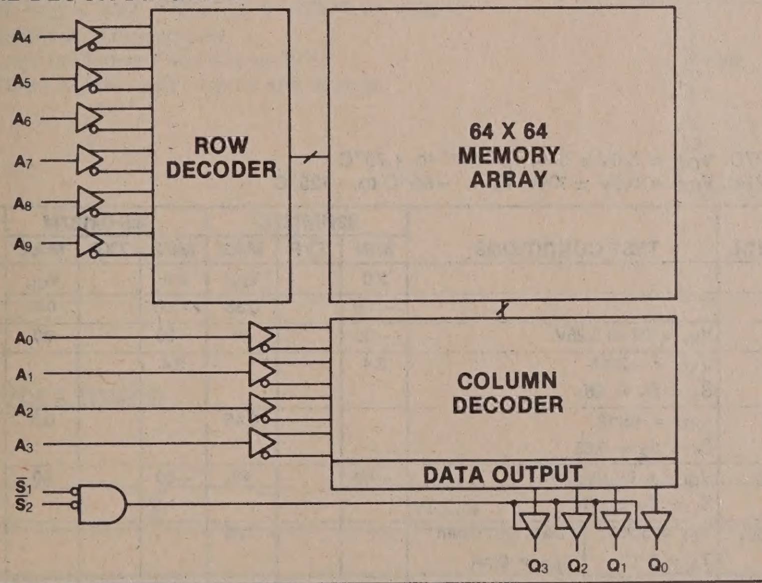
The 82HM137 is a high speed 4096 bit read-only memory (ROM) organized 1024 words by 4 bits. The device is fabricated using Intersil's SELOX HMOS technology, a single-layer polysilicon, selective-oxidation arsenic diffusion process, to minimize memory cell area and optimize circuit performance.

The 82HM137 is an exact pinout and function replacement for industry standard 1024 x 4 Bipolar PROMs.

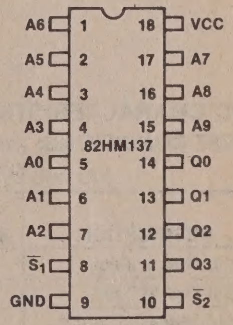
Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. Two chip select inputs allow for ease of memory expansion.

The standard 82HM137 operates over 5V ±5% at 120mA with an access time of 70ns.

LOGICAL BLOCK DIAGRAM

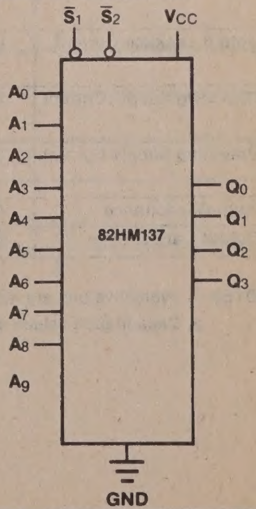

A4
A5
A6
A7
A8
A9
ROW DECODER
64 X 64 MEMORY ARRAY
A0
A1
A2
A3
COLUMN DECODER
DATA OUTPUT
S̄1
S̄2
Q3
Q2
Q1
Q0

PIN CONFIGURATION


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
S̄1 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 Q0
13 Q1
12 Q2
11 Q3
10 S̄2
82HM137

(outline dwgs JN, PN)

LOGIC SYMBOL


S̄1
S̄2
Vcc
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
82HM137
Q0
Q1
Q2
Q3
GND

PIN NAMES

A_0-A_9	ADDRESS INPUTS
Q_0-Q_3	DATA OUTPUTS
$\bar{S}_1$, $\bar{S}_2$	CHIP SELECTS

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
82HM137CPN	18 PIN PLASTIC	0°C to +75°C
82HM137CJN	18 PIN CERDIP	0°C to +75°C
82HM137MJN/883B	18 PIN CERDIP	−55°C to +125°C

NOTE: Plastic package not yet available
- pending qualification

PROM REPLACEMENT GUIDE

SUPPLIER	PART NUMBER
AMD	AM27S33
FAIRCHILD	93453
HARRIS	HM7643
MMI	6353
MOTOROLA	MCM7643
NATIONAL	74S573
RAYTHEON	29641
SIGNETICS	82S137
TI	TBP24S41

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7V
Voltage On Any Pin Relative to GND	−0.5V to +7.0V
Commercial Operating Temperature Range	0° to +75°C
Military Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: 82HM137C: $V_{CC} = 5.0V \pm 5\%$, $T_A = 0°$ to $+75°C$
82HM137M: $V_{CC} = 5.0V \pm 10\%$, $T_A = -55°C$ to $+125°C$

DESCRIPTION	SYMBOL	TEST CONDITIONS	82HM137C MIN	82HM137C TYP	82HM137C MAX	82HM137M MIN	82HM137M TYP	82HM137M MAX	UNITS
Input High Voltage	V_{IH}		2.0		V_{CC}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}		−1.0		0.85	−1.0		0.8	
Input Leakage Current	I_{ILK}	V_{IN} = 0V to 5.25V	−20		20	−20		20	µA
Output High Voltage	V_{OH}	$I_{OUT} = -2mA$ $\overline{S}_1 = \overline{S}_2 = .85V$	2.4			2.4			V
Output Low Voltage	V_{OL}	$I_{OUT} = 16mA$ $\overline{S}_1 = \overline{S}_2 = 0.85$			0.45			0.5	
Output Leakage Current	I_{OLK}	V_{OUT} = 0V to 5.25V $\overline{S}_1 = \overline{S}_2 = 2.0V$	−40		40	−60		60	µA
Operating Supply Current	I_{CCOP_1}	$V_{IN} = 5.25V$ $T_A = 0°C$ Data Out Open $I_{I/O} = 0mA$ $\overline{S}_1 = \overline{S}_2 = 0.85V$			120				mA
Operating Supply Current	I_{CCOP_2}	$V_{IN} = 5.5V$ $T_A = -55°C$						130	
Input Capacitance	C_{IN}	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$		5			5		pF
Output Capacitance	C_{OUT}	$V_{CC} = 5.0V$, $V_{OUT} = 2.0V$		8			8		

NOTES: 1. Typical values are measured at $V_{CC} = 5.0V$ and $T_A = +25°C$
2. Capacitance values are sampled, not 100% tested.

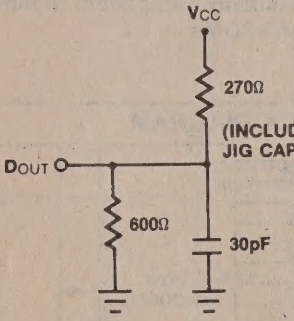
AC CHARACTERISTICS

DESCRIPTION	SYMBOL	JEDEC SYMBOL	82HM137C TYP	82HM137C MAX	82HM137M TYP	82HM137M MAX	UNITS
Address Access Time	t_{aa}	TAVQV	60	70	70	80	ns
Chip Enable Access Time	t_{ce}	TSVQV	30	40	30	40	
Output Disable Time	t_{cd}	TSXQZ	30	40	30	40	

NOTE: Superior speed selection is available

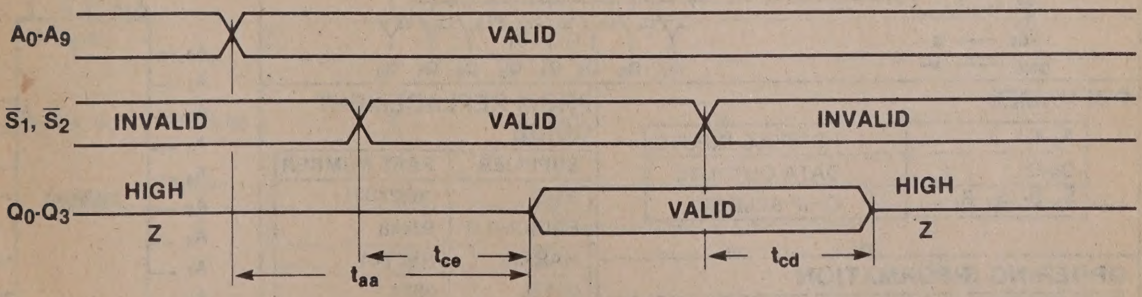
AC TEST CONDITIONS

82HM137C: V_{CC} = 5.0V ± 5%, T_A = 0° to +75°C
82HM137M: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C
Input pulse levels - 0.0V and 3.0V
Input rise and fall times - 5ns (10% to 90%)
Timing reference level - 1.5V - Inputs and outputs


VCC
270Ω
(INCLUDES SCOPE AND JIG CAPACITANCE)
DOUT
600Ω
30pF

OUTPUT LOAD CIRCUIT

READ CYCLE TIMING


A0-A9
VALID
S1, S2
INVALID
VALID
INVALID
Q0-Q3
HIGH
Z
VALID
HIGH
Z
tce
taa
tcd

INTERSIL

82HM141
4096 Bit
(512 x 8) HMOS ROM

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

- **High speed-70ns maximum access time**
- **Completely static - no clock required**
- **Single +5V supply**
- **Fully TTL compatible**
- **Four chip select inputs**
- **Three-state outputs**
- **883B processing available**
- **Mil temp operation (–55°C to +125°C) available**
- **Pinout and functionally compatible to industry standard Bipolar PROMs**

GENERAL DESCRIPTION

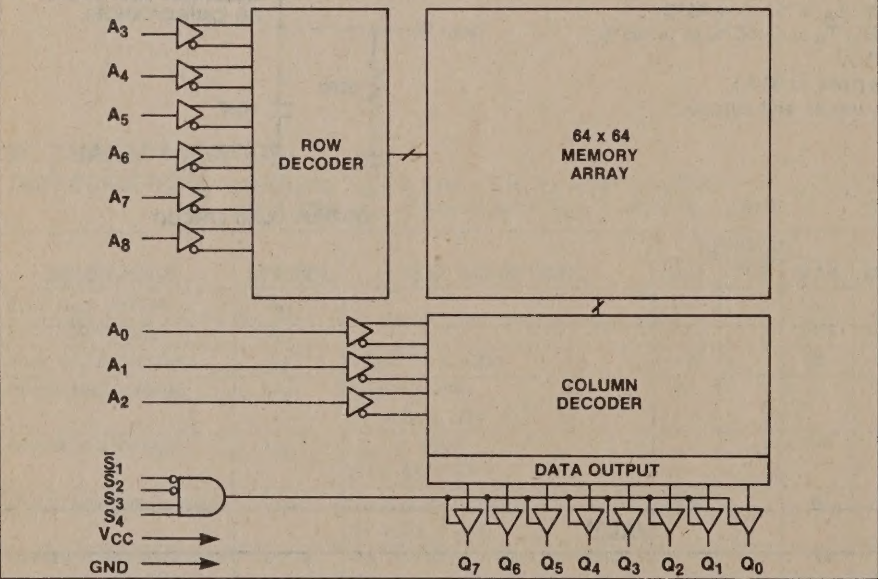
The 82HM141 is a high speed 4,096 bit read-only memory (ROM) organized 512 words by 8 bits. The device is fabricated using Intersil's SELOX HMOS technology, a single-layer polysilicon, selective-oxidation arsenic diffusion process, to minimize memory cell area and optimize circuit performance.

The 82HM141 is an exact pinout and functional replacement for industry standard 512 x 8 Bipolar PROMs.

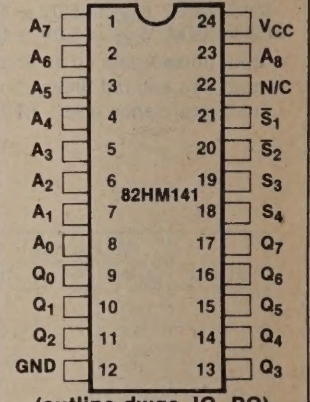
Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. Four chip select inputs allow for ease of memory expansion.

The standard 82HM141 operates over 5V ± 5% at 175mA with an access time of 70ns.

LOGICAL BLOCK DIAGRAM

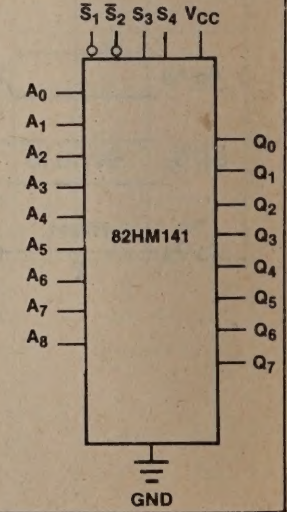

A3
A4
A5
A6
A7
A8
ROW DECODER
64 x 64 MEMORY ARRAY
A0
A1
A2
COLUMN DECODER
DATA OUTPUT
S̄1
S̄2
S3
S4
VCC
GND
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0

PIN CONFIGURATION


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 VCC
23 A8
22 N/C
21 S̄1
20 S̄2
19 S3
18 S4
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
82HM141

(outline dwgs JG, PG)

LOGIC SYMBOL


S̄1 S̄2 S3 S4 VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
82HM141
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
GND

PIN NAMES

A_0-A_8	ADDRESS INPUTS
Q_0-Q_7	DATA OUTPUTS
$\bar{S}_1$, $\bar{S}_2$, S_3, S_4	CHIP SELECTS

PROM REPLACEMENT GUIDE

SUPPLIER	PART NUMBER
AMD	AM27S31
FAIRCHILD	93448
HARRIS	HM7641
INTEL	3624
MMI	6341
NATIONAL	87S296
RAYTHEON	29625
SIGNETICS	82S141
TI	TBP28S45

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
82HM141 CPG	24 Pin PLASTIC	0°C to +75°C
82HM141 CJG	24 Pin CERDIP	0°C to +75°C
82HM141 MJG/883B	24 Pin CERDIP	–55°C to +125°C

NOTE: Plastic package not yet available
- pending qualification

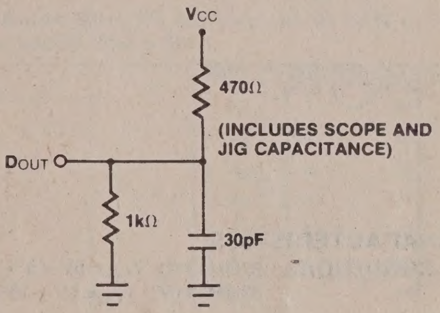
AC CHARACTERISTICS

DESCRIPTION	SYMBOL	JEDEC SYMBOL	82HM141C		82HM141M		UNITS
			TYP	MAX	TYP	MAX	
Address Access Time	t_{aa}	TAVQV		70		90	ns
Chip Enable Access Time	t_{ce}	TSVQV		40		50	
Output Disable Time	t_{cd}	TSXQZ		40		50	

NOTE: Superior speed selection is available

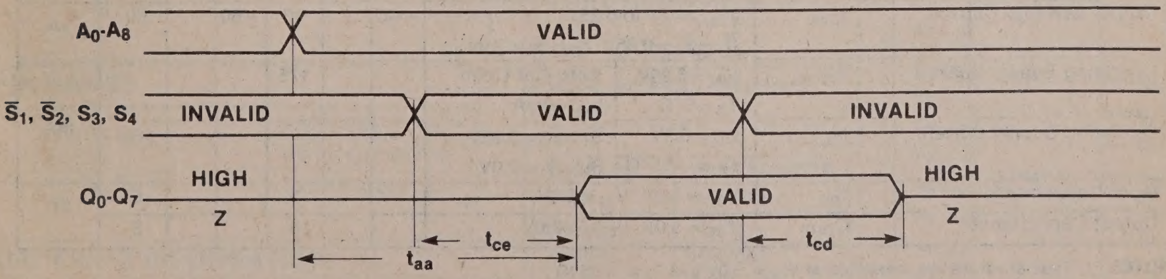
AC TEST CONDITIONS

82HM141C: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $+75°C$
82HM141M: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$
Input pulse levels - 0.0V and 3.0V
Input rise and fall times - 5ns (10% to 90%)
Timing reference level - 1.5V - Inputs and outputs


V_{CC}
470Ω
(INCLUDES SCOPE AND JIG CAPACITANCE)
D_{OUT}
1kΩ
30pF

OUTPUT LOAD CIRCUIT

READ CYCLE TIMING


A_0-A_8
VALID
$\overline{S}_1, \overline{S}_2, S_3, S_4$
INVALID
VALID
INVALID
Q_0-Q_7
HIGH
Z
VALID
HIGH
Z
t_{ce}
t_{aa}
t_{cd}

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Voltage On Any Pin Relative to GND	−0.5V to +7.0V
Commercial Operating Temperature Range	0°C to +75°C
Military Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: 82HM141C: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $+75°C$
82HM141M: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$

DESCRIPTION	SYMBOL	TEST CONDITIONS	82HM141C			82HM141M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input High Voltage	V_{IH}		2.0		V_{CC}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}		−1.0		0.85	−1.0		0.80	
Input Leakage Current	I_{ILK}	$V_{IN} =$ 0V to 5.25V	−20		20	−20		20	μA
Output High Voltage	V_{OH}	$I_{OUT} = -2mA$ $\overline{S}_1 = \overline{S}_2 = 0.85V$, $S_3 = S_4 = 2.0V$	2.4			2.4			V
Output Low Voltage	V_{OL}	$I_{OUT} = 9.6mA$ $\overline{S}_1 = \overline{S}_2 = 0.85V$, $S_3 = S_4 = 2.0V$			0.45			0.5	
Output Leakage Current	I_{OLK}	$V_{OUT} = 0V$ to 5.25V $\overline{S}_1 = \overline{S}_2 = 0.85V$, $S_3 = S_4 = 2.0V$	−40		40	−60		60	μA
Operating Supply Current	I_{CCOP_1}	$V_{IN} = 5.25V$ $T_A = 0°C$ Data Out Open $I_{I/O} = 0mA$ $\overline{S}_1 = \overline{S}_2 = 0.85V$ $S_3 = S_4 = 2.0V$			175				mA
Operating Supply Current	I_{CCOP_2}	$V_{IN} = 5.5V$ $T_A = -55°C$						185	
Input Capacitance	C_{IN}	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$			5			5	pF
Output Capacitance	C_{OUT}	$V_{CC} = 5.0V$, $V_{OUT} = 2.0V$			8			8	

NOTES: 1. Typical values are measured at $V_{CC} = 5.0V$ and $T_A = +25°C$
2. Capacitance values are sampled, not 100% tested.

INTERSIL

PRELIMINARY
Specifications Subject To Change Without Notice

82HM181
8192 Bit
(1024 x 8) HMOS ROM

FEATURES

- High speed- 70ns maximum access time
- Completely static - no clock required
- Single +5V supply
- Fully TTL compatible
- Four chip select inputs
- Three-state outputs
- 883B processing available
- Mil temp operation (−55°C to +125°C) available
- Pinout and functionally compatible to industry standard Bipolar PROMs

GENERAL DESCRIPTION

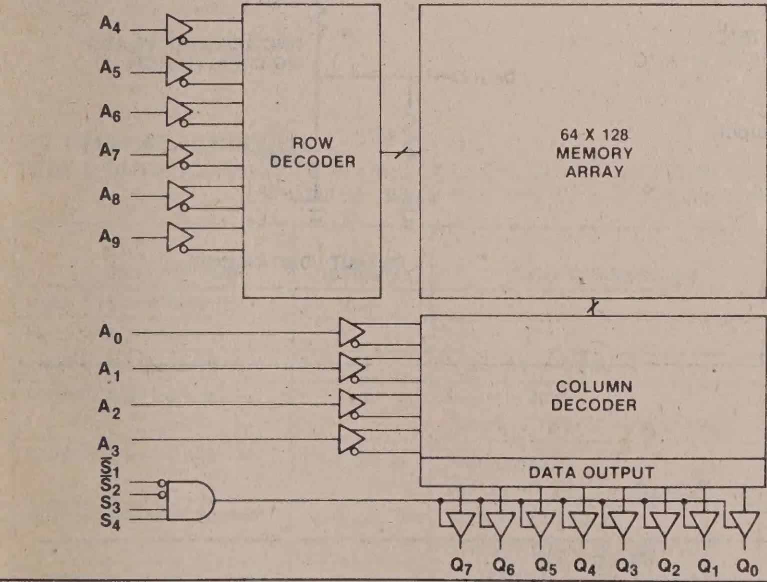
The 82HM181 is a high speed 8,192 bit read-only memory (ROM) organized 1024 words by 8 bits. The device is fabricated using Intersil's SELOX HMOS technology, a single-layer polysilicon, selective-oxidation arsenic diffusion process, to minimize memory cell area and optimize circuit performance.

The 82HM181 is an exact pinout and functional replacement for industry standard 1k x 8 Bipolar PROMs.

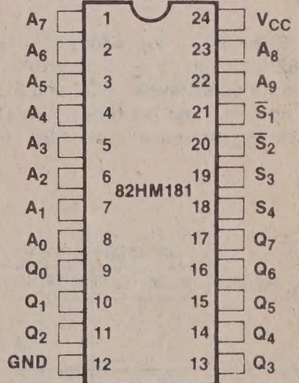
Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. Four chip select inputs allow for ease of memory expansion.

The standard 82HM181 operates over 5V ±5% at 175mA with an access time of 70ns.

LOGICAL BLOCK DIAGRAM


A_4
A_5
A_6
A_7
A_8
A_9
ROW DECODER
64 X 128 MEMORY ARRAY
A_0
A_1
A_2
A_3
COLUMN DECODER
DATA OUTPUT
$\bar{S}_1$
$\bar{S}_2$
S_3
S_4
Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0

PIN CONFIGURATION


A_7 1
A_6 2
A_5 3
A_4 4
A_3 5
A_2 6
A_1 7
A_0 8
Q_0 9
Q_1 10
Q_2 11
GND 12
24 V_{CC}
23 A_8
22 A_9
21 $\bar{S}_1$
20 $\bar{S}_2$
19 S_3
18 S_4
17 Q_7
16 Q_6
15 Q_5
14 Q_4
13 Q_3
82HM181

(outline dwgs JG, PG)

PIN NAMES

A_0-A_9	ADDRESS INPUTS
Q_0-Q_7	DATA OUTPUTS
$\bar{S}_1$, $\bar{S}_2$, S_3, S_4	CHIP SELECTS

ORDERING INFORMATION

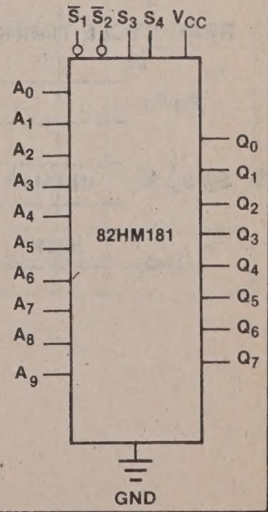
PART NUMBER	PACKAGE	TEMP. RANGE
82HM181 CPG	24 Pin PLASTIC	0°C to +75°C
82HM181 CJG	24 Pin CERDIP	0°C to +75°C
82HM181MJG/883B	24 Pin CERDIP	−55°C to +125°C

NOTE: Plastic package not yet available
- pending qualification

PROM REPLACEMENT GUIDE

SUPPLER	PART NUMBER
AMD	AM27S181
FAIRCHILD	93451
HARRIS	HM7681
INTEL	3628
MMI	63S881
NATIONAL	87S181
RAYTHEON	29631
SIGNETICS	82S181
TI	TBP28S86

LOGIC SYMBOL


$\bar{S}_1$ $\bar{S}_2$ S_3 S_4 V_{CC}
A_0
A_1
A_2
A_3
A_4
A_5
A_6
A_7
A_8
A_9
82HM181
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
GND

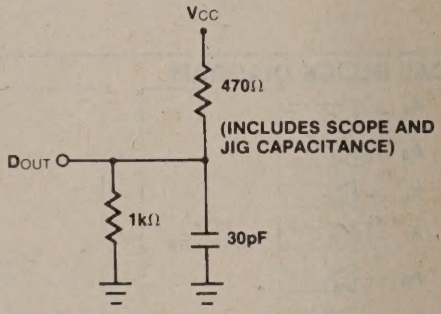
AC CHARACTERISTICS

DESCRIPTION	SYMBOL	JEDEC SYMBOL	82HM181C TYP	82HM181C MAX	82HM181M TYP	82HM181M MAX	UNITS
Address Access Time	t_{aa}	TAVQV		70		90	ns
Chip Enable Access Time	t_{ce}	TSVQV		40		50	
Output Disable Time	t_{cd}	TSXQZ		40		50	

NOTE: Superior speed selection is available

AC TEST CONDITIONS

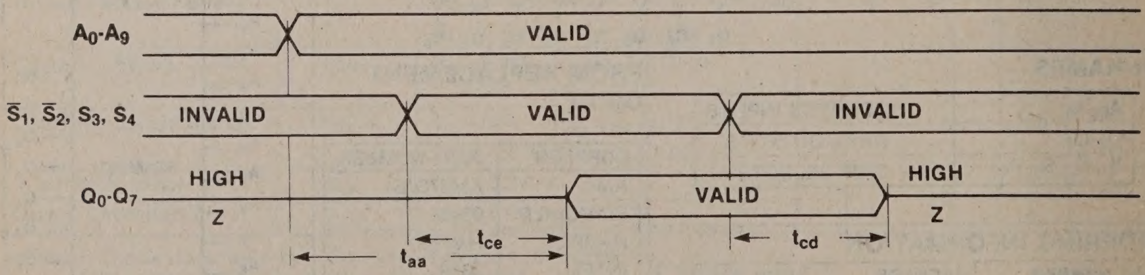
82HM181C: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $+75°C$
82HM181M: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$
Input pulse levels - 0.0V and 3.0V
Input rise and fall times - 5ns (10% to 90%)
Timing reference level - 1.5V - Inputs and outputs



V_{CC}
470Ω
(INCLUDES SCOPE AND JIG CAPACITANCE)
D_{OUT}
1kΩ
30pF

OUTPUT LOAD CIRCUIT

READ CYCLE TIMING



A_0-A_9
VALID
$\overline{S}_1$, $\overline{S}_2$, S_3, S_4
INVALID
VALID
INVALID
Q_0-Q_7
HIGH
Z
VALID
HIGH
Z
t_{ce}
t_{aa}
t_{cd}

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Voltage On Any Pin Relative to GND	−0.5V to +7.0V
Commercial Operating Temperature Range	0°C to +75°C
Military Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: 82HM181C: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $+75°C$
82HM181M: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$

DESCRIPTION	SYMBOL	TEST CONDITIONS		82HM181C			82HM181M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input High Voltage	V_{IH}			2.0		V_{CC}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}			−1.0		0.85	−1.0		0.80	
Input Leakage Current	I_{ILK}	$V_{IN} =$ 0V to 5.25V		−20		20	−20		20	µA
Output High Voltage	V_{OH}	$I_{OUT} = -2mA$ $\overline{S}_1 = \overline{S}_2 = 0.85V$, $S_3 = S_4 = 2.0V$		2.4			2.4			V
Output Low Voltage	V_{OL}	$I_{OUT} = 9.6mA$ $\overline{S}_1 = \overline{S}_2 = 0.85V$, $S_3 = S_4 = 2.0V$				0.45			0.5	
Output Leakage Current	I_{OLK}	$V_{OUT} = 0V$ to 5.25V $\overline{S}_1 = \overline{S}_2 = 0.85V$, $S_3 = S_4 = 2.0V$		−40		40	−60		60	µA
Operating Supply Current	I_{CCOP_1}	$V_{IN} = 5.25V$ $T_A = 0°C$	Data Out Open $I_{I/O} = 0mA$ $\overline{S}_1 = \overline{S}_2 = 0.85V$ $S_3 = S_4 = 2.0V$			175				mA
Operating Supply Current	I_{CCOP_2}	$V_{IN} = 5.5V$ $T_A = -55°C$							185	
Input Capacitance	C_{IN}	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$				5			5	pF
Output Capacitance	C_{OUT}	$V_{CC} = 5.0V$, $V_{OUT} = 2.0V$				8			8	

NOTES: 1. Typical values are measured at $V_{CC} = 5.0V$ and $T_A = +25°C$
2. Capacitance values are sampled, not 100% tested.

INTERSIL

82HM185
8192 BIT
(2048 x 4) HMOS ROM

ADVANCE INFORMATION
Specifications Subject To Change Without Notice

FEATURES

- High speed — 70ns maximum access time
- Low Power 630mW (82HM185C)
- Completely static — no clock required
- Single +5V supply
- Fully TTL compatible
- Chip Select input
- Three-state outputs
- 883B processing available
- Mil temp operation (−55°C to +125°C) available
- Pinout and functionally compatible to industry standard Bipolar PROMS, using only 75% the power

GENERAL DESCRIPTION

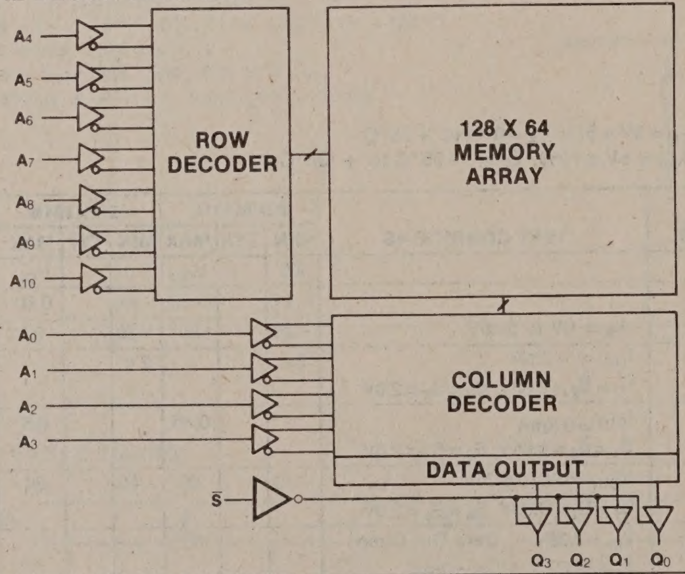
The 82HM185 is a high speed 8192 bit read-only memory (ROM) organized 2048 words by 4 bits. The device is fabricated using Intersil's SELOX HMOS technology, a single-layer polysilicon, selective-oxidation arsenic diffusion process, to minimize memory cell area and optimize circuit performance.

The 82HM185 is an exact pinout and function replacement for industry standard 2048 x 4 Bipolar PROMs.

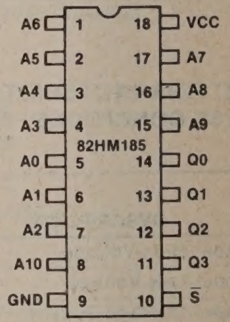
Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. A chip select input allows for ease of memory expansion.

The standard 82HM185 operates over 5V ±5% at 120mA with an access time of 70ns.

LOGICAL BLOCK DIAGRAM

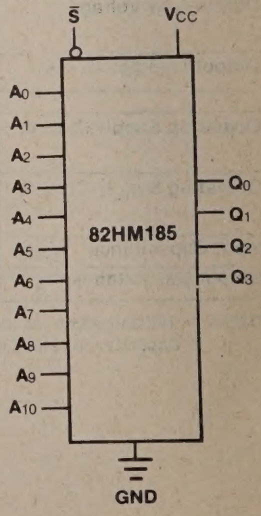

A4
A5
A6
A7
A8
A9
A10
ROW DECODER
128 X 64 MEMORY ARRAY
A0
A1
A2
A3
COLUMN DECODER
DATA OUTPUT
S̄
Q3
Q2
Q1
Q0

PIN CONFIGURATION


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
A10 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 Q0
13 Q1
12 Q2
11 Q3
10 S̄
82HM185

(outline dwgs JN, PN)

LOGIC SYMBOL


S̄
Vcc
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
82HM185
Q0
Q1
Q2
Q3
GND

PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
Q_0-Q_3	DATA OUTPUTS
$\overline{S}$	CHIP SELECT

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
82HM185CPN	18 PIN PLASTIC	0°C to +75°C
82HM185CJN	18 PIN CERDIP	0°C to +75°C
82HM185MJN/883B	18 PIN CERDIP	−55°C to +125°C

NOTE: Plastic package not yet available - pending qualification

PROM REPLACEMENT GUIDE

SUPPLIER	PART NUMBER
FUJITSU	MB7128
HARRIS	HM7685
MITSUBISHI	2708
MOTOROLA	MCM7685
NATIONAL	87S185
RAYTHEON	29651
SIGNETICS	82S185
TI	TBP24S81

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7V
Voltage On Any Pin Relative to GND	−0.5V to +7.0V
Commercial Operating Temperature Range	0° to +75°C
Military Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: 82HM185C: $V_{CC} = 5.0V \pm 5\%$, $T_A = 0°$ to $+75°C$
82HM185M: $V_{CC} = 5.0V \pm 10\%$, $T_A = -55°C$ to $+125°C$

DESCRIPTION	SYMBOL	TEST CONDITIONS	82HM185			82HM185			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input High Voltage	V_{IH}		2.0		V_{CC}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}		−1.0		0.85	−1.0		0.8	
Input Leakage Current	I_{ILK}	V_{IN} = 0V to 5.25V	−20		20	−20		20	μA
Output High Voltage	V_{OH}	$I_{OUT} = -2mA$ $\overline{S} = 0.85V$	2.4			2.4			V
Output Low Voltage	V_{OL}	$I_{OUT} = 16mA$ $\overline{S} = 0.85V$			0.45			0.5	
Output Leakage Current	I_{OLK}	V_{OUT} = 0V to 5.25V $\overline{S} = 2.0V$	−40		40	−60		60	μA
Operating Supply Current	I_{CCOP_1}	$V_{IN} = 5.25V$ $T_A = 0°C$ Data Out Open $I_{I/O} = 0mA$ $\overline{S} = 0.85V$			120				μA
Operating Supply Current	I_{CCOP_2}	$V_{IN} = 5.5V$ $T_A = -55°C$						130	
Input Capacitance	C_{IN}	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$		5			5		pF
Output Capacitance	C_{OUT}	$V_{CC} = 5.0$, $V_{OUT} = 2.0V$		8			8		

NOTES: 1. Typical values are measured at $V_{CC} = 5.0V$ and $T_A = +25°C$
2. Capacitance values are sampled, not 100% tested.

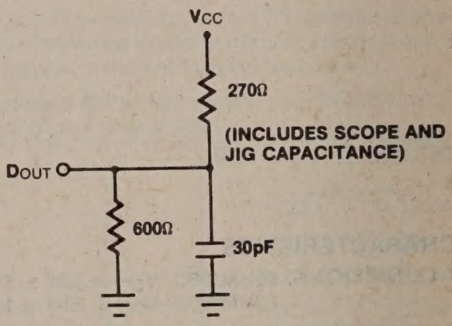
AC CHARACTERISTICS

DESCRIPTION	SYMBOL	JEDEC SYMBOL	82HM185C		82HM185M		UNITS
			TYP	MAX	TYP	MAX	
Address Access Time	t_{aa}	TAVQV	60	70	70	90	ns
Chip Enable Access Time	t_{ce}	TSVQV	30	40	30	50	
Output Disable Time	t_{cd}	TSXQZ	30	40	30	50	

NOTE: Superior speed selection is available

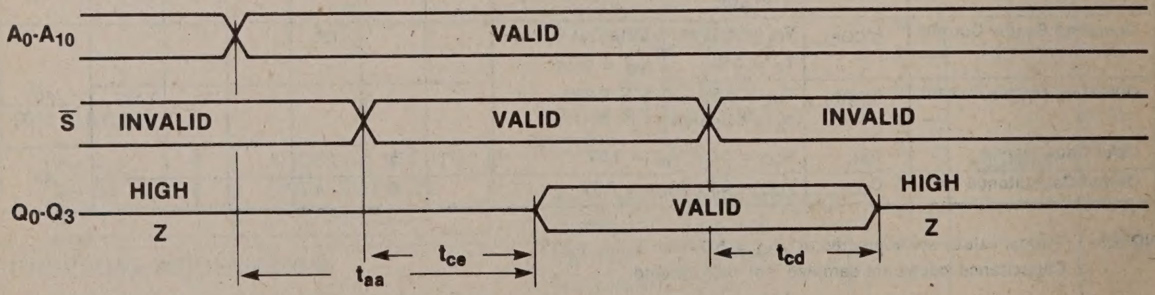
AC TEST CONDITIONS

82HM185C: V_{CC} = 5V ±5%, T_A = 0°C to +75% °C
82HM185M: V_{CC} = 5V ±10%, T_A = −55°C to +125°C
Input pulse levels - 0.0V and 3.0V
Input rise and fall times - 5ns (10% to 90%)
Timing reference level - 1.5V - Inputs and outputs


Vcc
270Ω
(INCLUDES SCOPE AND JIG CAPACITANCE)
DOUT
600Ω
30pF

OUTPUT LOAD CIRCUIT

READ CYCLE TIMING


A_0-A_{10}
VALID
$\overline{S}$
INVALID
VALID
INVALID
Q_0-Q_3
HIGH
Z
VALID
HIGH
Z
t_{ce}
t_{cd}
t_{aa}

INTERSIL

82HM191
16,384 Bit (2048 x 8) HMOS ROM

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

- **High speed - 80ns maximum access time**
- **Completely static - no clock required**
- **Single +5V supply**
- **Fully TTL compatible**
- **Three chip select inputs**
- **Three-state outputs**
- **883B processing available**
- **Mil temp operation (−55°C to +125°C) available**
- **Pinout and functionally compatible to industry standard Bipolar PROMs**

GENERAL DESCRIPTION

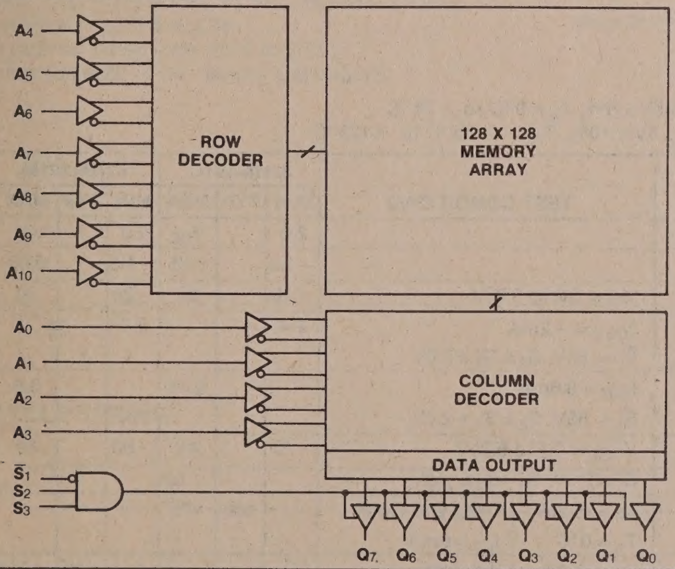
The 82HM191 is a high speed 16,384 bit read-only memory (ROM) organized 2048 words by 8 bits. The device is fabricated using Intersil's SELOX HMOS technology, a single-layer polysilicon, selective-oxidation arsenic diffusion process, to minimize memory cell area and optimize circuit performance.

The 82HM191 is an exact pinout and functional replacement for industry standard 2048 x 8 Bipolar PROMs.

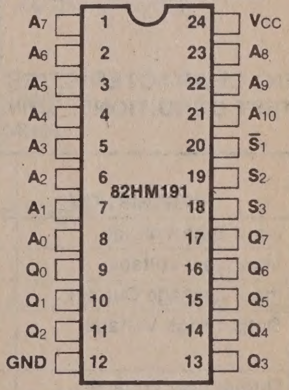
Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. Three chip select inputs allow for ease of memory expansion.

The standard 82HM191 operates over 5V ± 5% at 175mA with an access time of 80ns.

LOGICAL BLOCK DIAGRAM

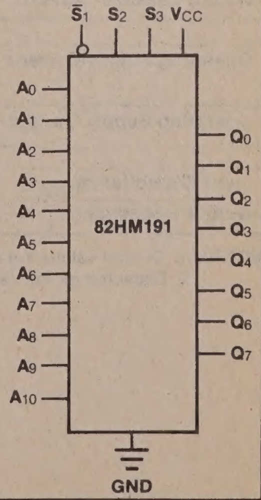

A4
A5
A6
A7
A8
A9
A10
ROW DECODER
128 X 128 MEMORY ARRAY
A0
A1
A2
A3
COLUMN DECODER
DATA OUTPUT
S̄1
S2
S3
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

PIN CONFIGURATION


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 VCC
23 A8
22 A9
21 A10
20 S̄1
19 S2
18 S3
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
82HM191

(outline dwgs JG, PG)

LOGIC SYMBOL


S̄1
S2
S3
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
82HM191
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
GND

PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
Q_0-Q_7	DATA OUTPUTS
$\overline{S}_1$, S_2, S_3	CHIP SELECTS

PROM REPLACEMENT GUIDE

SUPPLIER	PART NUMBER
AMD	AM27S191
FAIRCHILD	93511
HARRIS	HM76161
INTEL	3636
MMI	63S1681
NATIONAL	87S191
RAYTHEON	29681
SIGNETICS	82S191
TI	TBP28S166

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
82HM191CPG	24 Pin PLASTIC	0°C to +75°C
82HM191CJG	24 Pin CERDIP	0°C to +75°C
82HM191MJG/883B	24 Pin CERDIP	−55°C to +125°C

NOTE: Plastic package not yet available
- pending qualification

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Voltage On Any Pin Relative to GND	−0.5V to +7.0V
Commercial Operating Temperature Range	0°C to +75°C
Military Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: 82HM191C: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $+75°C$
82HM191M: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$

			82HM191C			82HM191M			
DESCRIPTION	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input High Voltage	V_{IH}		2.0		V_{CC}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}		−1.0		0.85	−1.0		0.80	
Input Leakage Current	I_{ILK}	$V_{IN} =$ 0V to 5.25V	−20		20	−20		20	μA
Output High Voltage	V_{OH}	$I_{OUT} = -2mA$ $\overline{S}_1 = .85V$, $S_2 = S_3 = 2.0V$	2.4			2.4			V
Output Low Voltage	V_{OL}	$I_{OUT} = 9.6mA$ $\overline{S}_1 = .85V$, $S_2 = S_3 = 2.0V$			0.45			0.5	
Output Leakage Current	I_{OLK}	$V_{OUT} =$ 0V to 5.25V $\overline{S}_1 = 2.0V$, $S_2 = S_3 = .85V$	−40		40	−60		60	μA
Operating Supply Current	I_{CCOP_1}	$V_{IN} = 5.25V$ $T_A = 0°C$ Data Out Open $I_{I/O} = 0mA$ $\overline{S}_1 = .85V$ $S_2 = S_3 = 2.0V$		100	175				mA
Operating Supply Current	I_{CCOP_2}	$V_{IN} = 5.5V$ $T_A = -55°C$					100	185	
Input Capacitance	C_{IN}	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$		5			5		pF
Output Capacitance	C_{OUT}	$V_{CC} = 5.0V$, $V_{OUT} = 2.0V$		8			8		

NOTES: 1. Typical values are measured at $V_{CC} = 5.0V$ and $T_A = +25°C$
2. Capacitance values are sampled, not 100% tested.

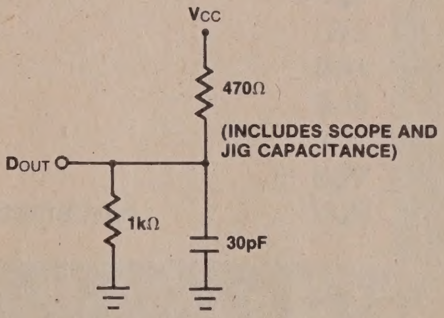
AC CHARACTERISTICS

DESCRIPTION	SYMBOL	JEDEC SYMBOL	82HM191C		82HM191M		UNITS
			TYP	MAX	TYP	MAX	
Address Access Time	t_{aa}	TAVQV	50	80	50	100	ns
Chip Enable Access Time	t_{ce}	TSVQV	20	40	20	50	
Output Disable Time	t_{cd}	TSXQZ	20	40	20	50	

NOTE: Superior speed selection is available

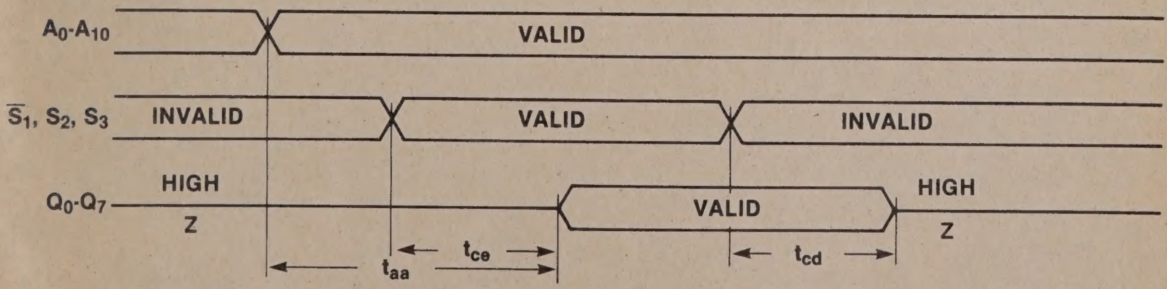
AC TEST CONDITIONS

82HM191C: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $+75°C$
82HM191M: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$
Input pulse levels - 0.0V and 3.0V
Input rise and fall times - 5ns (10% to 90%)
Timing reference level - 1.5V - Inputs and outputs


VCC
470Ω
(INCLUDES SCOPE AND JIG CAPACITANCE)
DOUT
1kΩ
30pF

OUTPUT LOAD CIRCUIT

READ CYCLE TIMING


A0-A10
VALID
S̄1, S2, S3
INVALID
VALID
INVALID
Q0-Q7
HIGH
Z
VALID
HIGH
Z
tce
taa
tcd

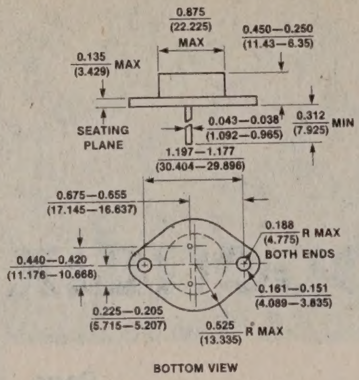
NOTES:

Appendix

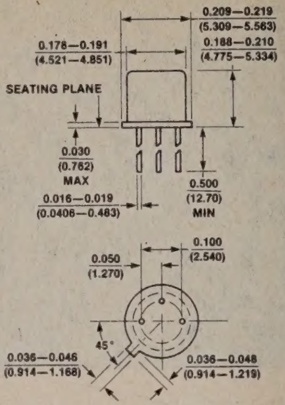
Page
Package Dimensions B-2
High Reliability Processing B-11
Application Note Summary B-19
Chip Ordering Information B-21
Intersil Part Numbering System B-27
Sales Offices, Distributors, and Representatives B-29

PACKAGE OUTLINES

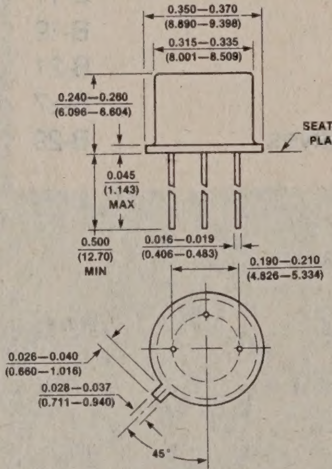
All dimensions given in inches and (millimeters).


0.875
(22.225)
MAX
0.450—0.250
(11.43—6.35)
0.135
(3.429) MAX
SEATING
PLANE
0.043—0.038
(1.092—0.965)
0.312
(7.925) MIN
1.197—1.177
(30.404—29.896)
0.675—0.655
(17.145—16.637)
0.188
(4.775) R MAX
BOTH ENDS
0.440—0.420
(11.176—10.668)
0.161—0.151
(4.089—3.835)
0.225—0.205
(5.715—5.207)
0.525
(13.335) R MAX
BOTTOM VIEW

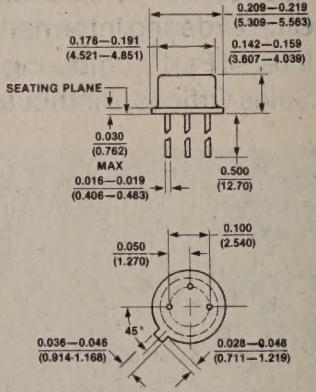
TO-3


0.209—0.219
(5.309—5.563)
0.178—0.191
(4.521—4.851)
0.188—0.210
(4.775—5.334)
SEATING PLANE
0.030
(0.762)
MAX
0.016—0.019
(0.0406—0.483)
0.500
(12.70)
MIN
0.100
(2.540)
0.050
(1.270)
45°
0.036—0.046
(0.914—1.168)
0.036—0.048
(0.914—1.219)

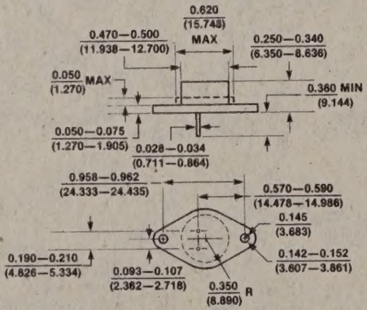
TO-18


0.350—0.370
(8.890—9.398)
0.315—0.335
(8.001—8.509)
0.240—0.260
(6.096—6.604)
SEATING
PLANE
0.045
(1.143)
MAX
0.500
(12.70)
MIN
0.016—0.019
(0.406—0.483)
0.190—0.210
(4.826—5.334)
0.026—0.040
(0.660—1.016)
0.028—0.037
(0.711—0.940)
45°

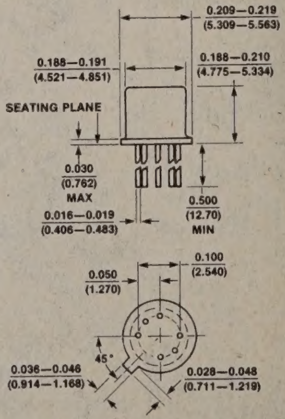
TO-39


0.209—0.219
(5.309—5.563)
0.178—0.191
(4.521—4.851)
0.142—0.159
(3.607—4.039)
SEATING PLANE
0.030
(0.762)
MAX
0.016—0.019
(0.406—0.483)
0.500
(12.70)
0.100
(2.540)
0.050
(1.270)
45°
0.036—0.046
(0.914-1.168)
0.028—0.048
(0.711—1.219)

TO-52


0.620
(15.748)
MAX
0.470—0.500
(11.938—12.700)
0.250—0.340
(6.350—8.636)
0.050
(1.270) MAX
0.360 MIN
(9.144)
0.050—0.075
(1.270—1.905)
0.028—0.034
(0.711—0.864)
0.958—0.962
(24.333—24.435)
0.570—0.590
(14.478—14.986)
0.145
(3.683)
0.190—0.210
(4.826—5.334)
0.093—0.107
(2.362—2.718)
0.142—0.152
(3.607—3.861)
0.350
(8.890) R

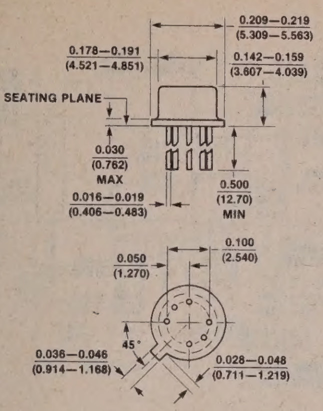
TO-66


0.209—0.219
(5.309—5.563)
0.188—0.191
(4.521—4.851)
0.188—0.210
(4.775—5.334)
SEATING PLANE
0.030
(0.762)
MAX
0.016—0.019
(0.406—0.483)
0.500
(12.70)
MIN
0.100
(2.540)
0.050
(1.270)
45°
0.036—0.046
(0.914—1.168)
0.028—0.048
(0.711—1.219)

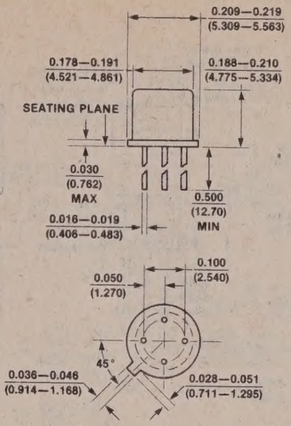
TO-71

PACKAGE OUTLINES

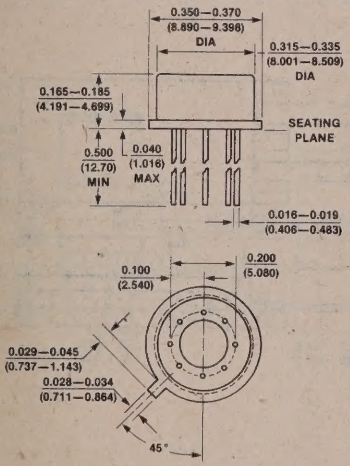
All dimensions given in inches and (millimeters).


0.209—0.219
(5.309—5.563)
0.178—0.191
(4.521—4.851)
0.142—0.159
(3.607—4.039)
SEATING PLANE
0.030
(0.762)
MAX
0.500
(12.70)
MIN
0.016—0.019
(0.406—0.483)
0.100
(2.540)
0.050
(1.270)
45°
0.036—0.046
(0.914—1.168)
0.028—0.048
(0.711—1.219)

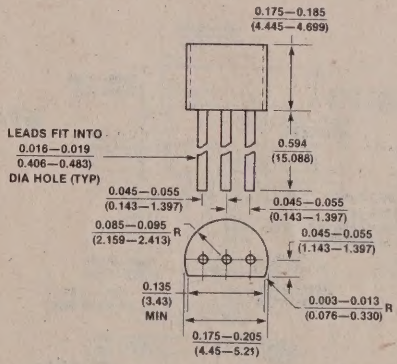
TO-71 LOW PROFILE


0.209—0.219
(5.309—5.563)
0.178—0.191
(4.521—4.861)
0.188—0.210
(4.775—5.334)
SEATING PLANE
0.030
(0.762)
MAX
0.500
(12.70)
MIN
0.016—0.019
(0.406—0.483)
0.100
(2.540)
0.050
(1.270)
45°
0.036—0.046
(0.914—1.168)
0.028—0.051
(0.711—1.295)

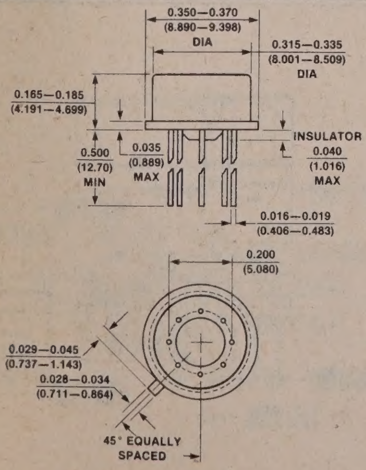
TO-72


0.350—0.370
(8.890—9.398)
DIA
0.315—0.335
(8.001—8.509)
DIA
0.165—0.185
(4.191—4.699)
SEATING PLANE
0.500
(12.70)
MIN
0.040
(1.016)
MAX
0.016—0.019
(0.406—0.483)
0.200
(5.080)
0.100
(2.540)
0.029—0.045
(0.737—1.143)
0.028—0.034
(0.711—0.864)
45°

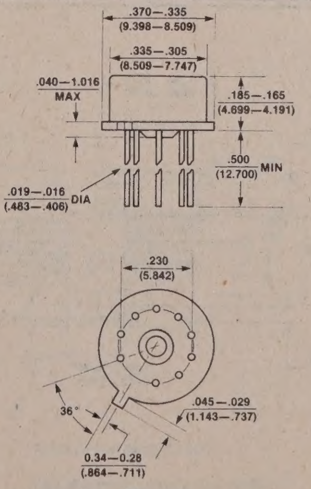
TO-78


0.175—0.185
(4.445—4.699)
LEADS FIT INTO
0.016—0.019
0.406—0.483)
DIA HOLE (TYP)
0.594
(15.088)
0.045—0.055
(0.143—1.397)
0.045—0.055
(0.143—1.397)
0.085—0.095
(2.159—2.413)
R
0.045—0.055
(1.143—1.397)
0.135
(3.43)
MIN
0.003—0.013
(0.076—0.330)
R
0.175—0.205
(4.45—5.21)

TO-92

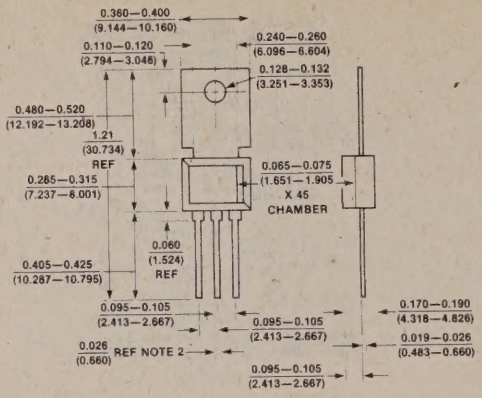

0.350—0.370
(8.890—9.398)
DIA
0.315—0.335
(8.001—8.509)
DIA
0.165—0.185
(4.191—4.699)
INSULATOR
0.500
(12.70)
MIN
0.035
(0.889)
MAX
0.040
(1.016)
MAX
0.016—0.019
(0.406—0.483)
0.200
(5.080)
0.029—0.045
(0.737—1.143)
0.028—0.034
(0.711—0.864)
45° EQUALLY
SPACED

TO-99

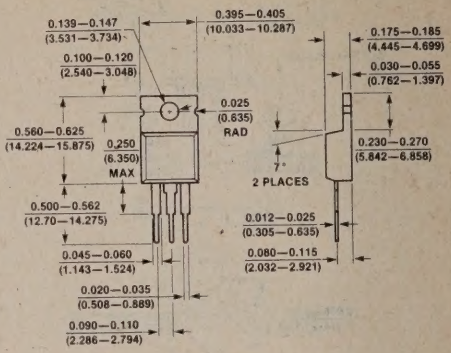

.370—.335
(9.398—8.509)
.335—.305
(8.509—7.747)
.040—1.016
MAX
.185—.165
(4.699—4.191)
.500
(12.700)
MIN
.019—.016
(.483—.406)
DIA
.230
(5.842)
36°
.045—.029
(1.143—.737)
0.34—0.28
(.864—.711)

TO-100

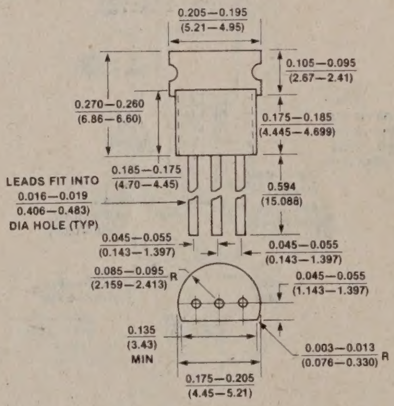
PACKAGE OUTLINES All dimensions given in inches and (millimeters).


0.360—0.400
(9.144—10.160)
0.110—0.120
(2.794—3.048)
0.240—0.260
(6.096—6.604)
0.128—0.132
(3.251—3.353)
0.480—0.520
(12.192—13.208)
1.21
(30.734)
REF
0.285—0.315
(7.237—8.001)
0.065—0.075
(1.651—1.905
X 45
CHAMBER
0.060
(1.524)
REF
0.405—0.425
(10.287—10.795)
0.095—0.105
(2.413—2.667)
0.095—0.105
(2.413—2.667)
0.170—0.190
(4.318—4.826)
0.026
(0.660)
REF NOTE 2
0.019—0.026
(0.483—0.660)
0.095—0.105
(2.413—2.667)

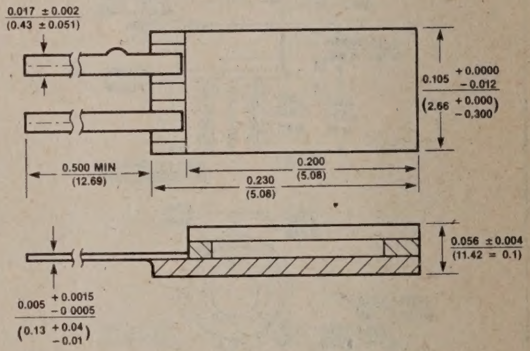
TO-202


0.139—0.147
(3.531—3.734)
0.395—0.405
(10.033—10.287)
0.175—0.185
(4.445—4.699)
0.100—0.120
(2.540—3.048)
0.030—0.055
(0.762—1.397)
0.025
(0.635)
RAD
0.560—0.625
(14.224—15.875)
0.250
(6.350)
MAX
0.230—0.270
(5.842—6.858)
7°
2 PLACES
0.500—0.562
(12.70—14.275)
0.012—0.025
(0.305—0.635)
0.045—0.060
(1.143—1.524)
0.080—0.115
(2.032—2.921)
0.020—0.035
(0.508—0.889)
0.090—0.110
(2.286—2.794)

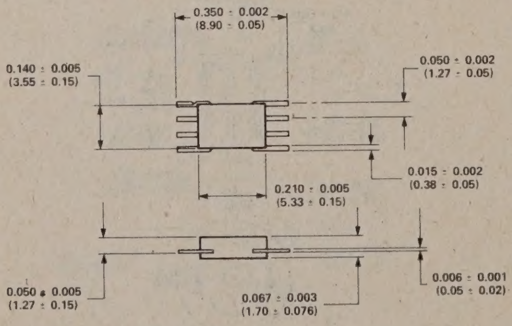
TO-220


0.205—0.195
(5.21—4.95)
0.105—0.095
(2.67—2.41)
0.270—0.260
(6.86—6.60)
0.175—0.185
(4.445—4.699)
LEADS FIT INTO
0.016—0.019
0.406—0.483)
DIA HOLE (TYP)
0.185—0.175
(4.70—4.45)
0.594
(15.088)
0.045—0.055
(0.143—1.397)
0.045—0.055
(0.143—1.397)
0.085—0.095
(2.159—2.413)
R
0.045—0.055
(1.143—1.397)
0.135
(3.43)
MIN
0.003—0.013
(0.076—0.330)
R
0.175—0.205
(4.45—5.21)

TO-237

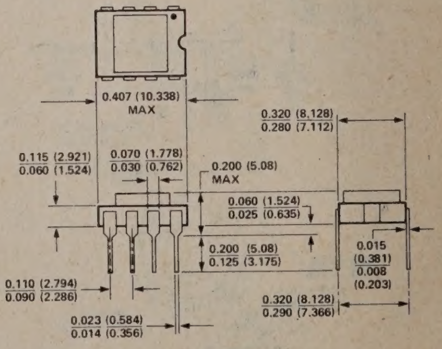

0.017 ±0.002
(0.43 ±0.051)
0.105 +0.0000 −0.012
(2.66 +0.000 −0.300)
0.500 MIN
(12.69)
0.200
(5.08)
0.230
(5.08)
0.056 ±0.004
(11.42 = 0.1)
0.005 +0.0015 −0.0005
(0.13 +0.04 −0.01)

2 LEAD CERAMIC (DH)


0.350 ± 0.002
(8.90 ± 0.05)
0.050 ± 0.002
(1.27 ± 0.05)
0.140 ± 0.005
(3.55 ± 0.15)
0.015 ± 0.002
(0.38 ± 0.05)
0.210 ± 0.005
(5.33 ± 0.15)
0.006 ± 0.001
(0.05 ± 0.02)
0.050 ± 0.005
(1.27 ± 0.15)
0.067 ± 0.003
(1.70 ± 0.076)

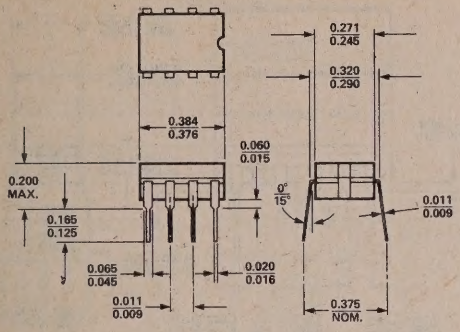
THIS DRAWING NOT TO SCALE.

8 LEAD FLATPACK (BA)

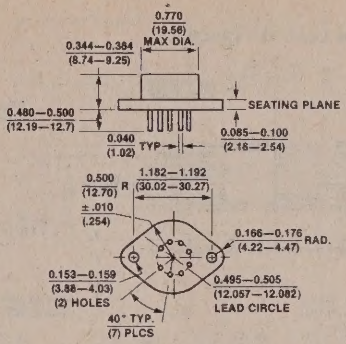

0.407 (10.338)
MAX
0.320 (8.128)
0.280 (7.112)
0.115 (2.921)
0.060 (1.524)
0.070 (1.778)
0.030 (0.762)
0.200 (5.08)
MAX
0.060 (1.524)
0.025 (0.635)
0.200 (5.08)
0.125 (3.175)
0.015
(0.381)
0.008
(0.203)
0.110 (2.794)
0.090 (2.286)
0.320 (8.128)
0.290 (7.366)
0.023 (0.584)
0.014 (0.356)

8 LEAD CERAMIC (DA)

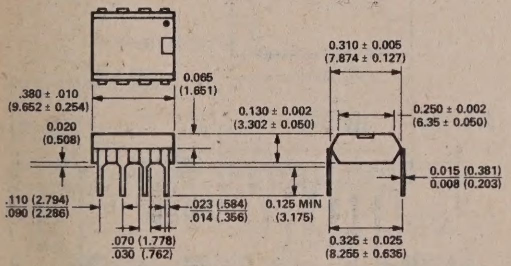
PACKAGE OUTLINES All dimensions given in inches and (millimeters).


0.271
0.245
0.320
0.290
0.384
0.376
0.060
0.015
0.200
MAX.
0°
15°
0.011
0.009
0.165
0.125
0.065
0.045
0.020
0.016
0.011
0.009
0.375
NOM.

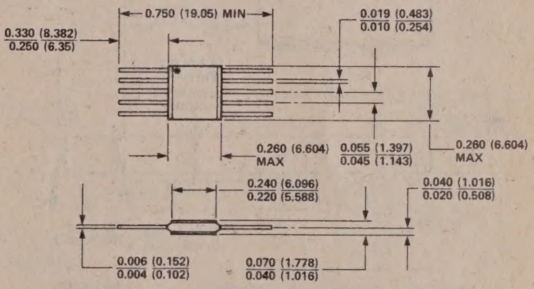
8 LEAD CERDIP (JA)


0.770
(19.56)
MAX DIA.
0.344—0.364
(8.74—9.25)
SEATING PLANE
0.480—0.500
(12.19—12.7)
0.040
(1.02)
TYP
0.085—0.100
(2.16—2.54)
0.500
(12.70)
R
± .010
(.254)
1.182—1.192
(30.02—30.27)
0.166—0.176
(4.22—4.47)
RAD.
0.153—0.159
(3.88—4.03)
(2) HOLES
0.495—0.505
(12.057—12.082)
LEAD CIRCLE
40° TYP.
(7) PLCS

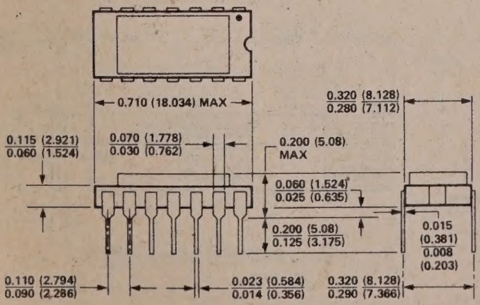
8 LEAD TO-3 CAN (KA)


0.310 ± 0.005
(7.874 ± 0.127)
.380 ± .010
(9.652 ± 0.254)
0.065
(1.651)
0.130 ± 0.002
(3.302 ± 0.050)
0.250 ± 0.002
(6.35 ± 0.050)
0.020
(0.508)
0.015 (0.381)
0.008 (0.203)
.110 (2.794)
.090 (2.286)
.023 (.584)
.014 (.356)
0.125 MIN
(3.175)
.070 (1.778)
.030 (.762)
0.325 ± 0.025
(8.255 ± 0.635)

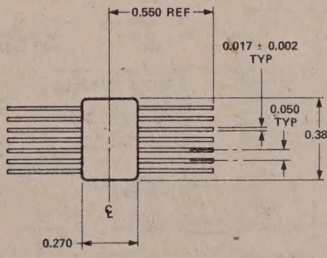
8 LEAD PLASTIC (PA)


0.750 (19.05) MIN
0.019 (0.483)
0.010 (0.254)
0.330 (8.382)
0.250 (6.35)
0.260 (6.604)
MAX
0.055 (1.397)
0.045 (1.143)
0.260 (6.604)
MAX
0.240 (6.096)
0.220 (5.588)
0.040 (1.016)
0.020 (0.508)
0.006 (0.152)
0.004 (0.102)
0.070 (1.778)
0.040 (1.016)

10 LEAD FLATPACK (FB)


0.710 (18.034) MAX
0.320 (8.128)
0.280 (7.112)
0.115 (2.921)
0.060 (1.524)
0.070 (1.778)
0.030 (0.762)
0.200 (5.08)
MAX
0.060 (1.524)
0.025 (0.635)
0.200 (5.08)
0.125 (3.175)
0.015
(0.381)
0.008
(0.203)
0.110 (2.794)
0.090 (2.286)
0.023 (0.584)
0.014 (0.356)
0.320 (8.128)
0.290 (7.366)

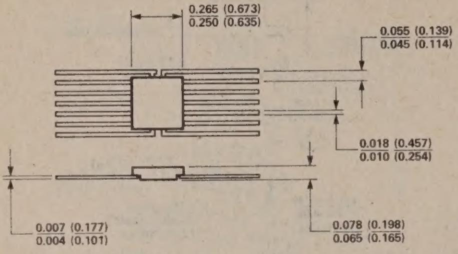
14 LEAD CERAMIC (DD)


0.550 REF
0.017 ± 0.002
TYP
0.050
TYP
0.385
0.270

14 LEAD FLATPACK (FD-1)

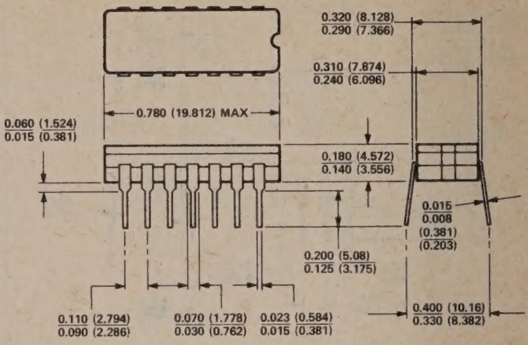
PACKAGE OUTLINES All dimensions given in inches and (millimeters).

14 LEAD FLATPACK (FD)



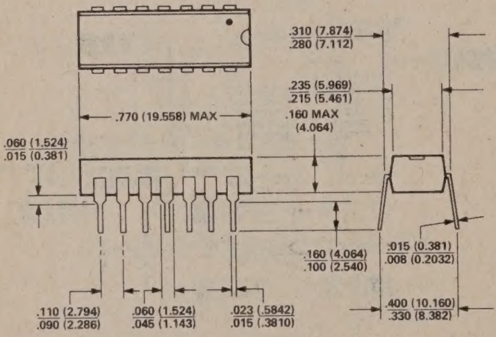
0.265 (0.673)
0.250 (0.635)
0.055 (0.139)
0.045 (0.114)
0.018 (0.457)
0.010 (0.254)
0.007 (0.177)
0.004 (0.101)
0.078 (0.198)
0.065 (0.165)

14 LEAD FLATPACK (FD-2)



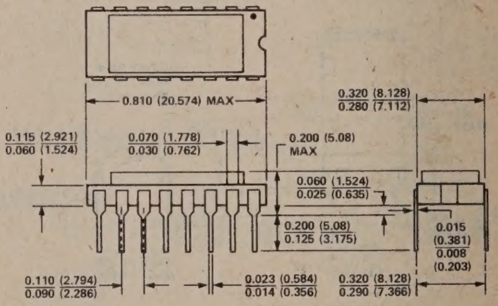
0.320 (8.128)
0.290 (7.366)
0.310 (7.874)
0.240 (6.096)
0.780 (19.812) MAX
0.060 (1.524)
0.015 (0.381)
0.180 (4.572)
0.140 (3.556)
0.015
0.008
(0.381)
(0.203)
0.200 (5.08)
0.125 (3.175)
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.023 (0.584)
0.015 (0.381)
0.400 (10.16)
0.330 (8.382)

14 LEAD CERDIP (JD)



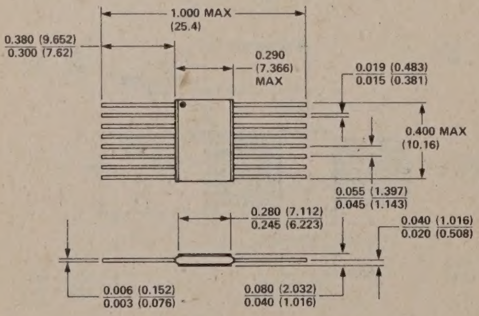
.310 (7.874)
.280 (7.112)
.235 (5.969)
.215 (5.461)
.160 MAX
(4.064)
.770 (19.558) MAX
.060 (1.524)
.015 (0.381)
.160 (4.064)
.100 (2.540)
.015 (0.381)
.008 (0.2032)
.110 (2.794)
.090 (2.286)
.060 (1.524)
.045 (1.143)
.023 (.5842)
.015 (.3810)
.400 (10.160)
.330 (8.382)

14 LEAD PLASTIC (PD)



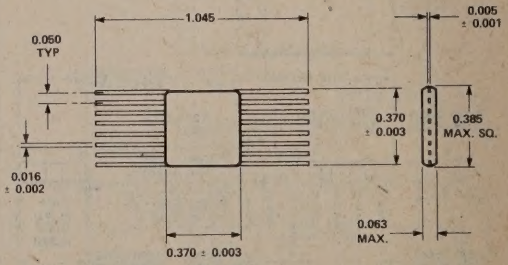
0.810 (20.574) MAX
0.320 (8.128)
0.280 (7.112)
0.115 (2.921)
0.060 (1.524)
0.070 (1.778)
0.030 (0.762)
0.200 (5.08)
MAX
0.060 (1.524)
0.025 (0.635)
0.200 (5.08)
0.125 (3.175)
0.015
(0.381)
0.008
(0.203)
0.110 (2.794)
0.090 (2.286)
0.023 (0.584)
0.014 (0.356)
0.320 (8.128)
0.290 (7.366)

16 LEAD CERAMIC (DE)



1.000 MAX
(25.4)
0.380 (9.652)
0.300 (7.62)
0.290
(7.366)
MAX
0.019 (0.483)
0.015 (0.381)
0.400 MAX
(10.16)
0.055 (1.397)
0.045 (1.143)
0.280 (7.112)
0.245 (6.223)
0.040 (1.016)
0.020 (0.508)
0.006 (0.152)
0.003 (0.076)
0.080 (2.032)
0.040 (1.016)

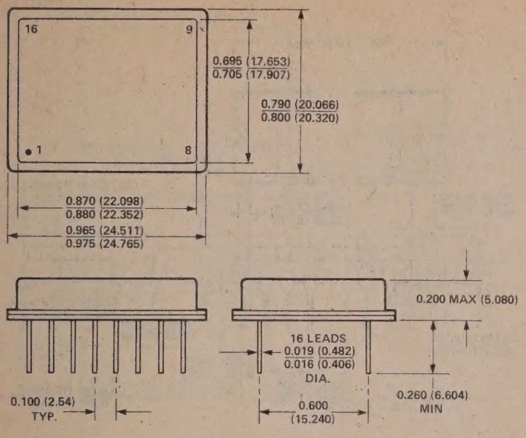
16 LEAD FLATPACK (FE-1)



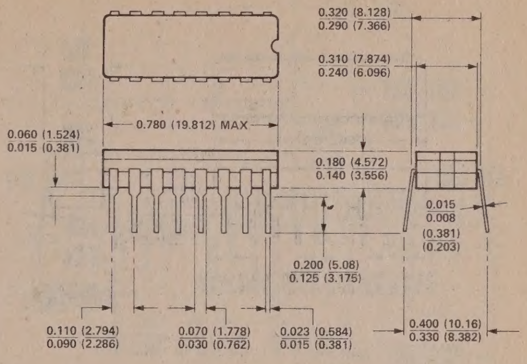
1.045
0.005
± 0.001
0.050
TYP
0.370
± 0.003
0.385
MAX. SQ.
0.016
± 0.002
0.063
MAX.
0.370 ± 0.003

16 LEAD FLATPACK (FE-2)

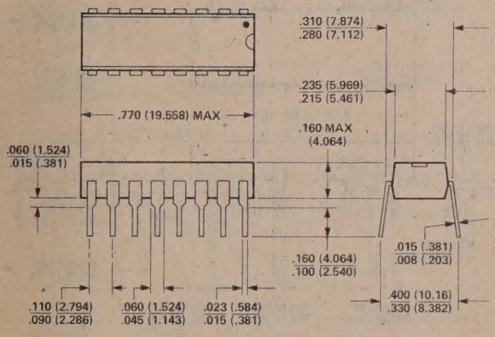
PACKAGE OUTLINES All dimensions given in inches and (millimeters).


16
9
1
8
0.695 (17.653)
0.705 (17.907)
0.790 (20.066)
0.800 (20.320)
0.870 (22.098)
0.880 (22.352)
0.965 (24.511)
0.975 (24.765)
0.200 MAX (5.080)
16 LEADS
0.019 (0.482)
0.016 (0.406)
DIA.
0.100 (2.54)
TYP.
0.600
(15.240)
0.260 (6.604)
MIN

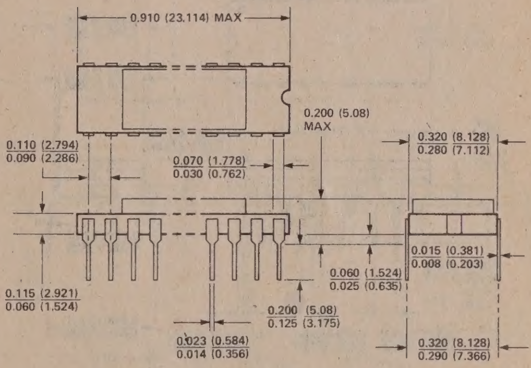
16 LEAD (.6 x .7) CERAMIC (IE)


0.320 (8.128)
0.290 (7.366)
0.310 (7.874)
0.240 (6.096)
0.780 (19.812) MAX
0.060 (1.524)
0.015 (0.381)
0.180 (4.572)
0.140 (3.556)
0.015
0.008
(0.381)
(0.203)
0.200 (5.08)
0.125 (3.175)
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.023 (0.584)
0.015 (0.381)
0.400 (10.16)
0.330 (8.382)

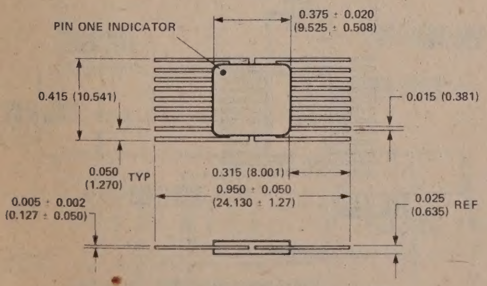
16 LEAD CERDIP (JE)


.310 (7.874)
.280 (7.112)
.235 (5.969)
.215 (5.461)
.770 (19.558) MAX
.160 MAX
(4.064)
.060 (1.524)
.015 (.381)
.160 (4.064)
.100 (2.540)
.015 (.381)
.008 (.203)
.400 (10.16)
.330 (8.382)
.110 (2.794)
.090 (2.286)
.060 (1.524)
.045 (1.143)
.023 (.584)
.015 (.381)

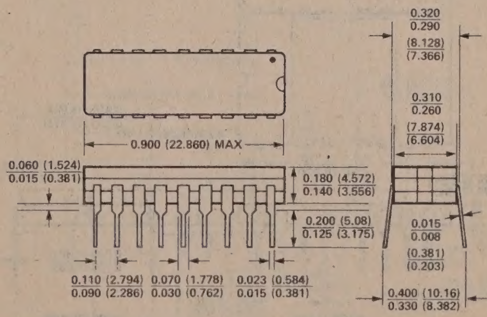
16 LEAD PLASTIC (PE)


0.910 (23.114) MAX
0.200 (5.08)
MAX
0.320 (8.128)
0.280 (7.112)
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.015 (0.381)
0.008 (0.203)
0.060 (1.524)
0.025 (0.635)
0.115 (2.921)
0.060 (1.524)
0.200 (5.08)
0.125 (3.175)
0.023 (0.584)
0.014 (0.356)
0.320 (8.128)
0.290 (7.366)

18 LEAD CERAMIC (DN)


PIN ONE INDICATOR
0.375 ± 0.020
(9.525 ± 0.508)
0.415 (10.541)
0.015 (0.381)
0.050
(1.270)
TYP
0.315 (8.001)
0.960 ± 0.050
(24.130 ± 1.27)
0.005 ± 0.002
(0.127 ± 0.050)
0.025
(0.635)
REF

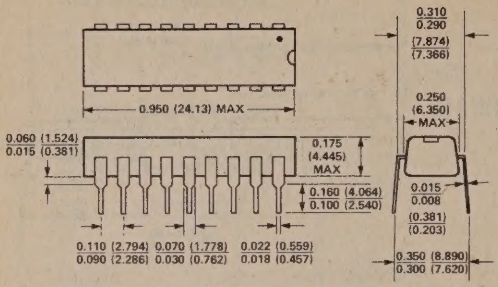
18 LEAD FLATPACK (FN)


0.320
0.290
(8.128)
(7.366)
0.310
0.260
(7.874)
(6.604)
0.900 (22.860) MAX
0.060 (1.524)
0.015 (0.381)
0.180 (4.572)
0.140 (3.556)
0.200 (5.08)
0.125 (3.175)
0.015
0.008
(0.381)
(0.203)
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.023 (0.584)
0.015 (0.381)
0.400 (10.16)
0.330 (8.382)

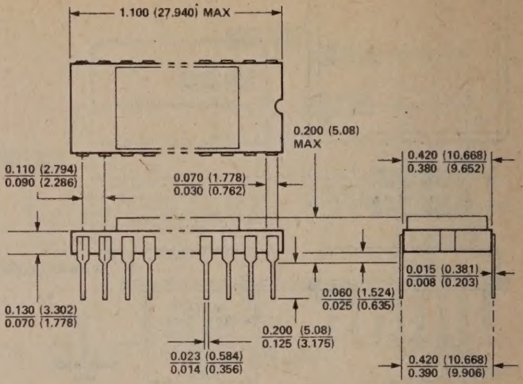
18 LEAD CERDIP (JN)

PACKAGE OUTLINES

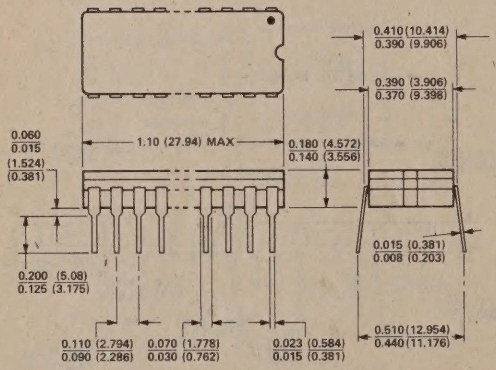
All dimensions given in inches and (millimeters).


0.950 (24.13) MAX
0.060 (1.524)
0.015 (0.381)
0.175
(4.445)
MAX
0.160 (4.064)
0.100 (2.540)
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.022 (0.559)
0.018 (0.457)
0.310
0.290
(7.874)
(7.366)
0.250
(6.350)
MAX
0.015
0.008
(0.381)
(0.203)
0.350 (8.890)
0.300 (7.620)

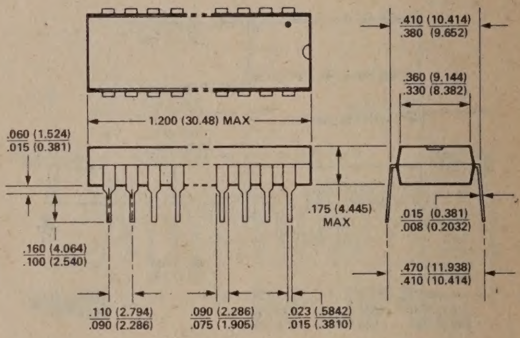
18 LEAD PLASTIC (PN)


1.100 (27.940) MAX
0.200 (5.08)
MAX
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.420 (10.668)
0.380 (9.652)
0.015 (0.381)
0.008 (0.203)
0.060 (1.524)
0.025 (0.635)
0.130 (3.302)
0.070 (1.778)
0.200 (5.08)
0.125 (3.175)
0.023 (0.584)
0.014 (0.356)
0.420 (10.668)
0.390 (9.906)

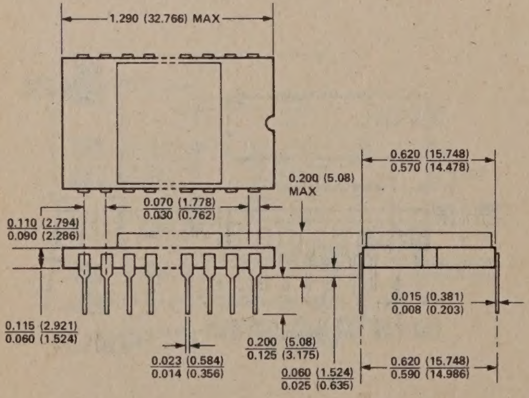
22 LEAD CERAMIC (DF)


0.410 (10.414)
0.390 (9.906)
0.390 (3.906)
0.370 (9.398)
0.060
0.015
(1.524)
(0.381)
1.10 (27.94) MAX
0.180 (4.572)
0.140 (3.556)
0.015 (0.381)
0.008 (0.203)
0.200 (5.08)
0.125 (3.175)
0.510 (12.954)
0.440 (11.176)
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.023 (0.584)
0.015 (0.381)

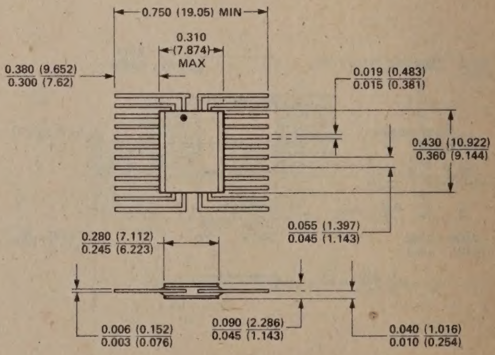
22 LEAD CERDIP (JF)


.410 (10.414)
.380 (9.652)
.360 (9.144)
.330 (8.382)
1.200 (30.48) MAX
.060 (1.524)
.015 (0.381)
.175 (4.445)
MAX
.015 (0.381)
.008 (0.2032)
.160 (4.064)
.100 (2.540)
.470 (11.938)
.410 (10.414)
.110 (2.794)
.090 (2.286)
.090 (2.286)
.075 (1.905)
.023 (.5842)
.015 (.3810)

22 LEAD PLASTIC (PF)

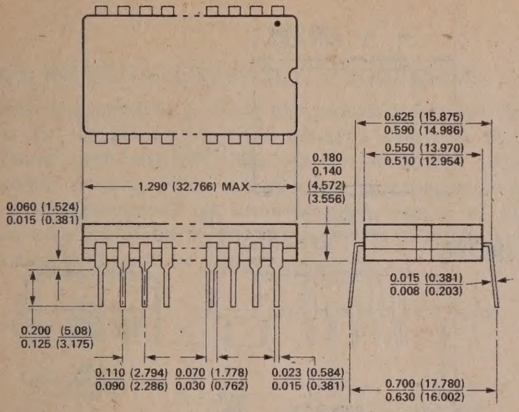

1.290 (32.766) MAX
0.620 (15.748)
0.570 (14.478)
0.200 (5.08)
MAX
0.070 (1.778)
0.030 (0.762)
0.110 (2.794)
0.090 (2.286)
0.015 (0.381)
0.008 (0.203)
0.115 (2.921)
0.060 (1.524)
0.200 (5.08)
0.125 (3.175)
0.023 (0.584)
0.014 (0.356)
0.060 (1.524)
0.025 (0.635)
0.620 (15.748)
0.590 (14.986)

24 LEAD CERAMIC (DG)

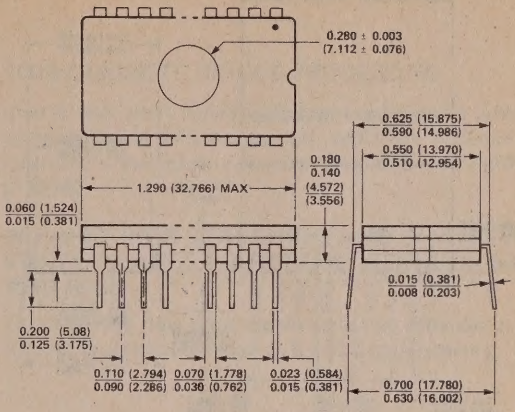

0.750 (19.05) MIN
0.310
(7.874)
MAX
0.380 (9.652)
0.300 (7.62)
0.019 (0.483)
0.015 (0.381)
0.430 (10.922)
0.360 (9.144)
0.055 (1.397)
0.045 (1.143)
0.280 (7.112)
0.245 (6.223)
0.006 (0.152)
0.003 (0.076)
0.090 (2.286)
0.045 (1.143)
0.040 (1.016)
0.010 (0.254)

24 LEAD FLATPACK (FG)

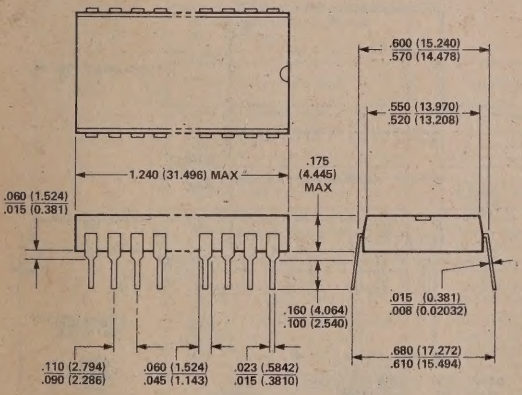
PACKAGE OUTLINES All dimensions given in inches and (millimeters).


0.625 (15.875)
0.590 (14.986)
0.550 (13.970)
0.510 (12.954)
0.180
0.140
(4.572)
(3.556)
1.290 (32.766) MAX
0.060 (1.524)
0.015 (0.381)
0.015 (0.381)
0.008 (0.203)
0.200 (5.08)
0.125 (3.175)
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.023 (0.584)
0.015 (0.381)
0.700 (17.780)
0.630 (16.002)

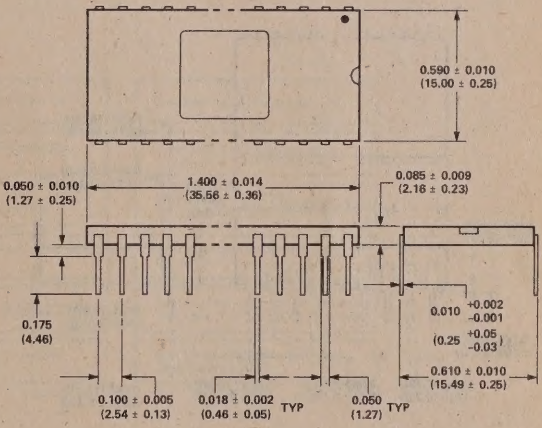
24 LEAD CERDIP (JG)


0.280 ± 0.003
(7.112 ± 0.076)
0.625 (15.875)
0.590 (14.986)
0.550 (13.970)
0.510 (12.954)
0.180
0.140
(4.572)
(3.556)
1.290 (32.766) MAX
0.060 (1.524)
0.015 (0.381)
0.015 (0.381)
0.008 (0.203)
0.200 (5.08)
0.125 (3.175)
0.110 (2.794)
0.090 (2.286)
0.070 (1.778)
0.030 (0.762)
0.023 (0.584)
0.015 (0.381)
0.700 (17.780)
0.630 (16.002)

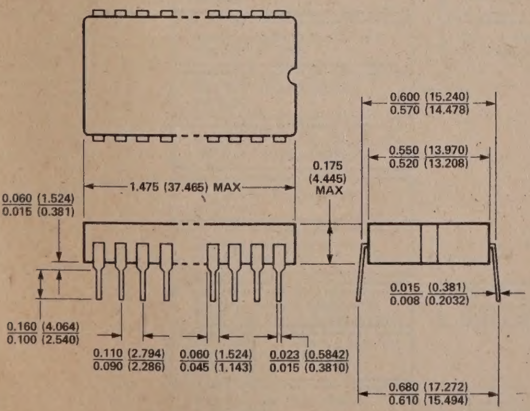
24 LEAD CERDIP WITH WINDOW (JG/W)


.600 (15.240)
.570 (14.478)
.550 (13.970)
.520 (13.208)
1.240 (31.496) MAX
.175
(4.445)
MAX
.060 (1.524)
.015 (0.381)
.160 (4.064)
.100 (2.540)
.015 (0.381)
.008 (0.02032)
.680 (17.272)
.610 (15.494)
.110 (2.794)
.090 (2.286)
.060 (1.524)
.045 (1.143)
.023 (.5842)
.015 (.3810)

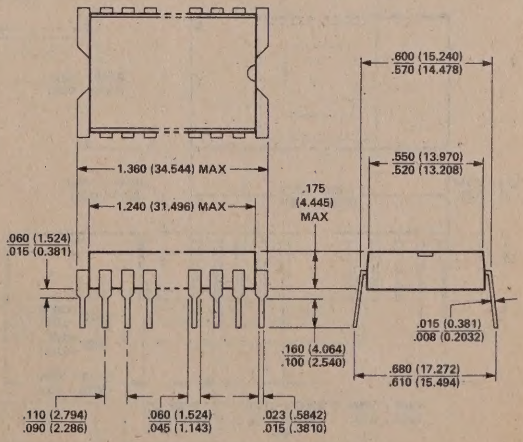
24 LEAD PLASTIC (PG)


0.590 ± 0.010
(15.00 ± 0.25)
0.050 ± 0.010
(1.27 ± 0.25)
1.400 ± 0.014
(35.56 ± 0.36)
0.085 ± 0.009
(2.16 ± 0.23)
0.010 +0.002 -0.001
(0.25 +0.05 -0.03)
0.175
(4.46)
0.610 ± 0.010
(15.49 ± 0.25)
0.100 ± 0.005
(2.54 ± 0.13)
0.018 ± 0.002
(0.46 ± 0.05)
TYP
0.050
(1.27)
TYP

28 LEAD CERAMIC (DI)


0.600 (15.240)
0.570 (14.478)
0.550 (13.970)
0.520 (13.208)
0.175
(4.445)
MAX
1.475 (37.465) MAX
0.060 (1.524)
0.015 (0.381)
0.015 (0.381)
0.008 (0.2032)
0.160 (4.064)
0.100 (2.540)
0.110 (2.794)
0.090 (2.286)
0.060 (1.524)
0.045 (1.143)
0.023 (0.5842)
0.015 (0.3810)
0.680 (17.272)
0.610 (15.494)

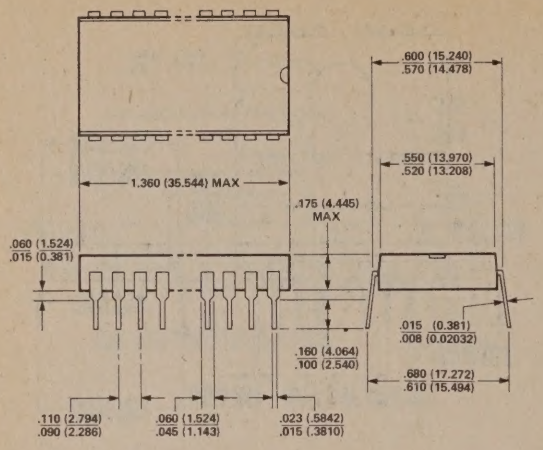
28 LEAD CERDIP (JI)


.600 (15.240)
.570 (14.478)
.550 (13.970)
.520 (13.208)
1.360 (34.544) MAX
.175
(4.445)
MAX
1.240 (31.496) MAX
.060 (1.524)
.015 (0.381)
.015 (0.381)
.008 (0.2032)
.160 (4.064)
.100 (2.540)
.680 (17.272)
.610 (15.494)
.110 (2.794)
.090 (2.286)
.060 (1.524)
.045 (1.143)
.023 (.5842)
.015 (.3810)

28 LEAD PLASTIC (PI-1)

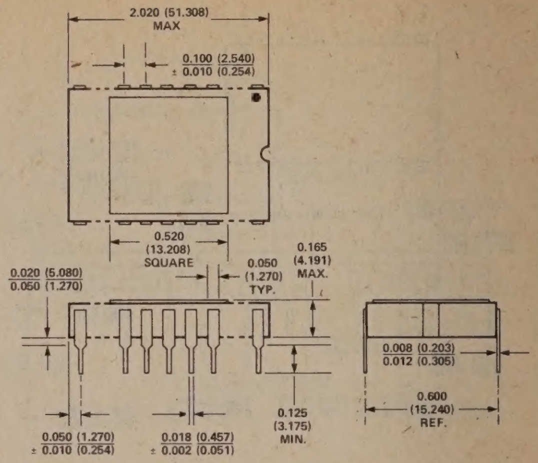
PACKAGE OUTLINES

All dimensions given in inches and (millimeters).



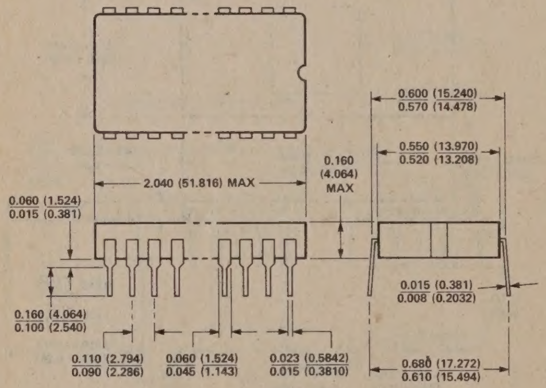
.600 (15.240)
.570 (14.478)
.550 (13.970)
.520 (13.208)
1.360 (35.544) MAX
.175 (4.445)
MAX
.060 (1.524)
.015 (0.381)
.015 (0.381)
.008 (0.02032)
.160 (4.064)
.100 (2.540)
.680 (17.272)
.610 (15.494)
.110 (2.794)
.090 (2.286)
.060 (1.524)
.045 (1.143)
.023 (.5842)
.015 (.3810)

28 LEAD PLASTIC (PI-2)



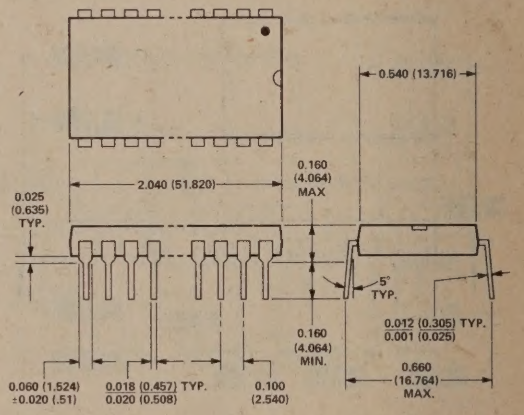
2.020 (51.308)
MAX
0.100 (2.540)
± 0.010 (0.254)
0.520
(13.208)
SQUARE
0.165
(4.191)
MAX.
0.050
(1.270)
TYP.
0.020 (5.080)
0.050 (1.270)
0.008 (0.203)
0.012 (0.305)
0.600
(15.240)
REF.
0.125
(3.175)
MIN.
0.050 (1.270)
± 0.010 (0.254)
0.018 (0.457)
± 0.002 (0.051)

40 LEAD CERAMIC (DL)



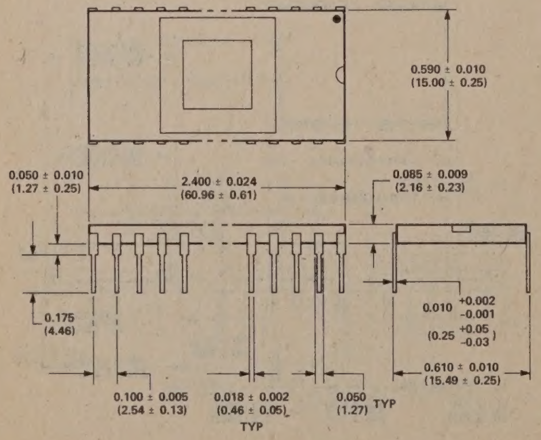
0.600 (15.240)
0.570 (14.478)
0.550 (13.970)
0.520 (13.208)
0.160
(4.064)
MAX
2.040 (51.816) MAX
0.060 (1.524)
0.015 (0.381)
0.015 (0.381)
0.008 (0.2032)
0.160 (4.064)
0.100 (2.540)
0.110 (2.794)
0.090 (2.286)
0.060 (1.524)
0.045 (1.143)
0.023 (0.5842)
0.015 (0.3810)
0.680 (17.272)
0.610 (15.494)

40 LEAD CERDIP (JL)



0.540 (13.716)
0.160
(4.064)
MAX
2.040 (51.820)
0.025
(0.635)
TYP.
5°
TYP.
0.012 (0.305) TYP.
0.001 (0.025)
0.160
(4.064)
MIN.
0.660
(16.764)
MAX.
0.060 (1.524)
±0.020 (.51)
0.018 (0.457) TYP.
0.020 (0.508)
0.100
(2.540)

40 LEAD PLASTIC (PL)



0.590 ± 0.010
(15.00 ± 0.25)
0.050 ± 0.010
(1.27 ± 0.25)
2.400 ± 0.024
(60.96 ± 0.61)
0.085 ± 0.009
(2.16 ± 0.23)
0.175
(4.46)
0.010 +0.002 -0.001
(0.25 +0.05 -0.03)
0.610 ± 0.010
(15.49 ± 0.25)
0.100 ± 0.005
(2.54 ± 0.13)
0.018 ± 0.002
(0.46 ± 0.05)
TYP
0.050
(1.27) TYP

48 LEAD CERAMIC (DM)

100% INTEGRATED CIRCUIT PROCESSING

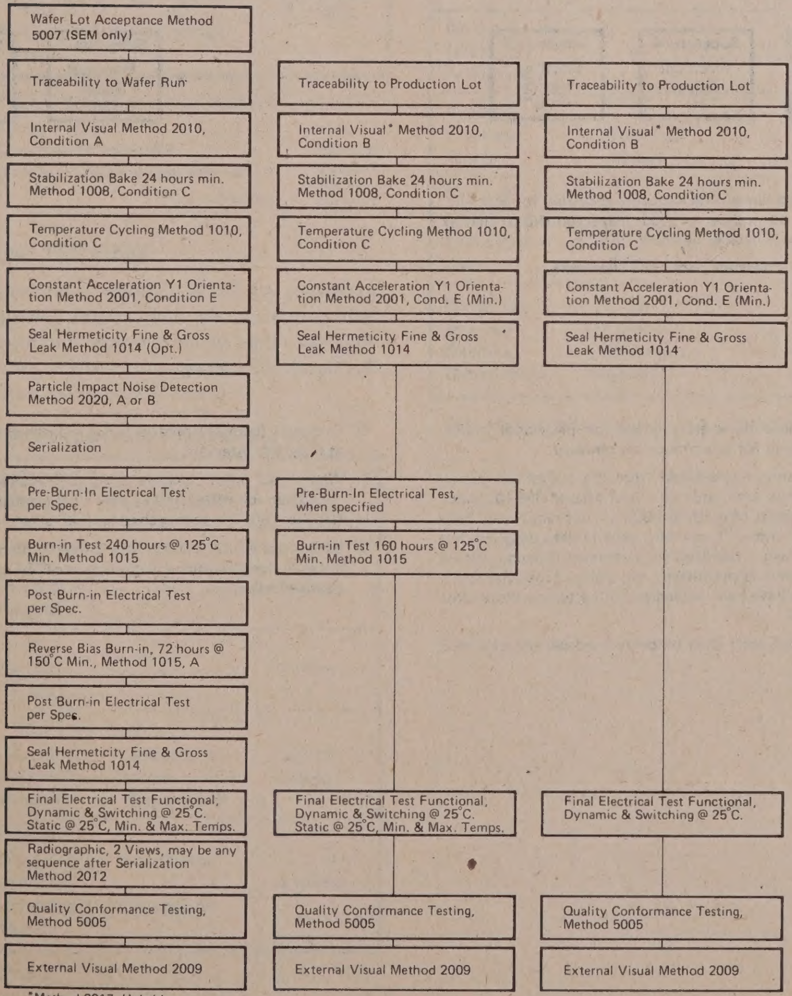
Intersil is committed to build and process integrated circuits for the Military/High-Rel market segments in conformance with MIL-STD-883 and MIL-M-38510. Any customer drawing which specifies testing as set forth in these documents will be automatically processed to the latest revisions of MIL-STD-883 and MIL-M-38510, unless specific requests are made to the contrary.

100% DISCRETE DEVICE PROCESSING

Intersil also offers several QPL-approved discrete products carrying the JANTX designation, which are screened and qualified to the latest revisions of MIL-STD-750 and MIL-S-19500.

MIL-STD-883B SCREENING AND QUALITY CONFORMANCE PROGRAMS, METHODS 5004 AND 5005

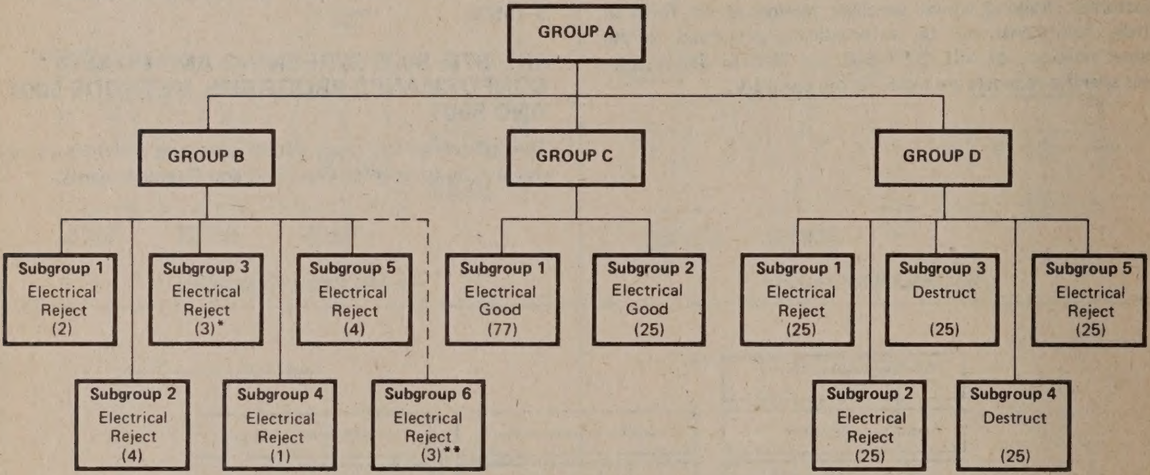
The following flow chart details screening activities as carried out by Intersil for Class S, B and C requirements.


Wafer Lot Acceptance Method 5007 (SEM only)
Traceability to Wafer Run
Internal Visual Method 2010, Condition A
Stabilization Bake 24 hours min. Method 1008, Condition C
Temperature Cycling Method 1010, Condition C
Constant Acceleration Y1 Orientation Method 2001, Condition E
Seal Hermeticity Fine & Gross Leak Method 1014 (Opt.)
Particle Impact Noise Detection Method 2020, A or B
Serialization
Pre-Burn-In Electrical Test per Spec.
Burn-in Test 240 hours @ 125°C Min. Method 1015
Post Burn-in Electrical Test per Spec.
Reverse Bias Burn-in, 72 hours @ 150°C Min., Method 1015, A
Post Burn-in Electrical Test per Spec.
Seal Hermeticity Fine & Gross Leak Method 1014
Final Electrical Test Functional, Dynamic & Switching @ 25°C. Static @ 25°C, Min. & Max. Temps.
Radiographic, 2 Views, may be any sequence after Serialization Method 2012
Quality Conformance Testing, Method 5005
External Visual Method 2009
Traceability to Production Lot
Internal Visual* Method 2010, Condition B
Stabilization Bake 24 hours min. Method 1008, Condition C
Temperature Cycling Method 1010, Condition C
Constant Acceleration Y1 Orientation Method 2001, Cond. E (Min.)
Seal Hermeticity Fine & Gross Leak Method 1014
Pre-Burn-In Electrical Test, when specified
Burn-in Test 160 hours @ 125°C Min. Method 1015
Final Electrical Test Functional, Dynamic & Switching @ 25°C. Static @ 25°C, Min. & Max. Temps.
Quality Conformance Testing, Method 5005
External Visual Method 2009
Traceability to Production Lot
Internal Visual* Method 2010, Condition B
Stabilization Bake 24 hours min. Method 1008, Condition C
Temperature Cycling Method 1010, Condition C
Constant Acceleration Y1 Orientation Method 2001, Cond. E (Min.)
Seal Hermeticity Fine & Gross Leak Method 1014
Final Electrical Test Functional, Dynamic & Switching @ 25°C.
Quality Conformance Testing, Method 5005
External Visual Method 2009

*Method 2017, Hybrid

QUALITY CONFORMANCE INSPECTION, CLASSES B AND C

The following diagram presents quality conformance inspection methods for Classes B and C as performed at Intersil.


GROUP A
GROUP B
GROUP C
GROUP D
Subgroup 1 Electrical Reject (2)
Subgroup 3 Electrical Reject (3)*
Subgroup 5 Electrical Reject (4)
Subgroup 2 Electrical Reject (4)
Subgroup 4 Electrical Reject (1)
Subgroup 6 Electrical Reject (3)**
Subgroup 1 Electrical Good (77)
Subgroup 2 Electrical Good (25)
Subgroup 1 Electrical Reject (25)
Subgroup 3 Destruct (25)
Subgroup 5 Electrical Reject (25)
Subgroup 2 Electrical Reject (25)
Subgroup 4 Destruct (25)

*Sample must have had temp/time exposure specified for burn-in. LTPD of 15 applies to number of leads inspected except that in no case shall less than 3 devices be used.

**Required only when a package contains a dessicant.

NOTES:

1. Group A and B inspections are required on individual inspection lots as a condition for acceptance for delivery.
2. Samples shall be randomly selected from the assembled inspection lot in accordance with appendix B of MIL-M-38510. Specified screen requirements of method 5004 are not required to have been completed for Intersil's standard generic data program, but will be performed when required by customer drawing. Where use of electrical rejects is permitted, and unless otherwise specified, they need not have been subjected to the temperature/time exposure of burn-in.
3. Group C (chip-related test) shall be performed periodically at 3 month intervals.
4. Group D (package related tests) shall be performed periodically at 6 month intervals.
5. Where end point measurements are required but no parameters have been identified, the critical final electrical parameters specified for 100% screening shall be used as end point measurements.
6. Subgroups within a group may be performed in any order but individual tests within a subgroup shall be performed in the sequence indicated.

QUALITY CONFORMANCE

The following steps are carried out when quality conformance testing is performed on a lot from which samples are taken.

QUALITY CONFORMANCE – CLASSES B & C

	STANDARD SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	45	0	3-5 days
Group B (Package Related)	14 Electrical Rejects	0	1 week
Group C (Die Related)	102 Good Electrical (Note 1)	1 from Subgroup 1 1 from Subgroup 2	8-10 weeks
Group D (Package Related)	50 Good Electrical (Note 2) 75 Electrical Rejects	1 from each of 5 Subgroups	4 weeks

NOTE 1: Non-destructive, shippable samples (102 units).

NOTE 2: Destructive tests:

Moisture resistance. Subgroup 3 sample size	25 units
Variable-frequency vibration. Subgroup 4 sample size	25 units
Total Destroyed	50 units

QUALIFICATION TESTING

When qualification testing is required, it will be equivalent to quality conformance testing, with the exception that Group A must be read and recorded on all applicable subgroups for the number of electrically-good units which will be required for samples for Groups C and D.

QUALIFICATION TESTING – GROUPS B & C

	STANDARD SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	184 (Read & Record)	5	5 days
Group B (Package Related)	14 Electrical Rejects	0	1 week
Group C (Die Related)	102 Good Electrical (Note 1)	1 from Subgroup 1 1 from Subgroup 2	10-12 weeks
Group D (Package Related)	50 Good Electrical (Note 2) 75 Electrical Rejects	1 from each of 5 Subgroups	4 weeks

NOTE 1: Shippable samples.

NOTE 2: 50 destroyed samples, subgroups 3 and 4.

LIMITED USAGE QUALIFICATION

A customer may elect to take advantage of a "Limited Usage" qualification per MIL-M-38510, in order to reduce the number of samples required. The following conditions must be met for eligibility for the "Limited Usage" qualification:

1. A maximum quantity of 500 microcircuits is included in a single order.
2. A maximum quantity of 2000 microcircuits is included in a given equipment-acquisition contract or program.
3. A maximum quantity of 2000 microcircuits is to be procured during a 12-month period for a given circuit type and vendor.

Microcircuits which qualify for limited usage cannot be assigned a JAN part number. Variable data will be taken only when specified in a customer drawing.

LIMITED USAGE QUALIFICATION – CLASS B(1)

	SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	45	0	5 days
Group B (Package Related)	14 Electrical Rejects	0	1 week
Group C (Die Related, Non-Destructive)	10 Good Electrical Parts	0	8-10 weeks
Group D (Package Related, Destructive)	25 (15 Good, 10 Electrical Rejects)	0	4 weeks

(1) Mil-M-38510, Paragraph 4.4.4; MIL-STD-883, Method 5005.

GLOSSARY OF MILITARY/AEROSPACE HIGH-REL DEFINITIONS/TERMINOLOGY

ACCELERATED BURN-IN – Same as "Burn-In", except that testing is carried out at an increased temperature (nominally 150° C) for reduced dwell time. Accelerated testing is not permissible for Class S devices.

ATTRIBUTES DATA – Go-No-Go data. Strictly pass/fail and number of rejects recorded. A typical requirement for post burn-in electrical tests on Class B devices.

BASELINE – Technique used to define manufacturing and test processes at time of order placement. Baselining usually involves development of a Program Plan and an Acceptance Test Plan which include flow charts, specification identification/revision letters, QA procedures, and actual specimens of certain important specifications. During subsequent manufacture and testing of parts, it is not permissible to make revisions or changes to any of the identified specifications, unless prior notification and possible customer approval occurs. Other terminology associated with baselining include "Critical Process Changes", "Minor Process Changes", and "Major Process Changes".

BURN-IN – A screening operation. Devices are subjected to high temperature (typically 125° C) and normal power/operation for 160 hours (Class B devices) or 240 hours (Class S devices).

CLASS S, B AND C INTEGRATED CIRCUITS – These classes set forth the screening, sampling and document control requirements for IC testing. Terminology is defined in MIL-M-38510 and in Test Methods 5004 and 5005 of MIL-M-38510. Classes, S, B and C are sometimes referred to as "Levels S, B and C." The Classes cover:

CLASS S – For space and satellite programs. Includes Condition A Precap, SEM, 240 hour burn-in, PIND test and elaborate qualification and quality conformance testing. Normally requires extensive data, documentation, and program planning. Formerly referred to as Class A. Class S devices are quite expensive.

CLASS B – For manned flight, and includes most frequently-procured military integrated circuits. Used for all but highest reliability requirements. Class B uses burn-in, pre-cap visual, etc.

CLASS C – For ground support equipment. Contains only environmental screening requirements with pre-cap visual. No burn-in required.

In all classes, LTPD (Lot Tolerance Percent Defective) is the sampling plan measurement criteria.

CORRECTIVE ACTION – Those actions which a given supplier (or user) agrees to perform so that a detected problem does not reoccur.

DESC – Defense Electronic Supply Center, located in Dayton, Ohio. The command includes two major subgroups, with functions as follows:

DESC-ECS – This group performs specification engineering work. After the original specifications are created at RADC, DESC-ECS implements and monitors the specifications. DESC-ECS is the industry's main interface on existing specifications.

DESC-EQM – The group which supervises supplier certifications and qualifications per MIL-M-38510. The group to which the industry submits applications when desiring to have devices qualified (QPL'd) on an existing JAN slash sheet. DESC-EQM surveys supplier facilities and grants line certification as various requirements are met. Also reviews manufacturer's qualification test data and issues JAN QPL's accordingly.

DESC-EQT – Same as EQM, except handles transistors per MIL-S-19500.

DESC LINE CERTIFICATION – The document which approves a supplier's facilities as an appropriate site to manufacture JAN parts.

DIE SHEAR TESTS – A sample test. Mounted chips are exercised to destruction. Degree of die adherence to lead frame is observed. Corrective action taken if required.

DPA – Destructive Physical Analysis. Finished products are opened and analyzed, in accordance with customer or MIL Spec criteria.

GENERIC DATA – Data pertaining to a device family; not necessarily the specific part number ordered by the customer, but representative of parts in the family. Group B, C and D generic data is frequently requested in lieu of the performance of special qual tests on a given order.

GROUP A – Sample electrical tests which are performed on each lot. Group A is defined in Test Method 5005 for integrated circuits and in MIL-S-19500 for diodes and transistors.

GROUP B – A collection of package-related environmental and "wear-and-tear" tests. Defined in Test Method 5005 for integrated circuits. For Class S screening, additional life tests are required, and are performed on every lot per MIL-M-38510. For diodes and transistors, Group B consists of both environmental and life tests, as defined in MIL-S-19500.

GROUP C – For Class B and C integrated circuits, only Group C includes life testing and temperature cycling/constant acceleration die-related sample tests. Defined in Test Method 5005 and performed every three months per MIL-M-38510.

GROUP D – A collection of additional environmental package-related sample tests as defined in Test Method 5005. Performed every six months per MIL-M-38510. For classes S, B, & C.

JAN — "Joint Army Navy", a registered trademark of the U.S. Government. The JAN marking denotes a device which is in full compliance to MIL-M-38510 or MIL-S-19500.

JAN TX — A JAN-qualified diode or transistor which has been subjected to additional screening (burn-in) tests. MIL-S-19500 only.

JAN TXV — A JAN-qualified diode or transistor which, in additional to burn-in testing, has been subjected to additional screening including pre-cap visual inspection, as witnessed by a government source inspector. Equivalent to Class B screening for integrated circuits. MIL-S-19500 only.

"M38510" CIRCUITS — Until a recent revision to MIL-M-38510, it was a common practice for users and suppliers alike to specify or offer integrated circuits marked "M38510/XXX" without a J or JAN prefix. This part numbering system indicated a device which was "near-JAN", "quasi-JAN" or "non-JAN". The practice tended to cause confusion between these devices and parts in full conformance to JAN levels. MIL-M-38510 now prohibits such marking with the exception of two special instances:

- When JAN QPL supplier for a given product does not exist, the government will permit "M38510/XXX" marking. While a customer may specify such marking, the supplier must furnish the government with evidence that the parts meet all applicable requirements.
- For certain parts destined for use in some programs, "M38510/XXX" marking is permissible, but orders for such parts must be accompanied by appropriate DESC certification letter.

M38510/XXX — Detail specifications (or "slash sheets") for integrated circuits. For example, the 101 specification covers Operational Amplifiers, with electrical requirements for the 741, LM101, 108, 747 types, etc.

MIL-M-38510 — The general military specification for integrated circuits.

MIL-S-19500 — The general military specifications for diodes and transistors.

MIL-S-19500/XXX — Detail specifications (or "slash sheets" for diodes and transistors.

MIL-STD-750 — Specifies Test Methods for diodes and transistors, such as burn-in, pre-cap, temperature cycling, etc.

MIL-STD-883 — Specifies Test Methods for integrated circuits, such as pre-cap, burn-in, hermeticity, storage life, etc.

NPFC — Naval Publications and Forms Center, Philadelphia. Printing and distribution source for military specifications.

NON-STANDARD PARTS — In government terminology, refers to non-JAN devices. Non-standard parts are typically covered by user Source Control Drawings (SCD).

NON-STANDARD PARTS APPROVAL — Approval by the government (frequently RADC) of non-JAN parts, typically on source control drawings, for use in a military system or program. This approval is essentially a waiver which permits non-JAN 38510 parts in a system which otherwise mandatorially requires JAN parts only.

OPERATING LIFE TEST — Same conditions as burn-in, but duration is usually 1000 hours. This is a sample test (Qualification and Quality Conformance).

PCA — Parts Configuration Analysis. A new term which has much the same meaning as "Baseline".

PDA — Percent Defective Allowable. Criteria sometimes applied to burn-in screening. A 10% PDA (the most common type) means that if more than 10% of that lot fails as a result of burn-in (as determined by pre- and post-burn-in electrical tests) the entire lot is considered to have failed.

PDS — Parameter Drift Screening. Measures the changes (Δs) in electrical parameters through burn-in. Common for Class S devices.

PIND — Particle Impact Noise Detection. This is an audio screening test to locate and elminate those parts which have loose internal particles. The test can isolate a high percentage of defectives, even in otherwise good lots. Repeatability of the tests is questionable. This test is one of the screening items for Class S integrated circuits.

PREPARING ACTIVITY — The organizational element of the government which writes specifications, frequently RADC.

PRESEAL VISUAL — A screening inspection which involves observation of a die through a microscope.

PROCURING ACTIVITY — Per MIL-M-38510, this is the organizational element in the government which contracts for articles or services. The Procuring Activity can be a subcontractor (OEM), providing that the government delegates this responsibility. In such a case, the subcontractor does not have the power to grant waivers, unless this authority has been approved by the government.

PRODUCT RELIABLIITY — Pertains to the level of quality of a product over a period of time. Reliability is usually measured or expressed in terms of Failure Rate (such as "0.002% per 1000 hours at a 60% confidence level at 25°C") or MTBF (mean time between failure in hours). MTBF is the reciprocal of Failure Rate.

QPL — Qualified Products List. In the case of JAN products, QPLs are identified as QPL-38510 for integrated circuits and QPL-19500 for diodes and transistors. QPL-38510 revisions occur approximately quarterly and QPL-19500 revisions occur approximately annually. In the interim, the government will notify suppliers via letter of any new device qualifications which may have been granted. Two types of QPLs exist for MIL-M-38510:

PART II QPL — This is an interim or temporary QPL which is granted on the basis of having obtained line certification and approval of an Application to Conduct Qualification Testing. A PART II QPL is automatically voided after 90 days whenever any one supplier is granted a PART I QPL.

PART I QPL — A "permanent" QPL, granted after all qualification testing is completed and test data is approved by the government.

QPLTT — Qualified Product List Throughput Time. That period which required to obtain device qualification. QPLTT is a function of (1) whether a JAN slash sheet exists; (2) whether a competitor already holds a Part I QPL; and (3) whether the applicant's production line is certified by DESC.

Following is a worst-case example, where a JAN slash sheet does not exist and government line certification has not been granted. QPLTT will be approximately 39.5 months, if the JAN slash sheet already exists, QPLTT will be cut to about 10.5 months. If the applicant already has line certification, QPLTT will be about 2 months to obtain Part II status.

Total time required to obtain a Part I QPL adds about 7 months to QPLTT; in a worst-case example, about 46 months will be required.

QUALIFYING ACTIVITY — Per MIL-M-38510, the organizational element in the government which designates certification (i.e., DESC).

QUALIFICATION TESTING — Initial one-time sample tests which are performed to determine whether device types and processes are good. For integrated circuits, this usually means testing to Groups A, B, C and D. For diodes and transistors, this usually means testing to Groups A, B and C.

QUALITY CONFORMANCE TESTING — These are sample tests which must be performed at prescribed intervals per MIL-M-38510 or MIL-S-19500, assuring that processes remain in control and that individual lots are passed.

B

RADC — Rome Air Development Command, Griffiss AFB, New York. This is the government organization which created semiconductor specifications; MIL-M-38510 and MIL-STD-883 were developed at RADC. This Air Force unit develops specifications for all U.S. military services. RADC is frequently involved in granting waivers for non-standard parts for Air Force systems.

READ AND RECORD DATA — Same as variable data.

REWORK PROVISION — For semiconductor devices, permissible rework of parts is usually limited to re-testing (screening), lead straightening or bending, re-marking, and cleaning.

S & V — Survivability and Vulnerability. Pertains to the ability of a device to resist radiation dosage.

SCREENING — Operations which are performed on devices on a 100% basis (not sampling). Examples include pre-cap visual, burn-in hermeticity, 100% electrical test, etc. For integrated circuits, Test Method 5004 defines screening flow.

SEM INSPECTION — Inspection by Scanning Electron Microscope. Die samples are examined at very high magnification for metallization defects. A common inspection for Class S devices.

SERIALIZATION — The marking of a unique part number on each part, with assigned numbers marked sequentially/consecutively.

SCDs — Source Control Drawings. Typically user-generated drawings which require development of internal IC vendor sheets. Although each drawing may be slightly different, all will be modelled around MIL-M-38510, MIL-S-19500, MIL-STD-883, or MIL-STD-750.

SOURCE INSPECTION — Can be either Customer Source Inspection (CSI) or Government Source Inspection (GSI). Source Inspection is initiated via purchase order, and can occur at one or more of the following points:

- Pre-cap Visual. Expensive and adds to throughput time.
- Final Inspection. Simple and inexpensive; little delivery impact.
- Throughout. Very expensive and time-consuming.

STANDARD PARTS — In government terminology, JAN parts.

TRACEABILITY — A production and manufacturing control system which includes:

- Wafer run identification number.
- Date pre-cap visual inspection was performed, identity of inspector, and specification number and revision.
- Lot number and inspection history.
- QA Group A electrical results.

VARIABLE DATA — Read and recorded electrical measurements (parametric values). Usually required for pre- and post-burn-in electrical tests. Also common for Group C and D testing.

WIRE PULL TESTS — Bond wire pull tests will be specified in two modes:

DESTRUCTIVE WIRE PULL — Generally performed periodically in assembly on a sample basis. Wires are pulled to destruction and the break point force is recorded. Corrective action is taken as required.

NON-DESTRUCTIVE WIRE PULL — Option for class 5 microcircuits, wire bonds are pulled to a max of 70% of the preseal minimum bond strengths for the applicable material on 100% of the lot.

Ordering Information for MIL-STD-883B Processed Devices

The following Intersil devices are available as a standard with Class B screening per method 5004 of MIL-STD-883B. To order, add 833B after the device number as shown below.

Part Number

82HM141MJG/883B
82HM181MJG/883B
82HM191MJG/883B

AD550M-12/883B
AD550S/883B
AD550T/883B
AD550U/883B
AD590JH/883B
AD590KH/883B
AD590LH/883B
AD590MH/883B
AD7520SD/883B
AD7520TD/883B
AD7520UD/883B
AD7521SD/883B
AD7521TD/883B
AD7521UD/883B
AD7523SD/883B
AD7523TD/883B
AD7523UD/883B
AD7533SD/883B
AD7533TD/883B
AD7533UD/883B
AD7541SD/883B
AD7541TD/883B

D125AK/883B
D125AL/883B
D125AP/883B

DG126AK/883B
DG126AL/883B
DG126AP/883B
DG129AK/883B
DG129AL/883B
DG129AP/883B
DG133AK/883B
DG133AL/883B
DG133AP/883B
DG134AK/883B

Part Number

DG134AL/883B
DG134AP/883B
DG139AK/883B
DG139AL/883B
DG139AP/883B
DG140AK/883B
DG140AL/883B
DG140AP/883B
DG141AK/883B
DG141AL/883B
DG141AP/883B
DG142AK/883B
DG142AL/883B
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DG146AL/883B
DG146AP/883B
DG151AK/883B
DG151AL/883B
DG151AP/883B
DG152AK/883B
DG152AL/883B
DG152AP/883B
DG154AK/883B
DG154AL/883B
DG154AP/883B
DG161AK/883B
DG161AL/883B
DG161AP/883B
DG162AK/883B
DG162AL/883B
DG162AP/883B

Part Number

DG163AK/883B
DG163AL/883B
DG163AP/883B
DG164AK/883B
DG164AL/883B
DG164AP/883B
DG180AA/883B
DG180AK/883B
DG180AL/883B
DG180AP/883B
DG181AA/883B
DG181AK/883B
DG181AL/883B
DG181AP/883B
DG182AA/883B
DG182AK/883B
DG182AL/883B
DG182AP/883B
DG183AK/883B
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DG183AP/883B
DG184AK/883B
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DG185AK/883B
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DG186AA/883B
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DG187AA/883B
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DG187AP/883B
DG188AA/883B
DG188AK/883B
DG188AL/883B
DG188AP/883B
DG189AK/883B
DG189AL/883B

Part Number

DG189AP/883B
DG190AK/883B
DG190AL/883B
DG190AP/883B
DG191AK/883B
DG191AL/883B
DG191AP/883B
DGM182AA/883B
DGM182AK/883B
DGM182AL/883B
DGM182AP/883B
DGM185AK/883B
DGM185AL/883B
DGM185AP/883B
DGM188AA/883B
DGM188AK/883B
DGM188AL/883B
DGM188AP/883B
DGM191AK/883B
DGM191AL/883B
DGM191AP/883B

G118AK/883B
G118AL/883B
G118AP/883B

ICH8510MKA/883B
ICH8520MKA/883B
ICH8530MKA/883B

ICL7109MDL/883B
ICL8007AMTV/883B
ICL8007MTY/883B
ICL8013AMTZ/883B
ICL8013BMTZ/883B
ICL8013CMTZ/883B
ICL8018AMJD/883B
ICL8018AMXJD/883B
ICL8018MJD/883B
ICL8019AMJD/883B
ICL8019AMXJD/883B

Part Number

ICL8019MJD/883B
ICL8020AMJD/883B
ICL8020MJD/883B
ICL8021MTY/883B
ICL8022MFD/883B
ICL8022MJD/883B
ICL8023MJE/883B
ICL8038AMJD/883B
ICL8038BMJD/883B
ICL8211MTY/883B
ICL8212MTY/883B

IH5048MJE/883B
IH5049MJE/883B
IH5050MJE/883B
IH5051MJE/883B
IH5140MDE/883B
IH5140MFD/883B
IH5140MJE/883B
IH5141MDE/883B
IH5141MFD/883B
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IH5141MTW/883B
IH5142MDE/883B
IH5142MFD/883B
IH5142MJE/883B
IH5142MTW/883B
IH5143MDE/883B
IH5143MFD/883B
IH5143MJE/883B
IH5144MDE/883B
IH5144MFD/883B
IH5144MJE T /883B

Part Number

IH5144MTW/883B
IH5145MDE/883B
IH5145MFD/883B
IH5145MJE/883B

IM5600MFE/883B
IM5600MJE/883B
IM5603AMFE/883B
IM5603AMJE/883B
IM5604MFE/883B
IM5604MJE/883B
IM5610MFE/883B
IM5610MJE/883B
IM5623MFE/883B
IM5623MJE/883B
IM5624MFE/883B
IM5624MJE/883B
IM6100-1MDL/883B
IM6100AMDL/883B
IM6101-1MDL/883B
IM6101AMDL/883B
IM6102-1MDL/883B
IM6102AMDL/883B
IM6103-1MDL/883B
IM6103AMDL/883B
IM6312AMFN/883B
IM6312AMJN/883B
IM6312MFN/883B
IM6312MJN/883B
IM6402-1MDL/883B
IM6402AMDL/883B
IM6403-1MDL/883B
IM6403AMDL/883B

Part Number

IM6512AMFN/883B
IM6512AMJN/883B
IM6512MFN/883B
IM6512MJN/883B
IM65X08-1MFE/883B
IM65X08-1MJE/883B
IM65X08A-1MFE/883B
IM65X08A-1MJE/883B
IM65X08AMFE/883B
IM65X08AMJE/883B
IM65X08MFE/883B
IM65X08MJE/883B
IM65X18-1MFN/883B
IM65X18-1MJN/883B
IM65X18A-1MFN/883B
IM65X18A-1MJN/883B
IM65X18AMFN/883B
IM65X18AMJN/883B
IM65X18MFN/883B
IM65X18MJN/883B
IM65X51AMJF/883B
IM65X51MJF/883B
IM65X61AMFN/883B
IM65X61AMJN/883B
IM65X61MFN/883B
IM65X61MJN/883B

LM100H/883B
LM101AF/883B
LM101AH/883B
LM101H/883B
LM105H/883B
LM107F/883B

Part Number

LM107H/883B
LM107J-14/883B
LM108AH/883B
LM108H/883B
LM110F/883B
LM110H/883B
LM111H/883B
LM111J/883B
LM124J/883B
LM139AJ/883B
LM139J/883B

SE555F/883B
SE555T/883B
SE556F/883B

μA723DMQB
μA723HMQB
μA741DMQB
μA741FMQB
μA741HMQB

APPLICATION NOTE SUMMARY

The following are brief descriptions of current Intersil Application notes.

A003 **UNDERSTANDING AND APPLYING THE ANALOG SWITCH**

Introduces analog switches and compares them to relays. Describes CMOS, hybrid (FET + driver), J-FET "virtual ground" and J-FET "positive signal" types. Application information included.

A004 **IH5009 LOW COST ANALOG SWITCH SERIES**

Compares the members of the IH5009 "virtual ground" analog switches and provides suggested applications.

A005 **THE 8007–A HIGH PERFORMANCE FET INPUT OP AMP**

Compares the 8007 with the 741, which is pin compatible and suggests applications such as log-antilog amplifier, sample and hold circuit, photometer, peak detector, etc.

A006 **A NEW CMOS ANALOG GATE TECHNOLOGY**

Introduces Intersil's "Floating Body" process for manufacturing CMOS analog gate and multiplexer devices. This process virtually eliminates destructive latch up.

A007 **USING THE 8048/8049 MONOLITHIC LOG-ANTILOG AMPLIFIER**

Describes in detail the operation of the 8048 logarithmetic amplifier, and its counterpart, the 8049 antilog amp.

A011 **A PRECISION FOUR QUADRANT MULTIPLIER–THE 8013**

Describes, in detail, the operation of the 8013 analog multiplier. Included are multiplication, division, and square root applications.

A013 **EVERYTHING YOU ALWAYS WANTED TO KNOW ABOUT THE 8038**

This note includes 17 of the most asked questions regarding the use of the 8038.

A015 **DESIGN FOR A BATTERY OPERATED FREQUENCY COUNTER**

Describes a low cost battery operated frequency/period counter using the 7207A and 7208. Includes specifications, schematics, PC layout, etc.

A016 **SELECTING A/D CONVERTERS**

Describes the differences between integrating converters and successive approximation converters. Includes a checklist for decision making, and a note on multiplexed data systems.

A017 **THE INTEGRATING A/D CONVERTER**

Provides an explanation of integrating A/D converters, together with a detailed error analysis.

A018 **DO'S AND DONT'S OF APPLYING A/D CONVERTERS**

An analysis of proper design techniques using D/A converters.

A019 **4½ DIGIT PANEL METER DEMONSTRATION/ INSTRUMENTATION BOARDS**

Describes two typical PC board layouts using the 8052A/7103A 4½ digit A/D pair. Includes schematics, parts layout, list of materials, etc. Also see A028.

A020 **A COOKBOOK APPROACH TO HIGH SPEED DATA ACQUISITION AND MICROPROCESSOR INTERFACING**

Uses the building block approach to design a complete 12 volt system. Explains the significance of each component and demonstrates methods for microprocessor interfacing, including the use of control signals.

A021 **POWER D/A CONVERTERS USING THE ICH 8510**

Detailed analysis of the 8510. Included are a section describing the linearity of the device and application notes for driving servo motors, linear and rotary actuators, etc. Also see A026.

A022 **A NEW J-FET STRUCTURE–THE VARAFET**

Describes in detail the operation of the varafet, a standard J-FET with the analog gate interfacing components monolithically built-in.

A023 **LOW COST DIGITAL PANEL METER DESIGNS**

Provides a detailed explanation of the 7106 and 7107 3½ digit panel meter IC's, and describes two of the evaluation kits available from Intersil.

A026 **DC SERVO MOTOR SYSTEMS USING THE ICH8510**

This companion note to A021 explains the design techniques utilized in using the ICH8510 family to drive closed loop servo motor systems.

A027 **POWER SUPPLY DESIGN USING THE ICL-8211 AND ICL8212**

Explains the operation of the ICL8211/12 and describes various power supply configurations. Included are positive and negative voltage regulators, constant current source, programmable current source, current limiting, voltage crowbarring, power supply window detector, etc.

A028 **BUILDING AN AUTO RANGING DMM WITH THE ICL7103A/8052A CONVERTER PAIR**

This companion app note to A019 explains the use of the 8052A/7103A converter pair to build a ±4½ digit auto ranging digital multimeter. Included are schematics, circuit descriptions, tips and hints, etc.

A029 **POWER OP AMP HEAT SINK KIT**

Describes the heat sinks for the ICH8510 family. These heat sinks may be ordered from the factory.

A030 **THE ICL7104: A BINARY OUTPUT A/D CONVERTER FOR MICROPROCESSORS**

Describes in detail the operation of the 7104. Includes digital interfacing, handshake mode, buffer gain, auto-zero and external zero. Appendix includes detailed discussion of auto-zero loop residual errors in dual slope A/D conversion.

A031 **COIL DRIVE ALARM DESIGN CONSIDERATIONS**

Explains the procedure used when using watch circuits to drive piezoelectric transducers.

A032 **UNDERSTANDING THE AUTO-ZERO AND COMMON MODE PERFORMANCE OF THE ICL7106/7107/7109 FAMILY.**

Explains in detail the operation of the ICL7106/7/9 family of A/D Converters.

A033 **THE POWER MOSFET – A BREAKTHROUGH IN POWER DEVICE TECHNOLOGY**

Demonstrates differences in chip geometries and completely explains the significance of input and output parameters.

A034 **THE DESIGN OF SWITCHMODE CONVERTERS ABOVE 100 MHz**

Defines problems, compares circuit topologies, explains component performance at high frequencies and suggests design methods.

A035 **SWITCHMODE CONVERTER TOPOLOGIES – MAKE THEM WORK FOR YOU**

Compares buck, boost and DC transformer types, combinations of the three, and variations of each. Explains duality principle, bilateral inversion, and overlapping conduction. Includes design examples.

A037 **450 VOLT HIGH PERFORMANCE OFF LINE SWITCH MODE POWER SUPPLY**

Compares bipolar supplies and MOSFET supplies, explains design procedures and problems. Includes a complete schematic for a 5V, 50A supply.

A046 **BUILDING A BATTERY OPERATED AUTO RANGING DVM WITH THE ICL7106**

Explains principles of auto ranging, problems and solutions. Includes clock circuits, power supply requirements, design hints, schematics, etc.

M009 **DESIGNING LOW POWER 12-BIT MICROPROCESSOR SYSTEMS**

Explains effects of word length, architecture, and I/O structure on low power designs. Shows examples of typical circuits.

FET, MOSFET, AND DUAL TRANSISTOR CHIPS

INTRODUCTION

Intersil recognizes the increasing need for transistors and FETs in die form. To fulfill this need, Intersil offers a full line of JFETs, MOSFETs, and dual transistors in die form.

Die sales do, however, present some unique problems. In many cases the chips cannot be guaranteed to the same electrical specifications as the packaged part. This is due to the fact that leakage, noise, AC parameters and temperature testing cannot be tested to the same degree of accuracy for dice as it can for packaged devices. This is due to equipment limitations and handling problems.

PURCHASE OPTIONS

Intersil offers dice which are delivered in a number of forms:

- Chips which have been electrically probed, inked, visually inspected and diced.
- Wafers which have been electrically probed, inked, visually inspected and scribed only.
- Wafers which have been electrically probed, inked, and visually inspected only.

GENERAL PHYSICAL INFORMATION

- Consult individual product information sheets for dimensions. Except for the aluminum bonding pads, the chips are completely covered with vapox (silicon dioxide). This minimizes damage to the chip caused by handling problems.
- Dice are 100% tested to electrical specifications, then visually inspected. When wafers are ordered, dice which fail the electrical test are inked out.
- Generally the minimum size of the die-attaching pad metallization should be at least 5 mils larger (on every edge) than the chip dimensions. For example, a 15 mil chip should be attached on at least a 25 mil pad.

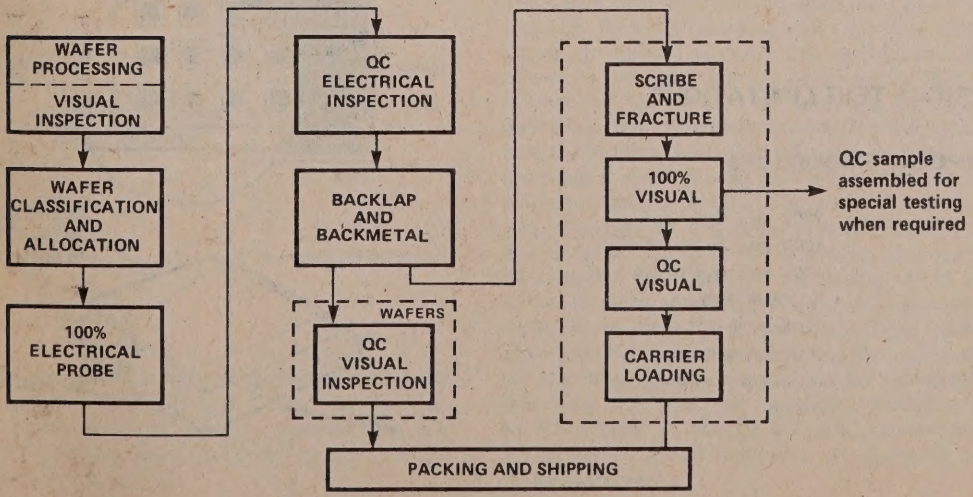
Small Signal Devices

- Chips are available with exact length X width dimensions plus tolerance (see individual data sheets). Chip height ranges from .003″ to .006″.
- To facilitate die attaching, chips are gold backed. Approximate thickness is 1000 angstroms. In general, dice should be attached to gold, platinum, or palladium metallization. Thin-film gold, moly-gold and most of the thick-film metallization materials are compatible.
- All chips have aluminum metallization and aluminum bonding pads. Typical aluminum thickness is 12,000 angstroms.

Power FETs

- Chip height ranges from .007″ to .020″.
- To facilitate die attaching, chips have gold or silver backing.
- Top side metal is aluminum with a thickness of 10,000 - 30,000 angstroms.

CHIP AND WAFER PROCESSING FLOW CHART


WAFER PROCESSING
VISUAL INSPECTION
WAFER CLASSIFICATION AND ALLOCATION
100% ELECTRICAL PROBE
QC ELECTRICAL INSPECTION
BACKLAP AND BACKMETAL
WAFERS
QC VISUAL INSPECTION
SCRIBE AND FRACTURE
100% VISUAL
QC VISUAL
CARRIER LOADING
QC sample assembled for special testing when required
PACKING AND SHIPPING

RECOMMENDED DICE ASSEMBLY PROCEDURE

CLEANING

Dice supplied in die form do not require cleaning prior to assembly. Dice supplied in wafer form should be cleaned after scribing and breaking. Freon TF in a vapor degreaser is the preferred cleaning method. However, an alternative is to boil the die in TCE for five minutes with a rinse in isopropyl alcohol for 1-2 minutes.

DIE ATTACH:

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidation. A preform should be used if the mounting surface has less than 50 microinches of gold and the die should be handled on the edges with tweezers. Die attach temperature should be between 385° C and 400° C with eutectic visible on three sides of the die after attachment.

BONDING:

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The gold ball should be about 3 times the diameter of the gold wire. The ball should cover the bonding pad, but not excessively, or it may short out surrounding metallization. 1-mil aluminum wire may be used on most dice, but should not be used if the assembled unit will be plastic encapsulated.

HANDLING OF DICE:

All dice shown in this catalog are passivated devices and Intersil warrants that they will meet or exceed published specifications when handled with the following precautions:

- Dice should be stored in a dry inert-gas atmosphere.
- Dice should be assembled using normal semiconductor techniques.
- Dice should be attached in a gaseous nitrogen spray at a temperature less than 430° C.

ELECTRICAL TEST LIMITATIONS

DUAL BIPOLAR TRANSISTORS

LV_{CEO}	100V max. @ ≤1 mA
BV_{CBO}	100V max. @ ≥1 µA
BV_{EBO}	100V max. @ ≤10 mA
h_{FE}	≤1000 @ ≥10 µA
$V_{CE(sat)}$	≥10 mV @ ≤10 mA
I_{CBO}	≥100 pA @ ≤100V
$V_{BE1}-V_{BE2}$	≥1 mV @ ≥10 µA
$I_{B1}-I_{B2}$	≥2 nA

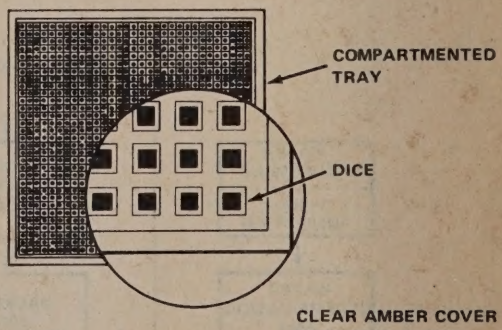
FETS

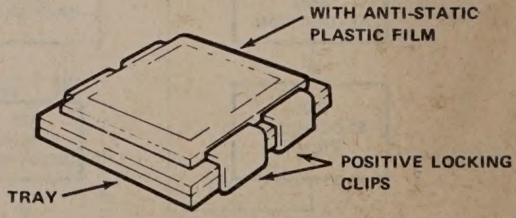
Breakdown voltage	100V max. @ 1 µA
Pinch-off voltage	0-20V @ ≥1 nA
$V_{GS(th)}$	0-20V @ ≥10 µA
$r_{DS(on)}$	20 Ω min. @ V_{GS} = 0 (V_{GS} = 30 MOSFETs)
I_{DSS} & I_{DSS}	100 mA max.
g_{fs}	10,000 µMHOS max. @ I_D ≤ 10 mA
$I_{D(off)}$, $I_{S(off)}$, I_{GSS}	100 pA min.
V_{GS1} - V_{GS2} (Duals)	10 mV min.

Electrical testing is guaranteed to a 10% LTPD. AC parameters such as capacitance and switching time cannot be tested in wafer or dice form.

STANDARD DIE CARRIER PACKAGE

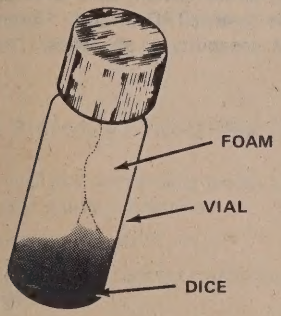
- Easy to handle, store and inventory.
- 100% electrically probed dice with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection — dice in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usuable in customer production area.
- Carrier may be storage container for unused dice.
- Carriers hold 25, 100, or 400 dice, depending on die size and quantity ordered.
- Part numbers shown in this catalog are for carrier packaging.





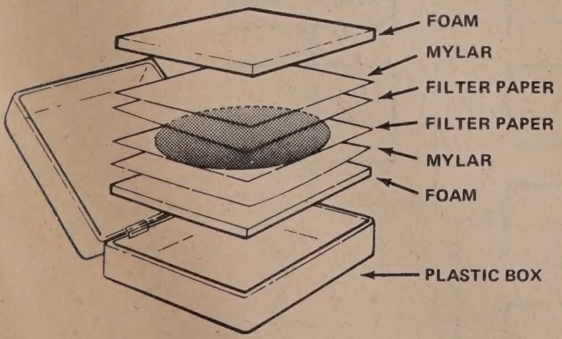
OPTIONAL VIAL PACKAGE

- 100% electrically probed dice with rejects inked but included in vial. Bulk shipment.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lower cost.
- For vial package – replace "D" in catalog number with "V", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/V (2N4416 dice in vial).



OPTIONAL WAFER PACKAGE

- 100% electrically probed – rejects inked.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lowest cost.
- Wafer is supplied unscribed.
- For wafer package – replace "D" in catalog number with "W", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/W (2N4416 dice in wafer).



NOTE:

Intersil reserves the right to improve device geometries and manufacturing processes as required. These improvements may result in slight geometry changes. However, they will not affect the electrical limits, basic pad layouts or maximum die sizes in this catalog.

ELECTRICAL TEST CAPABILITY

As an example of how to use the capability chart to see what Intersil actually guarantees and tests for, on a 100% basis, compare the 2N4391 in a TO-18 package to the 2N4391 delivered as a chip.

Electrical Test Spec.	2N4391 in a TO-18	2N4391 Chip
I_{GSS} @ 25C	100 pA max.	100 pA max.
BV_{GSS}	40V min.	40V min.
$I_{D(off)}$ @ 25C	100 pA max.	100 pA max.
$V_{GS(forward)}$	1V max.	See note 1
$V_{GS(off)}$ or V_P	4V to 10V	4V to 10V
I_{DSS}	50 to 150 mA	50 to 100 mA
$V_{DS(on)}$	0.4V max.	0.4V max.
$r_{DS(on)}$	30Ω max.	30Ω max.
C_{iss}	14 pF max.	Guaranteed by Design
C_{rss}	3.5 pF max.	Guaranteed by Design
t_d	15ns max.	Guaranteed by Design
t_r	5ns max.	Guaranteed by Design
t_{off}	20ns max.	Guaranteed by Design
t_f	15 ns max.	Guaranteed by Design

NOTE 1: This parameter is very dependent upon quality of metallization surface to which chip is attached.

SUMMARY

Of the 14 items specified for the package part, only 7 can be tested and guaranteed in die form. It is to be noted that those specifications which cannot be tested in die form can be sample tested in package form as an indicator of lot performance. Many of the tests, however, such as capacitance tests, are design parameters.

The above electrical testing is guaranteed to a 10% LTPD. However, there are occasions where customer requirements cannot be satisfied by wafer sort testing alone. While the previously described tests will be done on a 100% basis, Intersil recognizes the need for additional testing to obtain confidence that a particular customer's needs can be met with a reasonably high yield. Toward this end Intersil has instituted a dice sampling plan which is two-fold. First, random samples of the dice are packaged and tested to assure adherence to the electrical specification. When required, wafers are identified and wafer identity is tied to the samples. This tests both the electrical character of the die and its ability to perform electrically after going through the high temperature dice attachment stage. Second, more severe testing can be performed on the packaged devices per individual customer needs. When testing is required other than that called out in the data sheet, Intersil issues an ITS number to describe the part. Examples of tighter testing which can be performed on packaged samples is shown as follows:

CHIP ORDERING INFORMATION

FET & DUAL FET PAIRS

1. Leakages to 1 pA (I_{GSS})
2. $r_{DS\ (on)}$ to as low as 4 ohms
3. $I_{D\ (off)}$ to 10 pA
4. I_{DSS} to 1 amp (pulsed)
5. g_{fs} to 10,000 µmho
6. g_{os} to 1 µmho
7. e_n noise to 5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz to 100 Hz.
8. CMRR to 100 dB
9. $\Delta(V_{GS1}-V_{GS2})/\Delta T$ down to 10µV/°C to an LTPD of 20%
10. g_m match to 5%
11. I_{DSS} match to 5%

TRANSISTOR PAIRS

1. Leakages to as low as 1 pA
2. Beta with collector current up to 50 mA and as low as 100 nA
3. f_T up to 500 MHz with collector currents in the range of 10 µA to 10 mA
4. Noise measurements as low as 5 nV/$\sqrt{Hz}$ from 10 Hz to 100 kHz
5. $\Delta(V_{BE1}-V_{BE2})/\Delta T$ to 10µV/°C to an LTPD of 20%

VISUAL INSPECTION

Individual chips are 100% inspected to MIL-STD-750, Method 2072 or, as an option, MIL-STD-883, Level B. Inspection is done to an LTPD of 20%. As an option, Intersil offers S.E.M. capability on all wafers.

CMOS INTEGRATED CIRCUIT CHIPS

INTRODUCTION

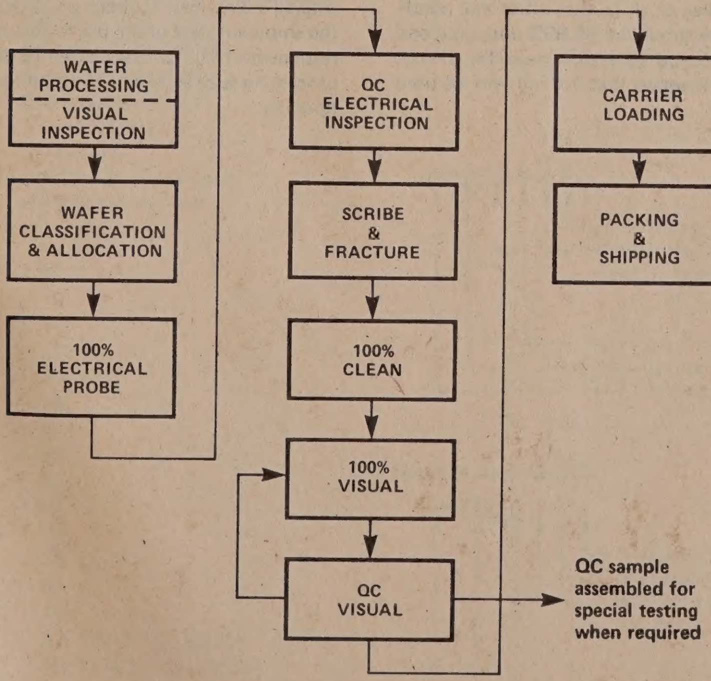
In addition to discrete device chips, Intersil also offers a full line of metal gate CMOS integrated circuits in die form. Die sales, however, present some unique problems. In many cases, chips cannot be guaranteed to the same electrical specifications as can the packaged parts. This is because leakage, noise, AC parameters and temperature testing cannot be guaranteed to the same degree of accuracy for dice as for packaged devices.

GENERAL PHYSICAL INFORMATION

- Chips are available with precise length and width dimensions, ±2 mils in either dimension.
- Chip thickness is 15 mils ±1 mil.
- Bonding pad and interconnect material is aluminum, 10K to 15K Å thick.
- Each die surface is protected by planar passivation and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by an HF etchant; bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.
- Dice are 100% inspected to electrical specifications, then visually inspected according to MIL-STD-883, Method 2010.2, Condition B, with modifications reflecting CMOS requirements.
- Bonding pad dimensions are 4.0 x 4.0 mils minimum.
- Storage temperature is -40°C to +150°C.
- Operating temperature is -20°C to +70°C.
- Guaranteed AQL Levels:

Visual	2.0%
Functional electrical testing	1.0%
Parametric DC testing	4.0%
Untested parameters	10.0%

CMOS INTEGRATED CIRCUIT CHIP PROCESSING FLOW CHART


WAFER PROCESSING
VISUAL INSPECTION
WAFER CLASSIFICATION & ALLOCATION
100% ELECTRICAL PROBE
QC ELECTRICAL INSPECTION
SCRIBE & FRACTURE
100% CLEAN
100% VISUAL
QC VISUAL
CARRIER LOADING
PACKING & SHIPPING
QC sample assembled for special testing when required

RECOMMENDED DICE ASSEMBLY PROCEDURES

CLEANING

Dice supplied in die form do not require cleaning prior to assembly. However, if cleaning is desired, dice should be subjected to freon TF in a vapor degreaser and then vapor-dried.

RECOMMENDED HANDLING

Intersil recommends that dice be stored in the vacuum-sealed plastic bags which hold the dice carriers. Once removed from the sealed bags, the dice should be stored in a dry, inert-gas atmosphere.

Extreme care should be used when handling dice. Both electrical and visual damage can occur as the result of an unclean environment or harsh handling techniques.

DIE ATTACH

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidization. If a eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C. If hermetic packages are used, epoxy die attach should be carried out with caution so that there will be no "outgassing" of the epoxy.

BONDING

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The wire should be 99.99% pure gold and the aluminum wire should be 99% aluminum/1% silicon. In either case, it is recommended that 1.0 mil wire be used for normal power circuits.

STANDARD DIE CARRIER PACKAGE

- Easy to handle, store and inventory.
- 100% electrically probed with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection — dice are in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usable in customer production area.
- Carrier may be used as storage contained for unused dice.
- Carriers hold 25, 100 or 400 dice, depending on die size and quantity ordered.
- Packaging of integrated circuit dice in carriers is identical to illustration shown earlier for discrete device, except that IC chips are not available in vial packs or in wafer form.

CHANGES

Intersil reserves the right in improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect dice electrical limits, pad layouts, or maximum die sizes.

USER RESPONSIBILITY

Written notification of any non-conformance by Intersil of Intersil's dice specifications must be made within 75 days of the shipment date of the die to the user. Intersil assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

PART NUMBERING SYSTEM

Examples of Intersil Part Numbers

BASIC	ELECTRICAL OPTION	TEMP	PKG	PIN	
ICH8500	A	C	T	V	ICH8500ACTV
ICL8038	C	C	P	D	ICL8038CCPD
IH5040		M	D	E	IH5040MDE

ON ALL INTERSIL IC PART NUMBERS. THE LAST THREE LETTERS ARE TEMPERATURE, PACKAGE, AND PIN NUMBER, RESPECTIVELY.

TEMPERATURE:
C — Commercial
I — Industrial
M — Military

PACKAGE:
B — Plastic Flatpak (minipak)
D — Ceramic Dual-In-Line
E — Small TO-8 Type
F — Ceramic Flatpak
I — 16 Pin Dip (0.6 X 0.7) Lead Space
J — Cerdip Dual-In-Line
K — 8 Lead TO-3 Metal Can
L — Leadless, Ceramic
P — Epoxy Dual-In-Line
Q — 2 Lead Metal Can
T — TO-5 Type
DR — TO-72 with No. 4 Lead Connected to Case

NUMBER OF PINS:
A — 8
B — 10
C — 12
D — 14
E — 16
N — 18
P — 20
F — 22
G — 24
I — 28
J — 32
K — 36
L — 40
M — 48
V — 8, 0.230 in. Pin Circle
W — 10, 0.230 in. Pin Circle
Y — 8, Pin 4 Connected to Case
Z — 10, Pin 5 Connected to Case

LINEAR:

ICL 8038 C C P D

D — Number of Pins
P — Package
C — Temperature Range:
M — -55°C to +125°C
I — -20°C to + 85°C
C — 0°C to + 70°C
C — Electrical Option
8038 — Device Chip Type
ICL — Intersil Linear Circuit

HYBRIDS:

DG 126 A L

L — Package:
A — Metal Can
L — Flat pack
P — Ceramic
A — Temperature Range:
A — -55°C to +125°C
B — -20°C to + 85°C
C — 0°C to + 70°C
126 — Device Chip Type
DG — Device Family
DG — Drivers
D — Drivers
G — Multi-channel FET

IH 5043 B M F D

D — Number of Pins
F — Package
M — Temperature Range:
M — -55°C to +125°C
C — 0°C to + 70°C
B — Electrical Option
5043 — Device Chip Type
IH — Intersil Hybrid/Analog Gate

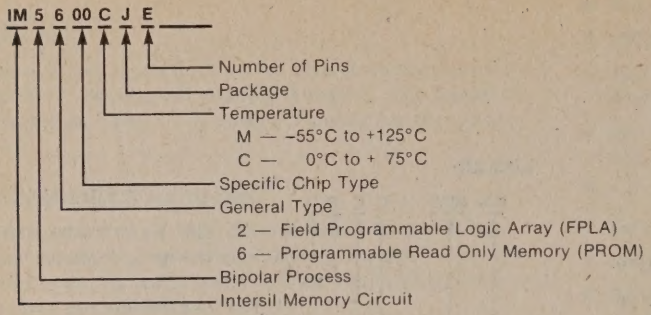
WATCH AND CLOCK:

ICM 7045 A I P I

I — Number of Pins
P — Package
I — Temperature Range:
M — -55°C to +125°C
I — -20°C to + 70°C
C — 0°C to + 70°C
A — Electrical Option
7045 — Device Chip Type
ICM — Intersil Watch and Clock Circuit

PART NUMBERS AND ORDER INFORMATION

BIPOLAR MEMORY:



IM 5 6 00 C J E

Number of Pins

Package

Temperature

M — −55°C to +125°C

C — 0°C to + 75°C

Specific Chip Type

General Type

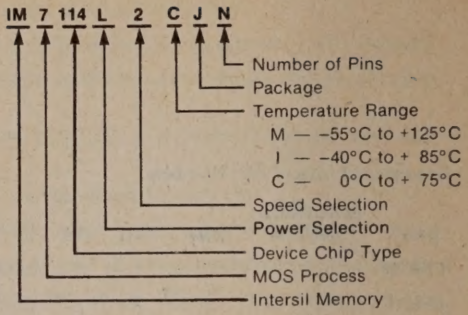
2 — Field Programmable Logic Array (FPLA)

6 — Programmable Read Only Memory (PROM)

Bipolar Process

Intersil Memory Circuit

MOS MEMORY:



IM 7 114 L 2 C J N

Number of Pins

Package

Temperature Range

M — −55°C to +125°C

I — −40°C to + 85°C

C — 0°C to + 75°C

Speed Selection

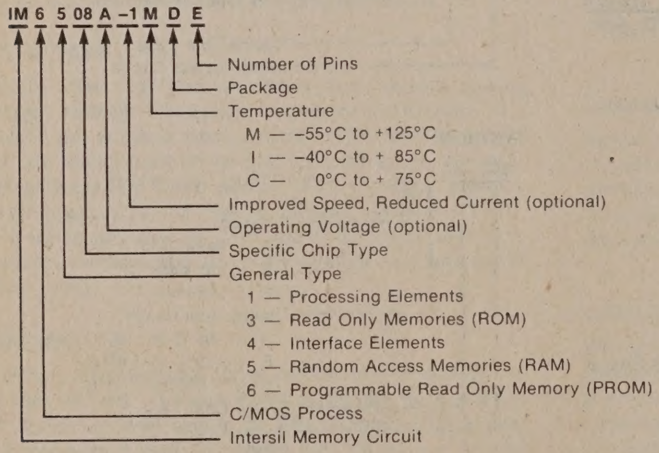
Power Selection

Device Chip Type

MOS Process

Intersil Memory

C/MOS MEMORY:



IM 6 5 08 A −1 M D E

Number of Pins

Package

Temperature

M — −55°C to +125°C

I — −40°C to + 85°C

C — 0°C to + 75°C

Improved Speed, Reduced Current (optional)

Operating Voltage (optional)

Specific Chip Type

General Type

1 — Processing Elements

3 — Read Only Memories (ROM)

4 — Interface Elements

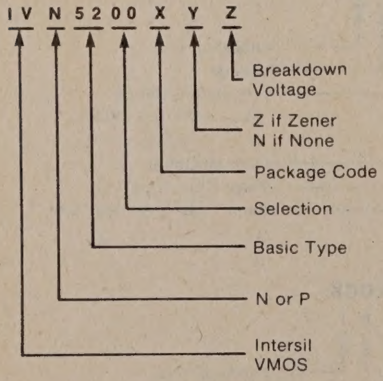
5 — Random Access Memories (RAM)

6 — Programmable Read Only Memory (PROM)

C/MOS Process

Intersil Memory Circuit

VERTICAL POWER MOSFET PART NUMBERING (PROPRIETARY PARTS)



I V N 5 2 0 0 X Y Z

Breakdown Voltage

Z if Zener
N if None

Package Code

Selection

Basic Type

N or P

Intersil VMOS

B

BREAKDOWN VOLTAGE

A	20
B	30
C	35
D	40
E	60
F	80
G	90
H	100
J	125
K	150
L	175
M	200
N	225
P	250
Q	300
R	350
S	400
T	450
U	500

PACKAGE CODES

TO-237 (92+)	A
TO-202	B
TO-220	C
DICE	D
TO-66	H
TO-3	K
TO-52	S
TO-39	T

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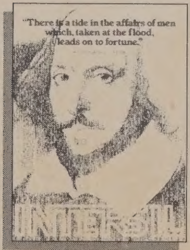
"There is a tide in the affairs of men which, taken at the flood, leads on to fortune."
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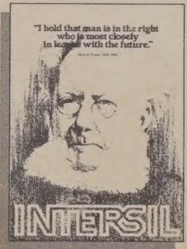
"I hold that man is in the right who is most closely in league with the future."
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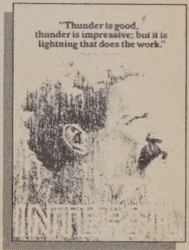
"Thunder is good, thunder is impressive; but it is lightning that does the work."
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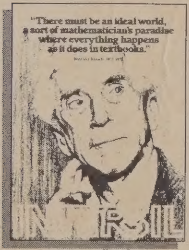
"There must be an ideal world, a sort of mathematician's paradise where everything happens as it does in textbooks."
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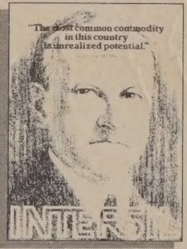
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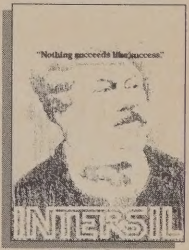
"Nothing succeeds like success."
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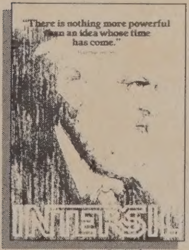
"There is nothing more powerful than an idea whose time has come."
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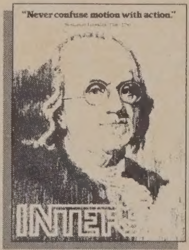
"Never confuse motion with action."
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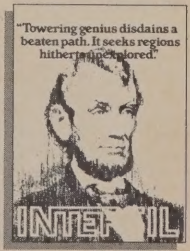
"Towering genius disdains a beaten path. It seeks regions hitherto unexplored."
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